

## AD8613/AD8617/AD8619

### FEATURES

- Offset voltage: 2.2 mV maximum**
- Low input bias current: 1 pA maximum**
- Single-supply operation: 1.8 V to 5 V**
- Low noise: 22 nV/ $\sqrt{\text{Hz}}$**
- Micropower: 50  $\mu\text{A}$ /amplifier maximum over temperature**
- No phase reversal**
- Unity gain stable**
- Qualified for automotive applications**

### APPLICATIONS

- Battery-powered instrumentation**
- Multipole filters**
- Current shunt sense**
- Sensors**
- ADC predrivers**
- DAC drivers/level shifters**
- Low power ASIC input or output amplifiers**

### GENERAL DESCRIPTION

The AD8613/AD8617/AD8619 are single, dual, and quad micro-power, rail-to-rail input and output amplifiers that feature low supply current, as well as low input voltage and current noise.

The parts are fully specified to operate from 1.8 V to 5 V single supply, or  $\pm 0.9$  V and  $\pm 2.5$  V dual supply. The combination of low noise, very low input bias currents, and low power consumption make the AD8613/AD8617/AD8619 especially useful in portable and loop-powered instrumentation.

The ability to swing rail-to-rail at both the input and output enables designers to buffer CMOS ADCs, DACs, ASICs, and other wide output swing devices in low power, single-supply systems.

The AD8613 is available in a 5-lead SC70 package and a 5-lead TSOT-23 package. The AD8617 is available in 8-lead MSOP, 8-lead SOIC, and 8-lead LFCSP packages. The AD8619 is available in 14-lead TSSOP and 14-lead SOIC packages. The AD8617W is qualified for automotive applications and is available in an 8-lead MSOP package and an 8-lead SOIC package.

### PIN CONFIGURATIONS

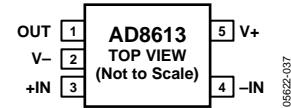


Figure 1. 5-Lead SC70 and 5-Lead TSOT-23

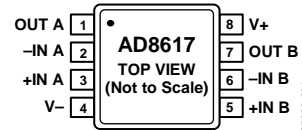
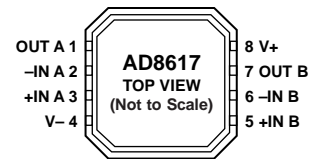


Figure 2. 8-Lead MSOP and 8-Lead SOIC\_N



#### NOTES

1. PIN 4 AND THE EXPOSED PAD MUST BE CONNECTED TO V-.

Figure 3. 8-Lead LFCSP\_VD

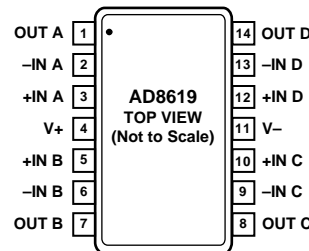


Figure 4. 14-Lead TSSOP

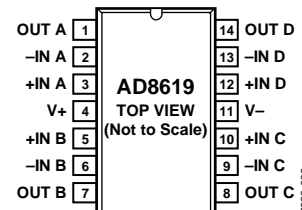


Figure 5. 14-Lead SOIC\_N

#### Rev. E

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## REVISION HISTORY

### 3/10—Rev. D to Rev. E

Changes to General Description .....	1
Changes to Ordering Guide .....	15

### 3/10—Rev. C to Rev. D

Changes to General Description .....	1
Changes to Ordering Guide .....	15

### 10/09—Rev. B to Rev. C

Added 8-Lead LFCSP Package.....	Universal
Changes to Features Section, Figure 2 Caption, General Description Section, and Figure 3 .....	1
Changed $V_S$ to $V_{SY}$ Throughout.....	3
Changes to Input Characteristics, Input Voltage Range Parameter; Dynamic Performance, Settling Time to 0.1% and Phase Margin Parameters; and Noise Performance, Peak-to-Peak Noise Parameter, Table 1 .....	3
Changes to Input Characteristics, Input Voltage Range Parameter; Dynamic Performance, Settling Time to 0.1% and Phase Margin Parameters; and Noise Performance, Peak-to-Peak Noise Parameter, Table 2 .....	4
Changes to Table 3 and Table 4.....	5
Changes to Figure 12 to Figure 15.....	7
Changes to Figure 18 Caption.....	8
Changes to Figure 30 and Figure 31.....	10
Updated Outline Dimensions .....	12
Added Figure 44; Renumbered Sequentially .....	14
Changes to Ordering Guide .....	15

### 1/06—Rev. A to Rev. B

Added AD8613 .....	Universal
Changes to Features .....	1
Changes to Table 1.....	3
Changes to Table 2.....	4
Updated Outline Dimensions .....	12
Changes to Ordering Guide .....	13

### 10/05—Rev. 0 to Rev. A

Added AD8619 .....	Universal
Change to Specifications Section .....	3
Updated Outline Dimensions .....	12
Changes to Ordering Guide .....	13

### 9/05—Revision 0: Initial Version

## SPECIFICATIONS

Electrical characteristics at  $V_{SY} = 5\text{ V}$ ,  $V_{CM} = V_{SY}/2$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage	$V_{OS}$	$-0.3\text{ V} < V_{CM} < +5.3\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ , $-0.3\text{ V} < V_{CM} < +5.2\text{ V}$		0.4	2.2	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1	2.2	mV
AD8613				2.5	4.5	$\mu\text{V}/^\circ\text{C}$
Input Bias Current	$I_B$	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.2	1	pA
Input Offset Current	$I_{OS}$	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.1	0.5	pA
Input Voltage Range	IVR		0		5	V
Common-Mode Rejection Ratio	CMRR	$0\text{ V} < V_{CM} < 5\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		68	95	dB
Large Signal Voltage Gain	$A_{VO}$	$R_L = 10\text{ k}\Omega$ , $0.5\text{ V} < V_O < 4.5\text{ V}$	235	500		V/mV
Input Capacitance	$C_{DIFF}$ $C_{CM}$			1.9	2.5	pF
						pF
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage High	$V_{OH}$	$I_L = 1\text{ mA}$ $-40^\circ\text{C}$ to $+125^\circ\text{C}$	4.95	4.98		V
		$I_L = 10\text{ mA}$ $-40^\circ\text{C}$ to $+125^\circ\text{C}$	4.9	4.7		V
Output Voltage Low	$V_{OL}$	$I_L = 1\text{ mA}$ $-40^\circ\text{C}$ to $+125^\circ\text{C}$	4.50	20	30	mV
		$I_L = 10\text{ mA}$ $-40^\circ\text{C}$ to $+125^\circ\text{C}$		190	275	mV
Short-Circuit Current	$I_{SC}$	$-40^\circ\text{C}$ to $+125^\circ\text{C}$		$\pm 80$	335	mV
Closed-Loop Output Impedance	$Z_{OUT}$	$f = 10\text{ kHz}$ , $A_V = 1$		15		$\Omega$
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio	PSRR	$1.8\text{ V} < V_{SY} < 5\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	67	94		dB
Supply Current/Amplifier	$I_{SY}$	$V_O = V_{SY}/2$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	64	38	50	$\mu\text{A}$
						$\mu\text{A}$
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 10\text{ k}\Omega$		0.1		V/ $\mu\text{s}$
Settling Time to 0.1%	$t_s$	$G = \pm 1$ , $V_{IN} = 2\text{ V}$ step, $C_L = 20\text{ pF}$ , $R_L = 1\text{ k}\Omega$		23		$\mu\text{s}$
Gain Bandwidth Product	GBP	$R_L = 100\text{ k}\Omega$ $R_L = 10\text{ k}\Omega$		400		kHz
Phase Margin	$\phi_M$	$R_L = 10\text{ k}\Omega$ , $R_L = 100\text{ k}\Omega$ , $C_L = 20\text{ pF}$		350	70	kHz
						Degrees
<b>NOISE PERFORMANCE</b>						
Peak-to-Peak Noise	$e_n$ p-p	0.1 Hz to 10 Hz		2.3	3.5	$\mu\text{V}$
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$ $f = 10\text{ kHz}$		25		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 1\text{ kHz}$		22		$\text{nV}/\sqrt{\text{Hz}}$
				0.05		$\text{pA}/\sqrt{\text{Hz}}$

# AD8613/AD8617/AD8619

Electrical characteristics at  $V_{SY} = 1.8\text{ V}$ ,  $V_{CM} = V_{SY}/2$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 2.**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage	$V_{OS}$	$-0.3\text{ V} < V_{CM} < +1.9\text{ V}$ $-0.3\text{ V} < V_{CM} < +1.8\text{ V}; -40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.4	2.2	mV
Offset Voltage Drift AD8613	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1	8.5	$\mu\text{V}/^\circ\text{C}$
Input Bias Current	$I_B$	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.2	1	pA
Input Offset Current	$I_{OS}$	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.1	0.5	pA
Input Voltage Range	IVR		0		1.8	V
Common-Mode Rejection Ratio	CMRR	$0\text{ V} < V_{CM} < 1.8\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	58	86		dB
Large Signal Voltage Gain	$A_{VO}$	$R_L = 10\text{ k}\Omega$ , $0.5\text{ V} < V_O < 1.3\text{ V}$	85	1000		V/mV
Input Capacitance	$C_{DIFF}$ $C_{CM}$			2.1		pF
				3.8		pF
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage High	$V_{OH}$	$I_L = 1\text{ mA}$ $-40^\circ\text{C}$ to $+125^\circ\text{C}$	1.65	1.73		V
Output Voltage Low	$V_{OL}$	$I_L = 1\text{ mA}$ $-40^\circ\text{C}$ to $+125^\circ\text{C}$		44	60	mV
Short-Circuit Current	$I_{SC}$			$\pm 7$	80	mV
Closed-Loop Output Impedance	$Z_{OUT}$	$f = 10\text{ kHz}$ , $A_V = 1$		15		$\Omega$
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio	PSRR	$1.8\text{ V} < V_S < 5\text{ V}$	67	94		dB
Supply Current/Amplifier	$I_{SY}$	$V_O = V_{SY}/2$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		38	50	$\mu\text{A}$
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 10\text{ k}\Omega$		0.1		V/ $\mu\text{s}$
Settling Time to 0.1%	$t_S$	$G = \pm 1$ , $V_{IN} = 1\text{ V}$ step, $C_L = 20\text{ pF}$ , $R_L = 1\text{ k}\Omega$		6.5		$\mu\text{s}$
Gain Bandwidth Product	GBP	$R_L = 100\text{ k}\Omega$ $R_L = 10\text{ k}\Omega$		400		kHz
Phase Margin	$\phi_M$	$R_L = 10\text{ k}\Omega$ , $R_L = 100\text{ k}\Omega$ , $C_L = 20\text{ pF}$		350		kHz
				70		Degrees
<b>NOISE PERFORMANCE</b>						
Peak-to-Peak Noise	$e_n$ p-p	0.1 Hz to 10 Hz		2.3	3.5	$\mu\text{V}$
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$ $f = 10\text{ kHz}$		25		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 1\text{ kHz}$		22		$\text{nV}/\sqrt{\text{Hz}}$
				0.05		$\text{pA}/\sqrt{\text{Hz}}$

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 3.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	$V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$
Input Current	$\pm 10\text{ mA}$
Differential Input Voltage	$\pm 6\text{ V}$
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Lead Temperature (Soldering, 60 sec)	$300^\circ\text{C}$
Operating Temperature Range	$-40^\circ\text{C}$ to $+125^\circ\text{C}$
Junction Temperature Range	$-65^\circ\text{C}$ to $+150^\circ\text{C}$

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL RESISTANCE

$\theta_{JA}$  is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Characteristics

Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
5-Lead TSOT-23 (UJ-5)	207	61	$^\circ\text{C}/\text{W}$
5-Lead SC70 (KS-5)	376	126	$^\circ\text{C}/\text{W}$
8-Lead MSOP (RM-8)	210	45	$^\circ\text{C}/\text{W}$
8-Lead SOIC_N (R-8)	158	43	$^\circ\text{C}/\text{W}$
8-Lead LFCSP_VD (CP-8-9)	81	20	$^\circ\text{C}/\text{W}$
14-Lead SOIC_N (R-14)	120	36	$^\circ\text{C}/\text{W}$
14-Lead TSSOP (RU-14)	180	35	$^\circ\text{C}/\text{W}$

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{SY} = 5\text{ V}$  or  $\pm 2.5\text{ V}$ , unless otherwise noted.



Figure 6. Input Offset Voltage Distribution

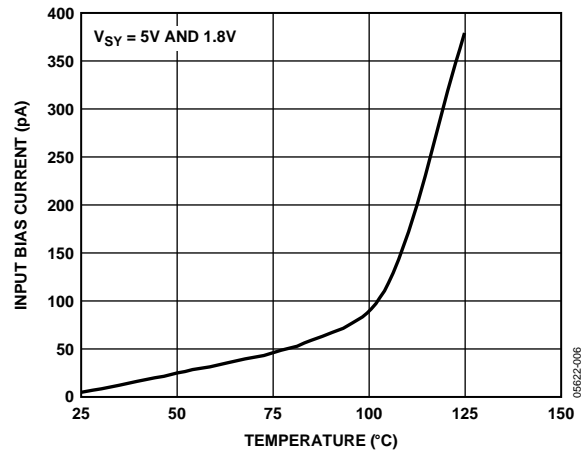


Figure 9. Input Bias Current vs. Temperature

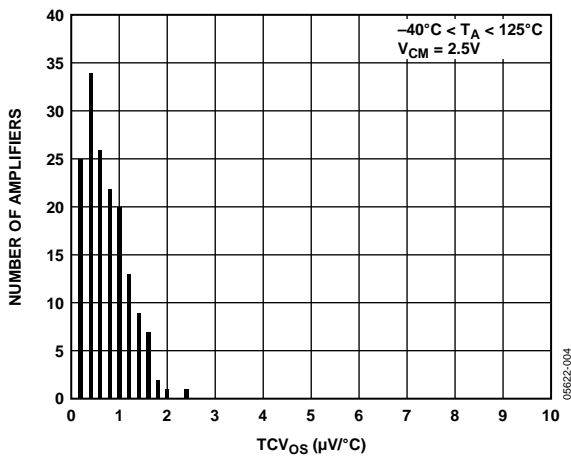


Figure 7. Input Offset Voltage Drift Distribution

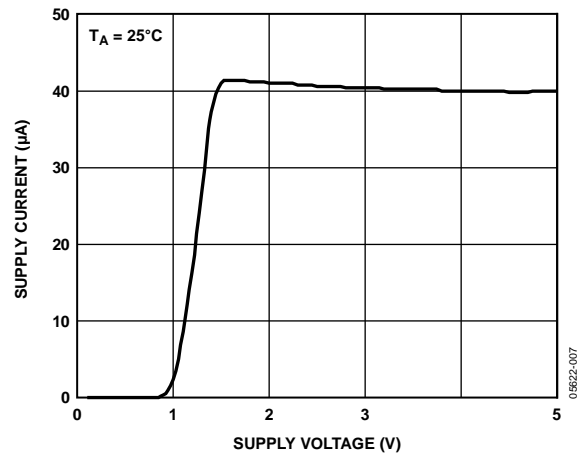


Figure 10. Supply Current vs. Supply Voltage

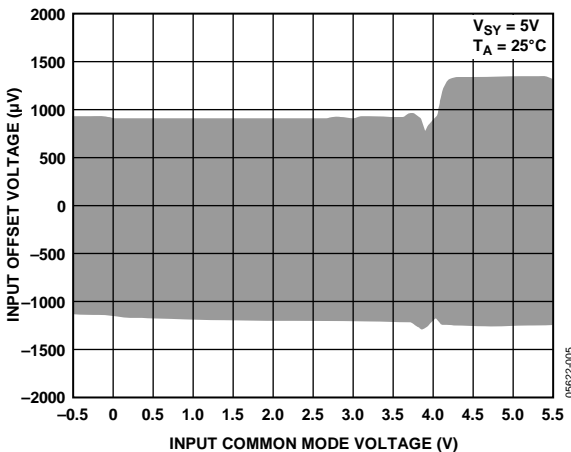


Figure 8. Input Offset Voltage vs. Input Common-Mode Voltage

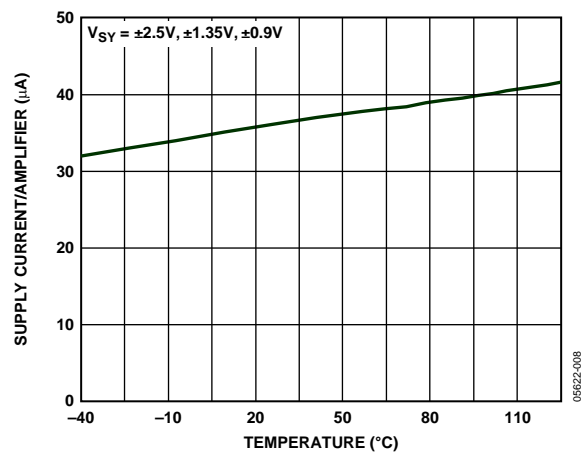


Figure 11. Supply Current vs. Temperature



Figure 12. Output Voltage to Supply Rail vs. Load Current



Figure 15. Open-Loop Gain and Phase vs. Frequency



Figure 13. Output Voltage to Supply Rail vs. Temperature ( $I_L = 1 \text{ mA}$ )

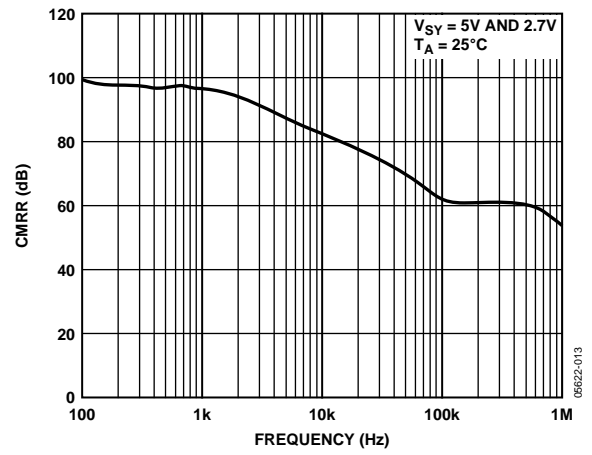


Figure 16. CMRR vs. Frequency



Figure 14. Output Voltage to Supply Rail vs. Temperature ( $I_L = 10 \text{ mA}$ )

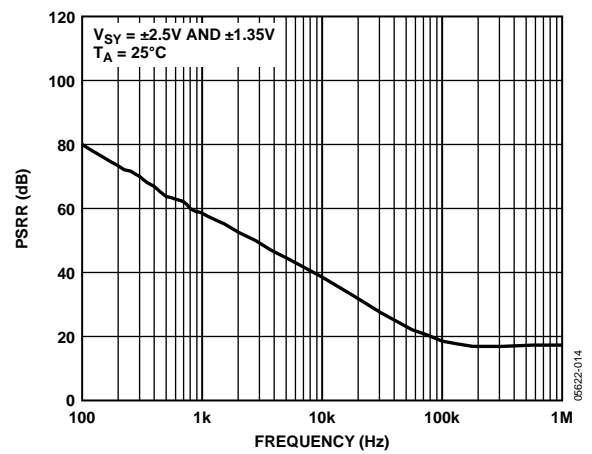


Figure 17. PSRR vs. Frequency

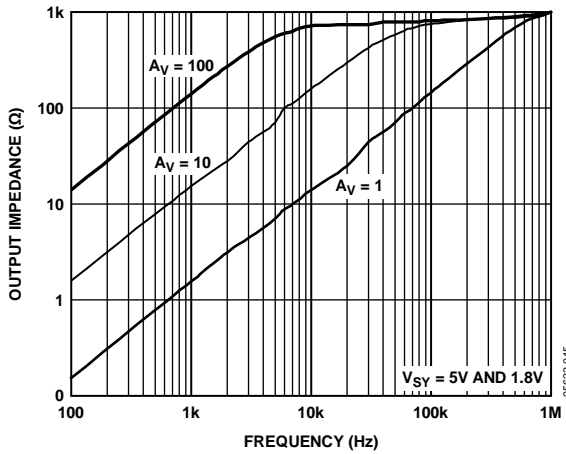


Figure 18. Output Impedance vs. Frequency

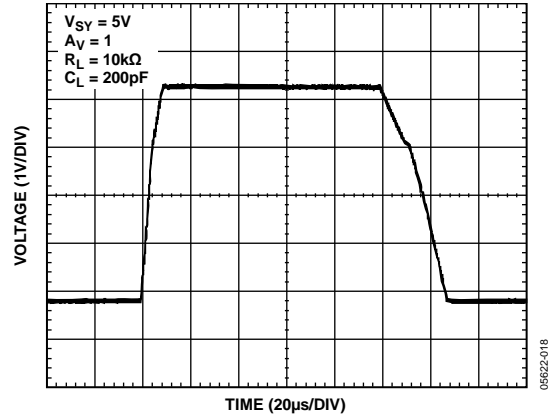


Figure 21. Large Signal Transient Response

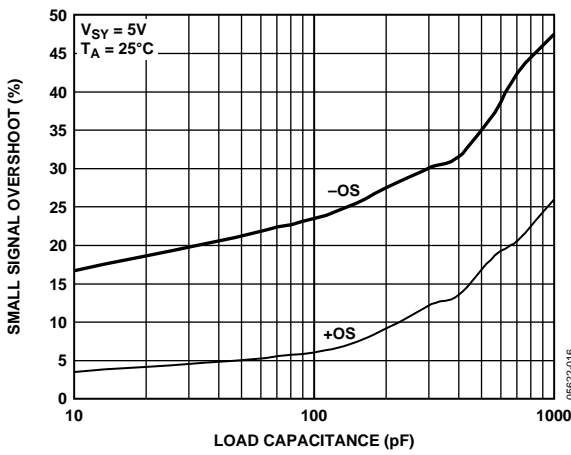


Figure 19. Small Signal Overshoot vs. Load Capacitance



Figure 22. Positive Overload Recovery



Figure 20. Small Signal Transient Response



Figure 23. Negative Overload Recovery





Figure 24. No Phase Reversal

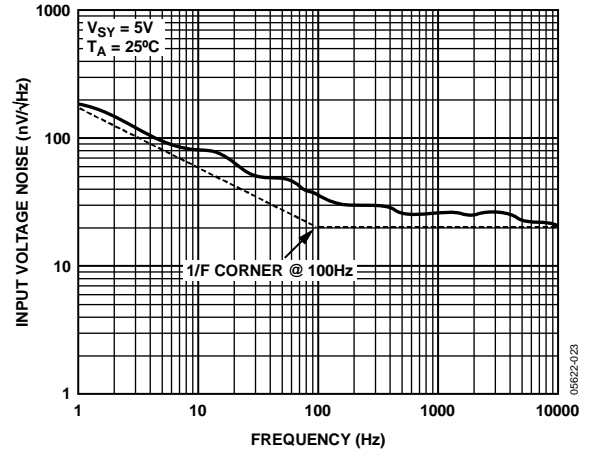


Figure 26. Voltage Noise Density

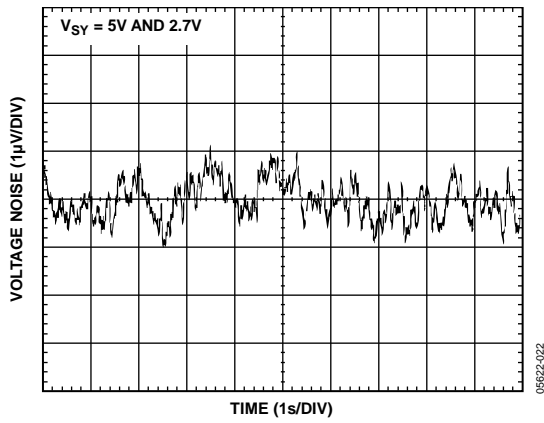


Figure 25. 0.1 Hz to 10 Hz Input Voltage Noise



Figure 27. Channel Separation

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$V_{SY} = 1.8\text{ V}$  or  $\pm 0.9\text{ V}$ , unless otherwise noted.



Figure 28. Input Offset Voltage Distribution



Figure 31. Output Voltage to Supply Rail vs. Temperature ( $I_L = 1\text{ mA}$ )



Figure 29. Input Offset Voltage vs. Input Common-Mode Voltage



Figure 32. CMRR vs. Frequency



Figure 30. Output Voltage to Supply Rail vs. Load Current



Figure 33. PSRR vs. Frequency



Figure 34. Small Signal Overshoot vs. Load Capacitance



Figure 36. 0.1 Hz to 10 Hz Input Voltage Noise

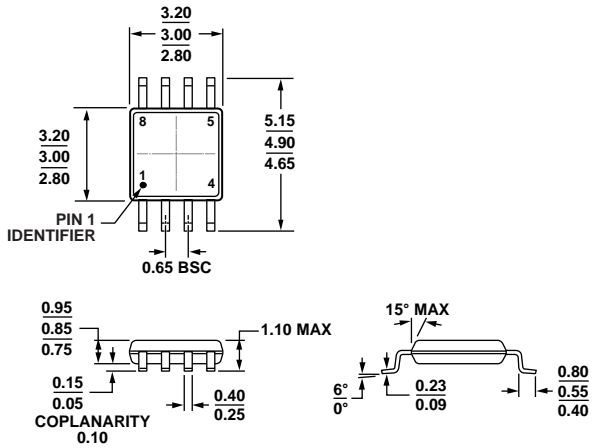


Figure 35. Large Signal Transient Response



Figure 37. Voltage Noise Density

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-AA  
 Figure 38. 8-Lead Mini Small Outline Package [MSOP] (RM-8)  
 Dimensions shown in millimeters

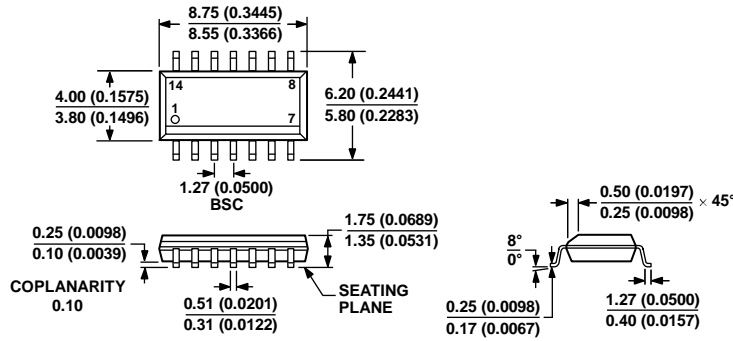
100709-B



COMPLIANT TO JEDEC STANDARDS MS-012-AA  
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 39. 8-Lead Standard Small Outline Package [SOIC\_N] Narrow Body (R-8)  
 Dimensions shown in millimeters and (inches)

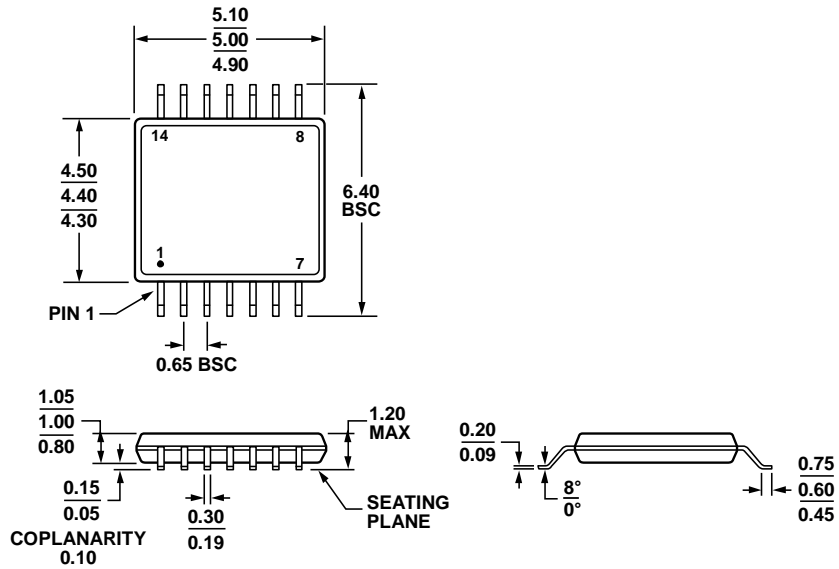
012407-A



COMPLIANT TO JEDEC STANDARDS MS-012-AB  
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 40. 14-Lead Standard Small Outline Package [SOIC\_N] Narrow Body (R-14)  
 Dimensions shown in millimeters and (inches)

060606-A

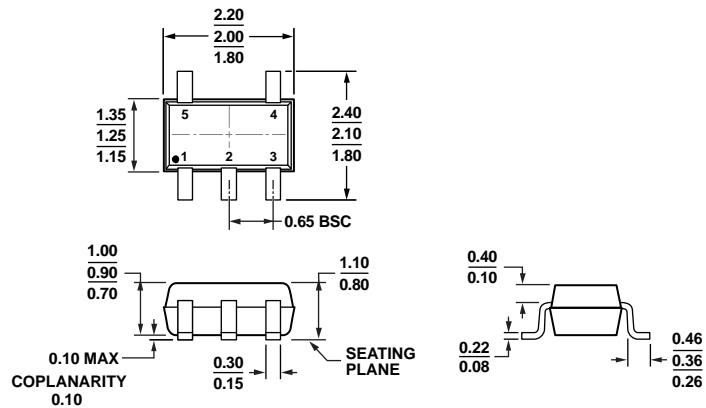


COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

Figure 41. 14-Lead Thin Shrink Small Outline Package [TSSOP] (RU-14)

Dimensions shown in millimeters

061908-A



COMPLIANT TO JEDEC STANDARDS MO-203-AA

Figure 42. 5-Lead Thin Shrink Small Outline Transistor Package [SC70] (KS-5)

Dimensions shown in millimeters

072809-A

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\*COMPLIANT TO JEDEC STANDARDS MO-193-AB WITH THE EXCEPTION OF PACKAGE HEIGHT AND THICKNESS.

Figure 43. 5-Lead Thin Small Outline Transistor Package [TSOT-23] (UJ-5)

Dimensions shown in millimeters

100708-A



Figure 44. 8-Lead Lead Frame Chip Scale Package [LFCSP\_VD]

3 mm x 3 mm Body, Very Thin, Dual Lead (CP-8-9)

Dimensions shown in millimeters

0519809-A

**ORDERING GUIDE**

Model <sup>1</sup>	Temperature Range	Package Description	Package Option	Branding
AD8613AKSZ-R2	-40°C to +125°C	5-Lead SC70	KS-5	A0Y
AD8613AKSZ-REEL	-40°C to +125°C	5-Lead SC70	KS-5	A0Y
AD8613AKSZ-REEL7	-40°C to +125°C	5-Lead SC70	KS-5	A0Y
AD8613AUJZ-R2	-40°C to +125°C	5-Lead TSOT-23	UJ-5	A0Y
AD8613AUJZ-REEL	-40°C to +125°C	5-Lead TSOT-23	UJ-5	A0Y
AD8613AUJZ-REEL7	-40°C to +125°C	5-Lead TSOT-23	UJ-5	A0Y
AD8617ACPZ-R2	-40°C to +125°C	8-Lead LFCSP_VD	CP-8-9	A0T
AD8617ACPZ-R7	-40°C to +125°C	8-Lead LFCSP_VD	CP-8-9	A0T
AD8617ACPZ-RL	-40°C to +125°C	8-Lead LFCSP_VD	CP-8-9	A0T
AD8617ARMZ	-40°C to +125°C	8-Lead MSOP	RM-8	A0T
AD8617ARMZ-REEL	-40°C to +125°C	8-Lead MSOP	RM-8	A0T
AD8617ARZ	-40°C to +125°C	8-Lead SOIC_N	R-8	
AD8617ARZ-REEL	-40°C to +125°C	8-Lead SOIC_N	R-8	
AD8617ARZ-REEL7	-40°C to +125°C	8-Lead SOIC_N	R-8	
AD8617WARMZ-REEL <sup>2</sup>	-40°C to +125°C	8-Lead MSOP	RM-8	A23
AD8617WARZ-R7 <sup>2</sup>	-40°C to +125°C	8-Lead SOIC_N	R-8	
AD8617WARZ-RL <sup>2</sup>	-40°C to +125°C	8-Lead SOIC_N	R-8	
AD8619ARUZ	-40°C to +125°C	14-Lead TSSOP	RU-14	
AD8619ARUZ-REEL	-40°C to +125°C	14-Lead TSSOP	RU-14	
AD8619ARZ	-40°C to +125°C	14-Lead SOIC_N	R-14	
AD8619ARZ-REEL	-40°C to +125°C	14-Lead SOIC_N	R-14	
AD8619ARZ-REEL7	-40°C to +125°C	14-Lead SOIC_N	R-14	

<sup>1</sup> Z = RoHS Compliant Part.

<sup>2</sup> Qualified for automotive applications.

**AD8613/AD8617/AD8619**

## **NOTES**