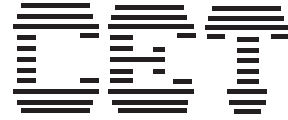


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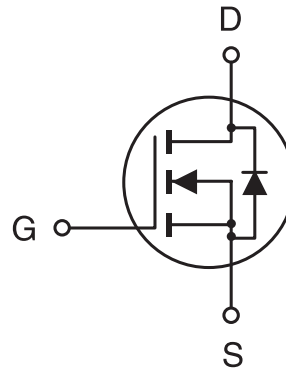
PRELIMINARY

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N-Channel Logic Level Enhancement Mode Field Effect Transistor

FEATURES

- 30V , 75A , $R_{DS(ON)}=6m\Omega$ @ $V_{GS}=10V$.
 $R_{DS(ON)}=9m\Omega$ @ $V_{GS}=4.5V$.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability.
- TO-220 & TO-263 package.



ABSOLUTE MAXIMUM RATINGS (Tc=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	30	V
Gate-Source Voltage	V _{GS}	±16	V
Drain Current-Continuous -Pulsed	I _D	75	A
	I _{DM}	156	A
Drain-Source Diode Forward Current	I _S	75	A
Maximum Power Dissipation @T _c =25°C Derate above 25°C	P _D	50	W
		0.4	W/°C
Operating and Storage Temperature Range	T _J , T _{STG}	-65 to 175	°C

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Case	R _{θJC}	2.5	°C/W
Thermal Resistance, Junction-to-Ambient	R _{θJA}	62.5	°C/W

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ELECTRICAL CHARACTERISTICS (Tc=25°C unless otherwise noted)

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Parameter	Symbol	Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	30			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =24V, V _{GS} =0V			10	μA
Gate-Body Leakage	I _{GSS}	V _{GS} =±16V, V _{DS} =0V			±100	nA
ON CHARACTERISTICS^a						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1		3	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =37.5A			6	mΩ
		V _{GS} =4.5V, I _D =30A			9	mΩ
On-State Drain Current	I _{D(ON)}	V _{GS} =10V, V _{DS} =10V	75			A
Forward Transconductance	g _{FS}	V _{DS} =10V, I _D =26A		32		S
DYNAMIC CHARACTERISTICS^b						
Input Capacitance	C _{ISS}	V _{DS} =15V, V _{GS} =0V f=1.0MHz		3898	5100	pF
Output Capacitance	C _{OSS}			1876	2500	pF
Reverse Transfer Capacitance	C _{RSS}			270	350	pF
SWITCHING CHARACTERISTICS^b						
Turn-On Delay Time	t _{D(ON)}	V _{DD} =15V, I _D =52A, V _{GS} =10V R _{GEN} =24Ω		10	16	ns
Rise Time	t _r			200	250	ns
Turn-Off Delay Time	t _{D(OFF)}			50	90	ns
Fall Time	t _f			140	200	ns
Total Gate Charge	Q _g	V _{DS} =10V, I _D =52A, V _{GS} =10V		44	60	nC
Gate-Source Charge	Q _{gs}			6		nC
Gate-Drain Charge	Q _{gd}			14		nC

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ELECTRICAL CHARACTERISTICS ($T_c=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS ^a						
Diode Forward Voltage	V_{SD}	$V_{GS} = 0V, I_S = 37.5A$		0.9	1.3	V

Notes

a. Pulse Test: Pulse Width $\leq 300 \mu s$, Duty Cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

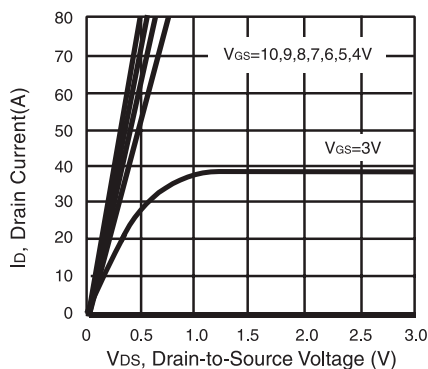


Figure 1. Output Characteristics

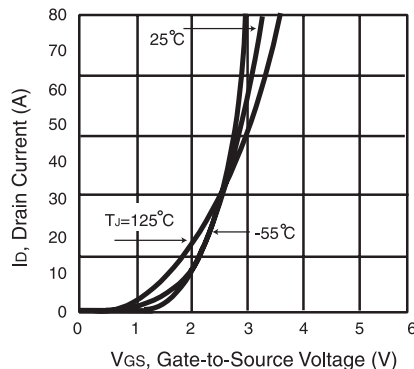


Figure 2. Transfer Characteristics

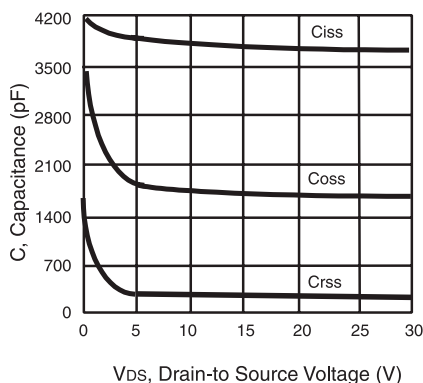


Figure 3. Capacitance

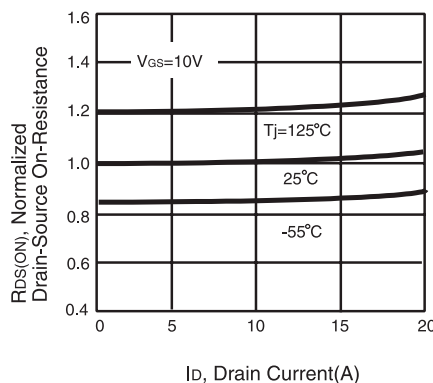


Figure 4. On-Resistance Variation with Drain Current and Temperature

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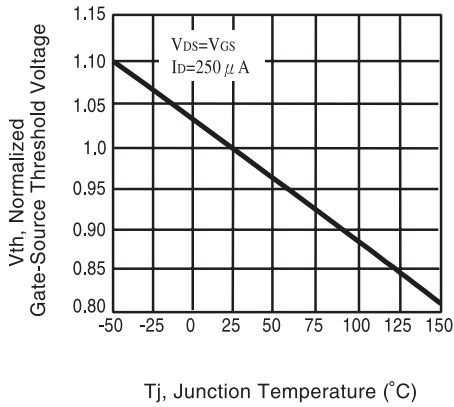


Figure 5. Gate Threshold Variation with Temperature

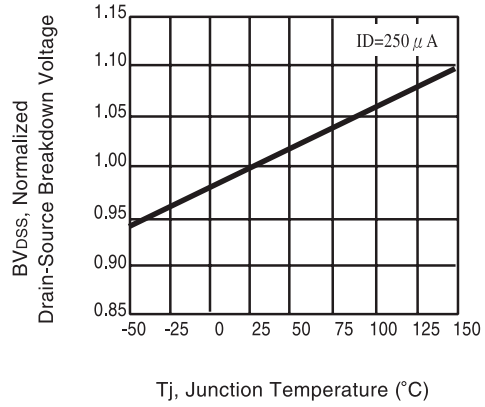


Figure 6. Breakdown Voltage Variation with Temperature

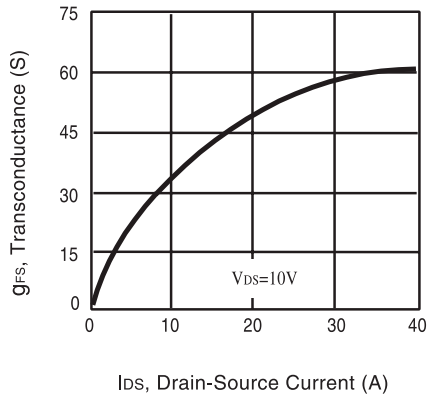


Figure 7. Transconductance Variation with Drain Current

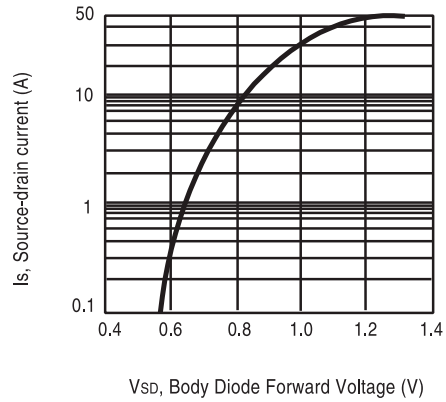


Figure 8. Body Diode Forward Voltage Variation with Source Current

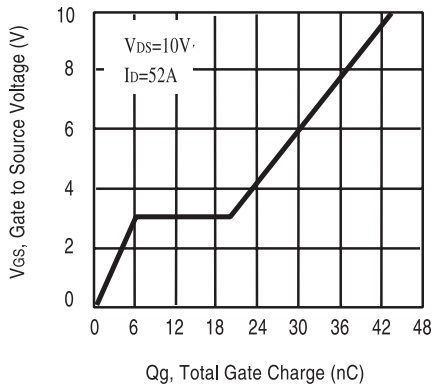


Figure 9. Gate Charge

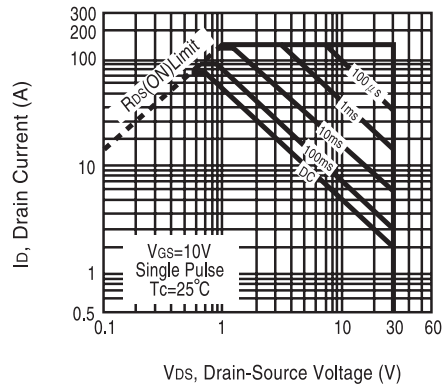


Figure 10. Maximum Operating Area

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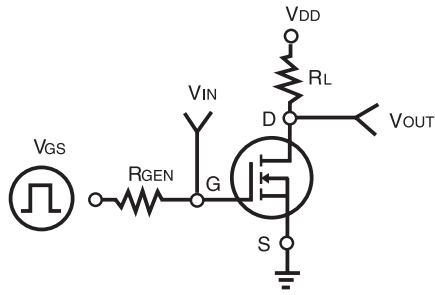


Figure 11. Switching Test Circuit

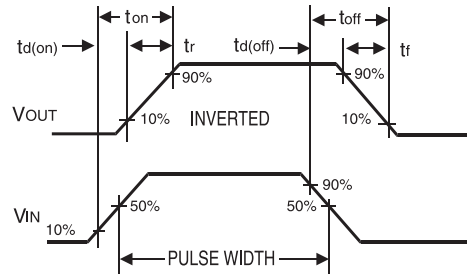


Figure 12. Switching Waveforms

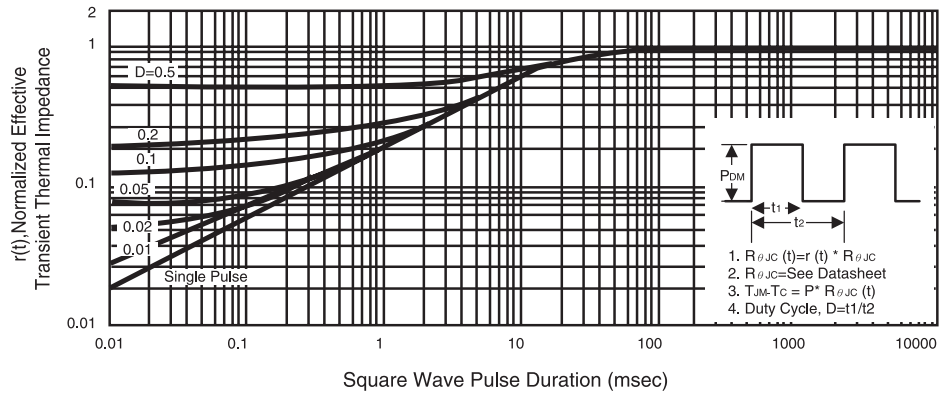


Figure 13. Normalized Thermal Transient Impedance Curve