18 V, Precision, Micropower CMOS RRIO Operational Amplifier

AD8657

FEATURES

Micropower at high voltage (18 V): 18 μA typical
Low offset voltage: 350 μV maximum
Single-supply operation: 2.7 V to 18 V
Dual-supply operation: ±1.35 V to ±9 V
Low input bias current: 20 pA
Gain bandwidth: 200 kHz
Unity-gain stable
Excellent electromagnetic interference immunity

APPLICATIONS

Portable operating systems
Current monitors
4 mA to 20 mA loop drivers
Buffer/level shifting
Multipole filters
Remote/wireless sensors
Low power transimpedance amplifiers

PIN CONFIGURATION

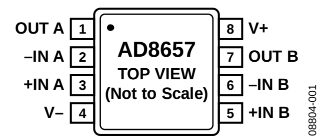

Figure 1. 8-Lead MSOP

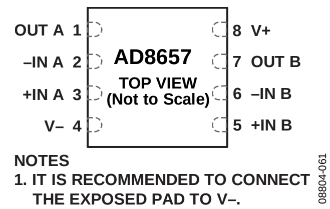

Figure 2. 8-Lead LFCSP

GENERAL DESCRIPTION

The AD8657 is a dual, micropower, precision, rail-to-rail input/output amplifier optimized for low power and wide operating supply voltage range applications.

The AD8657 operates from 2.7 V up to 18 V with a typical quiescent supply current of 18 μA. It uses the Analog Devices, Inc., patented DigiTrim® trimming technique, which achieves low offset voltage. The AD8657 also has high immunity to electromagnetic interference.

The combination of low supply current, low offset voltage, very low input bias current, wide supply range, and rail-to-rail input and output makes the AD8657 ideal for current monitoring and current loops in process and motor control applications. The combination of precision specifications makes this device ideal for dc gain and buffering of sensor front ends or high impedance input sources in wireless or remote sensors or transmitters.

The AD8657 is specified over the extended industrial temperature range (−40°C to +125°C) and is available in an 8-lead MSOP package and an 8-lead LFCSP package.

Table 1. Micropower Op Amps

Supply Voltage	5 V	12 V to 16 V	36 V
Single	AD8500 ADA4505-1 AD8505 AD8541 AD8603	AD8663	
Dual	AD8502 ADA4505-2 AD8506 AD8542 AD8607	AD8667 OP281	OP295 ADA4062-2
Quad	AD8504 ADA4505-4 AD8508 AD8544 AD8609	AD8669 OP481	OP495 ADA4062-4

Rev. A

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REVISION HISTORY

3/11—Rev. 0 to Rev. A

Added LFCSP Package Information .... Throughout
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1/11—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—2.7 V OPERATION

V_{SY} = 2.7 V, V_{CM} = V_{SY}/2 V, T_A = 25°C, unless otherwise specified.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	V_{CM} = 0 V to 2.7 V			350	μV
		V_{CM} = 0.3 V to 2.4 V; −40°C ≤ T_A ≤ +85°C			1	mV
		V_{CM} = 0.3 V to 2.4 V; −40°C ≤ T_A ≤ +125°C			2.5	mV
		V_{CM} = 0 V to 2.7 V; −40°C ≤ T_A ≤ +125°C			4	mV
Input Bias Current	I_B			1	10	pA
		−40°C ≤ T_A ≤ +125°C			2.6	nA
Input Offset Current	I_{OS}				20	pA
		−40°C ≤ T_A ≤ +125°C			500	pA
Input Voltage Range			0		2.7	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 2.7 V	79	95		dB
		V_{CM} = 0.3 V to 2.4 V; −40°C ≤ T_A ≤ +85°C	70			dB
		V_{CM} = 0.3 V to 2.4 V; −40°C ≤ T_A ≤ +125°C	63			dB
		V_{CM} = 0 V to 2.7 V; −40°C ≤ T_A ≤ +125°C	60			dB
Large Signal Voltage Gain	A_{VO}	R_L = 100 kΩ, V_O = 0.5 V to 2.2 V	94	105		dB
		−40°C ≤ T_A ≤ +85°C	75			dB
		−40°C ≤ T_A ≤ +125°C	65			dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			2		μV/°C
Input Resistance	R_{IN}			10		GΩ
Input Capacitance, Differential Mode	C_{INDM}			3.5		pF
Input Capacitance, Common Mode	C_{INCM}			3.5		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 100 kΩ to V_{CM}; −40°C ≤ T_A ≤ +125°C	2.69			V
Output Voltage Low	V_{OL}	R_L = 100 kΩ to V_{CM}; −40°C ≤ T_A ≤ +125°C			10	mV
Short-Circuit Current	I_{SC}			±4		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 kHz, A_V = 1		20		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 2.7 V to 18 V	105	125		dB
		−40°C ≤ T_A ≤ +125°C	70			dB
Supply Current per Amplifier	I_{SY}	I_O = 0 mA		18	22	μA
		−40°C ≤ T_A ≤ +125°C			33	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 1 MΩ, C_L = 10 pF, A_V = 1		38		V/ms
Settling Time to 0.1%	t_s	V_{IN} = 1 V step, R_L = 100 kΩ, C_L = 10 pF		14		μs
Gain Bandwidth Product	GBP	R_L = 1 MΩ, C_L = 10 pF, A_V = 1		170		kHz
Phase Margin	Φ_M	R_L = 1 MΩ, C_L = 10 pF, A_V = 1		60		Degrees
Channel Separation	CS	f = 10 kHz, R_L = 1 MΩ		105		dB
EMI Rejection Ratio of +IN x	EMIRR	V_{IN} = 100 mV_{PEAK}; f = 400 MHz, 900 MHz, 1800 MHz, 2400 MHz		90		dB
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	f = 0.1 Hz to 10 Hz		6		μV p-p
Voltage Noise Density	e_n	f = 1 kHz		60		nV/√Hz
		f = 10 kHz		56		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.1		pA/√Hz

ELECTRICAL CHARACTERISTICS—10 V OPERATION

V_{SY} = 10 V, V_{CM} = V_{SY}/2 V, T_A = 25°C, unless otherwise specified.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	V_{CM} = 0 V to 10 V			350	µV
		V_{CM} = 0 V to 10 V; −40°C ≤ T_A ≤ +125°C			9	mV
Input Bias Current	I_B			2	15	pA
		−40°C ≤ T_A ≤ +125°C			2.6	nA
Input Offset Current	I_{OS}				30	pA
		−40°C ≤ T_A ≤ +125°C			500	pA
Input Voltage Range			0		10	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 10 V	90	105		dB
		V_{CM} = 0 V to 10 V; −40°C ≤ T_A ≤ +125°C	64			dB
Large Signal Voltage Gain	A_{VO}	R_L = 100 kΩ, V_O = 0.5 V to 9.5 V	105	120		dB
		−40°C ≤ T_A ≤ +85°C	95			dB
		−40°C ≤ T_A ≤ +125°C	67			dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			2		µV/°C
Input Resistance	R_{IN}			10		GΩ
Input Capacitance, Differential Mode	C_{INDM}			3.5		pF
Input Capacitance, Common Mode	C_{INCM}			3.5		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 100 kΩ to V_{CM}; −40°C ≤ T_A ≤ +125°C	9.98			V
Output Voltage Low	V_{OL}	R_L = 100 kΩ to V_{CM}; −40°C ≤ T_A ≤ +125°C			20	mV
Short-Circuit Current	I_{SC}			±11		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 kHz, A_V = 1		15		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 2.7 V to 18 V	105	125		dB
		−40°C ≤ T_A ≤ +125°C	70			dB
Supply Current per Amplifier	I_{SY}	I_O = 0 mA		18	22	µA
		−40°C ≤ T_A ≤ +125°C			33	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 1 MΩ, C_L = 10 pF, A_V = 1		60		V/ms
Settling Time to 0.1%	t_s	V_{IN} = 1 V step, R_L = 100 kΩ, C_L = 10 pF		13		µs
Gain Bandwidth Product	GBP	R_L = 1 MΩ, C_L = 10 pF, A_V = 1		200		kHz
Phase Margin	Φ_M	R_L = 1 MΩ, C_L = 10 pF, A_V = 1		60		Degrees
Channel Separation	CS	f = 10 kHz, R_L = 1 MΩ		105		dB
EMI Rejection Ratio of +IN x	EMIRR	V_{IN} = 100 mV_{PEAK}; f = 400 MHz, 900 MHz, 1800 MHz, 2400 MHz		90		dB
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	f = 0.1 Hz to 10 Hz		5		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		50		nV/√Hz
		f = 10 kHz		45		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.1		pA/√Hz

ELECTRICAL CHARACTERISTICS—18 V OPERATION

V_{SY} = 18 V, V_{CM} = V_{SY}/2 V, T_A = 25°C, unless otherwise specified.

Table 4.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	V_{CM} = 0 V to 18 V			350	µV
		V_{CM} = 0.3 V to 17.7 V; −40°C ≤ T_A ≤ +85°C			1.2	mV
		V_{CM} = 0.3 V to 17.7 V; −40°C ≤ T_A ≤ +125°C			2	mV
		V_{CM} = 0 V to 18 V; −40°C ≤ T_A ≤ +125°C			11	mV
Input Bias Current	I_B			5	20	pA
		−40°C ≤ T_A ≤ +125°C			2.9	nA
Input Offset Current	I_{OS}				40	pA
		−40°C ≤ T_A ≤ +125°C			500	pA
Input Voltage Range			0		18	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 18 V	95	110		dB
		V_{CM} = 0.3 V to 17.7 V; −40°C ≤ T_A ≤ +85°C	83			dB
		V_{CM} = 0.3 V to 17.7 V; −40°C ≤ T_A ≤ +125°C	80			dB
		V_{CM} = 0 V to 18 V; −40°C ≤ T_A ≤ +125°C	67			dB
Large Signal Voltage Gain	A_{VO}	R_L = 100 kΩ, V_O = 0.5 V to 17.5 V	110	120		dB
		−40°C ≤ T_A ≤ +85°C	105			dB
		−40°C ≤ T_A ≤ +125°C	73			dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			2		µV/°C
Input Resistance	R_{IN}			10		GΩ
Input Capacitance, Differential Mode	C_{INDM}			3.5		pF
Input Capacitance, Common Mode	C_{INCM}			10.5		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 100 kΩ to V_{CM}; −40°C ≤ T_A ≤ +125°C	17.97			V
Output Voltage Low	V_{OL}	R_L = 100 kΩ to V_{CM}; −40°C ≤ T_A ≤ +125°C			30	mV
Short-Circuit Current	I_{SC}			±12		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 kHz, A_V = 1		15		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 2.7 V to 18 V	105	125		dB
		−40°C ≤ T_A ≤ +125°C	70			dB
Supply Current per Amplifier	I_{SY}	I_O = 0 mA		18	22	µA
		−40°C ≤ T_A ≤ +125°C			33	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 1 MΩ, C_L = 10 pF, A_V = 1		70		V/ms
Settling Time to 0.1%	t_s	V_{IN} = 1 V step, R_L = 100 kΩ, C_L = 10 pF		12		µs
Gain Bandwidth Product	GBP	R_L = 1 MΩ, C_L = 10 pF, A_V = 1		200		kHz
Phase Margin	Φ_M	R_L = 1 MΩ, C_L = 10 pF, A_V = 1		60		Degrees
Channel Separation	CS	f = 10 kHz, R_L = 1 MΩ		105		dB
EMI Rejection Ratio of +IN x	EMIRR	V_{IN} = 100 mV_{PEAK}; f = 400 MHz, 900 MHz, 1800 MHz, 2400 MHz		90		dB
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	f = 0.1 Hz to 10 Hz		5		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		50		nV/√Hz
		f = 10 kHz		45		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.1		pA/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	20.5 V
Input Voltage	(V−) − 300 mV to (V+) + 300 mV
Input Current[1]	±10 mA
Differential Input Voltage	$\pm V_{SY}$
Output Short-Circuit Duration to GND	Indefinite
Temperature Range	
Storage	−65°C to +150°C
Operating	−40°C to +125°C
Junction	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

[1] The input pins have clamp diodes to the power supply pins. Limit the input current to 10 mA or less whenever input signals exceed the power supply rail by 0.3 V.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

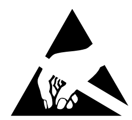
THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages using a standard 4-layer JEDEC board. The exposed pad is soldered to the board.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead MSOP (RM-8)	142	45	°C/W
8-Lead LFCSP (CP-8-11)	75	12	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

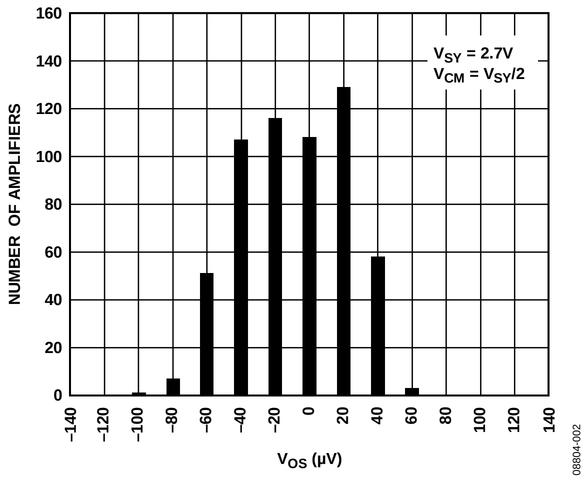


Figure 3. Input Offset Voltage Distribution

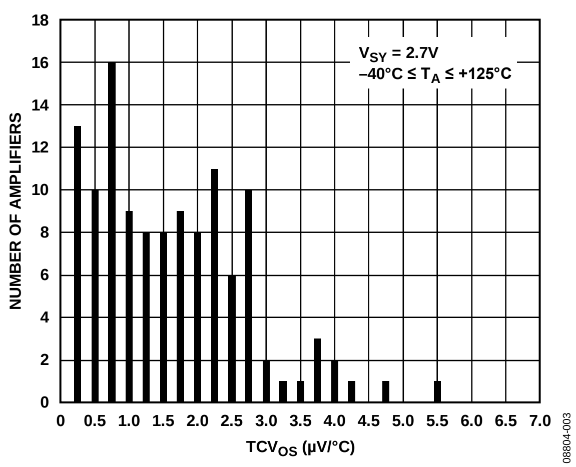


Figure 4. Input Offset Voltage Drift Distribution

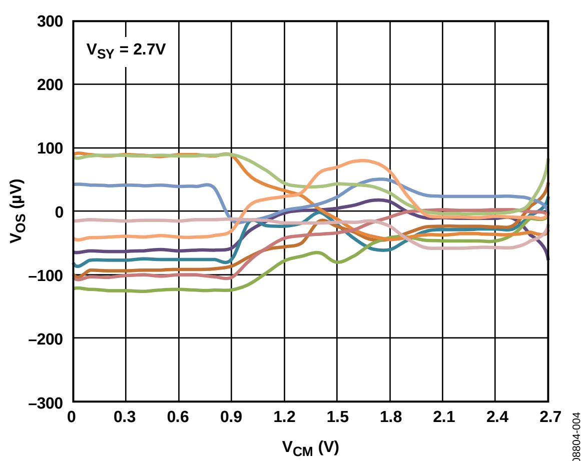


Figure 5. Input Offset Voltage vs. Common-Mode Voltage

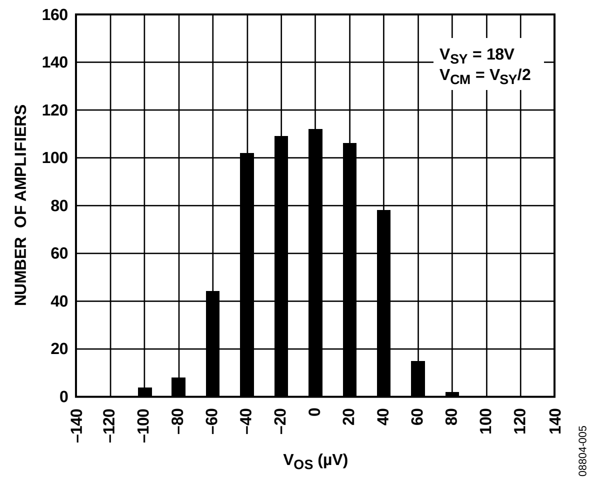


Figure 6. Input Offset Voltage Distribution

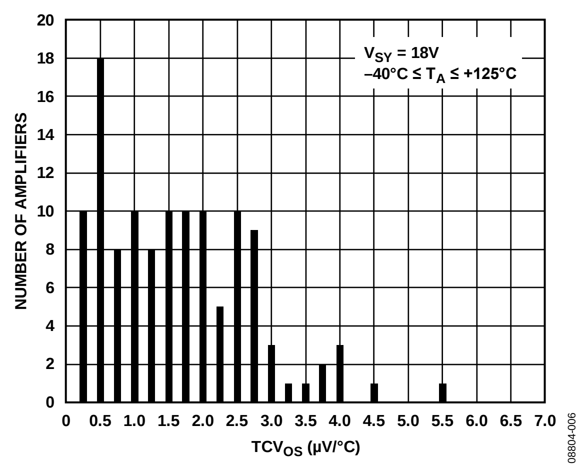


Figure 7. Input Offset Voltage Drift Distribution

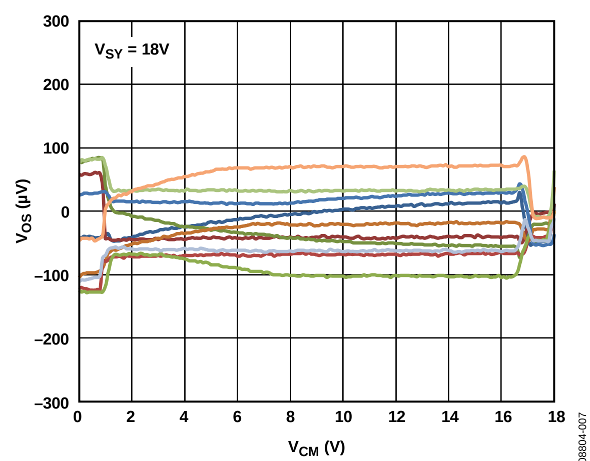


Figure 8. Input Offset Voltage vs. Common-Mode Voltage

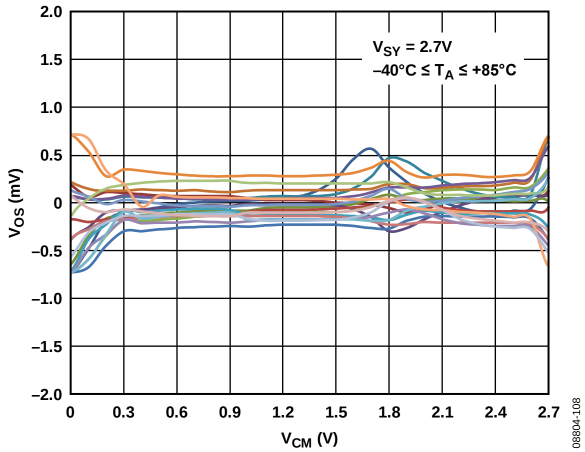


Figure 9. Input Offset Voltage vs. Common-Mode Voltage

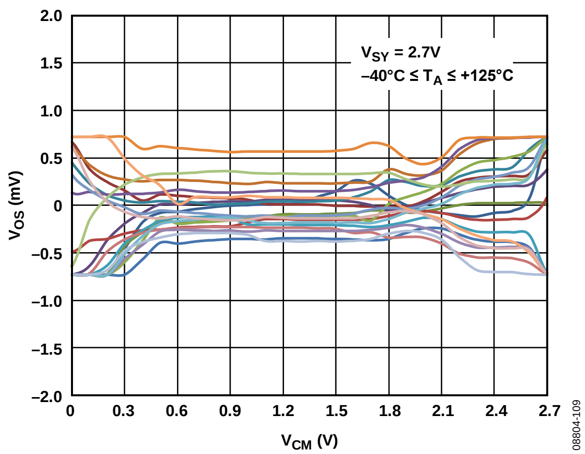


Figure 10. Input Offset Voltage vs. Common-Mode Voltage

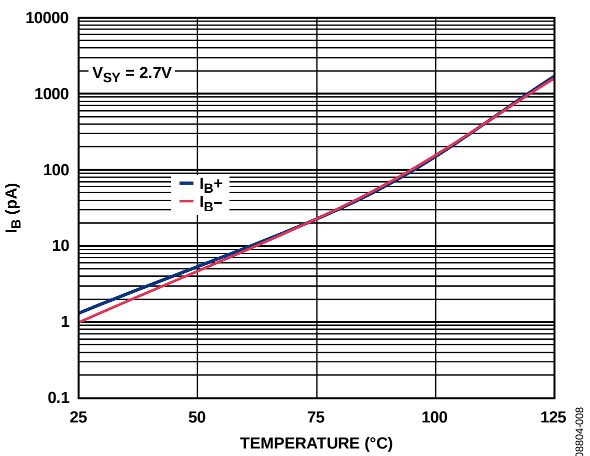


Figure 11. Input Bias Current vs. Temperature

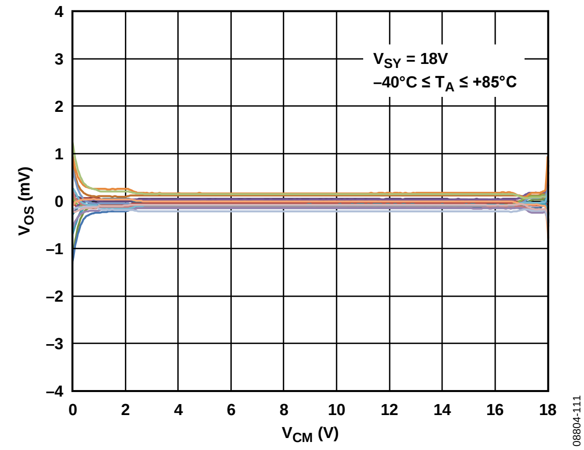


Figure 12. Input Offset Voltage vs. Common-Mode Voltage

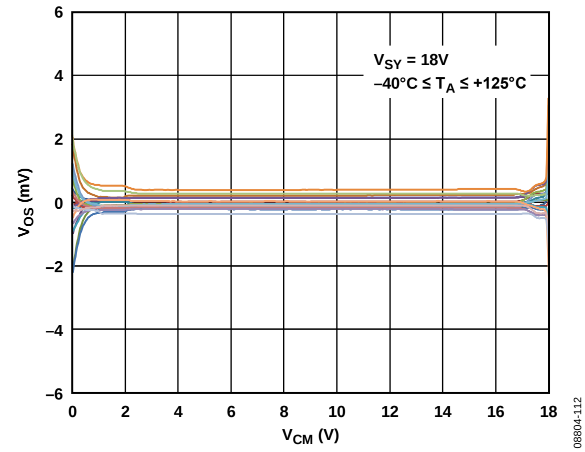


Figure 13. Input Offset Voltage vs. Common-Mode Voltage

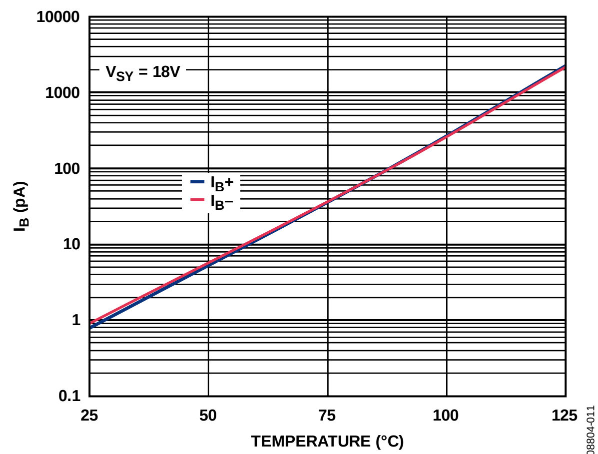


Figure 14. Input Bias Current vs. Temperature

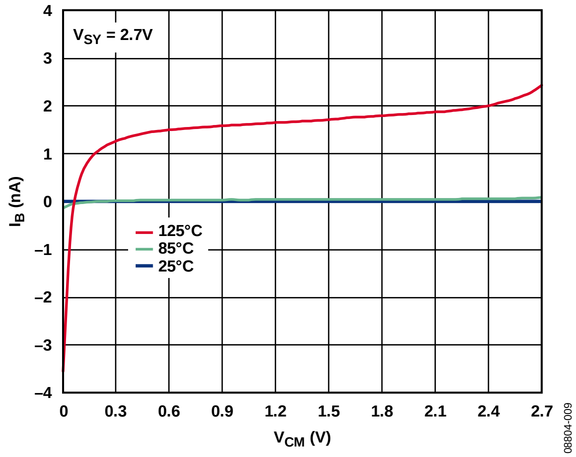


Figure 15. Input Bias Current vs. Common-Mode Voltage

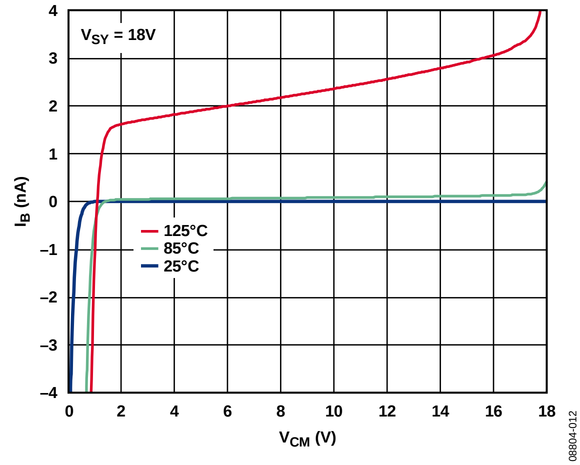


Figure 18. Input Bias Current vs. Common-Mode Voltage

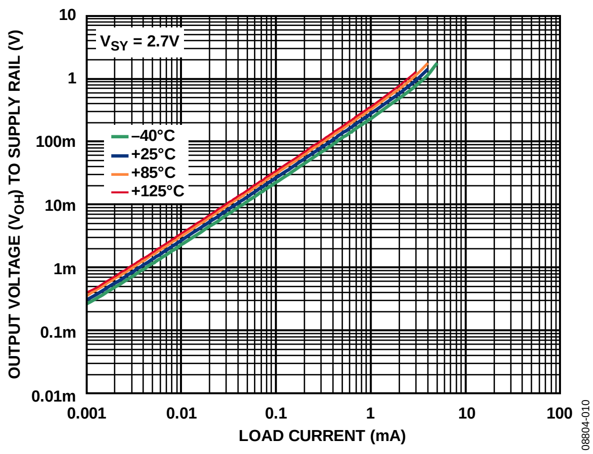


Figure 16. Output Voltage (V_{OH}) to Supply Rail vs. Load Current

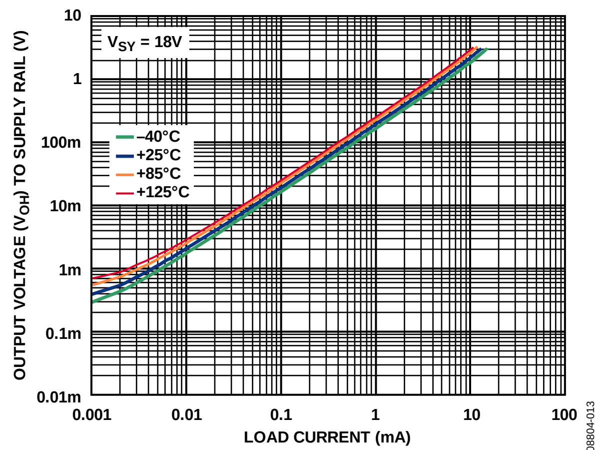


Figure 19. Output Voltage (V_{OH}) to Supply Rail vs. Load Current

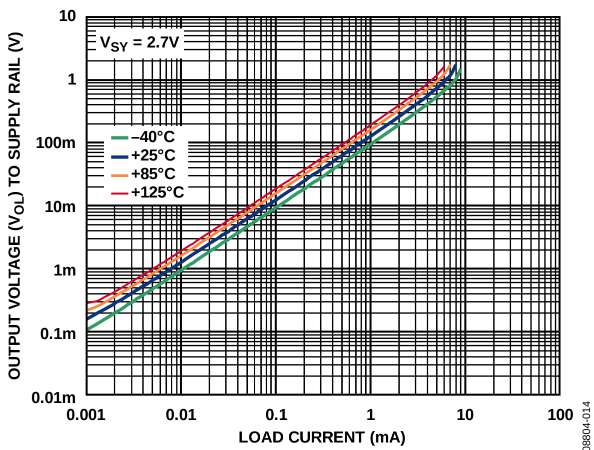


Figure 17. Output Voltage (V_{OL}) to Supply Rail vs. Load Current

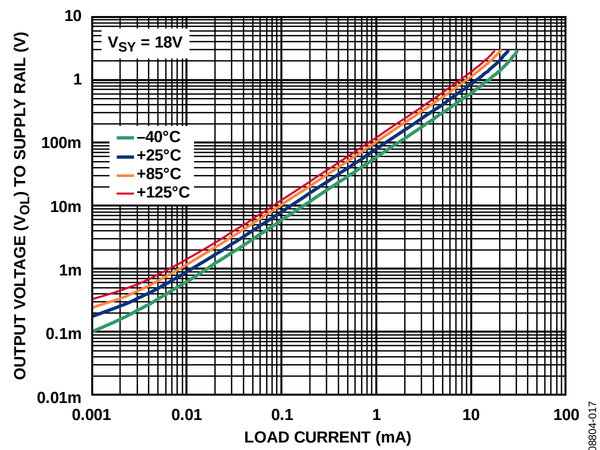


Figure 20. Output Voltage (V_{OL}) to Supply Rail vs. Load Current

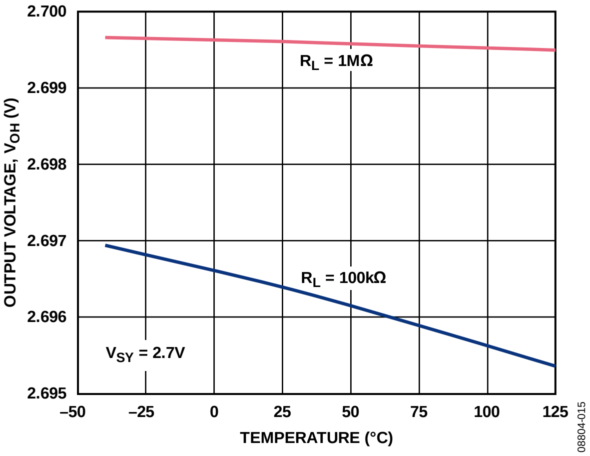


Figure 21. Output Voltage (V_{OH}) vs. Temperature

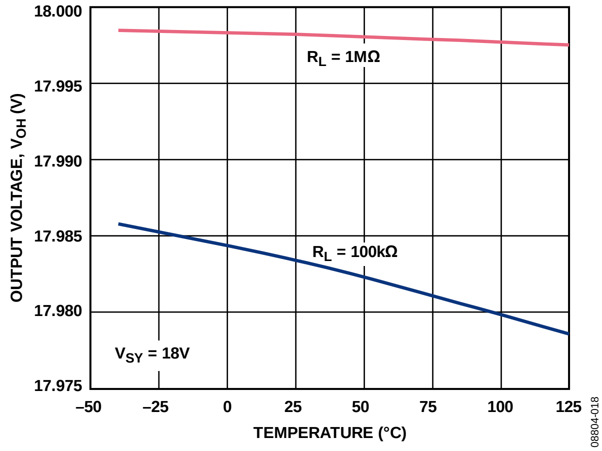


Figure 24. Output Voltage (V_{OH}) vs. Temperature

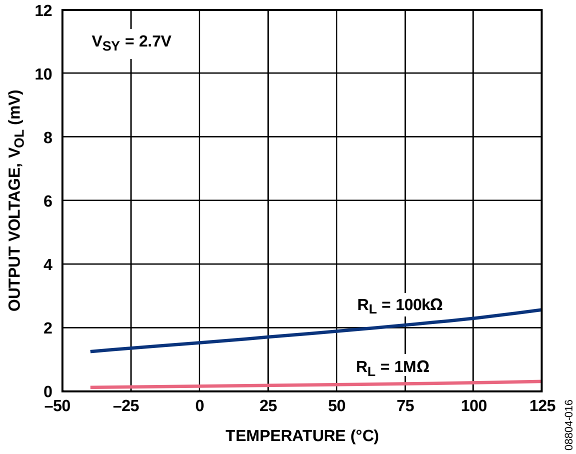


Figure 22. Output Voltage (V_{OL}) vs. Temperature

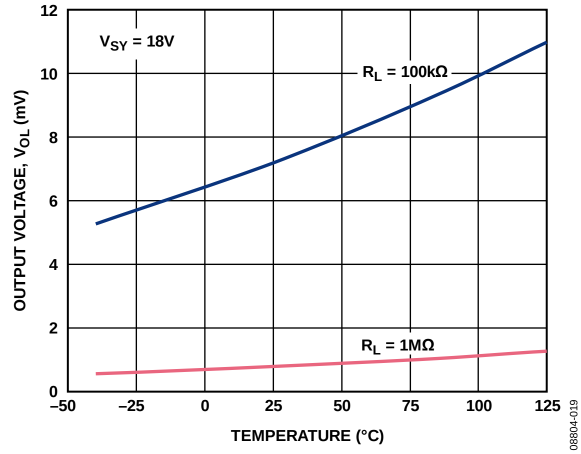


Figure 25. Output Voltage (V_{OL}) vs. Temperature

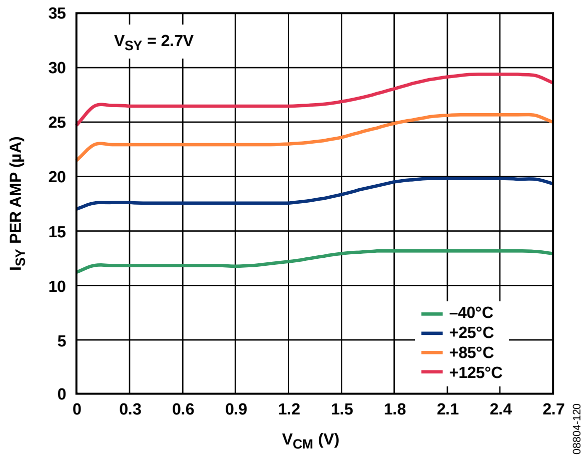


Figure 23. Supply Current vs. Common-Mode Voltage

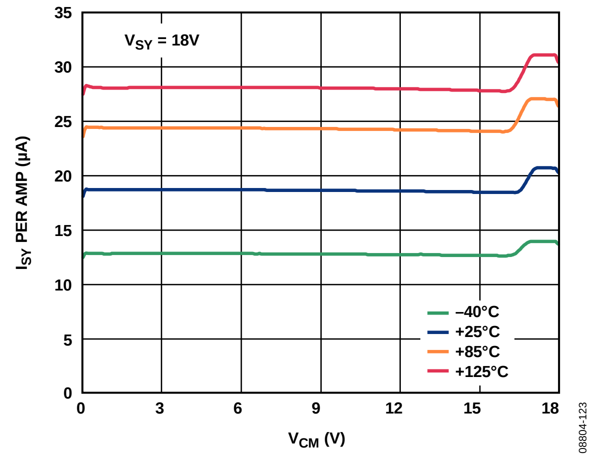


Figure 26. Supply Current vs. Common-Mode Voltage

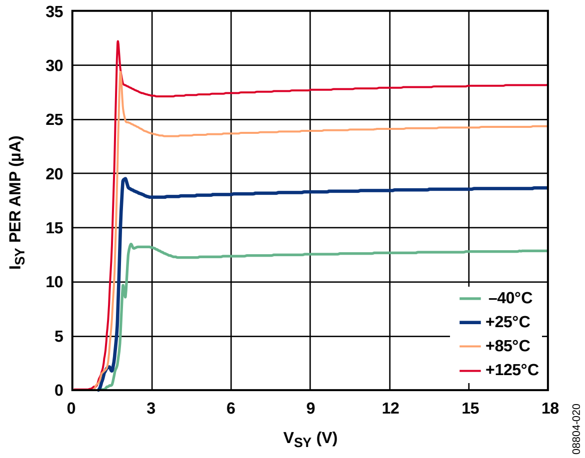


Figure 27. Supply Current vs. Supply Voltage

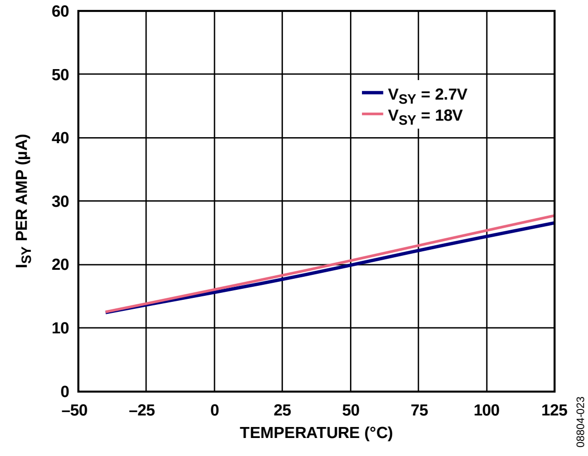


Figure 30. Supply Current vs. Temperature

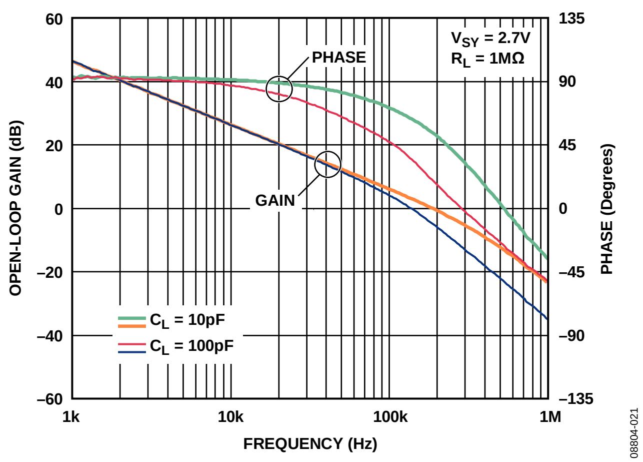


Figure 28. Open-Loop Gain and Phase vs. Frequency

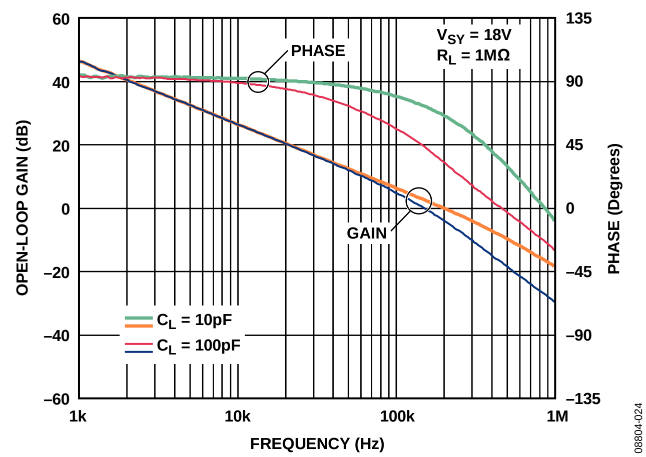


Figure 31. Open-Loop Gain and Phase vs. Frequency

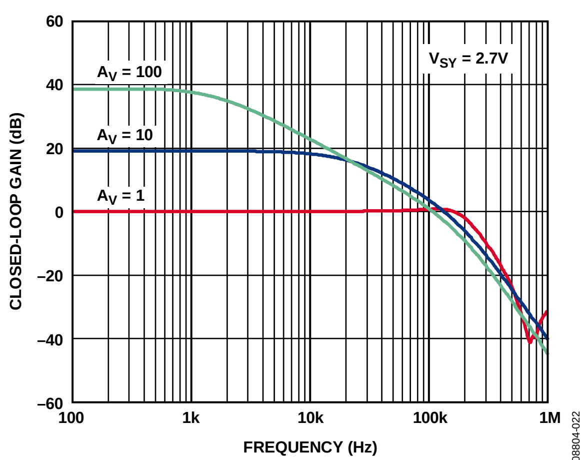


Figure 29. Closed-Loop Gain vs. Frequency

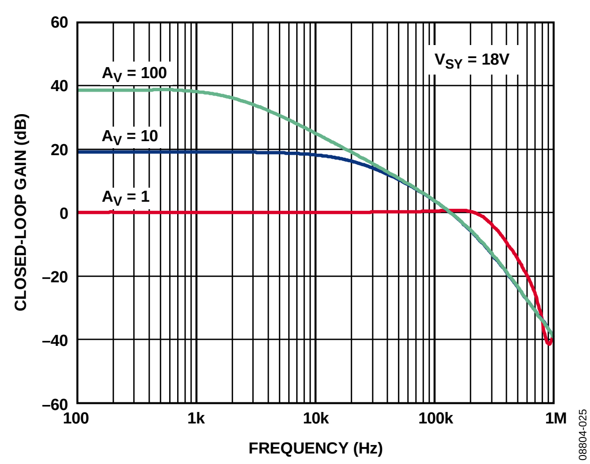


Figure 32. Closed-Loop Gain vs. Frequency

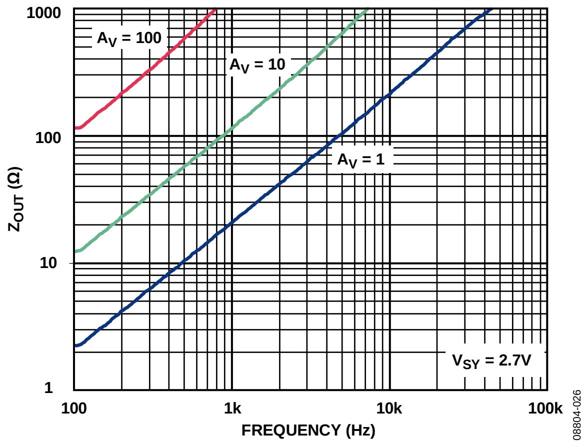


Figure 33. Output Impedance vs. Frequency

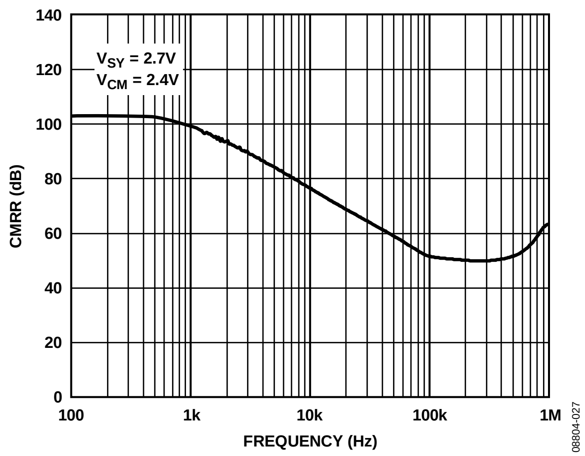


Figure 34. CMRR vs. Frequency

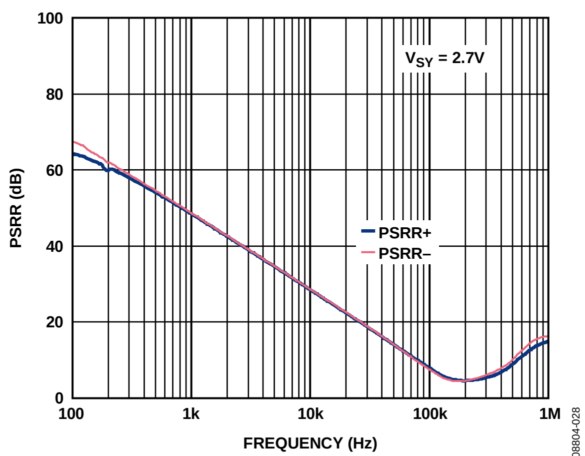


Figure 35. PSRR vs. Frequency

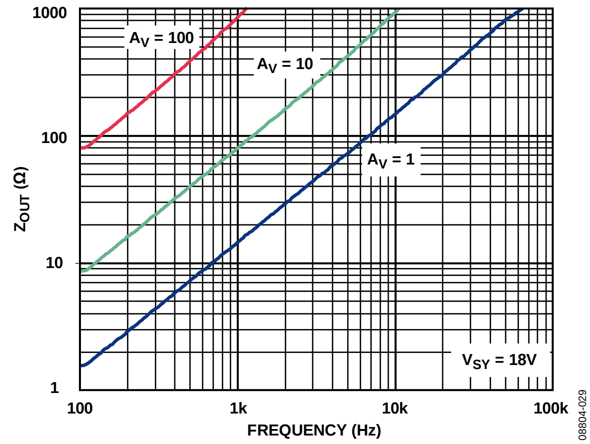


Figure 36. Output Impedance vs. Frequency

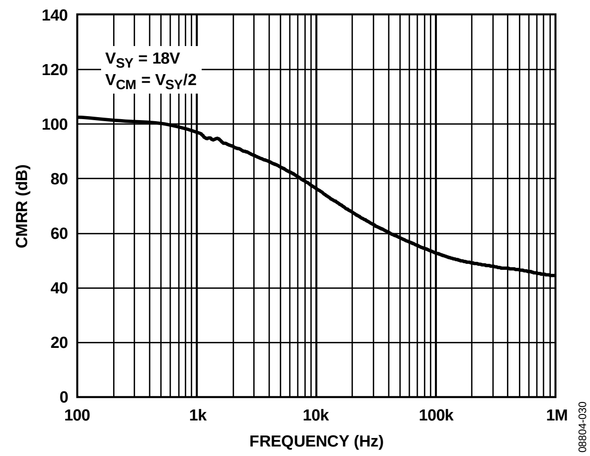


Figure 37. CMRR vs. Frequency

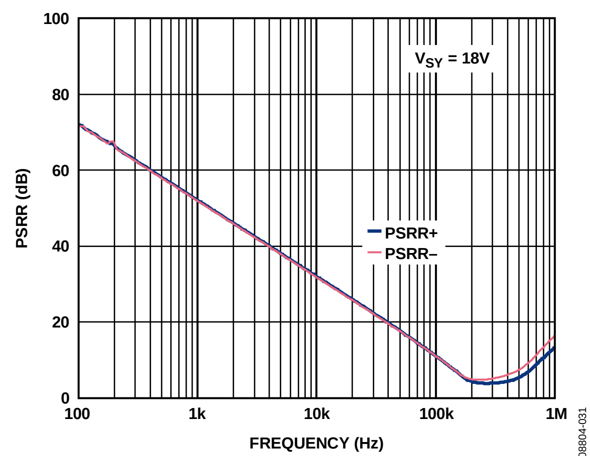


Figure 38. PSRR vs. Frequency

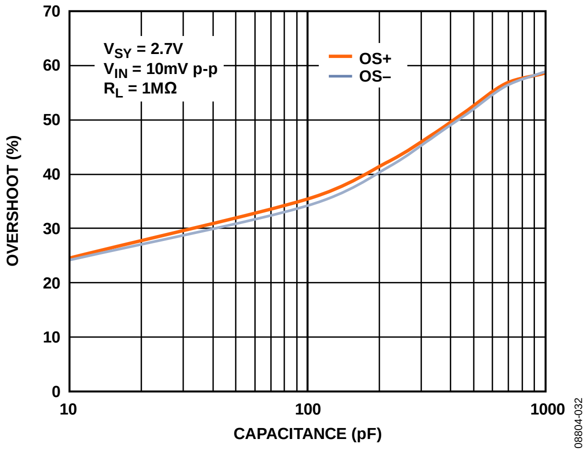


Figure 39. Small Signal Overshoot vs. Load Capacitance

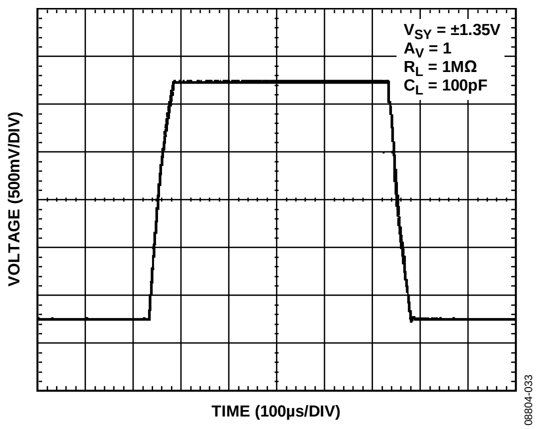


Figure 40. Large Signal Transient Response

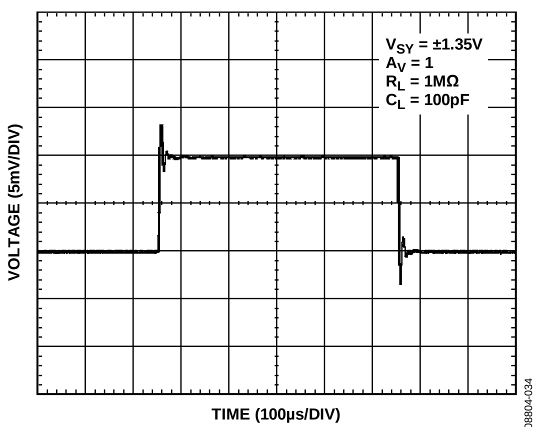


Figure 41. Small Signal Transient Response

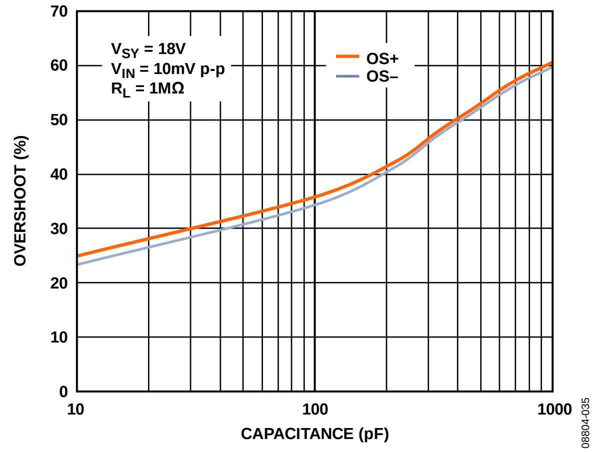


Figure 42. Small Signal Overshoot vs. Load Capacitance

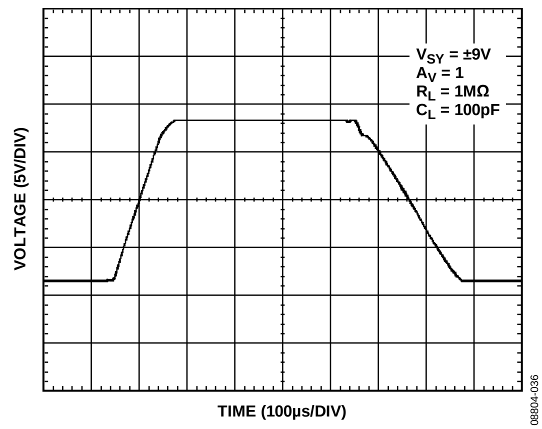


Figure 43. Large Signal Transient Response

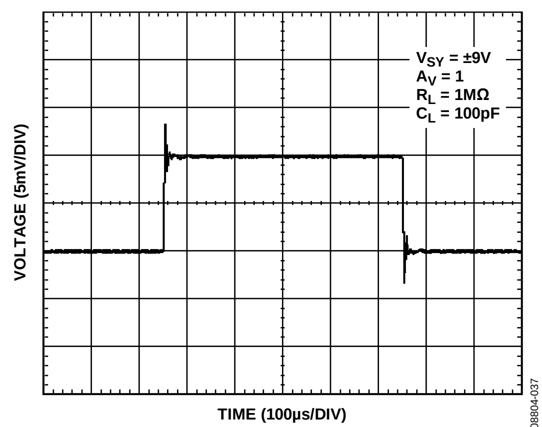


Figure 44. Small Signal Transient Response

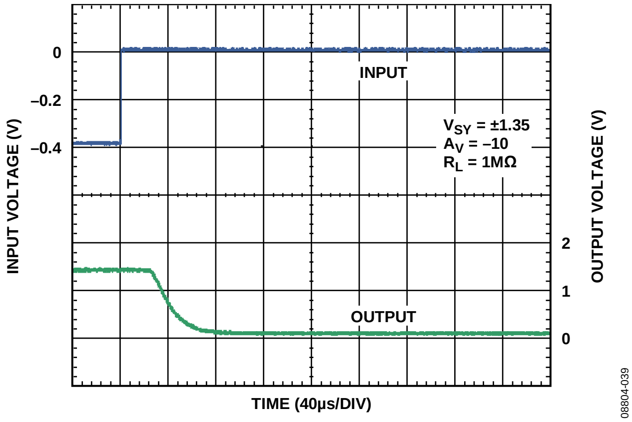


Figure 45. Positive Overload Recovery

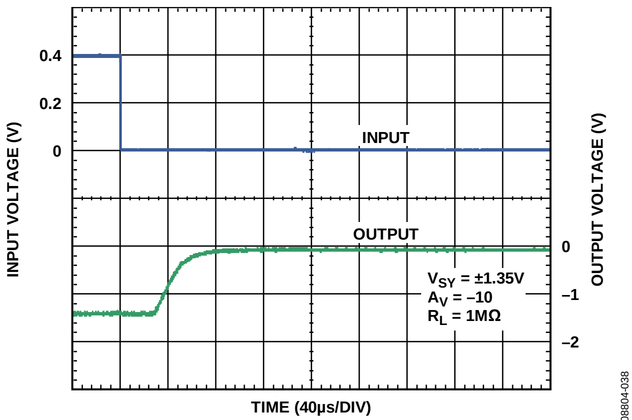


Figure 46. Negative Overload Recovery

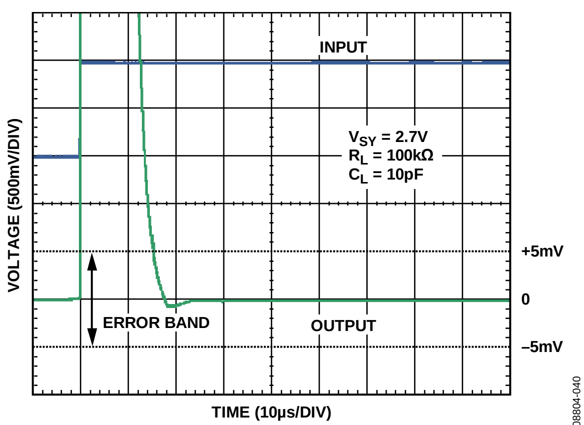


Figure 47. Positive Settling Time to 0.1%

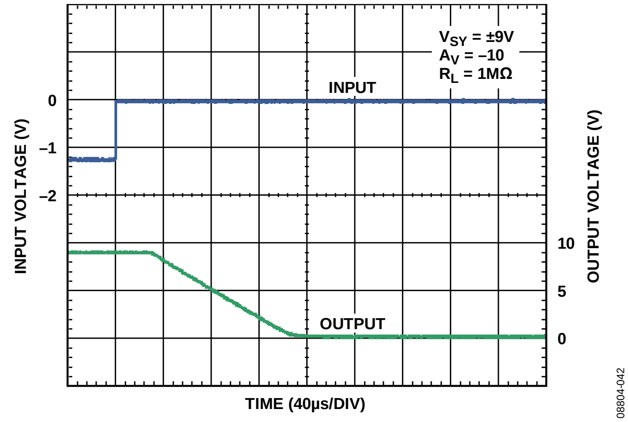


Figure 48. Positive Overload Recovery

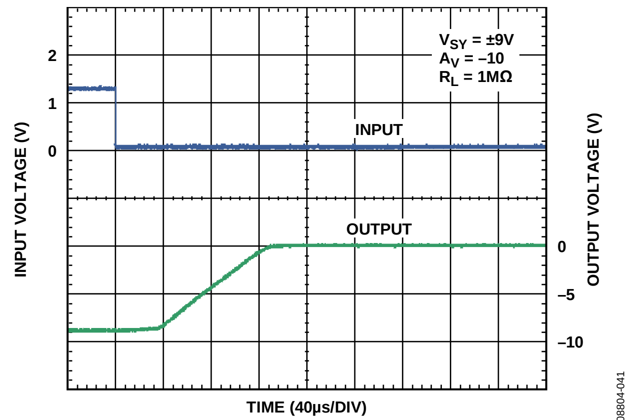


Figure 49. Negative Overload Recovery

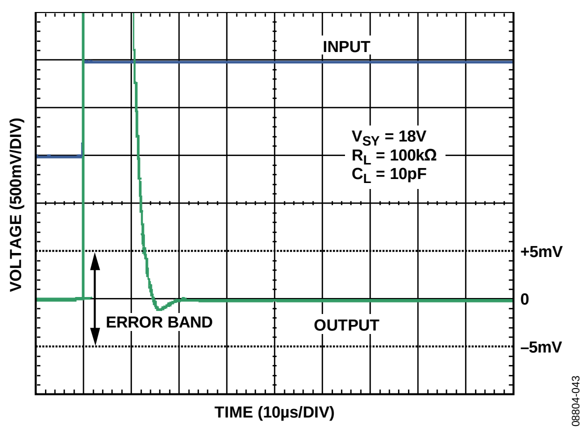


Figure 50. Positive Settling Time to 0.1%

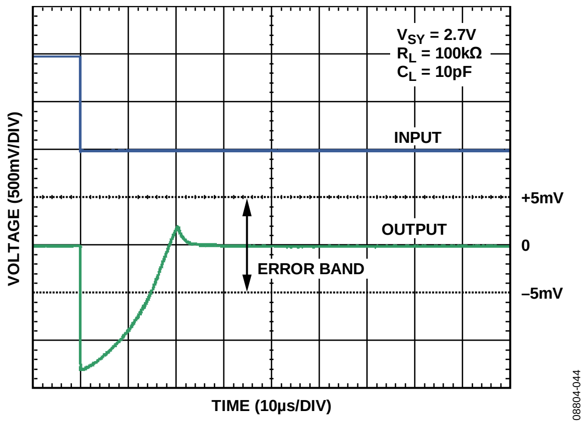


Figure 51. Negative Settling Time to 0.1%

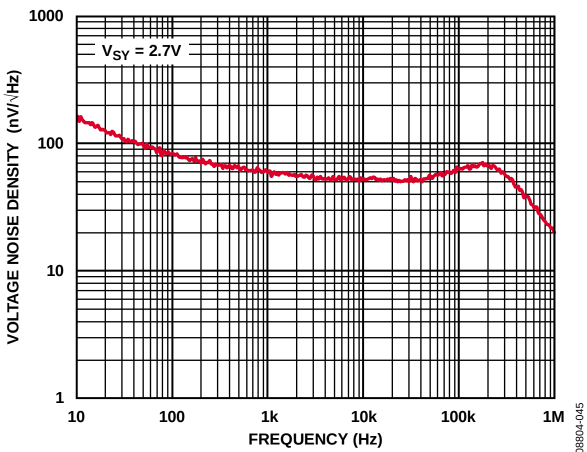


Figure 52. Voltage Noise Density vs. Frequency

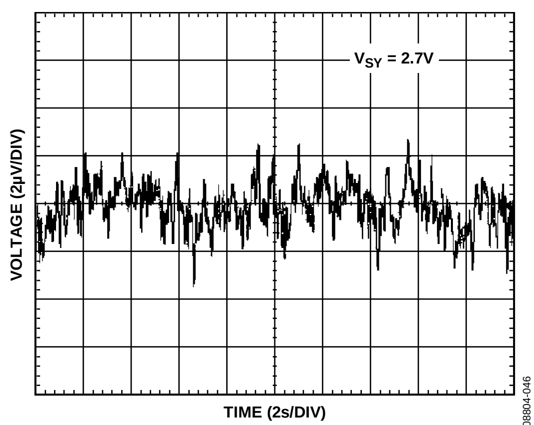


Figure 53. 0.1 Hz to 10 Hz Noise

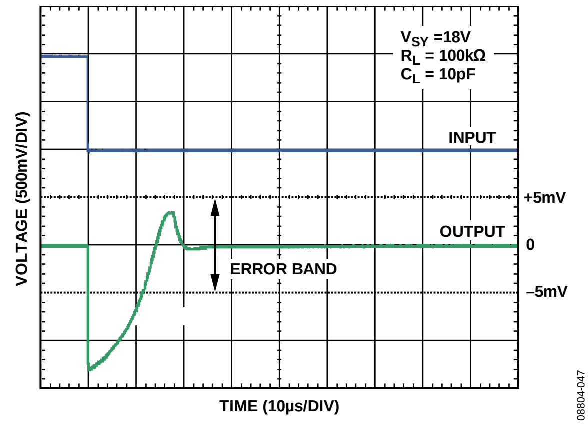


Figure 54. Negative Settling Time to 0.1%

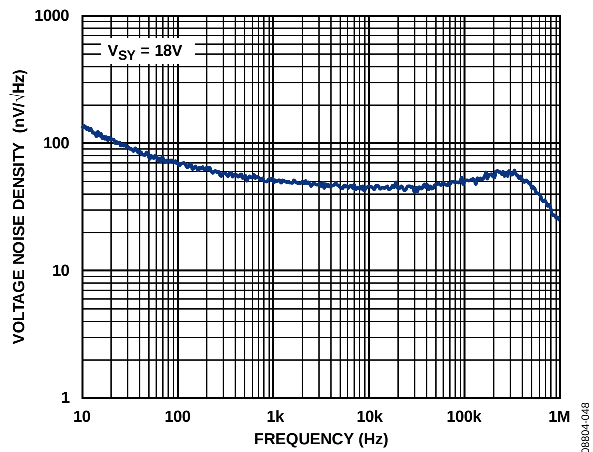


Figure 55. Voltage Noise Density vs. Frequency

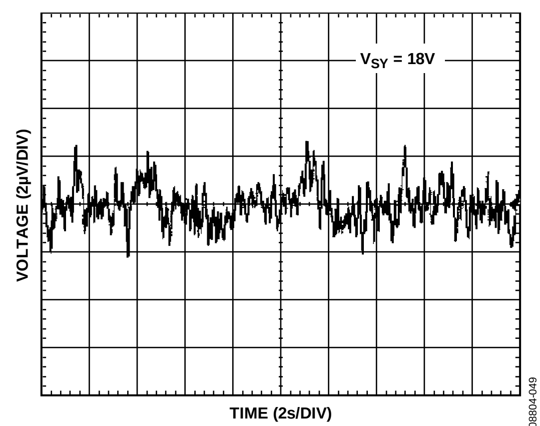


Figure 56. 0.1 Hz to 10 Hz Noise

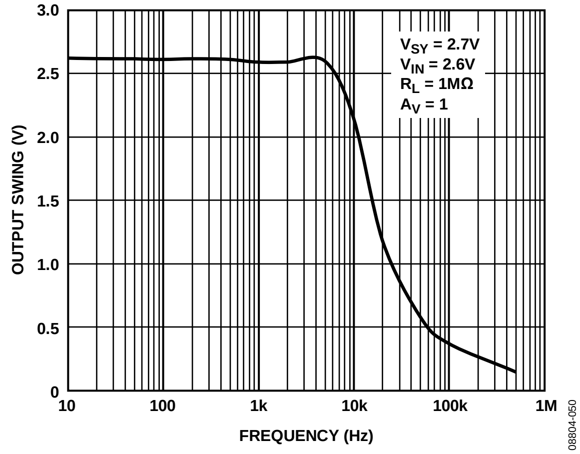


Figure 57. Output Swing vs. Frequency

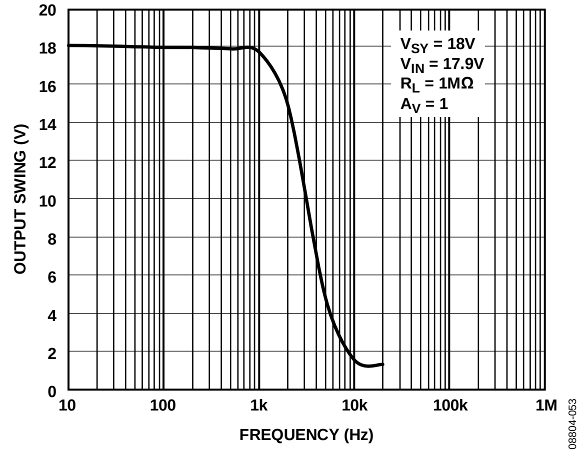


Figure 60. Output Swing vs. Frequency

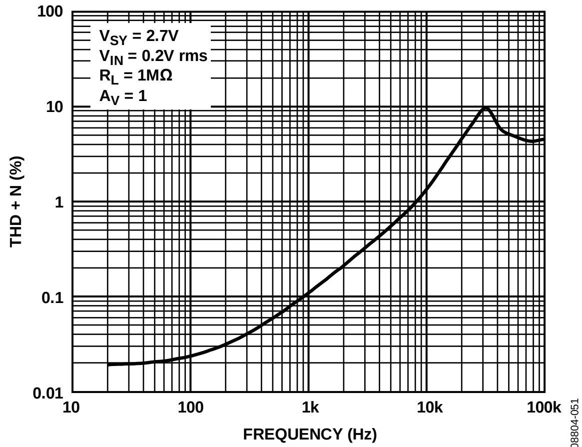


Figure 58. THD + N vs. Frequency

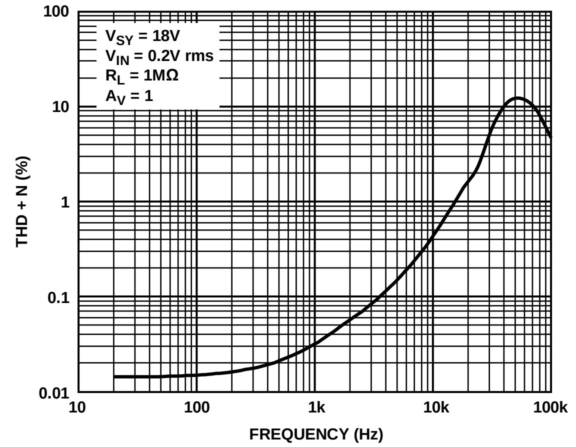


Figure 61. THD + N vs. Frequency

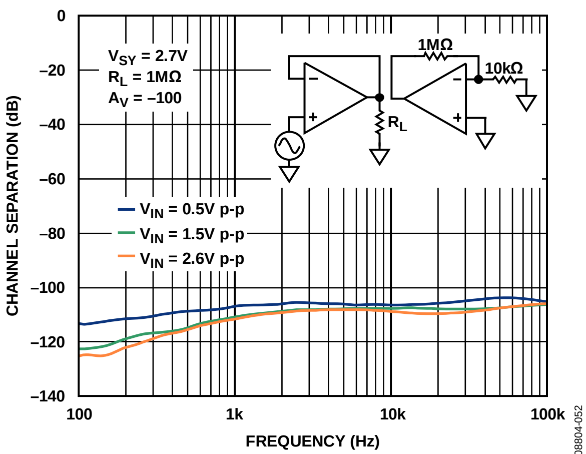


Figure 59. Channel Separation vs. Frequency

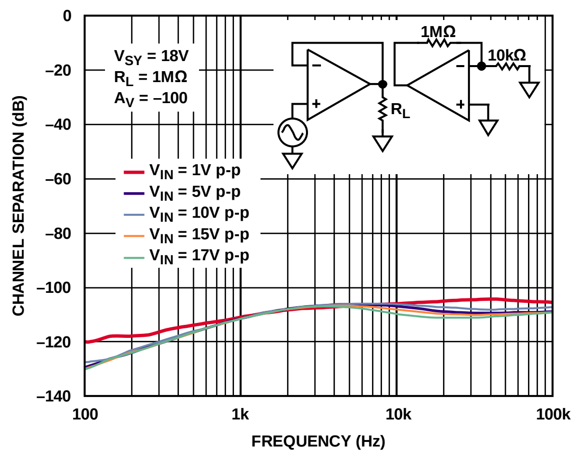


Figure 62. Channel Separation vs. Frequency

APPLICATIONS INFORMATION

The AD8657 is a low power, rail-to-rail input and output precision CMOS amplifier that operates over a wide supply voltage range of 2.7 V to 18 V. This amplifier uses the Analog Devices DigiTrim technique to achieve a higher degree of precision than is available from other CMOS amplifiers. The DigiTrim technique is a method of trimming the offset voltage of an amplifier after assembly. The advantage of postpackage trimming is that it corrects any shifts in offset voltage caused by mechanical stresses of assembly.

The AD8657 also employs unique input and output stages to achieve a rail-to-rail input and output range with a very low supply current.

INPUT STAGE

Figure 63 shows the simplified schematic of the AD8657. The input stage comprises two differential transistor pairs, an NMOS pair (M1, M2) and a PMOS pair (M3, M4). The input common-mode voltage determines which differential pair turns on and is more active than the other.

The PMOS differential pair is active when the input voltage approaches and reaches the lower supply rail. The NMOS pair is needed for input voltages up to and including the upper supply rail. This topology allows the amplifier to maintain a wide dynamic input voltage range and to maximize signal swing to both supply rails.

For the majority of the input common-mode voltage range, the PMOS differential pair is active. Differential pairs commonly exhibit different offset voltages. The handoff from one pair to the other creates a step-like characteristic that is visible in the V_{OS} vs. V_{CM} graph (see Figure 5 and Figure 8). This is inherent in all rail-to-rail amplifiers that use the dual differential pair topology. Therefore, always choose a common-mode voltage that does not include the region of handoff from one input differential pair to the other.

Additional steps in the V_{OS} vs. V_{CM} curves are also visible as the input common-mode voltage approaches the power supply rails. These changes are a result of the load transistors (M8, M9, M14, and M15) running out of headroom. As the load transistors are forced into the triode region of operation, the mismatch of their drain impedances contributes to the offset voltage of the amplifier. This problem is exacerbated at high temperatures due to the decrease in the threshold voltage of the input transistors (see Figure 9, Figure 10, Figure 12, and Figure 13 for typical performance data).

Current Source I1 drives the PMOS transistor pair. As the input common-mode voltage approaches the upper rail, I1 is steered away from the PMOS differential pair through the M5 transistor. The bias voltage, VB1, controls the point where this transfer occurs. M5 diverts the tail current into a current mirror consisting of the M6 and M7 transistors. The output of the current mirror then drives the NMOS pair. Note that the activation of this current mirror causes a slight increase in supply current at high common-mode voltages (see Figure 23 and Figure 26 for more details).

The AD8657 achieves its high performance by using low voltage MOS devices for its differential inputs. These low voltage MOS devices offer excellent noise and bandwidth per unit of current. Each differential input pair is protected by proprietary regulation circuitry (not shown in the simplified schematic). The regulation circuitry consists of a combination of active devices that maintain the proper voltages across the input pairs during normal operation and passive clamping devices that protect the amplifier during fast transients. However, these passive clamping devices begin to forward bias as the common-mode voltage approaches either power supply rail. This causes an increase in the input bias current (see Figure 15 and Figure 18).

The input devices are also protected from large differential input voltages by clamp diodes (D1 and D2). These diodes are buffered from the inputs with two 10 kΩ resistors (R1 and R2). The differential diodes turn on whenever the differential voltage exceeds approximately 600 mV; in this condition, the differential input resistance drops to 20 kΩ.

OUTPUT STAGE

The AD8657 features a complementary output stage consisting of the M16 and M17 transistors. These transistors are configured in Class AB topology and are biased by the voltage source, VB2. This topology allows the output voltage to go within millivolts of the supply rails, achieving a rail-to-rail output swing. The output voltage is limited by the output impedance of the transistors, which are low R_{ON} MOS devices. The output voltage swing is a function of the load current and can be estimated using the output voltage to the supply rail vs. load current diagrams (see Figure 16, Figure 17, Figure 19, and Figure 20).

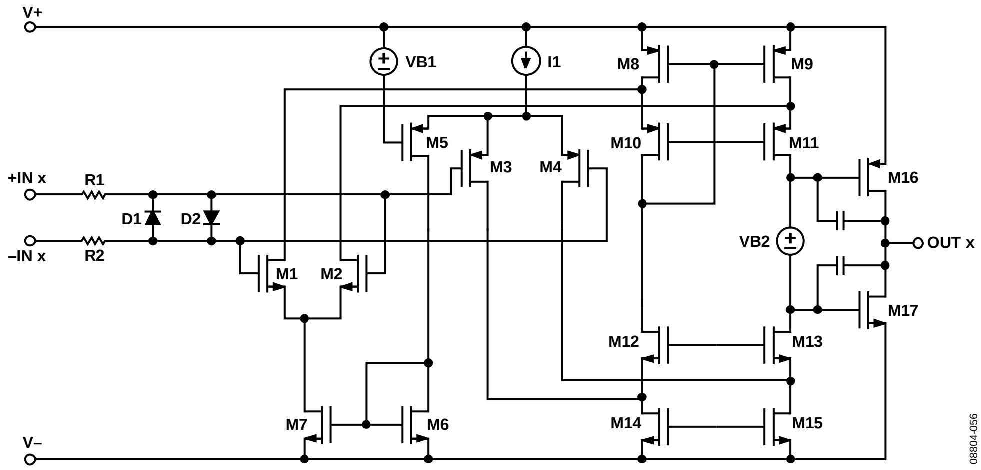


Figure 63. Simplified Schematic

RAIL TO RAIL

The AD8657 features rail-to-rail input and output with a supply voltage from 2.7 V to 18 V. Figure 64 shows the input and output waveforms of the AD8657 configured as a unity-gain buffer with a supply voltage of ±9 V and a resistive load of 1 MΩ. With an input voltage of ±9 V, the AD8657 allows the output to swing very close to both rails. Additionally, it does not exhibit phase reversal.

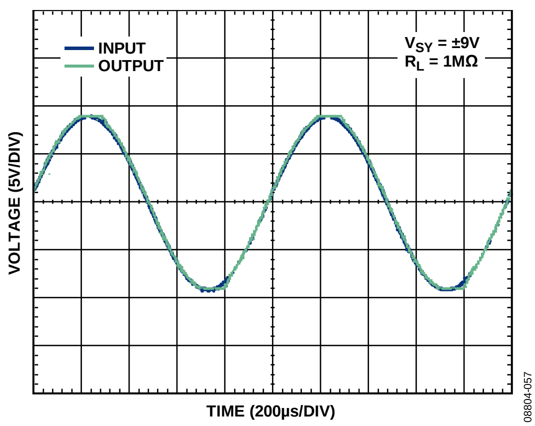


Figure 64. Rail-to-Rail Input and Output

RESISTIVE LOAD

The feedback resistor alters the load resistance that an amplifier sees. It is, therefore, important to be aware of the value of feedback resistors chosen for use with the AD8657. The AD8657 is capable of driving resistive loads down to 100 kΩ. The following two examples, inverting and noninverting configurations, show how the feedback resistor changes the actual load resistance seen at the output of the amplifier.

Inverting Configuration

Figure 65 shows AD8657 in an inverting configuration with a resistive load, R_L, at the output. The actual load seen by the amplifier is the parallel combination of the feedback resistor, R2, and load, R_L. Having a feedback resistor of 1 kΩ and a load of 1 MΩ results in an equivalent load resistance of 999 Ω at the output. In this condition, the AD8657 is incapable of driving such a heavy load; therefore, its performance degrades greatly. To avoid loading the output, use a larger feedback resistor, but consider the resistor thermal noise effect on the overall circuit.

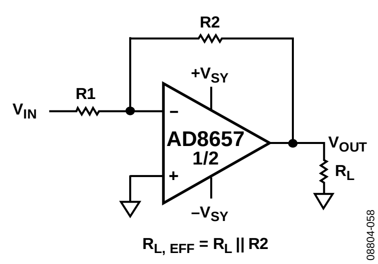


Figure 65. Inverting Op Amp

Noninverting Configuration

Figure 66 shows the AD8657 in a noninverting configuration with a resistive load, R_L, at the output. The actual load seen by the amplifier is the parallel combination of R1 + R2 and R_L.

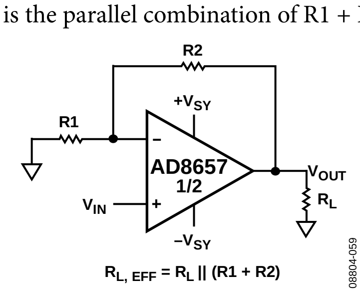


Figure 66. Noninverting Op Amp

COMPARATOR OPERATION

Op amps are designed to operate in a closed-loop configuration with feedback from its output to its inverting input. Figure 67 shows the AD8657 configured as a voltage follower with an input voltage that is always kept at midpoint of the power supplies. The same configuration is applied to the unused channel. A1 and A2 indicate the placement of ammeters to measure supply current. $I_{SY}+$ refers to the current flowing from the upper supply rail to the op amp, and $I_{SY}-$ refers to the current flowing from the op amp to the lower supply rail. As shown in Figure 68, as expected, in normal operating condition, the total current flowing into the op amp is equivalent to the total current flowing out of the op amp, where, $I_{SY}+ = I_{SY}- = 36$ µA for the dual AD8657 at $V_{SY} = 18$ V.

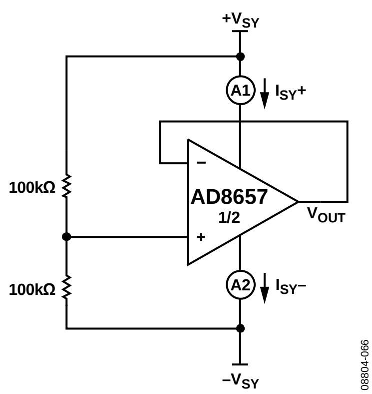


Figure 67. Voltage Follower

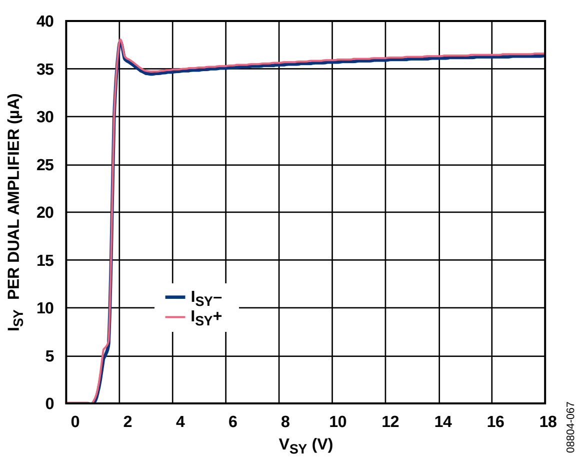


Figure 68. Supply Current vs. Supply Voltage (Voltage Follower)

In contrast to op amps, comparators are designed to work in an open-loop configuration and to drive logic circuits. Although op amps are different from comparators, occasionally an unused section of a dual op amp is used as a comparator to save board space and cost; however, this is not recommended.

Figure 69 and Figure 70 show the AD8657 configured as a comparator, with 100 kΩ resistors in series with the input pins. Any unused channels are configured as buffers with the input voltage kept at the midpoint of the power supplies. The AD8657 has input devices that are protected from large differential input voltages by Diode D1 and Diode D2 (refer to Figure 63). These diodes consist of substrate PNP bipolar transistors, and conduct whenever the differential input voltage exceeds approximately 600 mV; however, these diodes also allow a current path from the input to the lower supply rail, thus resulting in an increase in the total supply current of the system. As shown in Figure 71, both configurations yield the same result. At 18 V of power supply, $I_{SY}+$ remains at 36 µA per dual amplifier, but $I_{SY}-$ increases to 140 µA in magnitude per dual amplifier.

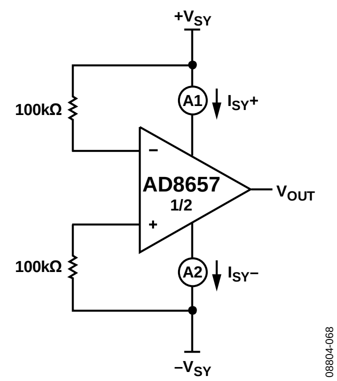


Figure 69. Comparator A

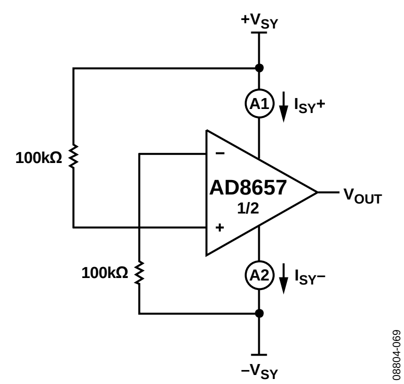


Figure 70. Comparator B

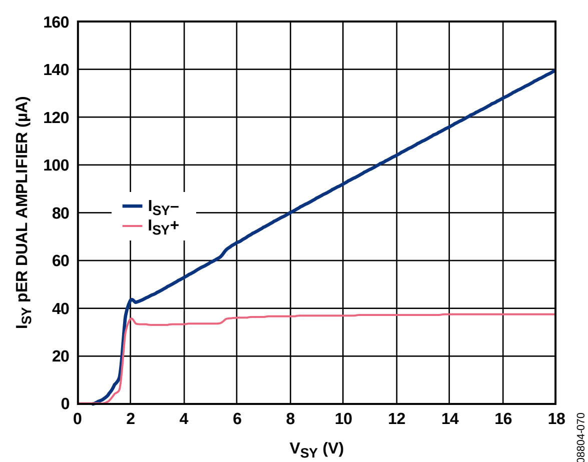


Figure 71. Supply Current vs. Supply Voltage (AD8657 as a Comparator)

Note that 100 kΩ resistors are used in series with the input of the op amp. If smaller resistor values are used, the supply current of the system increases much more. For more details on op amps as comparators, refer to the AN-849 Application Note *Using Op Amps as Comparators*.

EMI REJECTION RATIO

Circuit performance is often adversely affected by high frequency electromagnetic interference (EMI). In the event where signal strength is low and transmission lines are long, an op amp must accurately amplify the input signals. However, all op amp pins—the noninverting input, inverting input, positive supply, negative supply, and output pins—are susceptible to EMI signals. These high frequency signals are coupled into an op amp by various means such as conduction, near field radiation, or far field radiation. For instance, wires and PCB traces can act as antennas and pick up high frequency EMI signals.

Precision op amps, such as the AD8657, do not amplify EMI or RF signals because of their relatively low bandwidth. However, due to the nonlinearities of the input devices, op amps can rectify these out-of-band signals. When these high frequency signals are rectified, they appear as a dc offset at the output.

To describe the ability of the AD8657 to perform as intended in the presence of an electromagnetic energy, the electromagnetic interference rejection ratio (EMIRR) of the noninverting pin is specified in Table 2, Table 3, and Table 4 of the Specifications section. A mathematical method of measuring EMIRR is defined as follows:

$$EMIRR = 20 \log (V_{IN\_PEAK}/\Delta V_{OS})$$

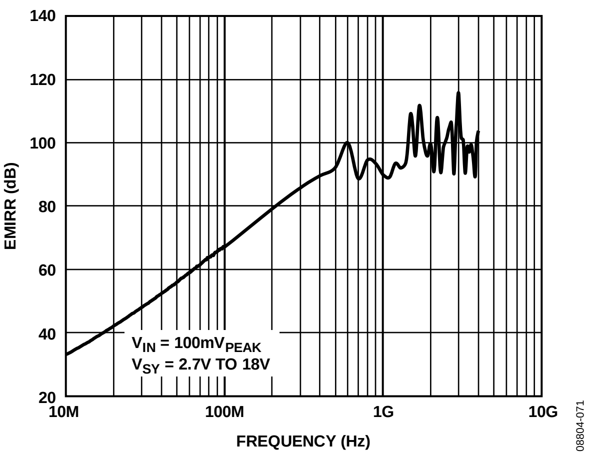


Figure 72. EMIRR vs. Frequency

4 mA TO 20 mA PROCESS CONTROL CURRENT LOOP TRANSMITTER

The 2-wire current transmitters are often used in distributed control systems and process control applications to transmit analog signals between sensors and process controllers. Figure 73 shows a 4 mA to 20 mA current loop transmitter.

The transmitter powers directly from the control loop power supply, and the current in the loop carries signal from 4 mA to 20 mA. Thus, 4 mA establishes the baseline current budget within which the circuit must operate. Using the AD8657 is an excellent choice due to its low supply current of 33 µA per amplifier over temperature and supply voltage. The current transmitter controls the current flowing in the loop, where a zero-scale input signal is represented by 4 mA of current and a full-scale input signal is represented by 20 mA. The transmitter also floats from the control loop power supply, V_{DD}, while signal ground is in the receiver. The loop current is measured at the load resistor, R_L, at the receiver side.

With a zero-scale input, a current of V_{REF}/R_{NULL} flows through R´. This creates a current flowing through the sense resistor, I_{SENSE}, determined by the following equation (see Figure 73 for details):

$$I_{SENSE,\ MIN} = (V_{REF} \times R')/(R_{NULL} \times R_{SENSE})$$

With a full-scale input voltage, current flowing through R´ is increased by the full-scale change in V_{IN}/R_{SPAN}. This creates an increase in the current flowing through the sense resistor.

$$I_{SENSE,\ DELTA} = (Full\text{-}Scale\ Change\ in\ V_{IN} \times R')/(R_{SPAN} \times R_{SENSE})$$

Therefore

$$I_{SENSE,\ MAX} = I_{SENSE,\ MIN} + I_{SENSE,\ DELTA}$$

When R´ >> R_{SENSE}, the current through the load resistor at the receiver side is almost equivalent to I_{SENSE}.

Figure 73 is designed for a full-scale input voltage of 5 V. At 0 V of input, loop current is 3.5 mA, and at a full scale of 5 V, the loop current is 21 mA. This allows software calibration to fine tune the current loop to the 4 mA to 20 mA range.

The AD8657 and ADR125 both consume only 160 µA quiescent current, making 3.34 mA current available to power additional signal conditioning circuitry or to power a bridge circuit.

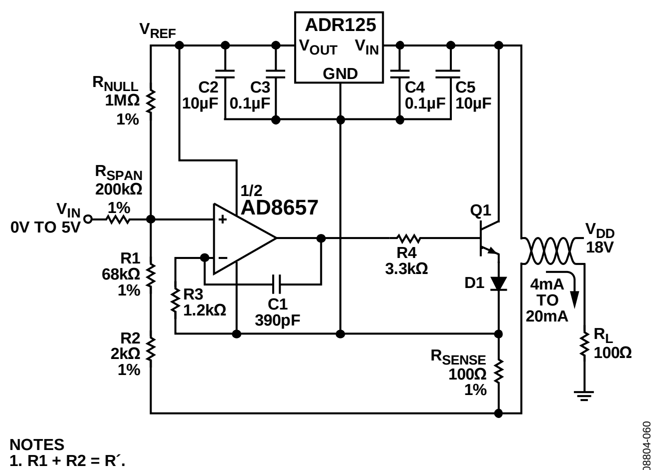


Figure 73. 4 mA to 20 mA Current Loop Transmitter

OUTLINE DIMENSIONS

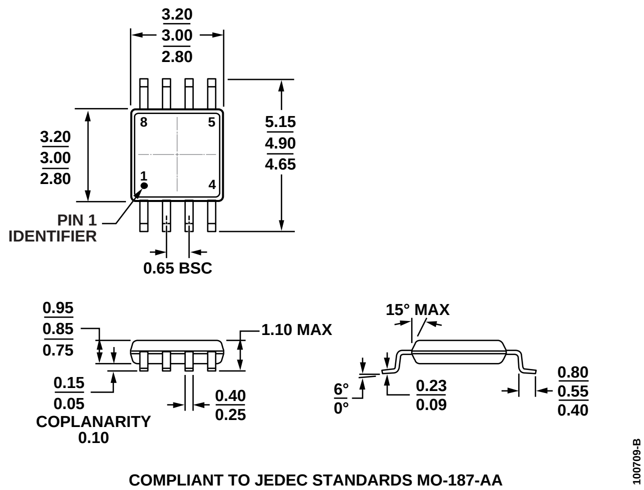


Figure 74. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

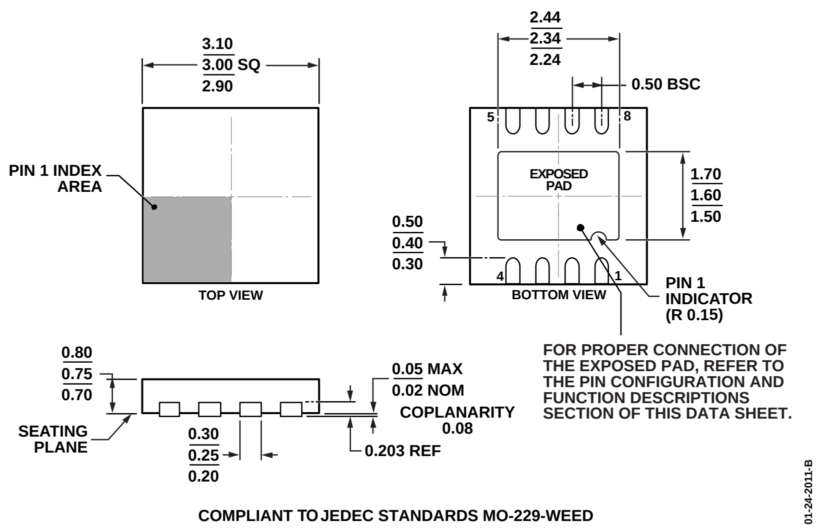


Figure 75. 8-Lead Lead Frame Chip Scale Package [LFCSP_WD]
3 mm × 3 mm Body, Very Very Thin, Dual Lead
(CP-8-11)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
AD8657ARMZ	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2N
AD8657ARMZ-R7	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2N
AD8657ARMZ-RL	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2N
AD8657ACPZ-R7	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-8-11	A2N
AD8657ACPZ-RL	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-8-11	A2N

[1] Z = RoHS Compliant Part.

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