Quad 12-Bit Serial Voltage Output DAC

DAC8420

FEATURES

Guaranteed monotonic over temperature
Excellent matching between DACs
Unipolar or bipolar operation
Buffered voltage outputs
High speed serial digital interface
Reset-to-zero scale or midscale
Wide supply range, +5 V only to ±15 V
Low power consumption (35 mW maximum)
Available in 16-Lead PDIP, SOIC, and CERDIP packages

APPLICATIONS

Software controlled calibration
Servo controls
Process control and automation
ATE

FUNCTIONAL BLOCK DIAGRAM

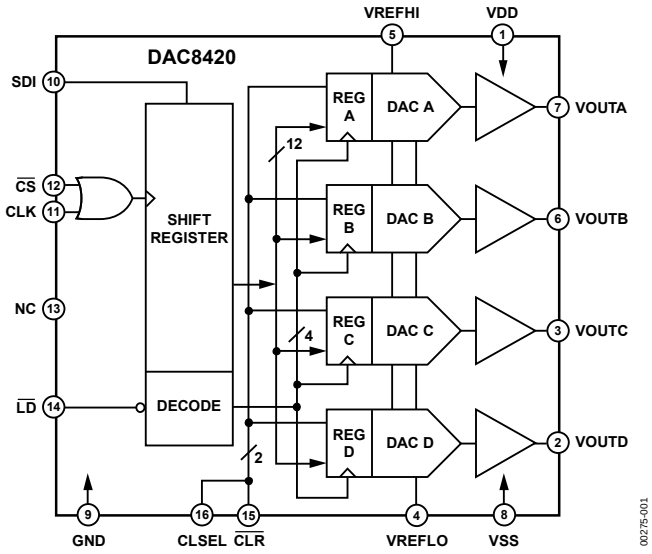

Figure 1.

GENERAL DESCRIPTION

The DAC8420 is a quad, 12-bit voltage-output DAC with serial digital interface in a 16-lead package. Utilizing BiCMOS technology, this monolithic device features unusually high circuit density and low power consumption. The simple, easy-to-use serial digital input and fully buffered analog voltage outputs require no external components to achieve a specified performance.

The 3-wire serial digital input is easily interfaced to microprocessors running at 10 MHz with minimal additional circuitry. Each DAC is addressed individually by a 16-bit serial word consisting of a 12-bit data word and an address header. The user-programmable reset control $\overline{CLR}$ forces all four DAC outputs to either zero scale or midscale, asynchronously overriding the current DAC register values. The output voltage range, determined by the inputs VREFHI and VREFLO, is set by the user for positive or negative unipolar or bipolar signal swings within the supplies, allowing considerable design flexibility.

The DAC8420 is available in 16-lead PDIP, SOIC, and CERDIP packages. Operation is specified with supplies ranging from +5 V only to ±15 V, with references of +2.5 V to ±10 V, respectively. Power dissipation when operating from ±15 V supplies is less than 255 mW (maximum) and only 35 mW (maximum) with a +5 V supply.

Rev. B

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9/03—Rev. 0 to Rev. A

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Updated Ordering Guide ... 4
Added Power-Up Sequence section ... 12
Updated Outline Dimensions ... 17

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS[1]

@ V_{DD} = +5.0 V ± 5%, V_{SS} = 0 V, V_{VREFHI} = +2.5 V, V_{VREFLD} = 0 V, and V_{SS} = −5.0 V ± 5%, V_{VREFLO} = −2.5 V, −40°C ≤ T_A ≤ +85°C unless otherwise noted.[2]

Table 1.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
STATIC ACCURACY						
Integral Linearity E Grade	INL			±¼	±1	LSB
Integral Linearity E Grade	INL	V_{SS} = 0 V[3]		±½	±3	LSB
Integral Linearity F Grade	INL			±¾	±2	LSB
Integral Linearity F Grade	INL	V_{SS} = 0 V[3]		±1	±4	LSB
Differential Linearity	DNL	Monotonic over temperature		±¼	±1	LSB
Zero-Scale Error	ZSE	R_L = 2 kΩ, V_{SS} = −5 V			±4	LSB
Full-Scale Error	FSE	R_L = 2 kΩ, V_{SS} = −5 V			±4	LSB
Zero-Scale Error	ZSE	R_L = 2 kΩ, V_{SS} = 0 V[3]			±8	LSB
Full-Scale Error	FSE	R_L = 2 kΩ, V_{SS} = 0 V[3]			±8	LSB
Zero-Scale Temperature Coefficient	TC_{ZSE}	R_L = 2 kΩ, V_{SS} = −5 V[4]		±10		ppm/°C
Full-Scale Temperature Coefficient	TC_{FSE}	R_L = 2 kΩ, V_{SS} = −5 V[4]		±10		ppm/°C
MATCHING PERFORMANCE						
Linearity Matching				±1		LSB
REFERENCE						
Positive Reference Input Range[5]	V_{VREFHI}		V_{VREFLO} + 2.5		V_{DD} − 2.5	V
Negative Reference Input Range[5]	V_{VREFLO}		V_{SS}		V_{VREFHI} − 2.5	V
Negative Reference Input Range	V_{VREFLO}	V_{SS} = 0 V[5]	0		V_{VREFHI} − 2.5	V
Reference High Input Current	I_{VREFHI}	Code 0x000, Code 0x555	−0.75	±0.25	+0.75	mA
Reference Low Input Current	I_{VREFLO}	Code 0x000, Code 0x555, V_{SS} = −5 V	−1.0	−0.6		mA
AMPLIFIER CHARACTERISTICS						
Output Current	I_{OUT}	V_{SS} = −5 V	−1.25		+1.25	mA
Settling Time	t_S	To 0.01%[6]		8		µs
Slew Rate	SR	10% to 90%[6]		1.5		V/µs
LOGIC CHARACTERISTICS						
Logic Input High Voltage	V_{INH}		2.4			V
Logic Input Low Voltage	V_{INL}				0.8	V
Logic Input Current	I_{IN}				10	µA
Input Capacitance[4]	C_{IN}			13		pF
LOGIC TIMING CHARACTERISTICS[4, 7]						
Data Setup Time	t_{DS}		25			ns
Data Hold	t_{DH}		55			ns
Clock Pulse Width High	t_{CH}		90			ns
Clock Pulse Width Low	t_{CL}		120			ns
Select Time	t_{CSS}		90			ns
Deselect Delay	t_{CSH}		5			ns
Load Disable Time	t_{LD1}		130			ns
Load Delay	t_{LD2}		35			ns
Load Pulse Width	t_{LDW}		80			ns
Clear Pulse Width	t_{CLRW}		150			ns

Parameter	Symbol	Condition	Min	Typ	Max	Unit
SUPPLY CHARACTERISTICS						
Power Supply Sensitivity	PSRR			0.002	0.01	%/%
Positive Supply Current	I_{DD}			4	7	mA
Negative Supply Current	I_{SS}		−6	−3		mA
Power Dissipation	P_{DISS}	V_{SS} = 0 V		20	35	mW

[1] Typical values indicate performance measured at 25°C.
[2] All supplies can be varied ±5% and operation is guaranteed. Device is tested with V_{DD} = 4.75 V.
[3] For single-supply operation (V_{VREFLO} = 0 V, V_{SS} = 0 V), due to internal offset errors INL and DNL are measured beginning at Code 0x005.
[4] Guaranteed, but not tested.
[5] Operation is guaranteed over this reference range, but linearity is neither tested nor guaranteed.
[6] V_{OUT} swing between +2.5 V and −2.5 V with V_{DD} = 5.0 V.
[7] All input control signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

@ V_{DD} = +15.0 V ± 5%, V_{SS} = −15.0 V ± 5%, V_{VREFHI} = +10.0 V, V_{VREFLO} = −10.0 V, −40°C ≤ T_A ≤ +85°C unless otherwise noted.[1, 2]

Table 2.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
STATIC ACCURACY						
Integral Linearity E Grade	INL			±¼	±½	LSB
Integral Linearity F Grade	INL			±½	±1	LSB
Differential Linearity	DNL	Monotonic over temperature		±¼	±1	LSB
Zero-Scale Error	ZSE	R_L = 2 kΩ			±2	LSB
Full-Scale Error	FSE	R_L = 2 kΩ			±2	LSB
Zero-Scale Temperature Coefficient	TC_{ZSE}	R_L = 2 kΩ[3]		±4		ppm/°C
Full-Scale Temperature Coefficient	TC_{FSE}	R_L = 2 kΩ[3]		±4		ppm/°C
MATCHING PERFORMANCE						
Linearity Matching				±1		LSB
REFERENCE						
Positive Reference Input Range[4]	V_{VREFHI}		V_{VREFLO} + 2.5		V_{DD} − 2.5	V
Negative Reference Input Range[4]	V_{VREFLO}		−10		V_{VREFHI} − 2.5	V
Reference High Input Current	I_{VREFHI}	Code 0x000, Code 0x555	−2.0	±1.0	+2.0	mA
Reference Low Input Current	I_{VREFLO}	Code 0x000, Code 0x555	−3.5	−2.0		mA
AMPLIFIER CHARACTERISTICS						
Output Current	I_{OUT}		−5		+5	mA
Settling Time	t_S	To 0.01%[5]		13		µs
Slew Rate	SR	10% to 90%[5]		2		V/µs
DYNAMIC PERFORMANCE						
Analog Crosstalk[3]				>64		dB
Digital Feedthrough[3]				>72		dB
Large Signal Bandwidth		3 dB, V_{VREFHI} = 5 V + 10 V p-p, V_{VREFLO} = −10 V[3]		90		kHz
Glitch Impulse		Code Transition = 0x7FF to 0x800[3]		6		µV-s
LOGIC CHARACTERISTICS						
Logic Input High Voltage	V_{INH}		2.4			V
Logic Input Low Voltage	V_{INL}				0.8	V
Logic Input Current	I_{IN}				10	µA
Input Capacitance[3]	C_{IN}			13		pF
LOGIC TIMING CHARACTERISTICS[3, 6]						
Data Setup Time	t_{DS}		25			ns
Data Hold	t_{DH}		20			ns
Clock Pulse Width High	t_{CH}		30			ns
Clock Pulse Width Low	t_{CL}		50			ns
Select Time	t_{CSS}		55			ns
Deselect Delay	t_{CSH}		15			ns
Load Disable Time	t_{LD1}		40			ns
Load Delay	t_{LD2}		15			ns
Load Pulse Width	t_{LDW}		45			ns
Clear Pulse Width	t_{CLRW}		70			ns
SUPPLY CHARACTERISTICS						
Power Supply Sensitivity	PSRR			0.002	0.01	%/%
Positive Supply Current	I_{DD}			6	9	mA
Negative Supply Current	I_{SS}		−8	−5		mA
Power Dissipation	P_{DISS}				255	mW

[1] Typical values indicate performance measured at 25°C.
[2] All supplies can be varied ±5% and operation is guaranteed.
[3] Guaranteed, but not tested.
[4] Operation is guaranteed over this reference range, but linearity is neither tested nor guaranteed.
[5] V_{OUT} swing between +10 V and −10 V.
[6] All input control signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V, +18.0 V
V_{SS} to GND	+0.3 V, −18.0 V
V_{SS} to V_{DD}	−0.3 V, +36.0 V
V_{SS} to V_{VREFLO}	−0.3 V, V_{SS} − 2.0 V
V_{VREFHI} to V_{VREFLO}	+2.0 V, V_{DD} − V_{SS}
V_{VREFHI} to V_{DD}	+2.0 V, +33.0 V
I_{VREFHI}, I_{VREFLO}	10 mA
Digital Input Voltage to GND	−0.3 V, V_{DD} + 0.3 V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	
EP, FP, ES, FS, EQ, FQ	–40°C to +85°C
Dice Junction Temperature	150°C
Storage Temperature Range	–65°C to +150°C
Power Dissipation	1000 mW
Lead Temperature	JEDEC Industry Standard
Soldering	J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Table 4.

Package Type	θ_{JA}	θ_{JC}	Unit
16-Lead PDIP (N)	70[1]	27	°C/W
16-Lead CERDIP (Q)	82[1]	9	°C/W
16-Lead SOIC (RW)	86[2]	22	°C/W

[1] θ_{JA} is specified for worst case mounting conditions, that is, θ_{JA} is specified for device in socket.
[2] θ_{JA} is specified for device on board.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

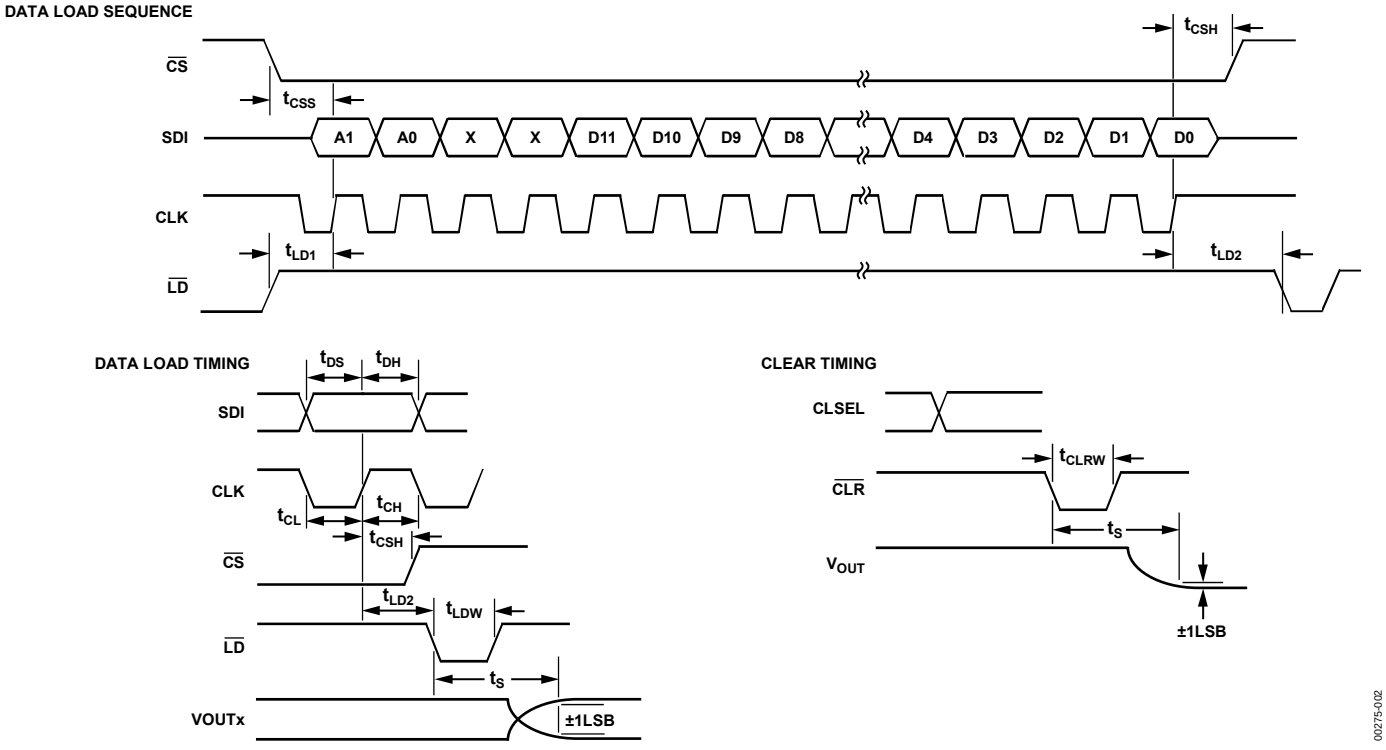


Figure 2. Timing Diagram

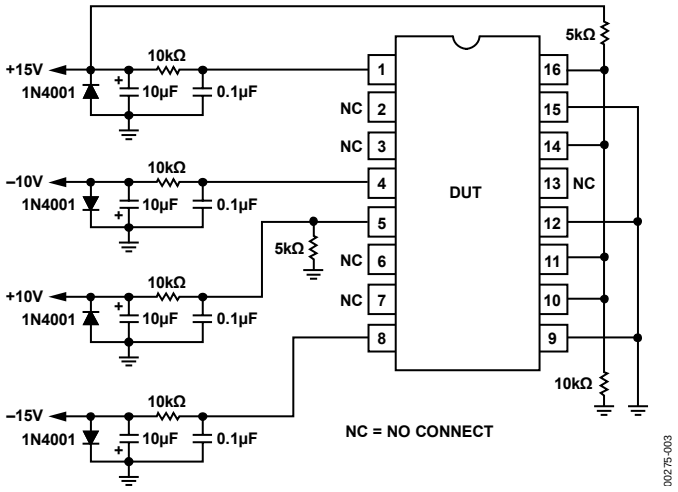


Figure 3. Burn-In Diagram

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

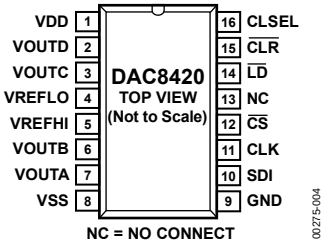


Figure 4. PDIP and CERDIP

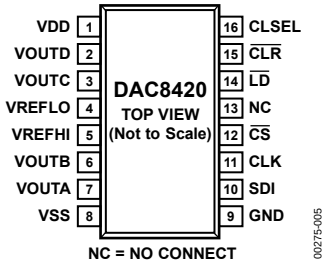


Figure 5. SOIC

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VDD	Positive Power Supply, 5 V to 15 V.
4	VREFLO	Reference Input. Lower DAC ladder reference voltage input, equal to zero-scale output. Allowable range is V_{SS} to (V_{VREFHI} − 2.5 V).
5	VREFHI	Reference Input. Upper DAC ladder reference voltage input. Allowable range is (V_{DD} − 2.5 V) to (V_{VREFLO} + 2.5 V).
7, 6, 3, 2	VOUTA through VOUTD	Buffered DAC Analog Voltage Outputs.
8	VSS	Negative Power Supply, 0 V to −15 V.
9	GND	Power Supply, Digital Ground.
10	SDI	Serial Data Input. Data presented to this pin is loaded into the internal serial-parallel shift register, which shifts data in, beginning with DAC Address Bit A1. This input is ignored when $\overline{CS}$ is high. SDI is CMOS/TTL compatible. The format of the 16-bit serial word is shown in Table 8.
11	CLK	System Serial Data Clock Input, TTL/CMOS Levels. Data presented to the input SDI is shifted into the internal serial-parallel input register on the rising edge of clock. This input is logically OR'ed with $\overline{CS}$.
12	$\overline{CS}$	Control Input, Device Chip Select, Active Low. This input is logically OR'ed with the clock and disables the serial data register input when high. When low, data input clocking is enabled (see Table 6). $\overline{CS}$ is CMOS/TTL compatible.
13	NC	No Connect = Don't Care.
14	$\overline{LD}$	Control Input, Asynchronous DAC Register Load Control, Active Low. The data currently contained in the serial input shift register is shifted out to the DAC data registers on the falling edge of $\overline{LD}$, independent of $\overline{CS}$. Input data must remain stable while $\overline{LD}$ is low. $\overline{LD}$ is CMOS/TTL compatible.
15	$\overline{CLR}$	Control Input, Asynchronous Clear, Active Low. Sets internal data Register A through Register D to zero or midscale, depending on current state of CLSEL. The data in the serial input shift register is unaffected by this control. $\overline{CLR}$ is CMOS/TTL compatible.
16	CLSEL	Control Input, Determines action of $\overline{CLR}$. If high, a clear command sets the internal DAC Register A through Register D to midscale (0x800). If low, the registers are set to zero (0x000). CLSEL is CMOS/TTL compatible.

Table 6. Control Function Logic Table

CLK[1]	$\overline{CS}$[1]	$\overline{LD}$	$\overline{CLR}$	CLSEL	Serial Input Shift Register	DAC Register A to DAC Register D
NC[2]	High	High	Low	High	No change	Loads midscale value (0x800)
NC[2]	High	High	Low	Low	No change	Loads zero-scale value (0x000)
NC[2]	High	High	↑	High /Low	No change	Latches value
↑	Low	High	High	NC[2]	Shifts register one bit	No change
Low	↑	High	High	NC[2]	Shifts register one bit	No change
High	NC (↑)[2]	↓	High	NC[2]	No change	Loads the serial data-word[3]
High	NC[2]	Low	High	NC[2]	No change	Transparent[4]
NC[2]	High	High	High	NC[2]	No change	No change

[1] CLK and $\overline{CS}$ are interchangeable.
[2] NC = Don't Care.
[3] Returning $\overline{CS}$ high while CLK is high avoids an additional false clock of serial input data. CLK and $\overline{CS}$ are interchangeable.
[4] Do not clock in serial data while $\overline{LD}$ is low.

TYPICAL PERFORMANCE CHARACTERISTICS

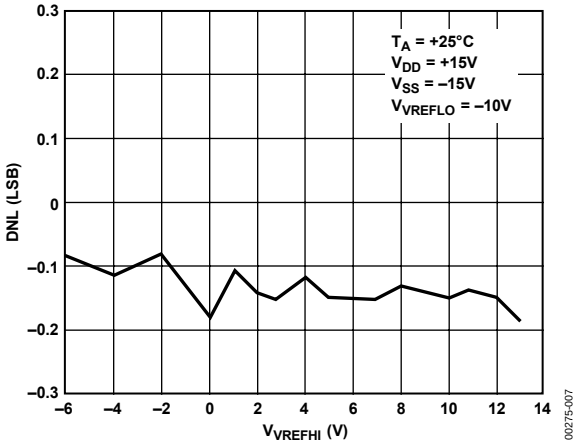


Figure 6. DNL vs. V_{VREFHI} (±15 V)

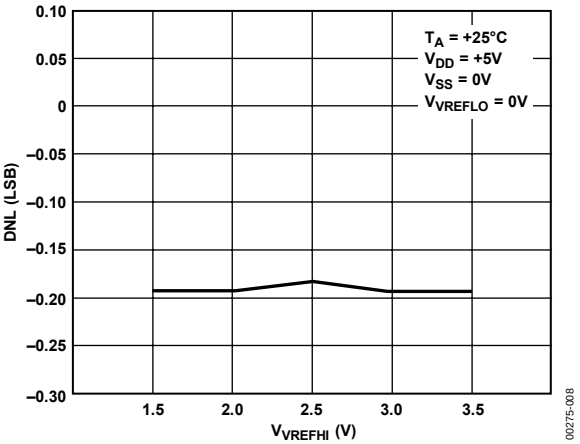


Figure 7. DNL vs. V_{VREFHI} (+5 V)

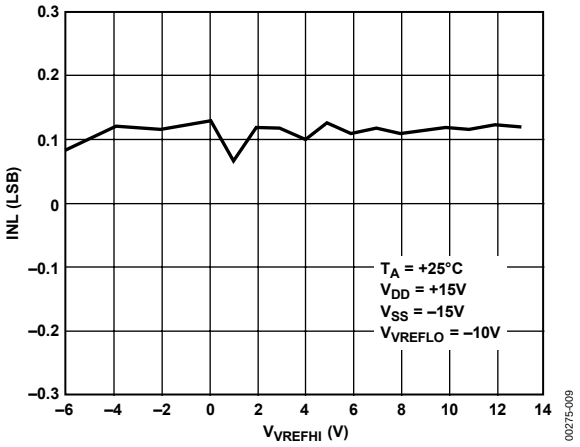


Figure 8. INL vs. VREFHI (±15 V)

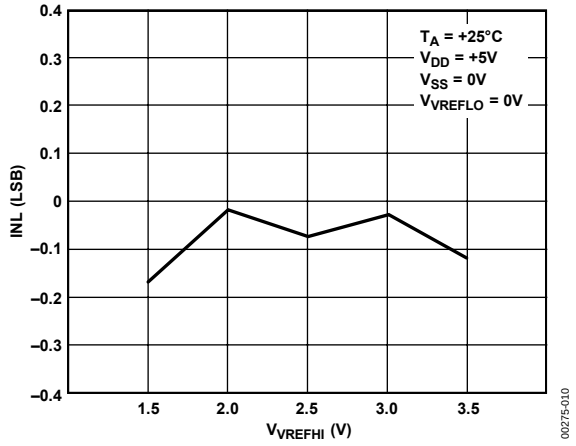


Figure 9. INL vs. V_{VREFHI} (+5 V)

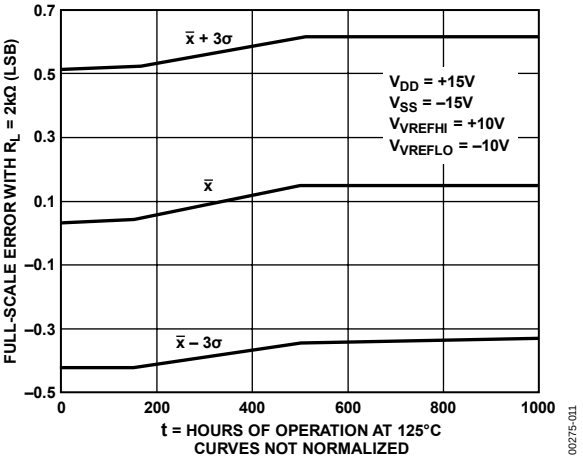


Figure 10. Full-Scale Error vs. Time Accelerated by Burn-In

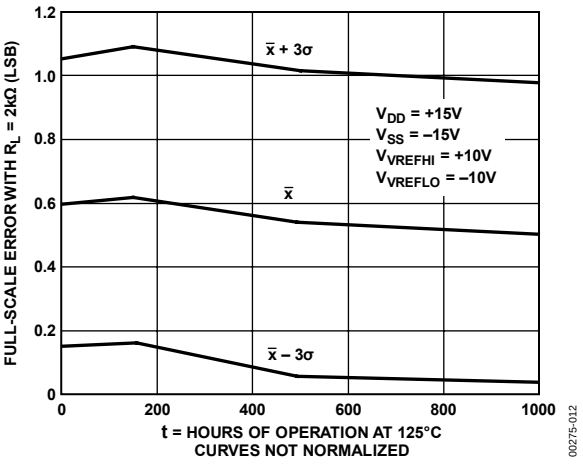


Figure 11. Zero-Scale Error vs. Time Accelerated by Burn-In

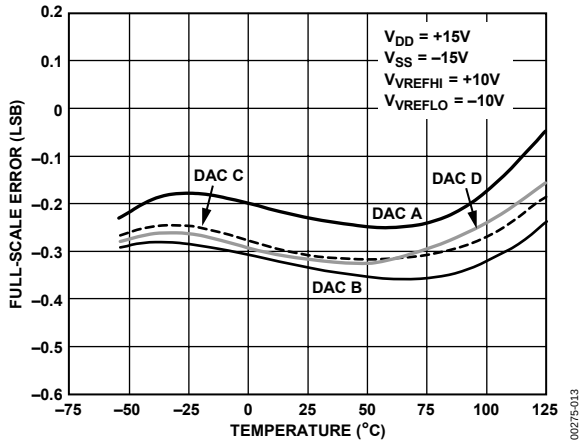


Figure 12. Full-Scale Error vs. Temperature

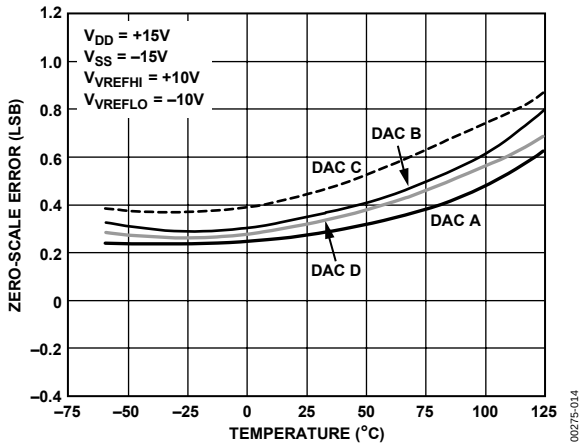


Figure 13. Zero-Scale Error vs. Temperature

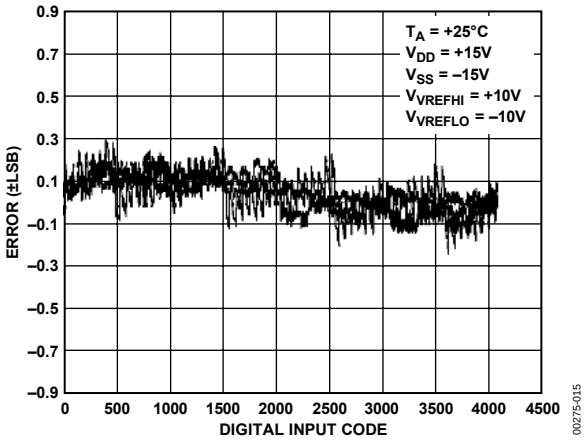


Figure 14. Channel-to-Channel Matching

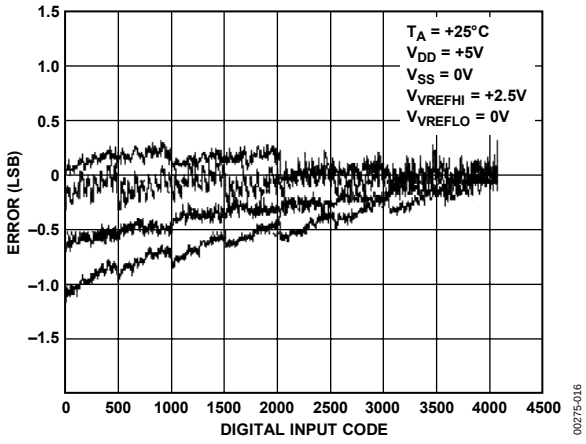


Figure 15. Channel-to-Channel Matching

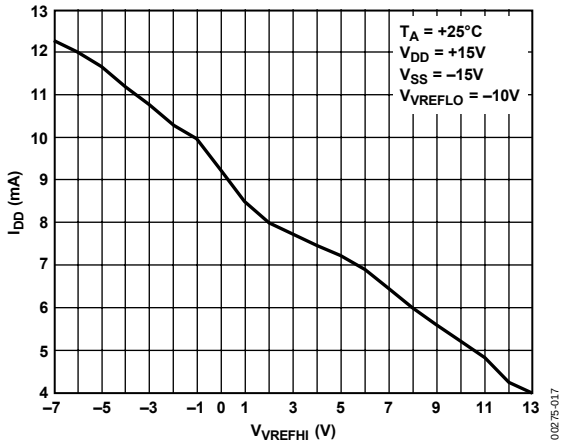


Figure 16. I_{DD} vs. V_{VREFHI}, All DACs High

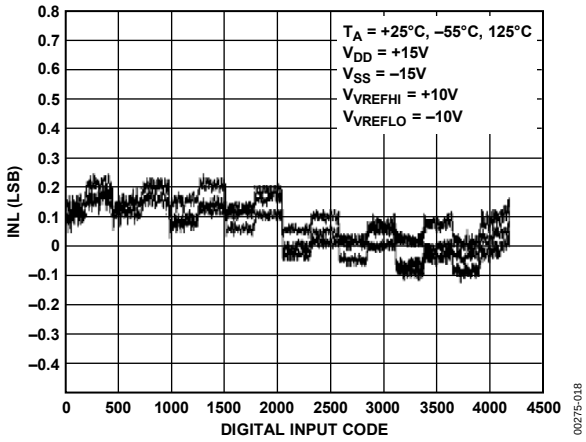


Figure 17. INL vs. Code

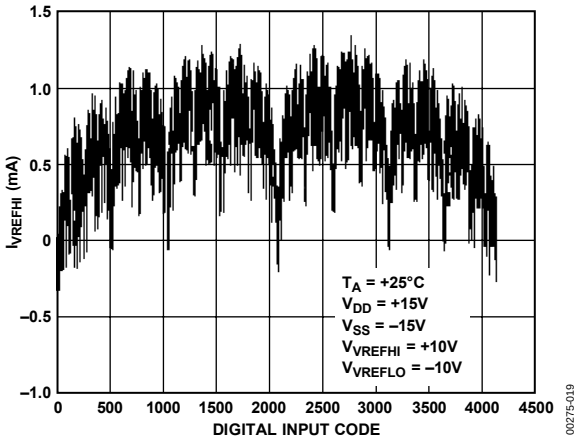


Figure 18. I_{VREFHI} vs. Code

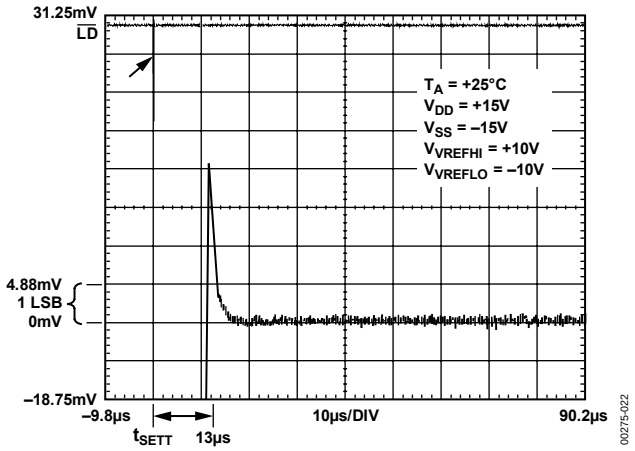


Figure 21. Positive Settling Time (±15 V)

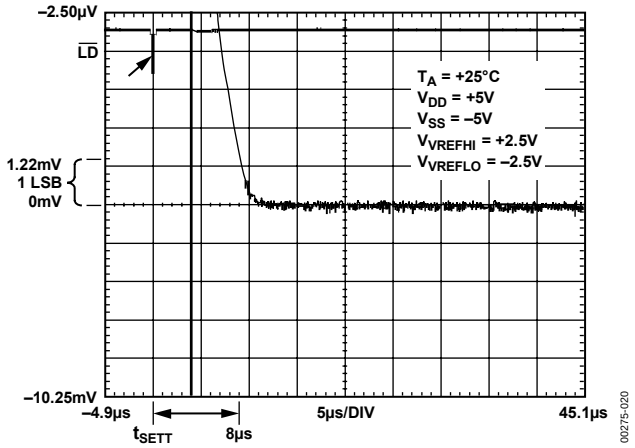


Figure 19. Positive Settling Time (±5 V)

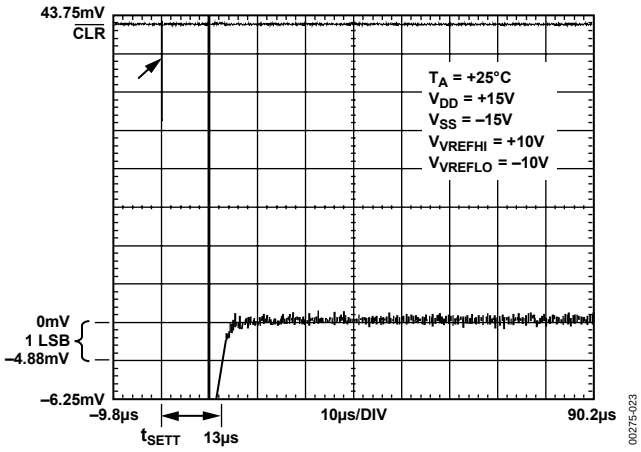


Figure 22. Negative Settling Time (±15 V)

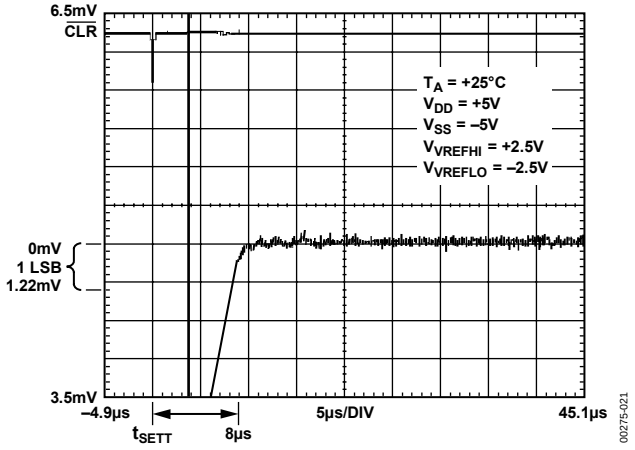


Figure 20. Negative Settling Time (±5 V)

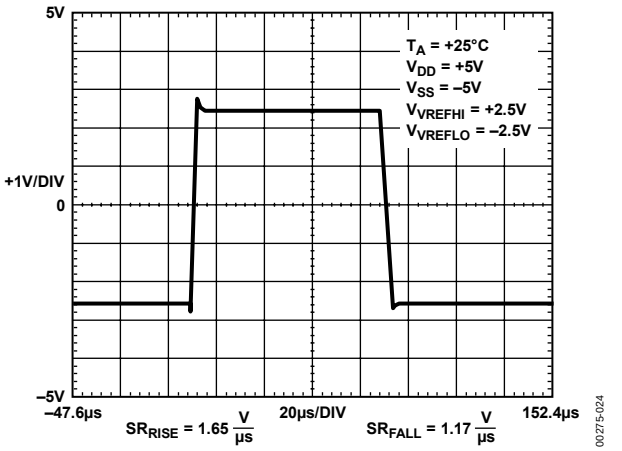


Figure 23. Slew Rate (±5 V)

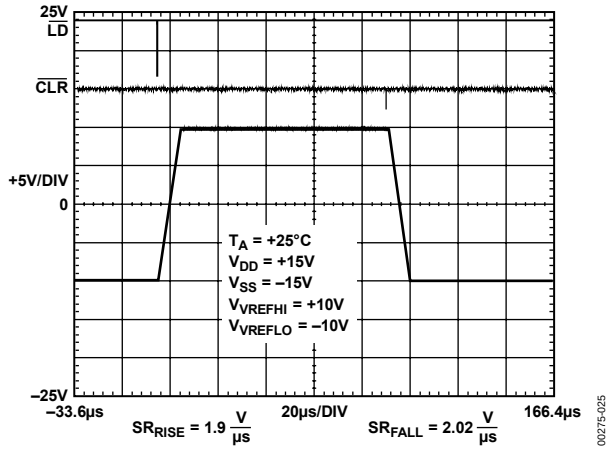


Figure 24. Slew Rate (±15 V)

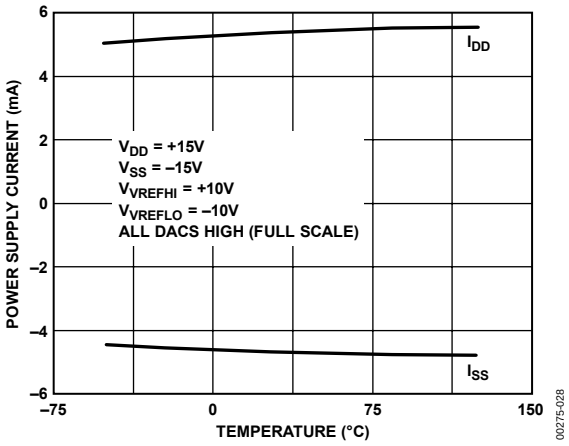


Figure 27. Power Supply Current vs. Temperature

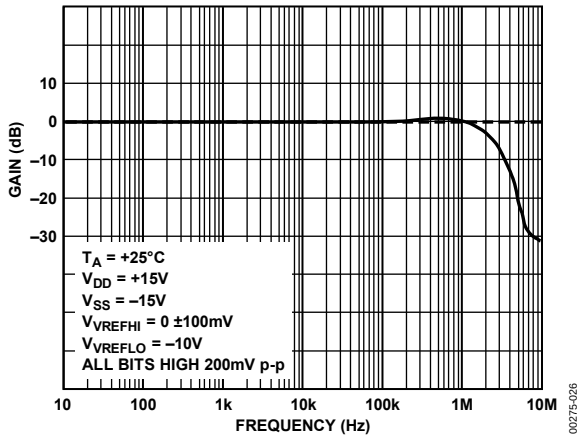


Figure 25. Small-Signal Response

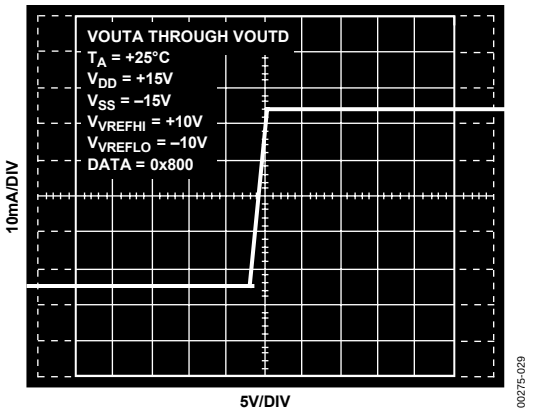


Figure 28. DAC Output Current vs. VOUTx

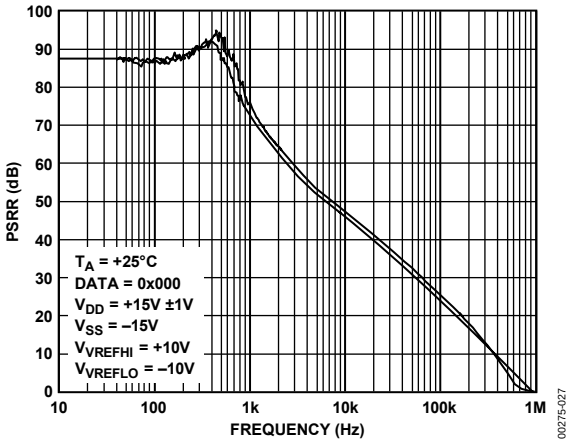


Figure 26. PSRR vs. Frequency

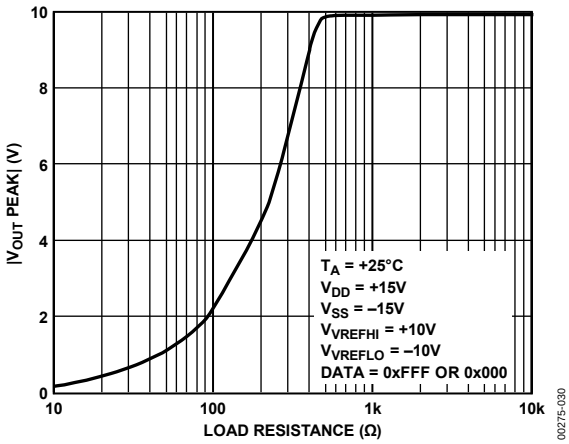


Figure 29. Output Swing vs. Load Resistance

THEORY OF OPERATION

INTRODUCTION

The DAC8420 is a quad, voltage-output 12-bit DAC with a serial digital input capable of operating from a single 5 V supply. The straightforward serial interface can be connected directly to most popular microprocessors and microcontrollers, and can accept data at a 10 MHz clock rate when operating from ±15 V supplies. A unique voltage reference structure ensures maximum utilization of the DAC output resolution by allowing the user to set the zero-scale and full-scale output levels within the supply rails. The analog voltage outputs are fully buffered, and are capable of driving a 2 kΩ load. Output glitch impulse during major code transitions is a very low 64 nV-s (typ).

DIGITAL INTERFACE OPERATION

The serial input of the DAC8420, consisting of $\overline{CS}$, SDI, and $\overline{LD}$, is easily interfaced to a wide variety of microprocessor serial ports. While $\overline{CS}$ is low, the data presented to the input SDI is shifted into the internal serial-to-parallel shift register on the rising edge of the clock, with the address MSB first, data LSB last, as shown in Table 6 and in the timing diagram (Figure 2). The data format, shown in Table 8, is two bits of DAC address and two don't care fill bits, followed by the 12-bit DAC data-word. Once all 16 bits of the serial data-word have been input, the load control $\overline{LD}$ is strobed and the word is parallel-shifted out onto the internal data bus. The two address bits are decoded and used to route the 12-bit data-word to the appropriate DAC data register (see the Applications section).

CORRECT OPERATION OF $\overline{CS}$ AND CLK

In Table 6, the control pins CLK and $\overline{CS}$ require some attention during a data load cycle. Since these two inputs are fed to the same logical OR gate, the operation is in fact identical. The user must take care to operate them accordingly to avoid clocking in false data bits. In the timing diagram, CLK must be halted high or $\overline{CS}$ must be brought high during the last high portion of the CLK following the rising edge that latched in the last data bit. Otherwise, an additional rising edge is generated by $\overline{CS}$ rising while CLK is low, causing $\overline{CS}$ to act as the clock and allowing a false data bit into the serial input register. The same issue must also be considered in the beginning of the data load sequence.

USING $\overline{CLR}$ AND CLSEL

The clear ($\overline{CLR}$) control allows the user to perform an asynchronous reset function. Asserting $\overline{CLR}$ loads all four DAC data-word registers, forcing the DAC outputs to either zero scale (0x000) or midscale (0x800), depending on the state of CLSEL as shown in Table 6. The clear function is asynchronous and totally independent of $\overline{CS}$. When $\overline{CLR}$ returns high, the DAC outputs remain latched at the reset value until $\overline{LD}$ is strobed, reloading the individual DAC data-word registers with either the data held in the serial input register prior to the reset or with new data loaded through the serial interface.

Table 7. DAC Address Word Decode Table

A1	A0	DAC Addressed
0	0	DAC A
0	1	DAC B
1	0	DAC C
1	1	DAC D

PROGRAMMING THE ANALOG OUTPUTS

The unique differential reference structure of the DAC8420 allows the user to tailor the output voltage range precisely to the needs of the application. Instead of spending DAC resolution on an unused region near the positive or negative rail, the DAC8420 allows the user to determine both the upper and lower limits of the analog output voltage range. Thus, as shown in Table 9 and Figure 30, the outputs of DAC A through DAC D range between VREFHI and VREFLO, within the limits specified in the Specifications section. Note also that VREFHI must be greater than VREFLO.

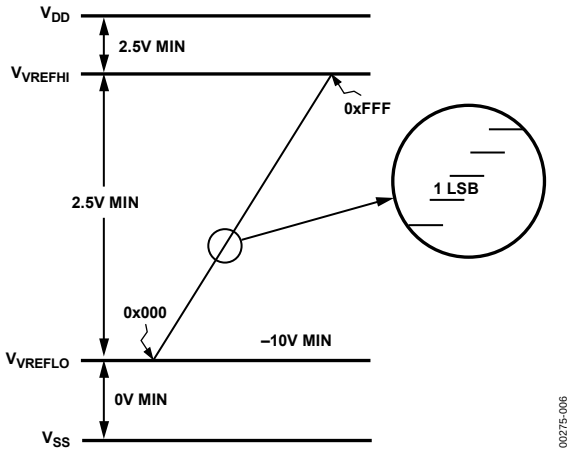


Figure 30. Output Voltage Range Programming

Table 8.

(FIRST) (LAST)

B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15
A1	A0	NC	NC	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
—Address Word—				(MSB)					—DAC Data-Word—						(LSB)

Table 9. Analog Output Code

DAC Data-Word (Hex)	V_{OUT}	Note
0xFFF	$VREFLO + \frac{(VREFHI - VREFLO)}{4096} \times 4095$	Full-scale output
0x801	$VREFLO + \frac{(VREFHI - VREFLO)}{4096} \times 2049$	Midscale + 1
0x800	$VREFLO + \frac{(VREFHI - VREFLO)}{4096} \times 2048$	Midscale
0x7FF	$VREFLO + \frac{(VREFHI - VREFLO)}{4096} \times 2047$	Midscale – 1
0x000	$VREFLO + \frac{(VREFHI - VREFLO)}{4096} \times 0$	Zero scale

VREFHI INPUT REQUIREMENTS

The DAC8420 utilizes a unique, patented DAC switch driver circuit that compensates for different supply, reference voltage, and digital code inputs. This ensures that all DAC ladder switches are always biased equally, ensuring excellent linearity under all conditions. Thus, as shown in Table 1, the VREFHI input of the DAC8420 requires both sourcing and sinking current capabilities from the reference voltage source. Many positive voltage references are intended as current sources only and offer little sinking capability. The user should consider references such as the AD584, AD586, AD587, AD588, AD780, and REF43 for such an application.

POWER-UP SEQUENCE

To prevent a CMOS latch-up condition, power up VDD, VSS, and GND prior to any reference voltages. The ideal power-up sequence is GND, VSS, VDD, VREFHI, VREFLO, and digital inputs. Noncompliance with the power-up sequence over an extended period can elevate the reference currents and eventually damage the device. On the other hand, if the noncompliant power-up sequence condition is as short as a few milliseconds, the device can resume normal operation without being damaged once VDD/VSS is powered.

APPLICATIONS

POWER SUPPLY BYPASSING AND GROUNDING

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The DAC8420 has a single ground pin that is internally connected to the digital section as the logic reference level. The first thought may be to connect this pin to digital ground; however, in large systems digital ground is often noisy because of the switching currents of other digital circuitry. Any noise that is introduced at the ground pin can couple into the analog output. Thus, to avoid error-causing digital noise in the sensitive analog circuitry, the ground pin should be connected to the system analog ground. The ground path (circuit board trace) should be as wide as possible to reduce any effects of parasitic inductance and ohmic drops. A ground plane is recommended if possible. The noise immunity of the on-board digital circuitry, typically in the hundreds of millivolts, is well able to reject the common-mode noise typically seen between system analog and digital grounds. Finally, the analog and digital ground should be connected to each other at a single point in the system to provide a common reference. This is preferably done at the power supply.

Good grounding practice is also essential to maintaining analog performance in the surrounding analog support circuitry. With two reference inputs and four analog outputs capable of moderate bandwidth and output current, there is a significant potential for ground loops. Again, a ground plane is recommended as the most effective solution to minimizing errors due to noise and ground offsets.

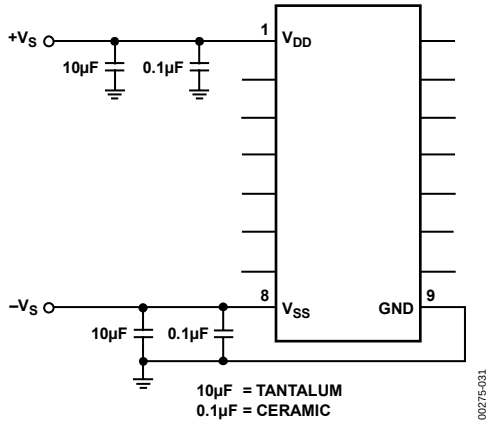


Figure 31. Recommended Supply Bypassing Scheme

The DAC8420 should have ample supply bypassing, located as close to the package as possible. Figure 31 shows the recommended capacitor values of 10 µF in parallel with 0.1 µF. The 0.1 µF capacitor should have low effective series resistance (ESR) and effective series inductance (ESI) (such as any common ceramic type capacitor), which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching. To preserve the specified analog performance of the device, the supply should be as noise free as possible. In the case of 5 V only systems, it is desirable to use the same 5 V supply for both the analog circuitry and the digital portion of the circuit. Unfortunately, the typical 5 V supply is extremely noisy due to the fast edge rates of the popular CMOS logic families, which induce large inductive voltage spikes, and busy microcontroller or microprocessor buses, and therefore commonly have large current spikes during bus activity. However, by properly filtering the supply as shown in Figure 32, the digital 5 V supply can be used. The inductors and capacitors generate a filter that not only rejects noise due to the digital circuitry, but also filters out the lower frequency noise of switch mode power supplies. The analog supply should be connected as close as possible to the origin of the digital supply to minimize noise pickup from the digital section.

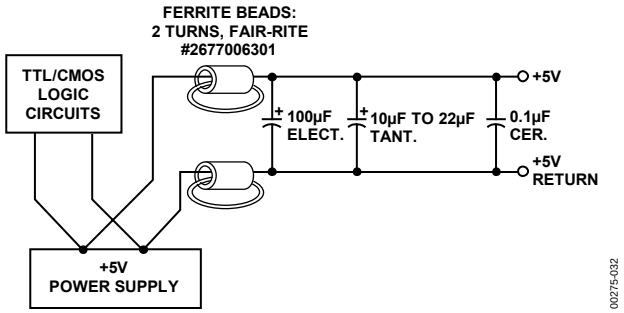


Figure 32. Single-Supply Analog Supply Filter

ANALOG OUTPUTS

The DAC8420 features buffered analog voltage outputs capable of sourcing and sinking up to 5 mA when operating from ±15 V supplies, eliminating the need for external buffer amplifiers in most applications while maintaining specified accuracy over the rated operating conditions. The buffered outputs are simply an op amp connected as a voltage follower, and thus have output characteristics very similar to the typical operational amplifier. These amplifiers are short-circuit protected. The user should verify that the output load meets the capabilities of the device, in terms of both output current and load capacitance. The DAC8420 is stable with capacitive loads up to 2 nF typically. However, any capacitive load will increase the settling time, and should be minimized if speed is a concern.

The output stage includes a P-channel MOSFET to pull the output voltage down to the negative supply. This is very important in single-supply systems where VREFLO usually has the same potential as the negative supply. With no load, the zero-scale output voltage in these applications is less than 500 µV typically, or less than 1 LSB when V_{VREFHI} = 2.5 V. However, when sinking current, this voltage does increase because of the finite impedance of the output stage. The effective value of the pull-down resistor in the output stage is typically 320 Ω. With a 100 kΩ resistor connected to 5 V, the resulting zero-scale output voltage

is 16 mV. Thus, the best single-supply operation is obtained with the output load connected to ground, so the output stage does not have to sink current.

Like all amplifiers, the DAC8420 output buffers do generate voltage noise, 52 nV/√Hz typically. This is easily reduced by adding a simple RC low-pass filter on each output.

REFERENCE CONFIGURATION

The two reference inputs of the DAC8420 allow a great deal of flexibility in circuit design. The user must take care, however, to observe the minimum voltage input levels on VREFHI and VREFLO to maintain the accuracy shown in the data sheet. These input voltages can be set anywhere across a wide range within the supplies, but must be a minimum of 2.5 V apart in any case (see Figure 30). A wide output voltage range can be obtained with ±5 V references, which can be provided by the AD588 as shown in Figure 33. Many applications utilize the DACs to synthesize symmetric bipolar waveforms, which require an accurate, low drift bipolar reference. The AD588 provides both voltages and needs no external components. Additionally, the part is trimmed in production for 12-bit accuracy over the full temperature range without user calibration. Performing a clear with the reset select CLSEL high allows the user to easily reset the DAC outputs to midscale, or 0 V in these applications.

When driving the reference inputs VREFHI and VREFLO, it is important to note that VREFHI both sinks and sources current, and that the input currents of both are code dependent. Many voltage reference products have a limited current sinking capability and must be buffered with an amplifier to drive VREFHI in order to maintain overall system accuracy. The input VREFLO, however, has no such requirement.

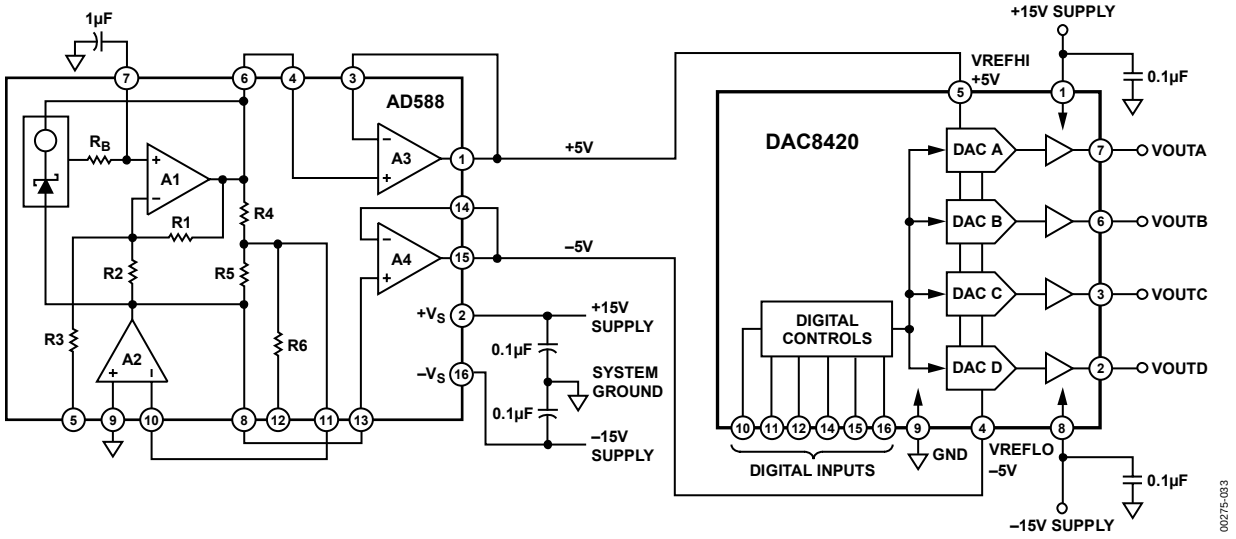


Figure 33. ±10 V Bipolar Reference Configuration Using the AD588

For a single 5 V supply, V_{VREFHI} is limited to at most 2.5 V, and must always be at least 2.5 V less than the positive supply to ensure linearity of the device. For these applications, the REF43 is an excellent low drift 2.5 V reference that consumes only 450 µA (max). It works well with the DAC8420 in a single 5 V system as shown in Figure 34.

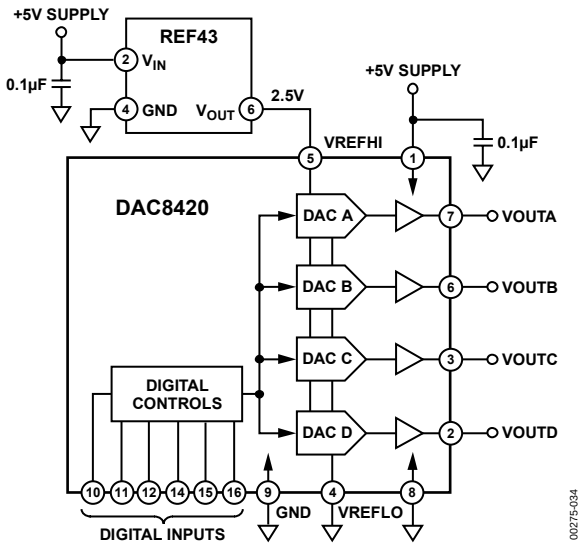


Figure 34. 5 V Single-Supply Operation Using REF43

ISOLATED DIGITAL INTERFACE

Because the DAC8420 is ideal for generating accurate voltages in process control and industrial applications, due to noise, from the central controller; it may be necessary to isolate it from the central controller. This can be easily achieved by using opto-isolators, which are commonly used to provide electrical isolation in excess of 3 kV. Figure 35 shows a simple 3-wire interface scheme for controlling the clock, data, and load pulse. For normal operation, $\overline{CS}$ is tied permanently low so that the DAC8420 is always selected. The resistor and capacitor on the $\overline{CLR}$ pin provide a power-on reset with 10 ms time constant. The three opto-isolators are used for the SDI, CLK, and $\overline{LD}$ lines.

One opto-isolated line ($\overline{LD}$) can be eliminated from this circuit by adding an inexpensive 4-bit TTL counter to generate the load pulse for the DAC8420 after 16 clock cycles. The counter is used to count the number of clock cycles loading serial data to the DAC8420. After all 16 bits have been clocked into the converter, the counter resets, and a load pulse is generated on Clock 17. In either circuit, the serial interface of the DAC8420 provides a simple, low cost method of isolating the digital control.

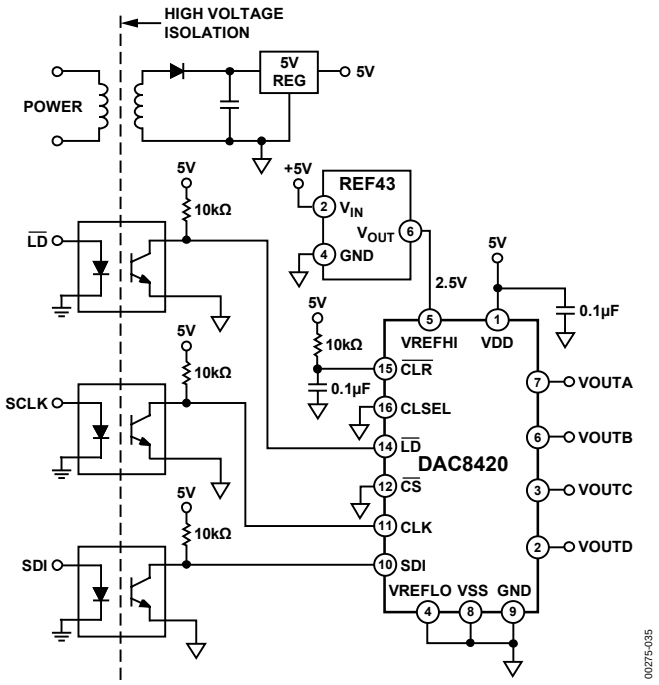


Figure 35. Opto-Isolated 3-Wire Interface

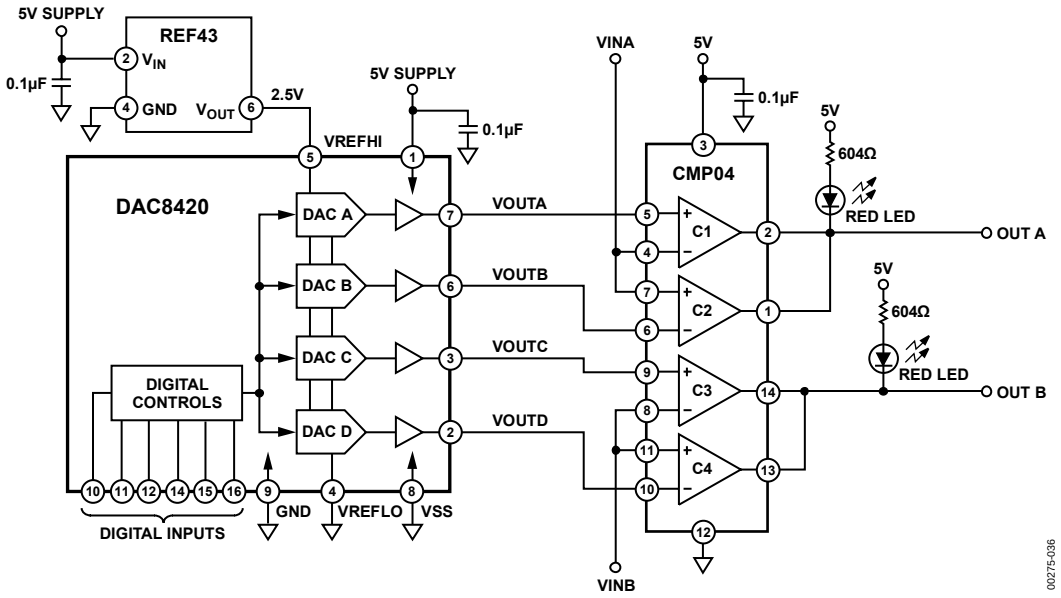


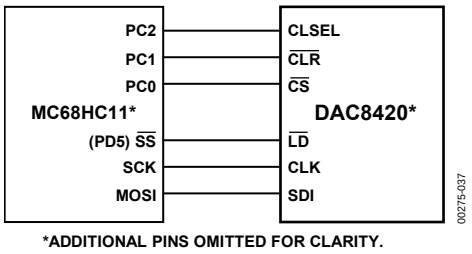
Figure 36. Dual Programmable Window Comparator

DUAL WINDOW COMPARATOR

Often a comparator is needed to signal an out-of-range warning. Combining the DAC8420 with a quad comparator such as the CMP04 provides a simple dual window comparator with adjustable trip points as shown in Figure 36. This circuit can be operated with either a dual supply or a single supply. For the A input channel, DAC B sets the low trip point, and DAC A sets the upper trip point. The CMP04 has open-collector outputs that are connected together in a wire-OR'ed configuration to generate an out-of-range signal. For example, when VINA goes below the trip point set by DAC B, Comparator C2 pulls the output down, turning on the red LED. The output can also be used as a logic signal for further processing.

MC68HC11 MICROCONTROLLER INTERFACING

Figure 37 shows a serial interface between the DAC8420 and the MC68HC11 8-bit microcontroller. The SCK output of the port outputs the serial data to load into the SDI input of the DAC. The port lines (PD5, PC0, PC1, and PC2) provide the controls to the DAC as shown.



*ADDITIONAL PINS OMITTED FOR CLARITY.

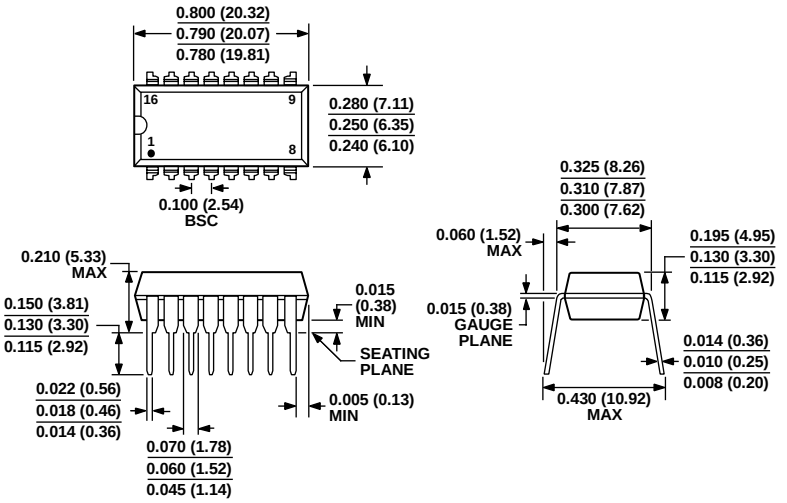
Figure 37. MC68HC11 Microcontroller Interface

For correct operation, the MC68HC11 should be configured such that its CPOL bit and CPHA bit are both set to 1. In this configuration, serial data on MOSI of the MC68HC11 is valid on the rising edge of the clock, which is the required timing for the DAC8420. Data is transmitted in 8-bit bytes (MSB first), with only eight rising clock edges occurring in the transmit cycle. To load data to the input register of the DAC8420, PC0 is taken low and held low during the entire loading cycle. The first eight bits are shifted in address first, immediately followed by another eight bits in the second least-significant byte to load the complete 16-bit word. At the end of the second byte load, PC0 is then taken high. To prevent an additional advancing of the internal shift register, SCK must already be asserted before PC0 is taken high. To transfer the contents of the input shift register to the DAC register, PD5 is then taken low, asserting the $\overline{LD}$ input of the DAC and completing the loading process. PD5 should return high before the next load cycle begins. The $\overline{CLR}$ input of the DAC8420 (controlled by the output PC1) provides an asynchronous clear function.

DAC8420 TO M68HC11 INTERFACE ASSEMBLY PROGRAM

```
* M68HC11 Register Definitions
PORTC EQU $1003 Port C control register
* "0,0,0,0;0,CLSEL,CLR,CS"
DDRC EQU $1007 Port C data direction
PORTD EQU $1008 Port D data register
* "0,0,LD,SCLK;SDI,0,0,0"
DDRD EQU $1009 Port D data direction
SPCR EQU $1028 SPI control register
* "SPIE,SPE,DWOM,MSTR;CPOL,CPHA,SPR1,SPR0"
SPSR EQU $1029 SPI status register
* "SPIF,WCOL,0,MODF;0,0,0,0"
SPDR EQU $102A SPI data register; Read-Buffer; Write-Shifter
*
* SDI RAM variables: SDI1 is encoded from 0 (Hex) to CF (Hex)
* To select: DAC A – Set SDI1 to $0X
  DAC B – Set SDI1 to $4X
  DAC C – Set SDI1 to $8X
  DAC D – Set SDI1 to $CX
  SDI2 is encoded from 00 (Hex) to FF (Hex)
* DAC requires two 8-bit loads – Address + 12 bits
SDI1 EQU $00 SDI packed byte 1 "A1,A0,0,0;MSB,DB10,DB9,DB8"
SDI2 EQU $01 SDI packed byte 2
"DB7,DB6,DB5,DB4;DB3,DB2,DB1,DB0"
* Main Program
ORG $C000 Start of user's RAM in EVB
INIT LDS #$CFFF Top of C page RAM
* Initialize Port C Outputs
  LDAA #$07 0,0,0,0;0,1,1,1
* CLSEL-Hi, CLR-Hi, CS-Hi
* To reset DAC to ZERO-SCALE, set CLSEL-Lo ($03)
* To reset DAC to MID-SCALE, set CLSEL-Hi ($07)
  STAA PORTC Initialize Port C Outputs
  LDAA #$07 0,0,0,0;0,1,1,1
  STAA DDRC CLSEL, CLR, and CS are now enabled as outputs
* Initialize Port D Outputs
  LDAA #$30 0,0,1,1;0,0,0,0
* LD-Hi,SCLK-Hi,SDI-Lo
  STAA PORTD Initialize Port D Outputs
  LDAA #$38 0,0,1,1;1,0,0,0
  STAA DDRD LD,SCLK, and SDI are now enabled as outputs
* Initialize SPI Interface
  LDAA #$5F
  STAA SPCR SPI is Master,CPHA=1,CPOL=1,Clk rate=E/32
* Call update subroutine
  BSR UPDATE Xfer 2 8-bit words to DAC-8420
  JMP $E000 Restart BUFFALO
* Subroutine UPDATE
UPDATE PSHX Save registers X, Y, and A
  PSHY
  PSHA
* Enter Contents of SDI1 Data Register (DAC# and 4 MSBs)
  LDAA #$80 1,0,0,0;0,0,0,0
  STAA SDI1 SDI1 is set to 80 (Hex)
* Enter Contents of SDI2 Data Register
  LDAA #$00 0,0,0,0;0,0,0,0
  STAA SDI2 SDI2 is set to 00 (Hex)
  LDX #SDI1 Stack pointer at 1st byte to send via SDI
  LDY #$1000 Stack pointer at on-chip registers
* Clear DAC output to zero
  BCLR PORTC,Y $02 Assert CLR
  BSET PORTC,Y $02 Deassert CLR
* Get DAC ready for data input
  BCLR PORTC,Y $01 Assert CS
TFRLP LDAA 0,X Get a byte to transfer via SPI
  STAA SPDR Write SDI data reg to start xfer
WAIT LDAA SPSR Loop to wait for SPIF
  BPL WAIT SPIF is the MSB of SPSR
*                 (when SPIF is set, SPSR is negated)
  INX             Increment counter to next byte for xfer
  CPX #SDI2+ 1 Are we done yet ?
  BNE TFRLP If not, xfer the second byte
* Update DAC output with contents of DAC register
  BCLR PORTD,Y 520 Assert LD
  BSET PORTD,Y $20 Latch DAC register
  BSET PORTC,Y $01 De-assert CS
  PULA When done, restore registers X, Y & A
  PULY
  PULX
  RTS       ** Return to Main Program **
```

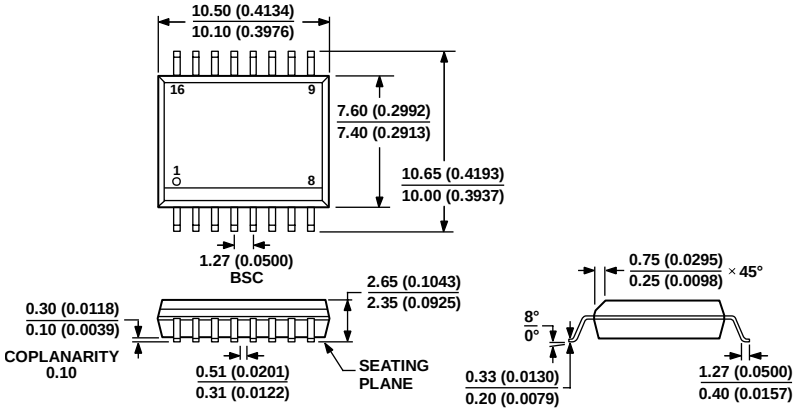
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-001-AB
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

073106-B

Figure 38. 16-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body
(N-16)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-013- AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

032707-B

Figure 39. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-16)
Dimensions shown in millimeters and (inches)

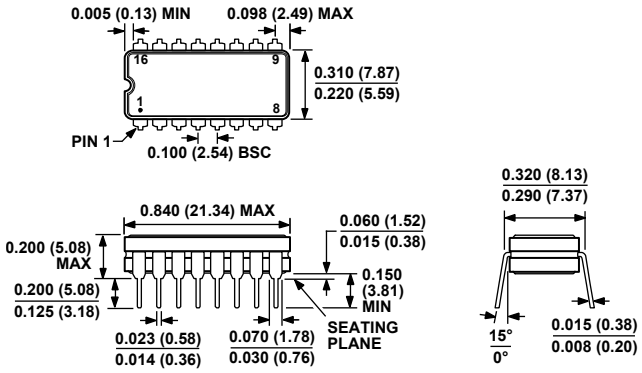


Figure 40. 16-Lead Ceramic Dual In-Line Package [CERDIP]
(Q-16)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	INL[1] (±LSB)
DAC8420EP	−40°C to +85°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16	0.5
DAC8420EPZ[2]	−40°C to +85°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16	0.5
DAC8420ES	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16	0.5
DAC8420ES-REEL	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16	0.5
DAC8420ESZ[2]	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16	0.5
DAC8420ESZ-REEL[2]	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16	0.5
DAC8420FP	−40°C to +85°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16	1.0
DAC8420FPZ[2]	−40°C to +85°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16	1.0
DAC8420FQ	−40°C to +85°C	16-Lead Ceramic Dual In-Line Package [CERDIP]	Q-16	1.0
DAC8420FS	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16	1.0
DAC8420FS-REEL	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16	1.0
DAC8420FSZ[2]	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16	1.0
DAC8420FSZ-REEL[2]	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16	1.0

[1] INL measured at VDD = +15 V and VSS = −15 V.
[2] Z = RoHS Compliant Part.

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