24-Bit, 156 kSPS, 112 dB Sigma-Delta ADC with On-Chip Buffers and Serial Interface

AD7765

FEATURES

High performance, 24-bit Σ-Δ ADC
115 dB dynamic range at 78 kHz output data rate
112 dB dynamic range at 156 kHz output data rate
156 kHz maximum fully filtered output word rate
Pin-selectable oversampling rate (128× and 256×)
Low power mode
Flexible SPI
Fully differential modulator input
On-chip differential amplifier for signal buffering
On-chip reference buffer
Full band low-pass finite impulse response (FIR) filter
Overrange alert pin
Digital gain correction registers
Power-down mode
Synchronization of multiple devices via $\overline{\text{SYNC}}$ pin
Daisy chaining

APPLICATIONS

Data acquisition systems
Vibration analysis
Instrumentation

GENERAL DESCRIPTION

The AD7765 is a high performance, 24-bit sigma-delta (Σ-Δ) analog-to-digital converter (ADC). It combines wide input bandwidth, high speed, and performance of 112 dB dynamic range at a 156 kHz output data rate. With excellent dc specifications, the converter is ideal for high speed data acquisition of ac signals where dc data is also required.

Using the AD7765 eases the front-end antialias filtering requirements, simplifying the design process significantly. The AD7765 offers pin-selectable decimation rates of 128× and 256×. Other features include an integrated buffer to drive the reference, as well as a fully differential amplifier to buffer and level shift the input to the modulator.

An overrange alert pin indicates when an input signal has exceeded the acceptable range. The addition of internal gain and internal overrange registers makes the AD7765 a compact, highly integrated data acquisition device requiring minimal peripheral components.

The AD7765 also offers a low power mode, significantly reducing power dissipation without reducing the output data rate or available input bandwidth.

FUNCTIONAL BLOCK DIAGRAM

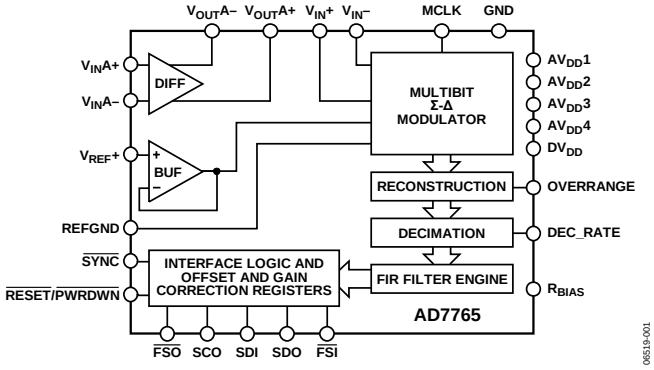

Figure 1.

The differential input is sampled at up to 40 MSPS by an analog modulator. The modulator output is processed by a series of low-pass filters. The external clock frequency applied to the AD7765 determines the sample rate, filter corner frequencies, and output word rate.

The AD7765 device boasts a full band on-board FIR filter. The full stop-band attenuation of the filter is achieved at the Nyquist frequency. This feature offers increased protection from signals that lie above the Nyquist frequency being aliased back into the input signal bandwidth.

The reference voltage supplied to the AD7765 determines the input range. With a 4 V reference, the analog input range is ±3.2768 V differential, biased around a common mode of 2.048 V. This common-mode biasing can be achieved using the on-chip differential amplifier, further reducing the external signal conditioning requirements.

The AD7765 is available in a 28-lead TSSOP package and is specified over the industrial temperature range of −40°C to +85°C.

Table 1. Related Devices

Part No.	Description
AD7760	2.5 MSPS, 100 dB, parallel output, on-chip buffers
AD7762	625 kSPS, 109 dB, parallel output, on-chip buffers
AD7763	625 kSPS, 109 dB, serial output, on-chip buffers
AD7764	312 kSPS, 109 dB, serial output, on-chip buffers
AD7766	128/64/32 kSPS, 8.5 mW, 109 dB SNR
AD7767	128/64/32 kSPS, 8.5 mW, 109 dB SNR

Rev. A

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6/07—Revision 0: Initial Version

SPECIFICATIONS

$AV_{DD}1 = DV_{DD} = 2.5$ V, $AV_{DD}2 = AV_{DD}3 = AV_{DD}4 = 5$ V, $V_{REF}+ = 4.096$ V, MCLK amplitude = 5 V, $T_A = +25°C$, normal power mode, using the on-chip amplifier with components as shown in the Optimal row in Table 7, unless otherwise noted.[1]

Table 2.

Parameter	Test Conditions/Comments	Specification	Unit
DYNAMIC PERFORMANCE			
Decimate 256×			
Normal Power Mode	MCLK = 40 MHz, ODR = 78.125 kHz, f_{IN} = 1 kHz sine wave		
Dynamic Range	Modulator inputs shorted	115	dB typ
		110	dB min
	Differential amplifier inputs shorted	113.4	dB typ
Signal-to-Noise Ratio (SNR)[2]	Input amplitude = −0.5 dB	109	dB typ
		106	dB min
Spurious-Free Dynamic Range (SFDR)	Nonharmonic	130	dBFS typ
Total Harmonic Distortion (THD)	Input amplitude = −0.5 dB	−105	dB typ
	Input amplitude = −6 dB	−103	dB typ
	Input amplitude = −60 dB	−71	dB typ
Low Power Mode	MCLK = 40 MHz, ODR = 78.125 kHz, f_{IN} = 1 kHz sine wave		
Dynamic Range	Modulator inputs shorted	113	dB typ
		110	dB min
	Differential amplifier inputs shorted	112	dB typ
Signal-to-Noise Ratio (SNR)[2]	Input amplitude = −0.5 dB	109	dB typ
		106	dB min
Total Harmonic Distortion (THD)	Input amplitude = −0.5 dB	−105	dB typ
	Input amplitude = −6 dB	−111	dB typ
	Input amplitude = −6 dB	−100	dB max
	Input amplitude = −60 dB	−76	dB typ
Decimate 128×			
Normal Power Mode	MCLK = 40 MHz, ODR = 156.25 kHz, f_{IN} = 1 kHz sine wave		
Dynamic Range	Modulator inputs shorted	112	dB typ
		108	dB min
	Differential amplifier inputs shorted	110.4	dB typ
Signal-to-Noise Ratio (SNR)[2]		107	dB typ
		105	dB min
Spurious-Free Dynamic Range (SFDR)	Nonharmonic	130	dBFS typ
Total Harmonic Distortion (THD)	Input amplitude = −0.5 dB	−105	dB typ
	Input amplitude = −6 dB	−103	dB typ
Intermodulation Distortion (IMD)	Input amplitude = −6 dB, f_{IN} A = 50.3 kHz, f_{IN} B = 47.3 kHz		
	Second-order terms	−117	dB typ
	Third-order terms	−108	dB typ
Low Power Mode	MCLK = 40 MHz, ODR = 156.25 kHz, f_{IN} = 1 kHz sine wave		
Dynamic Range	Modulator inputs shorted	110	dB typ
		109	dB min
	Differential amplifier inputs shorted	109	dB typ
Signal-to-Noise Ratio (SNR)[2]	Input amplitude = −0.5 dB	107	dB typ
		105	dB min
Total Harmonic Distortion (THD)	Input amplitude = −0.5 dB	−105	dB typ
	Input amplitude = −6 dB	−111	dB typ
	Input amplitude = −6 dB	−100	dB max
Intermodulation Distortion (IMD)	Input amplitude = −6 dB, f_{IN} A= 50.3 kHz, f_{IN} B = 47.3 kHz		
	Second-order terms	−134	dB typ
	Third-order terms	−110	dB typ

Parameter	Test Conditions/Comments	Specification	Unit
DC ACCURACY			
Resolution	Guaranteed monotonic to 24 bits	24	Bits
Integral Nonlinearity	Normal power mode	0.0036	% typ
	Low power mode	0.0014	% typ
Zero Error	Normal power mode	0.006	% typ
		0.03	% max
	Including on-chip amplifier	0.04	% typ
	Low power mode	0.002	% typ
		0.024	% max
Gain Error		0.018	% typ
	Including on-chip amplifier	0.04	% typ
Zero Error Drift		0.00006	%FS/°C typ
Gain Error Drift		0.00005	%FS/°C typ
DIGITAL FILTER CHARACTERISTICS			
Pass-Band Ripple		0.1	dB typ
Pass Band[3]	−1 dB frequency	ODR × 0.4016	kHz
−3 dB Bandwidth[3]		ODR × 0.4096	kHz
Stop Band[3]	Beginning of stop band	ODR × 0.5	kHz
Stop-Band Attenuation	Decimate 128×	120	dB typ
	Decimate 256×	115	
Group Delay			
Decimate 128×	MCLK = 40 MHz	177	µs typ
Decimate 256×	MCLK = 40 MHz	358	µs typ
ANALOG INPUT			
Differential Input Voltage	Modulator input pins: $V_{IN}+ - V_{IN}-$, $V_{REF}+ = 4.096$ V	±3.2768	V p-p
Input Capacitance	At on-chip differential amplifier inputs	5	pF typ
	At modulator inputs	29	pF typ
REFERENCE INPUT/OUTPUT			
V_{REF+} Input Voltage	$AV_{DD}3 = 5$ V ± 5%	4.096	V
V_{REF+} Input DC Leakage Current		±1	µA max
V_{REF+} Input Capacitance		5	pF typ
DIGITAL INPUT/OUTPUT			
MCLK Input Amplitude		2.25 to 5.25	V
Input Capacitance		7.3	pF typ
Input Leakage Current		±1	µA/pin max
V_{INH}		0.8 × DV_{DD}	V min
V_{INL}		0.2 × DV_{DD}	V max
V_{OH}[4]		2.2	V min
V_{OL}		0.1	V max
ON-CHIP DIFFERENTIAL AMPLIFIER			
Input Impedance		>1	MΩ
Bandwidth for 0.1 dB Flatness		125	kHz
Common-Mode Input Voltage	Voltage range at input pins: $V_{IN}A-$ and $V_{IN}A+$	−0.5 to +2.2	V
Common-Mode Output Voltage	On-chip differential amplifier pins: $V_{OUT}A+$ and $V_{OUT}A-$	2.048	V
POWER REQUIREMENTS			
$AV_{DD}1$ (Modulator Supply)	±5%	2.5	V
$AV_{DD}2$ (General Supply)	±5%	5	V
$AV_{DD}3$ (Differential Amplifier Supply)	±5%	5	V min/max
$AV_{DD}4$ (Reference Buffer Supply)	±5%	5	V min/max
DV_{DD}	±5%	2.5	V

Parameter	Test Conditions/Comments	Specification	Unit
Normal Power Mode			
$AI_{DD}1$ (Modulator)		19	mA typ
$AI_{DD}2$ (General)[5]	MCLK = 40 MHz	13	mA typ
$AI_{DD}3$ (Differential Amplifier)	$AV_{DD}3$ = 5 V	10	mA typ
$AI_{DD}4$ (Reference Buffer)	$AV_{DD}4$ = 5 V	9	mA typ
DI_{DD}[5]	MCLK = 40 MHz	37	mA typ
Low Power Mode			
$AI_{DD}1$ (Modulator)		10	mA typ
$AI_{DD}2$ (General)[5]	MCLK = 40 MHz	7	mA typ
$AI_{DD}3$ (Differential Amplifier)	$AV_{DD}3$ = 5 V	5.5	mA typ
$AI_{DD}4$ (Reference Buffer)	$AV_{DD}4$ = 5 V	5	mA typ
DI_{DD}[5]	MCLK = 40 MHz	20	mA typ
POWER DISSIPATION			
Normal Power Mode	MCLK = 40 MHz, decimate 128×	300	mW typ
		371	mW max
Low Power Mode	MCLK = 40 MHz, decimate 128×	160	mW typ
		215	mW max
Power-Down Mode[6]	$\overline{\text{PWRDWN}}$ held logic low	1	mW typ

[1] See Terminology section.
[2] SNR specifications in decibels are referred to a full-scale input, FS. Tested with an input signal at 0.5 dB below full scale, unless otherwise specified.
[3] Output data rate (ODR) = [(MCLK/2)]/decimation rate. That is, the maximum ODR for AD7765 = [(40 MHz/2)/128] = 156.25 kHz.
[4] Tested with a 400 µA load current.
[5] Tested at MCLK = 40 MHz. This current scales linearly with the MCLK frequency applied.
[6] Tested at 125°C.

TIMING SPECIFICATIONS

$AV_{DD}1 = DV_{DD} = 2.5$ V, $AV_{DD}2 = AV_{DD}3 = AV_{DD}4 = 5$ V, $V_{REF}+ = 4.096$ V, $T_A = 25°C$, $C_{LOAD} = 25$ pF.

Table 3.

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Description
f_{MCLK}	500	kHz min	Applied master clock frequency
	40	MHz max	
f_{ICLK}	250	kHz min	Internal modulator clock derived from MCLK
	20	MHz max	
t_1	$1 \times t_{ICLK}$	typ	SCO high period
t_2	$1 \times t_{ICLK}$	typ	SCO low period
t_3	1	ns typ	SCO rising edge to $\overline{FSO}$ falling edge
t_4	2	ns typ	Data access time, $\overline{FSO}$ falling edge to data active
t_5	8	ns max	MSB data access time, SDO active to SDO valid
t_6	40	ns min	Data hold time (SDO valid to SCO rising edge)
t_7	9.5	ns max	Data access time (SCO rising edge to SDO valid)
t_8	2	ns typ	SCO rising edge to $\overline{FSO}$ rising edge
t_9	$32 \times t_{SCO}$	max	$\overline{FSO}$ low period
t_{10}	12	ns min	Setup time from $\overline{FSI}$ falling edge to SCO falling edge
t_{11}	$1 \times t_{SCO}$	min	$\overline{FSI}$ low period
t_{12}[1]	$32 \times t_{SCO}$	max	$\overline{FSI}$ low period
t_{13}	12	ns min	SDI setup time for the first data bit
t_{14}	12	ns min	SDI setup time
t_{15}	0	ns max	SDI hold time
$t_{R\ MIN}$	$1 \times t_{MCLK}$	min	Minimum time for a valid $\overline{RESET}$ pulse
$t_{R\ HOLD}$	5	ns min	Minimum time between the MCLK rising edge and $\overline{RESET}$ rising edge
$t_{R\ SETUP}$	5	ns min	Minimum time between the $\overline{RESET}$ rising edge and MCLK rising edge
$t_{S\ MIN}$	$4 \times t_{MCLK}$	min	Minimum time for a valid $\overline{SYNC}$ pulse
$t_{S\ HOLD}$	5	ns min	Minimum time between the MCLK falling edge and $\overline{SYNC}$ rising edge
$t_{S\ SETUP}$	5	ns min	Minimum time between the $\overline{SYNC}$ rising edge and MCLK falling edge

[1] This is the maximum time $\overline{FSI}$ can be held low when writing to an individual device (a device that is not daisy-chained).

TIMING DIAGRAMS

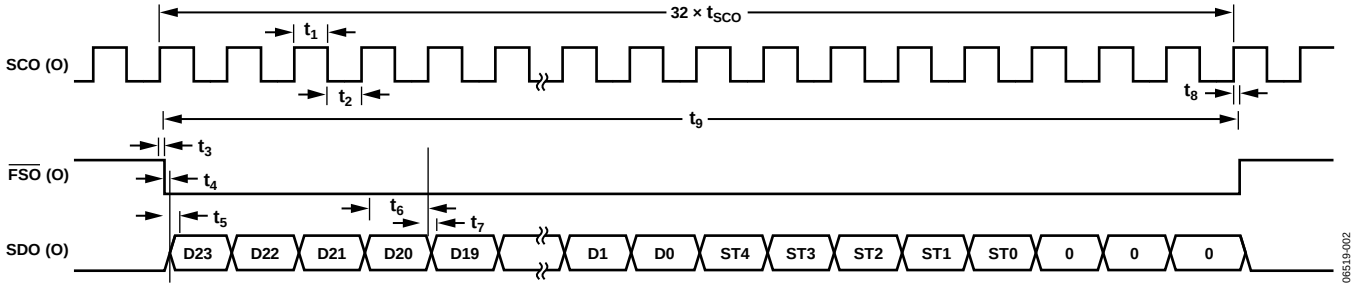


Figure 2. Serial Read Timing Diagram

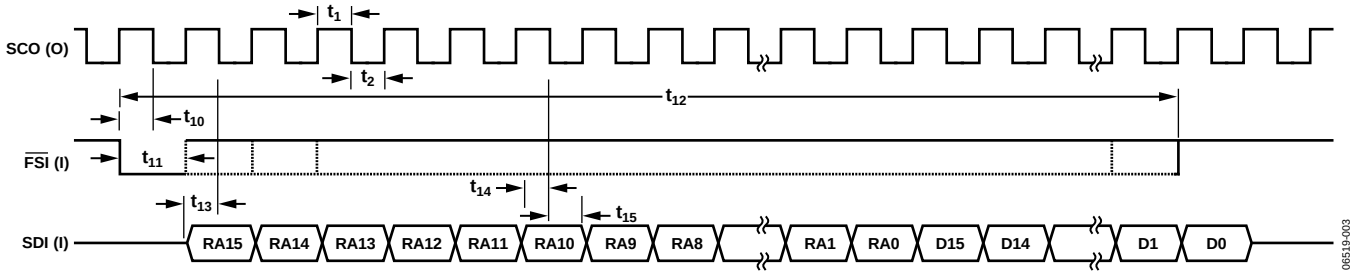


Figure 3. AD7765 Register Write

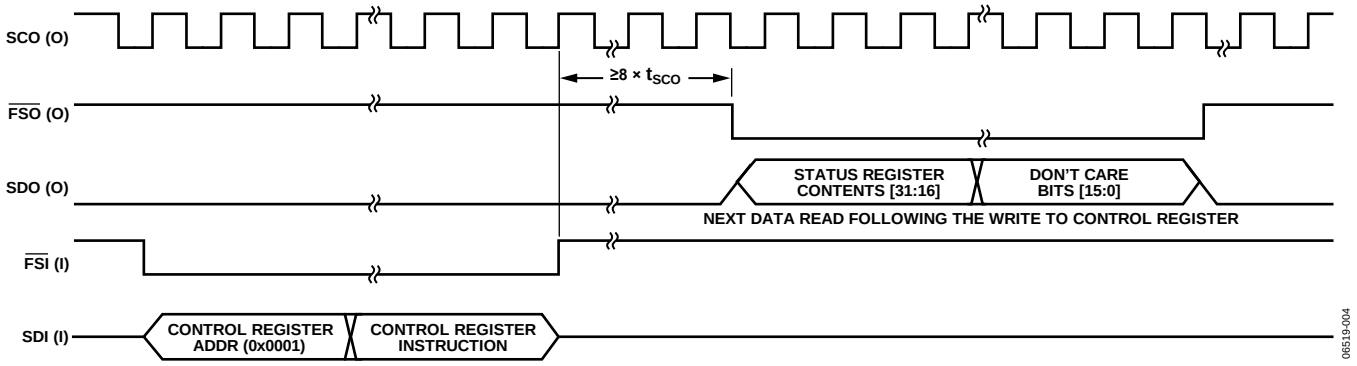


Figure 4. AD7765 Status Register Read Cycle

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameters	Rating
$AV_{DD}1$ to GND	−0.3 V to +2.8 V
$AV_{DD}2$, $AV_{DD}3$, $AV_{DD}4$ to GND	−0.3 V to +6 V
DV_{DD} to GND	−0.3 V to +2.8 V
$V_{IN}A+$, $V_{IN}A-$ to GND[1]	−0.3 V to +6 V
$V_{IN}+$, $V_{IN}-$ to GND[1]	−0.3 V to +6 V
Digital Input Voltage to GND[2]	−0.3 V to +2.8 V
$V_{REF}+$ to GND[3]	−0.3 V to +6 V
Input Current to Any Pin Except Supplies[4]	±10 mA
Operating Temperature Range	
Commercial	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
TSSOP Package	
θ_{JA} Thermal Impedance	143°C/W
θ_{JC} Thermal Impedance	45°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
ESD	1 kV

[1] Absolute maximum voltage for $V_{IN}-$, $V_{IN}+$, $V_{IN}A-$, and $V_{IN}A+$ is 6.0 V or $AV_{DD}3$ + 0.3 V, whichever is lower.
[2] Absolute maximum voltage on digital inputs is 3.0 V or DV_{DD} + 0.3 V, whichever is lower.
[3] Absolute maximum voltage on V_{REF+} input is 6.0 V or $AV_{DD}4$ + 0.3 V, whichever is lower.
[4] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

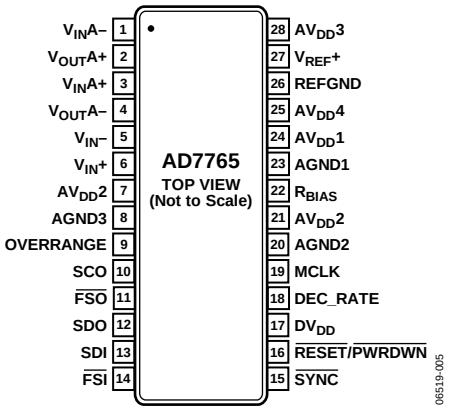


Figure 5. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
24	$AV_{DD}1$	2.5 V Power Supply for Modulator. This pin should be decoupled to AGND1 (Pin 23) with a 100 nF capacitor.
7 and 21	$AV_{DD}2$	5 V Power Supply. Pin 7 should be decoupled to AGND3 (Pin 8) with a 100 nF capacitor. Pin 21 should be decoupled to AGND1 (Pin 23) with a 100 nF capacitor.
28	$AV_{DD}3$	3.3 V to 5 V Power Supply for Differential Amplifier. This pin should be decoupled to the ground plane with a 100 nF capacitor.
25	$AV_{DD}4$	3.3 V to 5 V Power Supply for Reference Buffer. This pin should be decoupled to AGND1 (Pin 23) with a 100 nF capacitor.
17	DV_{DD}	2.5 V Power Supply for Digital Circuitry and FIR Filter. This pin should be decoupled to the ground plane with a 100 nF capacitor.
22	R_{BIAS}	Bias Current Setting Pin. This pin must be decoupled to the ground plane. For more details, see the Bias Resistor Selection section.
23	AGND1	Power Supply Ground for Analog Circuitry.
20	AGND2	Power Supply Ground for Analog Circuitry.
8	AGND3	Power Supply Ground for Analog Circuitry.
26	REFGND	Reference Ground. Ground connection for the reference voltage.
27	$V_{REF}+$	Reference Input.
1	$V_{IN}A-$	Negative Input to Differential Amplifier.
2	$V_{OUT}A+$	Positive Output from Differential Amplifier.
3	$V_{IN}A+$	Positive Input to Differential Amplifier.
4	$V_{OUT}A-$	Negative Output from Differential Amplifier.
5	$V_{IN}-$	Negative Input to the Modulator.
6	$V_{IN}+$	Positive Input to the Modulator.
9	OVERRANGE	Overrange Pin. This pin outputs a logic high to indicate that the user has applied an analog input that is approaching the limit of the analog input to the modulator.
10	SCO	Serial Clock Out. This clock signal is derived from the internal ICLK signal. The frequency of this clock is equal to ICLK. See the Clocking the AD7765 section for further details.
11	$\overline{FSO}$	Frame Sync Out. This signal frames the serial data output and is 32 SCO periods wide.
12	SDO	Serial Data Out. Data and status are output on this pin during each serial transfer. Each bit is clocked out on an SCO rising edge and is valid on the falling edge. See the AD7765 Interface section for further details.
13	SDI	Serial Data In. The first data bit (MSB) must be valid on the next SCO falling edge after the $\overline{FSI}$ event is latched. Thirty-two bits are required for each write; the first 16-bit word contains the device and register address and the second word contains the data. See the AD7765 Interface section for further details.

Pin No.	Mnemonic	Description
14	$\overline{\text{FSI}}$	Frame Sync Input. The status of this pin is checked on the falling edge of SCO. If this pin is low, then the first data bit is latched in on the next SCO falling edge. See the AD7765 Interface section for further details.
15	$\overline{\text{SYNC}}$	Synchronization Input. A falling edge on this pin resets the internal filter. This can be used to synchronize multiple devices in a system. See the Synchronization section for further details.
16	$\overline{\text{RESET}}$/ $\overline{\text{PWRDWN}}$	Reset/Power-Down Pin. When a logic low is sensed on this pin, the part is powered down and all internal circuitry is reset.
19	MCLK	Master Clock Input. A low jitter digital clock must be applied to this pin. The output data rate depends on the frequency of this clock. See the Clocking the AD7765 section for more details.
18	DEC_RATE	Decimation Rate. This pin selects one of the three decimation rate modes. When 2.5 V is applied to this pin, a decimation rate of 128× is selected. A decimation rate of 256× is selected by setting the pin to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

$AV_{DD}1 = DV_{DD} = 2.5$ V, $AV_{DD}2 = AV_{DD}3 = AV_{DD}4 = 5$ V, $V_{REF}+ = 4.096$ V, MCLK amplitude = 5 V, $T_A = 25°C$. Linearity plots measured to 16-bit accuracy; input signal reduced to avoid modulator overload and digital clipping; fast Fourier transforms (FFTs) generated from 8,192 samples.

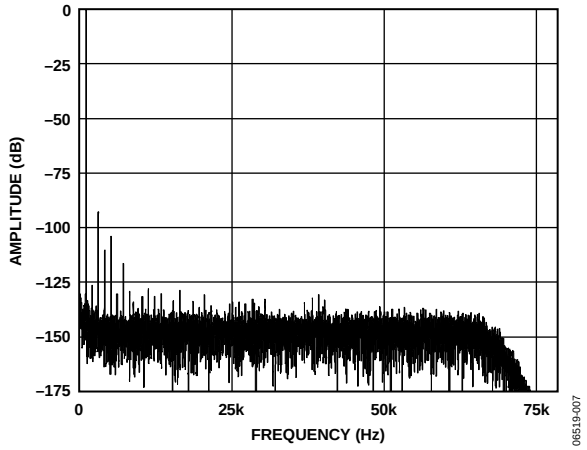


Figure 6. Normal Power Mode; FFT, 1 kHz, −0.5 dB Input Tone, 128× Decimation Rate

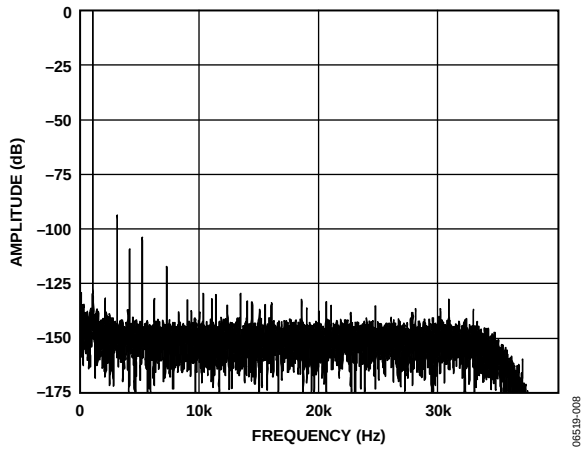


Figure 7. Normal Power Mode; FFT, 1 kHz, −0.5 dB Input Tone, 256× Decimation Rate

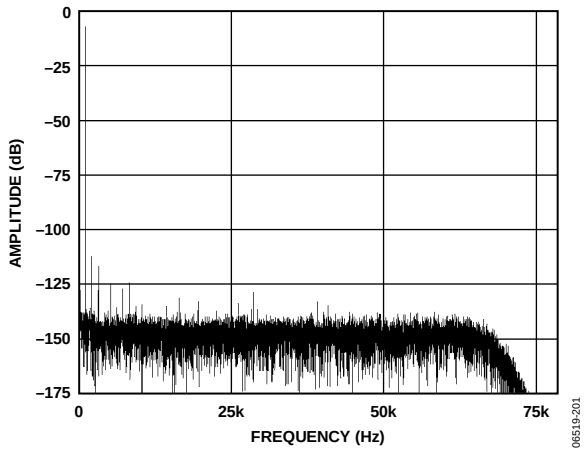


Figure 8. Normal Power Mode; FFT, 1 kHz, −6 dB Input Tone, 128× Decimation Rate

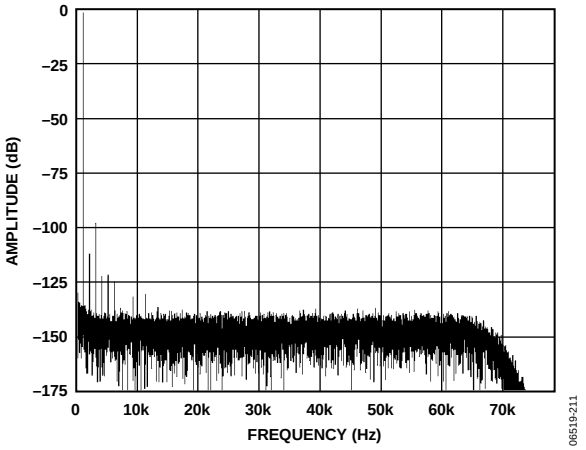


Figure 9. Low Power Mode; FFT, 1 kHz, −0.5 dB Input Tone, 128× Decimation Rate

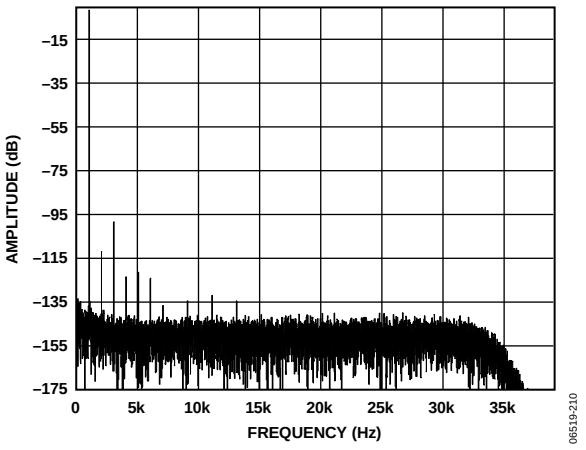


Figure 10. Low Power Mode; FFT, 1 kHz, −0.5 dB Input Tone, 256× Decimation Rate

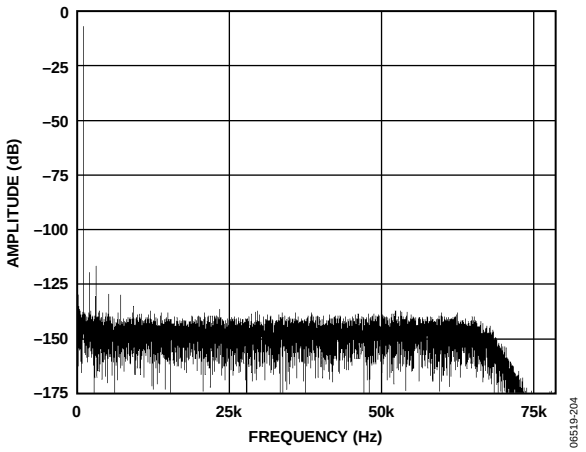


Figure 11. Low Power Mode; FFT, 1 kHz, −6 dB Input Tone, 128× Decimation Rate

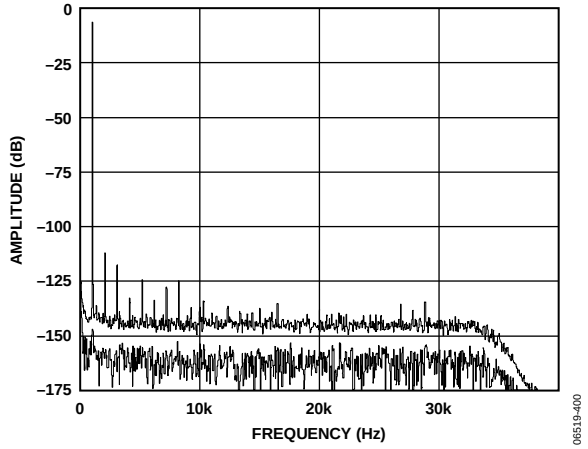


Figure 12. Normal Power Mode; FFT, 1 kHz, –6 dB Input Tone, 256× Decimation Rate

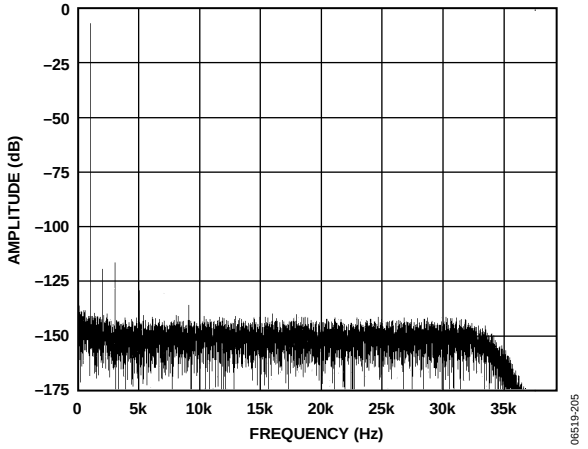


Figure 15. Low Power Mode; FFT, 1 kHz, –6 dB Input Tone, 256× Decimation Rate

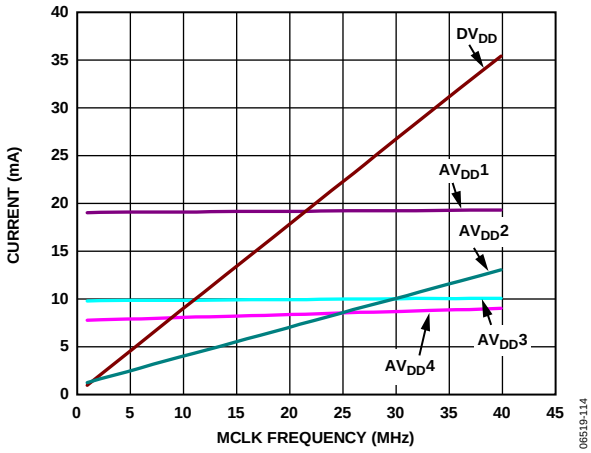


Figure 13. Normal Power Mode; Current Consumption vs. MCLK Frequency, 128× Decimation Rate

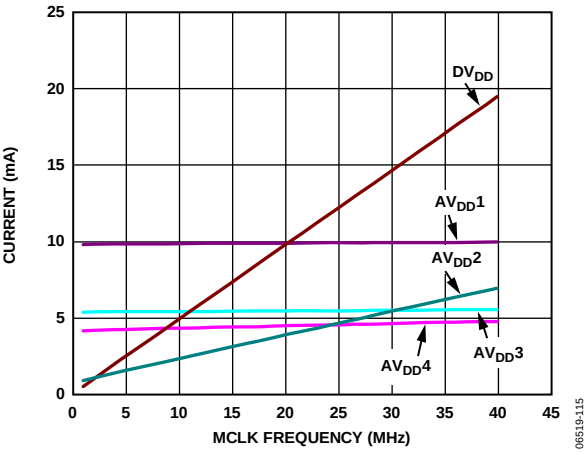


Figure 16. Low Power Mode; Current Consumption vs. MCLK Frequency, 128× Decimation Rate

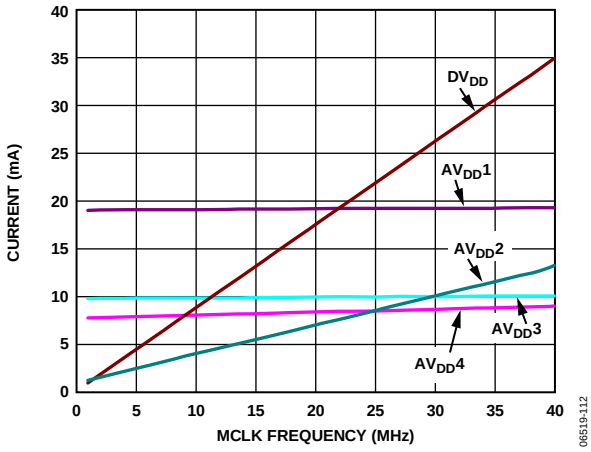


Figure 14. Normal Power Mode; Current Consumption vs. MCLK Frequency, 256× Decimation Rate

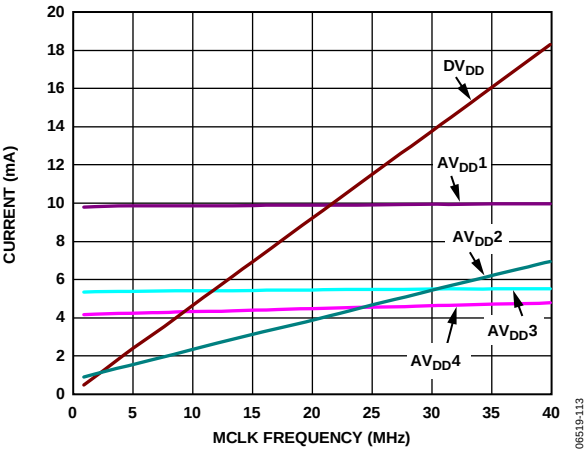


Figure 17. Low Power Mode; Current Consumption vs. MCLK Frequency, 256× Decimation Rate

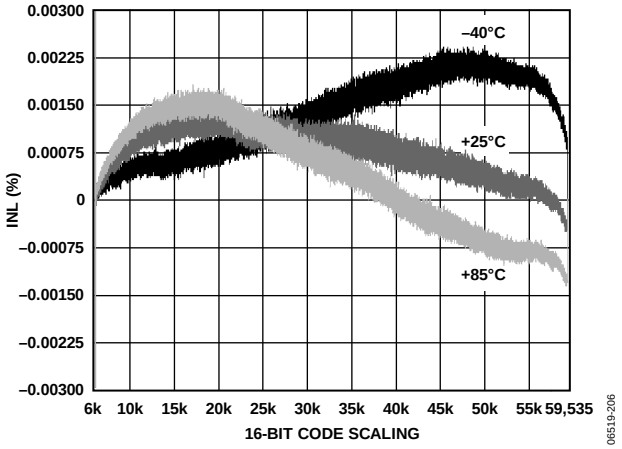


Figure 18. Normal Power Mode INL

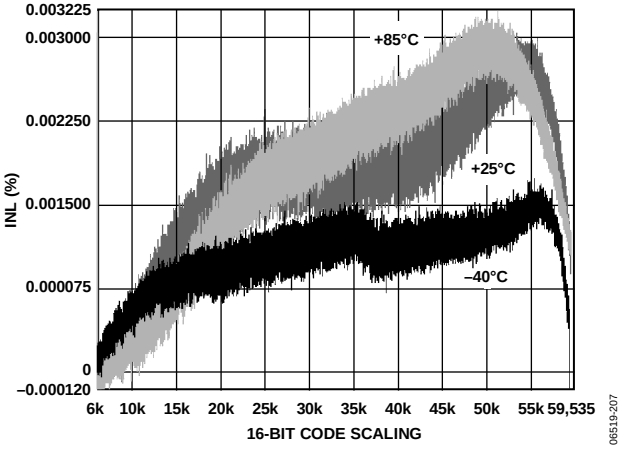


Figure 21. Low Power Mode INL

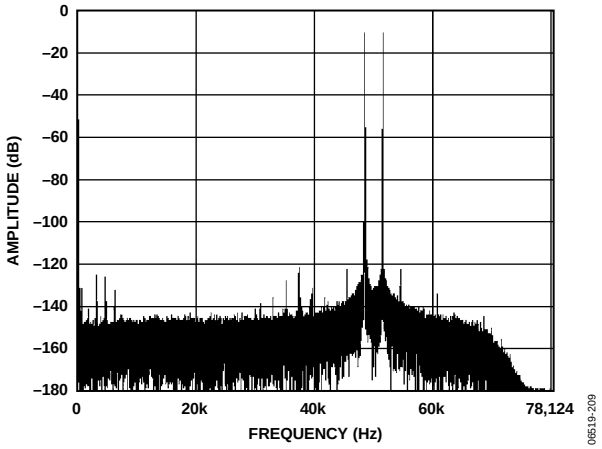


Figure 19. Normal Power Mode; IMD, f_{IN} A = 49.7 kHz, f_{IN} B = 50.3 kHz, 50 kHz Center Frequency, 128× Decimation Rate

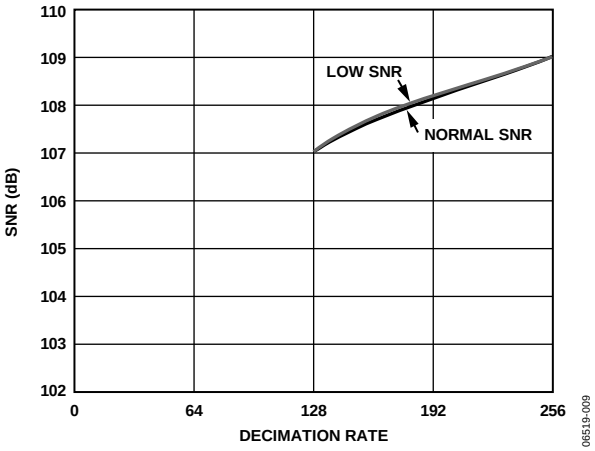


Figure 22. Normal and Low Power Mode; SNR vs. Decimation Rate, 1 kHz, –0.5 dB Input Tone

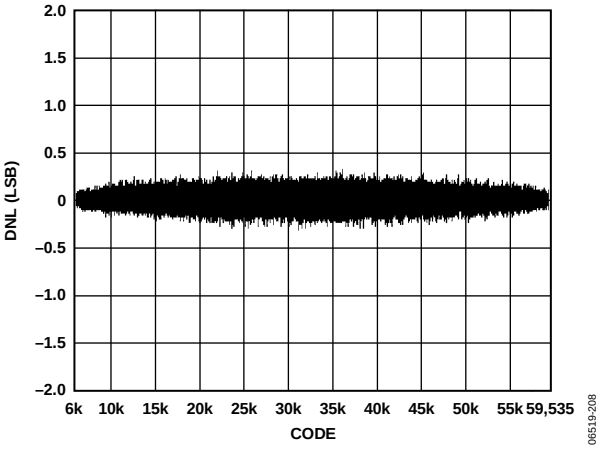


Figure 20. DNL Plot

TERMINOLOGY

Signal-to-Noise Ratio (SNR)
The ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels (dB).

Total Harmonic Distortion (THD)
The ratio of the rms sum of harmonics to the fundamental. For the AD7765, it is defined as

$$THD(\text{dB}) = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where:
V_1 is the rms amplitude of the fundamental.
V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second to the sixth harmonics.

Nonharmonic Spurious-Free Dynamic Range (SFDR)
The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component, excluding harmonics.

Dynamic Range
The ratio of the rms value of the full scale to the rms noise measured with the inputs shorted together. The value for dynamic range is expressed in dB.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3, and so on. Intermodulation distortion terms are those for which neither m nor n is equal to 0. For example, the second-order terms include (fa + fb) and (fa − fb), while the third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa − 2fb).

The AD7765 is tested using the CCIF standard, where two input frequencies near the top end of the input bandwidth are used. In this case, the second-order terms are usually distanced in frequency from the original sine waves and the third-order terms are usually at a frequency close to the input frequencies. As a result, the second- and third-order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification, that is, the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dB.

Integral Nonlinearity (INL)
The maximum deviation from a straight line passing through the endpoints of the ADC transfer function.

Differential Nonlinearity (DNL)
The difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Zero Error
The difference between the ideal midscale input voltage (when both inputs are shorted together) and the actual voltage producing the midscale output code.

Zero Error Drift
The change in the actual zero error value due to a temperature change of 1°C. It is expressed as a percentage of full scale at room temperature.

Gain Error
The first transition (from 100…000 to 100…001) should occur for an analog voltage 1/2 LSB above the nominal negative full scale. The last transition (from 011…110 to 011…111) should occur for an analog voltage 1 1/2 LSB below the nominal full scale. The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition, from the difference between the ideal levels.

Gain Error Drift
The change in the actual gain error value due to a temperature change of 1°C. It is expressed as a percentage of full scale at room temperature.

THEORY OF OPERATION

The AD7765 features an on-chip fully differential amplifier to feed the Σ-Δ modulator pins, an on-chip reference buffer, and a FIR filter block to perform the required digital filtering of the Σ-Δ modulator output. Using this Σ-Δ conversion technique with the added digital filtering, the analog input is converted into an equivalent digital word.

Σ-Δ MODULATION AND DIGITAL FILTERING

The input waveform applied to the modulator is sampled, and an equivalent digital word is output to the digital filter at a rate equal to ICLK. By employing oversampling, the quantization noise is spread across a wide bandwidth from 0 to f_{ICLK}. This means that the noise energy contained in the signal band of interest is reduced (see Figure 23). To further reduce the quantization noise, a high order modulator is employed to shape the noise spectrum so that most of the noise energy is shifted out of the signal band (see Figure 24).

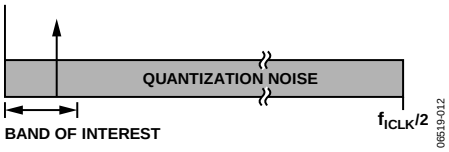


Figure 23. Σ-Δ ADC, Quantization Noise

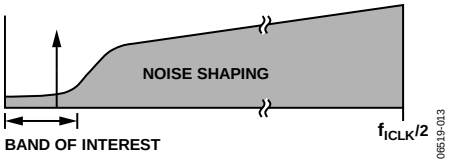


Figure 24. Σ-Δ ADC, Noise Shaping

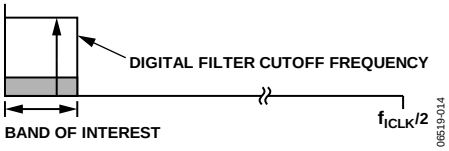


Figure 25. Σ-Δ ADC, Digital Filter Cutoff Frequency

The digital filtering that follows the modulator removes the large out-of-band quantization noise (see Figure 25) while also reducing the data rate from f_{ICLK} at the input of the filter to $f_{ICLK}/128$ or less at the output of the filter, depending on the decimation rate used.

The AD7765 employs three FIR filters in series. By using different combinations of decimation ratios, data can be obtained from the AD7765 at three data rates.

The first filter receives data from the modulator at ICLK MHz where it is decimated 4× to output data at (ICLK/4) MHz. The second filter allows a choice of decimation rates: 16× or 32×.

The third filter has a fixed decimation rate of 2×. Table 6 shows some characteristics of the digital filtering where ICLK = MCLK/2. The group delay of the filter is defined to be the delay to the center of the impulse response and is equal to the computation plus the filter delays. The delay until valid data is available (the FILTER-SETTLE status bit is set) is approximately twice the filter delay plus the computation delay. This is listed in terms of MCLK periods in Table 6.

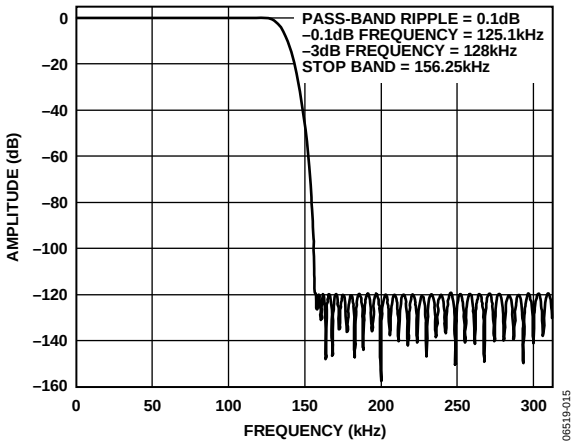


Figure 26. Filter Frequency Response (156.25 kHz ODR)

Table 6. Configuration with Default Filter

ICLK Frequency	Decimation Rate	Data State	Computation Delay	Filter Delay	$\overline{SYNC}$ to FILTER-SETTLE	Pass-Band Bandwidth	Output Data Rate (ODR)
20 MHz	128×	Fully filtered	3.1 µs	174 µs	14217 × t_{MCLK}	62.5 kHz	156.25 kHz
20 MHz	256×	Fully filtered	4.65 µs	346.8 µs	27895 × t_{MCLK}	31.25 kHz	78.125 kHz
12.288 MHz	128×	Fully filtered	5.05 µs	283.2 µs	14217 × t_{MCLK}	38.4 kHz	96 kHz
12.288 MHz	256×	Fully filtered	7.57 µs	564.5 µs	27895 × t_{MCLK}	19.2 kHz	48 kHz

AD7765 ANTIALIAS PROTECTION

The decimation of the AD7765, along with its counterparts in the AD776x family, namely the AD7760, AD7762, AD7763, and AD7764, provides top of the range antialias protection.

The decimation filter of the AD7765 features more than 115 dB of attenuation across the full stop band, which ranges from the Nyquist frequency, namely ODR/2, up to ICLK − ODR/2 (where ODR is the output data rate). Starting the stop band at the Nyquist frequency prevents any signal component above Nyquist (and up to ICLK − ODR/2) from aliasing into the desired signal bandwidth.

Figure 26 shows the frequency response of the decimation filter when the AD7765 is operated with a 40 MHz MCLK in decimate 128× mode. Note that the first stop-band frequency occurs at Nyquist. The frequency response of the filter scales with both the decimation rate chosen and the MCLK frequency applied. When using low power mode, the modulator sample rate is MCLK/4.

Taking as an example the AD7765 in normal power and in decimate 128× mode, the first possible alias frequency is at the ICLK frequency minus the pass band of the digital filter (see Figure 27).

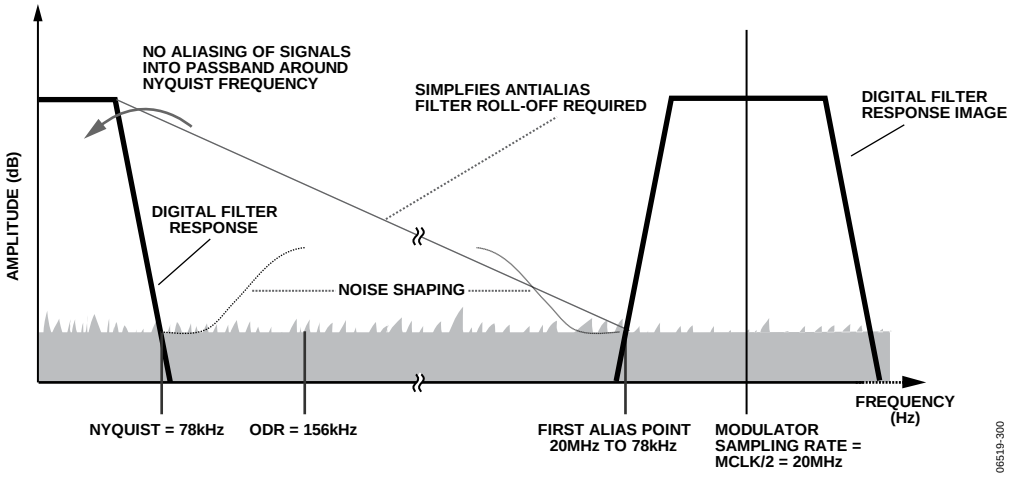


Figure 27. Antialias Example Using the AD7765 in Normal Mode, Decimate 128× Using MCLK/2 = ICLK = 20 MHz

AD7765 INPUT STRUCTURE

The AD7765 requires a 4.096 V input to the reference pin $V_{REF}+$, supplied by a high precision reference, such as the ADR444. Because the input to the device's Σ-Δ modulator is fully differential, the effective differential reference range is 8.192 V.

$$V_{REF+(Diff)} = 2 \times 4.096 = 8.192\,V$$

As is inherent in Σ-Δ modulators, only a certain portion of this full reference may be used. In the case of the AD7765, 80% of the full differential reference can be applied to the modulator's differential inputs.

$$Modulator\_Input_{FULLSCALE} = 8.192\,V \times 0.8 = 6.5536\,V$$

This means that a maximum of ±3.2768 V p-p can be applied to each of the AD7765 modulator inputs (Pin 5 and Pin 6), with the AD7765 being specified with an input −0.5 dB down from full scale (−0.5 dBFS). The AD7765 modulator inputs must have a common-mode input of 2.048 V.

Figure 28 shows the relative scaling between the differential voltages applied to the modulator pins and the respective 24-bit twos complement digital outputs.

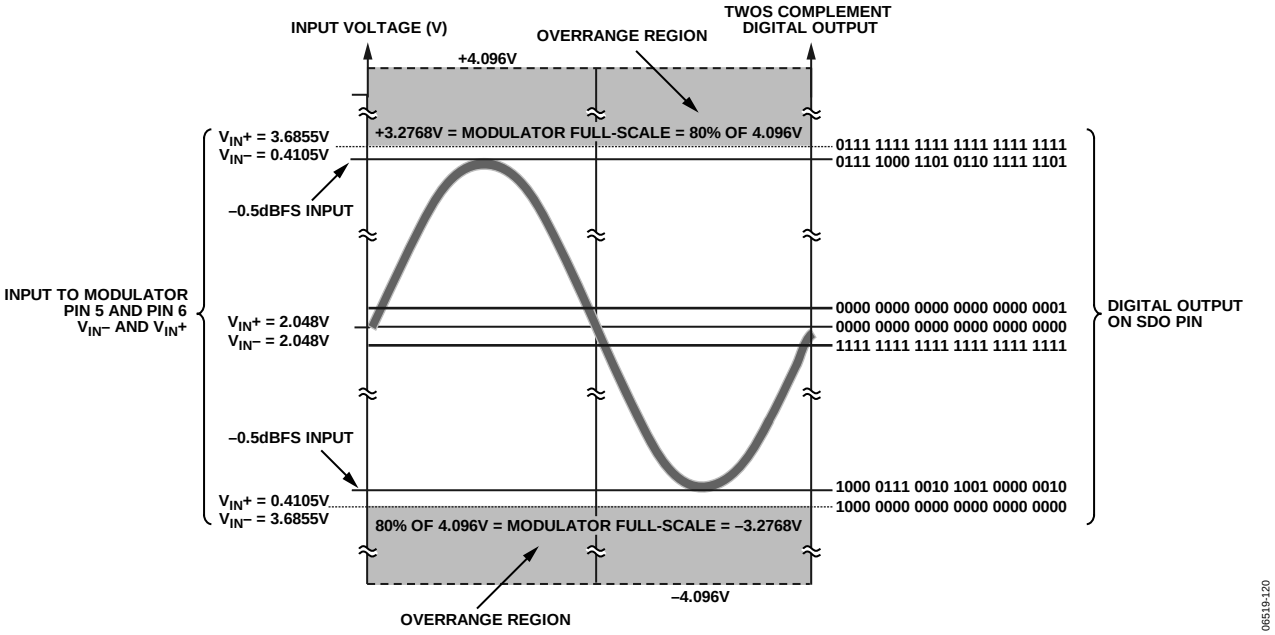


Figure 28. AD7765 Scaling; Modulator Input Voltage vs. Digital Output Code

ON-CHIP DIFFERENTIAL AMPLIFIER

The AD7765 contains an on-board differential amplifier that is recommended to drive the modulator input pins. Pin 1, Pin 2, Pin 3, and Pin 4 on the AD7765 are the differential input and output pins of the amplifier. The external components, R_{IN}, R_{FB}, C_{FB}, C_S, and R_M, are placed around Pin 1 through Pin 6 to create the recommended configuration. To achieve the specified performance, the differential amplifier should be configured as a first-order antialias filter, as shown in Figure 29, using the component values listed in Table 7. The inputs to the differential amplifier are then routed through this external component network before being applied to the modulator inputs $V_{IN}-$ and $V_{IN}+$(Pin 5 and Pin 6). Using the optimal values in the table as an example yields a 25 dB attenuation at the first alias point of 19.84 MHz.

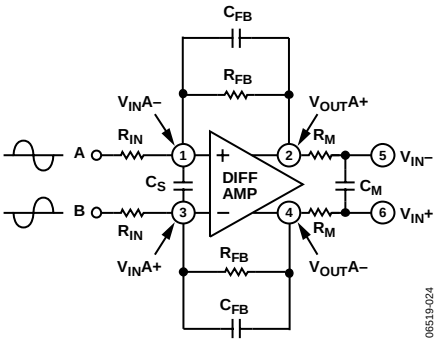


Figure 29. Differential Amplifier Configuration

Table 7. On-Chip Differential Filter Component Values

	R_{IN} (kΩ)	R_{FB} (kΩ)	R_M (Ω)	C_S (pF)	C_{FB} (pF)	C_M (pF)
Optimal	4.75	3.01	43	8.2	47	33
Tolerance Range[1]	2.37 to 5.76	2.4 to 4.87	36 to 47	0 to 10	20 to 100	39 to 56

[1] Values shown were the acceptable tolerances for each component when altered relative to the optimal values used to achieve the stated specifications of the device.

The range of values that can be used for each of the listed components in the differential amplifier configuration is also listed in Table 7. When using the differential amplifier to gain the input voltages to the required modulator input range, it is advisable to implement the gain function by changing R_{IN}, leaving the R_{FB} as the listed optimal value.

The common-mode input at each of the differential amplifier inputs (Pin $V_{IN}A+$ and Pin $V_{IN}A-$) can range from−0.5 V dc to 2.2 V dc. The amplifier has a constant output common-mode voltage of 2.048 V, that is, $V_{REF}/2$, the requisite common-mode voltage for the modulator input pins ($V_{IN}+$ and $V_{IN}-$).

Figure 30 shows the signal conditioning that occurs using the differential amplifier configuration detailed in Table 7 with a ±2.5 V input signal to the differential amplifier. The amplifier in this example is biased around ground and is scaled to give ±3.168 V p-p (−0.5 dBFS) on each modulator input with a 2.048 V common mode.

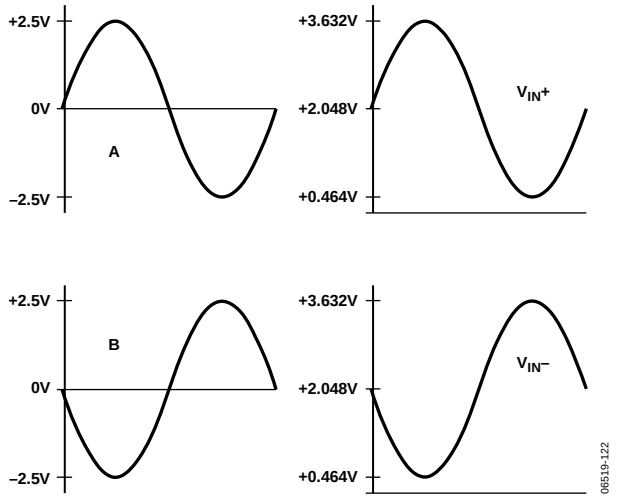


Figure 30. Differential Amplifier Signal Conditioning

To obtain maximum performance from the AD7765, it is advisable to drive the ADC with differential signals. Figure 31 shows how a bipolar, single-ended signal biased around ground can drive the AD7765 with the use of an external op amp, such as the AD8021.

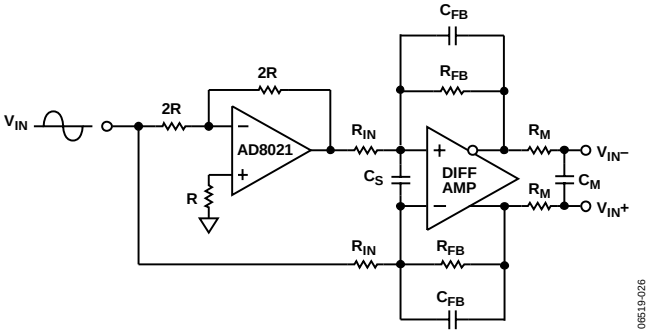


Figure 31. Single-Ended-to-Differential Conversion

MODULATOR INPUT STRUCTURE

The AD7765 employs a double-sampling front end, as shown in Figure 32. For simplicity, only the equivalent input circuitry for $V_{IN}+$ is shown. The equivalent circuitry for $V_{IN}-$ is the same.

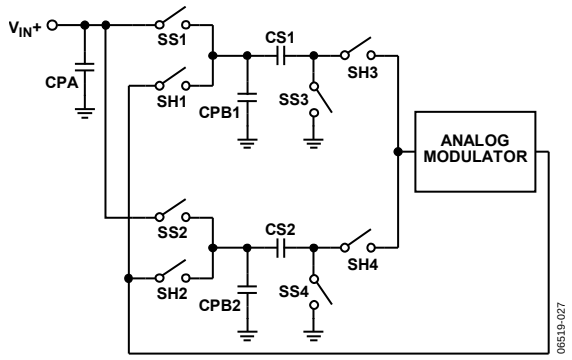


Figure 32. Equivalent Input Circuit

The SS1 and SS3 sampling switches are driven by ICLK, whereas the SS2 and SS4 sampling switches are driven by $\overline{ICLK}$. When ICLK is high, the analog input voltage is connected to CS1. On the falling edge of ICLK, the SS1 and SS3 switches open and the analog input is sampled on CS1. Similarly, when ICLK is low, the analog input voltage is connected to CS2. On the rising edge of ICLK, the SS2 and SS4 switches open, and the analog input is sampled on CS2.

The CPA, CPB1, and CPB2 capacitors represent parasitic capacitances that include the junction capacitances associated with the MOS switches.

Table 8. Equivalent Component Values

CS1	CS2	CPA	CPB1/CPB2
13 pF	13 pF	13 pF	5 pF

DRIVING THE MODULATOR INPUTS DIRECTLY

The AD7765 can be configured so that the on-board differential amplifier can be disabled and the modulator can be driven directly using discrete amplifiers. This allows the user to lower the power dissipation.

To power down the on board differential amplifier, the user issues a write to set the AMP OFF bit in the control register to logic high (see Figure 33).

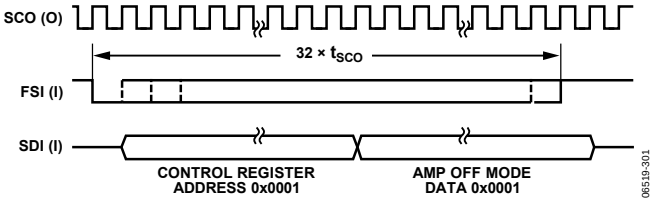


Figure 33. Writing to the AD7765 Control Register Turning Off the On-Board Differential Amplifier

The AD7765 modulator inputs must have a common-mode voltage of 2.048 V and adhere to the amplitudes as described in the AD7765 Input Structure section.

An example of a typical circuit to drive the AD7765 for applications requiring excellent ac and dc performance is shown in Figure 34. Either the AD8606 or AD8656 can be used to drive the AD7765 modulator inputs directly.

Best practice is to short the differential amplifier inputs to ground through the typical input resistors and leave the typical feedback resistors in place.

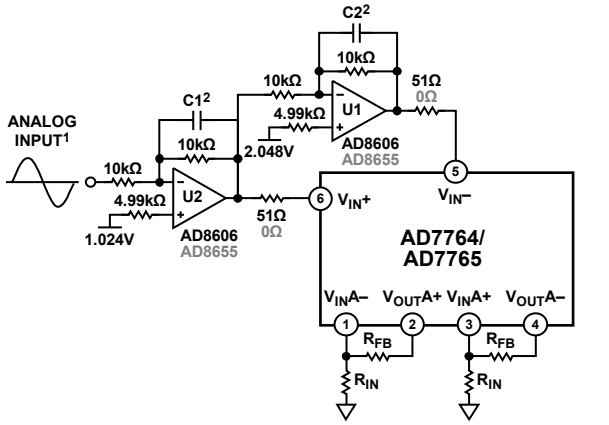


Figure 34. Driving the AD7765 Modulator Inputs Directly from a Single-Ended Source (On-Board Differential Amplifier Powered Down)

AD7765 INTERFACE

READING DATA

The AD7765 uses an SPI-compatible serial interface. The timing diagram in Figure 2 shows how the AD7765 transmits its conversion results.

The data read from the AD7765 is clocked out using the serial clock output (SCO). The SCO frequency is half that of the MCLK input to the AD7765.

The conversion result output on the serial data output (SDO) line is framed by the frame synchronization output, $\overline{\text{FSO}}$, which is sent logic low for 32 SCO cycles. Each bit of the new conversion result is clocked onto the SDO line on the rising SCO edge and is valid on the falling SCO edge. The 32-bit result consists of the 24 data bits followed by five status bits followed further by three zeros. The five status bits are listed in Table 9 and described below the table.

Table 9. Status Bits During Data Read

D7	D6	D5	D4	D3
FILTER-SETTLE	OVR	LPWR	DEC_RATE 1	Don't care

- The FILTER-SETTLE bit indicates whether the data output from the AD7765 is valid. After resetting the device (using the $\overline{\text{RESET}}$ pin) or clearing the digital filter (using the $\overline{\text{SYNC}}$ pin), the FILTER-SETTLE bit goes logic low to indicate that the full settling time of the filter has not yet passed and that the data is not yet valid. The FILTER-SETTLE bit also goes to zero when the input to the part has asserted the overrange alerts.
- The OVR (overrange) bit is described in the Overrange Alerts section.
- The LPWR bit is set to logic high when the AD7765 is operating in low power mode. See the Power Modes section for further details.
- The DEC_RATE 1 and DEC_RATE 0 bits indicate the decimation ratio used. Table 10 is a truth table for the decimation rate bits.

Table 10. Truth Table

Decimate	DEC_RATE 1
128×	1
256×	0

READING STATUS AND OTHER REGISTERS

The AD7765 features a gain correction register, an overrange register, and a read-only status register. To read back the contents of these registers, the user must first write to the control register of the device and set the bit that corresponds to the register to be read. The next read operation outputs the contents of the selected register (on the SDO pin) instead of a conversion result.

To ensure that the next read cycle contains the contents of the register written to, the write operation to that register must be completed a minimum of $8 \times t_{SCO}$ before the falling edge of $\overline{\text{FSO}}$, which indicates the start of the next read cycle. See Figure 4 for further details.

The AD7765 Registers section provides more information on the relevant bits in the control register.

WRITING TO THE AD7765

A write operation to the AD7765 is shown in Figure 3. The serial writing operation is synchronous to the SCO signal. The status of the frame synchronization input, $\overline{\text{FSI}}$, is checked on the falling edge of the SCO signal. If the $\overline{\text{FSI}}$ line is low, then the first data bit on the serial data in (SDI) line is latched in on the next SCO falling edge.

Set the active edge of the $\overline{\text{FSI}}$ signal to occur at a position when the SCO signal is high or low to allow setup and hold times from the SCO falling edge to be met. The width of the $\overline{\text{FSI}}$ signal can be set to between 1 and 32 SCO periods wide. A second, or subsequent, falling edge that occurs before 32 SCO periods have elapsed is ignored.

Figure 3 details the format for the serial data being written to the AD7765 through the SDI pin. Thirty-two bits are required for a write operation. The first 16 bits are used to select the register address for which the data being read is intended. The second 16 bits contain the data for the selected register.

Writing to the AD7765 is allowed at any time, even while reading a conversion result. Note that, after writing to the devices, valid data is not output until after the settling time for the filter has elapsed. The FILTER-SETTLE status bit is asserted at this point to indicate that the filter has settled and that valid data is available at the output.

AD7765 FUNCTIONALITY

SYNCHRONIZATION

The $\overline{\text{SYNC}}$ input to the AD7765 provides a synchronization function that allows the user to begin gathering samples of the analog front-end input from a known point in time.

The $\overline{\text{SYNC}}$ function allows multiple AD7765 devices, operated from the same master clock that use common $\overline{\text{SYNC}}$ and $\overline{\text{RESET}}$ signals, to be synchronized so that each ADC simultaneously updates its output register. Note that all devices being synchronized must operate in the same power mode and at the same decimation rate.

In the case of a system with multiple AD7765s, connect common MCLK, $\overline{\text{SYNC}}$, and $\overline{\text{RESET}}$ signals to each AD7765.

The AD7765 $\overline{\text{SYNC}}$ pin is polled by the falling edge of MCLK. The AD7765 device goes into $\overline{\text{SYNC}}$ when an MCLK falling edge senses that the $\overline{\text{SYNC}}$ input signal is logic low. At this point, the digital filter sequencer is reset to 0. The filter is held in a reset state (in $\overline{\text{SYNC}}$ mode) until the first MCLK falling edge senses $\overline{\text{SYNC}}$ to be logic high.

Where possible, ensure that all transitions of $\overline{\text{SYNC}}$ occur synchronously with the rising edge of MCLK (that is, as far away as possible from MCLK falling edge, or decision edge). Otherwise, abide by the timing specified in Figure 35, which excludes the $\overline{\text{SYNC}}$ rising edge from occurring in a 10 ns window centered around the MCLK falling edge.

Keep $\overline{\text{SYNC}}$ logic low for a minimum of four MCLK periods. When the MCLK falling edge senses that $\overline{\text{SYNC}}$ has returned to logic high, the AD7765 filters begin to gather input samples simultaneously. The $\overline{\text{FSO}}$ falling edges are also synchronized, allowing for simultaneous output of conversion data.

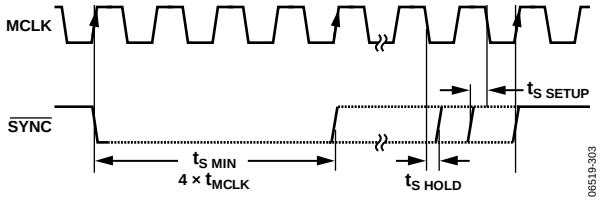


Figure 35. $\overline{\text{SYNC}}$ Timing Relative to MCLK

Following a $\overline{\text{SYNC}}$, the digital filter needs time to settle before valid data can be read from the AD7765. The user knows there is valid data on the SDO line by checking the FILTER-SETTLE status bit (see D7 in Table 9) that is output with each conversion result. The time from the rising edge of $\overline{\text{SYNC}}$ until the FILTER-SETTLE bit asserts depends on the filter configuration used. See the Theory of Operation section and the values listed in Table 6 for details on calculating the time until FILTER-SETTLE asserts.

Note that the FILTER-SETTLE bit is designed as a reactionary flag to alert the user when the conversion data output is valid.

OVERRANGE ALERTS

The AD7765 offers an overrange function in both a pin and status bit output. The overrange alerts indicate when the voltage applied to the AD7765 modulator input pins exceeds the limit set in the overrange register, indicating that the voltage applied is approaching an overrange level for the modulator. To set this limit, the user must program the register. The default overrange limit is set to 80% of the $V_{REF}+$ voltage (see the AD7765 Registers section).

The OVERRANGE pin outputs logic high to alert the user that the modulator has sampled an input voltage greater in magnitude than the overrange limit as set in the overrange register. The OVERRANGE pin is set to logic high when the modulator samples an input above the overrange limit. After the input returns below the limit, the OVERRANGE pin returns to zero. The OVERRANGE pin is updated after the first FIR filter stage. Its output changes at the ICLK/4 frequency.

The OVR status bit is output as Bit D6 on SDO during a data conversion and can be checked in the AD7765 status register. This bit is less dynamic than the OVERRANGE pin output. It is updated on each conversion result output; that is, the bit changes at the output data rate. If the modulator has sampled a voltage input that exceeded the overrange limit during the process of gathering samples for a particular conversion result output, then the OVR bit is set to logic high.

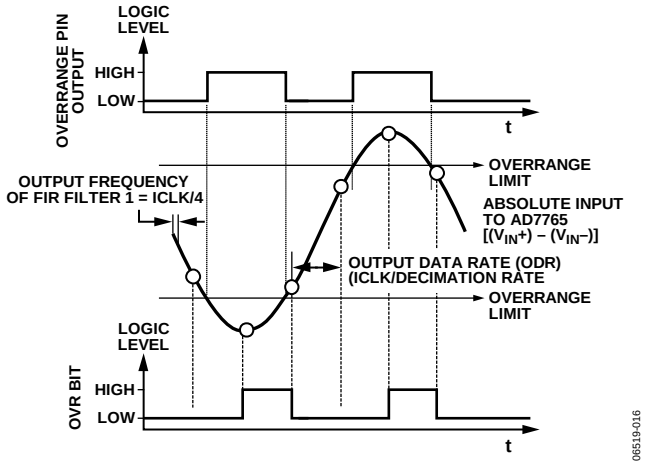


Figure 36. OVERRANGE Pin and OVR Bit vs. Absolute Voltage Applied to Modulator

The output points from FIR Filter 1 in Figure 36 are not drawn to scale relative to the output data rate points. The FIR Filter 1 output is updated either 16× or 32× faster than the output data rate, depending on the decimation rate in operation.

POWER MODES

Low Power Mode

During power-up, the AD7765 defaults to operate in normal power mode. There is no register write required.

The AD7765 also offers low power mode. To operate the device in low power mode, the user sets the LPWR bit in the control register to logic high (see Figure 37). Operating the AD7765 in low power mode has no impact on the output data rate or available bandwidth.

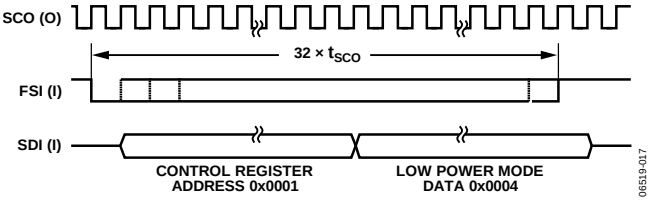


Figure 37. Write Scheme for Low Power Mode

$\overline{\text{RESET}}$/$\overline{\text{PWRDWN}}$ Mode

The AD7765 features a $\overline{\text{RESET}}$/$\overline{\text{PWRDWN}}$ pin. Holding the input to this pin logic low places the AD7765 in power-down mode. All internal circuitry is reset. Apply a $\overline{\text{RESET}}$ pulse to the AD7765 after initial power-up of the device.

The AD7765 RESET pin is polled by the rising edge of MCLK. The AD7765 device goes into reset when an MCLK rising senses the $\overline{\text{RESET}}$ input signal to be logic low. AD7765 comes out of $\overline{\text{RESET}}$ on the first MCLK rising edge that senses $\overline{\text{RESET}}$ to be logic high.

The best practice is to ensure that all transitions of $\overline{\text{RESET}}$ occur synchronously with the falling edge of MCLK; otherwise, adhere to the timing requirements shown in Figure 38.

$\overline{\text{RESET}}$ should be kept logic low for a minimum of 1 MCLK period for a valid reset to occur.

In cases where multiple AD7765 devices are being synchronized using the $\overline{\text{SYNC}}$ pulse and in the case of daisy chaining multiple AD7765 devices, a common $\overline{\text{RESET}}$ pulse must be provided in addition to the common $\overline{\text{SYNC}}$ and MCLK signals.

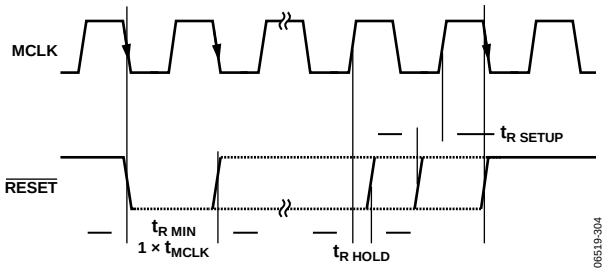


Figure 38. $\overline{\text{RESET}}$ Timing Synchronous to MCLK

DECIMATION RATE PIN

The decimation rate of the AD7765 is selected using the DEC_RATE pin. Table 11 shows the voltage input settings required for each of the three decimation rates.

Table 11. DEC_RATE Pin Settings

Decimate	DEC_RATE Pin	Maximum Output Data Rate
128×	DV_{DD}	156.25 kHz
256×	GND	78.125 kHz

DAISY CHAINING

Daisy chaining allows numerous devices to use the same digital interface lines. This feature is especially useful for reducing component count and wiring connections, such as in isolated multiconverter applications or for systems with a limited interfacing capacity. Data readback is analogous to clocking a shift register. When daisy chaining is used, all devices in the chain must operate in a common power mode and at a common decimation rate.

The block diagram in Figure 39 shows how to connect devices to achieve daisy-chain functionality. Figure 39 shows four AD7765 devices daisy-chained together with a common MCLK signal applied.

READING DATA IN DAISY-CHAIN MODE

Referring to Figure 39, note that the SDO line of AD7765 (A) provides the output data from the chain of AD7765 converters. Also, note that for the last device in the chain, AD7765 (D), the SDI pin is connected to ground. All of the devices in the chain must use common MCLK and $\overline{\text{SYNC}}$ signals.

To enable the daisy-chain conversion process, apply a common $\overline{\text{SYNC}}$ pulse to all devices (see the Synchronization section).

After a $\overline{\text{SYNC}}$ pulse is applied to all devices, the filter settling time must pass before the FILTER-SETTLE bit is asserted indicating valid conversion data at the output of the chain of devices. As shown in Figure 40, the first conversion result is output from the device labeled AD7765 (A). This 32-bit conversion result is then followed by the conversion results from the devices AD7765 (B), AD7765 (C), and AD7765 (D), with all conversion results output in an MSB-first sequence. The signals output from the daisy chain are the stream of conversion results from the SDO pin of AD7765 (A) and the $\overline{\text{FSO}}$ signal output by the first device in the chain, AD7765 (A).

The falling edge of $\overline{\text{FSO}}$ signals the MSB of the first conversion output in the chain. $\overline{\text{FSO}}$ stays logic low throughout the 32 SCO clock periods needed to output the AD7765 (A) result and then goes logic high during the output of the conversion results from the AD7765 (B), AD7765 (C), and AD7765 (D) devices.

The maximum number of devices that can be daisy-chained is dependent on the decimation rate selected. Calculate the maximum number of devices that can be daisy-chained by simply dividing the chosen decimation rate by 32 (the number of bits that must be clocked out for each conversion). Table 12 provides the maximum number of chained devices for each decimation rate.

Table 12. Maximum Chain Length for All Decimation Rates

Decimation Rate	Maximum Chain Length
256×	8
128×	4

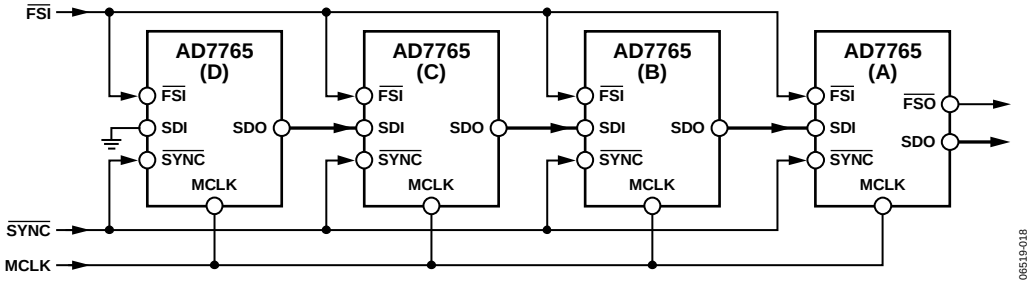


Figure 39. Daisy Chaining Four Devices in Decimate 128× Mode Using a 40 MHz MCLK Signal

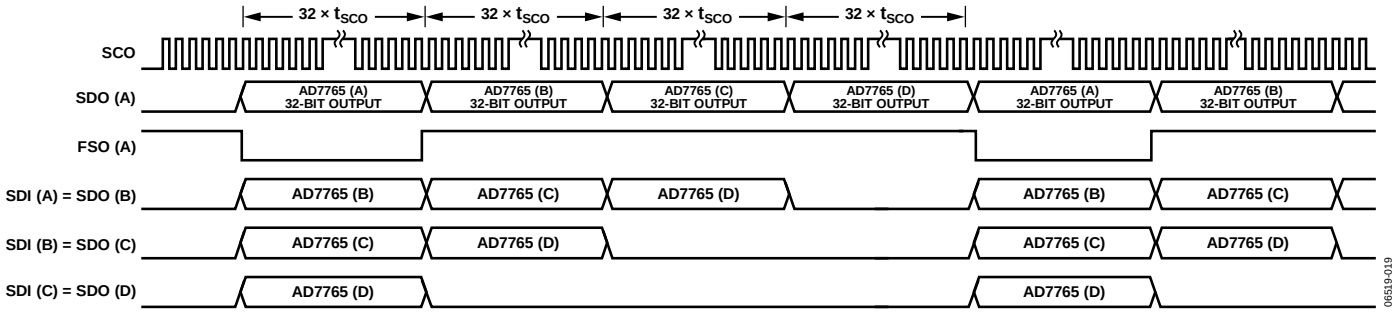


Figure 40. Daisy-Chain Mode, Data Read Timing Diagram (for the Daisy-Chain Configuration Shown in Figure 39)

WRITING DATA IN DAISY-CHAIN MODE

Writing to AD7765 devices in daisy-chain mode is similar to writing to a single device. The serial writing operation is synchronous to the SCO signal. The status of the frame synchronization input, $\overline{FSI}$, is checked on the falling edge of the SCO signal. If the $\overline{FSI}$ line is low, then the first data bit on the serial data in the SDI line is latched in on the next SCO falling edge.

Writing data to the AD7765 in daisy-chain mode operates with the same timing structure as writing to a single device (see Figure 3). The difference between writing to a single device and writing to a number of daisy-chained devices is in the implementation of the $\overline{FSI}$ signal. The number of devices that are in the daisy chain determines the period for which the $\overline{FSI}$ signal must remain logic low. To write to n number of devices in the daisy chain, the period between the falling edge of $\overline{FSI}$ and the rising edge of $\overline{FSI}$ must be between 32 × (n − 1) to 32 × n SCO periods. For example, if three AD7765 devices are being written to in daisy-chain mode, $\overline{FSI}$ is logic low for between 32 × (3 − 1) to 32 × 3 SCO pulses. This means that the rising edge of FSI must occur between the 64th and 96th SCO period.

The AD7765 devices can be written to at any time. The falling edge of $\overline{FSI}$ overrides all attempts to read data from the SDO pin. In the case of a daisy chain, the $\overline{FSI}$ signal remaining logic low for more than 32 SCO periods indicates to the AD7765 device that there are more devices further on in the chain. This means that the AD7765 directs data that is input on the SDI pin to its SDO pin. This ensures that data is passed to the next device in the chain.

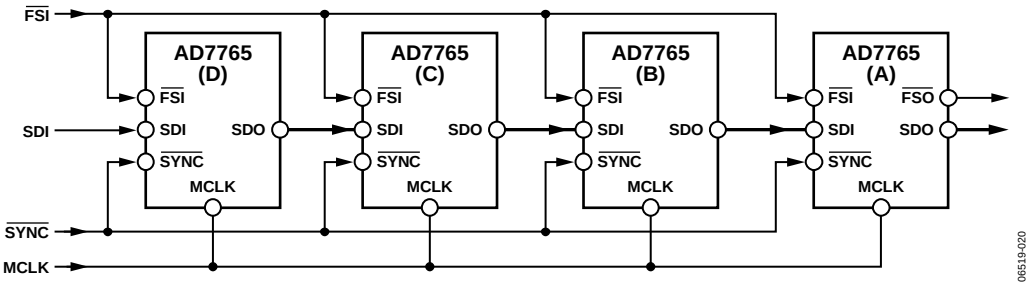


Figure 41. Writing to an AD7765 Daisy-Chain Configuration

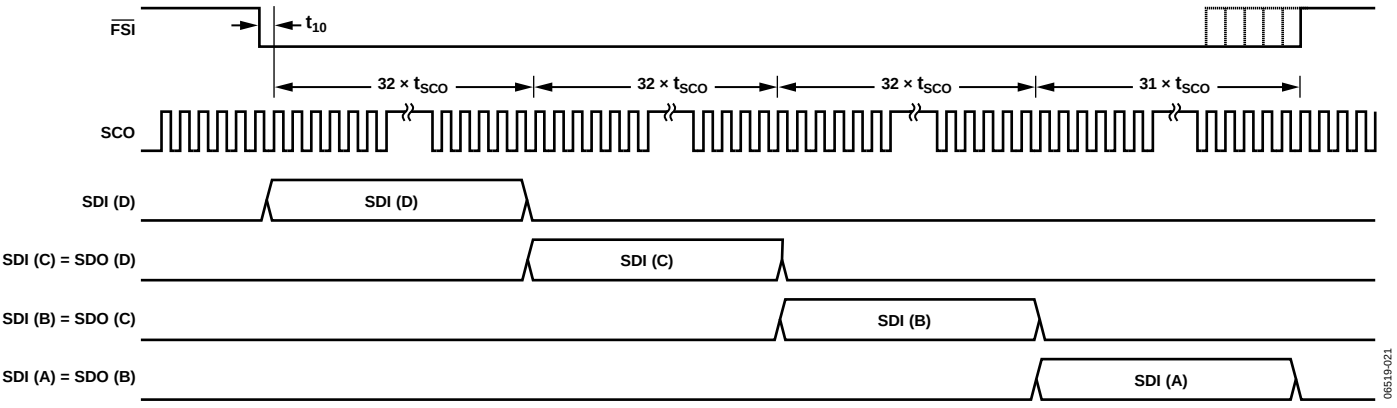


Figure 42. Daisy-Chain Write Timing Diagram; Writing to Four AD7765 Devices

CLOCKING THE AD7765

The AD7765 requires an external low jitter clock source. This signal is applied to the MCLK pin. An internal clock signal (ICLK) is derived from the MCLK input signal. The ICLK controls the internal operation of the AD7765. The maximum ICLK frequency is 20 MHz. To generate the ICLK,

$$ICLK = MCLK/2$$

For output data rates equal to those used in audio systems, a 12.288 MHz ICLK frequency can be used. As shown in Table 6, output data rates of 96 kHz and 48 kHz are achievable with this ICLK frequency.

MCLK JITTER REQUIREMENTS

The MCLK jitter requirements depend on a number of factors and are given by

$$t_{j(rms)} = \frac{\sqrt{OSR}}{2 \times \pi \times f_{IN} \times 10^{\frac{SNR\ (\text{dB})}{20}}}$$

where:
OSR = oversampling ratio = f_{ICLK}/ODR.
f_{IN} = maximum input frequency.
SNR (dB) = target SNR.

Example 1

This example can be taken from Table 6, where:
ODR = 156.25 kHz.
f_{ICLK} = 20 MHz.
f_{IN} (max) = 78.625 kHz.
SNR = 104 dB.

$$t_{j(rms)} = \frac{\sqrt{128}}{2 \times \pi \times 78.625 \times 10^3 \times 10^{5.35}} = 102.29\,\text{ps}$$

This is the maximum allowable clock jitter for a full-scale, 78.625 kHz input tone with the given ICLK and output data rate.

Example 2

This second example can also be taken from Table 6, where:
ODR = 48 kHz.
f_{ICLK} = 12.288 MHz.
f_{IN} (max) = 19.2 kHz.
SNR = 109 dB.

$$t_{j(rms)} = \frac{\sqrt{256}}{2 \times \pi \times 19.2 \times 10^3 \times 10^{5.45}} = 470\ \text{ps}$$

The input amplitude also has an effect on these jitter figures. For example, if the input level is 3 dB below full scale, the allowable jitter is increased by a factor of √2, increasing the first example to 144.65 ps rms. This happens when the maximum slew rate is decreased by a reduction in amplitude.

Figure 43 and Figure 44 illustrate this point, showing the maximum slew rate of a sine wave of the same frequency but with different amplitudes.

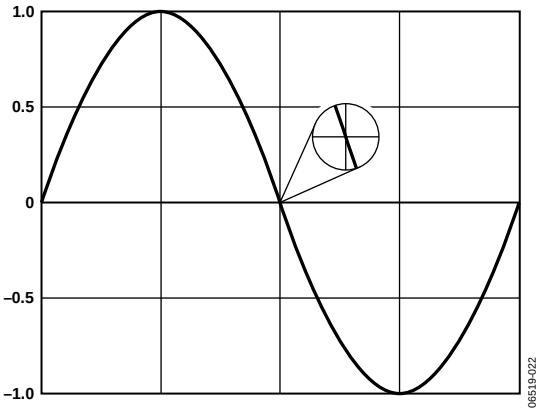


Figure 43. Maximum Slew Rate of a Sine Wave with an Amplitude of 2 V p-p

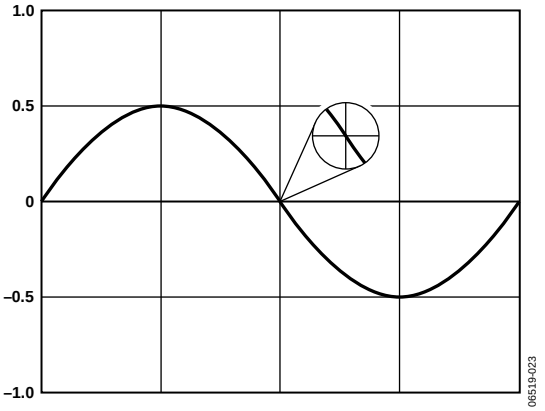


Figure 44. Maximum Slew Rate of the Same Frequency Sine Wave as in Figure 43 with an Amplitude of 1 V p-p

DECOUPLING AND LAYOUT INFORMATION

SUPPLY DECOUPLING

The decoupling of the supplies applied to the AD7765 is important in achieving maximum performance. Each supply pin must be decoupled to the correct ground pin with a 100 nF, 0603 case size capacitor.

Pay particular attention to decoupling Pin 7 ($AV_{DD}2$) directly to the nearest ground pin (Pin 8). The digital ground pin, AGND2 (Pin 20) is routed directly to ground. Also, connect REFGND (Pin 26) directly to ground.

The DV_{DD} (Pin 17) and $AV_{DD}3$ (Pin 28) supplies should be decoupled to the ground plane at a point away from the device.

It is advised to decouple the supplies that are connected to the following supply pins through 0603 size, 100 nF capacitors to a star ground point linked to Pin 23 (AGND1).

- $V_{REF}+$ (Pin 27)
- $AV_{DD}4$ (Pin 25)
- $AV_{DD}1$ (Pin 24)
- $AV_{DD}2$ (Pin 21)

A layout decoupling scheme for these supplies, which connect to the right side of the AD7765, is shown in Figure 45. Note the star-point ground created at Pin 23.

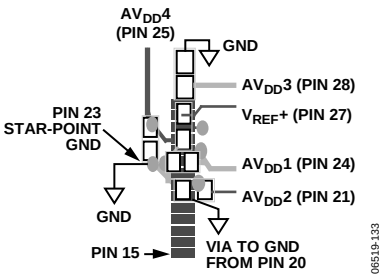


Figure 45. AD7765 Supply Decoupling

REFERENCE VOLTAGE FILTERING

A low noise reference source, such as the ADR444 or ADR434 (4.096 V), is suitable for use with the AD7765. The reference voltage supplied to the AD7765 should be decoupled and filtered, as shown in Figure 46.

The recommended scheme for the reference voltage supply is a 200 Ω series resistor connected to a 100 µF tantalum capacitor, followed by a 10 nF decoupling capacitor very close to the $V_{REF}+$ pin.

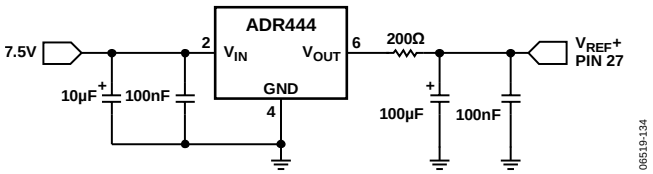


Figure 46. Reference Connection

DIFFERENTIAL AMPLIFIER COMPONENTS

The correct components for use around the on-chip differential amplifier are detailed in Table 7. Matching the components on both sides of the differential amplifier is important to minimize distortion of the signal applied to the amplifier. A tolerance of 0.1% or better is required for these components. Symmetrical routing of the tracks on both sides of the differential amplifier also assists in achieving stated performance. Figure 47 shows a typical layout for the components around the differential amplifier. Note that the traces for both differential paths are made as symmetrical as possible and that the feedback resistors and capacitors are placed on the underside of the PCB to enable the simplest routing.

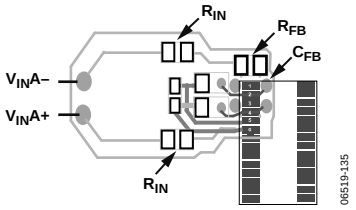


Figure 47. Typical Layout Structure for Surrounding Components

LAYOUT CONSIDERATIONS

While using the correct components is essential to achieving optimum performance, the correct layout is just as important. The AD7765 product page on www.analog.com contains the Gerber files for the AD7765 evaluation board. These files should be downloaded and used as a reference when designing any system using the AD7765.

The use of ground planes should also be carefully considered. To ensure that the return currents through the decoupling capacitors are flowing to the correct ground pin, the ground side of the capacitors should be as close to the ground pin associated with that supply as recommended in the Supply Decoupling section.

USING THE AD7765

The following is the recommended sequence for powering up and using the AD7765:

1. Apply power to the device.
2. Apply the MCLK signal.
3. Take $\overline{\text{RESET}}$ low for a minimum of one MCLK cycle, preferably synchronous to the falling MCLK edge. If multiple parts are to be synchronized, apply a common $\overline{\text{RESET}}$ to all devices.
4. Wait a minimum of two MCLK cycles after $\overline{\text{RESET}}$ has been released.
5. If multiple parts are being synchronized, a $\overline{\text{SYNC}}$ pulse must be applied to the parts, preferably synchronous with the MCLK rising edge. In the case where devices are not being synchronized, no $\overline{\text{SYNC}}$ pulse is required; a logic high signal should simply be applied to the $\overline{\text{SYNC}}$ pin.

   When applying the $\overline{\text{SYNC}}$ pulse,

   - The issue of a $\overline{\text{SYNC}}$ pulse to the device must not coincide with a write to the device.
   - Ensure that the $\overline{\text{SYNC}}$ pulse is taken low for a minimum of four MCLK periods.

Data can then be read from the device using the default gain and overrange threshold values. The conversion data read is not valid, however, until the settling time of the filter has elapsed. Once this has occurred, the FILTER-SETTLE status bit is set, indicating that the data is valid.

Values for gain and overrange thresholds can be written to or read from the respective registers at this stage.

BIAS RESISTOR SELECTION

The AD7765 requires a resistor to be connected between the R_{BIAS} and AGNDx pins. The resistor value should be selected to give a current of 25 μA through the resistor to ground. For a 4.096 V reference voltage, the correct resistor value is 160 kΩ.

AD7765 REGISTERS

The AD7765 has a number of user-programmable registers. The control register is used to set the functionality of the on-chip buffer and differential amplifier and provides an option to power down the AD7765. There are also digital gain and overrange threshold registers. Writing to these registers involves writing the register address followed by a 16-bit data word. The register addresses, details of individual bits, and default values are provided in this section.

CONTROL REGISTER

Table 13. Control Register (Address 0x0001, Default Value 0x0000)

MSB **LSB**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	RD OVR	RD GAIN	0	RD STAT	0	SYNC	0	BYPASS REF	0	0	0	PWR DOWN	LPWR	REF BUF OFF	AMP OFF

Table 14. Bit Descriptions of the Control Register

Bit	Mnemonic	Comment
14	RD OVR[1, 2]	Read overrange. If this bit is set, the next read operation outputs the contents of the overrange threshold register instead of a conversion result.
13	RD GAIN	Read gain. If this bit is set, the next read operation outputs the contents of the digital gain register.
11	RD STAT	Read status. If this bit is set, the next read operation outputs the contents of the status register.
9	SYNC	Synchronize. Setting this bit initiates an internal synchronization routine. Setting this bit simultaneously on multiple devices synchronizes all filters.
7	BYPASS REF	Bypass reference. Setting this bit bypasses the reference buffer if the buffer is off.
3	PWR DOWN	Power-down. A logic high powers the device down without resetting. Writing a 0 to this bit powers the device back up.
2	LPWR	Low power mode. Set to Logic 1 when AD7765 is in low power mode.
1	REF BUF OFF	Reference buffer off. Asserting this bit powers down the reference buffer.
0	AMP OFF	Amplifier off. Asserting this bit switches the differential amplifier off.

[1] Bit 14 to Bit 11 and Bit 9 are self-clearing bits.
[2] Only one of the bits can be set in any write operation because it determines the contents of the next read operation.

STATUS REGISTER

Table 15. Status Register (Read Only)

MSB **LSB**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PARTNO	1	0	0	0	FILTER-SETTLE	0	OVR	0	1	0	REF BUF ON	AMP ON	LPWR	DEC 1	DEC 0

Table 16. Bit Descriptions of the Status Register

Bit	Mnemonic	Comment
15	PARTNO	Part number. This bit is set to 1 for the AD7765.
10	FILTER-SETTLE	Filter settling bit. This bit corresponds to the FILTER-SETTLE bit in the status word output in the second 16-bit read operation. It indicates when data is valid.
9	0	Zero. This bit is set to Logic 0.
8	OVR	Overrange. If the current analog input exceeds the current overrange threshold, this bit is set.
4	REF BUF ON	Reference buffer on. This bit is set when the reference buffer is in use.
3	AMP ON	Amplifier on. This bit is set when the input amplifier is in use.
2	LPWR	Low power mode. This bit is set when operating in low power mode.
1 to 0	DEC[1:0]	Decimation rate. These bits correspond to the decimation rate in use.

GAIN REGISTER—ADDRESS 0x0004

Non-Bit-Mapped, Default Value 0xA000

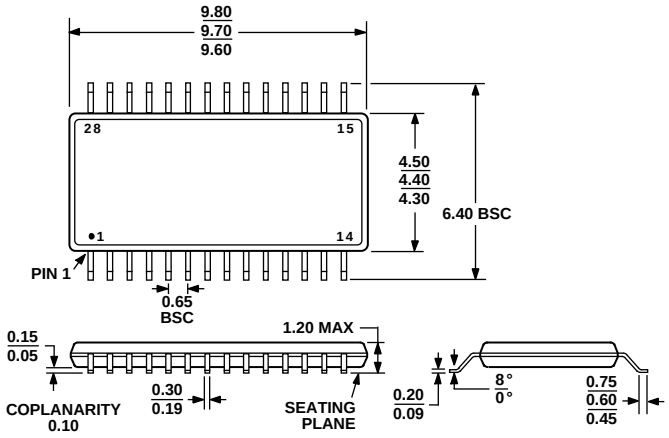
The gain register is scaled such that 0x8000 corresponds to a gain of 1.0. The default value of this register is 1.25 (0xA000). This results in a full-scale digital output when the input is at 80% of V_{REF}+, tying in with the maximum analog input range of ±80% of V_{REF}+ p-p.

OVERRANGE REGISTER—ADDRESS 0x0005

Non-Bit-Mapped, Default Value 0xCCCC

The overrange register value is compared with the output of the first decimation filter to obtain an overload indication with minimum propagation delay. This is prior to any gain scaling or offset adjustment. The default value is 0xCCCC, which corresponds to 80% of V_{REF}+ (the maximum permitted analog input voltage). Assuming V_{REF}+ = 4.096 V, the bit is then set when the input voltage exceeds approximately 6.55 V p-p differential. The overrange bit is set immediately if the analog input voltage exceeds 100% of V_{REF}+ for more than four consecutive samples at the modulator rate.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AE

Figure 48. 28-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-28)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD7765BRUZ[1]	−40°C to +85°C	28-Lead Thin Shrink Small Outline Package [TSSOP]	RU-28
AD7765BRUZ-REEL7[1]	−40°C to +85°C	28-Lead Thin Shrink Small Outline Package [TSSOP]	RU-28
EVAL-AD7765EDZ[1]		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

NOTES

D06519-0-8/09(A)