

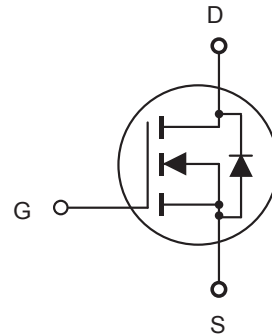


# CEP50N06/CEB50N06

## N-Channel Enhancement Mode Field Effect Transistor

### FEATURES

- 60V, 50A,  $R_{DS(ON)} = 17m\Omega$  (typ) @  $V_{GS} = 10V$ .
- Super high dense cell design for extremely low  $R_{DS(ON)}$ .
- High power and current handling capability.
- Lead free product is acquired.
- TO-220 & TO-263 package.



### ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ C$ unless otherwise noted

Parameter	Symbol	Limit	Units
Drain-Source Voltage	$V_{DS}$	60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	50	A
Drain Current-Pulsed <sup>a</sup>	$I_{DM}$	150	A
Maximum Power Dissipation @ $T_C = 25^\circ C$ - Derate above $25^\circ C$	$P_D$	131	W
		0.88	W/ $^\circ C$
Single Pulsed Avalanche Energy <sup>d</sup>	$E_{AS}$	225	mJ
Single Pulsed Avalanche Current <sup>d</sup>	$I_{AS}$	50	A
Operating and Store Temperature Range	$T_J, T_{stg}$	-55 to 175	$^\circ C$

### Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.14	W/ $^\circ C$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	W/ $^\circ C$

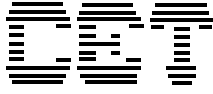


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## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

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Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	60			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 54V, V_{GS} = 0V$			1	$\mu A$
Gate Body Leakage Current, Forward	$I_{GSSF}$	$V_{GS} = 20V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	$I_{GSSR}$	$V_{GS} = -20V, V_{DS} = 0V$			-100	nA
<b>On Characteristics<sup>b</sup></b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	2		4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 50A$		17	22	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS} = 10V, I_D = 25A$		19		S
<b>Dynamic Characteristics<sup>c</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 25V, V_{GS} = 0V,$ $f = 1.0\text{ MHz}$		1420		pF
Output Capacitance	$C_{oss}$			400		pF
Reverse Transfer Capacitance	$C_{rss}$			50		pF
<b>Switching Characteristics<sup>c</sup></b>						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 30V, I_D = 48A,$ $V_{GS} = 10V, R_{GEN} = 7.5\Omega$		17.2	34.4	ns
Turn-On Rise Time	$t_r$			5	10	ns
Turn-Off Delay Time	$t_{d(off)}$			32.5	65	ns
Turn-Off Fall Time	$t_f$			10	20	ns
Total Gate Charge	$Q_g$	$V_{DS} = 48V, I_D = 48A,$ $V_{GS} = 10V$		28.2	37.5	nC
Gate-Source Charge	$Q_{gs}$			8.5		nC
Gate-Drain Charge	$Q_{gd}$			7		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
Drain-Source Diode Forward Current	$I_S$				50	A
Drain-Source Diode Forward Voltage <sup>b</sup>	$V_{SD}$	$V_{GS} = 0V, I_S = 50A$			1.5	V
<b>Notes :</b> □ a.Repetitive Rating : Pulse width limited by maximum junction temperature. b.Pulse Test : Pulse Width $\leq 300\mu s$ , Duty Cycle $\leq 2\%$ . □ c.Guaranteed by design, not subject to production testing. □ d.L = $90\mu H$ , $I_{AS} = 50A$ , $V_{DD} = 24V$ , $R_G = 25\Omega$ , Starting $T_J = 25^\circ C$						



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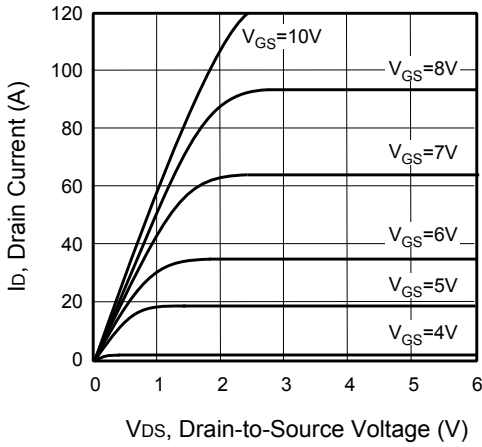


Figure 1. Output Characteristics

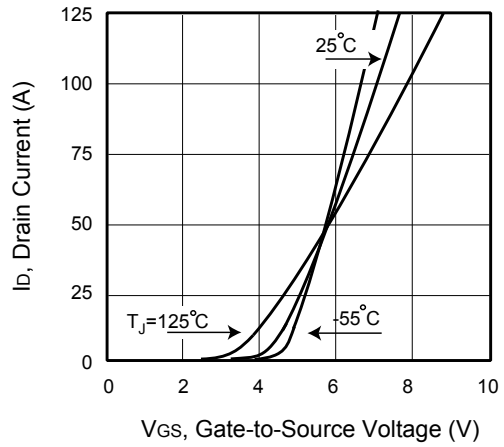


Figure 2. Transfer Characteristics

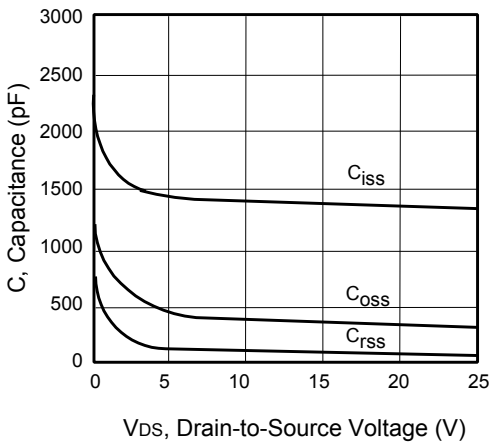


Figure 3. Capacitance

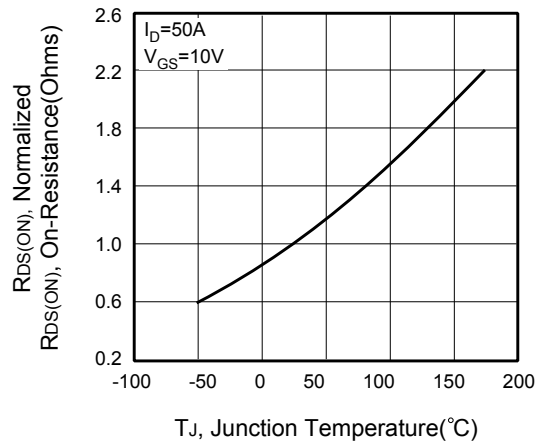


Figure 4. On-Resistance Variation with Temperature

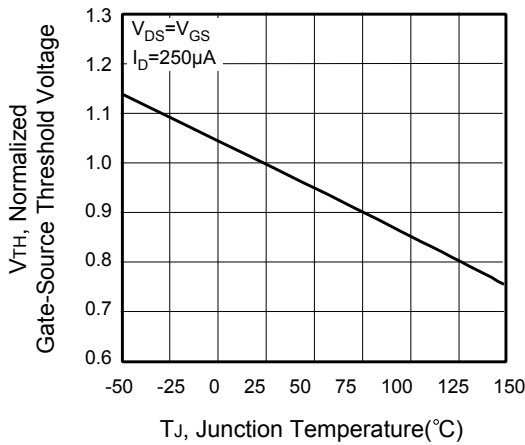


Figure 5. Gate Threshold Variation with Temperature

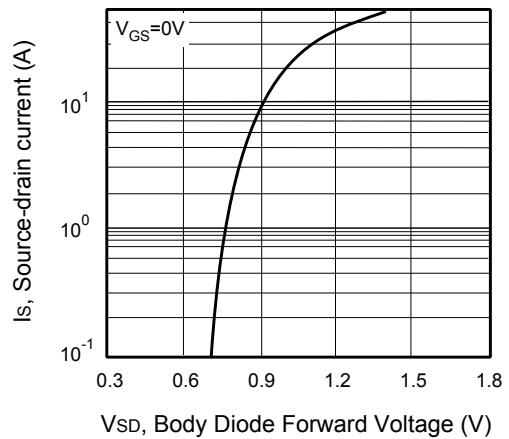


Figure 6. Body Diode Forward Voltage Variation with Source Current



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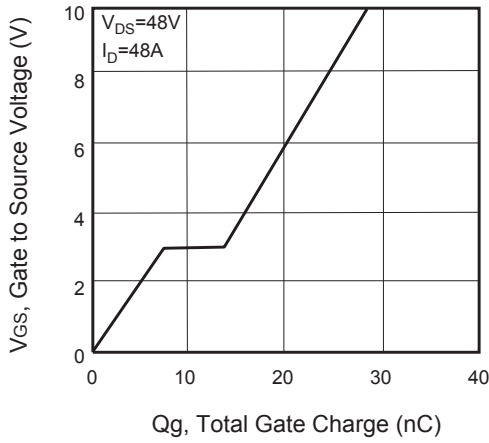


Figure 7. Gate Charge

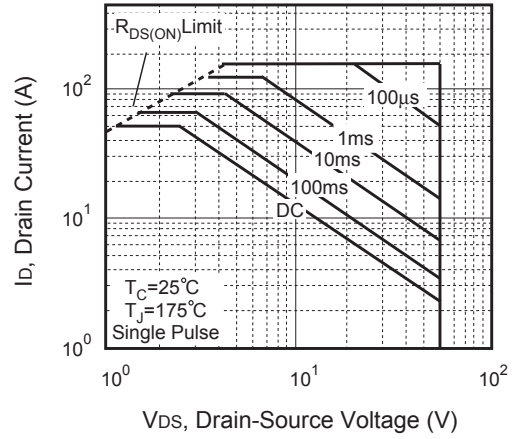


Figure 8. Maximum Safe Operating Area

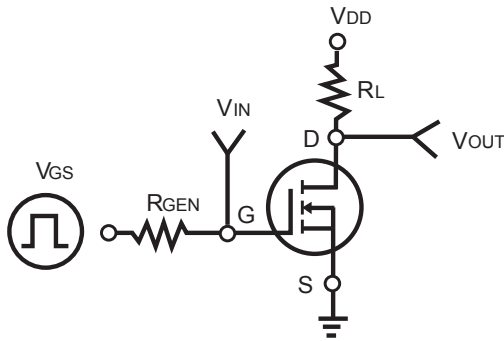


Figure 9. Switching Test Circuit

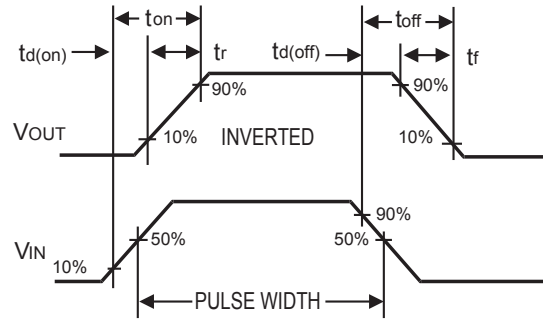


Figure 10. Switching Waveforms

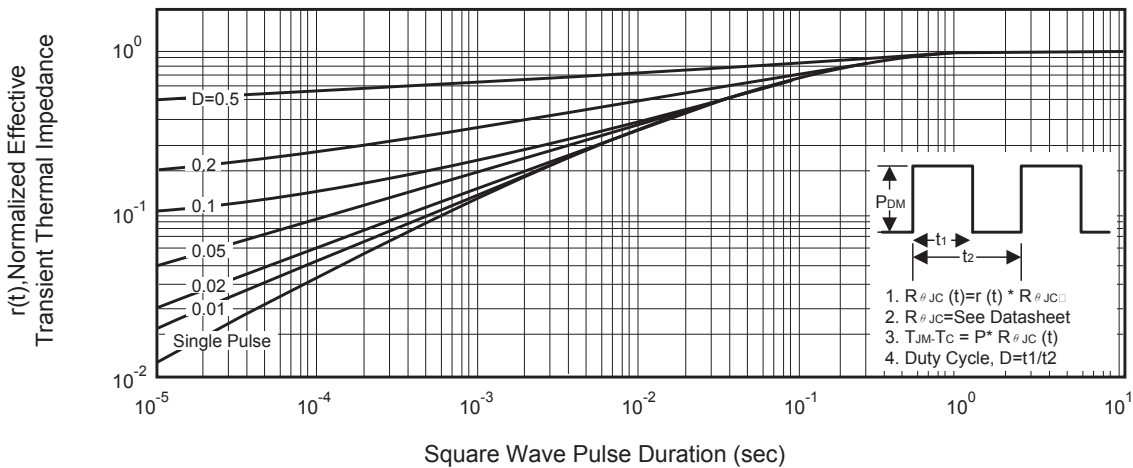


Figure 11. Normalized Thermal Transient Impedance Curve