

CEP7030L/CEB7030L

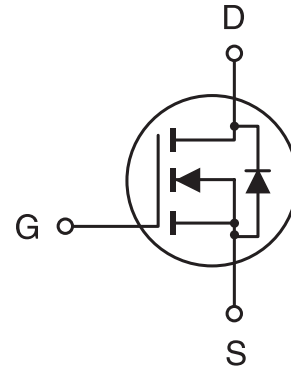
JUN 1998

N-Channel Logic Level Enhancement Mode Field Effect Transistor

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FEATURES

- 30V , 65A , $R_{DS(ON)} = 8m\Omega$ @ $V_{GS} = 10V$.
 $R_{DS(ON)} = 12m\Omega$ @ $V_{GS} = 4.5V$.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability.
- TO-220 & TO-263 package.



ABSOLUTE MAXIMUM RATINGS ($T_c = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	30	V
Gate-Source Voltage	V _{GS}	±16	V
Drain Current-Continuous @ $T_J = 125^\circ\text{C}$ -Pulsed	I _D	65	A
	I _{DM}	180	A
Drain-Source Diode Forward Current	I _S	65	A
Maximum Power Dissipation @ $T_c = 25^\circ\text{C}$ Derate above 25°C	P _D	50	W
		0.4	W/°C
Operating and Storage Temperature Range	T _J , T _{STG}	-65 to 175	°C

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Case ^a	R _{θJC}	2.5	°C/W
Thermal Resistance, Junction-to-Ambient ^a	R _{θJA}	62.5	°C/W

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ELECTRICAL CHARACTERISTICS (T_c=25°C unless otherwise noted)

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Parameter	Symbol	Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	30	35		V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =24V, V _{GS} =0V			10	μA
Gate-Body Leakage	I _{GSS}	V _{GS} =±16V, V _{DS} =0V			±100	nA
ON CHARACTERISTICS^a						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1	1.5	3	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =35A		7.4	8	mΩ
		V _{GS} =4.5V, I _D =28A		10.6	12	mΩ
On-State Drain Current	I _{D(ON)}	V _{GS} =10V, V _{DS} =10V	60			A
Forward Transconductance	g _{FS}	V _{DS} =10V, I _D =35A		50		S
DYNAMIC CHARACTERISTICS^b						
Input Capacitance	C _{ISS}	V _{DS} =15V, V _{GS} =0V f=1.0MHz		2000	2200	pF
Output Capacitance	C _{OSS}			1011	1250	pF
Reverse Transfer Capacitance	C _{RSS}			131	400	pF
SWITCHING CHARACTERISTICS^b						
Turn-On Delay Time	t _{D(ON)}	V _{DD} =15V, I _D =60A, V _{GEN} =10V R _G =1.8 Ω R _L =0.25 Ω		15		ns
Rise Time	t _r			210		ns
Turn-Off Delay Time	t _{D(OFF)}			30		ns
Fall Time	t _f			55		ns
Total Gate Charge	Q _g	V _{DS} =24V, I _D =60A, V _{GS} =10V		60	110	nC
Gate-Source Charge	Q _{gs}			9	31	nC
Gate-Drain Charge	Q _{gd}			20	57	nC

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ELECTRICAL CHARACTERISTICS ($T_c=25^\circ\text{C}$ unless otherwise noted)

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Parameter	Symbol	Condition	Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS ^a						
Diode Forward Voltage	V_{SD}	$V_{GS} = 0V, I_s = 35A$		0.93	1.3	V

Notes

a. Pulse Test: Pulse Width $\leq 300 \mu s$, Duty Cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

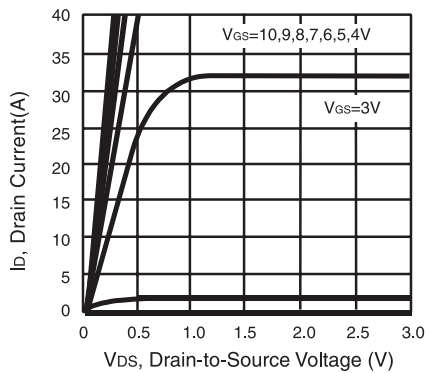


Figure 1. Output Characteristics

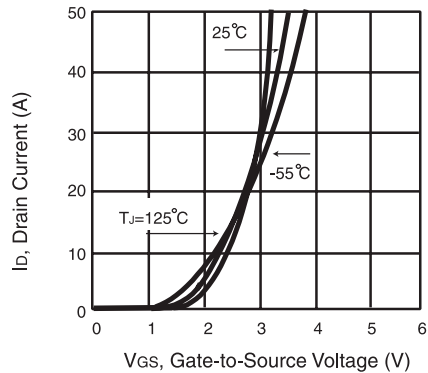


Figure 2. Transfer Characteristics

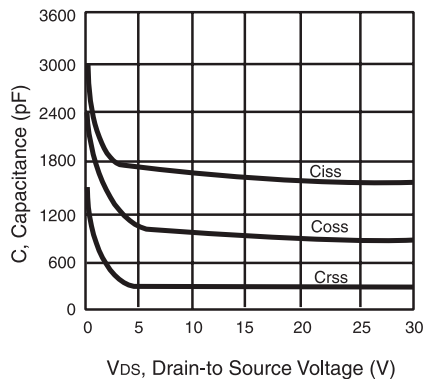


Figure 3. Capacitance

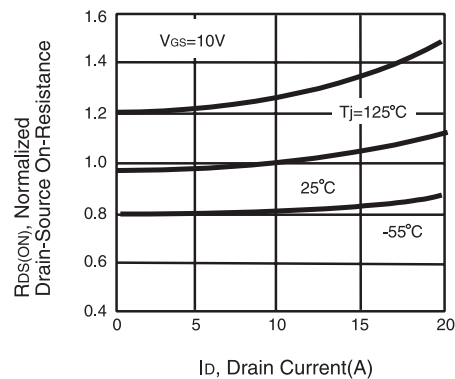


Figure 4. On-Resistance Variation with Drain Current and Temperature

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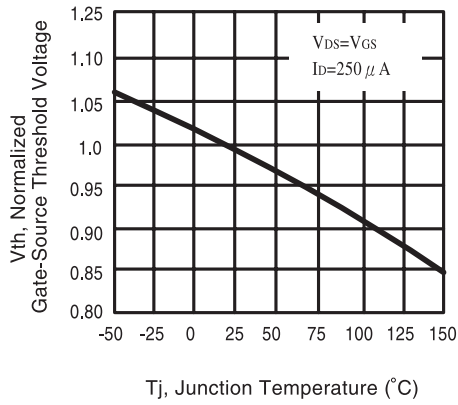


Figure 5. Gate Threshold Variation with Temperature

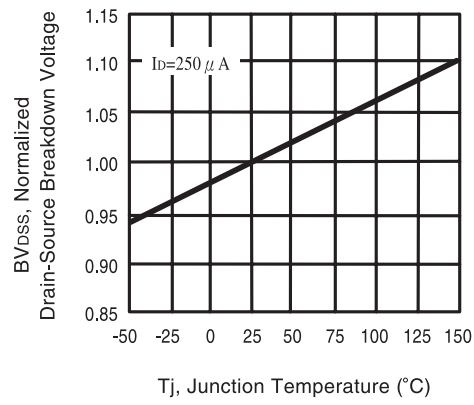


Figure 6. Breakdown Voltage Variation with Temperature

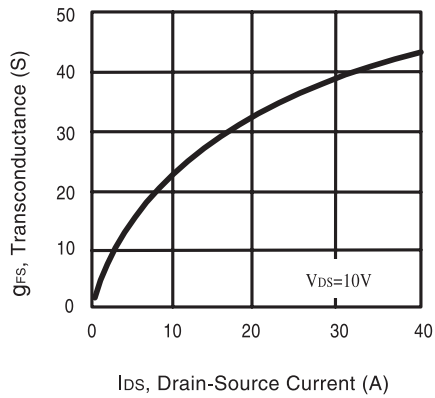


Figure 7. Transconductance Variation with Drain Current

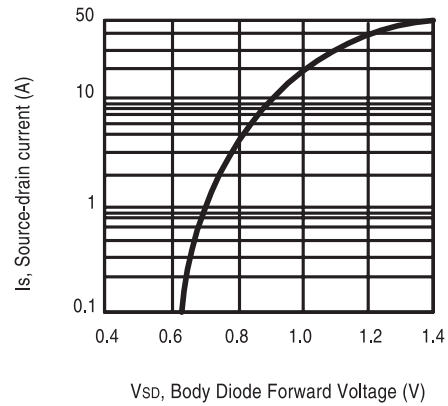


Figure 8. Body Diode Forward Voltage Variation with Source Current

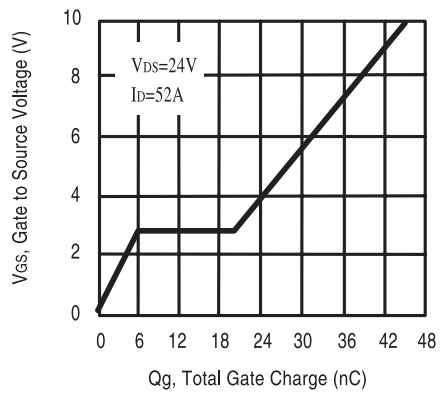


Figure 9. Gate Charge

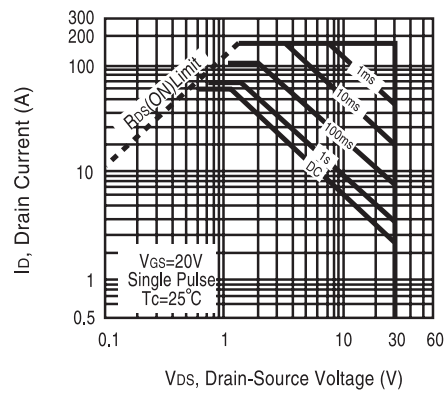


Figure 10. Maximum Safe Operating Area

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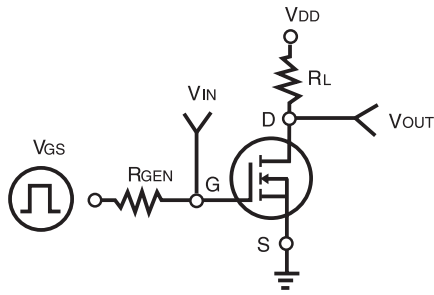


Figure 11. Switching Test Circuit

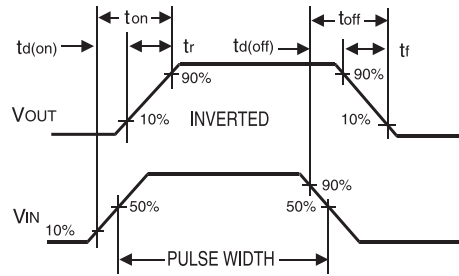


Figure 12. Switching Waveforms

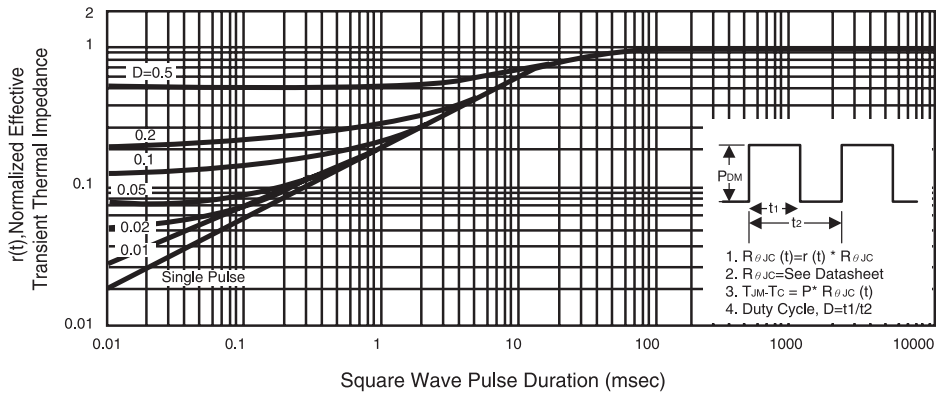


Figure 13. Normalized Thermal Transient Impedance Curve