

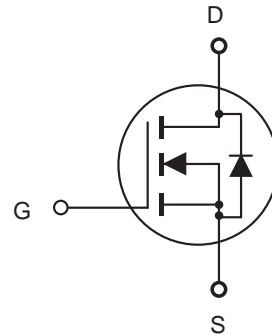


CED73A3/CEU73A3

N-Channel Enhancement Mode Field Effect Transistor

FEATURES

- 30V, 65A, $R_{DS(ON)} = 7.8m\Omega(\text{typ}) @ V_{GS} = 10V$.
 $R_{DS(ON)} = 10m\Omega(\text{typ}) @ V_{GS} = 4.5V$.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability.
- Lead free product is acquired.
- TO-251 & TO-252 package.



ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Limit	Units
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	65	A
Drain Current-Pulsed ^a	I_{DM}	350	A
Maximum Power Dissipation @ $T_C = 25^\circ\text{C}$ - Derate above 25°C	P_D	60	W
		0.48	W/ $^\circ\text{C}$
Single Pulsed Avalanche Energy ^d	E_{AS}	160	mJ
Single Pulsed Avalanche Current ^d	I_{AS}	25	A
Operating and Store Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.1	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	50	$^\circ\text{C/W}$



CED73A3/CEU73A3

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	30			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 25V, V_{GS} = 0V$			1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	$V_{GS} = 20V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	$V_{GS} = -20V, V_{DS} = 0V$			-100	nA
On Characteristics ^b						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	1		3	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 30A$		7.8	9	$m\Omega$
		$V_{GS} = 4.5V, I_D = 30A$		10	13	$m\Omega$
Forward Transconductance	g_{FS}	$V_{DS} = 10V, I_D = 15A$		20		S
Dynamic Characteristics ^c						
Input Capacitance	C_{iss}	$V_{DS} = 15V, V_{GS} = 0V, f = 1.0\text{ MHz}$		2923		pF
Output Capacitance	C_{oss}			506		pF
Reverse Transfer Capacitance	C_{rss}			202		pF
Switching Characteristics ^c						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15V, I_D = 1A, V_{GS} = 10V, R_{GEN} = 6\Omega$		19	23	ns
Turn-On Rise Time	t_r			6.8	12	ns
Turn-Off Delay Time	$t_{d(off)}$			71	128	ns
Turn-On Fall Time	t_f			12.8	17.5	ns
Total Gate Charge	Q_g	$V_{DS} = 15V, I_D = 20A, V_{GS} = 4.5V$		24	30	nC
Gate-Source Charge	Q_{gs}			9.1		nC
Gate-Drain Charge	Q_{gd}			7.5		nC
Drain-Source Diode Characteristics and Maximum Ratings						
Drain-Source Diode Forward Current	I_S				20	A
Drain-Source Diode Forward Voltage ^b	V_{SD}	$V_{GS} = 0V, I_S = 20A$			1.5	V
Notes : a.Repetitive Rating : Pulse width limited by maximum junction temperature. b.Pulse Test : Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$. c.Guaranteed by design, not subject to production testing. d.L = 0.5mH, $I_{AS} = 25A, V_{DD} = 24V, R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$						

6



CED73A3/CEU73A3

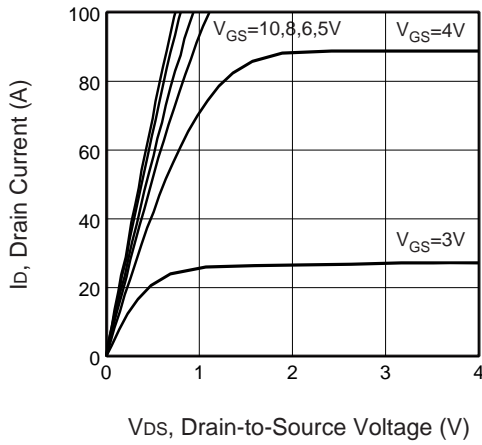


Figure 1. Output Characteristics

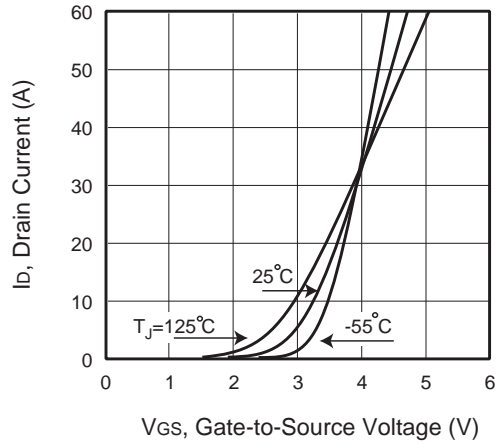


Figure 2. Transfer Characteristics

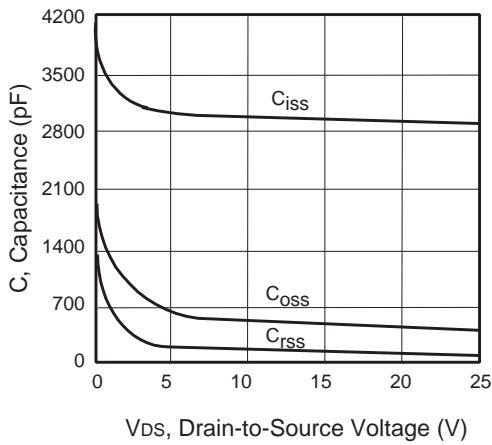


Figure 3. Capacitance

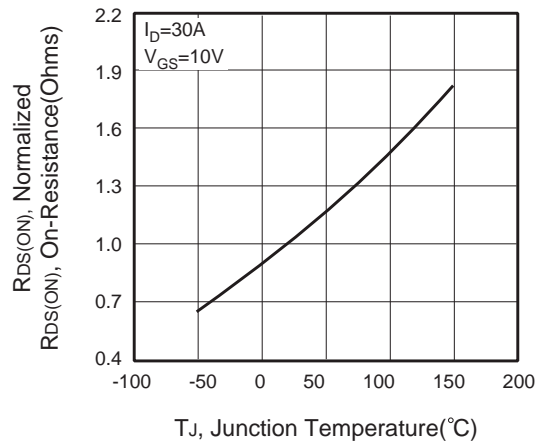


Figure 4. On-Resistance Variation with Temperature

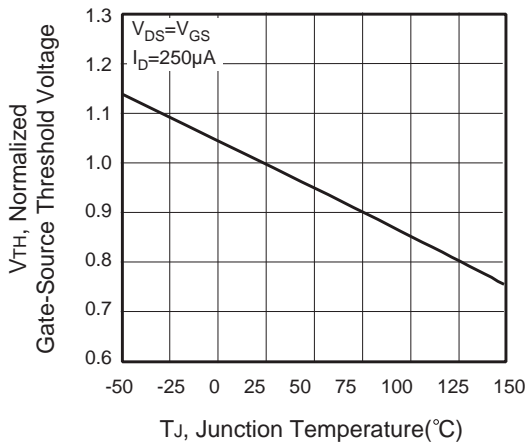


Figure 5. Gate Threshold Variation with Temperature

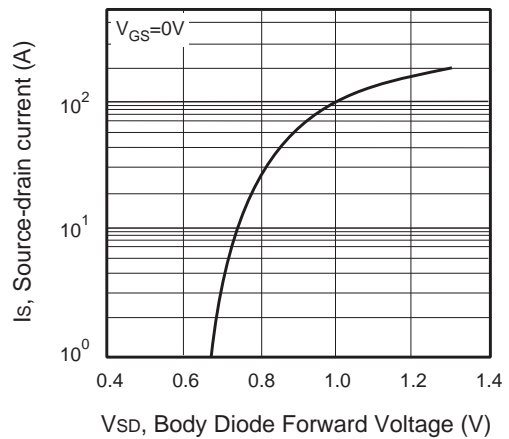


Figure 6. Body Diode Forward Voltage Variation with Source Current



CED73A3/CEU73A3

6

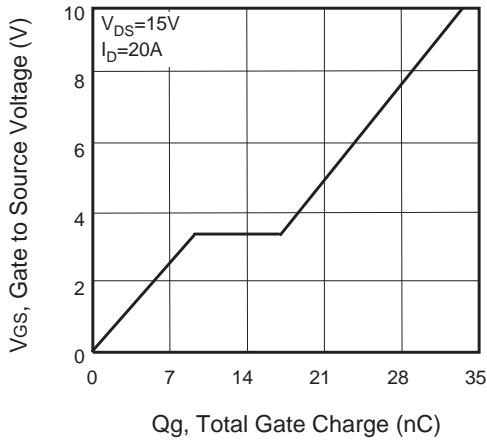


Figure 7. Gate Charge

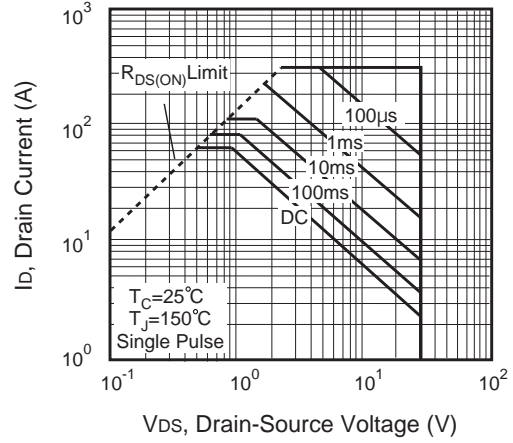


Figure 8. Maximum Safe Operating Area

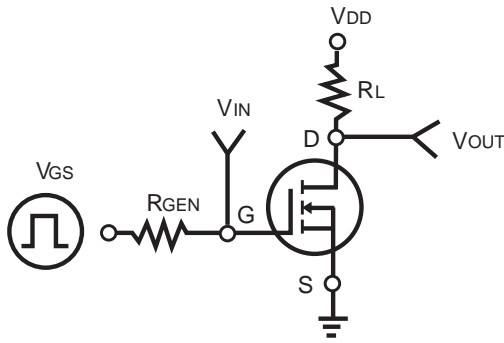


Figure 9. Switching Test Circuit

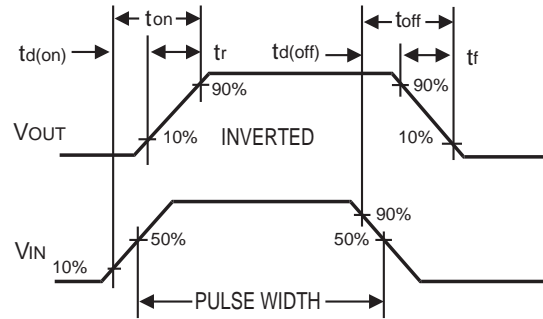


Figure 10. Switching Waveforms

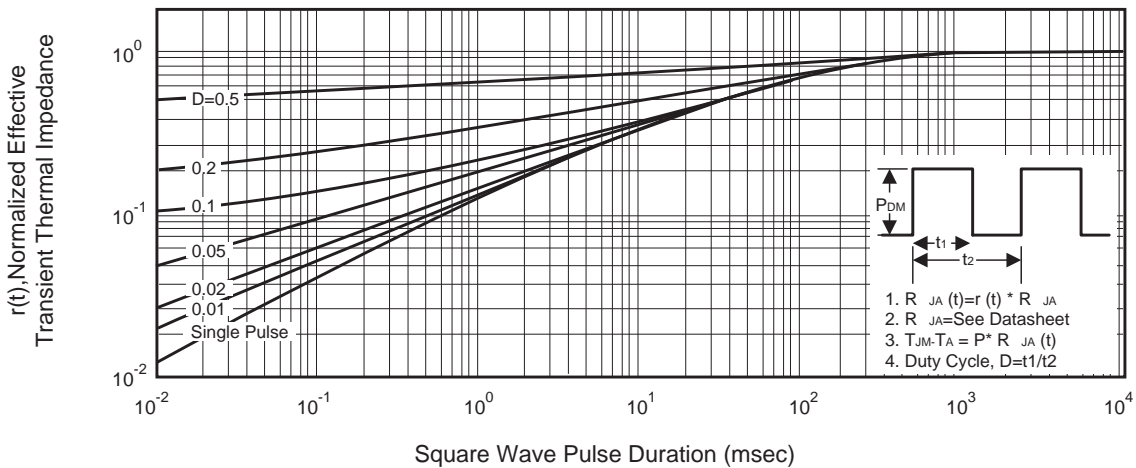


Figure 11. Normalized Thermal Transient Impedance Curve