

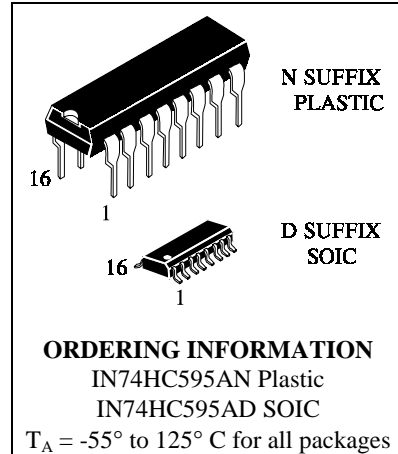
**IN74HC595A**

**8-Bit Serial-Input/Serial or Parallel-Output Shift Register with Latched 3-State Outputs  
High-Performance Silicon-Gate CMOS**

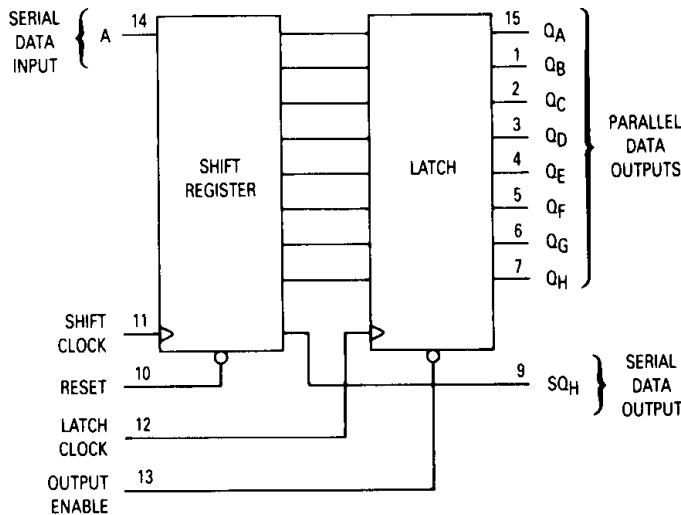
The IN74HC595A is identical in pinout to the LS/ALS595. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALSTTL outputs.

The IN74HC595A consists of an 8-bit shift register and an 8-bit D-type latch with three-state parallel outputs. The shift register accepts serial data and provides a serial output. The shift register also provides parallel data to the 8-bit latch. The shift register and latch have independent clock inputs. This device also has an asynchronous reset for the shift register.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices

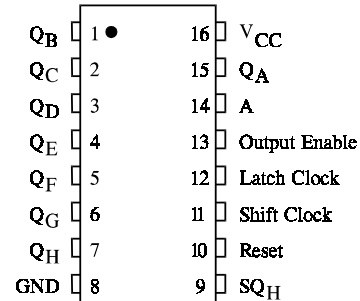


**LOGIC DIAGRAM**



PIN 16 =  $V_{CC}$   
 PIN 8 = GND

**PIN ASSIGNMENT**



## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
$V_{IN}$	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
$V_{OUT}$	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
$I_{IN}$	DC Input Current, per Pin	$\pm 20$	mA
$I_{OUT}$	DC Output Current, per Pin	$\pm 35$	mA
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	$\pm 75$	mA
$P_D$	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
$T_{stg}$	Storage Temperature	-65 to +150	°C
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C

SOIC Package: : - 7 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
$V_{IN}, V_{OUT}$	DC Input Voltage, Output Voltage (Referenced to GND)	0	$V_{CC}$	V
$T_A$	Operating Temperature, All Package Types	-55	+125	°C
$t_r, t_f$	Input Rise and Fall Time (Figure 1)			
	$V_{CC} = 2.0$ V	0	1000	ns
	$V_{CC} = 4.5$ V	0	500	
	$V_{CC} = 6.0$ V	0	400	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{IN}$  and  $V_{OUT}$  should be constrained to the range  $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

**DC ELECTRICAL CHARACTERISTICS**(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>OUT</sub> =0.1 V or V <sub>CC</sub> -0.1 V   I <sub>OUT</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low - Level Input Voltage	V <sub>OUT</sub> =0.1 V or V <sub>CC</sub> -0.1 V   I <sub>OUT</sub>   ≤ 20 μA	2.0	0.5	0.5	0.5	V
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V <sub>OH</sub>	Minimum High-Level Output Voltage, Q <sub>A</sub> -Q <sub>H</sub>	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>   I <sub>OUT</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>   I <sub>OUT</sub>   ≤ 6.0 mA   I <sub>OUT</sub>   ≤ 7.8 mA	4.5	3.98	3.84	3.7	
			6.0	5.48	5.34	5.2	
V <sub>OL</sub>	Maximum Low-Level Output Voltage, Q <sub>A</sub> -Q <sub>H</sub>	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>   I <sub>OUT</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>   I <sub>OUT</sub>   ≤ 6.0 mA   I <sub>OUT</sub>   ≤ 7.8 mA	4.5	0.26	0.33	0.4	
			6.0	0.26	0.33	0.4	
V <sub>OH</sub>	Minimum High-Level Output Voltage, S <sub>Q<sub>H</sub></sub>	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>   I <sub>OUT</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>   I <sub>OUT</sub>   ≤ 4.0 mA   I <sub>OUT</sub>   ≤ 5.2 mA	4.5	3.98	3.84	3.7	
			6.0	5.48	5.34	5.2	
V <sub>OL</sub>	Maximum Low-Level Output Voltage, S <sub>Q<sub>H</sub></sub>	V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>   I <sub>OUT</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>   I <sub>OUT</sub>   ≤ 4.0 mA   I <sub>OUT</sub>   ≤ 5.2 mA	4.5	0.26	0.33	0.4	
			6.0	0.26	0.33	0.4	
I <sub>IN</sub>	Maximum Input Leakage Current	V <sub>IN</sub> =V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
I <sub>OZ</sub>	Maximum Three-State Leakage Current, Q <sub>A</sub> -Q <sub>H</sub>	Output in High-Impedance State V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>IN</sub> =V <sub>CC</sub> or GND	6.0	±0.5	±5.0	±10	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA	6.0	4.0	40	160	μA

## AC ELECTRICAL CHARACTERISTICS ( $C_L=50\text{pF}$ , Input $t_r=t_f=6.0\text{ ns}$ )

Symbol	Parameter	$V_{CC}$ V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85 °C	≤125 °C	
$f_{max}$	Minimum Clock Frequency (50% Duty Cycle) (Figures 1 and 7)	2.0	6.0	4.8	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Shift Clock to $SQ_H$ (Figures 1 and 7)	2.0	140	175	210	ns
		4.5	28	35	42	
		6.0	24	30	36	
$t_{PHL}$	Maximum Propagation Delay, Reset to $SQ_H$ (Figures 2 and 7)	2.0	145	180	220	ns
		4.5	29	36	44	
		6.0	25	31	38	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Latch Clock to $Q_A-Q_H$ (Figures 3 and 7)	2.0	140	175	210	ns
		4.5	28	35	42	
		6.0	24	30	36	
$t_{PLZ}$ , $t_{PHZ}$	Maximum Propagation Delay, Output Enable to $Q_A-Q_H$ (Figures 4 and 8)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
$t_{PZL}$ , $t_{PZH}$	Maximum Propagation Delay, Output Enable to $Q_A-Q_H$ (Figures 4 and 8)	2.0	135	170	205	ns
		4.5	27	34	41	
		6.0	23	29	35	
$t_{TLH}$ , $t_{THL}$	Maximum Output Transition Time, $Q_A-Q_H$ (Figures 3 and 7)	2.0	60	75	90	ns
		4.5	12	15	18	
		6.0	10	13	15	
$t_{TLH}$ , $t_{THL}$	Maximum Output Transition Time, $SQ_H$ (Figures 1 and 7)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
$C_{IN}$	Maximum Input Capacitance	-	10	10	10	pF
$C_{OUT}$	Maximum Three-State Output Capacitance (Output in High-Impedance State), $Q_A-Q_H$	-	15	15	15	pF
$C_{PD}$	Power Dissipation Capacitance (Per Package)	Typical @25°C, $V_{CC}=5.0\text{ V}$				pF
	Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$	300				

**TIMING REQUIREMENTS**( $C_L=50\text{pF}$ ,Input  $t_r=t_f=6.0\text{ ns}$ )

Symbol	Parameter	$V_{CC}$ V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125°C	
$t_{su}$	Minimum Setup Time,Serial Data Input A to Shift Clock (Figure 5)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9	11	13	
$t_{su}$	Minimum Setup Time, Shift Clock to Latch Clock (Figure 6)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
$t_h$	Minimum Hold Time, Shift Clock to Serial Data Input A (Figure 5)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
$t_{rec}$	Minimum Recovery Time, Reset Inactive to Shift Clock (Figure 2)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9	11	13	
$t_w$	Minimum Pulse Width, Reset (Figure 2)	2.0	60	75	90	ns
		4.5	12	15	18	
		6.0	10	13	15	
$t_w$	Minimum Pulse Width, Shift Clock (Figure 1)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9	11	13	
$t_w$	Minimum Pulse Width, Latch Clock (Figure 6)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9	11	13	
$t_r, t_f$	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

**FUNCTION TABLE**

Operation	Inputs					Resulting Function			
	Reset	Serial Input A	Shift Clock	Latch Clock	Output Enable	Shift Register Contents	Latch Register Contents	Serial Output SQ <sub>H</sub>	Parallel Outputs Q <sub>A</sub> -Q <sub>H</sub>
Reset shift register	L	X	X		L	L	U	L	U
Shift data into shift register	H	D			L	D → SR <sub>A</sub> SR <sub>N</sub> → SR <sub>N+1</sub>	U	SR <sub>G</sub> → SR <sub>H</sub>	U
Shift register remains unchanged	H	X			L	U	U	U	U
Transfer shift register contents to latch register	H	X			L	U	SR <sub>N</sub> → LR <sub>N</sub>	U	SR <sub>N</sub>
Latch register remains unchanged	X	X	X		L	*	U	*	U
Enable parallel outputs	X	X	X	X	L	*	**	*	Enabled
Force outputs into high-impedance state	X	X	X	X	H	*	**	*	Z

SR = shift register contents

X = don't care

LR = latch register contents

Z = high impedance

D = data (L,H) logic level

\* = depends on Reset and Shift Clock inputs

U = remains unchanged

\*\* = depends on Latch Clock input

**PIN DESCRIPTIONS**

**INPUTS:**

**A** - Serial Data Input. The data on this pin is shifted into the 8-bit serial shift register.

**CONTROL INPUTS:**

**Shift Clock** - Shift Register Clock Input. A low-to-high transition on this input causes the data at the Serial Input pin to be shifted into the 8-bit shift register.

**Reset** - Active-low, Asynchronous, Shift Register Reset Input. A low on this pin resets the shift register portion of this device only. The 8-bit latch is not affected.

**Latch Clock** - Storage Latch Clock Input. A low-to-high transition on this input latches the shift register data.

**Output Enable** - Active-Low Output Enable. A low on this input allows the data from the latches to be represented at the outputs. A high on this input forces the outputs (Q<sub>A</sub>-Q<sub>H</sub>) into the high-impedance state. The serial output is not affected by this control unit.

**OUTPUTS:**

**Q<sub>A</sub>-Q<sub>H</sub>** - Noninverted, 3-state, latch outputs.

**SQ<sub>H</sub>** - Noninverted, Serial Data Output. This is the output of the eighth stage of the 8-bit shift register. This output does not have three-state capability.

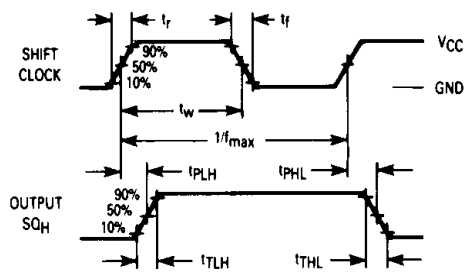


Figure 1. Switching Waveforms

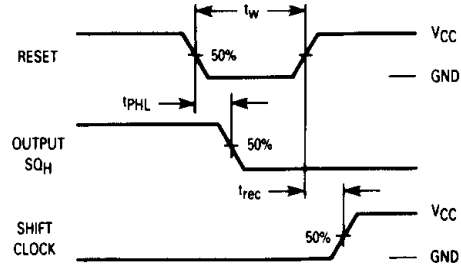


Figure 2. Switching Waveforms

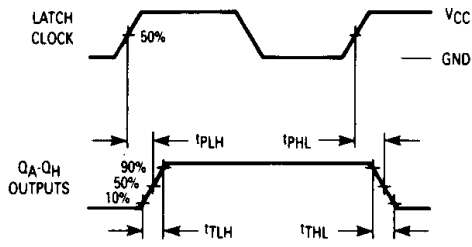


Figure 3. Switching Waveforms

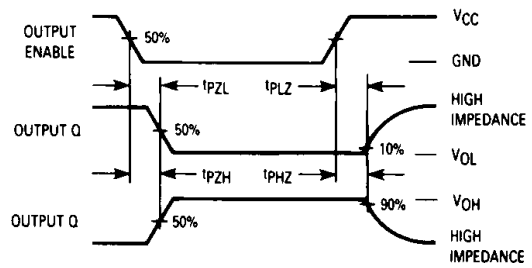


Figure 4. Switching Waveforms

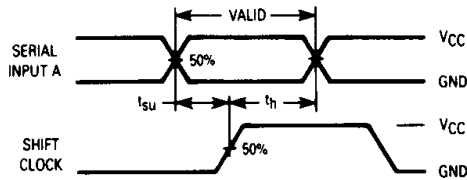


Figure 5. Switching Waveforms

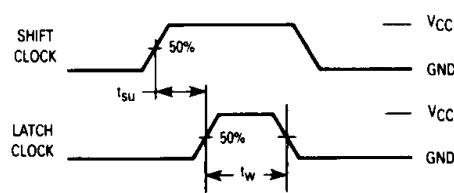
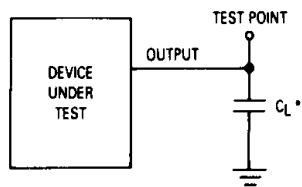
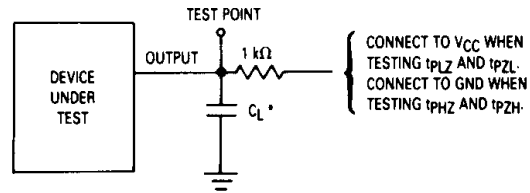


Figure 6. Switching Waveforms



\*Includes all probe and jig capacitance.

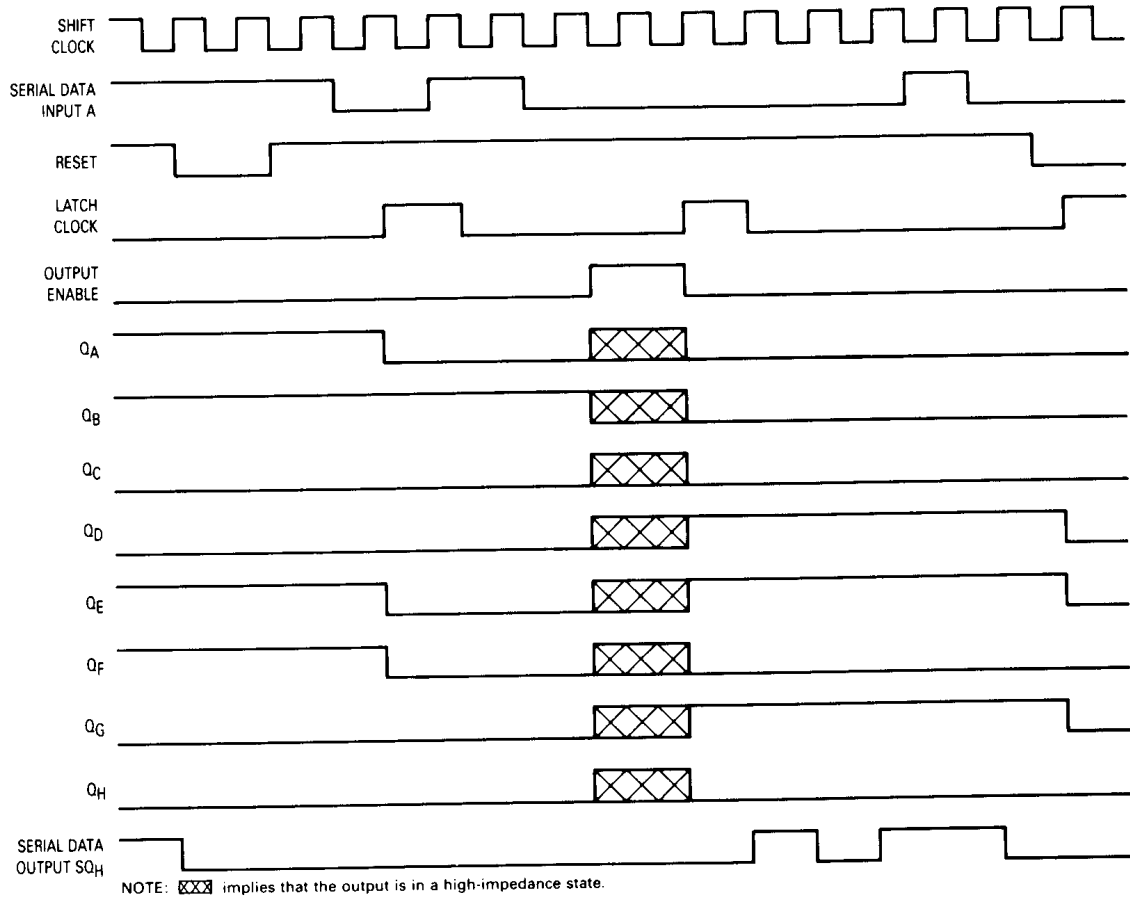
Figure 7. Test Circuit



\*Includes all probe and jig capacitance.

Figure 8. Test Circuit

TIMING DIAGRAM





EXPANDED LOGIC DIAGRAM

