

Features

- High Performance, Low Power AVR[®] 8-bit Microcontroller
- Advanced RISC Architecture
 - 123 Powerful Instructions – Most Single Clock Cycle Execution
 - 32 x 8 General Purpose Working Registers
 - Fully Static Operation
- Non-volatile Program and Data Memories
 - 8K/16K Bytes of In-System Programmable Flash Program Memory
 - Endurance: 10,000 Write/Erase Cycles
 - 512 Bytes of In-System Programmable EEPROM
 - Endurance: 100,000 Write/Erase Cycles
 - 512 Bytes of Internal SRAM
 - Data retention: 20 Years at 85°C / 100 Years at 25°C
 - In-System Programmable via SPI Port
 - Low size LIN/UART Software In-System Programmable
 - Programming Lock for Software Security
- Peripheral Features
 - LIN 2.1 and 1.3 Controller or 8-bit UART
 - One 8-bit Asynchronous Timer/Counter with Prescaler
 - Output Compare or 8-bit PWM Channel
 - One 16-bit Synchronous Timer/Counter with Prescaler
 - External Event Counter
 - 2 Output Compare Units or PWM Channels each Driving up to 4 Output Pins
 - Master/Slave SPI Serial Interface
 - Universal Serial Interface with Start Condition Detector
 - 10-bit ADC
 - 11 Single Ended Channels
 - 8 Differential ADC Channel Pairs with Programmable Gain (8x or 20x)
 - On-chip Analog Comparator with Selectable Voltage Reference
 - 100 μ A \pm 10% Current Source for LIN Node Identification
 - On-chip Temperature Sensor
 - Programmable Watchdog Timer with Separate On-chip Oscillator
- Special Microcontroller Features
 - Software Controlled Clock Switching for Power Control, EMC Reduction
 - debugWIRE On-chip Debug System
 - External and Internal Interrupt Sources
 - Low Power Idle, ADC Noise Reduction, and Power-down Modes
 - Power-on Reset and Programmable Brown-out Detection
 - Internal 8MHz Calibrated Oscillator
 - 4-16 MHz and 32 KHz Crystal/Ceramic Resonator Oscillators
- I/O and Packages
 - 16 Programmable I/O Lines
 - 20-pin SOIC, 32-pad MLF and 20-pin TSSOP
- Operating Voltage:
 - 1.8 – 5.5V for ATtiny87/167
- Speed Grade:
 - 0 – 4 MHz @ 1.8 – 5.5V
 - 0 – 8 MHz @ 2.7 – 5.5V
 - 0 – 16 MHz @ 4.5 – 5.5V
- Industrial Temperature Range



8-bit AVR[®] Microcontroller with 8K/16K Bytes In-System Programmable Flash and LIN Controller

ATtiny87
ATtiny167

Preliminary

Summary

Rev. 8265BS-AVR-09/10



1. Description

1.1 Comparison Between ATtiny87 and ATtiny167

ATtiny87 and ATtiny167 are hardware and software compatible. They differ only in memory sizes as shown in [Table 1-1](#).

Table 1-1. Memory Size Summary

Device	Flash	Flash	Flash	Interrupt Vector size
ATtiny167	16K Bytes	512 Bytes	512 Bytes	2-instruction-words / vector
ATtiny87	8K Bytes	512 Bytes	512 Bytes	2-instruction-words / vector

1.2 Part Description

The ATtiny87/167 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATtiny87/167 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

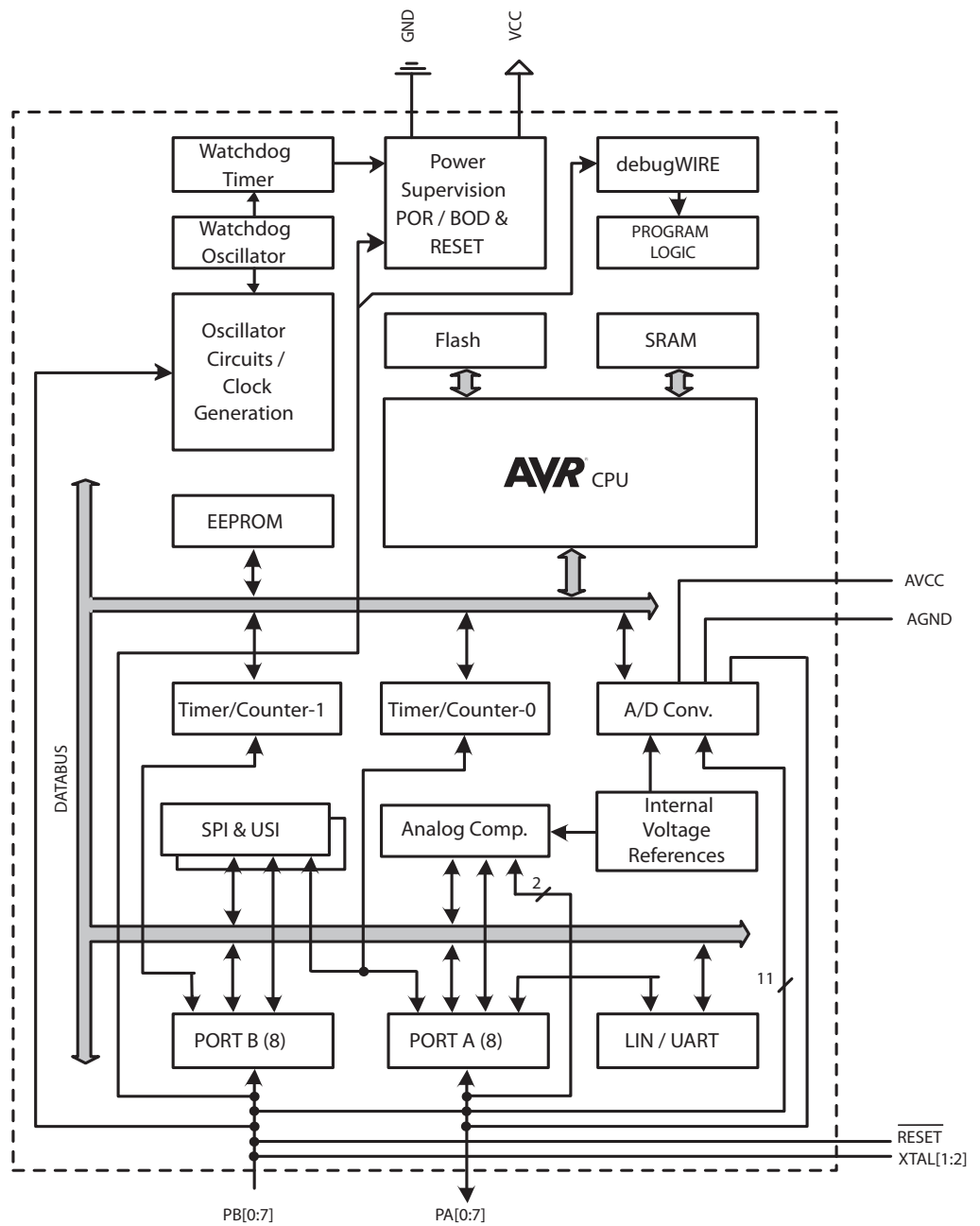
The ATtiny87/167 provides the following features: 8K/16K byte of In-System Programmable Flash, 512 bytes EEPROM, 512 bytes SRAM, 16 general purpose I/O lines, 32 general purpose working registers, one 8-bit Timer/Counter with compare modes, one 8-bit high speed Timer/Counter, Universal Serial Interface, a LIN controller, Internal and External Interrupts, a 11-channel, 10-bit ADC, a programmable Watchdog Timer with internal Oscillator, and three software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counter, ADC, Analog Comparator, and Interrupt system to continue functioning. The Power-down mode saves the register contents, disabling all chip functions until the next Interrupt or Hardware Reset. The ADC Noise Reduction mode stops the CPU and all I/O modules except ADC, to minimize switching noise during ADC conversions.

The device is manufactured using Atmel's high density non-volatile memory technology. The On-chip ISP Flash allows the Program memory to be re-programmed In-System through an SPI serial interface, by a conventional non-volatile memory programmer or by an On-chip boot code running on the AVR core. The Boot program can use any interface to download the application program in the Flash memory. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATtiny87/167 is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The ATtiny87/167 AVR is supported with a full suite of program and system development tools including: C Compilers, Macro Assemblers, Program Debugger/Simulators, In-Circuit Emulators, and Evaluation kits.

1.3 Block Diagram

Figure 1-1. Block Diagram



1.4 Pin Configuration

Figure 1-2. Pinout ATtiny87/167 - SOIC20 & TSSOP20

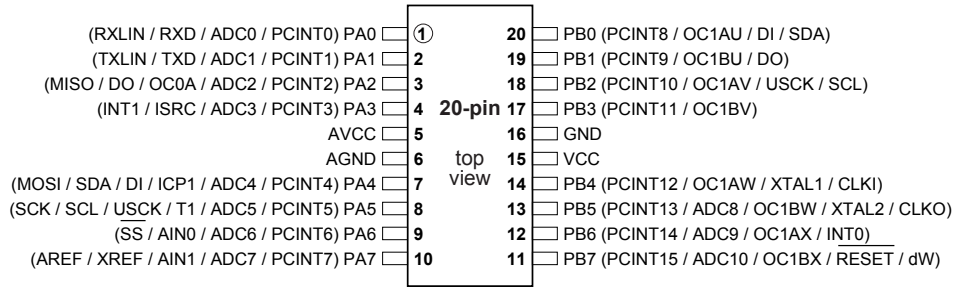
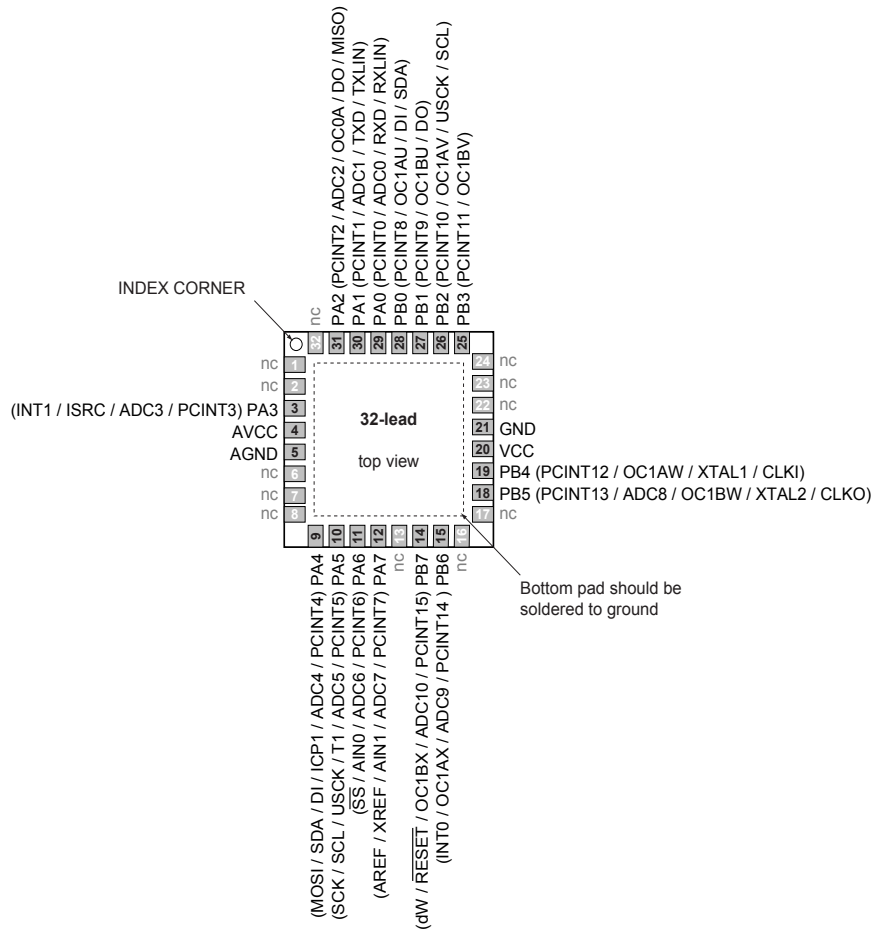


Figure 1-3. Pinout ATtiny87/167 - QFN32/MLF32



1.5 Pin Description

1.5.1 VCC

Supply voltage.

1.5.2 GND

Ground.

1.5.3 AVCC

Analog supply voltage.

1.5.4 AGND

Analog ground.

1.5.5 Port A (PA7:PA0)

Port A is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port A output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port A pins that are externally pulled low will source current if the pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port A also serves the functions of various special features of the ATtiny87/167 as listed on [Section 9.3.3 “Alternate Functions of Port A” on page 76](#).

1.5.6 Port B (PB7:PB0)

Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B also serves the functions of various special features of the ATtiny87/167 as listed on [Section 9.3.4 “Alternate Functions of Port B” on page 81](#).

1.6 Resources

A comprehensive set of development tools, application notes and datasheets are available for download on <http://www.atmel.com/avr>.

1.7 About Code Examples

This documentation contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C compiler documentation for more details.

1.8 Data Retention

Reliability Qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C or 100 years at 25°C.

1.9 Disclaimer

Typical values contained in this datasheet are based on simulations and characterization of other AVR microcontrollers manufactured on the same process technology. Min and Max values will be available after the device has been characterized.

2. Register Summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0xFF)	Reserved									
(0xFE)	Reserved									
(0xFD)	Reserved									
(0xFC)	Reserved									
(0xFB)	Reserved									
(0xFA)	Reserved									
(0xF9)	Reserved									
(0xF8)	Reserved									
(0xF7)	Reserved									
(0xF6)	Reserved									
(0xF5)	Reserved									
(0xF4)	Reserved									
(0xF3)	Reserved									
(0xF2)	Reserved									
(0xF1)	Reserved									
(0xF0)	Reserved									
(0xEF)	Reserved									
(0xEE)	Reserved									
(0xED)	Reserved									
(0xEC)	Reserved									
(0xEB)	Reserved									
(0xEA)	Reserved									
(0xE9)	Reserved									
(0xE8)	Reserved									
(0xE7)	Reserved									
(0xE6)	Reserved									
(0xE5)	Reserved									
(0xE4)	Reserved									
(0xE3)	Reserved									
(0xE2)	Reserved									
(0xE1)	Reserved									
(0xE0)	Reserved									
(0xDF)	Reserved									
(0xDE)	Reserved									
(0xDD)	Reserved									
(0xDC)	Reserved									
(0xDB)	Reserved									
(0xDA)	Reserved									
(0xD9)	Reserved									
(0xD8)	Reserved									
(0xD7)	Reserved									
(0xD6)	Reserved									
(0xD5)	Reserved									
(0xD4)	Reserved									
(0xD3)	Reserved									
(0xD2)	LINDAT	LDATA7	LDATA6	LDATA5	LDATA4	LDATA3	LDATA2	LDATA1	LDATA0	page 187
(0xD1)	LINSEL	–	–	–	–	/LAINC	LINDX2	LINDX1	LINDX0	page 186
(0xD0)	LINIDR	LP1	LP0	LID5 / LDL1	LID4 / LDL0	LID3	LID2	LID1	LID0	page 186
(0xCF)	LINDLR	LTXDL3	LTXDL2	LTXDL1	LTXDL0	LRXDL3	LRXDL2	LRXDL1	LRXDL0	page 185
(0xCE)	LINBRRH	–	–	–	–	LDIV11	LDIV10	LDIV9	LDIV8	page 185
(0xCD)	LINBRRL	LDIV7	LDIV6	LDIV5	LDIV4	LDIV3	LDIV2	LDIV1	LDIV0	page 185
(0xCC)	LINBTR	LDISR	–	LBT5	LBT4	LBT3	LBT2	LBT1	LBT0	page 184
(0xCB)	LINERR	LABORT	LTOERR	LOVERR	LFERR	LSERR	LPERR	LCERR	LBERR	page 183
(0xCA)	LINENIR	–	–	–	–	LENERR	LENIDOK	LENTXOK	LENRXOK	page 183
(0xC9)	LINSIR	LIDST2	LIDST1	LIDST0	LBUSY	LERR	LIDOK	LTXOK	LRXOK	page 182
(0xC8)	LINCR	LSWRES	LIN13	LCONF1	LCONF0	LENA	LCMD2	LCMD1	LCMD0	page 181
(0xC7)	Reserved									
(0xC6)	Reserved									
(0xC5)	Reserved									
(0xC4)	Reserved									
(0xC3)	Reserved									
(0xC2)	Reserved									
(0xC1)	Reserved									
(0xC0)	Reserved									
(0xBF)	Reserved									



Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0xBE)	Reserved									
(0xBD)	Reserved									
(0xBC)	USIPP								USIPOS	page 161
(0xBB)	USIBR	USIB7	USIB6	USIB5	USIB4	USIB3	USIB2	USIB1	USIB0	page 157
(0xBA)	USIDR	USID7	USID6	USID5	USID4	USID3	USID2	USID1	USID0	page 156
(0xB9)	USISR	USISIF	USIOIF	USIPF	USIDC	USICNT3	USICNT2	USICNT1	USICNT0	page 157
(0xB8)	USICR	USISIE	USIOIE	USIWM1	USIWM0	USICS1	USICS0	USICLK	USITC	page 158
(0xB7)	Reserved									
(0xB6)	ASSR	–	EXCLK	AS0	TCN0UB	OCR0AUB	–	TCR0AUB	TCR0BUB	page 103
(0xB5)	Reserved									
(0xB4)	Reserved									
(0xB3)	Reserved									
(0xB2)	Reserved									
(0xB1)	Reserved									
(0xB0)	Reserved									
(0xAF)	Reserved									
(0xAE)	Reserved									
(0xAD)	Reserved									
(0xAC)	Reserved									
(0xAB)	Reserved									
(0xAA)	Reserved									
(0xA9)	Reserved									
(0xA8)	Reserved									
(0xA7)	Reserved									
(0xA6)	Reserved									
(0xA5)	Reserved									
(0xA4)	Reserved									
(0xA3)	Reserved									
(0xA2)	Reserved									
(0xA1)	Reserved									
(0xA0)	Reserved									
(0x9F)	Reserved									
(0x9E)	Reserved									
(0x9D)	Reserved									
(0x9C)	Reserved									
(0x9B)	Reserved									
(0x9A)	Reserved									
(0x99)	Reserved									
(0x98)	Reserved									
(0x97)	Reserved									
(0x96)	Reserved									
(0x95)	Reserved									
(0x94)	Reserved									
(0x93)	Reserved									
(0x92)	Reserved									
(0x91)	Reserved									
(0x90)	Reserved									
(0x8F)	Reserved									
(0x8E)	Reserved									
(0x8D)	Reserved									
(0x8C)	Reserved									
(0x8B)	OCR1BH	OCR1B15	OCR1B14	OCR1B13	OCR1B12	OCR1B11	OCR1B10	OCR1B9	OCR1B8	page 137
(0x8A)	OCR1BL	OCR1B7	OCR1B6	OCR1B5	OCR1B4	OCR1B3	OCR1B2	OCR1B1	OCR1B0	page 137
(0x89)	OCR1AH	OCR1A15	OCR1A14	OCR1A13	OCR1A12	OCR1A11	OCR1A10	OCR1A9	OCR1A8	page 137
(0x88)	OCR1AL	OCR1A7	OCR1A6	OCR1A5	OCR1A4	OCR1A3	OCR1A2	OCR1A1	OCR1A0	page 137
(0x87)	ICR1H	ICR115	ICR114	ICR113	ICR112	ICR111	ICR110	ICR19	ICR18	page 138
(0x86)	ICR1L	ICR17	ICR16	ICR15	ICR14	ICR13	ICR12	ICR11	ICR10	page 138
(0x85)	TCNT1H	TCNT115	TCNT114	TCNT113	TCNT112	TCNT111	TCNT110	TCNT19	TCNT18	page 137
(0x84)	TCNT1L	TCNT17	TCNT16	TCNT15	TCNT14	TCNT13	TCNT12	TCNT11	TCNT10	page 137
(0x83)	TCCR1D	OC1BX	OC1BW	OC1BV	OC1BU	OC1AX	OC1AW	OC1AV	OC1AU	page 136
(0x82)	TCCR1C	FOC1A	FOC1B	–	–	–	–	–	–	page 136
(0x81)	TCCR1B	ICNC1	ICES1	–	WGM13	WGM12	CS12	CS11	CS10	page 135
(0x80)	TCCR1A	COM1A1	COM1A0	COM1B1	COM1B0	–	–	WGM11	WGM10	page 132
(0x7F)	DIDR1	–	ADC10D	ADC9D	ADC8D	–	–	–	–	page 210
(0x7E)	DIDR0	ADC7D/AIN1D	ADC6D/AIN0D	ADC5D	ADC4D	ADC3D	ADC2D	ADC1D	ADC0D	page 209, page 214
(0x7D)	Reserved									

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0x7C)	ADMUX	REFS1	REFS0	ADLAR	MUX4	MUX3	MUX2	MUX1	MUX0	page 205
(0x7B)	ADCSRB	BIN	ACME	ACIR1	ACIR0	–	ADTS2	ADTS1	ADTS0	page 209, page 213
(0x7A)	ADCSRA	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0	page 207
(0x79)	ADCH	- / ADC9	- / ADC8	- / ADC7	- / ADC6	- / ADC5	- / ADC4	ADC9 / ADC3	ADC8 / ADC2	page 208
(0x78)	ADCL	ADC7 / ADC1	ADC6 / ADC0	ADC5 / -	ADC4 / -	ADC3 / -	ADC2 / -	ADC1 / -	ADC0 / -	page 208
(0x77)	AMISCR	–	–	–	–	–	AREFEN	XREFEN	ISRCEN	page 190, page 210
(0x76)	Reserved									
(0x75)	Reserved									
(0x74)	Reserved									
(0x73)	Reserved									
(0x72)	Reserved									
(0x71)	Reserved									
(0x70)	Reserved									
(0x6F)	TIMSK1	–	–	ICIE1	–	–	OCIE1B	OCIE1A	TOIE1	page 138
(0x6E)	TIMSK0	–	–	–	–	–	–	OCIE0A	TOIE0	page 105
(0x6D)	Reserved									
(0x6C)	PCMSK1	PCINT15	PCINT14	PCINT13	PCINT12	PCINT11	PCINT10	PCINT9	PCINT8	page 65
(0x6B)	PCMSK0	PCINT7	PCINT6	PCINT5	PCINT4	PCINT3	PCINT2	PCINT1	PCINT0	page 65
(0x6A)	Reserved									
(0x69)	EICRA	–	–	–	–	ISC11	ISC10	ISC01	ISC00	page 63
(0x68)	PCICR	–	–	–	–	–	–	PCIE1	PCIE0	page 64
(0x67)	Reserved									
(0x66)	OSCCAL	CAL7	CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	page 37
(0x65)	Reserved									
(0x64)	PRR	–	–	PRLIN	PRSPI	PRTIM1	PRTIM0	PRUSI	PRADC	page 47
(0x63)	CLKSELR	–	COUT	CSUT1	CSUT0	CSEL3	CSEL2	CSEL1	CSEL0	page 40
(0x62)	CLKCSR	CLKCCE	–	–	CLKRDY	CLKC3	CLKC2	CLKC1	CLKC0	page 38
(0x61)	CLKPR	CLKPCE	–	–	–	CLKPS3	CLKPS2	CLKPS1	CLKPS0	page 38
(0x60)	WDTCR	WDIF	WDIE	WDP3	WDCE	WDE	WDP2	WDP1	WDP0	page 57
0x3F (0x5F)	SREG	I	T	H	S	V	N	Z	C	page 9
0x3E (0x5E)	SPH	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	page 11
0x3D (0x5D)	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	page 11
0x3C (0x5C)	Reserved									
0x3B (0x5B)	Reserved									
0x3A (0x5A)	Reserved									
0x39 (0x59)	Reserved									
0x38 (0x58)	Reserved									
0x37 (0x57)	SPMCSR	–	RWWSB	SIGRD	CTPB	RFLB	PGWRT	PGERS	SPMEN	page 219
0x36 (0x56)	Reserved									
0x35 (0x55)	MCUCR	–	BODS	BODSE	PUD	–	–	–	–	page 47, page 75
0x34 (0x54)	MCUSR	–	–	–	–	WDRF	BORF	EXTRF	PORF	page 52
0x33 (0x53)	SMCR	–	–	–	–	–	SM1	SM0	SE	page 46
0x32 (0x52)	Reserved									
0x31 (0x51)	DWDR	DWDR7	DWDR6	DWDR5	DWDR4	DWDR3	DWDR2	DWDR1	DWDR0	page 216
0x30 (0x50)	ACSR	ACD	ACIRS	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	page 213
0x2F (0x4F)	Reserved									
0x2E (0x4E)	SPDR	SPD7	SPD6	SPD5	SPD4	SPD3	SPD2	SPD1	SPD0	page 147
0x2D (0x4D)	SPSR	SPIF	WCOL	–	–	–	–	–	SPI2X	page 147
0x2C (0x4C)	SPCR	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	page 145
0x2B (0x4B)	GPIOR2	GPIOR27	GPIOR26	GPIOR25	GPIOR24	GPIOR23	GPIOR22	GPIOR21	GPIOR20	page 23
0x2A (0x4A)	GPIOR1	GPIOR17	GPIOR16	GPIOR15	GPIOR14	GPIOR13	GPIOR12	GPIOR11	GPIOR10	page 23
0x29 (0x49)	Reserved									
0x28 (0x48)	OCR0A	OCR0A7	OCR0A6	OCR0A5	OCR0A4	OCR0A3	OCR0A2	OCR0A1	OCR0A0	page 103
0x27 (0x47)	TCNT0	TCNT07	TCNT06	TCNT05	TCNT04	TCNT03	TCNT02	TCNT01	TCNT00	page 103
0x26 (0x46)	TCCR0B	FOC0A	–	–	–	–	CS02	CS01	CS00	page 102
0x25 (0x45)	TCCR0A	COM0A1	COM0A0	–	–	–	–	WGM01	WGM00	page 100
0x24 (0x44)	Reserved									
0x23 (0x43)	GTCCR	TSM	–	–	–	–	–	PSR0	PSR1	page 106, page 109
0x22 (0x42)	EEARH⁽¹⁾	–	–	–	–	–	–	–	EEAR8	page 21
0x21 (0x41)	EEARL	EEAR7	EEAR6	EEAR5	EEAR4	EEAR3	EEAR2	EEAR1	EEAR0	page 21
0x20 (0x40)	EEDR	EEDR7	EEDR6	EEDR5	EEDR4	EEDR3	EEDR2	EEDR1	EEDR0	page 22
0x1F (0x3F)	EEDR	–	–	EEDR5	EEDR4	EEDR3	EEDR2	EEDR1	EEDR0	page 22
0x1E (0x3E)	GPIOR0	GPIOR07	GPIOR06	GPIOR05	GPIOR04	GPIOR03	GPIOR02	GPIOR01	GPIOR00	page 23
0x1D (0x3D)	EIMSK	–	–	–	–	–	–	INT1	INT0	page 63
0x1C (0x3C)	EIFR	–	–	–	–	–	–	INTF1	INTF0	page 64
0x1B (0x3B)	PCIFR	–	–	–	–	–	–	PCIF1	PCIF0	page 65

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x1A (0x3A)	Reserved									
0x19 (0x39)	Reserved									
0x18 (0x38)	Reserved									
0x17 (0x37)	Reserved									
0x16 (0x36)	TIFR1	–	–	ICF1	–	–	OCF1B	OCF1A	TOV1	page 139
0x15 (0x35)	TIFR0	–	–	–	–	–	–	OCF0A	TOV0	page 105
0x14 (0x34)	Reserved									
0x13 (0x33)	Reserved									
0x12 (0x32)	PORTCR	–	–	BBMB	BBMA	–	–	PUDB	PUDA	page 75
0x11 (0x31)	Reserved									
0x10 (0x30)	Reserved									
0x0F (0x2F)	Reserved									
0x0E (0x2E)	Reserved									
0x0D (0x2D)	Reserved									
0x0C (0x2C)	Reserved									
0x0B (0x2B)	Reserved									
0x0A (0x2A)	Reserved									
0x09 (0x29)	Reserved									
0x08 (0x28)	Reserved									
0x07 (0x27)	Reserved									
0x06 (0x26)	Reserved									
0x05 (0x25)	PORTB	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	page 86
0x04 (0x24)	DDRB	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	page 86
0x03 (0x23)	PINB	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	page 86
0x02 (0x22)	PORTA	PORTA7	PORTA6	PORTA5	PORTA4	PORTA3	PORTA2	PORTA1	PORTA0	page 86
0x01 (0x21)	DDRA	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0	page 86
0x00 (0x20)	PINA	PINA7	PINA6	PINA5	PINA4	PINA3	PINA2	PINA1	PINA0	page 86

- Notes:
1. Address bits exceeding EEAMSB ([Table 21-8 on page 228](#)) are don't care.
 2. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
 3. I/O Registers within the address range 0x00 - 0x1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions.
 4. Some of the status flags are cleared by writing a logical one to them. Note that, unlike most other AVRs, the CBI and SBI instructions will only operate on the specified bit, and can therefore be used on registers containing such status flags. The CBI and SBI instructions work with registers 0x00 to 0x1F only.
 5. When using the I/O specific commands IN and OUT, the I/O addresses 0x00 - 0x3F must be used. When addressing I/O Registers as data space using LD and ST instructions, 0x20 must be added to these addresses. The ATtiny87/167 is a complex microcontroller with more peripheral units than can be supported within the 64 location reserved in Opcode for the IN and OUT instructions. For the Extended I/O space from 0x60 - 0xFF in SRAM, only the ST/STS/STD and LD/LDS/LDD instructions can be used.

3. Instruction Set Summary

Mnemonics	Operands	Description	Operation	Flags	#Clock
ARITHMETIC AND LOGIC INSTRUCTIONS					
ADD	Rd, Rr	Add two Registers	$Rd \leftarrow Rd + Rr$	Z,C,N,V,H	1
ADC	Rd, Rr	Add with Carry two Registers	$Rd \leftarrow Rd + Rr + C$	Z,C,N,V,H	1
ADIW	Rdl,K	Add Immediate to Word	$Rdh:Rdl \leftarrow Rdh:Rdl + K$	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract two Registers	$Rd \leftarrow Rd - Rr$	Z,C,N,V,H	1
SUBI	Rd, K	Subtract Constant from Register	$Rd \leftarrow Rd - K$	Z,C,N,V,H	1
SBC	Rd, Rr	Subtract with Carry two Registers	$Rd \leftarrow Rd - Rr - C$	Z,C,N,V,H	1
SBCI	Rd, K	Subtract with Carry Constant from Reg.	$Rd \leftarrow Rd - K - C$	Z,C,N,V,H	1
SBIW	Rdl,K	Subtract Immediate from Word	$Rdh:Rdl \leftarrow Rdh:Rdl - K$	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND Registers	$Rd \leftarrow Rd \cdot Rr$	Z,N,V	1
ANDI	Rd, K	Logical AND Register and Constant	$Rd \leftarrow Rd \cdot K$	Z,N,V	1
OR	Rd, Rr	Logical OR Registers	$Rd \leftarrow Rd \vee Rr$	Z,N,V	1
ORI	Rd, K	Logical OR Register and Constant	$Rd \leftarrow Rd \vee K$	Z,N,V	1
EOR	Rd, Rr	Exclusive OR Registers	$Rd \leftarrow Rd \oplus Rr$	Z,N,V	1
COM	Rd	One's Complement	$Rd \leftarrow 0xFF - Rd$	Z,C,N,V	1
NEG	Rd	Two's Complement	$Rd \leftarrow 0x00 - Rd$	Z,C,N,V,H	1
SBR	Rd,K	Set Bit(s) in Register	$Rd \leftarrow Rd \vee K$	Z,N,V	1
CBR	Rd,K	Clear Bit(s) in Register	$Rd \leftarrow Rd \cdot (0xFF - K)$	Z,N,V	1
INC	Rd	Increment	$Rd \leftarrow Rd + 1$	Z,N,V	1
DEC	Rd	Decrement	$Rd \leftarrow Rd - 1$	Z,N,V	1
TST	Rd	Test for Zero or Minus	$Rd \leftarrow Rd \cdot Rd$	Z,N,V	1
CLR	Rd	Clear Register	$Rd \leftarrow Rd \oplus Rd$	Z,N,V	1
SER	Rd	Set Register	$Rd \leftarrow 0xFF$	None	1
BRANCH INSTRUCTIONS					
RJMP	k	Relative Jump	$PC \leftarrow PC + k + 1$	None	2
IJMP		Indirect Jump to (Z)	$PC \leftarrow Z$	None	2
JMP	k	Direct Jump	$PC \leftarrow k$	None	3
RCALL	k	Relative Subroutine Call	$PC \leftarrow PC + k + 1$	None	3
ICALL		Indirect Call to (Z)	$PC \leftarrow Z$	None	3
CALL	k	Direct Subroutine Call	$PC \leftarrow k$	None	4
RET		Subroutine Return	$PC \leftarrow STACK$	None	4
RETI		Interrupt Return	$PC \leftarrow STACK$	I	4
CPSE	Rd,Rr	Compare, Skip if Equal	if (Rd = Rr) $PC \leftarrow PC + 2$ or 3	None	1/2/3
CP	Rd,Rr	Compare	$Rd - Rr$	Z, N,V,C,H	1
CPC	Rd,Rr	Compare with Carry	$Rd - Rr - C$	Z, N,V,C,H	1
CPI	Rd,K	Compare Register with Immediate	$Rd - K$	Z, N,V,C,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b)=0) $PC \leftarrow PC + 2$ or 3	None	1/2/3
SBRS	Rr, b	Skip if Bit in Register is Set	if (Rr(b)=1) $PC \leftarrow PC + 2$ or 3	None	1/2/3
SBIC	P, b	Skip if Bit in I/O Register Cleared	if (P(b)=0) $PC \leftarrow PC + 2$ or 3	None	1/2/3
SBIS	P, b	Skip if Bit in I/O Register is Set	if (P(b)=1) $PC \leftarrow PC + 2$ or 3	None	1/2/3
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BREQ	k	Branch if Equal	if (Z = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRNE	k	Branch if Not Equal	if (Z = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRCS	k	Branch if Carry Set	if (C = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRCC	k	Branch if Carry Cleared	if (C = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRSH	k	Branch if Same or Higher	if (C = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRLO	k	Branch if Lower	if (C = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRMI	k	Branch if Minus	if (N = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRPL	k	Branch if Plus	if (N = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRGE	k	Branch if Greater or Equal, Signed	if (N \oplus V = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRLT	k	Branch if Less Than Zero, Signed	if (N \oplus V = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRTS	k	Branch if T Flag Set	if (T = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRTC	k	Branch if T Flag Cleared	if (T = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BIT AND BIT-TEST INSTRUCTIONS					
SBI	P,b	Set Bit in I/O Register	$I/O(P,b) \leftarrow 1$	None	2
CBI	P,b	Clear Bit in I/O Register	$I/O(P,b) \leftarrow 0$	None	2
LSL	Rd	Logical Shift Left	$Rd(n+1) \leftarrow Rd(n), Rd(0) \leftarrow 0$	Z,C,N,V	1



Mnemonics	Operands	Description	Operation	Flags	#Clock
LSR	Rd	Logical Shift Right	$Rd(n) \leftarrow Rd(n+1), Rd(7) \leftarrow 0$	Z,C,N,V	1
ROL	Rd	Rotate Left Through Carry	$Rd(0) \leftarrow C, Rd(n+1) \leftarrow Rd(n), C \leftarrow Rd(7)$	Z,C,N,V	1
ROR	Rd	Rotate Right Through Carry	$Rd(7) \leftarrow C, Rd(n) \leftarrow Rd(n+1), C \leftarrow Rd(0)$	Z,C,N,V	1
ASR	Rd	Arithmetic Shift Right	$Rd(n) \leftarrow Rd(n+1), n=0..6$	Z,C,N,V	1
SWAP	Rd	Swap Nibbles	$Rd(3..0) \leftarrow Rd(7..4), Rd(7..4) \leftarrow Rd(3..0)$	None	1
BSET	s	Flag Set	$SREG(s) \leftarrow 1$	SREG(s)	1
BCLR	s	Flag Clear	$SREG(s) \leftarrow 0$	SREG(s)	1
BST	Rr, b	Bit Store from Register to T	$T \leftarrow Rr(b)$	T	1
BLD	Rd, b	Bit load from T to Register	$Rd(b) \leftarrow T$	None	1
SEC		Set Carry	$C \leftarrow 1$	C	1
CLC		Clear Carry	$C \leftarrow 0$	C	1
SEN		Set Negative Flag	$N \leftarrow 1$	N	1
CLN		Clear Negative Flag	$N \leftarrow 0$	N	1
SEZ		Set Zero Flag	$Z \leftarrow 1$	Z	1
CLZ		Clear Zero Flag	$Z \leftarrow 0$	Z	1
SEI		Global Interrupt Enable	$I \leftarrow 1$	I	1
CLI		Global Interrupt Disable	$I \leftarrow 0$	I	1
SES		Set Signed Test Flag	$S \leftarrow 1$	S	1
CLS		Clear Signed Test Flag	$S \leftarrow 0$	S	1
SEV		Set Twos Complement Overflow.	$V \leftarrow 1$	V	1
CLV		Clear Twos Complement Overflow	$V \leftarrow 0$	V	1
SET		Set T in SREG	$T \leftarrow 1$	T	1
CLT		Clear T in SREG	$T \leftarrow 0$	T	1
SEH		Set Half Carry Flag in SREG	$H \leftarrow 1$	H	1
CLH		Clear Half Carry Flag in SREG	$H \leftarrow 0$	H	1
DATA TRANSFER INSTRUCTIONS					
MOV	Rd, Rr	Move Between Registers	$Rd \leftarrow Rr$	None	1
MOVW	Rd, Rr	Copy Register Word	$Rd+1:Rd \leftarrow Rr+1:Rr$	None	1
LDI	Rd, K	Load Immediate	$Rd \leftarrow K$	None	1
LD	Rd, X	Load Indirect	$Rd \leftarrow (X)$	None	2
LD	Rd, X+	Load Indirect and Post-Inc.	$Rd \leftarrow (X), X \leftarrow X + 1$	None	2
LD	Rd, -X	Load Indirect and Pre-Dec.	$X \leftarrow X - 1, Rd \leftarrow (X)$	None	2
LD	Rd, Y	Load Indirect	$Rd \leftarrow (Y)$	None	2
LD	Rd, Y+	Load Indirect and Post-Inc.	$Rd \leftarrow (Y), Y \leftarrow Y + 1$	None	2
LD	Rd, -Y	Load Indirect and Pre-Dec.	$Y \leftarrow Y - 1, Rd \leftarrow (Y)$	None	2
LDD	Rd, Y+q	Load Indirect with Displacement	$Rd \leftarrow (Y + q)$	None	2
LD	Rd, Z	Load Indirect	$Rd \leftarrow (Z)$	None	2
LD	Rd, Z+	Load Indirect and Post-Inc.	$Rd \leftarrow (Z), Z \leftarrow Z + 1$	None	2
LD	Rd, -Z	Load Indirect and Pre-Dec.	$Z \leftarrow Z - 1, Rd \leftarrow (Z)$	None	2
LDD	Rd, Z+q	Load Indirect with Displacement	$Rd \leftarrow (Z + q)$	None	2
LDS	Rd, k	Load Direct from SRAM	$Rd \leftarrow (k)$	None	2
ST	X, Rr	Store Indirect	$(X) \leftarrow Rr$	None	2
ST	X+, Rr	Store Indirect and Post-Inc.	$(X) \leftarrow Rr, X \leftarrow X + 1$	None	2
ST	-X, Rr	Store Indirect and Pre-Dec.	$X \leftarrow X - 1, (X) \leftarrow Rr$	None	2
ST	Y, Rr	Store Indirect	$(Y) \leftarrow Rr$	None	2
ST	Y+, Rr	Store Indirect and Post-Inc.	$(Y) \leftarrow Rr, Y \leftarrow Y + 1$	None	2
ST	-Y, Rr	Store Indirect and Pre-Dec.	$Y \leftarrow Y - 1, (Y) \leftarrow Rr$	None	2
STD	Y+q, Rr	Store Indirect with Displacement	$(Y + q) \leftarrow Rr$	None	2
ST	Z, Rr	Store Indirect	$(Z) \leftarrow Rr$	None	2
ST	Z+, Rr	Store Indirect and Post-Inc.	$(Z) \leftarrow Rr, Z \leftarrow Z + 1$	None	2
ST	-Z, Rr	Store Indirect and Pre-Dec.	$Z \leftarrow Z - 1, (Z) \leftarrow Rr$	None	2
STD	Z+q, Rr	Store Indirect with Displacement	$(Z + q) \leftarrow Rr$	None	2
STS	k, Rr	Store Direct to SRAM	$(k) \leftarrow Rr$	None	2
LPM		Load Program Memory	$R0 \leftarrow (Z)$	None	3
LPM	Rd, Z	Load Program Memory	$Rd \leftarrow (Z)$	None	3
LPM	Rd, Z+	Load Program Memory and Post-Inc	$Rd \leftarrow (Z), Z \leftarrow Z + 1$	None	3
SPM		Store Program Memory	$(Z) \leftarrow R1:R0$	None	-
IN	Rd, P	In Port	$Rd \leftarrow P$	None	1
OUT	P, Rr	Out Port	$P \leftarrow Rr$	None	1
PUSH	Rr	Push Register on Stack	$STACK \leftarrow Rr$	None	2
POP	Rd	Pop Register from Stack	$Rd \leftarrow STACK$	None	2
MCU CONTROL INSTRUCTIONS					
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep function)	None	1
WDR		Watchdog Reset	(see specific descr. for WDR/timer)	None	1
BREAK		Break	For On-chip Debug Only	None	N/A

4. Ordering Information

4.1 ATtiny87

Speed (MHz)	Power Supply (V)	Ordering Code	Package ⁽¹⁾	Operational Range
16	1.8 – 5.5	ATtiny87-MU ATtiny87-MUR ⁽²⁾ ATtiny87-SU ATtiny87-SUR ⁽²⁾ ATtiny87-XU ATtiny87-XUR ⁽²⁾	32M1-A 32M1-A 20S2 20S2 20X 20X	Industrial (-40°C to +85°C) ⁽³⁾

- Notes:
1. All packages are Pb-free, halide-free and fully green and they comply with the European directive for Restriction of Hazardous Substances (RoHS).
 2. Tape and reel.
 3. These devices can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

Package Type	
32M1-A	32-pad, 5 x 5 x 1.0 mm Body, Lead Pitch 0.50 mm, Micro Lead Frame Package (MLF)
20S2	20-lead, 0.300" Wide, Plastic Gull Wing Small Outline Package (SOIC)
20X	20-lead, 4.4 mm Wide, Plastic Thin Shrink Small Outline Package (TSSOP)



4.2 ATtiny167

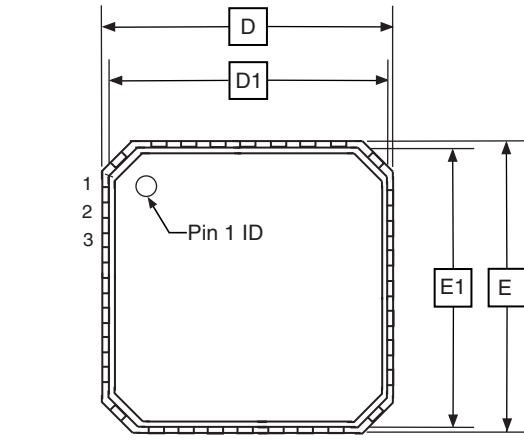
Speed (MHz)	Power Supply (V)	Ordering Code	Package ⁽¹⁾	Operational Range
20	1.8 – 5.5	ATtiny167-MU ATtiny167-MUR ⁽²⁾ ATtiny167-SU ATtiny167-SUR ⁽²⁾ ATtiny167-XU ATtiny167-XUR ⁽²⁾	32M1-A 32M1-A 20S2 20S2 20X 20X	Industrial (-40°C to +85°C) ⁽³⁾

- Notes:
1. All packages are Pb-free, halide-free and fully green and they comply with the European directive for Restriction of Hazardous Substances (RoHS).
 2. Tape and reel.
 3. These devices can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

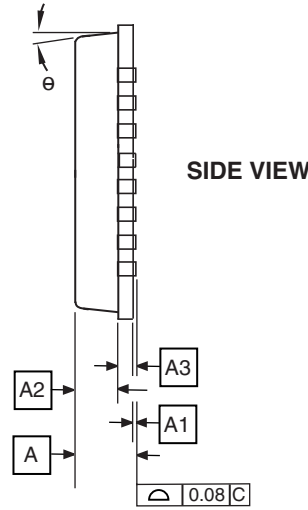
Package Type	
32M1-A	32-pad, 5 x 5 x 1.0 mm Body, Lead Pitch 0.50 mm, Micro Lead Frame Package (MLF)
20S2	20-lead, 0.300" Wide, Plastic Gull Wing Small Outline Package (SOIC)
20X	20-lead, 4.4 mm Wide, Plastic Thin Shrink Small Outline Package (TSSOP)

5. Packaging Information

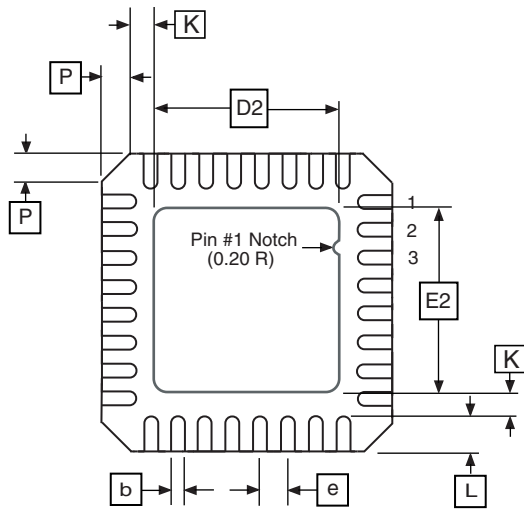
5.1 32M1-A



TOP VIEW



SIDE VIEW



BOTTOM VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	-	0.02	0.05	
A2	-	0.65	1.00	
A3	0.20 REF			
b	0.18	0.23	0.30	
D	4.90	5.00	5.10	
D1	4.70	4.75	4.80	
D2	2.95	3.10	3.25	
E	4.90	5.00	5.10	
E1	4.70	4.75	4.80	
E2	2.95	3.10	3.25	
e	0.50 BSC			
L	0.30	0.40	0.50	
P	-	-	0.60	
θ	-	-	12°	
K	0.20	-	-	

Note: JEDEC Standard MO-220, Fig. 2 (Anvil Singulation), VHHD-2.

5/25/06



2325 Orchard Parkway
San Jose, CA 95131

TITLE

32M1-A, 32-pad, 5 x 5 x 1.0 mm Body, Lead Pitch 0.50 mm,
3.10 mm Exposed Pad, Micro Lead Frame Package (MLF)

DRAWING NO.

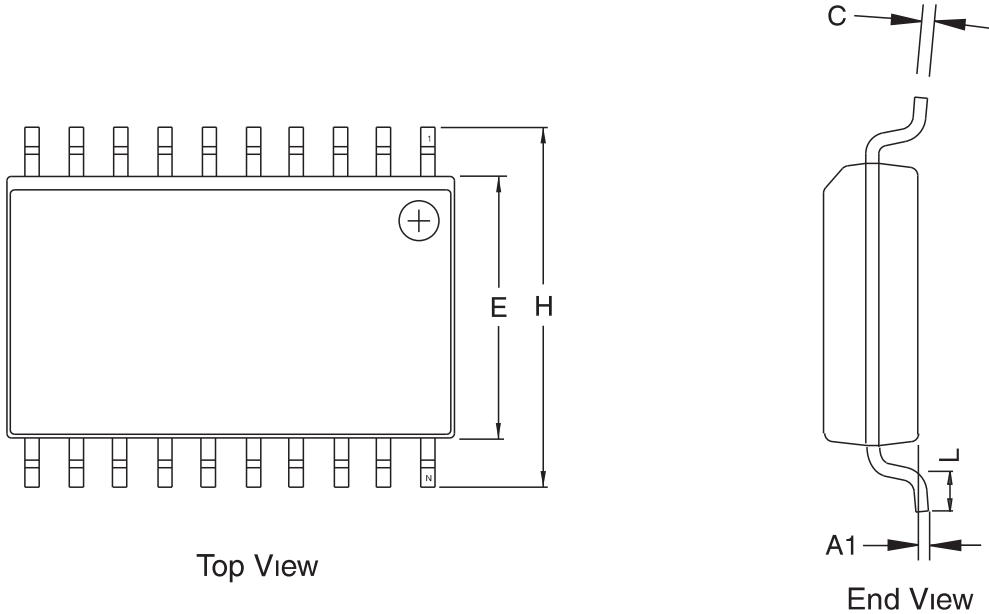
32M1-A

REV.

E

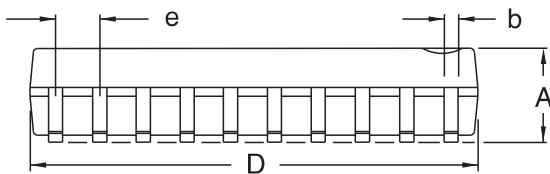


5.2 20S2



Top View

End View



Side View

COMMON DIMENSIONS
(Unit of Measure – mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	2.35		2.65	
A1	0.10		0.30	
b	0.33		0.51	4
C	0.23		0.32	
D	12.60		13.00	1
E	7.40		7.60	2
H	10.00		10.65	
L	0.40		1.27	3
e	1.27 BSC			

- Notes.
1. This drawing is for general information only; refer to JEDEC Drawing MS-013, Variation AC for additional information.
 2. Dimension 'D' does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006") per side.
 3. Dimension 'E' does not include inter-lead Flash or protrusion. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010") per side.
 4. 'L' is the length of the terminal for soldering to a substrate.
 5. The lead width 'b', as measured 0.36 mm (0.014") or greater above the seating plane, shall not exceed a maximum value of 0.61 mm (0.024") per side.

11/6/06



2325 Orchard Parkway
San Jose, CA 95131

TITLE

20S2, 20-lead, 0.300" Wide Body, Plastic Gull Wing Small Outline Package (SOIC)

DRAWING NO.

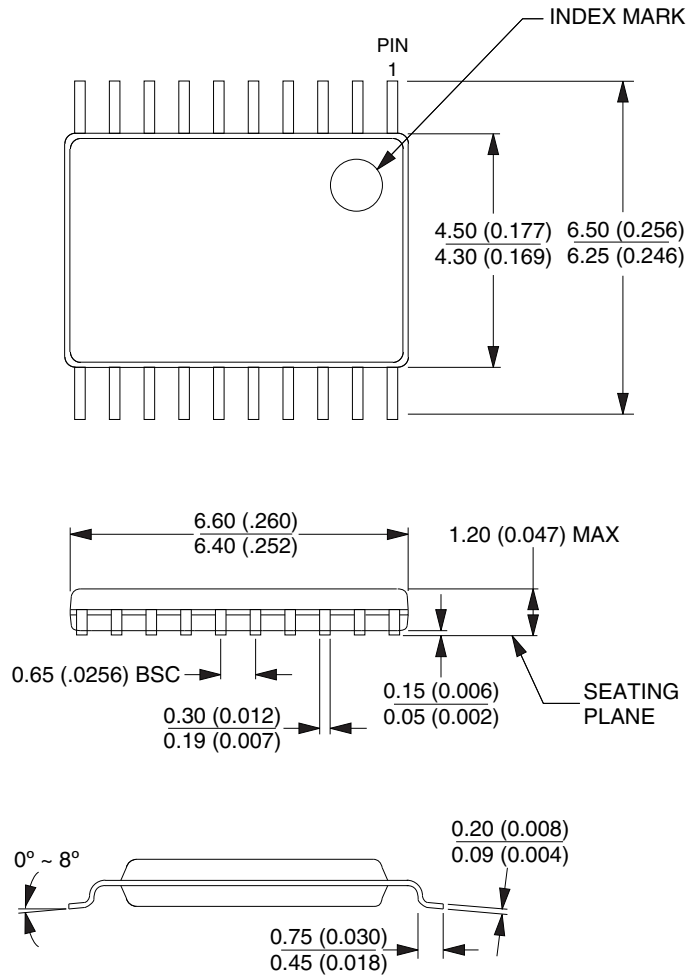
20S2

REV.

B

5.3 20X

Dimensions in Millimeters and (Inches).
 Controlling dimension: Millimeters.
 JEDEC Standard MO-153 AC



10/23/03



2325 Orchard Parkway
 San Jose, CA 95131

TITLE

20X, (Formerly 20T), 20-lead, 4.4 mm Body Width,
 Plastic Thin Shrink Small Outline Package (TSSOP)

DRAWING NO.

20X

REV.

C



6. Errata

6.1 Errata ATtiny87

The revision letter in this section refers to the revision of the ATtiny87 device.

6.1.1 Rev. C

- Gain control of the crystal oscillator.
- ‘Disable Clock Source’ command remains enabled.

6.1.2 Rev. A - B

Not sampled.

6.2 Errata ATtiny167

The revision letter in this section refers to the revision of the ATtiny167 device.

6.2.1 Rev. C

- Gain control of the crystal oscillator.
- ‘Disable Clock Source’ command remains enabled.

6.2.2 Rev. A - B

Not sampled.

6.3 Errata Description

1. Gain control of the crystal oscillator.

The crystal oscillator (0.4 -> 16 MHz) doesn't latch its gain control (CKSEL/CSEL[2:0] bits):

- a. The ‘Recover System Clock Source’ command doesn't returns CSEL[2:0] bits.
- b. The gain control can be modified on the fly if CLKSELR changes.

Problem fix / workaround .

- a. No workaround.
- b. As soon as possible, after any CLKSELR modification, re-write the appropriate crystal oscillator setting (CSEL[3]=1 and CSEL[2:0] / CSUT[1:0] bits) in CLKSELR.

Code example:

```

; Select crystal oscillator ( 16MHz crystal, fast rising power)
ldi    temp1, ((0x0F<<CSEL0) | (0x02<<CSUT0))
sts    CLKSELR, temp1

; Enable clock source (crystal oscillator)
ldi    temp2, (1<<CLKCCE)
ldi    temp3, (0x02<<CLKC0)    ; CSEL = "0010"
sts    CLKCSR, temp2          ; Enable CLKCSR register access
sts    CLKCSR, temp3          ; Enable crystal oscillator clock

; Clock source switch
ldi    temp3, (0x04<<CLKC0)    ; CSEL = "0100"
sts    CLKCSR, temp2          ; Enable CLKCSR register access

```

```

    sts    CLKCSR,temp3          ; Clock source switch
; Select watchdog clock ( 128KHz, fast rising power)
    ldi    temp3, ((0x03<<CSEL0) | (0x02<<CSUT0))
    sts    CLKSELR, temp3      ; (*)
; (*) !!! Loose gain control of crystal oscillator !!!
; ==> WORKAROUND ...
    sts    CLKSELR, temp1
; ...

```

3. 'Disable Clock Source' command remains enabled.

In the Dynamic Clock Switch module, the 'Disable Clock Source' command remains running after disabling the targeted clock source (the clock source is set in the CLKSELR register).

Problem fix / workaround.

After a 'Disable Clock Source' command, reset the CLKCSR register writing 0x80.

Code example:

```

; Select crystal oscillator
    ldi    temp1, (0x0F<<CSEL0)
    sts    CLKSELR, temp1
; Disable clock source (crystal oscillator)
    ldi    temp2, (1<<CLKCCE)
    ldi    temp3, (0x01<<CLKC0)    ; CSEL = "0001"
    sts    CLKCSR,temp2          ; Enable CLKCSR register access
    sts    CLKCSR,temp3          ; (*) Disable crystal oscillator clock
; (*) !!! At this moment, if any other clock source is selected by
; CLKSELR,
;     this clock source will also stop !!!
; ==> WORKAROUND ...
    sts    CLKCSR,temp2

```

7. Datasheet Revision History

Please note that the referring page numbers refer to the complete document.

7.1 Rev. 8265B – 9/10

Updated:

- [Section 9.3.3 “Alternate Functions of Port A” on page 76](#), Bit 3 and Bit 4
- [Section 26.2 “ATtiny167” on page 278](#), ordering codes
- [Section 10.11.1 “TCCR0A – Timer/Counter0 Control Register A” on page 100](#), Bit 1 and Bit 0 descriptions
- Bit syntax throughout the datasheet, e.g. from CS02:0 to CS0[2:0]

7.2 Rev. 8265A – 8/10

1. Initial revision created from document 7728G - 06/10.



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