

## Active Errata List

- During UART Reception, Clearing REN May Generate Unexpected IT
- Timer 2 – Baud Rate Generator – Long Start Time
- C51 Core – Bad Exit of Power-down in X2 Mode
- PCA – Incorrect Behavior with CPU X2 Mode Bit of HSB
- Timer0/1 – Extra Interrupt
- Boot process - Upper 2Kbytes execution with BLJB=0
- Flash/EEPROM - First Read after Load Disturbed

## Errata History

Lot Number	Errata List
All	1, 2, 3, 4, 5, 6, 7

## Errata Descriptions

### 1. During UART Reception, Clearing REN May Generate Unexpected IT

During UART reception, if the REN bit is cleared between start bit detection and the end of reception, the UART will not discard the data (RI is set).

#### Workaround

Test REN at the beginning of Interrupt routine directly after CLR RI, and run the Interrupt routine code only if REN is set.

### 2. Timer 2 – Baud Rate Generator – Long Start Time

When Timer 2 is used as a baud rate generator, TH2 is not loaded with RCAP2H at the beginning, then UART is not operational before 10,000 machine cycles.

#### Workaround

Add the initialization of TH2 and TL2 in the initialization of Timer 2.

### 3. C51 Core – Bad Exit of Power-down in X2 Mode

When exiting power-down mode by interrupt while CPU is in X2 mode, it leads to bad execution of the first instruction run when CPU restarts.

#### Workaround

Set the CPU in X1 mode directly before entering power-down mode.

### 4. PCA – Incorrect behavior with CPU X2 mode bit of HSB

When starting the microcontroller in X2 mode upon reset with the X2 fuse bit of the HSB, the PCA may not work properly when configured with Timer 0 in X1 mode as clock input.

#### Workaround

Set the CPU in X2 mode by software by writing CKCON register at the begin of the application.

### 5. Timer0/1 – Extra Interrupt

When Timer0 is in X1 mode and Timer1 in X2 mode and vice versa, extra interrupt may randomly occur for Timer0 or Timer1.

#### Workaround



80C51 MCUs

AT89C51RD2

AT89C51ED2

Errata Sheet

4257E-8051-08/07



Use the same mode for the two timers..

**6. Boot Process - Upper 2Kbytes Execution with BLJB = 0**

In case of Boot process with BLJB = 0 and BSB = 00, the User Application is executed but the program space located in the upper 2KBytes of the 64KBytes on chip Flash memory cannot be executed. This is due to ENBOOT bit which is set in this Bootloader flow.

**Workaround**

Clear ENBOOT bit at the beginning of user application software.

**7. Flash/EEPROM - First Read after Load Disturbed**

In the 'In-Application Programming' mode from the Flash, if the User software application loads the Column Latch Area prior to calling the programming sequence in the UART Bootloader.

The 'Read after load' issue leads to a wrong Opcode Fetch during the column latch load sequence.

**Workaround**

Update of the Flash API Library. A NOP instruction has to be inserted after the load instruction.

```
MOVX @DPTR,A ;Load Column latches
```

```
NOP ; ADDED INSTRUCTION
```

## Active UART Bootloader Errata List

- API program Data Byte - Incorrect Return Value
- API program Data Page - Incorrect Return Value

## UART Bootloader Errata History

Version Number	Errata List
0.0 (1.0.0 displayed by FLIP)	1,2

## UART Bootloader Errata Description

### 1. API Program Data Byte - Incorrect Return Value

The PROGRAM DATA BYTE API returns the '0xXX' instead of 0x00 in ACC, but the programmng operation is sucessfully completed.

### 2. API Program Data Page- Incorrect Return Value

The PROGRAM DATA PAGE API returns the '0xXX' instead of 0x00 in ACC, but the programmng operation is sucessfully completed.



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