MBM29PL160TD/BD-75/90

Data Sheet *(Retired Product)*

This product has been retired and is not recommended for new designs. Availability of this document is retained for reference and historical purposes only.

Continuity of Specifications

There is no change to this data sheet as a result of offering the device as a Spansion product. Any changes that have been made are the result of normal data sheet improvement and are noted in the document revision summary.

For More Information

Please contact your local sales office for additional information about Spansion memory solutions.

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SPANSION™ Flash Memory

Data Sheet

September 2003

This document specifies SPANSION™ memory products that are now offered by both Advanced Micro Devices and Fujitsu. Although the document is marked with the name of the company that originally developed the specification, these products will be offered to customers of both AMD and Fujitsu.

Continuity of Specifications

There is no change to this datasheet as a result of offering the device as a SPANSION™ product. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

Continuity of Ordering Part Numbers

AMD and Fujitsu continue to support existing part numbers beginning with "Am" and "MBM". To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information

Please contact your local AMD or Fujitsu sales office for additional information about SPANSION™ memory solutions.

PAGE MODE FLASH MEMORY

CMOS

16M (2M × 8/1M × 16) BIT

MBM29PL160TD/BD-75/90

■ DESCRIPTION

The MBM29PL160TD/BD is a 16 M-bit, 3.0 V-only Flash memory organized as 2 M bytes of 8 bits each or 1M words of 16 bits each. The MBM29PL160TD/BD is offered in a 48-pin TSOP (1), and 44-pin SOP packages. The device is designed to be programmed in-system with the standard system 3.0 V V_{CC} supply. 12.0 V V_{PP} and 5.0 V V_{CC} are not required for write or erase operations. The device can also be reprogrammed in standard EPROM programmers.

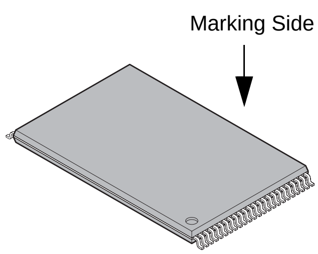
(Continued)

■ PRODUCT LINE UP

Part No.		MBM29PL160TD/160BD	
Ordering Part No.	$V_{CC} = 3.0\ V^{+0.6\ V}_{-0.3\ V}$	-75	-90
Max Address Access Time (ns)		75	90
Max Page Address Access Time (ns)		25	35
Max $\overline{CE}$ Access Time (ns)		75	90
Max $\overline{OE}$ Access Time (ns)		25	35

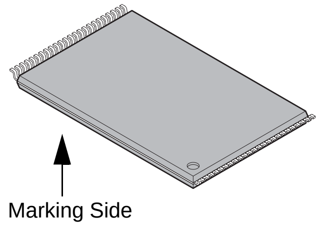
■ PACKAGES

48-pin plastic TSOP (1)



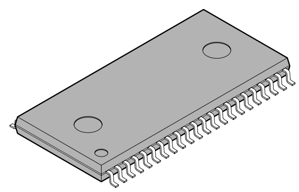
(FPT-48P-M19)

48-pin plastic TSOP (1)



(FPT-48P-M20)

44-pin plastic SOP



(FPT-44P-M16)

(Continued)

The standard MBM29PL160TD/BD offers access times of 75 ns and 90 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention the device has separate chip enable ($\overline{CE}$), write enable ($\overline{WE}$), and output enable ($\overline{OE}$) controls.

The MBM29PL160TD/BD is pin and command set compatible with JEDEC standard E^2PROMs. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 5.0 V and 12.0 V Flash or EPROM devices.

The MBM29PL160TD/BD is programmed by executing the program command sequence. This will invoke the Embedded Program Algorithm which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margins. Typically, each sector can be programmed and verified in about 2.0 seconds. Erase is accomplished by executing the erase command sequence. This will invoke the Embedded Erase Algorithm which is an internal algorithm that automatically preprograms the array if it is not already programmed before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margins.

Any individual sector is typically erased and verified in 4.8 second (If already preprogrammed).

The device also features a sector erase architecture. The sector mode allows each sector to be erased and reprogrammed without affecting other sectors. The MBM29PL160TD/BD is erased when shipped from the factory.

The device features single 3.0 V power supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations on the loss of power. The end of program or erase is detected by $\overline{\text{Data}}$ Polling of DQ_7 or by the Toggle Bit feature on DQ_6 output pin. Once the end of a program or erase cycle has been comleted, the device internally resets to the read mode.

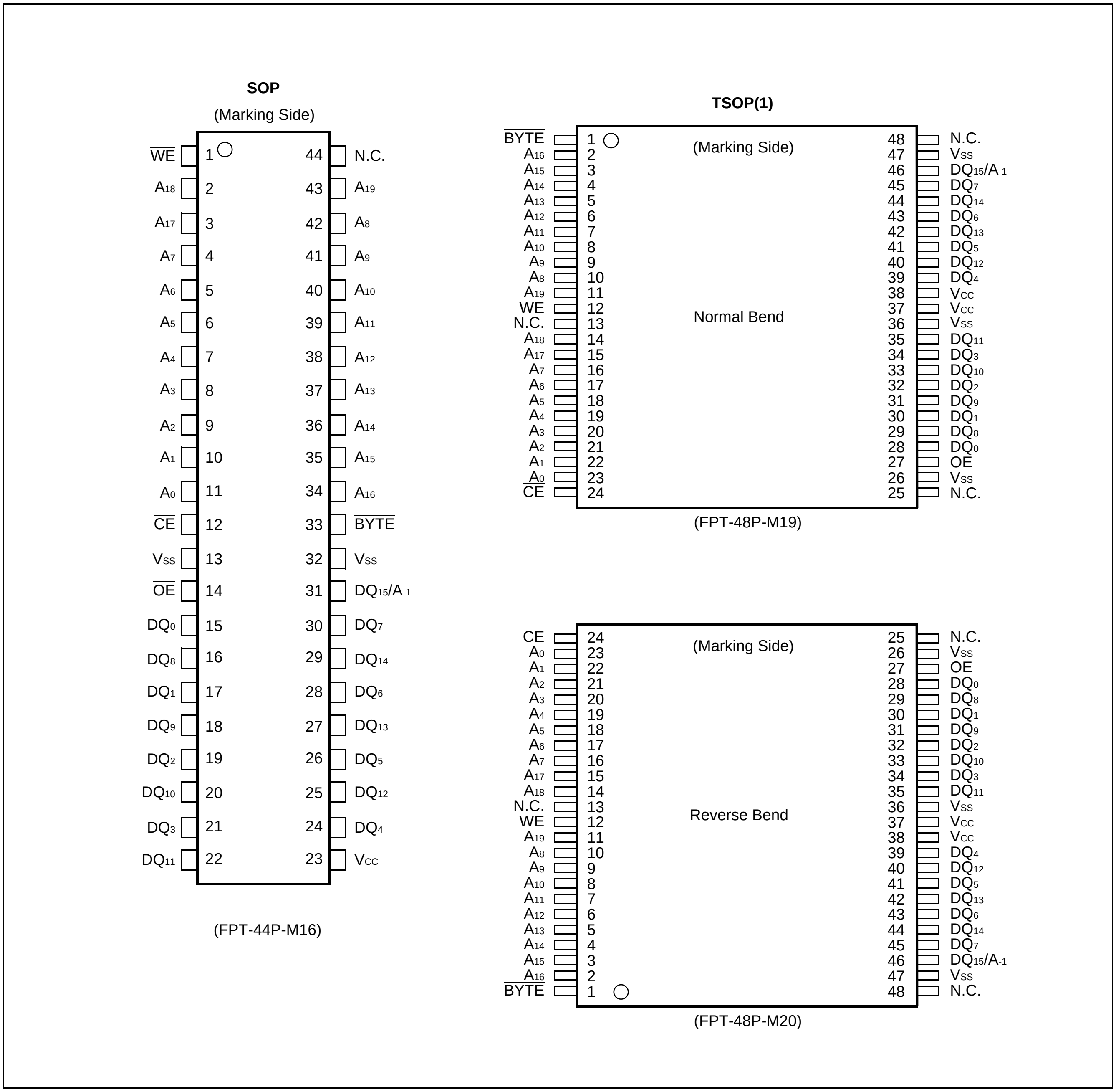
Fujitsu's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability, and cost effectiveness. The MBM29PL160TD/BD memory electrically erases all bits within a sector simultaneously via Fowler-Nordhiem tunneling. The bytes/words are programmed one byte/word at a time using the EPROM programming mechanism of hot electron injection.

■ FEATURES

- **Single 3.0 V read, program and erase**
  Minimizes system level power requirements
- **Compatible with JEDEC-standard commands**
  Uses same software commands as E^2PROMs
- **Compatible with MASK ROM pinouts**
  48-pin TSOP (1) (Package suffix: PFTN-Normal Bend Type, PFTR-Reversed Bend Type)
  44-pin SOP (Package suffix: PF)
- **Minimum 100,000 program/erase cycles**
- **High performance**
  25 ns maximum page access time (75 ns maximum random access time)
- **An 8 words page read mode function**
- **Sector erase architecture**
  One 8 K word, two 4 K words, one 112 K word, and seven 128 K words sectors in word mode
  One 16 K byte, two 8 K bytes, one 224 K byte, and seven 256 K bytes sectors in byte mode
  Any combination of sectors can be concurrently erased. Also supports full chip erase.
- **Boot Code Sector Architecture**
  T = Top sector
  B = Bottom sector
- **Embedded Erase™* Algorithms**
  Automatically pre-programs and erases the chip or any sector
- **Embedded program™* Algorithms**
  Automatically programs and verifies data at specified address
- **$\overline{\text{Data}}$ Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Ready/Busy output (RY/$\overline{\text{BY}}$)**
  Hardware method for detection of program or erase cycle completion
- **Automatic sleep mode**
  When addresses remain stable, automatically switches themselves to low power mode
- **Low V_{CC} write inhibit $\leq$ 2.5 V**
- **Erase Suspend/Resume**
  Suspends the erase operation to allow a read data and/or program in another sector within the same device
- **Sector protection**
  Hardware method disables any combination of sectors from program or erase operations
- **Temporary sector unprotection**
  Temporary sector unprotection with the software command
- **5 V tolerant (Data, Address, and Control Signals)**
- **In accordance with CFI (Common Flash Memory Interface)**

*: Embedded Erase™ and Embedded Program™ are trademarks of Advanced Micro Devices, Inc.

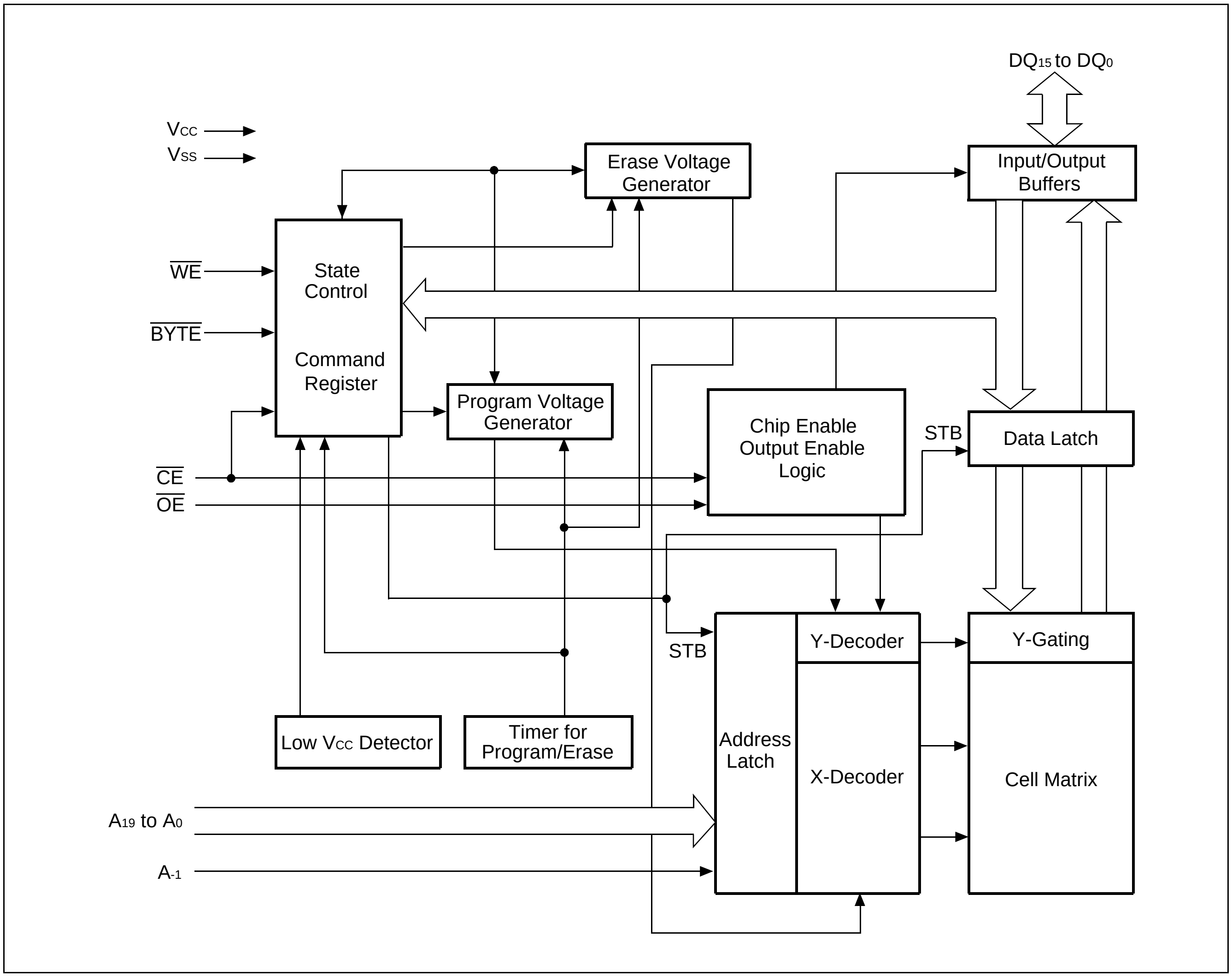
■ PIN ASSIGNMENTS



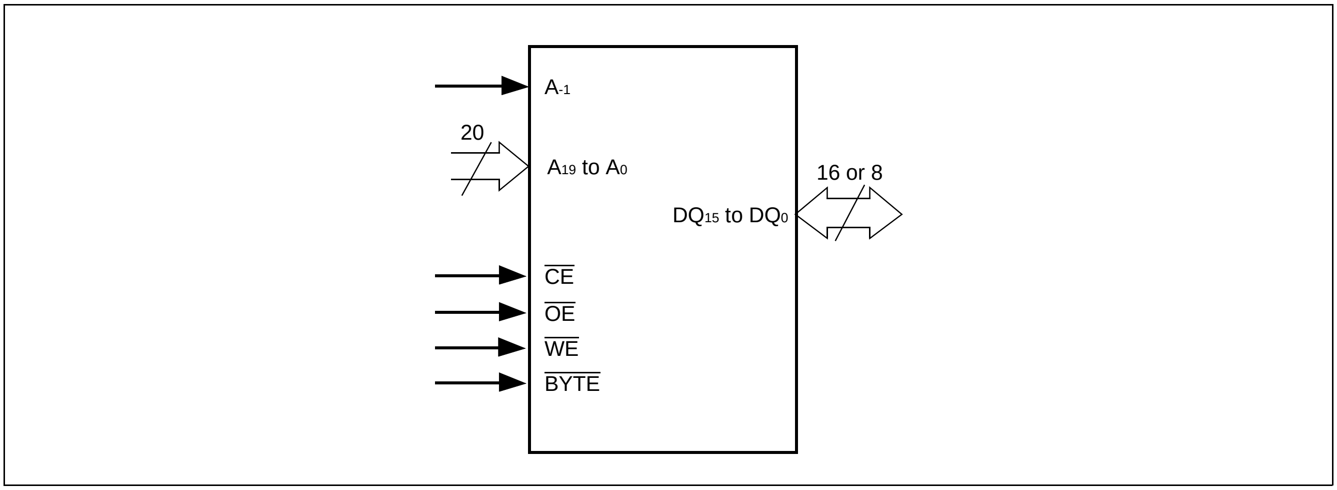
■ PIN DESCRIPTIONS

Pin name	Function
A_{19} to A_0, A_{-1}	Address Inputs
DQ_{15} to DQ_0	Data Inputs/Outputs
CE	Chip Enable
OE	Output Enable
WE	Write Enable
BYTE	Selects 8-bit or 16-bit mode
V_{SS}	Device Ground
V_{CC}	Device Power Supply (2.7 V to 3.6 V)
N.C.	Pin Not Connected Internally

■ BLOCK DIAGRAM



■ LOGIC SYMBOL



■ DEVICE BUS OPERATIONS

MBM29PL160TD/BD User Bus Operation Table ($\overline{BYTE}$ = V_{IH})

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A_0	A_1	A_6	A_9	DQ_{15} to DQ_0
Auto-Select Manufacture Code *1	L	L	H	L	L	L	V_{ID}	Code
Auto-Select Device Code *1	L	L	H	H	L	L	V_{ID}	Code
Read *3	L	L	H	A_0	A_1	A_6	A_9	D_{OUT}
Standby	H	X	X	X	X	X	X	High-Z
Output Disable	L	H	H	X	X	X	X	High-Z
Write (Program/Erase)	L	H	L	A_0	A_1	A_6	A_9	D_{IN}
Enable Sector Protection *2, *4	L	V_{ID}	$\sqcup$	L	H	L	V_{ID}	X
Verify Sector Protection *2, *4	L	L	H	L	H	L	V_{ID}	Code

Legend: L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}. $\sqcup$ = pulse input. See "■DC CHARACTERISTICS" for voltage levels.

*1: Manufacturer and device codes may also be accessed via a command register write sequence. See "MBM29PL160TD/BD Standard Command Definitions Table".

*2: Refer to the section on "Sector Protection" in ■FUNCTIONAL DESCRIPTION.

*3: $\overline{WE}$ can be V_{IL} if $\overline{OE}$ is V_{IL}, $\overline{OE}$ at V_{IH} initiates the write operations.

*4: V_{CC} = 3.3 V ±10%

MBM29PL160TD/BD User Bus Operation Table ($\overline{BYTE}$ = V_{IL})

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	DQ_{15}/ A_{-1}	A_0	A_1	A_6	A_9	DQ_7 to DQ_0
Auto-Select Manufacture Code *1	L	L	H	L	L	L	L	V_{ID}	Code
Auto-Select Device Code *1	L	L	H	L	H	L	L	V_{ID}	Code
Read *3	L	L	H	A_{-1}	A_0	A_1	A_6	A_9	D_{OUT}
Standby	H	X	X	X	X	X	X	X	High-Z
Output Disable	L	H	H	X	X	X	X	X	High-Z
Write (Program/Erase)	L	H	L	A_{-1}	A_0	A_1	A_6	A_9	D_{IN}
Enable Sector Protection *2, *4	L	V_{ID}	$\sqcup$	L	L	H	L	V_{ID}	X
Verify Sector Protection *2, *4	L	L	H	L	L	H	L	V_{ID}	Code

Legend: L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}. $\sqcup$ = pulse input. See "■DC CHARACTERISTICS" for voltage levels.

*1: Manufacturer and device codes may also be accessed via a command register write sequence. See "MBM29PL160TD/BD Standard Command Definitions Table".

*2: Refer to the section on "Sector Protection" in ■FUNCTIONAL DESCRIPTION.

*3: $\overline{WE}$ can be V_{IL} if $\overline{OE}$ is V_{IL}, $\overline{OE}$ at V_{IH} initiates the write operations.

*4: V_{CC} = 3.3 V ±10%

MBM29PL160TD/BD Standard Command Definitions Table

Command Sequence		Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read/Reset *1	Word /Byte	1	XXXh	F0h	—	—	—	—	—	—	—	—	—	—
Read/Reset *2	Word	3	555h	AAh	2AAh	55h	555h	F0h	RA*2	RD*2	—	—	—	—
	Byte		AAAh		555h		AAAh							
Autoselect	Word	3	555h	AAh	2AAh	55h	555h	90h	IA*2	ID*2	—	—	—	—
	Byte		AAAh		555h		AAAh							
Byte/Word Program	Word	4	555h	AAh	2AAh	55h	555h	A0h	PA	PD	—	—	—	—
	Byte		AAAh		555h		AAAh							
Chip Erase	Word	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	555h	10h
	Byte		AAAh		555h		AAAh		AAAh		555h		AAAh	
Sector Erase	Word	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	SA	30h
	Byte		AAAh		555h		AAAh		AAAh		555h			
Sector Erase Suspend	Erase can be suspended during sector erase with Addr (“H” or “L”), Data (B0h)													
Sector Erase Resume	Erase can be resumed after suspend with Addr (“H” or “L”), Data (30h)													
Temporary Unprotect Enable	Word	4	555h	AAh	2AAh	55h	555h	E0h	XXXh	01h	—	—	—	—
	Byte		AAAh		555h		AAAh							
Temporary Unprotect Dis-able	Word	4	555h	AAh	2AAh	55h	555h	E0h	XXXh	00h	—	—	—	—
	Byte		AAAh		555h		AAAh							

*1: Both Read/Reset commands are functionally equivalent, resetting the device to the read mode.

*2: The fourth bus cycle is only for read.

Notes :
- Address bits A_{19} to A_{11} = X = “H” or “L” for all address commands except or Program Address (PA) and Sector Address (SA).
- Bus operations are defined in "MBM29PL160TD/BD User Bus Operation Tables ($\overline{BYTE}$ = V_{IH} and $\overline{BYTE}$ = V_{IL})".
- RA = Address of the memory location to be read.
  IA = Autoselect read address that sets A_6, A_1, A_0.
  PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
  SA = Address of the sector to be erased. The combination of A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12} will uniquely select any sector.
- RD = Data read from location RA during read operation.
  ID = Device code/manufacture code for the address located by IA.
  PD = Data to be programmed at location PA. Data is latched on the rising edge of $\overline{WE}$.
- The system should generate the following address patterns:
  Word Mode: 555h or 2AAh to addresses A_{10} to A_0
  Byte Mode: AAAh or 555h to addresses A_{10} to A_{-1}
- The command combinations not described in “MBM29PL160TD/BD Standard Command Definitions Table” are illegal.

MBM29PL160TD/BD Extended Command Definitions Table

Command Sequence		Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read Cycle	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data
Set to Fast Mode	Word	3	555h	AAh	2AAh	55h	555h	20h	—	—
	Byte		AAAh		555h		AAAh			
Fast Program *1	Word	2	XXXh	A0h	PA	PD	—	—	—	—
	Byte		XXXh							
Reset from Fast Mode *1	Word	2	XXXh	90h	XXXh	F0h *3	—	—	—	—
	Byte		XXXh		XXXh					
Query Command *2	Word	2	55h	98h	—	—	—	—	—	—
	Byte		AAh							

*1: This command is valid during fast mode.

*2: Addresses from system set to A_6 to A_0. The other addresses are “Don’t care”.

*3: The data “00h” is also acceptable.

MBM29PL160TD/BD Sector Protection Verify Autoselect Code Table

Type			A_{19} to A_{12}	A_6	A_1	A_0	A_{-1}*1	Code (HEX)
Manufacture’s Code			X	V_{IL}	V_{IL}	V_{IL}	V_{IL}	04h
Device Code	MBM29PL160TD	Byte	X	V_{IL}	V_{IL}	V_{IH}	V_{IL}	27h
		Word					X	2227h
	MBM29PL160BD	Byte	X	V_{IL}	V_{IL}	V_{IH}	V_{IL}	45h
		Word					X	2245h
Sector Protection			Sector Addresses	V_{IL}	V_{IH}	V_{IL}	V_{IL}	01h*2
Temporary Sector Unprotection			X	V_{IL}	V_{IH}	V_{IH}	V_{IL}	01h*3

*1: A_{-1} is for Byte mode.

*2: Outputs 01h at protected sector addresses and outputs 00h at unprotected sector addresses.

*3: Outputs 01h at temporary sector unprotect and outputs 00h at non temporary sector unprotect.

Expanded Autoselect Code Table

Type			Code	DQ_{15}	DQ_{14}	DQ_{13}	DQ_{12}	DQ_{11}	DQ_{10}	DQ_{9}	DQ_{8}	DQ_{7}	DQ_{6}	DQ_{5}	DQ_{4}	DQ_{3}	DQ_{2}	DQ_{1}	DQ_{0}
Manufacture's Code*			04h	A_{-1}/0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
Device Code	MBM29PL160TD	(B)	27h	A_{-1}	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	0	0	1	0	0	1	1	1
		(W)	2227h	0	0	1	0	0	0	1	0	0	0	1	0	0	1	1	1
	MBM29PL160BD	(B)	45h	A_{-1}	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	0	1	0	0	0	1	0	1
		(W)	2245h	0	0	1	0	0	0	1	0	0	1	0	0	0	1	0	1
Sector Protection*			01h	A_{-1}/0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Temporary Sector Unprotection			01h	A_{-1}/0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

(B): Byte mode
(W): Word mode
HI-Z: High-Z

* : In byte mode, DQ_{15} to DQ_{8} are High-Z and DQ_{15} is A_{-1}, the lowest address.

■ FLEXIBLE SECTOR-ERASE ARCHITECTURE

- One 8 K word, two 4 K words, one 112 K word, and seven 128 K words sectors in word mode.
- One 16 K byte, two 8 K bytes, one 224 K byte, and seven 256 K bytes sectors in byte mode.
- Individual-sector, multiple-sector, or bulk-erase capability.
- Individual or multiple-sector protection is user definable.

MBM29PL160TD Top Boot Sector Architecture

Sector	Sector Size	(× 8) Address Range	(× 16) Address Range
SA0	256 Kbytes or 128 Kwords	000000h to 03FFFFh	00000h to 1FFFFh
SA1	256 Kbytes or 128 Kwords	040000h to 07FFFFh	20000h to 3FFFFh
SA2	256 Kbytes or 128 Kwords	080000h to 0BFFFFh	40000h to 5FFFFh
SA3	256 Kbytes or 128 Kwords	0C0000h to 0FFFFFh	60000h to 7FFFFh
SA4	256 Kbytes or 128 Kwords	100000h to 13FFFFh	80000h to 9FFFFh
SA5	256 Kbytes or 128 Kwords	140000h to 16FFFFh	A0000h to BFFFFh
SA6	256 Kbytes or 128 Kwords	180000h to 1BFFFFh	C0000h to DFFFFh
SA7	224 Kbytes or 112 Kwords	1C0000h to 1F7FFFh	E0000h to FBFFFh
SA8	8 Kbytes or 4 Kwords	1F8000h to 1F9FFFh	FC000h to FCFFFh
SA9	8 Kbytes or 4 Kwords	1FA000h to 1FBFFFh	FD000h to FDFFFh
SA10	16 Kbytes or 8 Kwords	1FC000h to 1FFFFFh	FE000h to FFFFFh

MBM29PL160BD Bottom Boot Sector Architecture

Sector	Sector Size	(× 8) Address Range	(× 16) Address Range
SA0	16 Kbytes or 8 Kwords	000000h to 003FFFh	00000h to 01FFFh
SA1	8 Kbytes or 4 Kwords	004000h to 005FFFh	02000h to 02FFFh
SA2	8 Kbytes or 4 Kwords	006000h to 007FFFh	03000h to 03FFFh
SA3	224 Kbytes or 112 Kwords	008000h to 03FFFFh	04000h to 1FFFFh
SA4	256 Kbytes or 128 Kwords	040000h to 07FFFFh	20000h to 3FFFFh
SA5	256 Kbytes or 128 Kwords	080000h to 0BFFFFh	40000h to 5FFFFh
SA6	256 Kbytes or 128 Kwords	0C0000h to 0FFFFFh	60000h to 7FFFFh
SA7	256 Kbytes or 128 Kwords	100000h to 13FFFFh	80000h to 9FFFFh
SA8	256 Kbytes or 128 Kwords	140000h to 17FFFFh	A0000h to BFFFFh
SA9	256 Kbytes or 128 Kwords	180000h to 1BFFFFh	C0000h to DFFFFh
SA10	256 Kbytes or 128 Kwords	1C0000h to 1FFFFFh	E0000h to FFFFFh

Sector Address Table (MBM29PL160TD)

Sector Address	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	(× 8) Address Range	(× 16) Address Range
SA0	0	0	0	X	X	X	X	X	000000h to 03FFFFh	00000h to 1FFFFh
SA1	0	0	1	X	X	X	X	X	040000h to 07FFFFh	20000h to 3FFFFh
SA2	0	1	0	X	X	X	X	X	080000h to 0BFFFFh	40000h to 5FFFFh
SA3	0	1	1	X	X	X	X	X	0C0000h to 0FFFFFh	60000h to 7FFFFh
SA4	1	0	0	X	X	X	X	X	100000h to 13FFFFh	80000h to 9FFFFh
SA5	1	0	1	X	X	X	X	X	140000h to 16FFFFh	A0000h to BFFFFh
SA6	1	1	0	X	X	X	X	X	180000h to 1BFFFFh	C0000h to DFFFFh
SA7	1	1	1	00000 - 11011					1C0000h to 1F7FFFh	E0000h to FBFFFh
SA8	1	1	1	1	1	1	0	0	1F8000h to 1F9FFFh	FC000h to FCFFFh
SA9	1	1	1	1	1	1	0	1	1FA000h to 1FBFFFh	FD000h to FDFFFh
SA10	1	1	1	1	1	1	1	X	1FC000h to 1FFFFFh	FE000h to FFFFFh

Sector Address Table (MBM29PL160BD)

Sector Address	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	(× 8) Address Range	(× 16) Address Range
SA0	0	0	0	0	0	0	0	X	000000h to 003FFFh	00000h to 01FFFh
SA1	0	0	0	0	0	0	1	0	004000h to 005FFFh	02000h to 02FFFh
SA2	0	0	0	0	0	0	1	1	006000h to 007FFFh	03000h to 03FFFh
SA3	0	0	0	00100 - 11111					008000h to 03FFFFh	04000h to 1FFFFh
SA4	0	0	1	X	X	X	X	X	040000h to 07FFFFh	20000h to 3FFFFh
SA5	0	1	0	X	X	X	X	X	080000h to 0BFFFFh	40000h to 5FFFFh
SA6	0	1	1	X	X	X	X	X	0C0000h to 0FFFFFh	60000h to 7FFFFh
SA7	1	0	0	X	X	X	X	X	100000h to 13FFFFh	80000h to 9FFFFh
SA8	1	0	1	X	X	X	X	X	140000h to 17FFFFh	A0000h to BFFFFh
SA9	1	1	0	X	X	X	X	X	180000h to 1BFFFFh	C0000h to DFFFFh
SA10	1	1	1	X	X	X	X	X	1C0000h to 1FFFFFh	E0000h to FFFFFh

Common Flash Memory Interface Code Table

Description	A_0 to A_6	DQ_{15} to DQ_0
Query-unique ASCII string "QRY"	10h 11h 12h	0051h 0052h 0059h
Primary OEM Command Set 2h : AMD/FJ standard type	13h 14h	0002h 0000h
Address for Primary Extended Table	15h 16h	0040h 0000h
Alternate OEM Command Set (00h = not applicable)	17h 18h	0000h 0000h
Address for Alternate OEM Extended Table	19h 1Ah	0000h 0000h
V_{CC} Min (write/erase) DQ_7 to DQ_4 : 1 V, DQ_3 to DQ_0 : 100 mV	1Bh	0027h
V_{CC} Max (write/erase) DQ_7 to DQ_4 : 1 V, DQ_3 to DQ_0 : 100 mV	1Ch	0036h
V_{PP} Min voltage	1Dh	0000h
V_{PP} Max voltage	1Eh	0000h
Typical timeout per single byte/word write 2^N µs	1Fh	0004h
Typical timeout for Min size buffer write 2^N µs	20h	0000h
Typical timeout per individual block erase 2^N ms	21h	000Ah
Typical timeout for full chip erase 2^N ms	22h	0000h
Max timeout for byte/word write 2^N times typical	23h	0005h
Max timeout for buffer write 2^N times typical	24h	0000h
Max timeout per individual block erase 2^N times typical	25h	0004h
Max timeout for full chip erase 2^N times typical	26h	0000h
Device Size = 2^N byte	27h	0015h
Flash Device Interface description	28h 29h	0002h 0000h
Max number of byte in multi-byte write = 2^N	2Ah 2Bh	0000h 0000h
Number of Erase Block Regions within device	2Ch	0004h

Description	A_0 to A_6	DQ_{15} to DQ_0
Erase Block Region 1 Information	2Dh 2Eh 2Fh 30h	0000h 0000h 0040h 0000h
Erase Block Region 2 Information	31h 32h 33h 34h	0001h 0000h 0020h 0000h
Erase Block Region 3 Information	35h 36h 37h 38h	0000h 0000h 0080h 0003h
Erase Block Region 4 Information	39h 3Ah 3Bh 3Ch	0006h 0000h 0000h 0004h
Query-unique ASCII string "PRI"	40h 41h 42h	0050h 0052h 0049h
Major version number, ASCII	43h	0031h
Minor version number, ASCII	44h	0030h
Address Sensitive Unlock 0 = Required 1 = Not Required	45h	0000h
Erase Suspend 0 = Not Supported 1 = To Read Only 2 = To Read & Write	46h	0002h
Sector Protect 0 = Not Supported X = Number of sectors in per group	47h	0001h
Sector Temporary Unprotect 00 = Not Supported 01 = Supported	48h	0001h
Sector Protection Algorithm	49h	0004h
Number of Sector for Bank 2	4Ah	00h
Burst Mode Type 00 = Not supported	4Bh	00h
Page Mode Type 00 = Not supported 01 = 4 word Page 02 = 8 word Page	4Ch	02h

■ FUNCTIONAL DESCRIPTION

Random Read Mode

The MBM29PL160TD/BD has two control functions which must be satisfied in order to obtain data at the outputs. $\overline{CE}$ is the power control and should be used for a device selection. $\overline{OE}$ is the output control and should be used to gate data to the output pins if a device is selected.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins (Assuming the addresses have been stable for at least t_{ACC} - t_{OE} time). See "(1) AC Waveforms for Read Operations" in ■TIMING DIAGRAM for timing specifications. When reading out a data without changing addresses after powe-up, it is necessary to input hardware reset or to change $\overline{CE}$ pin from "H" to "L".

Page Read Mode

The MBM29PL160TD/BD is capable of fast Page read mode and is compatible with the Page mode MASK ROM read operation. This mode provides faster read access speed for random locations within a page. The Page size of the MBM29PL160TD/BD device is 8 words, or 16 bytes, within the appropriate Page being selected by the higheraddress bits A_2 to A_0 (in the word mode) and A_2 to A_{-1} (in the byte mode) determining the specific word/ byte within that page. This is an asynchronous operation with the microprocessor supplying the specific word or byte location.

The rondom or initial page access is equal to t_{ACC} and subsequent Page read access (as long as the locations specified by the microprocessor fall within that Page) is equivalent to t_{PACC}. Here again, $\overline{CE}$ selects the device and $\overline{OE}$ is the output control and should be used to gate data to the output pins if the device is selected. Fast Page mode accesses are obtained by keeping A_{19} to A_3 constant and changing A_2 to A_0 to select the specific word, or changing A_2 to A_{-1} to select the specific byte, within that page. See "(2) AC Waveforms for Page Read Mode Operations" in ■TIMING DIAGRAM for timing specifications.

Standby Mode

The MBM29PL160TD/BD has a standby mode, a CMOS standby mode ($\overline{CE}$ input held at V_{CC} ±0.3 V.), when the current consumed is less than 50 µA. During Embedded Algorithm operation, V_{CC} Active current (I_{CC2}) is required even $\overline{CE}$ = “H”. The device can be read with standard access time (t_{CE}) from standby modes.

In the standby mode, the outputs are in the high-impedance state, independent of the $\overline{OE}$ input. If the device is deselected during erasure or programming, the device will draw active current until the operation is completed.

Automatic Sleep Mode

There is a function called automatic sleep mode to restrain power consumption during read-out of MBM29PL160TD/BD data. This mode can be used effectively with an application requesting low power consumption such as handy terminals.

To activate this mode, MBM29PL160TD/BD automatically switches itself to low power mode when addresses remain stable for 150 ns. It is not necessary to control $\overline{CE}$, $\overline{WE}$, and $\overline{OE}$ in this mode. During such mode, the current consumed is typically 50 µA (CMOS Level).

Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system.

Output Disable

If the $\overline{OE}$ input is at a logic high level (V_{IH}), output from the device is disabled. This will cause the output pins to be in a High-Z state.

Autoselect

The Autoselect mode allows the reading out of a binary code from the device and will identify its manufacturer and type. The intent is to allow programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. The Autoselect command may also be used to check the status of write-protected sectors (See "MBM29PL160TD/BD Sector Protection Verify Autoselect Code Table" and "Expanded Autoselect Code Table" in ■DEVICE BUS OPERATIONS). This mode is functional over the entire temperature range of the device.

To activate this mode, the programming equipment must force V_{ID} (11.5 V to 12.5 V) on address pin A_9. Two identifier bytes may then be sequenced from the devices outputs by toggling address A_0 from V_{IL} to V_{IH}. All addresses are DON’T CARES except A_0, A_1, and A_6 (A_{-1}). (See "MBM29PL160TD/BD User Bus Operation Table ($\overline{BYTE}$ = V_{IH} or $\overline{BYTE}$ = V_{IL})" in ■DEVICE BUS OPERATIONS.) (Recommend to set VIL for the other addresses pins.)

The manufacturer and device codes may also be read via the command register, for instances when the MBM29PL160TD/BD is erased or programmed in a system without access to high voltage on the A_9 pin. The command sequence is illustrated in "MBM29PL160TD/BD Standard Command Definitions Table" in ■DEVICE BUS OPERATIONS (see “Autoselect Command” in ■COMMAND DEFINITIONS.

Word 0 (A_0 = V_{IL}) represents the manufacture’s code and word 1 (A_0 = V_{IH}) represents the device identifier code. For the MBM29PL160TD/BD these two bytes are given in "Expanded Autoselect Code Table" (■DEVICE BUS OPERATIONS). All identifiers for manufactures and device will exhibit odd parity with DQ_7 defined as the parity bit. In order to read the proper device codes when executing the Autoselect, A_1 must be V_{IL}. (See "MBM29PL160TD/BD User Bus Operation Table ($\overline{BYTE}$ = V_{IH} or $\overline{BYTE}$ = V_{IL})" in ■DEVICE BUS OPERATIONS.)

If $\overline{BYTE}$ = V_{IL} (for byte mode), the device code is 27h (for top boot block) or 45h (for bottom boot block). If $\overline{BYTE}$ = V_{IH} (for word mode), the device code is 2227h (for top boot block) or 2245h (for bottom boot block).

In order to determine which sectors are write protected, A_1 must be at V_{IH} while running through the sector addresses; if the selected sector is protected, a logical ‘1’ will be output on DQ_0 (DQ_0 =1).

Write

Device erasure and programming are accomplished via the command register. The command register is written by bringing $\overline{WE}$ to V_{IL}, while $\overline{CE}$ is at V_{IL} and $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs later, while data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$ pulse, whichever occurs first. Standard microprocessor write timings are used. See "(3) AC Waveforms for Alternate $\overline{WE}$ Controlled Program Operations", "(4) AC Waveforms for Alternate $\overline{CE}$ Controlled Program Operations", and "(5) AC Waveforms for Chip/Sector Erase Operations" in ■TIMING DIAGRAM.

Refer to ■AC CHARACTERISTICS and ■TIMING DIAGRAM for specific timing parameters.

Sector Protection

The MBM29PL160TD/BD features hardware sector protection. This feature will disable both program and erase operations in any number of sectors (0 through 10). The sector protection feature is enabled using programming equipment at the user’s site. The device is shipped with all sectors unprotected.

To activate this mode, the programming equipment must force V_{ID} on address pin A_9 and control pin $\overline{OE}$, $\overline{CE}$ = V_{IL}, A_0 = A_6 = V_{IL}, A_1 = V_{IH}. The sector addresses pins (A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12}) should be set to the sector to be protected. "Sector Address Table (MBM29PL160TD)" and "Sector Address Table (MBM29PL160BD)" in ■FLEXIBLE SECTOR-ERASE ARCHITECTURE define the sector address for each of the eleven (11) individual sectors. Programming of the protection circuitry begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same. Sector addresses must be held constant during the $\overline{WE}$ pulse. See "(11) AC Waveforms for Sector Protection Timing Diagram" in ■TIMING DIAGRAM and "(5) Sector Protection Algorithm" in ■FLOW CHART for sector protection waveforms and algorithm.

To verify programming of the protection circuitry, the programming equipment must force V_{ID} on address pin A_9 with $\overline{CE}$ and $\overline{OE}$ at V_{IL} and $\overline{WE}$ at V_{IH}. Scanning the sector addresses (A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12})

while (A_6, A_1, A_0) = (0, 1, 0) will produce a logical “1” at device output DQ_0 for a protected sector. Otherwise the device will read 00h for an unprotected sector. In this mode, the lower order addresses, except for A_0, A_1, and A_6 are DON’T CARES. Address locations with $A_1 = V_{IL}$ are reserved for Autoselect manufacturer and device codes. A_{-1} requires to V_{IL} in byte mode.

It is also possible to determine if a sector is protected in the system by writing an Autoselect command. Performing a read operation at the address location XX02h, where the higher order addresses pins (A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12}) represents the sector address will produce a logical “1” at DQ_0 for a protected sector. See "MBM29PL160TD/BD Sector Protection Verify Autoselect Code Table" and "Expanded Autoselect Code Table" in ■DEVICE BUS OPERATIONS for Autoselect codes.

Word/Byte Configuration

The $\overline{\text{BYTE}}$ pin selects the byte (8-bit) mode or word (16-bit) mode for the MBM29PL160TD/BD device. When this pin is driven high, the device operates in the word (16-bit) mode. The data is read and programmed at DQ_{15} to DQ_0. When this pin is driven low, the device operates in byte (8-bit) mode. Under this mode, DQ_{15}/A_{-1} pin becomes the lowest address bit and DQ_{14} to DQ_8 bits are High-Z. However, the command bus cycle is always an 8-bit operation and hence commands are written at DQ_7 to DQ_0 and DQ_{15} to DQ_8 bits are ignored. Refer to "(8) Timing Diagram for Word Mode Configuration", "(9) Timing Diagram for Byte Mode Configuration", and "(10) $\overline{\text{BYTE}}$ Timing Diagram for Write Operations" in ■TIMING DIAGRAM for the timing diagrams.

■ COMMAND DEFINITIONS

Device operations are selected by writing specific address and data sequences into the command register. Writing incorrect address and data values or writing them in an improper sequence will reset the device to the read mode. "MBM29PL160TD/BD Standard Command Definitions Table" in ■DEVICE BUS OPERATIONS defines the valid register command sequences. Note that the Erase Suspend (B0h) and Erase Resume (30h) commands are valid only while the Sector Erase operation is in progress. Moreover both Read/Reset commands are functionally equivalent, resetting the device to the read mode. Please note that commands are always written at DQ_7 to DQ_0 and DQ_{15} to DQ_8 bits are ignored.

Read/Reset Command

In order to return from Autoselect mode or Exceeded Timing Limits (DQ_5 = 1) to read mode, the read/reset operation is initiated by writing the Read/Reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The device remains enabled for reads until the command register contents are altered.

The device will automatically power-up in the Read/Reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory contents occurs during the power transition. Refer to “Read Only Operations Characteristics” in ■AC CHARACTRISTICS and ■TIMING DIAGRAM for specific timing parameters. (See "(1) AC Waveforms for Read Operations" and “(2) AC Waveforms for Page Read Mode Operations” in ■TIMING DIAGRAM.)

Autoselect Command

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufactures and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A_9 to a high voltage. However, multiplexing high voltage onto the address lines is not generally desired system design practice.

The device contains an Autoselect command operation to supplement traditional PROM programming methodology. The operation is initiated by writing the Autoselect command sequence into the command register. Following the last command write, a read cycle from address XX00h retrieves the manufacture code of 04h. A read cycle from address XX01h for ×16 (XX02h for ×8) retrieves the device code (MBM29PL160TD = 27h and MBM29PL160BD = 45h for ×8 mode; MBM29PL160TD = 2227h and MBM29PL160BD = 2245h for ×16 mode). (See "MBM29PL160TD/BD Sector Protection Verify Autoselect Code Table" and "Expanded Autoselect Code Table" in ■DEVICE BUS OPERATIONS.)

All manufactures and device codes will exhibit odd parity with DQ_7 defined as the parity bit.
The sector state (protection or unprotection) will be indicated by address XX02h for ×16 (XX04h for ×8). Scanning the sector addresses (A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12}) while (A_6, A_1, A_0) = (0, 1, 0) will produce a logical “1” at device output DQ_0 for a protected sector. The programming verification should be perform margin mode verification on the protected sector. (See "MBM29PL160TD/BD User Bus Operation Tables ($\overline{BYTE}$ = V_{IH} and $\overline{BYTE}$ = V_{IL})" in ■DEVICE BUS OPERATIONS.)

To terminate the operation, it is necessary to write the Read/Reset command sequence into the register, and also to write the Autoselect command during the operation, by executing it after writing the Read/Reset command sequence.

Word/Byte Programming

The device is programmed on a byte-by-byte (or word-by-word) basis. Programming is a four bus cycle operation. There are two “unlock” write cycles. These are followed by the program set-up command and data write cycles. Addresses are latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever happens later and the data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever happens first. The rising edge of the last $\overline{CE}$ or $\overline{WE}$ (whichever happens first) begins programming. Upon executing the Embedded Program Algorithm command sequence, the system is not required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin. (See "(3) AC Waveforms for Alternate $\overline{WE}$

Controlled Program Operations" and "(4) AC Waveforms for Alternate $\overline{CE}$ Controlled Program Operations" in ■TIMING DIAGRAM.)

The automatic programming operation is completed when the data on DQ_7 is equivalent to data written to this bit at which time the device return to the read mode and addresses are no longer latched. (See "Hardware Sequence Flags Table".) Therefore, the device requires that a valid address be supplied by the system at this time. Hence, $\overline{\text{Data}}$ Polling must be performed at the memory location which is being programmed.

Any commands written to the chip during this period will be ignored. If hardware reset occures during the programming operation, it is impossible to guarantee whether the data being written is correct or not.

Programming is allowed in any sequence and across sector boundaries. Beware that a data “0” cannot be programmed back to a “1”. Attempting to do so may either hang up the device or result in an apparent success according to the data polling algorithm but a read from read/reset mode will show that the data is still “0”. Only erase operations can convert “0”s to “1”s.

"(1) Embedded Program™ Algorithm" in ■FLOW CHART illustrates the Embedded Program™ Algorithm using typical command strings and bus operations.

Chip Erase

Chip erase is a six-bus cycle operation. There are two “unlock” write cycles. These are followed by writing the “set-up” command. Two more “unlock” write cycles are then followed by the chip erase command.

Chip erase does not require the user to program the device prior to erase. Upon executing the Embedded Erase Algorithm command sequence the device will automatically program and verify the entire memory for an all zero data pattern prior to electrical erase. (Preprogram Function.) The system is not required to provide any controls or timings during these operations.

The automatic erase begins on the rising edge of the last $\overline{WE}$ or $\overline{OE}$ pulse in the command sequence and terminates when the data on DQ_7 is “1” (See “Write Operation Status” section.) at which time the device returns to read mode. (See "(5) AC Waveforms for Chip/Sector Erase Operations" in ■TIMING DIAGRAM.)

"(2) Embedded Erase™ Algorithm" in ■FLOW CHART illustrates the Embedded Erase™ Algorithm using typical command strings and bus operations.

Sector Erase

Sector erase is a six-bus cycle operation. There are two “unlock” write cycles, followed by writing the “set-up” command. Two more “unlock” write cycles are then followed by the Sector Erase command. The sector address (any address location within the desired sector) is latched on the falling edge of $\overline{WE}$, while the command (Data = 30h) is latched on the rising edge of $\overline{WE}$. After a time-out of 50 μs from the rising edge of the last sector erase command, the sector erase operation will begin.

Multiple sectors may be erased concurrently by writing six-bus cycle operations on "MBM29PL160TD/BD Standard Command Definitions Table" in ■DEVICE BUS OPERATIONS. This sequence is followed with writes of the Sector Erase command to addresses in other sectors desired to be concurrently erased. The time between writes must be less than 50 μs otherwise that command will not be accepted and erasure will start. It is recommended that processor interrupts be disabled during this time to guarantee this condition. The interrupts can be re-enabled after the last Sector Erase command is written. A time-out of 50 μs from the rising edge of the last $\overline{WE}$ will initiate the execution of the Sector Erase command(s). If another falling edge of the $\overline{WE}$ occurs within the 50 μs time-out window the timer is reset. Monitor DQ_3 to determine if the sector erase timer window is still open. (See section “DQ_3, Sector Erase Timer”.) Any command other than Sector Erase or Erase Suspend during this time-out period will reset the device to the read mode, ignoring the previous command string. Resetting the device once excution has begun will corrupt the data in the sector. In that case, restart the erase on those sectors and allow them to complete. (Refer to “Write Operation Status” section for Sector Erase Timer operation.) Loading the sector erase buffer may be done in any sequence and with any number of sectors (0 to 10).

Sector erase does not require the user to program the device prior to erase. The device automatically programs all memory locations in the sector(s) to be erased prior to electrical erase (Preprogram Function). When erasing a sector or sectors the remaining unselected sectors are not affected. The system is not required to provide any controls or timings during these operations. (See "(5) AC Waveforms for Chip/Sector Erase Operations" in ■TIMING DIAGRAM.)

The automatic sector erase begins after the 50 μs time out from the rising edge of the $\overline{WE}$ or $\overline{OE}$ pulse for the last sector erase command pulse and terminates when the data on DQ_7 is “1” (See “Write Operation Status” section) at which time the device returns to the read mode. $\overline{Data}$ polling must be performed at an address within any of the sectors being erased. Multiple Sector Erase Time; [Sector Program Time (Preprogramming) + Sector Erase Time] × Number of Sector Erase.

"(2) Embedded Erase™ Algorithm" in ■FLOW CHART illustrates the Embedded Erase™ Algorithm using typical command strings and bus operations.

Erase Suspend

The Erase Suspend command allows the user to interrupt a Sector Erase operation and then perform data reads from or program to a sector not being erased. This command is applicable ONLY during the Sector Erase operation which includes the time-out period for sector erase. The Erase Suspend command will be ignored if written during the Chip Erase operation or Embedded Program Algorithm. Writting the Erase Suspend command during the Sector Erase time-out results in immediate termination of the time-out period and suspension of the erase operation.

Writing the Erase Resume command resumes the erase operation. The addresses are “DON’T CARES” when writing the Erase Suspend or Erase Resume commands.

When the Erase Suspend command is written during the Sector Erase operation, the device will take a maximum of 20 μs to suspend the erase operation. When the devices have entered the erase-suspended mode, the DQ_7 bit will be at logic “1”, and DQ_6 will stop toggling. The user must use the address of the erasing sector for reading DQ_6 and DQ_7 to determine if the erase operation has been suspended. Further writes of the Erase Suspend command are ignored.

When the erase operation has been suspended, the device defaults to the erase-suspend-read mode. Reading data in this mode is the same as reading from the standard read mode except that the data must be read from sectors that have not been erase-suspended. Successively reading from the erase-suspended sector while the device is in the erase-suspend-read mode will cause DQ_2 to toggle. (See the section on “DQ_2”.)

After entering the erase-suspend-read mode, the user can program the device by writing the appropriate command sequence for Program. This Program mode is known as the erase-suspend-program mode. Again, programming in this mode is the same as programming in the regular Program mode except that the data must be programmed to sectors that are not erase-suspended. Successively reading from the erase-suspended sector while the devices are in the erase-suspend-program mode will cause DQ_2 to toggle. The end of the erase-suspended Program operation is detected by the Toggle Bit (DQ_6) which is the same as the regular Program operation. Note that DQ_7 must be read from the Program address while DQ_6 can be read from any address.

To resume the operation of Sector Erase, the Resume command (30h) should be written. Any further writes of the Resume command at this point will be ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

Extended Command

(1) Fast Mode

MBM29PL160TD/BD has Fast Mode function. This mode dispenses with the initial two unlock cycles required in the standard program command sequence writing Fast Mode command into the command register. In this mode, the required bus cycle for programming is two cycles instead of four bus cycles in standard program command. In Fast Mode, do not write any command other than the fast program/fast mode reset command. The read operation is also executed after exiting this mode. To exit this mode, it is necessary to write Fast Mode Reset command into the command register. (Refer to "(7) Embedded Programming Algorithm for Fast Mode" in ■FLOW CHART Extended algorithm.) The V_{CC} active current is required even $\overline{CE}$ = V_{IH} during Fast Mode.

(2) Fast Programming

During Fast Mode, the programming can be executed with two bus cycles operation. The Embedded Program Algorithm is executed by writing program set-up command (A0h) and data write cycles (PA/PD). (Refer to "(7) Embedded Programming Algorithm for Fast Mode" in ■FLOW CHART.)

(3) Temporary Sector Unprotection

This feature allows temporary unprotection of previously protected sectors of the MBM29PL160TD/BD devices in order to change data. The Temporary Sector Unprotection mode is activated by command register. During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once the mode is taken away using command register, all the previously protected sectors will be protected again. (See "(5) Sector Protection Algorithm" in ■FLOW CHART.)

Write Operation Status

Hardware Sequence Flags Table

Status			DQ_7	DQ_6	DQ_5	DQ_3	DQ_2
In Progress	Embedded Program Algorithm		$\overline{DQ_7}$	Toggle	0	0	1
	Embedded/Erase Algorithm		0	Toggle	0	1	Toggle
	Erase Suspend Mode	Erase Suspend Read (Erase Suspended Sector)	1	1	0	0	Toggle
		Erase Suspend Read (Non-Erase Suspended Sector)	Data	Data	Data	Data	Data
		Erase Suspend Program (Non-Erase Suspended Sector)	$\overline{DQ_7}$	Toggle *1	0	0	1 *2
Exceeded Time Limits	Embedded Program Algorithm		$\overline{DQ_7}$	Toggle	1	0	1
	Embedded/Erase Algorithm		0	Toggle	1	1	N/A
	Erase Suspend Program		$\overline{DQ_7}$	Toggle	1	0	N/A

*1: Performing successive read operations from any address will cause DQ_6 to toggle.

*2: Reading the byte address being programmed while in the erase-suspend program mode will indicate logic “1” at the DQ_2 bit. However, successive reads from the erase-suspended sector will cause DQ_2 to toggle.

Notes: • DQ_{15} to DQ_8 for ×16 are optional.
• DQ_0 and DQ_1 are reserve pins for future use.
• DQ_4 is Fujitsu internal use only.

DQ_7

$\overline{\text{Data}}$ Polling

The MBM29PL160TD/BD device features $\overline{\text{Data}}$ Polling as a method to indicate to the host that the Embedded Algorithms are in progress or completed. During the Embedded Program Algorithm, an attempt to read the devices will produce the complement of the data last written to DQ_7. Upon completion of the Embedded Program Algorithm, an attempt to read the device will produce the true data last written to DQ_7. During the Embedded Erase Algorithm, an attempt to read the device will produce a “0” at the DQ_7 output. Upon completion of the Embedded Erase Algorithm an attempt to read the device will produce a “1” at the DQ_7 output. The flowchart for $\overline{\text{Data}}$ Polling (DQ_7) is shown in "(3) $\overline{\text{Data}}$ Polling Algorithm" (■FLOW CHART).

For chip erase and sector erase, $\overline{\text{Data}}$ Polling is valid after the rising edge of the sixth $\overline{\text{WE}}$ pulse in the six-write pulse sequence. $\overline{\text{Data}}$ Polling must be performed at a sector address within any of the sectors being erased and not at a protected sector. Otherwise, the status may not be valid. Once the Embedded Algorithm operation is close to being completed, the MBM29PL160TD/BD data pins (DQ_7) may change asynchronously while the output enable ($\overline{\text{OE}}$) is asserted low. This means that the device is driving status information on DQ_7 at one instant of time and then that byte’s valid data at the next instant of time. Depending on when the system samples the DQ_7 output, it may read the status or valid data. Even if the device has completed the Embedded Program Algorithm operation and DQ_7 has a valid data, the data outputs on DQ_6 to DQ_0 may be still invalid. The valid data on DQ_7 to DQ_0 will be read on successive read attempts.

The $\overline{\text{Data}}$ Polling feature is only active during the Embedded Programming Algorithm, Embedded Erase Algorithm or sector erase time-out.

See "(6) AC Waveforms for $\overline{\text{Data}}$ Polling during Embedded Algorithm Operations" in ■TIMING DIAGRAM for the $\overline{\text{Data}}$ Polling timing specifications and diagrams.

DQ_6

Toggle Bit I

The MBM29PL160TD/BD also feature the “Toggle Bit I” as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.

During an Embedded Program or Erase Algorithm cycle, successive attempts to read ($\overline{\text{OE}}$ toggling) data from the device will result in DQ_6 toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, DQ_6 will stop toggling and valid data can be read on the next successive attempts. During programming, the Toggle Bit I is valid after the rising edge of the fourth $\overline{\text{WE}}$ pulse in the four write pulse sequence. For chip erase and sector erase, the Toggle Bit I is valid after the rising edge of the sixth $\overline{\text{WE}}$ pulse in the six-write pulse sequence. The Toggle Bit I is active during the sector time out.

In programming, if the sector being written to is protected, the toggle bit will toggle for about 1 μs and then stop toggling without the data having changed. In erase, the device will erase all the selected sectors except for the ones that are protected. If all selected sectors are protected, the chip will toggle the Toggle Bit I for about 100 μs and then drop back into read mode, having changed none of the data.

Either $\overline{\text{CE}}$ or $\overline{\text{OE}}$ toggling will cause the DQ_6 to toggle. In addition, an Erase Suspend/Resume command will cause the DQ_6 to toggle.

See "(7) AC Waveforms for Toggle Bit I during Embedded Algorithm Operations" in ■TIMING DIAGRAM and "(4) Toggle Bit Algorithm" in ■FLOW CHART for the Toggle Bit I timing specifications and diagrams.

DQ_5

Exceeded Timing Limits

DQ_5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions DQ_5 will produce a “1”. This is a failure condition which indicates that the program or erase cycle was not successfully completed. $\overline{\text{Data}}$ Polling is the only operating function of the device under this condition. The $\overline{\text{CE}}$ circuit will partially power down the device under these conditions. The $\overline{\text{OE}}$ and $\overline{\text{WE}}$ pins will control the output disable functions as described in "MBM29PL160TD/BD User Bus Operation Tables ($\overline{\text{BYTE}}$ = V_{IH} and $\overline{\text{BYTE}}$ = V_{IL})" in ■DEVICE BUS OPERATIONS.

The DQ_5 failure condition may also appear if a user tries to program a non blank location without erasing. In this case the device locks out and never completes the Embedded Algorithm operation. Hence, the system never reads a valid data on DQ_7 and DQ_6 never stops toggling. Once the device has exceeded timing limits, the DQ_5 bit will indicate a “1.” Please note that this is not a device failure condition since the device was incorrectly used. If this occurs, reset the device with command sequence.

DQ_3

Sector Erase Timer

After the completion of the initial sector erase command sequence the sector erase time-out will begin. DQ_3 will remain low until the time-out is complete. $\overline{\text{Data}}$ Polling and Toggle Bit I are valid after the initial sector erase command sequence.

If $\overline{\text{Data}}$ Polling or the Toggle Bit I indicates the device has been written with a valid erase command, DQ_3 may be used to determine if the sector erase timer window is still open. If DQ_3 is high (“1”) the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by $\overline{\text{Data}}$ Polling or Toggle Bit I. If DQ_3 is low (“0”), the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of DQ_3 prior to and following each subsequent sector erase command. If DQ_3 is high on the second status check, the command may not have been accepted.

See "Hardware Sequence Flags Table".

DQ_2

Toggle Bit II

This Toggle Bit II, along with DQ_6, can be used to determine whether the device is in the Embedded Erase Algorithm or in Erase Suspend.

Successive reads from the erasing sector will cause DQ_2 to toggle during the Embedded Erase Algorithm. If the device is in the erase-suspended-read mode, successive reads from the erase-suspended sector will cause DQ_2 to toggle. When the device is in the erase-suspended-program mode, successive reads from the byte address of the non-erase suspended sector will indicate a logic “1” at DQ_2.

DQ_6 is different from DQ_2 in that DQ_6 toggles only when the standard program or Erase, or Erase Suspend Program operation is in progress.

For example, DQ_2 and DQ_6 can be used together to determine if the erase-suspend-read mode is in progress. (DQ_2 toggles while DQ_6 does not.) See also "Toggle Bit Status Table" and "(12) DQ_2 vs. DQ_6" in ■TIMING DIAGRAM.

Furthermore, DQ_2 can also be used to determine which sector is being erased. When the device is in the erase mode, DQ_2 toggles if this bit is read from an erasing sector.

Toggle Bit Status Table

Mode	DQ_7	DQ_6	DQ_2
Program	$\overline{DQ_7}$	Toggle	1
Erase	0	Toggle	Toggle
Erase Suspend Read (Erase Suspended Sector) *1	1	1	Toggle
Erase-Suspend Program	$\overline{DQ_7}$	Toggle *1	1 *2

*1: Performing successive read operations from any address will cause DQ_6 to toggle.

*2: Reading the byte address being programmed while in the erase-suspend program mode will indicate logic “1” at the DQ_2 bit. However, successive reads from the erase-suspended sector will cause DQ_2 to toggle.

Data Protection

The MBM29PL160TD/BD is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up the device automatically resets the internal state machine to the Read mode. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific multi-bus cycle command sequence.

The device also incorporates several features to prevent inadvertent write cycles resulting form V_{CC} power-up and power-down transitions or system noise.

Low V_{CC} Write Inhibit

To avoid initiation of a write cycle during V_{CC} power-up and power-down, a write cycle is locked out for V_{CC} less than 2.3 V (typically 2.4 V). If $V_{CC} < V_{LKO}$, the command register is disabled and all internal program/erase circuits are disabled. Under this condition, the device will reset to the read mode. Subsequent writes will be ignored until the V_{CC} level is greater than V_{LKO}. It is the users responsibility to ensure that the control pins are logically correct to prevent unintentional writes when V_{CC} is above 2.3 V.

If the Embedded Erase Algorithm is interrupted, there is possibility that the erasing sector(s) will need to be erased again prior to programming.

Write Pulse “Glitch” Protection

Noise pulses of less than 5 ns (typical) on $\overline{OE}$, $\overline{CE}$, or $\overline{WE}$ will not change the command registers.

Logical Inhibit

Writing is inhibited by holding any one of $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IH}$, or $\overline{WE} = V_{IH}$. To initiate a write, $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

Power-up Write Inhibit

Power-up of the devices with $\overline{WE} = \overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$ will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to read mode on power-up.

Sector Protection

Device user is able to protect each sector individually to store and protect data. Protection circuit voids both program and erase commands that are addressed to protected sectors.

Any commands to program or erase addressed to protected sector are ignored (see “Sector Protection” in ■FUNCTIONAL DESCRIPTION).

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Storage Temperature	Tstg	–55	+125	°C
Ambient Temperature with Power Applied	T_A	–40	+85	°C
Voltage with respect to Ground All pins except A_9, $\overline{OE}$ *1, *2	V_{IN}, V_{OUT}	–0.5	+5.5	V
Power Supply Voltage *1	V_{CC}	–0.5	+4.0	V
A_9 and $\overline{OE}$ *3	V_{IN}	–0.5	+13.0	V

*1: Voltage is defined on the basis of V_{SS} = GND = 0 V.

*2: Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may undershoot V_{SS} to
–2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O pins is +6.0V. During voltage transitions, input or I/O pins may overshoot to V_{CC} +2.0 V for periods of up to 20 ns.

*3: Minimum DC input voltage on A_9, $\overline{OE}$ pins is –0.5 V. During voltage transitions, A_9, $\overline{OE}$ pins may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on A_9, $\overline{OE}$ pins is +13.0 V which may overshoot to +13.5 V for periods of up to 20 ns.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Ambient Temperature	T_A	-75	–20	—	+70	°C
		-90	–40	—	+85	
Power Supply Voltages *	V_{CC}	—	2.7	3.0	3.6	V

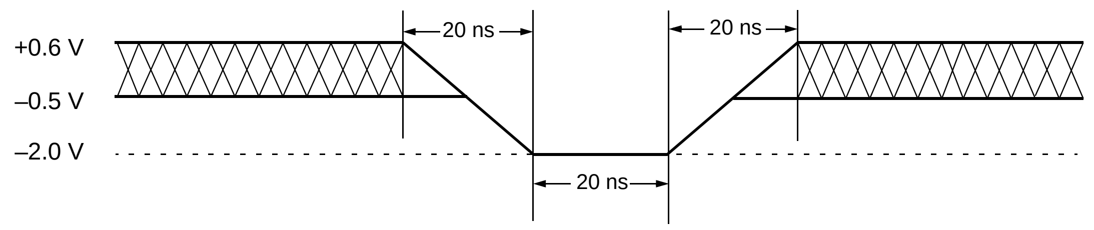
*: Voltage is defined on the basis of V_{SS} = GND = 0 V.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

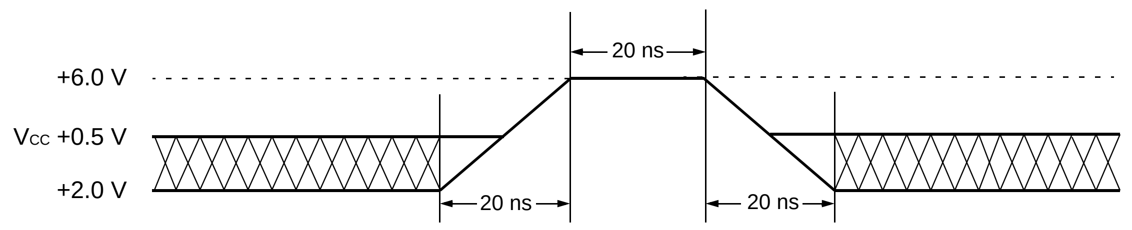
Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

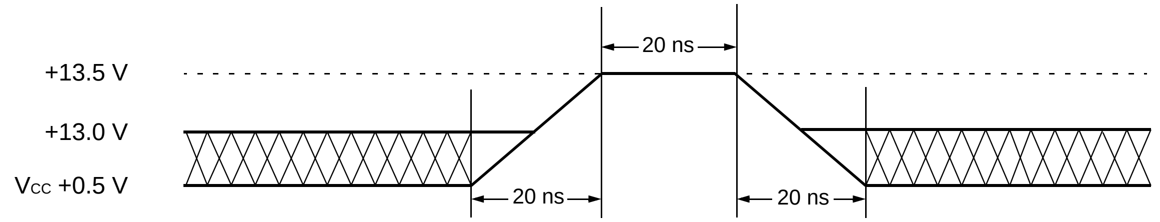
■ MAXIMUM OVERSHOOT/MAXIMUM UNDERSHOOT



Maximum Undershoot Waveform



Maximum Overshoot Waveform 1



Note : This waveform is applied for A_9, $\overline{OE}$.

Maximum Overshoot Waveform 2

■ DC CHARACTERISTICS

Parameter	Symbol	Conditions	Value Min	Value Typ	Value Max	Unit
Input Leakage Current	I_{LI}	$V_{IN} = V_{SS}$ to 5.5 V, $V_{CC} = V_{CC}$ Max	–1.0	—	+1.0	µA
Output Leakage Current	I_{LO}	$V_{OUT} = V_{SS}$ to 5.5 V, $V_{CC} = V_{CC}$ Max	–1.0	—	+1.0	µA
A_9, $\overline{OE}$, $\overline{RESET}$ Inputs Leakage Current	I_{LIT}	$V_{CC} = V_{CC}$ Max, A_9, $\overline{OE}$ = 12.5 V	—	—	35	µA
V_{CC} Active Current *1	I_{CC1}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$, f = 5 MHz	—	—	40	mA
		$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$, f = 10 MHz	—	—	70	mA
V_{CC} Active Current *2	I_{CC2}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	—	—	35	mA
V_{CC} Current (Standby)	I_{CC3}	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{CC} \pm 0.3$ V	—	1	5	µA
V_{CC} Current (Automatic Sleep Mode) *3	I_{CC4}	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{SS} \pm 0.3$ V, $V_{IN} = V_{CC} \pm 0.3$ V or $V_{SS} \pm 0.3$ V	—	1	5	µA
V_{CC} Active Current (Page Read Mode)	I_{CC5}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$, 30MHz	—	—	12	mA
		$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$, 40MHz	—	—	15	mA
Input Low Level	V_{IL}	—	–0.5	—	+0.8	V
Input High Level *5	V_{IH}	—	2.0	—	5.5	V
Voltage for Autoselect, Sector Protection (A_9, $\overline{OE}$) *4, *5	V_{ID}	—	11.5	12	12.5	V
Output Low Voltage Level	V_{OL}	I_{OL} = 4.0 mA, $V_{CC} = V_{CC}$ Min	—	—	0.45	V
Output High Voltage Level	V_{OH1}	I_{OH} = –2.0 mA, $V_{CC} = V_{CC}$ Min	2.4	—	—	V
	V_{OH2}	I_{OH} = –100 µA	V_{CC} – 0.4	—	—	V
Low V_{CC} Lock-Out Voltage	V_{LKO}	—	2.3	2.4	2.5	V

*1: The I_{CC} current listed includes both the DC operating current and the frequency dependent component.

*2: I_{CC} active while Embedded Erase or Embedded Program is in progress.

*3: Automatic sleep mode enables the low power mode when addresses remain stable for 150 ns.

*4: Applicable only for sector protection.

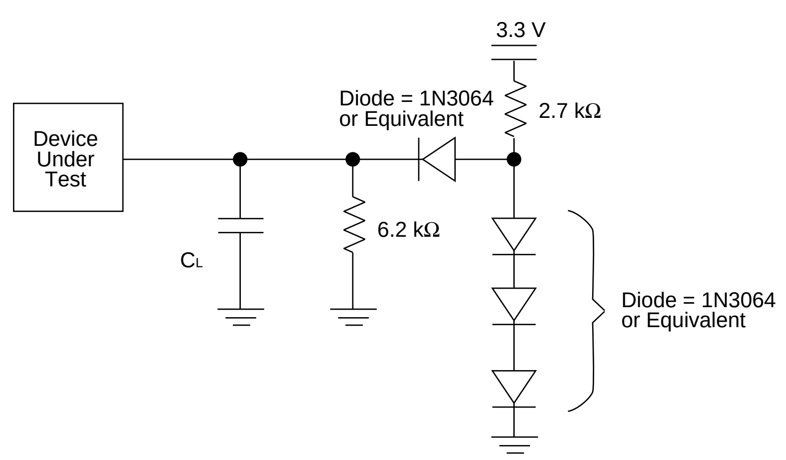
*5: Applicable only for V_{CC} applying.

■ AC CHARACTERISTICS

- **Read Only Operations Characteristics**

Parameter	Symbol		Conditions	Value				Unit
				-75		-90		
	JEDEC	Standard		Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	—	75	—	90	—	ns
Address to Output Delay	t_{AVQV}	t_{ACC}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IL}$	—	75	—	90	ns
Page Read Cycle Time	—	t_{PRC}	—	25	—	35	—	ns
Page Address to Output Delay	—	t_{PACC}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IL}$	—	25	—	35	ns
Chip Enable to Output Delay	t_{ELQV}	t_{CE}	$\overline{OE} = V_{IL}$	—	75	—	90	ns
Output Enable to Output Delay	t_{GLQV}	t_{OE}	—	—	25	—	35	ns
Chip Enable to Output High-Z	t_{EHQZ}	t_{DF}	—	—	20	—	30	ns
Output Enable to Output High-Z	t_{GHQZ}	t_{DF}	—	—	20	—	30	ns
Output Hold Time From Address, $\overline{CE}$ or $\overline{OE}$, Whichever Occurs First	t_{AXQX}	t_{OH}	—	4	—	5	—	ns
$\overline{CE}$ to $\overline{BYTE}$ Switching Low or High	—	t_{ELFL} t_{ELFH}	—	—	4	—	5	ns

Note: Test Conditions: Output Load: 1 TTL gate and 30 pF (MBM29PL160TD/BD-75)
1 TTL gate and 100 pF (MBM29PL160TD/BD-90)
Input rise and fall times: 5 ns
Input pulse levels: 0.0 V or 3.0 V
Timing measurement reference level
Input: 1.5 V
Output: 1.5 V



Notes: C_L = 30 pF including jig capacitance (MBM29PL160TD/BD-75)
C_L = 100 pF including jig capacitance (MBM29PL160TD/BD-90)

Test Conditions

- **Write (Erase/Program) Operations**

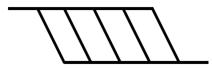
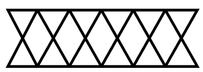
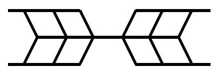
Parameter		Symbol		Value						Unit
				-75			-90			
		JEDEC	Standard	Min	Typ	Max	Min	Typ	Max	
Write Cycle Time		t_{AVAV}	t_{WC}	75	—	—	90	—	—	ns
Address Setup Time		t_{AVWL}	t_{AS}	0	—	—	0	—	—	ns
Address Hold Time		t_{WLAX}	t_{AH}	45	—	—	45	—	—	ns
Data Setup Time		t_{DVWH}	t_{DS}	35	—	—	45	—	—	ns
Data Hold Time		t_{WHDX}	t_{DH}	0	—	—	0	—	—	ns
Output Enable Setup Time		—	t_{OES}	0	—	—	0	—	—	ns
Output Enable Hold Time	Read	—	t_{OEH}	0	—	—	0	—	—	ns
	Toggle and $\overline{\text{Data}}$ Polling			10	—	—	10	—	—	ns
Read Recover Time Before Write		t_{GHWL}	t_{GHWL}	0	—	—	0	—	—	ns
Read Recover Time Before Write ($\overline{OE}$ High to $\overline{CE}$ Low)		t_{GHEL}	t_{GHEL}	0	—	—	0	—	—	ns
$\overline{CE}$ Setup Time		t_{ELWL}	t_{CS}	0	—	—	0	—	—	ns
$\overline{WE}$ Setup Time		t_{WLEL}	t_{WS}	0	—	—	0	—	—	ns
$\overline{CE}$ Hold Time		t_{WHEH}	t_{CH}	0	—	—	0	—	—	ns
$\overline{WE}$ Hold Time		t_{EHWH}	t_{WH}	0	—	—	0	—	—	ns
Write Pulse Width		t_{WLWH}	t_{WP}	35	—	—	35	—	—	ns
$\overline{CE}$ Pulse Width		t_{ELEH}	t_{CP}	35	—	—	35	—	—	ns
Write Pulse Width High		t_{WHWL}	t_{WPH}	20	—	—	30	—	—	ns
$\overline{CE}$ Pulse Width High		t_{EHEL}	t_{CPH}	20	—	—	30	—	—	ns
Programming Operation	Byte	t_{WHWH1}	t_{WHWH1}	—	8.6	—	—	8.6	—	µs
	Word			—	12.6	—	—	12.6	—	µs
Sector Erase Operation *1		t_{WHWH2}	t_{WHWH2}	—	4.8	—	—	4.8	—	s
V_{CC} Setup Time		—	t_{VCS}	50	—	—	50	—	—	µs
Voltage Transition Time *2		—	t_{VLHT}	4	—	—	4	—	—	µs
Write Pulse Width *2		—	t_{WPP}	100	—	—	100	—	—	µs
$\overline{OE}$ Setup Time to $\overline{WE}$ Active *2		—	t_{OESP}	4	—	—	4	—	—	µs
$\overline{CE}$ Setup Time to $\overline{WE}$ Active *2		—	t_{CSP}	4	—	—	4	—	—	µs
Recover Time From RY/$\overline{BY}$		—	t_{RB}	0	—	—	0	—	—	ns
$\overline{BYTE}$ Switching Low to Output High-Z		—	t_{FLQZ}	—	—	30	—	—	30	ns
$\overline{BYTE}$ Switching High to Output Active		—	t_{FHQV}	40	—	—	30	—	—	ns
Delay Time from Embedded Output Enable		—	t_{EOE}	—	—	75	—	—	90	ns

*1: This does not include the preprogramming time.

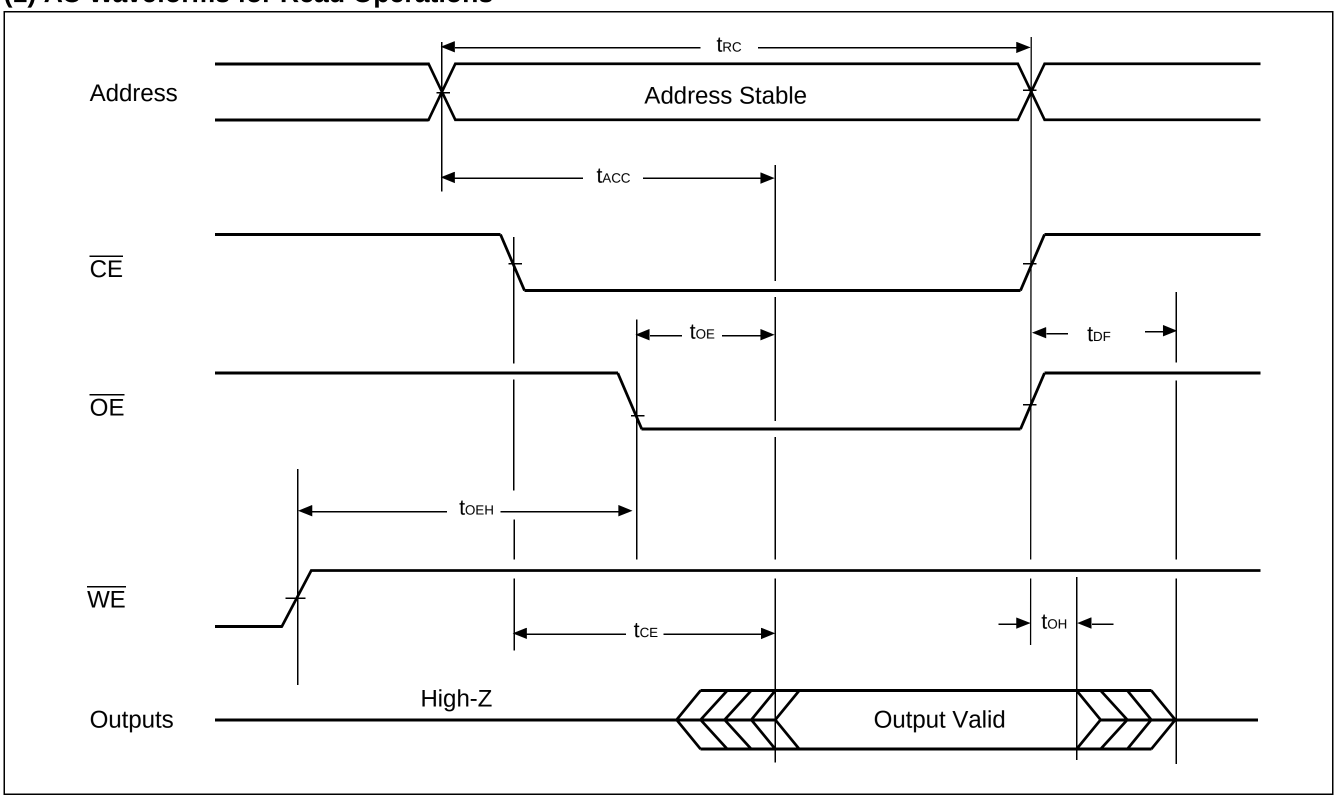
*2: This timing is for Sector Protection operation.

■ TIMING DIAGRAM

- **Key to Switching Waveforms**

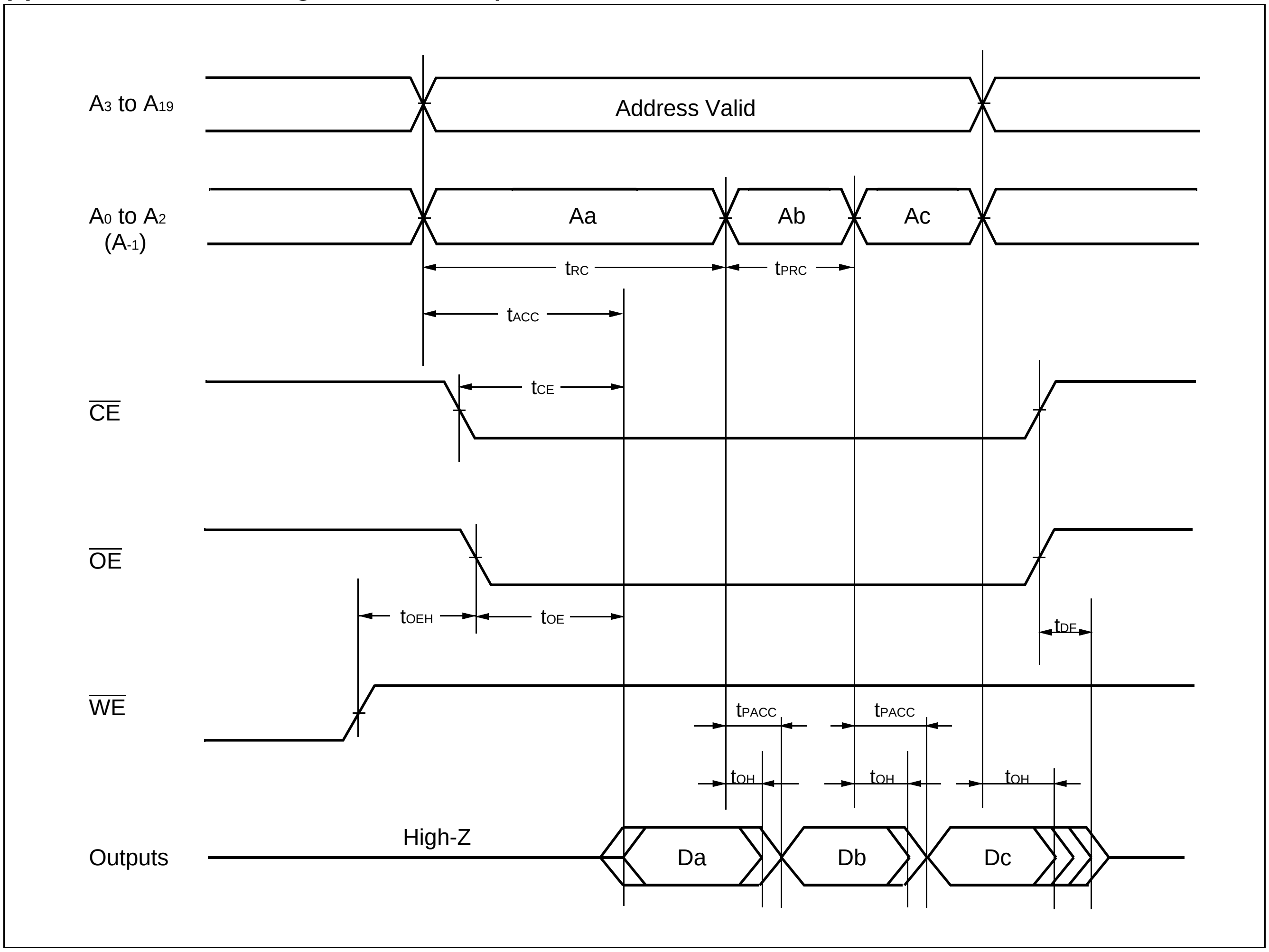
WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Change from H to L
	May Change from L to H	Will Be Change from L to H
	"H" or "L": Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

(1) AC Waveforms for Read Operations

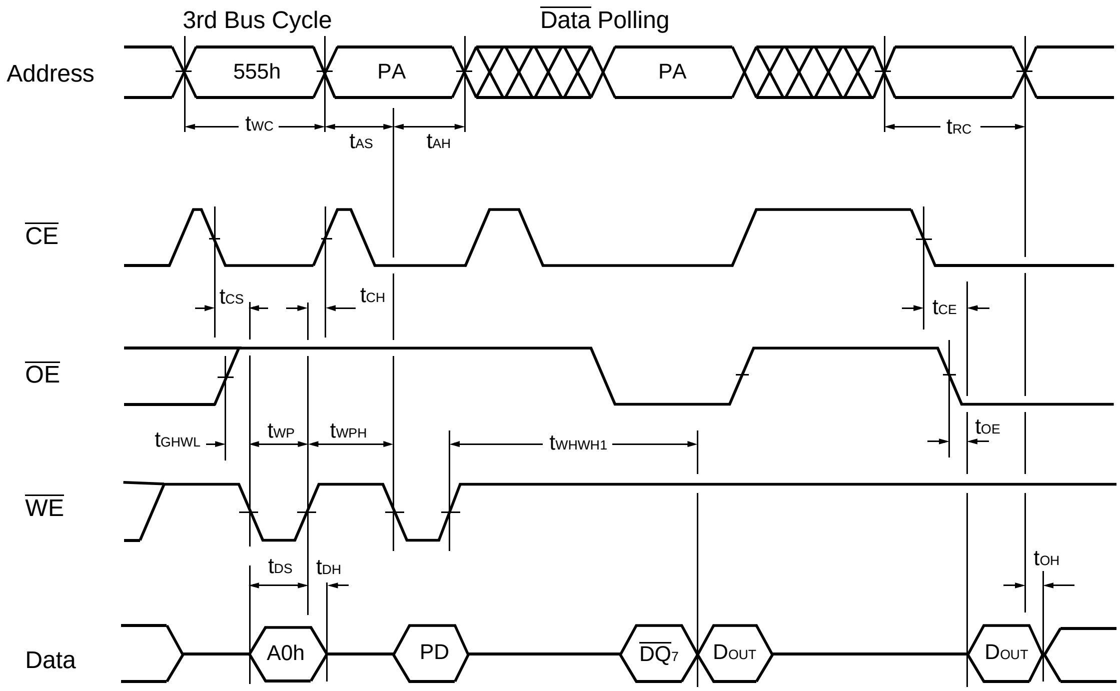


Retired Product DS05-20872-4E_July 31, 2007

(2) AC Waveforms for Page Read Mode Operations

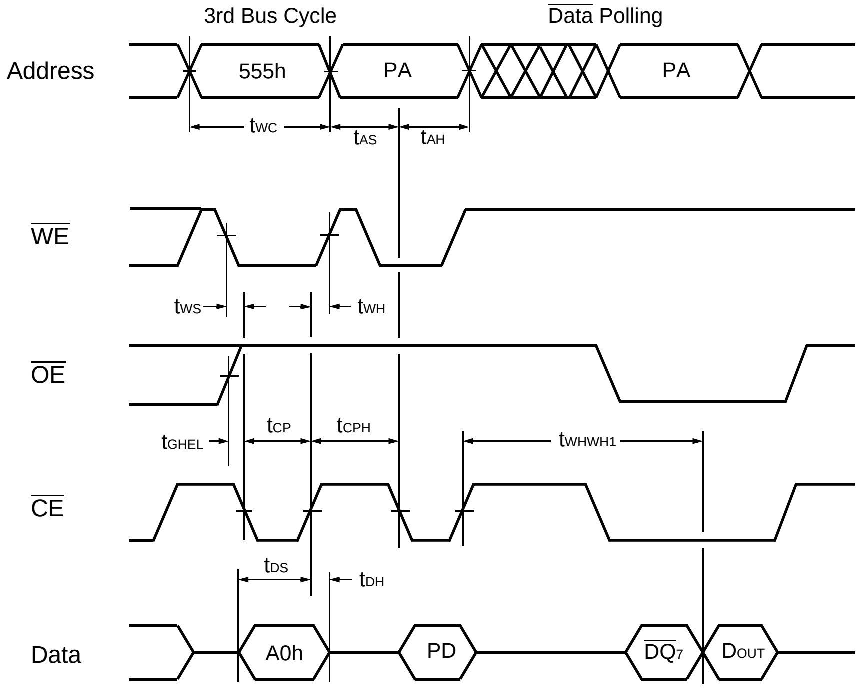


(3) AC Waveforms for Alternate $\overline{WE}$ Controlled Program Operations



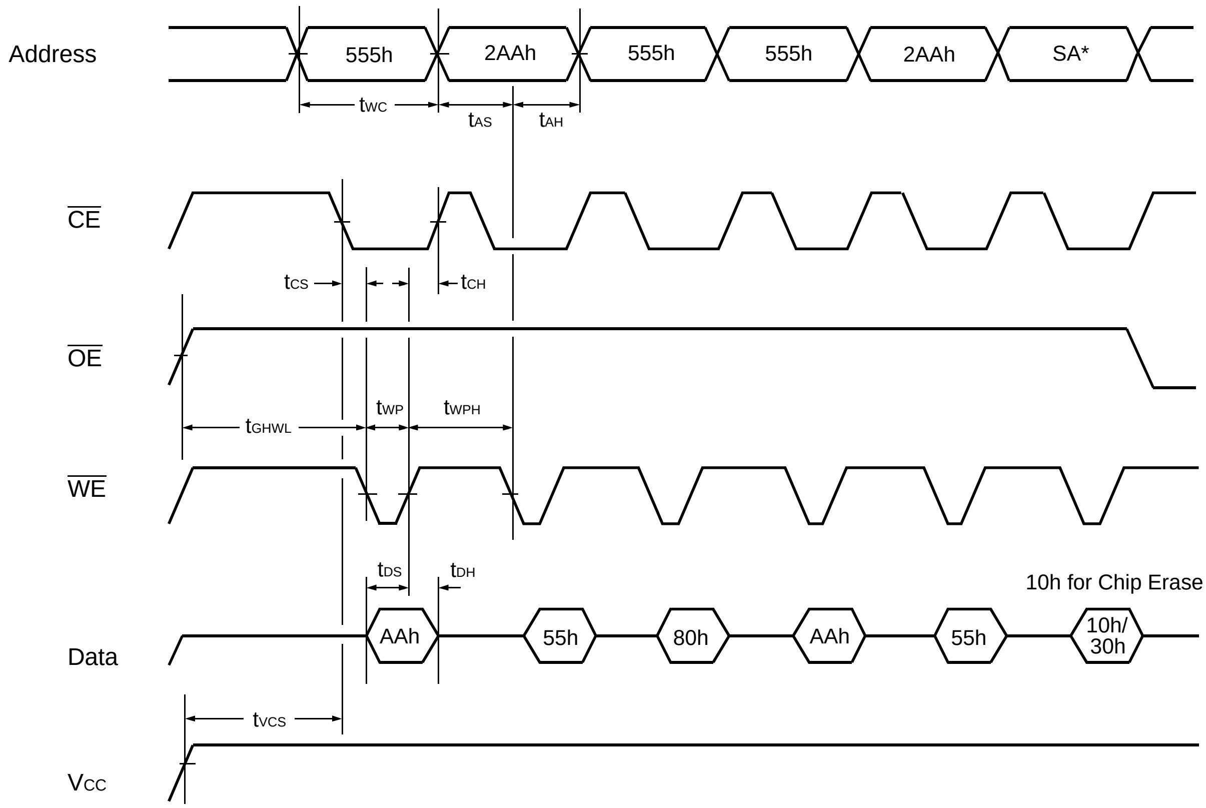
Notes:
- PA is address of the memory location to be programmed.
- PD is data to be programmed at word address.
- $\overline{DQ_7}$ is the output of the complement of the data written to the device.
- D_{OUT} is the output of the data written to the device.
- Figure indicates last two bus cycles out of four bus cycle sequence.
- These waveforms are for the ×16 mode. (The addresses differ from ×8 mode.)

(4) AC Waveforms for Alternate $\overline{CE}$ Controlled Program Operations



Notes:
- PA is address of the memory location to be programmed.
- PD is data to be programmed at word address.
- $\overline{DQ_7}$ is the output of the complement of the data written to the device.
- D_{OUT} is the output of the data written to the device.
- Figure indicates last two bus cycles out of four bus cycle sequence.
- These waveforms are for the ×16 mode. (The addresses differ from ×8 mode.)

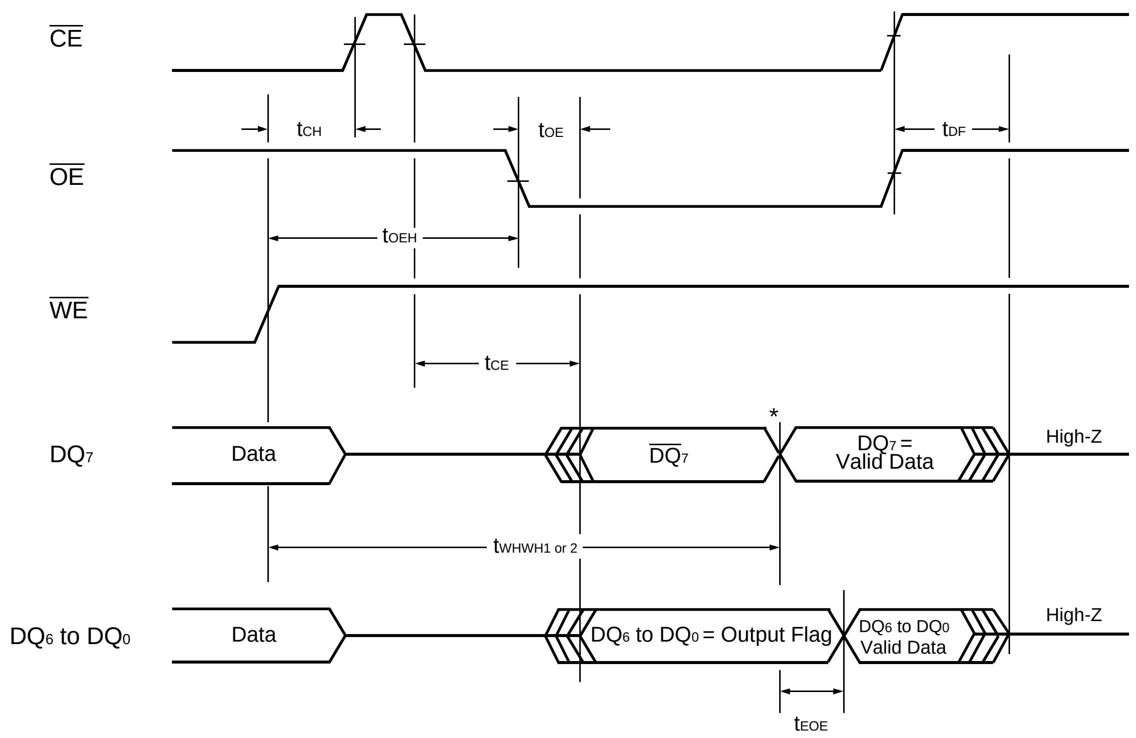
(5) AC Waveforms for Chip/Sector Erase Operations



*: SA is the sector address for Sector Erase. Addresses = 555h (Word) for Chip Erase.

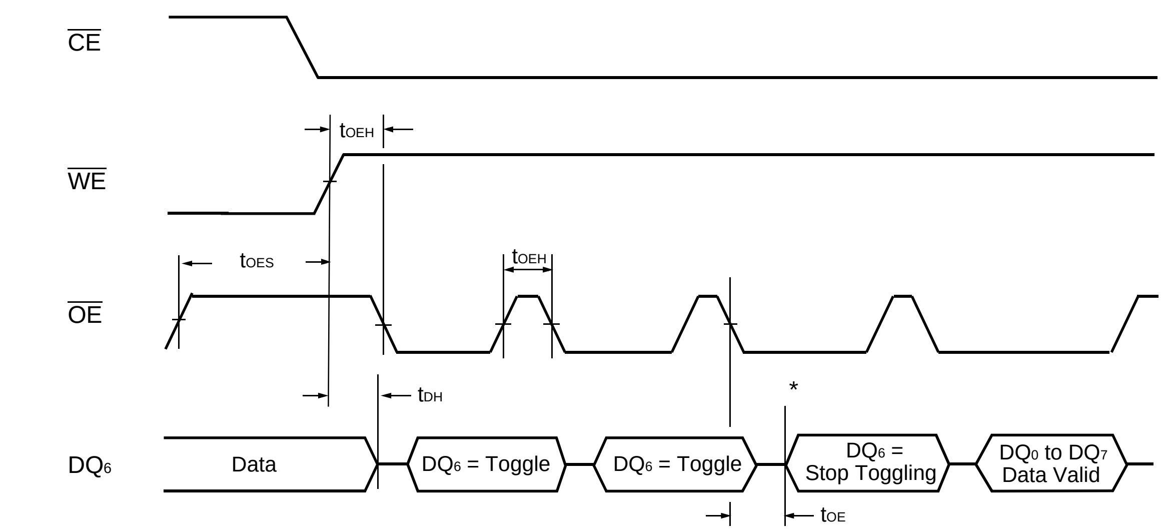
Note : These waveforms are for the ×16 mode. The addresses differ from ×8 mode.

(6) AC Waveforms for Data Polling during Embedded Algorithm Operations



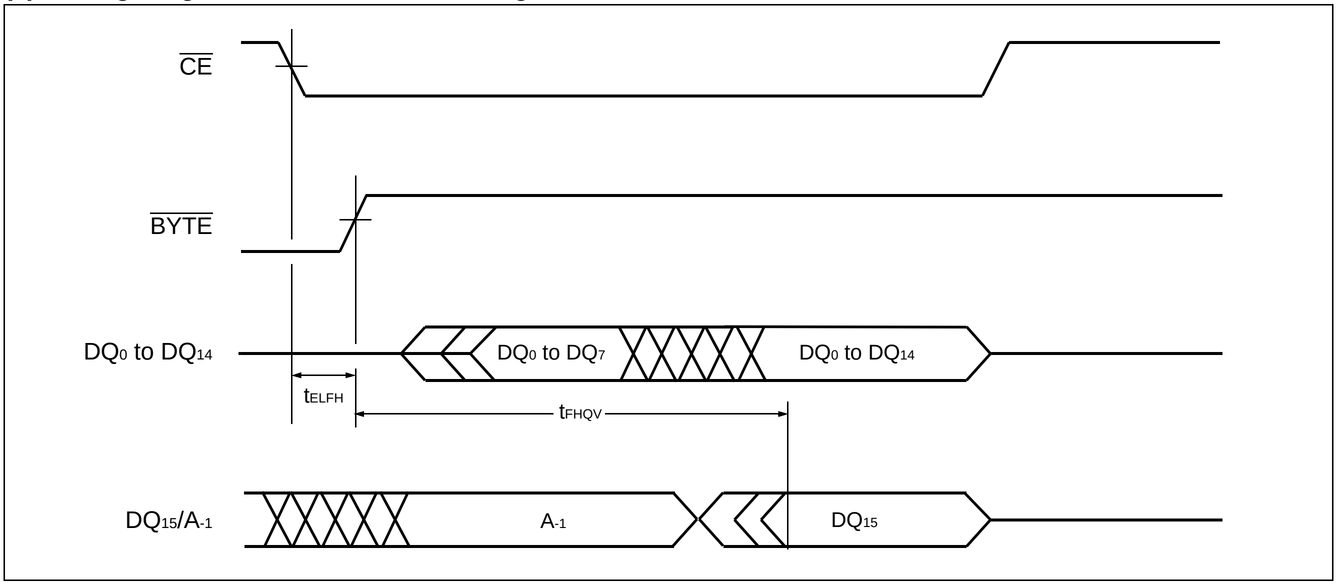
* : DQ_7 = Valid Data (The device has completed the Embedded operation.)

(7) AC Waveforms for Toggle Bit I during Embedded Algorithm Operations

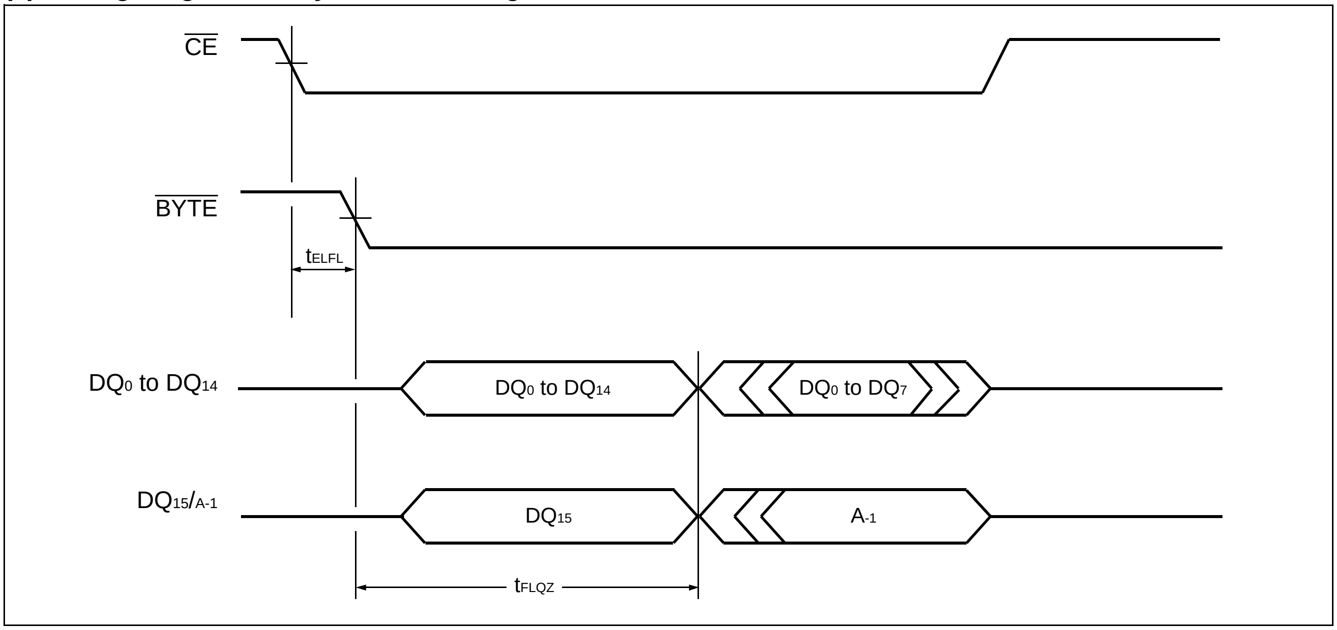


*: DQ_6 = Stops toggling. (The device has completed the Embedded operation.)

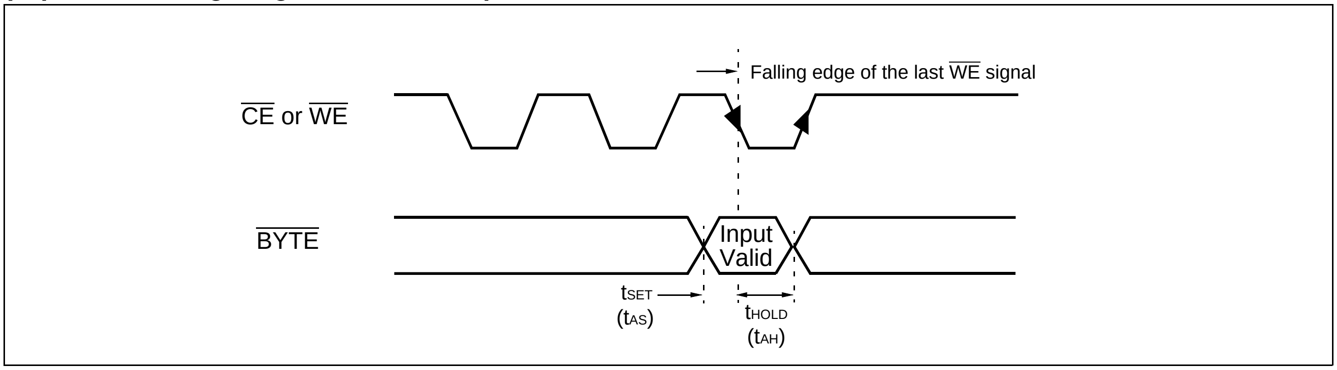
(8) Timing Diagram for Word Mode Configuration



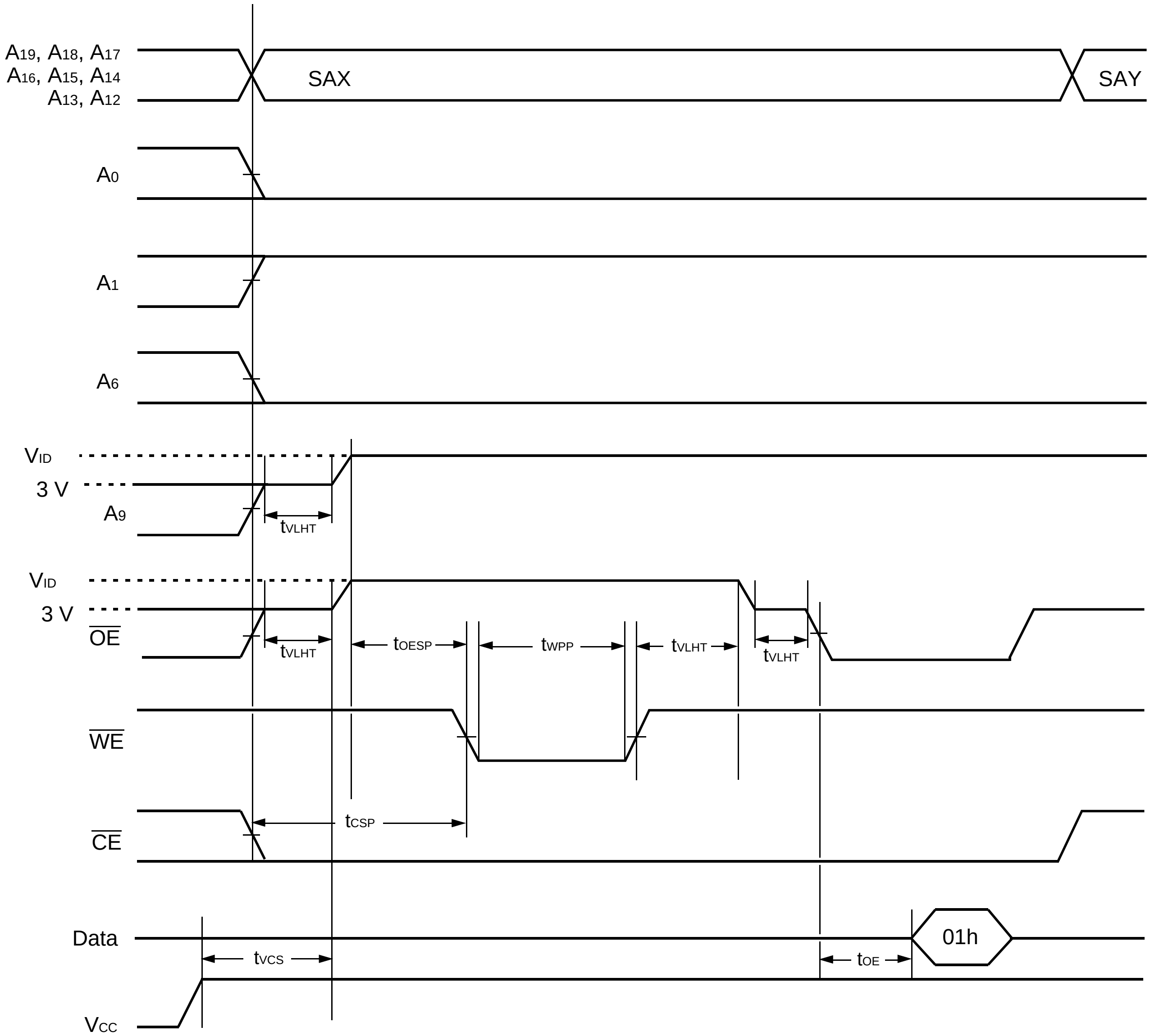
(9) Timing Diagram for Byte Mode Configuration



(10) BYTE Timing Diagram for Write Operations

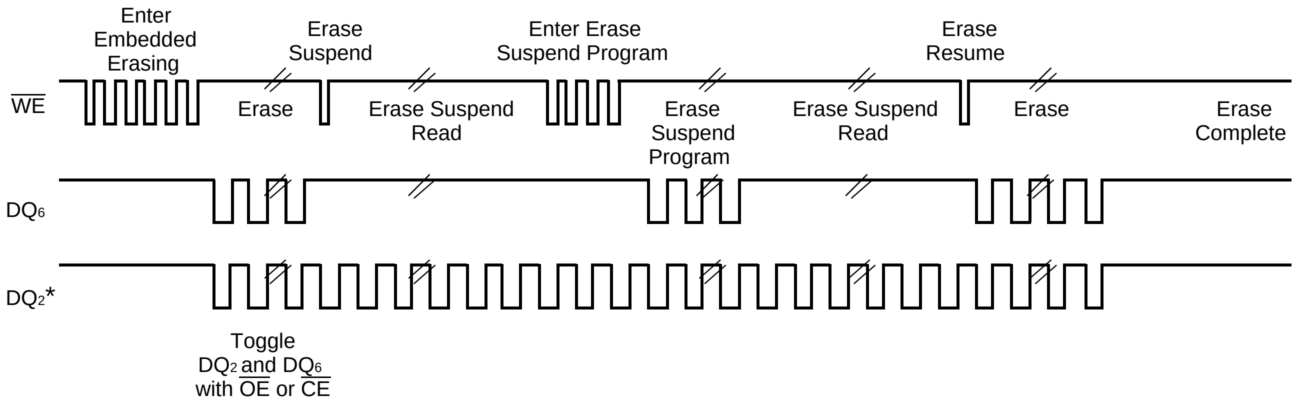


(11) AC Waveforms for Sector Protection Timing Diagram



SAX = Sector Address for initial sector
SAY = Sector Address for next sector
Note: A_{-1} is V_{IL} on byte mode.

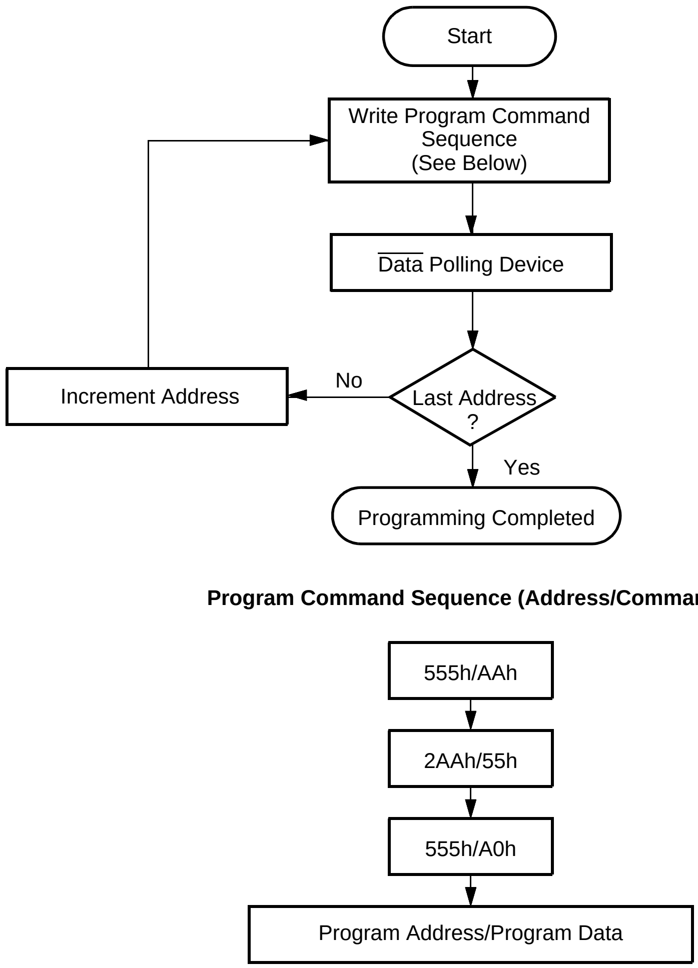
(12) DQ_2 vs. DQ_6



*: DQ_2 is read from the erase-suspended sector.

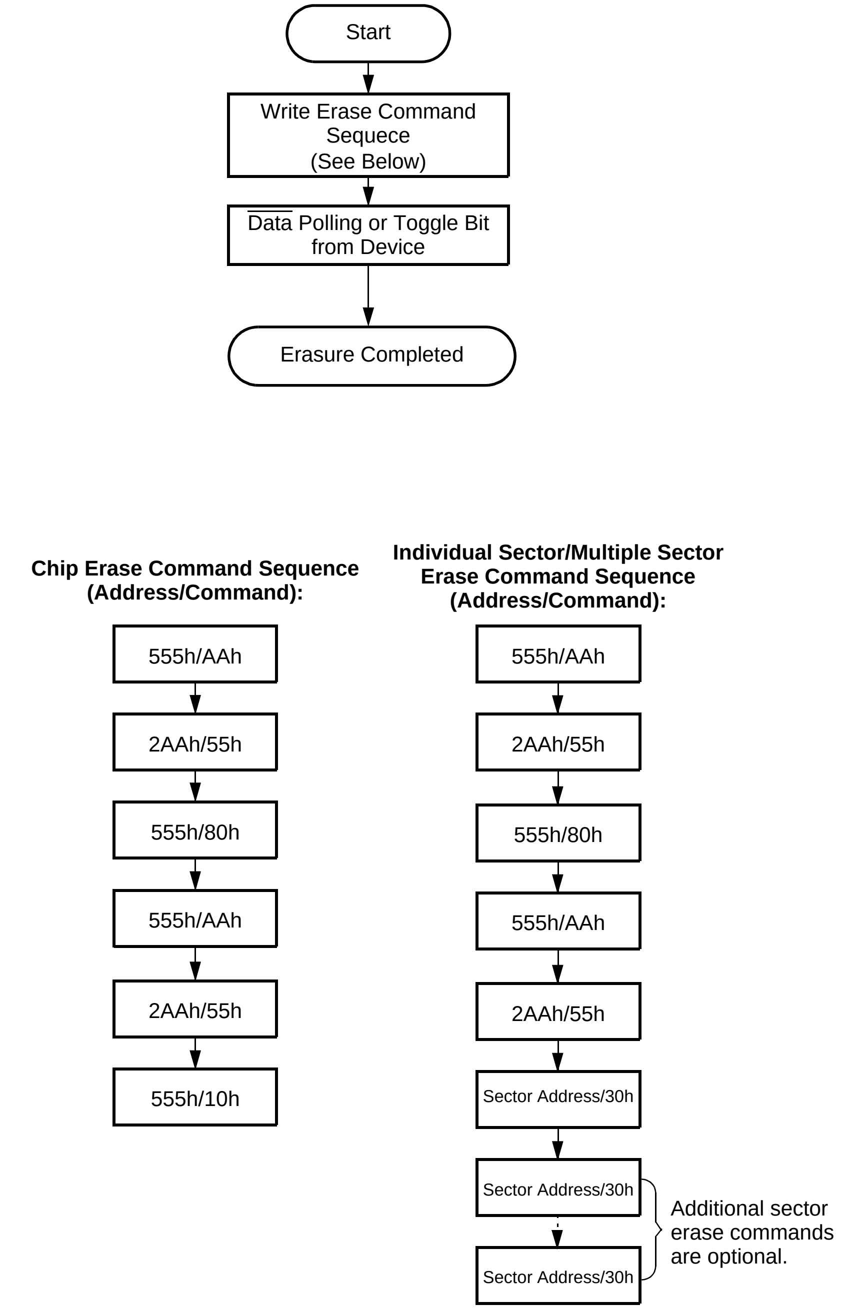
■ FLOW CHART

(1) Embedded Program™ Algorithm



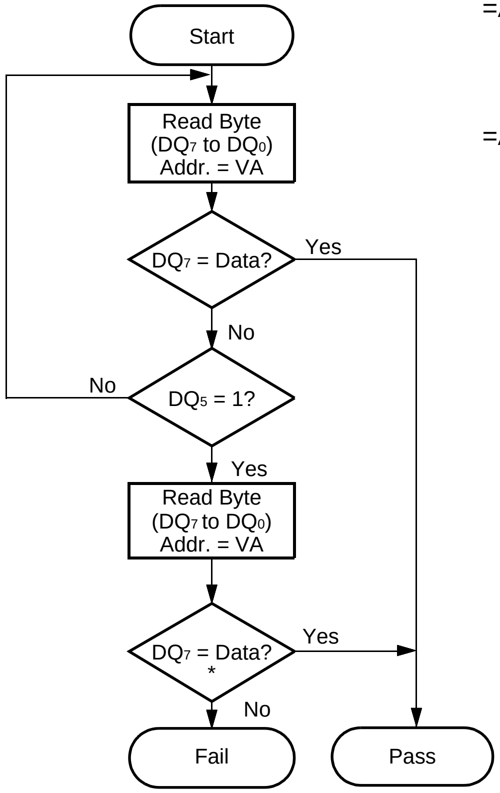
Note : The sequence is applied for ×16 mode.
The addresses differ from ×8 mode.

(2) Embedded Erase™ Algorithm



Note : The sequence is applied for ×16 mode.
The addresses differ from ×8 mode.

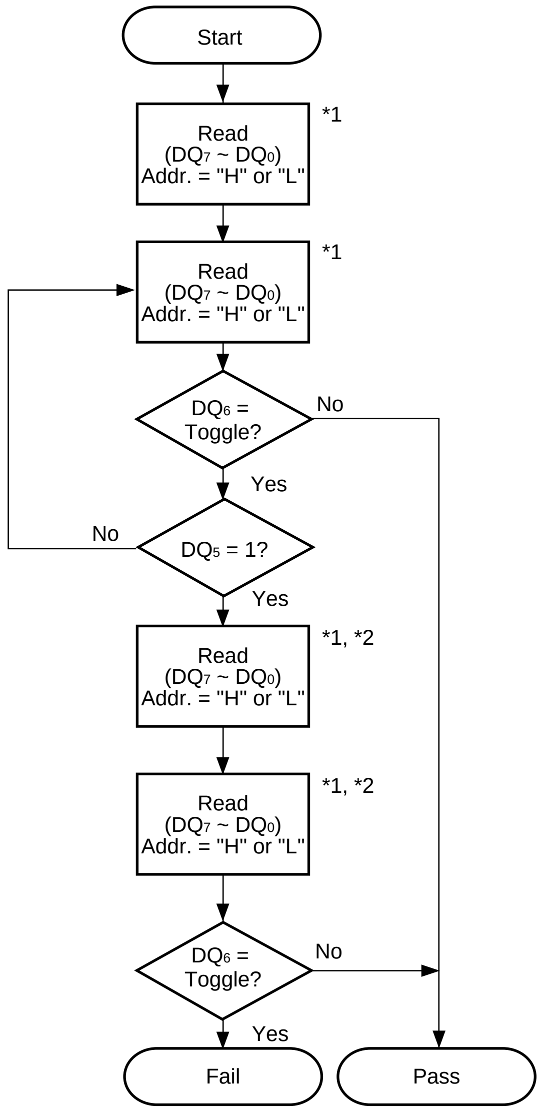
(3) $\overline{\text{Data}}$ Polling Algorithm



VA =Address for programming
=Any of the sector addresses within the sector being erased during sector erase or multiple erases operation.
=Any of the sector addresses within the sector not being protected during sector erase or multiple sector erases operation.

* : DQ_7 is rechecked even if DQ_5 = "1" because DQ_7 may change simultaneously with DQ_5.

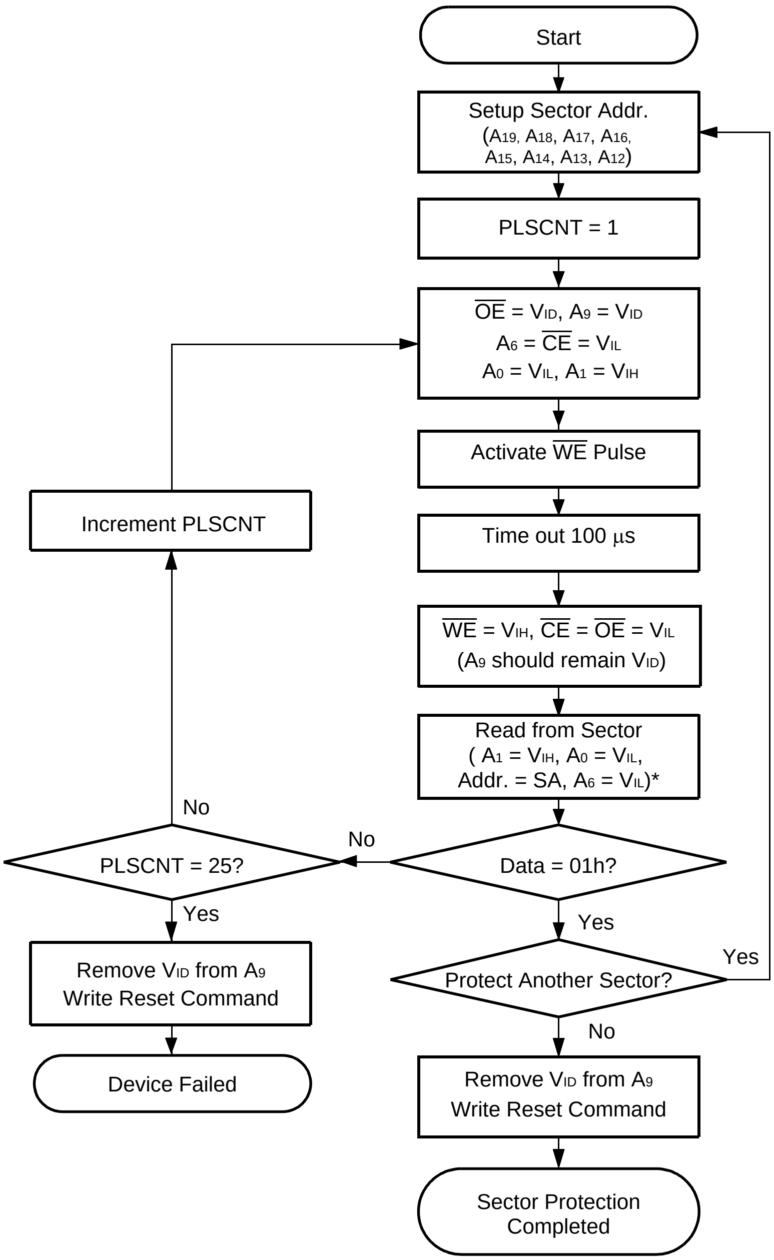
(4) Toggle Bit Algorithm



*1 : Read toggle bit twice to determine whether it is toggling.

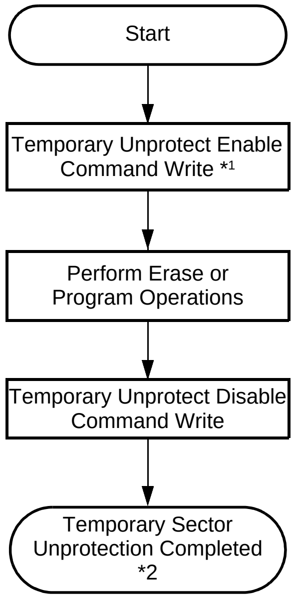
*2 : DQ_6 is rechecked even if DQ_5 = “1” because DQ_6 may stop toggling at the same time as DQ_5 changing to “1”.

(5) Sector Protection Algorithm



* : A_{-1} is V_{IL} on byte mode.

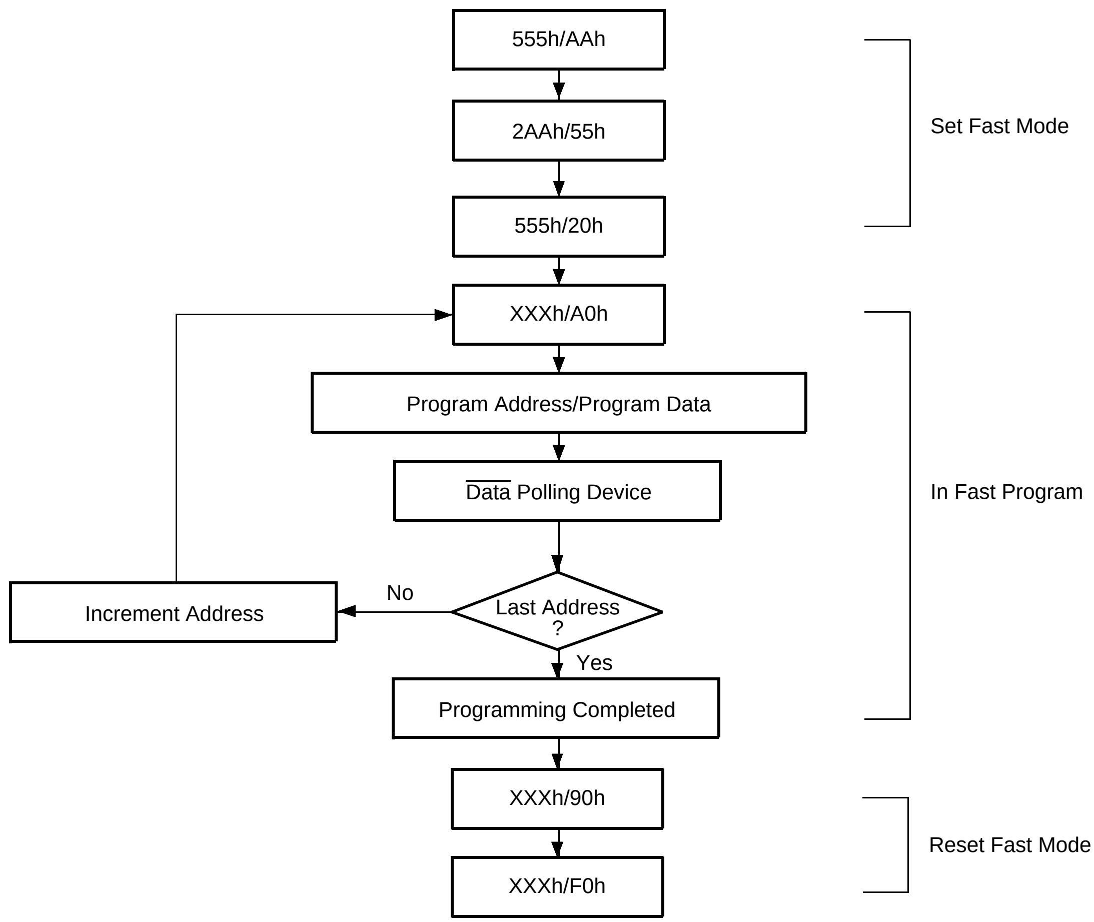
(6) Temporary Sector Unprotection Algorithm



*1: All protected sectors are unprotected.

*2: All previously protected sectors are protected once again.

(7) Embedded Programming Algorithm for Fast Mode



Note: The sequence is applied for ×16 mode.
The addresses differ from ×8 mode.

■ ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Comments
	Min	Typ	Max		
Sector Erase Time	—	4.8	60	s	Excludes programming time prior to erasure
Word Programming Time	—	12.6	360	µs	Excludes system-level overhead
Byte Programming Time	—	8.6	300	µs	Excludes system-level overhead
Chip Programming Time	—	18	140	s	Excludes system-level overhead
Erase/Program Cycle	100,000	—	—	cycle	

■ PIN CAPACITANCE

Parameter	Symbol	Test Setup	Value		Unit
			Typ	Max	
Input Capacitance	C_{IN}	$V_{IN} = 0$	6.0	7.5	pF
Output Capacitance	C_{OUT}	$V_{OUT} = 0$	8.5	12.0	pF
Control Pin Capacitance	C_{IN2}	$V_{IN} = 0$	8.0	11.5	pF

Notes: • Test conditions $T_A = +25°C$, f = 1.0 MHz
• DQ_{15}/A_{-1} pin capacitance is stipulated by output capacitance.

■ ORDERING INFORMATION

Part No.	Package	Access Time (ns)	Sector Architecture
MBM29PL160TD-75PF MBM29PL160TD-90PF	44-pin plastic SOP (FPT-44P-M16)	75 90	Top Sector
MBM29PL160TD-75PFTN MBM29PL160TD-90PFTN	48-pin plastic TSOP (1) (FPT-48P-M19) (Normal Bend)	75 90	
MBM29PL160TD-75PFTR MBM29PL160TD-90PFTR	48-pin plastic TSOP (1) (FPT-48P-M20) (Reverse Bend)	75 90	
MBM29PL160BD-75PF MBM29PL160BD-90PF	44-pin plastic SOP (FPT-44P-M16)	75 90	Bottom Sector
MBM29PL160BD-75PFTN MBM29PL160BD-90PFTN	48-pin plastic TSOP (1) (FPT-48P-M19) (Normal Bend)	75 90	
MBM29PL160BD-75PFTR MBM29PL160BD-90PFTR	48-pin plastic TSOP (1) (FPT-48P-M20) (Reverse Bend)	75 90	

MBM29PL160 T D -75 PFTN

PACKAGE TYPE
PFTN = 48-Pin Thin Small Outline Package (TSOP(1)) Normal Bend
PFTR = 48-Pin Thin Small Outline Package (TSOP(1)) Reverse Bend
PF = 44-Pin Small Outline Package (SOP)

SPEED OPTION
See Product Selector Guide

DEVICE REVISION

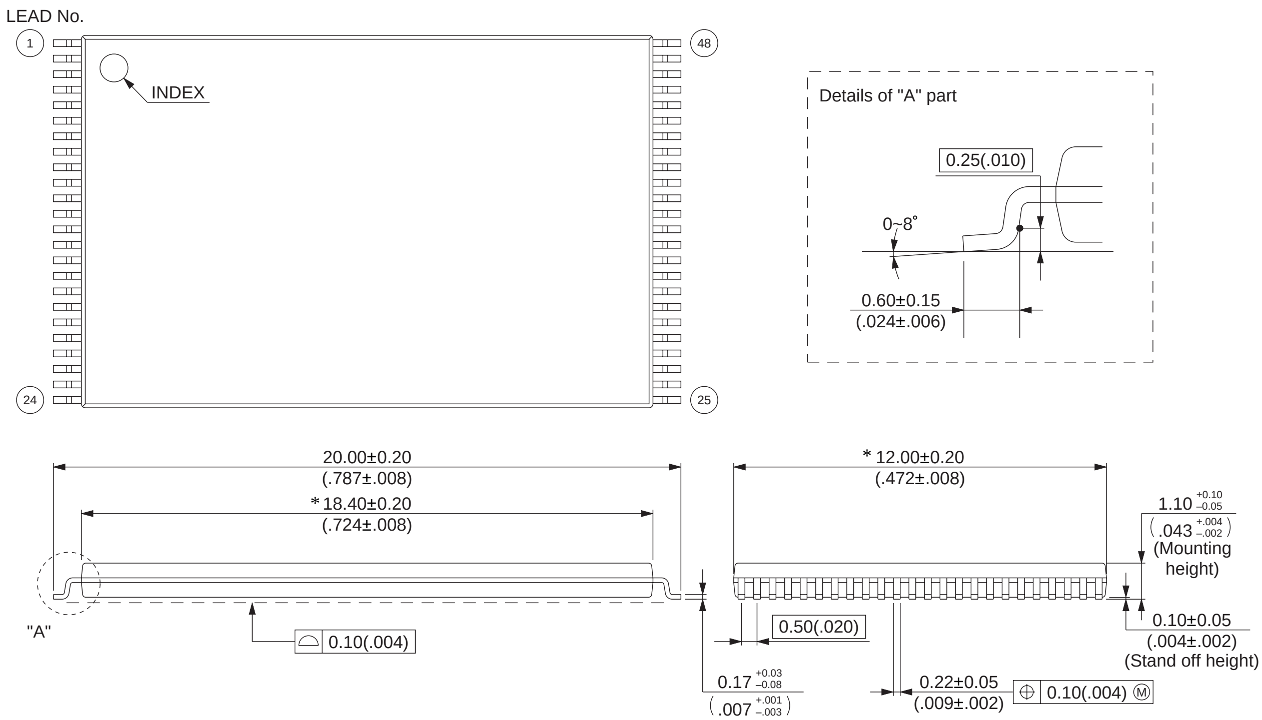
BOOT CODE SECTOR ARCHITECTURE
T = Top sector
B = Bottom sector

DEVICE NUMBER/DESCRIPTION
MBM29PL160
16 Mega-bit (2M × 8-Bit or 1M × 16-Bit) CMOS Page Mode Flash Memory
3.0 V-only Read, Write, and Erase

■ PACKAGE DIMENSIONS

48-pin plastic TSOP (1)
(FPT-48P-M19)

Note 1) * : Values do not include resin protrusion.
Resin protrusion and gate protrusion are +0.15(.006)Max(each side).
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.

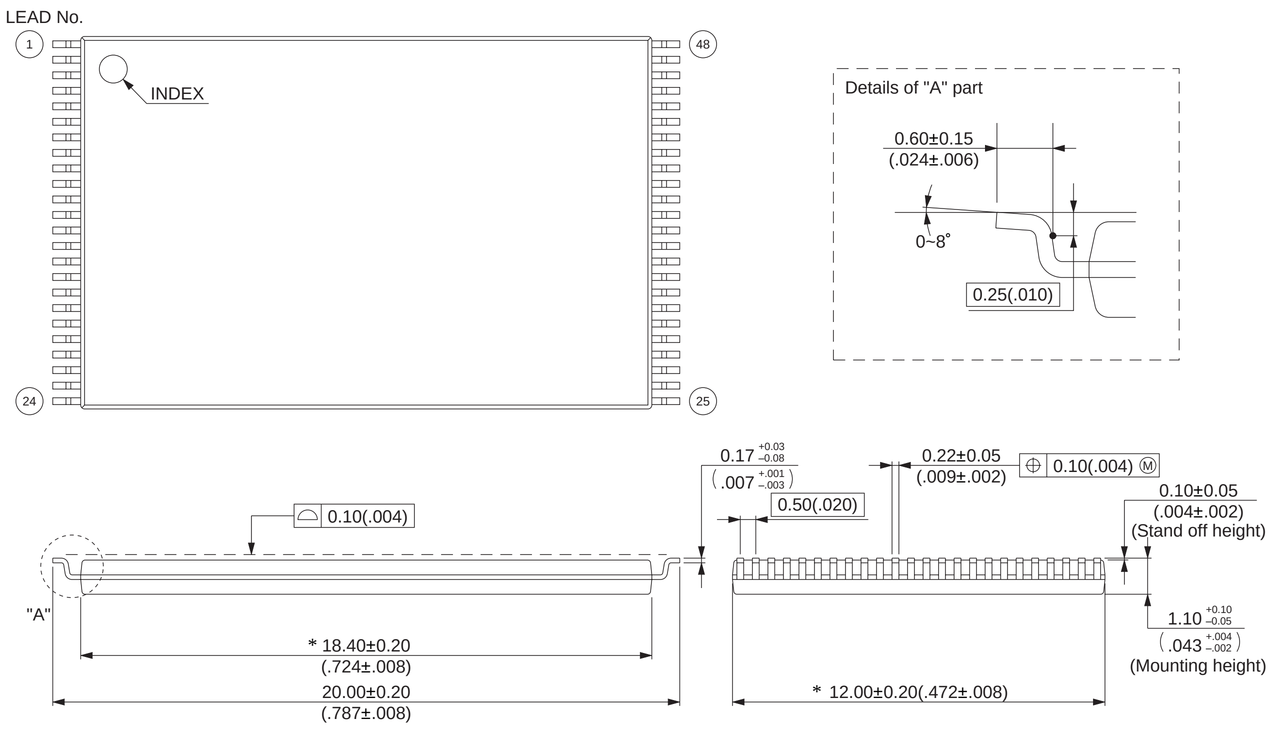


Dimensions in mm (inches).
Note: The values in parentheses are reference values.

(Continued)

48-pin plastic TSOP (1)
(FPT-48P-M20)

Note 1) * : Values do not include resin protrusion.
Resin protrusion and gate protrusion are +0.15(.006)Max(each side).
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



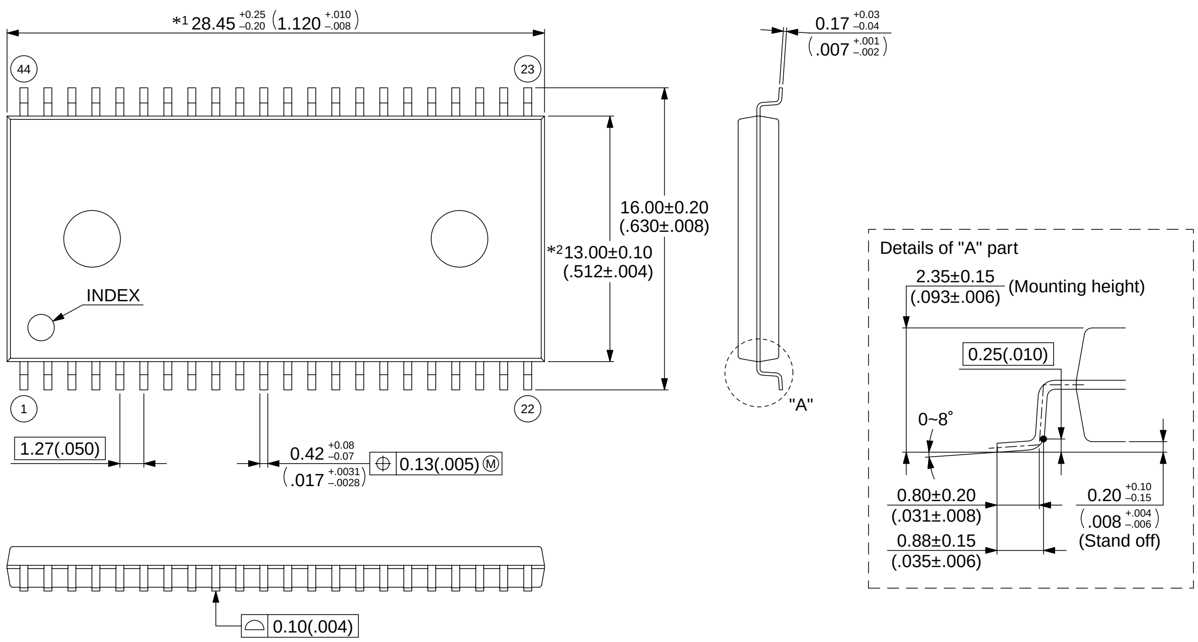
Dimensions in mm (inches).
Note: The values in parentheses are reference values.

(Continued)

(Continued)

44-pin plastic SOP
(FPT-44P-M16)

Note 1) *1 : These dimensions include resin protrusion.
Note 2) *2 : These dimensions do not include resin protrusion.
Note 3) Pins width and pins thickness include plating thickness.
Note 4) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

MEMO

MEMO

Revision History

Revision DS05-20872-4E（July 31, 2007）

The following comment is added.

This product has been retired and is not recommended for new designs. Availability of this document is retained for reference and historical purposes only.

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DS05-20872-3E