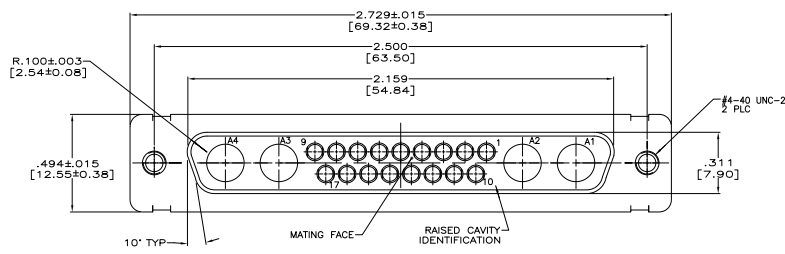
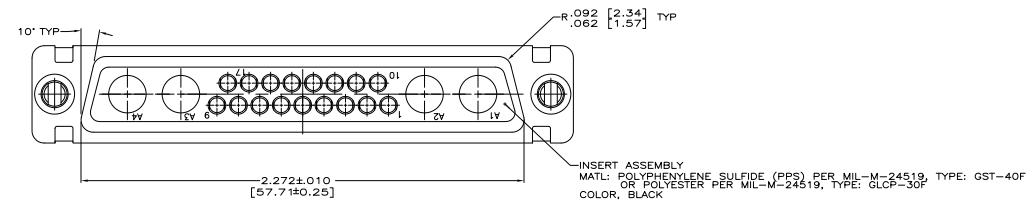
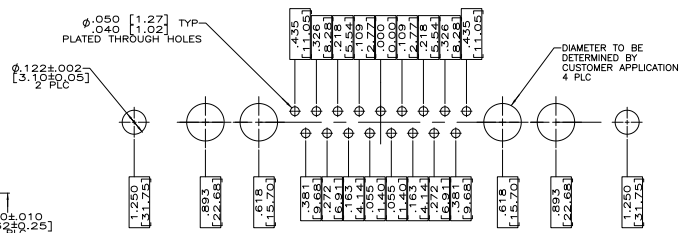
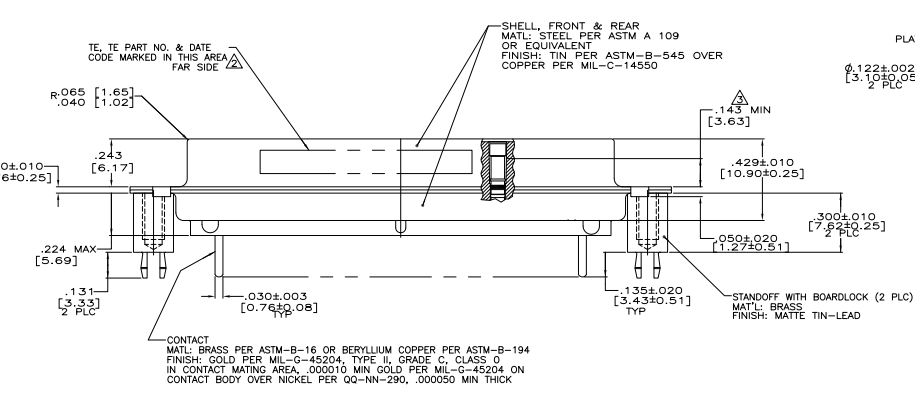


THIS DRAWING IS UNPUBLISHED  
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REV	DATE	DESCRIPTION	BY	CHK	APP
DF	DO				
C		REVISED PER ECO-08-013174			10-04-08 CT RL



- TRUE POSITION TOLERANCE FOR P.C. BOARD LAYOUT IS .010 [0.25] AT MAX MATERIAL CONDITION.
- MARKED WITH .047 [1.19]-.062 [1.57] HIGH CHARACTERS. FAR SIDE REFERS TO THE WIDE SIDE OF THE KEYSTONE. NEAR SIDE REFERS TO THE NARROW SIDE OF THE KEYSTONE.
- POINT OF ELECTRICAL ENGAGEMENT - AS MEASURED WITH A .0390 [0.991]-.0393 [0.998] DIA SQUARE ENDED TEST PIN.
- DIMENSIONS AND TOLERANCES PER ANSI Y14.5M-1982.
- THIS DRAWING SHALL BE INTERPRETED IN ACCORDANCE WITH APPLICABLE STANDARDS LISTED IN MIL-STD-100.
- BOARDLOCK FOR .062 [1.57] P.C. BOARD.



1218887-1  
 PART NO.

THIS DRAWING IS A CONTROLLED DOCUMENT.		REV. C	THOMAS	25-001-02	DATE	10-04-08	BY	CT	APP	RL
DESIGNED BY	THOMAS	REVISED BY	MILLER	REVISED DATE	10-04-08	DATE				
CHECKED BY		APPROVED BY								
DATE		DATE		DATE		DATE		DATE		DATE
SIZE	A1	SIZE	A1	SIZE	A1	SIZE	A1	SIZE	A1	SIZE
REVISED PER	ECO-08-013174	REVISED PER	ECO-08-013174	REVISED PER	ECO-08-013174	REVISED PER	ECO-08-013174	REVISED PER	ECO-08-013174	REVISED PER
CUSTOMER DRAWING		CUSTOMER DRAWING		CUSTOMER DRAWING		CUSTOMER DRAWING		CUSTOMER DRAWING		CUSTOMER DRAWING