8 PORT LOW COST 10/100 SWITCH

- Supports eight 10/100 Mbit/s Ethernet ports with MII interface
- Capable of trunking up to 800 Mbit/s link
- Full- and half-duplex mode operation
- Speed auto-negotiation through MDIO
- Built-in storage of 1K MAC addresses
- Designed to utilize low-cost SGRAM
- Serial EEPROM interface for low-cost system configuration
- Automatic source address learning
- Secure mode traffic filtering
- Broadcast storm control
- Port monitoring support
- IEEE 802.3x flow control for full duplex operation
- Optional backpressure flow control support for half-duplex operation
- Supports store-and-forward mode switching
- VLAN support
- 3.3V operation
- Packaged in 256-pin PQFP

Product Description

The AL102A is an eight-port 10/100 Mbit/s dual speed Ethernet switch. A low-cost Fast Ethernet switch can be implemented using the AL102A with low-cost SGRAM. The AL102A also supports VLAN and multiple port aggregation trunks.

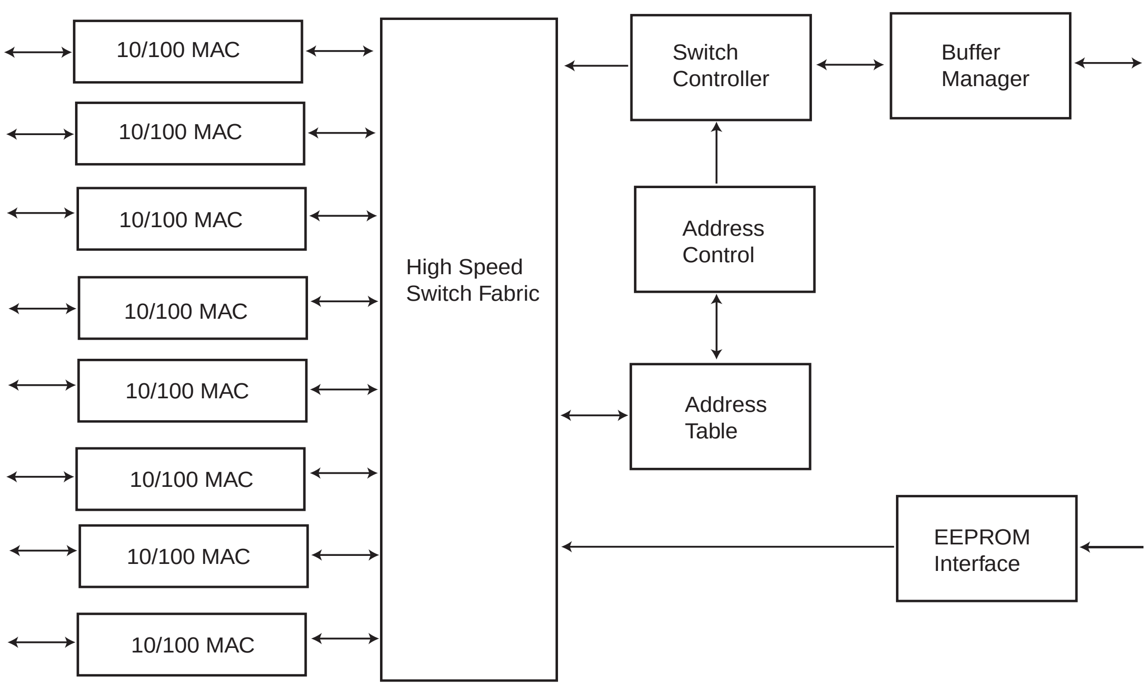

Figure 1 System Block Diagram

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Table of Contents

1. AL102A Overview

The AL102A provides eight 10/100 Mbit/s Ethernet ports. Each port supports both 10 and 100 Mbit/s data rate. The operation mode is auto-negotiated by the PHY. All ports are full-duplex capable. The device also supports VLAN for workgroup and segment switching applications.

The AL102A also supports trunking applications. The chip provides two optional load balancing schemes, explicit and dynamic. With trunking, one can group up to four full-duplex links together to form a single 800 Mbit/s link.

Data received from the MAC interface is stored in the external memory buffer. The AL102A utilizes cost effective SGRAM to provide 8-Mbit or 16-Mbit of buffer memory.

During transmission, the data is obtained from the buffer memory and routed to the destination port. For half-duplex operations, in the event of a collision, the MAC control will back off and retransmit in accordance to the IEEE 802.3 specification.

The AL102A provides two flow control methods. For half-duplex operations, an optional jamming based flow control (also known as backpressure) is available to prevent loss of data. With this method of flow control, the switch will generate a jam signal when the receive-buffer is full. The sending station will not transmit until the line is clear.

In the full-duplex mode, the AL102A utilizes IEEE 802.3x as the flow control mechanism.

All ports support multiple MAC addresses. The switch chip supports up to 1K MAC addresses internally. These MAC addresses are shared among all eight ports.

The initialization and configuration of the switch is programmed by an external EEPROM. For an unmanaged switch design, a CPU is not required. Field reconfiguration can be achieved by using a parallel interface to reprogram the EEPROM.

The AL102A supports port based VLAN. The VLAN register set is used to configure the destination ports for multicast and broadcast frames.

The device also provides two levels of security for intrusion protection. Security can be implemented on a per port basis.

The AL102A operates only in the store and forward mode. The entire frame is checked for error. Frames with errors are automatically filtered and will not be forwarded to the destination port.

Other features include port monitoring and broadcast storm throttling.

Pin Diagram

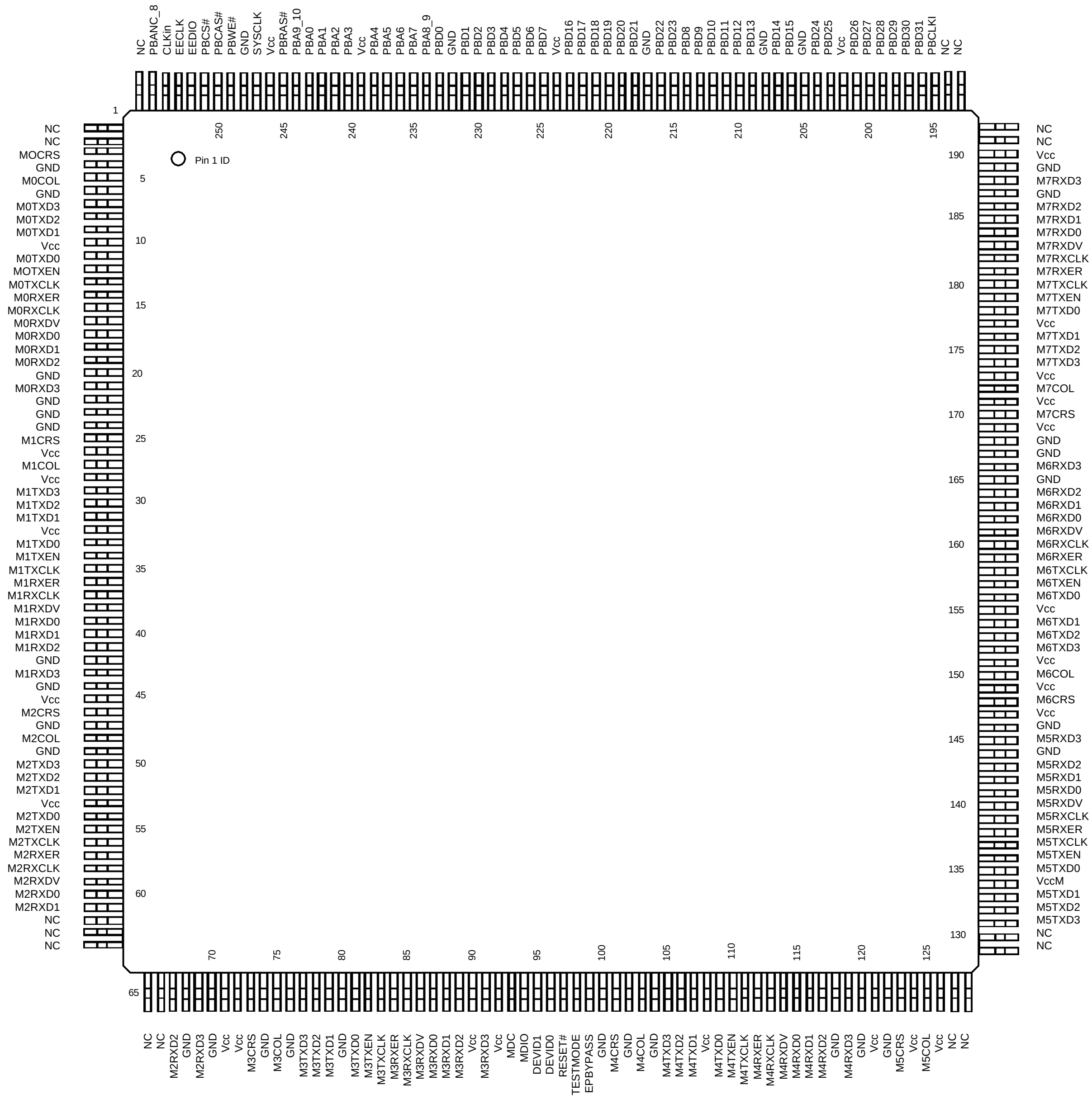


Figure 2 AL102A Pin Diagram (Top View)

2. Pin Descriptions

Table 1: MII Interface Port 0

PIN NAME	PIN NUMBER	I/O	DESCRIPTION
M0TXD3 M0TXD2 M0TXD1 M0TXD0	7 8 9 11	O	Transmit Data - NRZ data to be transmitted to transceiver. Signal TX_EN and TXD0 through TX_D3 are clocked out by the rising edge of TX_CLK.
M0TXEN	12	O	Transmit Enable. Synchronous to the transmit clock.
M0TXCLK	13	I	Transmit Clock Input. 25 MHz for 100 Mbit/s and 2.5 MHz for 10 Mbit/s.
M0RXD3 M0RXD2 M0RXD1 M0RXD0	21 19 18 17	I	Receive Data - NRZ from the transceiver. For MII interface, signal RX_DV, RX_ER and RX_D0 through RX_D3 are sampled by the rising edge of RX_CLK.
M0RXDV	16	I	Receive Data Valid.
M0RXCLK	15	I	Receive Clock.
M0RXER	14	I	Receive Data Error.
M0CRS	3	I	Carrier Sense.
M0COL	5	I	Collision Detect.

Table 2: MII Interface Port 1

PIN NAME	PIN NUMBER	I/O	DESCRIPTION
M1TXD3 M1TXD2 M1TXD1 M1TXD0	29 30 31 33	O	Transmit Data - NRZ data to be transmitted to transceiver. Signal TX_EN and TXD0 through TX_D3 are clocked out by the rising edge of TX_CLK.
M1TXEN	34	O	Transmit Enable. Synchronous to the transmit clock.
M1TXCLK	35	I	Transmit Clock Input. 25 MHz for 100 Mbit/s and 2.5 MHz for 10 Mbit/s.
M1RXD3 M1RXD2 M1RXD1 M1RXD0	43 41 40 39	I	Receive Data - NRZ from the transceiver. For MII interface, signal RX_DV, RX_ER and RX_D0 through RX_D3 are sampled by the rising edge of RX_CLK.
M1RXDV	38	I	Receive Data Valid.

Table 2: MII Interface Port 1 (Continued)

M1RXCLK	37	I	Receive Clock.
M1RXER	36	I	Receive Data Error.
M1CRS	25	I	Carrier Sense.
M1COL	27	I	Collision Detect.

Table 3: MII Interface Port 2

PIN NAME	PIN NUMBER	I/O	DESCRIPTION
M2TXD3 M2TXD2 M2TXD1 M2TXD0	50 51 52 54	O	Transmit Data - NRZ data to be transmitted to transceiver. Signal TX_EN and TXD0 through TX_D3 are clocked out by the rising edge of TX_CLK.
M2TXEN	55	O	Transmit Enable. Synchronous to the transmit clock.
M2TXCLK	56	I	Transmit Clock Input. 25 MHz for 100 Mbit/s and 2.5 MHz for 10 Mbit/s.
M2RXD3 M2RXD2 M2RXD1 M2RXD0	69 67 61 60	I	Receive Data - NRZ from the transceiver. For MII interface, signal RX_DV, RX_ER and RX_D0 through RX_D3 are sampled by the rising edge of RX_CLK.
M2RXDV	59	I	Receive Data Valid.
M2RXCLK	58	I	Receive Clock.
M2RXER	57	I	Receive Data Error.
M2CRS	46	I	Carrier Sense.
M2COL	48	I	Collision Detect.

Table 4: MII Interface Port 3

PIN NAME	PIN NUMBER	I/O	DESCRIPTION
M3TXD3 M3TXD2 M3TXD1 M3TXD0	77 78 79 81	O	Transmit Data - NRZ data to be transmitted to transceiver. Signal TX_EN and TXD0 through TX_D3 are clocked out by the rising edge of TX_CLK.
M3TXEN	82	O	Transmit Enable. Synchronous to the transmit clock.
M3TXCLK	83	I	Transmit Clock Input. 25 MHz for 100 Mbit/s and 2.5 MHz for 10 Mbit/s.
M3RXD3 M3RXD2 M3RXD1 M3RXD0	91 89 88 87	I	Receive Data - NRZ from the transceiver. For MII interface, signal RX_DV, RX_ER and RX_D0 through RX_D3 are sampled by the rising edge of RX_CLK.
M3RXDV	86	I	Receive Data Valid.
M3RXCLK	85	I	Receive Clock.
M3RXER	84	I	Receive Data Error.
M3CRS	73	I	Carrier Sense.
M3COL	75	I	Collision Detect.

Table 5: MII Interface Port 4

PIN NAME	PIN NUMBER	I/O	DESCRIPTION
M4TXD3 M4TXD2 M4TXD1 M4TXD0	105 106 107 109	O	Transmit Data - NRZ data to be transmitted to transceiver. Signal TX_EN and TXD0 through TX_D3 are clocked out by the rising edge of TX_CLK.
M4TXEN	110	O	Transmit Enable. Synchronous to the transmit clock.
M4TXCLK	111	I	Transmit Clock Input. 25 MHz for 100 Mbit/s and 2.5 MHz for 10 Mbit/s.
M4RXD3 M4RXD2 M4RXD1 M4RXD0	119 117 116 115	I	Receive Data - NRZ from the transceiver. For MII interface, signal RX_DV, RX_ER and RX_D0 through RX_D3 are sampled by the rising edge of RX_CLK.
M4RXDV	114	I	Receive Data Valid.
M4RXCLK	113	I	Receive Clock.

Table 5: MII Interface Port 4 (Continued)

M4RXER	112	I	Receive Data Error.
M4CRS	101	I	Carrier Sense.
M4COL	103	I	Collision Detect.

Table 6: MII Interface Port 5

PIN NAME	PIN NUMBER	I/O	DESCRIPTION
M5TXD3 M5TXD2 M5TXD1 M5TXD0	131 132 133 135	O	Transmit Data - NRZ data to be transmitted to transceiver. Signal TX_EN and TXD0 through TX_D3 are clocked out by the rising edge of TX_CLK.
M5TXEN	136	O	Transmit Enable. Synchronous to the transmit clock.
M5TXCLK	137	I	Transmit Clock Input. 25 MHz for 100 Mbit/s and 2.5 MHz for 10 Mbit/s.
M5RXD3 M5RXD2 M5RXD1 M5RXD0	145 143 142 141	I	Receive Data - NRZ from the transceiver. For MII interface, signal RX_DV, RX_ER and RX_D0 through RX_D3 are sampled by the rising edge of RX_CLK.
M5RXDV	140	I	Receive Data Valid.
M5RXCLK	139	I	Receive Clock.
M5RXER	138	I	Receive Data Error.
M5CRS	123	I	Carrier Sense.
M5COL	125	I	Collision Detect.

Table 7: MII Interface Port 6

PIN NAME	PIN NUMBER	I/O	DESCRIPTION
M6TXD3 M6TXD2 M6TXD1 M6TXD0	152 153 154 156	O	Transmit Data - NRZ data to be transmitted to transceiver. Signal TX_EN and TXD0 through TX_D3 are clocked out by the rising edge of TX_CLK.
M6TXEN	157	O	Transmit Enable. Synchronous to the transmit clock.
M6TXCLK	158	I	Transmit Clock Input. 25 MHz for 100 Mbit/s and 2.5 MHz for 10 Mbit/s.
M6RXD3 M6RXD2 M6RXD1 M6RXD0	166 164 163 162	I	Receive Data - NRZ data from the transceiver. For MII interface, signal RX_DV, RX_ER and RX_D0 through RX_D3 are sampled by the rising edge of RX_CLK.
M6RXDV	161	I	Receive Data Valid.
M6RXCLK	160	I	Receive Clock.
M6RXER	159	I	Receive Data Error.
M6CRS	148	I	Carrier Sense.
M6COL	150	I	Collision Detect.

Table 8: MII Interface Port 7

PIN NAME	PIN NUMBER	I/O	DESCRIPTION
M7TXD3 M7TXD2 M7TXD1 M7TXD0	174 175 176 178	O	Transmit Data - NRZ data to be transmitted to transceiver. Signal TX_EN and TXD0 through TX_D3 are clocked out by the rising edge of TX_CLK.
M7TXEN	179	O	Transmit Enable. Synchronous to the transmit clock.
M7TXCLK	180	I	Transmit Clock Input. 25 MHz for 100 Mbit/s and 2.5 MHz for 10 Mbit/s.
M7RXD3 M7RXD2 M7RXD1 M7RXD0	188 186 185 184	I	Receive Data - NRZ data from the transceiver. For MII interface, signal RX_DV, RX_ER and RX_D0 through RX_D3 are sampled by the rising edge of RX_CLK.
M7RXDV	183	I	Receive Data Valid.
M7RXCLK	182	I	Receive Clock.

Table 8: MII Interface Port 7 (Continued)

M7RXER	181	I	Receive Data Error.
M7CRS	170	I	Carrier Sense.
M7COL	172	I	Collision Detect.

Table 9: EEPROM Interface

PIN NAME	PIN NUMBER	I/O	DESCRIPTION
EEDIO	252	I/O	EEPROM Serial Data Input and Output.
EECLK	253	O	EEPROM Serial Clock.

Table 10: MII PHY Management Interface

PIN NAME	PIN NUMBER	I/O	DESCRIPTION
MDC	93	O	PHY Management Clock.
MDIO	94	I/O	PHY Management Data Input and Output.

Table 11: Power Interface

PIN NAME	PIN NUMBER	DESCRIPTION
GND	4, 6, 20, 22, 23, 24, 42, 44, 47, 49, 68, 70, 74, 76, 80, 100, 102, 104, 118, 120, 122, 144, 146, 165, 167, 168, 187, 189, 205, 208, 217, 232, 248	Ground
Vcc (3.3V)	10, 26, 28, 32, 45, 53, 71, 72, 90, 92, 108, 121, 124, 126, 147, 149, 151, 155, 169, 171, 173, 177, 190, 202, 224, 239, 246	3.3V Supply Voltage.
VccM	134	Supply Voltage for MII Interface. VccM = 5V (5V MII interface) VccM = 3.3V (3.3V MII interface)

Table 12: SGRAM Interface

PIN NAME	PIN NUMBER	I/O	DESCRIPTION
PBD31 PBD30 PBD29 PBD28 PBD27 PBD26 PBD25 PBD24 PBD23 PBD22 PBD21 PBD20 PBD19 PBD18 PBD17 PBD16 PBD15 PBD14 PBD13 PBD12 PBD11 PBD10 PBD9 PBD8 PBD7 PBD6 PBD5 PBD4 PBD3 PBD2 PBD1 PBD0	196 197 198 199 200 201 203 204 215 216 218 219 220 221 222 223 206 207 209 210 211 212 213 214 225 226 227 228 229 230 231 233	I/O	SGRAM Data Bus.
PBA9_10	244	O	SGRAM Address. For 16 Mbit/s SGRAM, this pin is PBA10 and for 8 Mbit/s SGRAM this pin is PBA 9.
PBA8_9	234	O	SGRAM Address. For 16 Mbit/s SGRAM, this pin is PBA9 and for 8 Mbit/s SGRAM this pin is PBA 8.
PBANC_8	255	O	SGRAM Address. For 16 Mbit/s SGRAM, this pin is PBA8 and unconnected when connected to 8 Mbit/s SGRAM.

Table 12: SGRAM Interface (Continued)

PBA7 PBA6 PBA5 PBA4 PBA3 PBA2 PBA1 PBA0	235 236 237 238 240 241 242 243	O	SGRAM Address line PBA0-PBA8 are sampled during the ACTIVE command (row address) and read/write command (column address with PBA8 defining auto precharge).
PBCS#	251	O	Chip Select. Enables and disables the command decoder of the SGRAM.
PBRAS#	245	O	SGRAM Row Address Strobe.
PBCAS#	250	O	SGRAM Column Address Strobe.
PBWE#	249	O	Write Enable.
PBCLKI	195	O	System Clock Output to drive the SGRAM.

Table 13: Miscellaneous Pins

PIN NAME	PIN NUMBER	DESCRIPTION
DEVID0 DEVID1	95 96	Device ID Number. For the AL102A, both pins should be connected to ground.
RESET#	97	Reset
TESTMODE	98	Test Mode Pin. This pin should be grounded for normal operation.
EPBYPASS	99	This pin bypasses the EEPROM setup. This pin should be tied to ground.
CLKIN	254	This pin should be tied to ground.
SYSCLK	247	75 MHz System Clock.
NC	1, 2, 62, 63, 64, 65, 66, 127, 128, 129, 130, 191, 192, 193, 194, 256	No Connect.

AL102A Interface Block Diagram

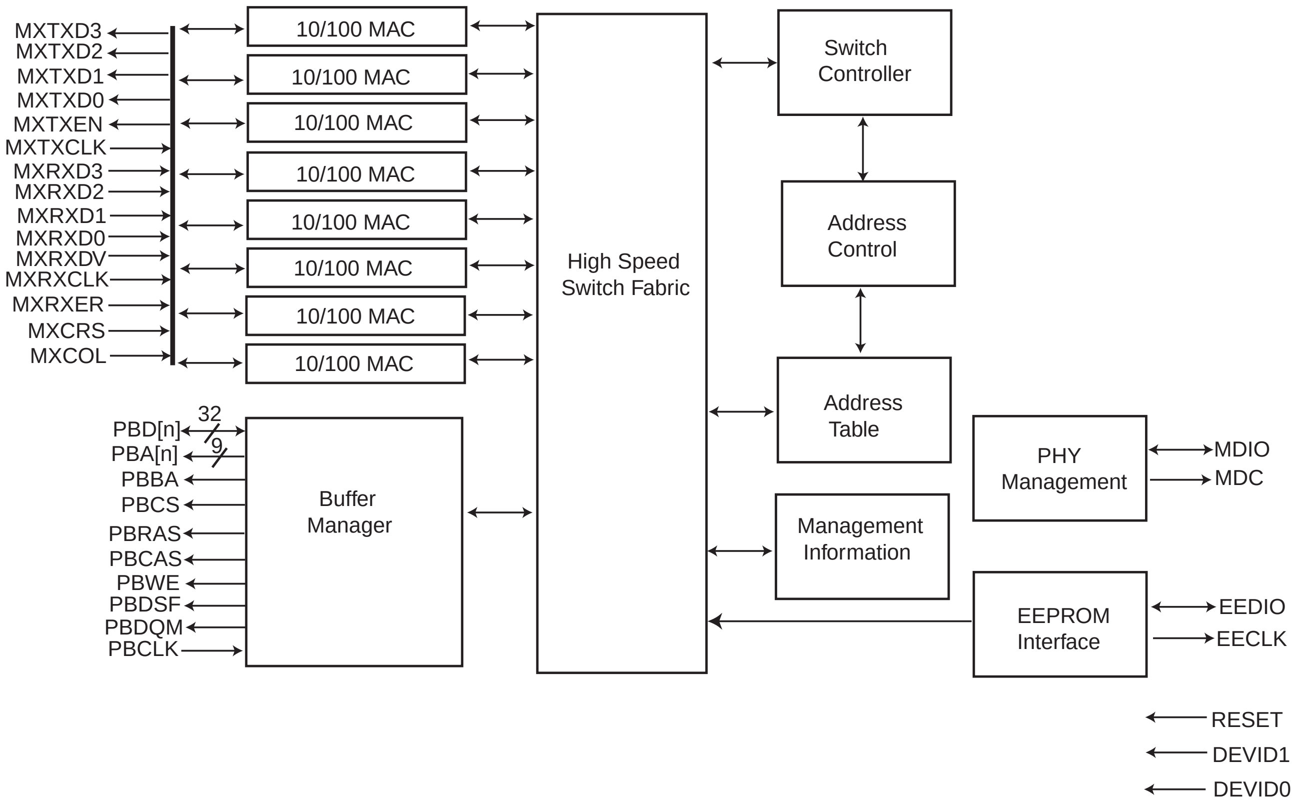


Figure 3 Interface Block Diagram

3. Functional Description

3.1 Data Reception

The port will go into the receive-state when RX_DV in the MII interface is asserted. The MII (Media Independent Interface) presents the received data in four-bit nibbles that are synchronous to the receive clock (25 MHz for 100 Mbit/s or 2.5 MHz for 10 Mbit/s). The AL102A will then attempt to detect the occurrence of the SFD (Start Frame Delimiter) pattern “10101011.” All preamble data prior to SFD are discarded. Once SFD is detected from the MII interface, the frame data is forwarded and stored in the buffer of the switch.

3.1.1 Illegal Frame Length

During the receiving process, the AL102A MAC will monitor the length of the received frame. Legal Ethernet frames should have a length of no less than 64 bytes and no more than 1536 bytes. Any frames with illegal frame length are discarded.

3.1.2 Long Frames

The AL102A can handle frame size up to 1536 bytes. All frames longer than 1536 bytes will be discarded. If the port continues to receive data after the 1536th byte, the port’s data will be filtered. If the port is in half-duplex mode, the port will no longer be able to transmit or receive data during the long frame reception.

3.1.3 False Carrier Events

If CRS (Carrier Sense) signal in the MII interface is asserted but the receive RX_DV (Receive Data Valid) signal is not asserted within 16BT (Bit Period), the port is considered to have a false carrier event. The false carrier event is recorded for the MIB counter.

3.1.4 Frame Filtering

The AL102A will make filtering and forwarding decisions for each frame received based on its frame routing table, VLAN Mapping, port state, and the system configuration.

Under the following conditions, received frames are filtered:

- The AL102A will check all received frames for errors such as symbol error, FCS error, short event, runt, long event, etc. Frames with any kind of error will not be forwarded to their destination port.
- Any frame heading to its own source port will be filtered.
- Frames heading to a disabled receiving port will be filtered.
- If the input buffer of the port is full, the incoming frame will be discarded. It is recommended that the flow control be used to prevent any loss of data. If the flow control option is enabled, this event will not occur. The remote station will transmit frame when the input buffer becomes available.
- If the frame has any security violation and the security option is enabled at the receiving port.

3.2 Frame Forwarding

After a frame is received, both source address (SA) and destination address (DA) are retrieved. The SA is used to update the port's address table and the DA is used to determine the frames destination port.

The Address Lookup Engine will attempt to match the destination address with the addresses stored in the address table. If there is a match found, a link between the source port and the destination port is then established.

If the first bit of the destination address is a "0," the frame is regarded as an unicast frame. The destination address is passed to the Address Lookup Engine, which returns a matched destination port number to identify which port the frame should be forwarded to. If the destination port is within the same VLAN of the receiving port, the frame will be forwarded. If the destination port does not belong to the VLANs specified at the receiving ports, the frame will be discarded. The event will be recorded as a VLAN boundary violation.

There are two ways that the AL102A handles frames with unknown destinations. The forwarding decision is controlled by the Flood Control option (System Configuration Register 00). If Flood Control is disabled, the frame will be forwarded to all ports (except the receiving port) within the same VLANs of the receiving port. If the Flood Control option is enabled, the AL102A will forward the frame only to the uplink port specified at the receiving port.

Note: The AL102A defines a port as either a single port or a trunk.

If the port monitoring function is enabled, the frame forwarding decision is also subject to the port monitoring configurations.

If the first bit of the destination address is a "1," the frame will be handled as a multicast or broadcast frame. The AL102A does not differentiate multicast frames from broadcast frames except for the reserved bridge management group address, as specified in table 3.5 of IEEE 802.1d standard. The destination ports of the broadcast frame are all ports within the same VLAN except the source port itself.

3.2.1 Broadcast Storm Control

One of the unique features provided by the AL102A is Broadcast Storm Control. This option allows the user to limit the number of broadcast frames into the switch. This option can be implemented on a per port basis. A threshold number of broadcast frames can be programmed in System Register II (register 01).

When Storm Control is enabled and the number of cumulated non-unicast frames is over the programmed threshold, the broadcast frame is discarded.

If Storm Control is disabled, or the number of non-unicast frames received is not over the programmed threshold, the AL102A will forward the frame to all ports (except the receiving port) specified within the VLANs at the receiving port.

If Broadcast-Storm-drop (BConly_SC) is enabled in System Register III (register 02), the AL102A will only drop broadcast frames but not the multicast frames.

3.2.2 Frame Transmission

The AL102A transmits all frames in accordance to IEEE 802.3 standards. The AL102A will send the frames with a guaranteed minimum IPG (Inter Packet/Frame Gap) of 96BT even if the received frames have an IPG less than the minimum requirement. The AL102A also supports transmission of frames with an IPG of 64BT (optional). This option can be selected in System Register III, (Bit 8, Register 02).

3.2.3 Frame Generation

During a transmit process the frame data is read from the memory buffer and forwarded to the destination port's PHY device in di-bits. Seven bytes of preamble signal (10101010) will be generated first before the SFD (10101011). Frame data is sent after the SFD along with four-bytes of FCS at the end.

3.3 Half Duplex Mode Operation

For half-duplex operation, the MAC logic will abort the transmit-process if collision is detected through the assertion of the collision (Col) signal by the MII. Re-transmission of the frame is scheduled in accordance to IEEE 802.3's truncated binary exponential back off algorithm. If the transmit process has encountered 16 consecutive collisions, an excessive collision error is reported and AL102A will not try to re-transmit the frame unless the retry-on-excessive-collision (REC) option is enabled. When REC is enabled, the number of collisions are reset to zero and transmission is started as soon as 96 bit-time of inter-packet gap is passed after the last collision. If a collision is detected after 512BT of the transmission, a late collision error will be reported but the frame will still be re-transmitted after proper back off time.

The AL102A also provides an option for an aggressive back off in the Port Configuration Register 01.3 (SuperMAC). This option allows the MAC to back off only three slots. This will create a more aggressive channel capture behavior than the standard IEEE back off algorithm.

3.4 Secure Mode Operation

The AL102A provides security support on a per port basis. Whenever the secure mode is enabled, the port will stop learning new addresses. The address table of each port will remain unchanged. In this mode of operation, the address lookup table will freeze and no additional new address will be learned.

The AL102A provides two levels of security protection. The most severe intrusion protection is disabling a port if intrusion is experienced. The security management (SecMgmt bit in register 01) will disable a port if a frame with unlearned source address (SA) is received from a secured port (security violation). Once a port is disabled, it can only be enabled by the network management. Security management is a global option.

An alternative is to enable security at the local port level without the security management. When the AL102A is configured this way, the device will only discard frames that have security violations, which prevents intruders from accessing the network.

3.5 Address Learning

The Table Lookup Engine provides the switching information required to route data frames. The address look up table is set-up through auto address learning (dynamic) or manual entry (static). The static addresses are assigned to the address table by the EEPROM. All static address entries will not be aged or updated by the AL102A.

After a frame is received by the AL102A, the embedded (SA) and destination address (DA) are retrieved. The source address retrieved from the received frame is automatically stored in a SA buffer. The AL102A will then check for error and security violations, and perform a SA search. If there is no error or security violation, the AL102A will store the source address in the address lookup table. If the SA has been previously stored in another port’s SA table, the AL102A will delete the SA from the previously stored location.

The Individual MAC Address is a 48-bit unique MAC address to be programmed or learned. Bit 0 of a SA will be masked, i.e. no multicast SA.

The AL102A provides an on-chip 1K MAC Address-to-PortID/TrunkID table for the frame destination look-up operations.

The AL102A address table contains both static addresses input by the EEPROM and dynamically learned address. It learns the individual MAC addresses from frame received with no errors from the local ports.

For received frames that contain a source address learned in another port’s address table, that hasn’t been aged out, perform the following based on the switches; if the security option is selected for the port, the AL102A considers this a security violation; if port is a non-protected port, the AL102A will delete the SA from the previous port’s address table and update it to the current port’s address table. However, if the SA is a static address entry, the address will not be updated.

3.5.1 Address Aging

A port’s MAC address register is cleared on power-up, or hardware reset. If the SA aging option is enabled, the dynamically learned SA will be cleared if it is not refreshed within the programmed time.

3.6 VLAN Support

Each port of the AL102A can be assigned to one or multiple VLANs. Frames from the source port will only be forwarded to destination ports within the same VLAN domain. A broadcast/multicast frame will be forwarded to all ports within the VLAN(s) except the source port itself. A unicast frame will be forwarded to the destination port only if the destination port is in the same VLAN as the source port. Otherwise, the frame will be treated as a frame with unknown DA. If the destination port belongs to the another VLAN, the frame will be discarded and the event will be recorded as a VLAN boundary violation.

Each port can be assigned with a dedicated uplink port. Unicast frames with unknown destination addresses will be forwarded to the uplink port of the source port. An uplink port can be either a single port or a trunk.

The AL102A provides one VLAN register per ports (register 1E to 2C) for mapping to eight-ports (eight-bits). Each register contains an eight-bit map to indicate the VLAN group for the port.

The VLAN registers hold a broadcast destination mask for each source port. The value “1” will indicate the broadcast frames will be routed from the source port to the specified port. Note that the source port bit must be set to “0” within the source port VLAN, because broadcast frames are not routed to the source port.

For setting up VLAN for trunking, please see the following section on trunking for detail.

VLAN Setup Example

A VLAN setup worksheet is provided in Appendix I. Simply marking the ports you wish to send broadcast frame to, you can complete the VLAN map easily.

For example, let’s assume we want to set up two VLAN groups in an 8-port switch:

Group 1 consists of: 0, 1, 2, 5, and 6.

Group 2 consists of: 2, 3, 4, and 7.

The completed VLAN bit maps is shown below. All other bits (15~8) not shown in the register, should be set to all “0.”

Table 14: VLAN Map for an 8-Port Switch

PORT	BIT	PORT 0/REG. 21	PORT 1/REG. 23	PORT 2/REG. 25	PORT 3/REG. 27	PORT 4/REG. 29	PORT 5/REG. 2B	PORT 6/REG. 2D	PORT 7/REG. 2F
7	7	0	0	1	1	1	0	0	0
6	6	1	1	1	0	0	1	0	0
5	5	1	1	1	0	0	0	1	0
4	4	0	0	1	1	0	0	0	1
3	3	0	0	1	0	1	0	0	1
2	2	1	1	0	1	1	1	1	1
1	1	1	0	1	0	0	1	1	0
0	0	0	1	1	0	0	1	1	0

3.7 Trunking (Port Aggregation)

The AL102A supports trunking/port aggregation. Port aggregation and trunking is essentially a method to treat multiple physical links as a single logical link. The benefit of trunking is the ability to group multiple lower speed links into one higher speed link. For example, four full-duplex 100 Mbit/s links can be used as one single 800-Mbps link. This is very useful for switch to switch, switch to server, and switch to router applications.

The AL102A considers a trunk as a single port entity regardless of the trunk composition. Two to four ports can be grouped together as a single trunk link. The grouping of the ports in the trunk must be from the top four ports or the bottom four ports of the device, i.e. port 0 to 3. A total of eight trunks can be supported by the RoX chip sets.

In a multiple link trunk, the links within the trunk should have a balanced amount of traffic in order to achieve maximum efficiency. One of the requirements for transmission is that the frames being transmitted must be in order. Therefore, some sort of load balancing among the links of the trunk must be deployed. The AL102A offers two methods of load balancing which can be selected in the System Configuration Register I (register 00).

3.7.1 Load Balancing

The two load-balancing methods that AL102A uses to support trunking are port based and MAC address based. Port based load balancing method is an explicit port assignment scheme. It requires each individual port be assigned to a specific link (trunk port) in the trunk. If the port is not assigned, the frame might be routed to the trunk randomly which may cause the frames to go out of order. The port based load balancing trunk can be assigned as a 2-, 3-, or 4-port trunk.

During transmission of the frame, it will be routed from the source port to the assigned trunk port. When a frame is received from any one of the trunk ports, it will be routed to the destination port within the VLAN. In essence, the AL102A treats a trunk as any single port within the same VLAN. If the ports traffic is evenly distributed among all the trunk ports, load balancing is achieved and the aggregate bandwidth of the trunk can be as high as 800 Mbit/s (full-duplex).

The alternative is the MAC address based load balancing. When the AL102A receives a frame with a trunk destination, it will automatically forward the frame to a port in the trunk based on the source MAC address. The MAC address load balancing decision is based on a proprietary algorithm. The algorithm assumes the trunk is a four port trunk. Therefore, if MAC address based load balancing is used, the trunk must consist of four ports. Use of MAC based load balancing in two or three port trunks could result in loss of frames.

3.7.2 Trunk Port Assignment

The maximum number of trunks for Allayer's RoX architecture is eight. The Port Configuration Registers (0D to 1C) provides the ability to designate a port to be a member of a trunk. The trunk can consist of up to four trunk ports. A trunk group must consist of either the top four ports or the bottom four ports. For example, a trunk can consist of either port 0, 1, 2, or 3, or port 4, 5, 6, or 7. Each trunk port's number is in sequence of 00, 01, 10, and 11 corresponding to the order of port of the devices. For example, port 1 and 5 are 01 (See Figure 4).

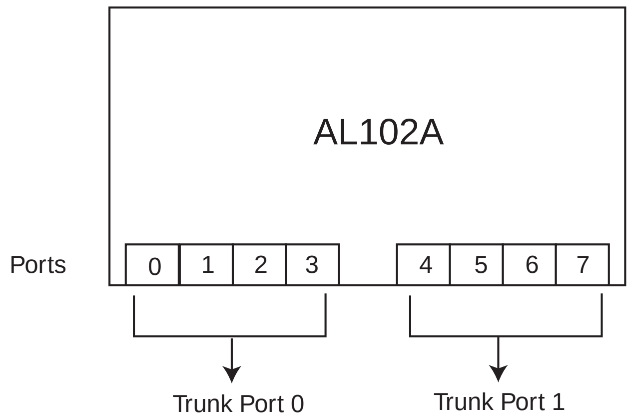


Figure 4 Trunk Port Numbering

3.7.3 Port Based Trunk Load Balancing

For port-based load balancing, a trunk port must be assigned to each port for all defined trunks. The port assignment is done by programming Port to Trunk Port registers (2D to 34). A port assignment worksheet is provided at the back of the data sheet. It is recommended that ports be evenly distributed among all trunk ports to prevent overloading any single trunk port.

Port Based Trunk Load Balancing Example

The example is for ports 3 and 4 as two-port trunk.

1. The desired trunk ports are 5, 6, and 7. Therefore, the port configuration register bits 15.9, 16.9, and 17.9 are set to 1.
2. We want to assign port 0 to trunk port 5, port 1 and 3 to trunk port 6, and port 2 and 4 to trunk port 7. Therefore, the port to trunk port register bits are as follows.

   08.2= 0, 08.3 =1

   09.2= 1. 09.3 =0

   10.2= 1, 10.3 =1

   11.2= 1. 11.3 =0

   12.2= 1, 12.3 =1
3. For the trunk ports, trunk ports should be assigned with their own the port number in the port to trunk port register. The port to trunk port bits.

13.2= 0, 13.3 =1

14.2= 1. 14.3 =0

15.2= 1, 15.3 =1

4. Assigning VLAN. The VLAN map is assigned as shown.

All bits are set to 1. The bits 21.1 and 21.0 are set to 0 because port 0 is assigned to port 5. All the other ports are set up similarly.

Table 15: VLAN Mapping for Port Based Load Balancing Trunk

PORT	BIT	PORT 0/REG. 1D	PORT 1/REG. 1F	PORT 2/REG. 21	PORT 3/REG. 23	PORT 4/REG. 25	PORT 5/REG. 27	PORT 6/REG. 29	PORT 7/REG. 2B
7	7	0	0	1	0	1	0	0	0
6	6	0	1	0	1	0	0	0	0
5	5	1	0	0	0	0	0	0	0
4	4	1	1	1	1	0	1	1	1
3	3	1	1	1	0	1	1	1	1
2	2	1	1	0	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1
0	0	0	1	1	1	1	1	1	1

3.8 Flow Control

The AL102A can operate at two different modes, half- and full-duplex. Each port can operate at either full- or half-duplex and be configured to have flow control enabled or no flow control independently on a per port basis.

3.8.1 Half Duplex Flow Control (Backpressure)

If the half-duplex flow control option is elected, backpressure will be used for flow control. Whenever the occupancy of the receiving frame buffer of a port is full, the MAC of the port will start sending JAM signal through the port. The remote station after sensing the JAM signal will defer transmission. Backpressure flow control is applied to ensure that there is no dropped frame. The AL102A supports two types of backpressure, collision based and carrier based.

Carrier based backpressure is generated by the AL102A, when the switch port's frame buffer is full. The AL102A will cease to jam the line, when the port has buffer space available for frame reception. The IPG of the jamming signal can be programmed be either 64BT or 96BT.

Collision Based backpressure is generated by the AL102A, only when the switch port receives a frame. The AL102A will cease to jam the line, when the line is idle.

The carrier based backpressure has several advantages over collision based backpressure.

1. Collision based backpressure can cause late collisions.
2. After 16 consecutive collisions, the MAC could drop frames. The AL102A has an option not to drop frame after 16 collisions. However, the end terminal may still drop frames.

Therefore, we recommend the use of carrier based back pressure as the preferred method for half-duplex flow control. In this mode of operation, we also recommend that the IPG of the JAM signal should be set at 64BT. This is because if the IPG is at 96BT, the far end terminal might still be able to transmit frame and cause collision. The excessive collision could cause frames to be dropped.

The AL102A also supports collision-based backpressure for customers that prefer collision based backpressure.

3.8.2 Full Duplex Flow Control (802.3x)

In the full-duplex mode, AL102A will transmit and receive the frame in accordance to 802.3x standards. The transmission channel and the receiving channel operate independently.

In the incoming direction, whenever the occupancy of the receiving frame buffer of a port is full, the MAC of the port will send out a PAUSE frame with its delay value set to maximum. The PAUSE frame will deter the any incoming frame from flowing into the port. After the occupancy of the receiving frame buffer is reduced below the FlowControlOff threshold, the MAC of the port will then send out a PAUSE frame with delay value set to zero, to resume receiving the incoming frame flow.

In the outgoing direction, whenever a incoming PAUSE frame with a non-zero delay value is received through a port, the MAC of the port will stop the next frame transmission after the ongoing frame transmission is finished, and start its pause timer. It will resume frame transmission either after the pause timer expired or when a PAUSE frame with a zero delay value is received.

When 802.3x flow control option is elected, the device will program the appropriate bit in the auto-negotiation capability field. When the AL102A is used in the full-duplex mode, it is recommended that flow control should be turned on. This is to prevent the buffer from overflow and loss of frames. If the connected device has no 802.3x capability, then the link is recommended to be set at half-duplex.

3.9 Queue Management

Each port of the AL102A has its own individual transmission and receive queues. All frames come into AL102A are stored into the shared memory buffer, and are lined up in the transmission queues of corresponding destination port.

Each port of the AL102A has an input frame queue, and a dedicated queue to buffer the locally generated management event messages.

Each output port maintains an output frame queue for, and a dedicated multicast queue for outgoing multicast frame parking. The transmit frame can be from one of two sources, local or from another device on the RoX ring. For an output queue, if the source selected is the multicast queue, the device will set up a channel to copy the frame in the head of the multicast queue to the output queue for transmission.

For an output queue, if the source selected is a local input queue, the device will set up a channel from the local DRAM buffer to the output queue upon the requested DRAM bandwidth is available.

For an output queue, if the source selected is from another device on the ring, the device will send a message, to that device, trying to set up a channel through the ring from the source input queue in that device to the local output queue.

For the multicast queue, if the source selected is a local input queue, the device will set up a channel from the local DRAM buffer to the multicast queue upon the requested DRAM bandwidth is available.

For the multicast queue, if the source selected is from another device on the ring, the device will send message to that device, trying to set up a channel through the ring from the source input queue in that device to the local multicast queue.

3.10 Uplink Port

The uplink port provides a means to connect the switch with a repeater hub, a workgroup switch, a router, or any type of interconnecting device compliance with IEEE 802.3 standards.

If flood control is enabled, the AL102A will send all frames with unmatched DA and multicast/ broadcast frames to the uplink port. It is very important that each port is assigned to an uplink port via the Port Configuration Register (0D to1C), or data frames might be lost. The uplink port should be configured to be within the same VLAN of the source port. If the uplink port is not a member of the VLANs, the broadcast or multicast frames will not be forwarded to its designated uplink port. Multiple VLANs can share the same uplink port.

The AL102A will direct the following frames to the uplink port:

- Frames with a unicast destination address that doesn’t match with any MAC address stored in the switch; and

- Frames with a broadcast/multicast destination address if the uplink port is in the same VLAN.

Note: When configuring an uplink port, the uplink port should designate itself as the uplink port.

For some applications, it might be desirable to configure a port to be a port without address learning capability. When a port is configured as such, that port becomes a “dumping” port for all frames with unknown DA.

An uplink port can be an individual port or trunk. It is recommended that the uplink port be set to the learning disabled state (Port Configuration Register 0D to 1C) to conserve MAC address table space.

3.11 Port Monitoring

The AL102A supports port monitoring. This feature provides complete network monitoring capability at 100 Mbit/s. A copy of egress (TX) data and ingress (RX) data of the monitored port is sent to their respective snooping ports.

The monitored port is selected by register 30. The AL102A allows transmit and receive data to be monitored by different snooping ports. The snooping ports are also selected by register 30.

Summary of Programmable Register

- Port Monitoring Register (register 0D) - this register selects the target monitored port and the snooping port. A five-bit Port_ID designates the port. The format of the Port_ID is [00].[Port_ID]. [00] is the device number and [Port_ID] is the port number.

3.12 Media Independent Interface (MII)

The MAC of each port of the AL102A is connected to the PHY through the standard MII interface. For receiving frames, the received data (RXD[3:0]) is sampled at the rising edge of the receive clock (RX_CLK). Assertion of the receive data valid (RX_DV) signal will cause the MAC to look for start of SFD. For transmission, the transmit data enable (TX_EN) signal is asserted when the first preamble nibble is sent on the transmit data (TXD[3:0]) lines. The transmit data is clocked out by the rising edge of the transmit clock (TX_CLK).

Prior to any transaction, the AL102A will output 32-bits of “1” as a preamble signal and then after the preamble, a “01” signal is used to indicate the start of the frame.

3.13 PHY Management

The AL102A supports transceiver management through the serial MDIO and MDC signal lines. The device provides two modes of management, master and slave mode. In the master mode of operation, the AL102A controls the operation modes of the link, but in the slave mode the PHY controls the operating mode.

3.13.1 PHY Management MDIO

For a write operation, the device will send a “01” to signal a write operation. Following the “01” write signal will be the five-bit ID address of the PHY device and the five-bit register address. A “10” turn around signal is then used to avoid contention during a read transaction. After the turn around, the 16-bit of data will be written into the register. After the completion of the write transaction, the line will be put in a high impedance state.

For a read operation, the AL102A will output a “10” to indicate read operation after the start of frame indicator. Following the “10” read signal will be the five-bit ID address of the PHY device and the five-bit register address. Then, the AL102A will cease driving the MDIO line, and wait for one bit time. During this time, the MDIO should be in a high impedance state. The device will then synchronize with the next bit of “0” driven by the PHY device, and continue on to read 16 bit of data from the register. The detail timing requirement on PHY management signals are described in the section “Timing Requirement.”

The MDIO port can be disabled through the use of port configuration register. This allows the engineers to use 100Base-TX transceiver without auto-negotiation capability or MII to MII interconnect. In this mode of operation, the PHY has no communication with the AL102A. Therefore, the AL102A will assert the link status as soon as initialization is completed and assumes the connected PHY is operating at the specified operating duplex mode and speed.

3.13.2 PHY Management Master Mode

In the master mode, the AL102A will continuously poll the status of the PHY devices through the serial management interface. The device will also configure the PHY capability fields to ensure proper operation of the link.

The configuration of the link is automatic. The link capability is programmed by the AL102A through the port configuration register. The AL102A reads from the standard IEEE PHY registers to determine the auto-negotiated operating speed and mode. If there is a need to manually set the operation mode because of flow control and cabling issues the AL102A can set the port operation mode through the MDIO interface (see EEPROM section for programming the AL102A).

3.13.3 PHY Management Slave Mode

In the slave mode, the PHY controls the programming of the operating mode. The AL102A will continuously poll the status of the PHY devices through the serial management interface to determine the operation mode of the link.

This mode of PHY management is very useful for unmanaged switch. The operating mode of the link can be changed by programming the mode pin of the PHY through a jumper.

The AL102A also supports 100Base-TX transceivers without a MDIO interface or MII to MII interface. When MDIO is disabled, the AL102A will operate in the operation mode specified in the Port Configuration Register (register 0D to 1C).

3.13.4 Non Auto-negotiation Mode

The AL102A can also turn off the auto-negotiation capability of the PHY. When auto-negotiation is turned off, the AL102A is in the slave mode and the transceiver will determine the link’s operating mode.

3.13.5 Other PHY Options

Some Legacy Fast Ethernet devices and other low cost devices have no auto-negotiation capability. In those cases when the transceiver will not be able to perform auto-negotiation, the switch transceiver will typically do a parallel detection and update the information in the transceiver's register. Unfortunately, such register addresses are vendor specific. The AL102A provides a register (register 05) to specify the register address of the PHY for the AL102A to read. The AL102A will read from that register and configure the port operation accordingly.

Register 05 also provides some additional flexibility's for some of the PHYs in the market. In general, the system designer should set the ID of the PHY devices as 0 for port 0, 1 for port 1, 7 for port 7, etc. Certain PHYs utilize PHY address 00000 as a broadcast address. Bit 1 of the register 05 allows the AL102A to start with PHY address 10000. This provision allows the engineers to work around the PHY's that have problems handling address 00000.

Quad PHYs may have two-port ordering in the chip pinout, both clockwise and counter clockwise. Register 05 bit 2, programs the AL102A port order to go in either direction. This provision enables engineers to easily implement designs with any PHY.

There is also a slow MDIO clock (17 KHz) available for PHY that is not capable of handling a high speed MDIO clock.

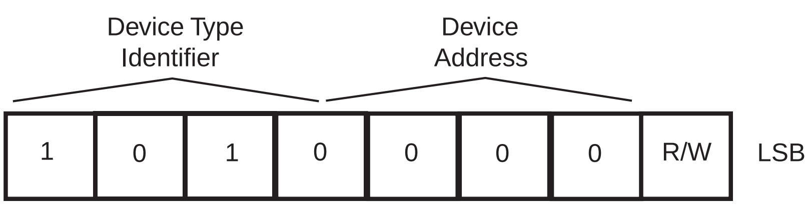
If for some reason, the transceiver is connected to a device and that device fails to auto-negotiate, the AL102A will default the data rate and duplex mode to the default setting in the port configuration register.

3.14 EEPROM Interface

The AL102A provides three functions with the EEPROM interface: system initialization, obtaining system status, and reconfiguring the system in real time. The AL102A uses the 24C02 serial EEPROM device (2048 bits organized as 256 bits x 8).

3.14.1 System Initialization

The EEPROM interface is provided so that the manufacturer can provide a pre-configured system to their customers which allows customers to change or reconfigure their system and retain their preferences. The EEPROM contains configuration and initialization information, which will be accessed at power up or reset.



If the reset pin is held low, the AL102A's EEPROM interface will go into a high impedance state. This feature is very useful for reprogramming the EEPROM during installation or reconfiguration.

The EEPROM can be reprogrammed by an external parallel port. For reprogramming using a parallel port, a signal is used to hold the RESET pin low. The EEPROM interface will then be in the high-impedance state. An external device can then program the EEPROM through the EEDIO and the EECLK pins. The EEPROM address should be set to 000.

3.14.2 Start and Stop Bit

The write cycle is started by a start bit and ended by a stop bit. A start bit is a transition from high to low of EEDIO when EEC is high. See Figure 5. The operation terminates when EEDIO goes from low to high when EEC is high. Following a start condition, the writing device must output the address of the EEPROM. The most significant four bit of the EEPROM address is the device type identifier which has an address of 1010. The EEPROM address should be set to be the same as the Device ID with A3 (EEPROM) grounded. For example, EEPROM of device 0 has an address of 000 and device 1 has and address of 001.

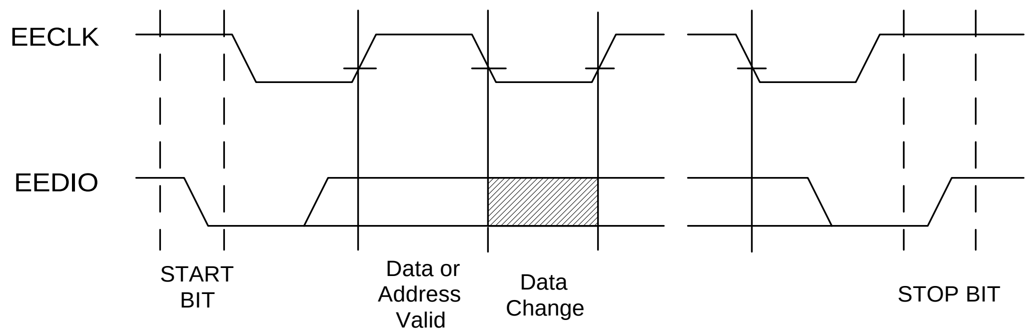


Figure 5 EEPROM Start and Stop Bit

3.14.3 Write Cycle Timing

The EECLK is an output from the AL102A while EEDIO is a bi-directional signal. When accessing the EEPROM, the reset pin has to be held low or initialization of the AL102A must be finished before a writing operation can begin. A typical write operation is shown in Figure 6.

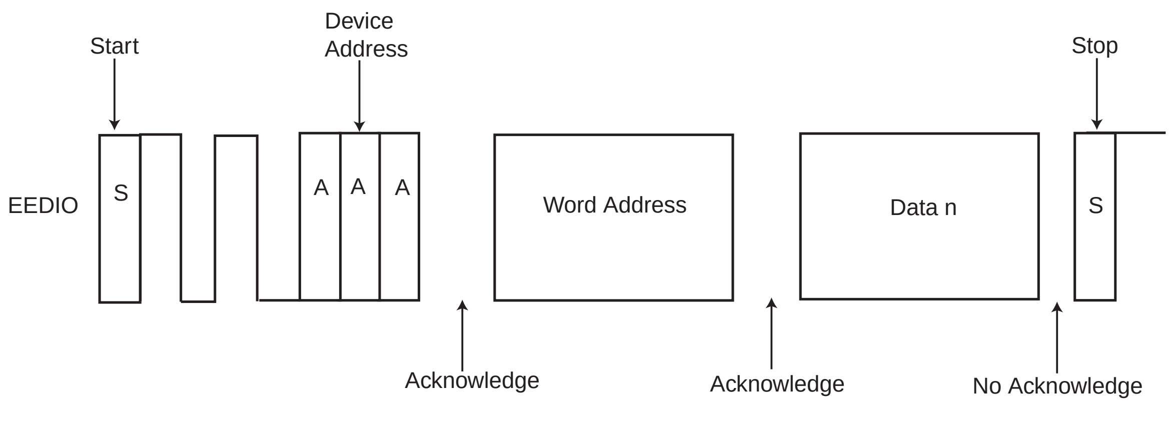


Figure 6 EEPROM Random Write Cycle

3.14.4 Read Cycle Timing

Read operations are initiated in the same manner as write operations, with the exception that the R/W bit of the EEPROM address is set to a "1."

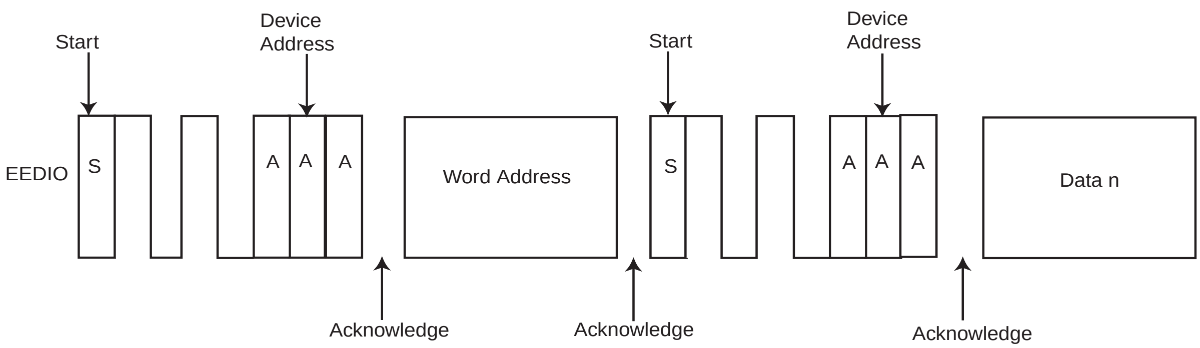


Figure 7 EEPROM Random Read Cycle

3.14.5 Reprogramming the EEPROM Configuration

There are two ways that the system can be reconfigured. Figure 8 shows an application using the parallel interface to reprogram the EEPROM. In this application, the parallel port holds the reset pins low, which forces the EEDIO pins to go in to high impedance. Once the pins are in high impedance, the EEPROM can now be programmed by the parallel port. Once the parallel port releases the reset pins, the devices will start to download the EEPROM data and reconfigure the devices.

An alternate way of reconfiguring the system is to directly change the register settings of the AL102A. After initialization, the EEPROM interface can act as a virtual EEPROM. In order for this method to work, the EEPROM's device address must be 000, while the AL102A's address will be 100. The customer can now program the AL102A as an EEPROM. The read and write timing is the same as an EEPROM.

Because you read as well as write to the AL102A, the registers status can be read from the AL102A. This will serve as a very useful tool for diagnostic of an unmanaged switch.

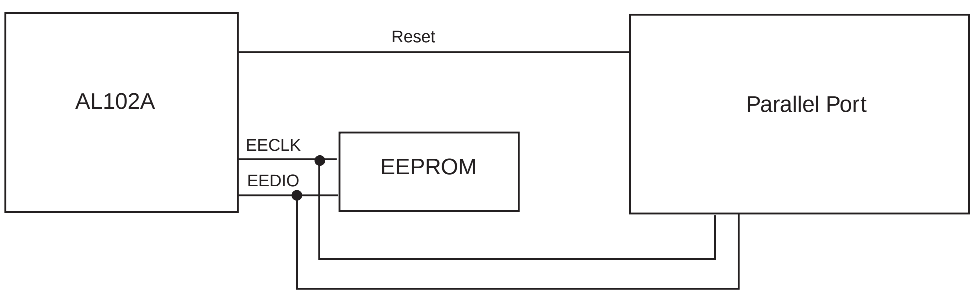


Figure 8 EEPROM Parallel Port

3.14.6 EEPROM Map

Table 16 shows the EEPROM address map cross-referenced to the register/bit set of the AL102A. Addresses 00 through 6D are for configuring the device. They are downloaded by the AL102A after reset or power up. Since the AL102A registers are 16-bit wide, it takes two EEPROM addresses for each AL102A register. Even numbered EEPROM addresses corresponds to the upper byte of the AL102A registers while the odd numbered EEPROM addresses corresponds to the lower byte of the AL102A registers.

Note: The specific bits in the register are reference by a “X.Y” notation, where X is the register number and Y is the bit number.

Address 06 and 07 should be programmed as 0000 0001 and 0001 0100. The address 6F indicates the last address entry. If no static address is used in the switch, the address 6F should be programmed. Addresses 70 to FF are used for programming the static address entry.

The following format is an example of Static Entry 1, Address 70-77.

Table 16: Static Address Entry Format for EEPROM

EEPROM ADDRESS	BIT							
	7	6	5	4	3	2	1	0
70	Reserved (Must be all zero)							
71	Reserved		Port ID YXXXXX or Trunk ID YXXYYY					
72	MAC Address [47:40]							
73	MAC Address [39:32]							
74	MAC Address [31:24]							
75	MAC Address [23:16]							
76	MAC Address [15:8]							
77	MAC Address [7:0]							

YXX represents:

Y = 0 then XX [port_ID] represents the five-bit individual port ID number

Y = 1 then XX = 00 [port_ID] represents the trunk ID number (0-1)

If XX = 11, then this represents the CPU port and [port_ID] is a don’t care.

Table 17: AL102A EEPROM Mapping

EEPROM PHYSICAL ADDRESS	DESCRIPTION	AL102A REGISTER/BIT
00	System Configuration I [15:8]	00.15 to 00.8
01	System Configuration I [7:0]	00.7 to 00.0
02-03	System Configuration II	01.15 to 01.0
04-05	System Configuration III	02.15 to 02.0
06-07	0000 0001 0001 0100	03.15 to 03.0
08-09	Reserved	04.15 to 04.0
0A-0B	Vendor Specific PHY	05.15 to 05.0
0C-0D	Snooping Port Configuration	06.15 to 06.0
0E-0F	Monitored Src Host I [47:32]	07.15 to 07.0
10-11	Monitored Src Host II [31:16]	08.15 to 08.0
12-13	Monitored Src Host III [15:0]	09.15 to 09.0
14-15	Monitored Dst Host I [47:32]	0A.15 to 0A.0
16-17	Monitored Dst Host II [31:16]	0B.15 to 0B.0
18-19	Monitored Dst Host III [15:0]	0C.15 to 0C.0
1A-1B	Port 0 Configuration I	0D.15 to 0D.0
1C-1D	Port 0 Configuration II	0E.15 to 0E.0
1E-1F	Port 1 Configuration I	0F.15 to 0F.0
20-21	Port 1 Configuration II	10.15 to 10.0
22-23	Port 2 Configuration I	11.15 to 11.0
24-25	Port 2 Configuration II	12.15 to 12.0
26-27	Port 3 Configuration I	13.15 to 13.0
28-29	Port 3 Configuration II	14.15 to 14.0
2A-2B	Port 4 Configuration I	15.15 to 15.0
2C-2D	Port 4 Configuration II	16.15 to 16.0
2E-2F	Port 5 Configuration I	17.15 to 17.0
30-31	Port 5 Configuration II	18.15 to 18.0
32-33	Port 6 Configuration I	19.15 to 19.0

Table 17: AL102A EEPROM Mapping (Continued)

34-35	Port 6 Configuration II	1A.15 to 1A.0
36-37	Port 7 Configuration I	1B.15 to 1B.0
38-39	Port 7 Configuration II	1C.15 to 1C.0
3A-3B	Port 0 VLAN Map I	1D.15 to 1D.0
3C-3D	Port 0 VLAN Map II	1E.15 to 1E.0
3E-3F	Port 1 VLAN Map I	1F.15 to 1F.0
40-41	Port 1 VLAN Map II	20.15 to 20.0
42-43	Port 2 VLAN Map I	21.15 to 21.0
44-45	Port 2 VLAN Map II	22.15 to 22.0
46-47	Port 3 VLAN Map I	23.15 to 23.0
48-49	Port 3 VLAN Map II	24.15 to 24.0
4A-4B	Port 4 VLAN Map I	25.15 to 25.0
4C-4D	Port 4 VLAN Map II	26.15 to 26.0
4E-4F	Port 5 VLAN Map I	27.15 to 27.0
50-51	Port 5 VLAN Map II	28.15 to 28.0
52-53	Port 6 VLAN Map I	29.15 to 29.0
54-55	Port 6 VLAN Map II	2A.15 to 2A.0
56-57	Port 7 VLAN Map I	2B.15 to 2B.0
58-59	Port 7 VLAN Map II	2C.15 to 2C.0
5A-5B	Reserved	
5C-5D	Checksum	47
5E-5F	Port 0 to Trunk Port Assignment	2D.15 to 2D.0
60-61	Port 1 to Trunk Port Assignment	2E.15 to 2E.0
62-63	Port 2 to Trunk Port Assignment	2F.15 to 2F.0
64-65	Port 3 to Trunk Port Assignment	30.15 to 30.0
66-67	Port 4 to Trunk Port Assignment	31.15 to 31.0
68-69	Port 5 to Trunk Port Assignment	32.15 to 32.0
6A-6B	Port 6 to Trunk Port Assignment	33.15 to 33.0
6C-6D	Port 7 to Trunk Port Assignment	34.15 to 34.0
6E	Reserved	

Table 17: AL102A EEPROM Mapping (Continued)

6F	Last Entry Address	
70-71	Static Entry 1 (Port Number)	
72-73	Static Entry 1 (MAC [47:32])	
74-75	Static Entry 1 (MAC [31:16])	
76-77	Static Entry 1 (MAC [15:0])	
78-7f	Static Entry 2	
80-87	Static Entry 2	
88-8f	Static Entry 4	
90-97	Static Entry 5	
98-9f	Static Entry 6	
A0-A7	Static Entry 7	
A8-AF	Static Entry 8	
B0-B7	Static Entry 9	
B8-BF	Static Entry 10	
C0-C7	Static Entry 11	
C8-CF	Static Entry 12	
D0-D7	Static Entry 13	
D8-DF	Static Entry 14	
E0-E7	Static Entry 15	
E8-EF	Static Entry 16	
F0-F7	Static Entry 17	
F8-FF	Static Entry 18	

3.15 SGRAM Interface

All ports of AL102A work in Store-And-Forward mode so that all ports can support both 10 Mbit/s and 100 Mbit/s data speed. The AL102A utilizes a central memory buffers pool, which is shared by all ports within the same device. After a frame is received, it is passed across the SGRAM interface and stored in the buffer.

During transmit, the frame is retrieved from the buffer pool and forwarded to the destination port.

The AL102A is designed to use 8-Mbit SGRAM or 16-Mbit SGRAM for cost and performance.

The SGRAM is accessed in page burst access mode for very high speed access. This burst mode is repeatedly access to the same column. If burst mode reaches end of the column address, then it wraps around to the first column address (=0) and continues to count until interrupted by the news read/write, pre-charge, or burst stop command.

The AL102A will initialize the SGRAM automatically. It pre-charges all banks and inserts 8 auto–refresh commands. It will also program the mode registers for the AL102A read and write operations.

SGRAM essentially is a SDRAM. Dynamic memories must be refreshed periodically to prevent data loss. The SGRAM uses refresh address counters to refresh automatically. The SGRAM Auto-refresh command generates a pre-charge command internally in the SGRAM. The AL102A will insert an auto-refresh command once every 15 us.

During transmit, the frame is retrieved from the buffer pool and forwarded to the destination port.

4. Register Descriptions

Table 18: Register Table Summary

REGISTER ID	REGISTER DESCRIPTION
00	System Configuration I
01	System Configuration II
02	System Configuration III
03	Reserved
04	Reserved
05	Vendor Specific PHY Status
06	Port Monitoring Configuration
07	Monitored Source Host I [47:32]
08	Monitored Source Host II [31:16]
09	Monitored Source Host III [15:0]
0A	Monitored Destination Host I [47:32]
0B	Monitored Destination Host II [31:16]
0C	Monitored Destination Host III [15:0]
0D	Port 0 Configuration I
0E	Port 0 Configuration II
0F	Port 1 Configuration I
10	Port 1 Configuration II
11	Port 2 Configuration I
12	Port 2 Configuration II
13	Port 3 Configuration I
14	Port 3 Configuration II
15	Port 4 Configuration I
16	Port 4 Configuration II
17	Port 5 Configuration I
18	Port 5 Configuration II
19	Port 6 Configuration I
1A	Port 6 Configuration II

Table 18: Register Table Summary (Continued)

1B	Port 7 Configuration I
1C	Port 7 Configuration II
1D	Port 0 VLAN Map I
1E	Reserved
1F	Port 1 VLAN Map I
20	Reserved
21	Port 2 VLAN Map I
22	Reserved
23	Port 3 VLAN Map I
24	Reserved
25	Port 4 VLAN Map I
26	Reserved
27	Port 5 VLAN Map I
28	Reserved
29	Port 6 VLAN Map I
2A	Reserved
2B	Port 7 VLAN Map I
2C	Reserved
2D	Port 0 to Trunk Port Assignment
2E	Port 1 to Trunk Port Assignment
2F	Port 2 to Trunk Port Assignment
30	Port 3 to Trunk Port Assignment
31	Port 4 to Trunk Port Assignment
32	Port 5 to Trunk Port Assignment
33	Port 6 to Trunk Port Assignment
34	Port 7 to Trunk Port Assignment
35	Reserved
36	Reserved
37	Reserved
38	Reserved

Table 18: Register Table Summary (Continued)

39	System Status Register
3A	Port 0 Operation Status
3B	Port 1 Operation Status
3C	Port 2 Operation Status
3D	Port 3 Operation Status
3E	Port 4 Operation Status
3F	Port 5 Operation Status
40	Port 6 Operation Status
41	Port 7 Operation Status
42~47	Reserved

System Configuration Register I (Register 00)

The registers 01 to 03 are global system configuration registers. The option selected in this register affect the overall system operation.

Table 19: System Configuration Register I (Register 00)

BIT	NAME	DESCRIPTION
15	Reserved	Set all to zero.
14	FloodCtl	Flooding Control. Control for the forwarding of unicast frames with unknown destinations received from the non-uplink ports. 0: Disable. Frames received with an unknown unicast destination MAC address will be forwarded to all the ports (excluding the receiving port) within the VLANs specified at the receiving port. 1: Enable. Frames received with an unknown unicast destination MAC address will be forwarded to the uplink port specified for the receiving port.
13	SecMgmt	Security Enforcement. 0: Security Off. The security violation at a secured port will not change its port state. 1: Security On. The security violation at a secured port will change the port into the DISABLE state.
12	AgeEn	Switch Table Entry Aging Control. 0: Disable. The table aging process will be stopped. 1: Enable. The table aging process will be running to age every dynamically learned table entries.
11	TCNVG	Table Convergence Control. Set all to zero.

Table 19: System Configuration Register I (Register 00) (Continued)

10	Reserved	Set all to zero.
9	PInMon	Port Incoming Frame Flow Monitoring Enable Cable. 0: Disable 1: Enable
8	POutMon	Port Outgoing Frame Flow Monitoring Enable Cable. 0: Disable 1: Enable
7~4	Reserved	Set all to zero.
3	L2Trunk	Layer 2 Trunk Loading Method. 0: Port based loading. Trunking decisions will be based on trunk port assignment registers. 1: MAC address based loading. Trunking decisions will be based on source port MAC addresses.
2	TimeoutEN	Frame Time Out Enable. 0: Device will not timeout frames based on MaxDelay. 1: Device will timeout frames.
1~0	Reserved	Reserved or factory use. Bits should be set to 0.

Table 20: System Configuration Register II (Register 01)

BIT	NAME	DESCRIPTION
15~8	MaxAge	Maximum age for dynamically learned MAC entries. 0000 0000: 1 sec. to 1111 1111: 256 sec.
7~6	MaxDelay	Maximum frame transition delay through the switch. 00: 1 second 01: 2 seconds 10: 3 seconds 11: 4 seconds
5~4	MaxStorm	Maximum number of broadcast frames that can be accumulated in each input frame buffer. 00: 16 frames 01: 32 frames 10: 48 frames 11: 64 frames
3	SuperMAC	0: Disable. Device will perform the IEEE standard exponential back off algorithm when a collision occurs. 1: Enable. When collisions occur, the AL102A will back off up to 3 slots.
2	REC	Retry on Excessive Collision. 0: Normal collision handling. 1: Retry transmission after 16 consecutive collisions.

Table 20: System Configuration Register II (Register 01)

1~0	L2TbitSel	Select the bits position for MAC address to trunk assignment. 00: Source MAC Address [1:0] 01: Source MAC Address [3:2] 10: Source MAC Address [5:4] 11: Source MAC Address [7:6]

Table 21: System Configuration Register III (Register 02)

BIT	NAME	DESCRIPTION
15~12	Reserved	Reserved (Must set to 0).
11	RegPg	0: First page. 1: Second page.
10	SlowAge	0: Normal aging. 1: Slow down aging.
9	BpIPG84	Backpressure IPG Select Enable. 0: IPG = 96BT. 1: IPG = 64BT.
8	IPG64	IPG Control. 0: IPG = 96BT. 1: IPG = 64BT.
7~6	Reserved	Reserved (Must set to 0).
5	SG16M	SGRAM Select. 0: 8 Mbit SGRAM. 1: 16 Mbit SGRAM.
4	BPCOL	Back Pressure Control. 0: Carrier based. 1: Collision based.
3~1	Reserved	Reserved (Must set to 0).
0	FlowCtrlBC	0: Flow control multicast. 1: Flow control broadcast.

Reserved Register (Register 03)

This register is reserved for Allayer's use. The bits should be set as 0000 0001 0001 0100.

Reserved Register (Register 04)

This register is reserved for Allayer's use. The bits should be set as 0000 0000 0000 1000.

Vendor Specific PHY Register (Register 05)

This register is used to program vendor specific PHY options. It is also used for programming the Vendor Specific PHY register location and bit location of the operation status.

Table 22: Vendor Specific PHY Register (Register 05)

BIT	NAME	DESCRIPTION
15	PHYAD	Setting this bit to 1 will program the MDIO PHY address to addresses 16 to 23.
14	MClkSpd	Setting this bit to 1 will reduce the MDIO clock speed to 17 HKz.
13	PortOrder	Setting this bit to 1 will reverse the PHY ID/port number of the switch.
12~8	PHYOpReg	PHY's Operation Status Register Number.
7~4	PHYSpBit	PHY's Data Rate Status Register Bit Number.
3~0	PHYDxModeBit	PHY's Operating Duplex Mode Status Register Bit Number.

Port Monitoring Configuration Register (Register 06)

This register configures port monitoring. It sets the monitored port and the TX and RX snooping ports.

Table 23: Port Monitoring Configuration Register (Register 06)

BIT	NAME	DESCRIPTION
15	Reserved	Bit should be set at 0.
14~10	MdPID	Monitored Port ID.
9~5	MgIPID	Snooping Port ID for Incoming Frame Flow.
4~0	MgOPID	Snooping Port ID for Outgoing Frame Flow.

RMON Source and Destination Registers (Registers 07 to 0C)

These registers are used by the RMON manager for frame counting. The RMON manager counts the frames to (destination) and from (source) these MAC addresses stored in the register.

The 48-bit MAC address is programmed in three separate registers. Source MAC address is stored in registers 07 to 09 and destination MAC address in register 0A to 0C.

Table 24: RMON Source and Destination Registers (Registers 07 to 09)

REGISTER	BIT	NAME	DESCRIPTION
07	15~0	SRCMAC [47:32]	Monitored Source Host MAC Address
08	15~0	SRCMAC [31:16]	Monitored Source Host MAC Address
09	15~0	SRCMAC [15:0]	Monitored Source Host MAC Address

Table 25: RMON Source and Destination Registers (Registers 0A to 0C)

REGISTER	BIT	NAME	DESCRIPTION
0A	15~0	DSTMAC [47:32]	Monitored Destination Host MAC Address
0B	15~0	DSTMAC [31:16]	Monitored Destination Host MAC Address
0C	15~0	DSTMAC [15:0]	Monitored Destination Host MAC Address

Port Configuration Registers (Registers 0D to 1C)

Registers 0D to 1C are for local port configuration. There are two port configurations per port. The port configuration for Port 0 uses register 0D and 0E, Port 1 register 15 and 16, etc.

Port Configuration Register I

- Uplink ID - this is a six-bit link ID to assign an uplink port to the local port. The uplink port can be one of three types; a single port, a trunk, or a CPU port.

  If the uplink is a single port, the format of the port is [0][Dev_ID][Port_ID].

  If the uplink is a trunk, then the bits should read [100][trunk number]. The trunk number is numbered [Dev_ID][Trunk_ID].

  If the local port is an uplink port, the uplink ID should be its own port ID. Any frame with unlearned SA will then be filtered.

Table 26: Port Configuration Register I

BIT	NAME	DESCRIPTION
15~10	UpLinkID	Uplink ID associated with the port. 0XXYYY: Port ID with XX as the device ID and YYY as the port ID. 100XXN: Trunk ID with XX as the device ID and N as the trunk ID. 111XXX: The CPU port. Others: Reserved.
9	Tmember	Trunk Member Port. 0: Individual port. 1: Member of trunk port.
8	Reserved	Bit should be set to zero.
7	StormCTL	Broadcast Storm Control Enable. 0: Storm control disable. The broadcast frame will not be throttled. 1: Storm control enable. If the accumulated number of broadcast frames in the input buffer of the port is over the threshold specified in the system configuration register, new incoming broadcast frames will be discarded until the number has been reduced below the threshold.
6	Security	Intrusion Protection. Provides security control for the frames received from non-uplink ports. 0: Security Off. The forwarding decision made about frames received from the port will not involve the source MAC address checking. 1: Security On. The frames received from the port with an unknown source MAC address or with source MAC address learned previously from another port will be discarded.
5	CPUOn	The CPU Port VLAN Membership. Set all to zero.
4	LrnDis	Learning Disable. 0: Source address from this port will be learned. 1: Source address from this port will not be learned.
3~2	PortST	Port State Control. 00: Disable. All incoming frames from the PHY will be discarded; all outgoing frames will be masked from the path to the PHY. 01: Blocking-N-Listening. All incoming frames except incoming BPDUs from the PHY will be discarded; all outgoing frames except outgoing BPDUs will be masked from the path to the PHY. 10: Learning. All incoming frames from the PHY will be learned about their source information; all incoming frames except incoming BPDUs from the PHY will be discarded after being learned; all outgoing frames except outgoing BPDUs will be masked from the path to the PHY. 11: Forwarding. All incoming frames from the PHY will be learned from their source information; all incoming frames will be forwarded based on the switch routing decision; all outgoing frames will be transmitted to the PHY.
1~0	Reserved	Reserved (Must set to 0)

Table 27: Port Configuration Register II

BIT	NAME	DESCRIPTION
15~12	Reserved	Reserved
11	FlowCtrlFdEn	Flow Control Full Duplex Enable.
10	FlowCtrlHdEn	Flow Control Half Duplex Enable.
9~6	MDIOCfg [3:0]	MDIO Configuration. 0001: Master mode PHY management. 0010: Slave mode PHY management. 0111: Force mode.
5	MDIODis	MDIO Disable. 0: MDIO is enabled. 1: MIDO is disabled.
4	LinkUp	This bit is not relevant when MDIO is enabled. When MDIO is disabled, this bit forces the port into link up or link down state. 0: Link Down. 1: Link Up.
3	PrtMode100F	100 Full Duplex Mode.
2	PrtMode100H	100 Half Duplex Mode.
1	PrtMode 10F	10 Full Duplex Mode.
0	PrtMode 10H	10 Half Duplex Mode.

Port VLAN Map Registers (Registers 1D to 2C)

These registers provide the VLAN map for each port.

A VLAN worksheet is provided in Appendix I.

Table 28: Port VLAN Map Registers (Registers 1D to 2C)

REGISTER	BIT	NAME	DESCRIPTION
1D Port0 1F Port1 21 Port2 23 Port3 25 Port4 27 Port5 29 Port6 2B Port7	7 6 5 4 3 2 1 0	Dev0Map	Port VLAN Map corresponding to the port7~port0 of the device with Dev_ID of 00. 0: Non-member port. 1: Member port.

Port Trunk Port Assignment Registers (Registers 2D to 34)

The Port to Trunk Port assignment register assigns a port to a trunk for port-based load balancing trunking. Please see example in the trunking section.

A port to trunk port work sheet is provided in Appendix II.

Table 29: Port Trunk Port Assignment Registers (Registers 2D to 34)

BIT	NAME	DESCRIPTION
15~4	Reserved	Reserved (Must set to 0).
3~2	Trunk 1	Trunk Port of Trunk 1. 00: Port 4, 01: Port 5 10: Port 6, 11: Port 7
1~0	Trunk 0	Trunk Port of Trunk 0. 00: Port 0, 01: Port 1 10: Port 2, 11: Port 3

Table 30: System Status Register (Register 39)

BIT	NAME	DESCRIPTION
15	Reserved	Reserved (Must set to 0)
14	CheckSumEr	EEPROM Checksum Error.
13	SGRAMinit	SGRAM Initialization Done.
12	SRAMinit	SRAM Initialization Done.
11	REGinit	Register Initialization Done.
10~7	Traffic Counter	Traffic Counter.
6~4	Reserved	
3~0	Chip ID	0000: AL102A

Port Operation Status Registers (Register 3A to 41)

Registers 3A to 41 are status indication on a per port basis. These are read only register. Port 0 port status is in register 3A; Port 1~3E, Port 2~3F, Port3~40, and Port 4~41.

Table 31: Port Operation Status Registers (Register 3A to 41)

BIT	NAME	DESCRIPTION
15	LinkFail	Port Link Status. 0: Normal 1: Fail
14	PHYError	Port PHY Status. 0: Normal 1: Error
13	Sviolation	Port Security Violation. 0: Normal 1: Violation
12	FlowCtrl	Flow Control. If port mode ([1:0]) is 2’b01 or 2’b11: 0: Pause disable. 1: Pause enable. If port mode ([1:0]) is 2’b00 or 2’b10: 0: Back pressure based on CRS. 1: Back pressure based on collision.
11	Stormed	Port Broadcast Storm Status. 0: Normal 1: Stormed
10	InBFull	Port Input Buffer Full Status. 0: Normal 1: Input buffer full experienced.
9	TblUNAVL	Table Entry Unavailability for MAC Learning. 0: Normal 1: Unavailability experienced.
8	Jabbered	Port Jabber Status. 0: Normal 1: Jabber experienced.
7	LateCOL	Port Late Collision Status. 0: Normal 1: Late collision experienced.
6	TxPaused	Port Transmit Pause Status. 0: No transmit pause experienced. 1: Transmit pause experienced.

Table 31: Port Operation Status Registers (Register 3A to 41) (Continued)

5	CRSLoss	Port Carrier Sense Loss During Transmission Status. 0: No carrier sense loss experienced. 1: Carrier sense loss experienced.
4	FalseCRS	False Carrier Status.
3	Underflow	Transmit Queue Underflow Status. 0: Normal 1: Underflow experienced.
2	TimeOut	Frame Time Out. 0: Normal 1: Frame time out experienced.
1~0	PortMode	Port Operating Mode. 00: 10 Mb half-duplex. 01: 10 Mb full-duplex. 10: 100 Mb half-duplex. 11: 100 Mb full-duplex.

Indirect Resource Access Command Register (Register 42)

The indirect resource access command allows the management (Reverse EEPROM Method) to access other resources other than the AL102A register values. PHY registers, both internal and external MAC address tables, and SGRAM contents can be accessed using this command.

Table 32: Indirect Resource Access Command Register (Register 42)

BIT	NAME	DESCRIPTION
15	CmdDone	Command Done. 0: Execute new command. 1: Command done. Clear this bit to execute a new command. When finished with the command, the AL102A will set the bit back to “1”.
14	Operation	Read/Write Operation Command. 0: Read operation. 1: Write operation.
13~11	ResType	Accessed Resource Type. 000: PHY registers. 001: EEPROM. 010: SGRAM. 011: MAC address table 1; Read: MAC table address read. Write: MAC address learn. 100: MAC address table 2; Read: MAC address search. Write: MAC address delete. 101-111: Reserved

Table 32: Indirect Resource Access Command Register (Register 42)

10	ExtRD	External MAC Address Table Read. If ResType = 011 and Operation = 0 0: On-chip address table read. 1: Off-chip address table read.
9~0	ResAddr	The address of the entry within the accessed resource.

Indirect Resource Access Data I Register (Register 43)

Indirect Resource Access Data I through IV are used with indirect resource access command.

Table 33: Indirect Resource Access Data I Register (Register 43)

BIT	NAME	DESCRIPTION
15~0	IRAData	Indirect Resource Access Data 1.

Table 34: Indirect Resource Access Data II Register (Register 44)

BIT	NAME	DESCRIPTION
15~0	IRAData	Indirect Resource Access Data 2.

Table 35: Indirect Resource Access Data III Register (Register 45)

BIT	NAME	DESCRIPTION
15~0	IRAData	Indirect Resource Access Data 3.

Table 36: Indirect Resource Access Data IV Register (Register 46)

BIT	NAME	DESCRIPTION
15~0	IRAData	Indirect Resource Access Data 4.

Table 37: Check Sum (Register 47)

BIT	NAME	DESCRIPTION
15~8	CheckSum	Checksum value of AL102A register contents.
7~0	Reserved	

5. Timing Requirements

Table 38: MII Transmit Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{tdv}	TXCLK to TXD valid time.	4	-	12	ns
t_{txev}	TXCLK to TXEN valid time.	4	-	12	ns

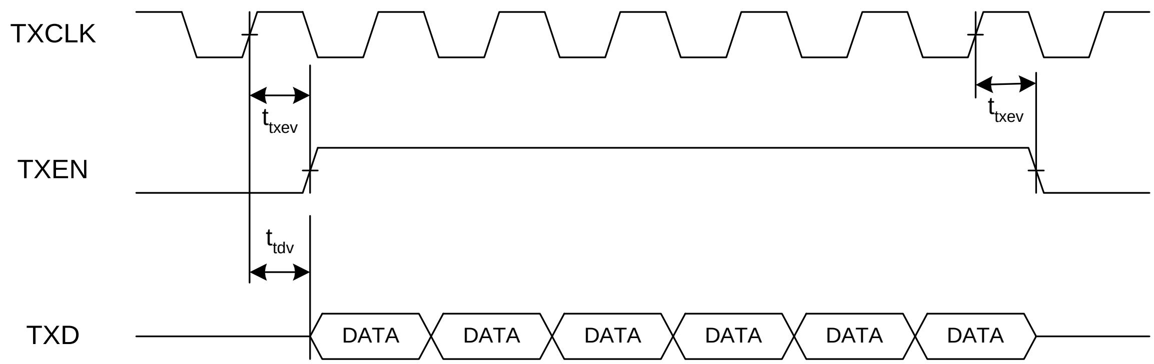


Figure 9 MII Transmit Timing

Table 39: MII Receive Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{rxds}	RX_DV, RXD, RX_ER, setup time.	10	-	-	ns
t_{rxdh}	RX_DV, RXD, RX_ER hold time.	5	-	-	ns

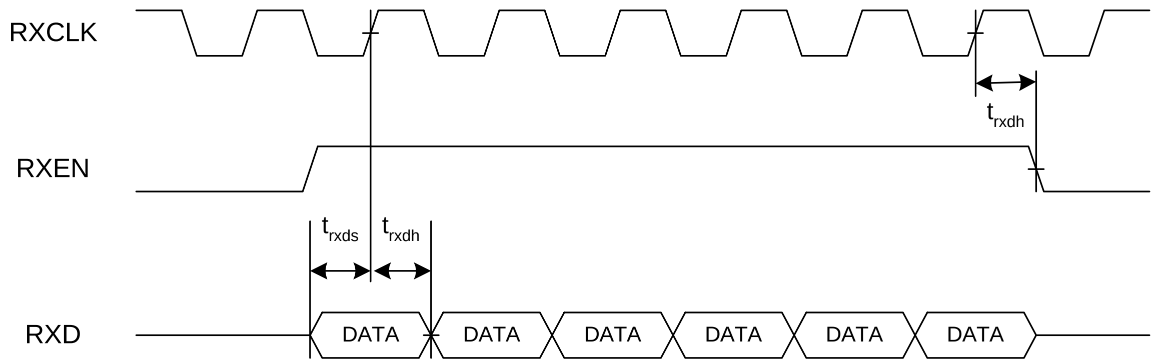


Figure 10 MII Receive Timing

Table 40: PHY Management (MDIO) Read Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{ch}	MDC high time.	420	425	430	ns
t_{cl}	MDC low time.	420	425	430	ns
t_{mc}	MDC period.	840	850	860	ns
t_{ms}	MDIO setup time.	10	-	15	ns
t_{mh}	MDIO hold time.	10	-	-	ns

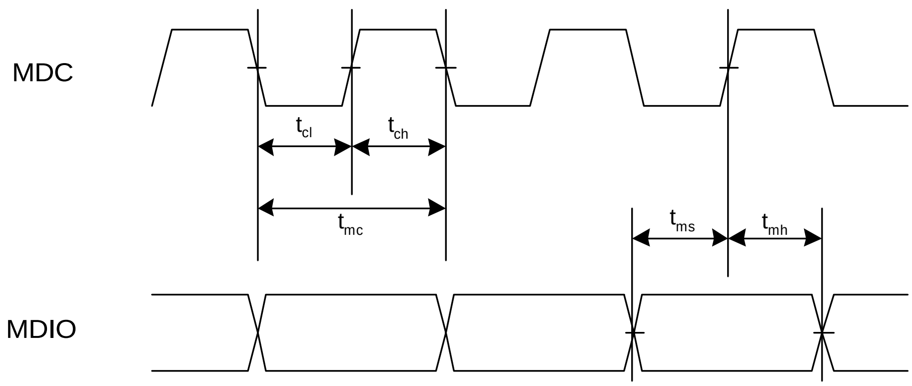


Figure 11 PHY Management Read Timing

Table 41: PHY Management (MDIO) Write Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{ch}	MDC high time.	420	425	430	ns
t_{cl}	MDC low time.	420	425	430	ns
t_{mc}	MDC period.	840	850	860	ns
t_d	MDIO output delay.	40	-	52	ns

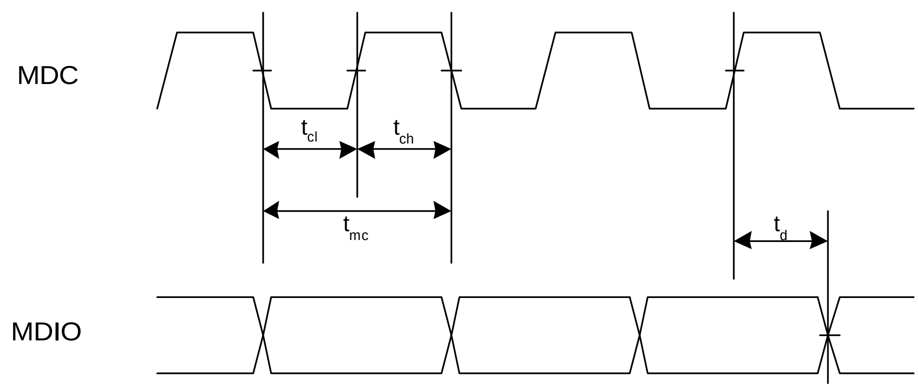


Figure 12 PHY Management Write Timing

Table 42: SGRAM Refresh Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{AH}	Access hold time.	1	-	-	ns
t_{AS}	Access setup time.	3	-	-	ns
t_{CH}	PBCS#, PBRAS#, PBWE# hold time.	1	-	-	ns
t_{CHI}	Clock high level width.	3.5	-	-	ns
t_{CK}	System clock cycle time.	10	-	-	ns
t_{CKH}	CKE hold time.	1	-	-	ns
t_{CKS}	CKE setup time.	3	-	-	ns
t_{CL}	Clock low level width.	3.5	-	-	ns
t_{CS}	PBCS#, PBRAS#, PBWE# setup time.	3	-	-	ns
t_{RP}	Precharge command period.	30	-	-	ns
t_{RC}	Auto-refresh to auto-refresh period.	90	-	-	ns

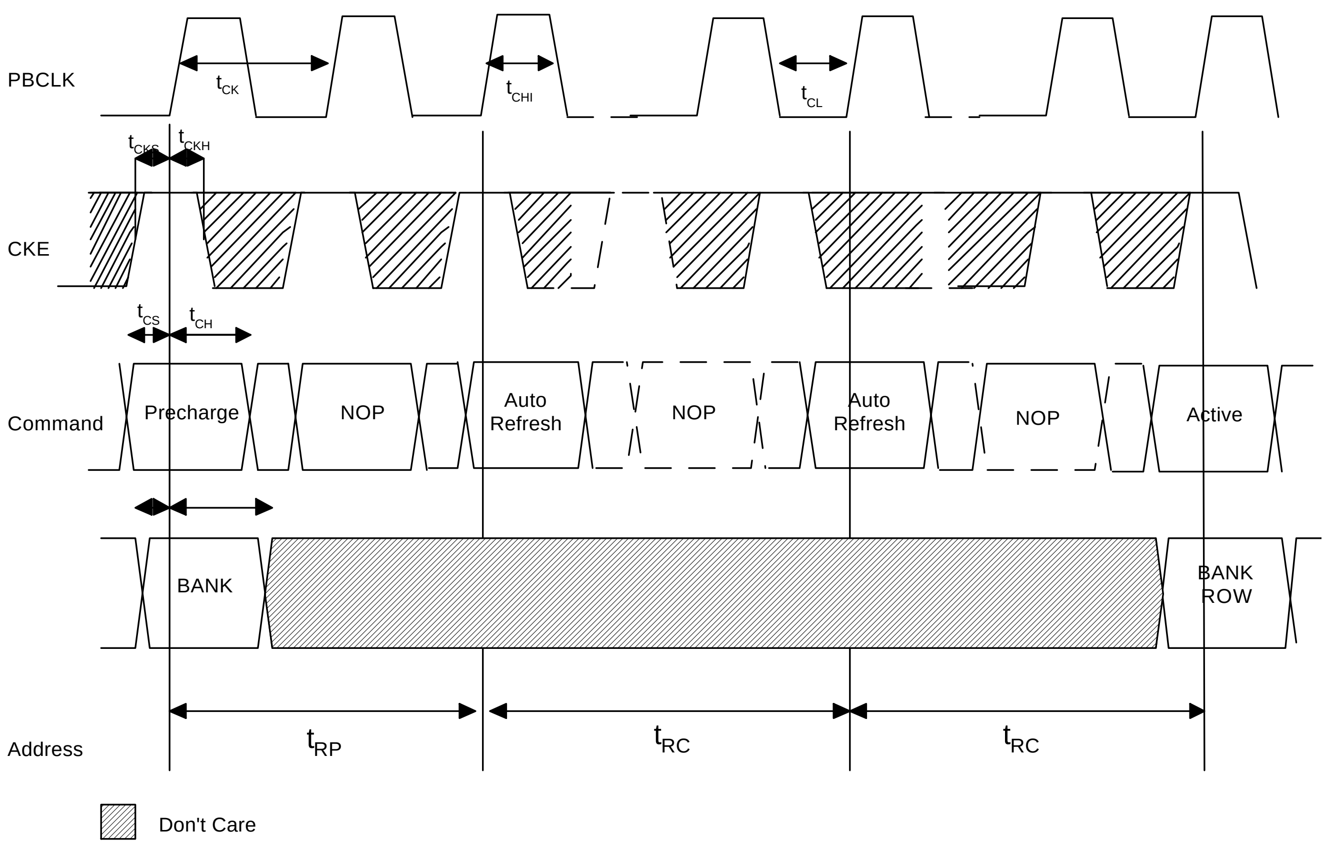


Figure 13 SGRAM Refresh Timing

Table 43: SGRAM Read Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{AC}	Access time.	-	-	10	ns
t_{AH}	Access hold time.	2	-	-	ns
t_{AS}	Access setup time.	2.5	-	-	ns
t_{CH}	PBCS#, PBRAS#, PBWE# hold time.	1	-	-	ns
t_{CHI}	Clock high level width.	3	-	-	ns
t_{CK}	System clock cycle time.	13	-	-	ns
t_{CKH}	CKE hold time.	2	-	-	ns
t_{CKS}	CKE setup time.	3	-	-	ns
t_{CL}	Clock low level width.	3	-	-	ns
t_{CS}	PBCS#, PBRAS#, PBWE# setup time.	2.5	-	-	ns
t_{HZ}	Data out high impedance time.	-	-	8	ns
t_{LZ}	Data out low impedance time.	2	-	-	ns
t_{OH}	Data out hold time.	2	-	-	ns
t_{RAS}	Active to precharge command period.	48	-	-	ns
t_{RCD}	Active to read delay.	24	-	-	ns

Note: This timing requirement is for a SGRAM running at CAS Latency 2. Typically a -8 speed grade SGRAM needs to be used.

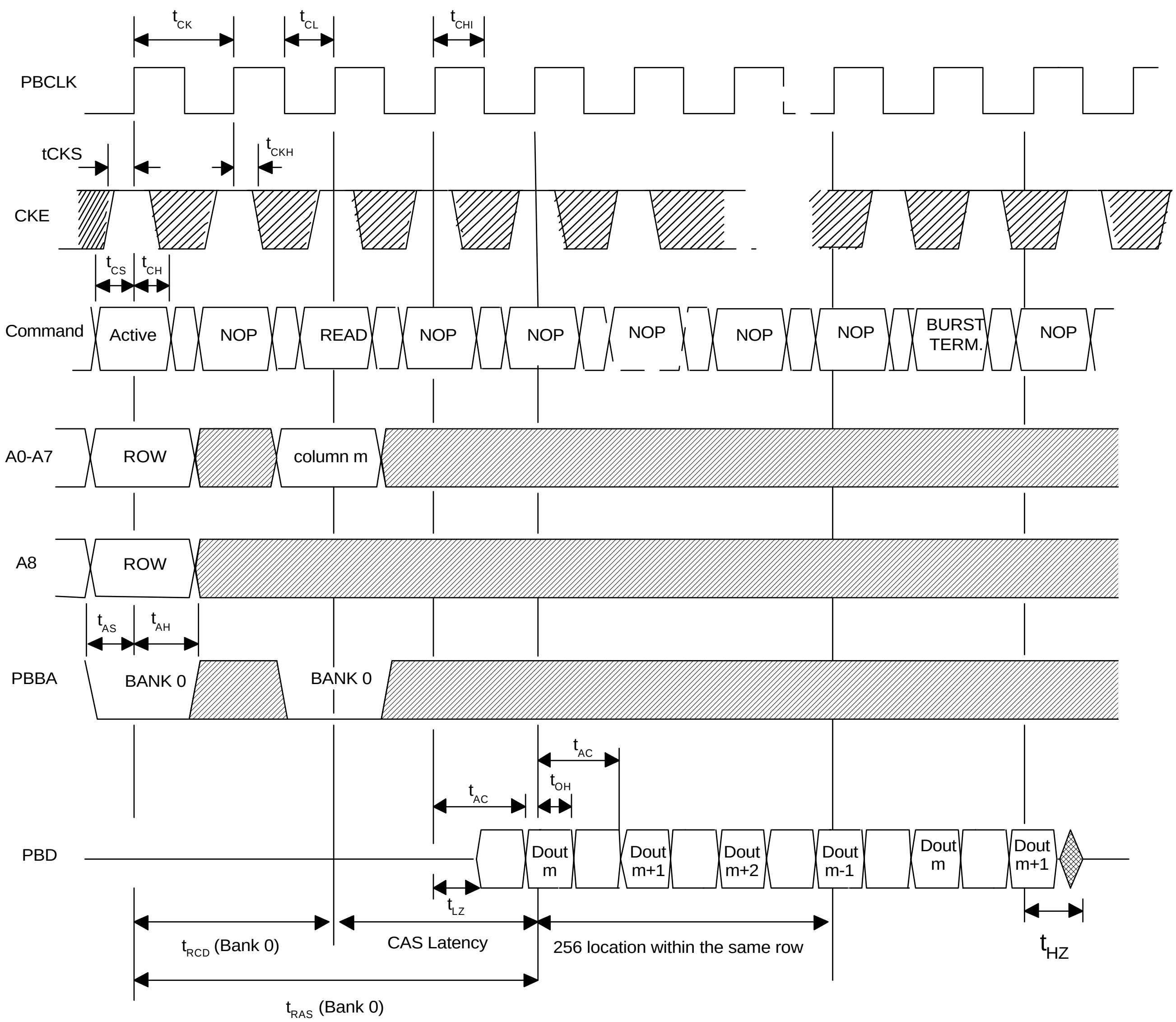


Figure 14 SGRAM Read Timing

Table 44: SGRAM Write Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{AH}	Access hold time.	2	-	-	ns
t_{AS}	Access setup time.	2.5	-	-	ns
t_{CH}	PBCS#, PBRAS#, PBWE# hold time.	1	-	-	ns
t_{CHI}	Clock high level width.	3	-	-	ns
t_{CK}	System clock cycle time.	13	-	-	ns
t_{CKH}	CKE hold time.	2	-	-	ns
t_{CKS}	CKE setup time.	3	-	-	ns
t_{CL}	Clock low level width.	3	-	-	ns
t_{CS}	PBCS#, PBRAS#, PBWE# setup time.	2.5	-	-	ns
t_{DH}	Data in hold time.	1	-	-	ns
t_{DS}	Data in setup time.	2.5	-	-	ns
t_{RAS}	Active to precharge command period.	48	-	100,000	ns
t_{RCD}	Active to read delay.	24	-	-	ns

Note: This timing requirement is for a SGRAM running at CAS Latency 2. Typically a -8 speed grade SGRAM needs to be used.

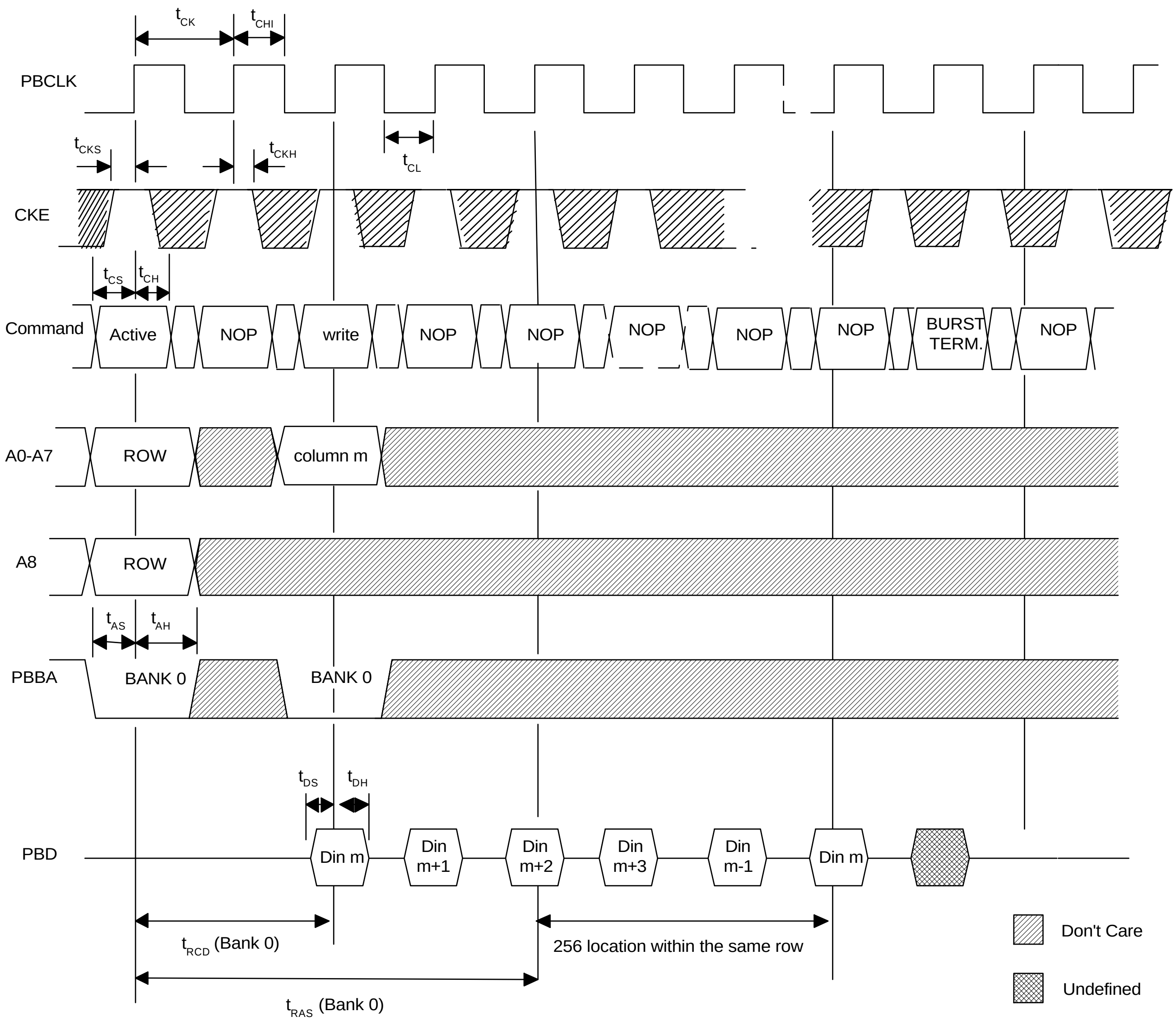


Figure 15 SGRAM Write Timing

6. Electrical Specifications

Note: Operation at absolute maximum ratings could cause permanent damage to the device.

Table 45: Maximum Ratings

DC Supply Voltage (Vcc)	-0.3V ~ + 3.6V
DC Input Voltage	-0.3 ~ Vcc + 0.3V
DC Output Voltage	-0.3 ~ Vcc + 0.3V
DC Supply Voltage to MII	-0.6V to 6.0V
DC Input Voltage to MII	-0.6 to Vcc5 + 0.3V
DC Output Voltage to MII	-0.6 to Vcc5 + 0.3V
Storage Temperature	-55 ^{o}C to +150 ^{o}C

Table 46: Recommended Operation Conditions

Supply Voltage	3.3V ± 0.3V
Operating Temperature	0 ^{o}C to 70 ^{o}C
Power Dissipation	1.7 W (typical)

Table 47: DC Electrical Characteristics

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
Voh	Output voltage-high, Ioh=4mA	2.4	-	-	V
Vol	Output voltage-low, Ioh=4mA	-	-	0.4	V
Ioz	High impedance state output current	-10	-	10	uA
Iih	Input current-high (With no pull-up or pull-down)	-10	-	10	uA
Iil	Input current-low (With no pull-up or pull-down)	-10	-	10	uA
Vih	Input high voltage	0.7*Vcc	-	-	V
Vil	Input low voltage	-	-	0.3*Vcc	V
Icc	Supply current	-	-	-	mA

7. AL102A Mechanical Data

256 PQFP Package

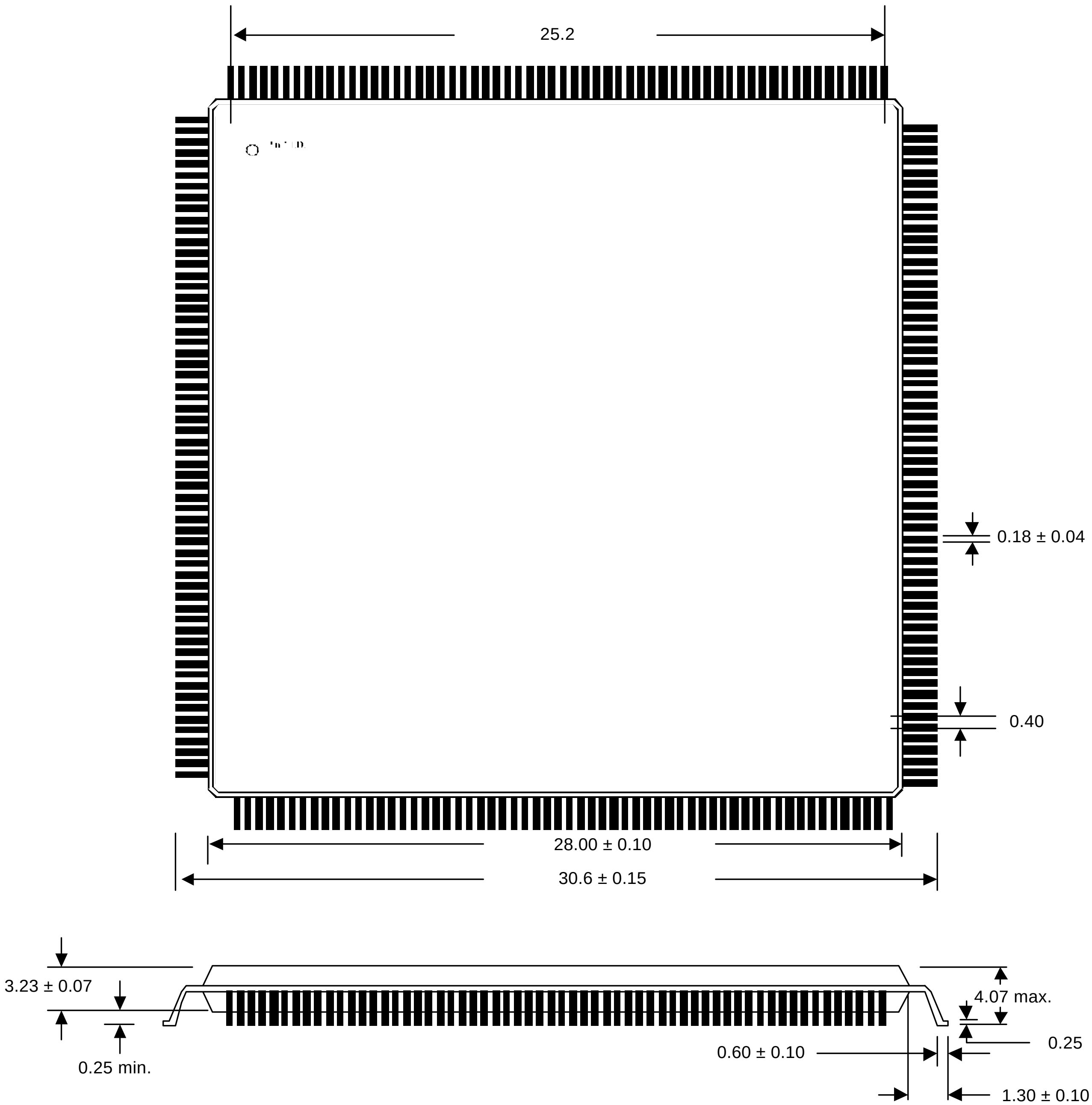


Figure 16 AL102A Mechanical Dimensions

8. Appendix I (VLAN Mapping Work Sheet)

PORT	BIT	PORT 0/REG. 1E	PORT 1/REG. 20	PORT 2/REG. 22	PORT 3/REG. 24	PORT 4/REG. 26	PORT 5/REG. 28	PORT 6/REG. 2A	PORT 7/REG. 2C
7	7								
6	6								
5	5								
4	4								
3	3								
2	2								
1	1								
0	0								

9. Appendix II (Port to Trunk Port Assignment Work Sheet)

	TRUNK / PORT	BIT/ VALUE	PORT 0/REG. 2D	PORT 1/REG. 2E	PORT 2/REG. 2F	PORT 3/REG. 30	PORT 4/REG. 31	PORT 5/REG. 32	PORT 6/REG. 33	PORT 7/REG. 34
TRUNK 1 BITS 3, 2	7	11								
	6	10								
	5	01								
	4	00								
TRUNK 0 BITS 1, 0	3	11								
	2	10								
	1	01								
	0	00								

10. Appendix III (Suggested Memory Components)

Note: This is only a partial list of memory components that can be used in Allayer devices.

The AL102A uses Frame Buffer SGRAM chips that require 32-bit wide SGRAM or SDRAM, that is 75 MHz or faster with CAS latency 2.

DEVICE	FREQ.	8 Mbit SGRAM	16 Mbit SGRAM
AL102A	75 MHz	MoSys - MG802C256Q-10 Etron - EM635327Q-8	MoSys - MG802C512L-8 Etron - EM636227Q-8 Winbond - W971632AF-8 Hitachi - HM5216326FP-8

Rev. History (Prelim. 1.1 to 1.2)

1. Reformatted and edited document.

2. Added memory information in appendix III.

Rev. History (Prelim 1.2 to 1.3)

3. Added new PHY management timing diagrams.

4. Added new RMII and MII timing diagrams.

Prelim 1.3 to Rev. 1.0

1. Fully released document.

Index