8-Port 10/100 Mbit/s Dual Speed Fast Ethernet Switch

- Supports eight 10/100 Mbit/s Ethernet ports with MII and RMII interface
- Capable of trunking up to 800 Mbit/s link with link fail-over
- Full- and half-duplex mode operation
- Supports 12K MAC addresses with tag VLAN or 16K without VLAN
- Scalable design for stackable switch implementation
- RoX-II expansion link supports 6.4 Gbit/s throughput
- Gigabit Ethernet ready with AL1022
- Flexible prioritized queueing for multimedia and data traffic
- Layer 3/4 switching with AL3000 on RoX-II
- IEEE 802.3x flow control for full-duplex operation
- Optional backpressure flow control support for half-duplex operation
- 802.1p support with four priority levels
- 802.1q tag-based and port-based VLAN support, 4K VLAN table
- IGMP frame trapping
- Supports 64 IP multicast groups
- RMON and SNMP support with the AL300A management (MIB) device
- 2.5V and 3.3V operation
- Packaged in 456-pin BGA

Product Description

The AL126 is an eight-port 10/100 Mbit/s dual speed Ethernet switch. A low-cost and scalable solution for up to 32 ports is achieved through the use of low-cost buffer memory and Allayer's proprietary RoX-II™ architecture. In addition, the AL126 supports port-based and 802.1q VLAN, 802.1p priority, IGMP frame trapping, and multiple port aggregation trunks.

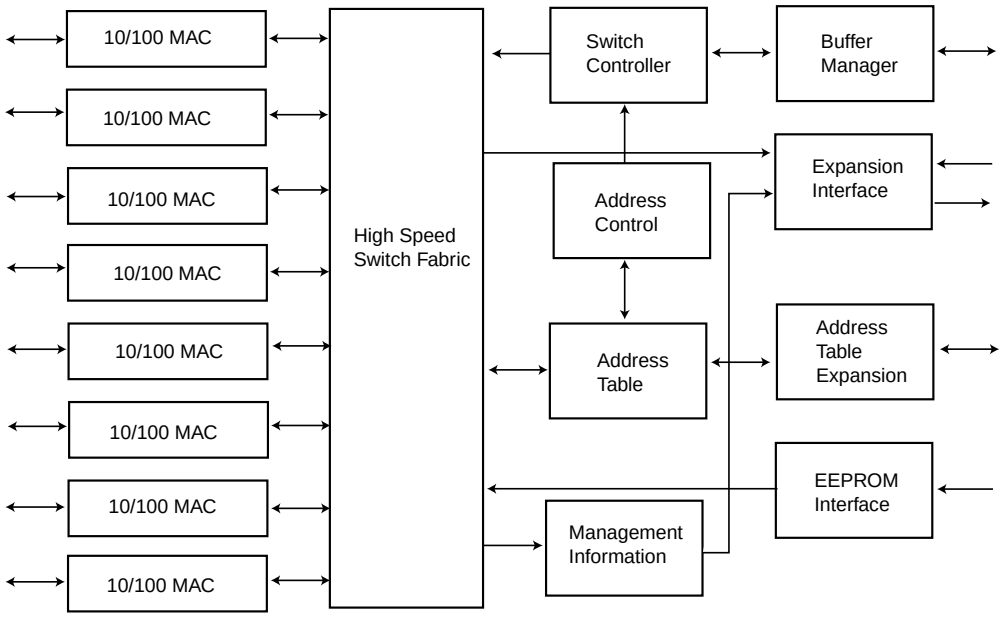

Figure 1 System Block Diagram

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1. AL126 Overview

The AL126 is an eight-port 10/100 Ethernet switch chip with RoX-II expansion interface. The RoX-II™ interface is a 3.2 Gbit/s data ring (6.4 Gbit/s full-duplex) and control ring interfaces. The RoX-II bus can support up to four switch chips and one management device (AL300A) or IP router (AL3000) chip. Various combinations can be used for different configurations. The maximum port configuration will be 32-port 100 Mbit/s ports or 24-port 10/100 Mbit/s plus two Gigabit Ethernet ports, or eight Gigabit ports.

The RoX-II interface supports the management device, the AL300A. SNMP and RMON are supported through this management device. The following diagram shows a 24+2G managed L3/4 router switch supported by the AL126, AL1022, and the AL300A.

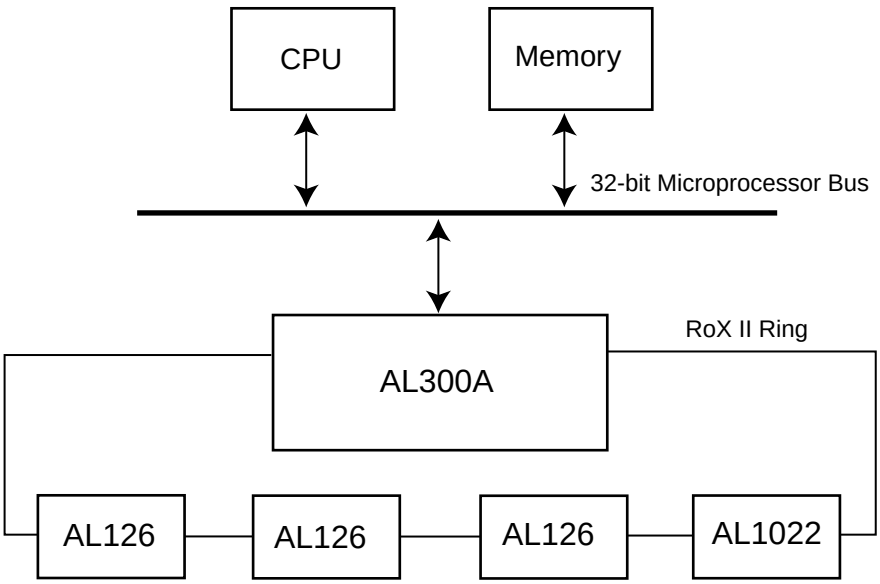

Figure 2 24+2G Managed Routing Switch

The AL126 provides eight 10/100 Mbit/s Ethernet ports with each port supporting both 10 and 100 Mbit/s data rate. The operation mode is auto-negotiated through the PHY.

The AL126 also supports trunking applications. The chip provides two optional load balancing schemes, explicit and dynamic. With trunking, it is possible to group up to eight full-duplex links together to form a single 1600-Mb link. The device also supports the current IEEE 802.3ad specification.

Data received from the MAC interface is stored in the external memory buffer. The AL126 utilizes cost effective SGRAM to provide 8-Mb or 16-Mb of buffer memory.

The AL126 provides two flow control methods. For half-duplex operations, an optional jamming based flow control (also known as backpressure) is available to prevent loss of data. With this method of flow control, the switch will generate a jam signal when the receive-buffer is full. In the full-duplex mode, the AL126 utilizes IEEE 802.3x as the flow control mechanism.

All ports support multiple MAC addresses. The switch chip supports up to 12K MAC addresses with 4K VLAN tag or 16K MAC without VLAN through external SSRAM.

For managed switch applications, the AL126 supports network management through the network management option. When the management option is enabled, network statistics for each port are gathered and sent across the RoX-II bus. The management information base chip on the bus will collect and store the data for the network management agent. Access to the statistic counters is provided via the CPU interface of the AL300A.

The AL126 operates only in the store and forward mode. The entire frame is checked for errors and any frames with errors are automatically filtered and are not forwarded to the destination port.

The device also provides 64 IP multicast group addresses for IP multicast applications. The AL126 can perform IGMP frame trapping and forward them to the CPU. This allows the CPU to participate in the IGMP protocol and determine which ports should participate in the multicast session.

The switch is initialized and configured by an external EEPROM. For an unmanaged switch design, there is no need for a CPU. A parallel interface can be utilized to reprogram the EEPROM for field reconfiguration.

The device supports port-based and tagged VLAN (IEEE 802.3ac/802.1q VLAN) for workgroup and segment switching applications.

The AL126 supports 802.1p with four levels of priority queues. Relative priority is controlled by either programmable Weighted Round-Robin or Strict Priority.

The device also provides two levels of security for intrusion protection. Security can be implemented on a per-port basis.

Other features include port monitoring and broadcast storm filtering to reduce broadcast traffic through the switch.

Pin Diagram

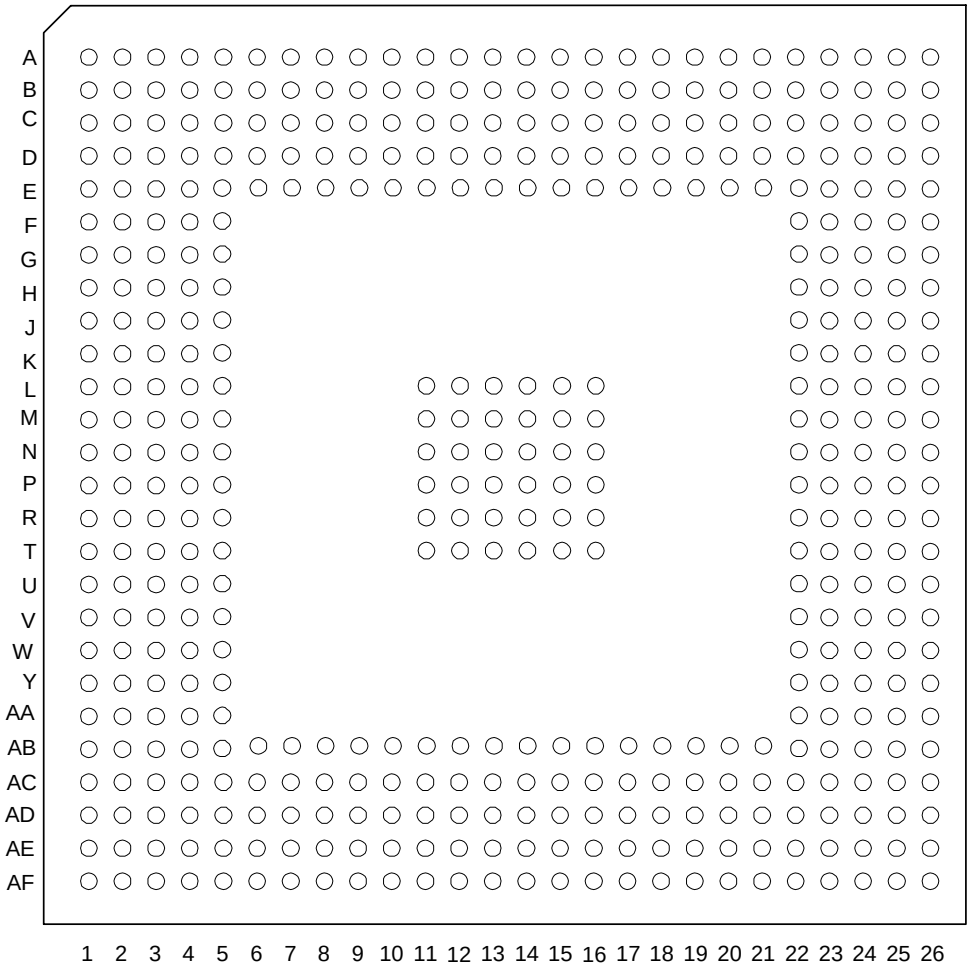

Figure 3 AL126 Pin Diagram (Top View)

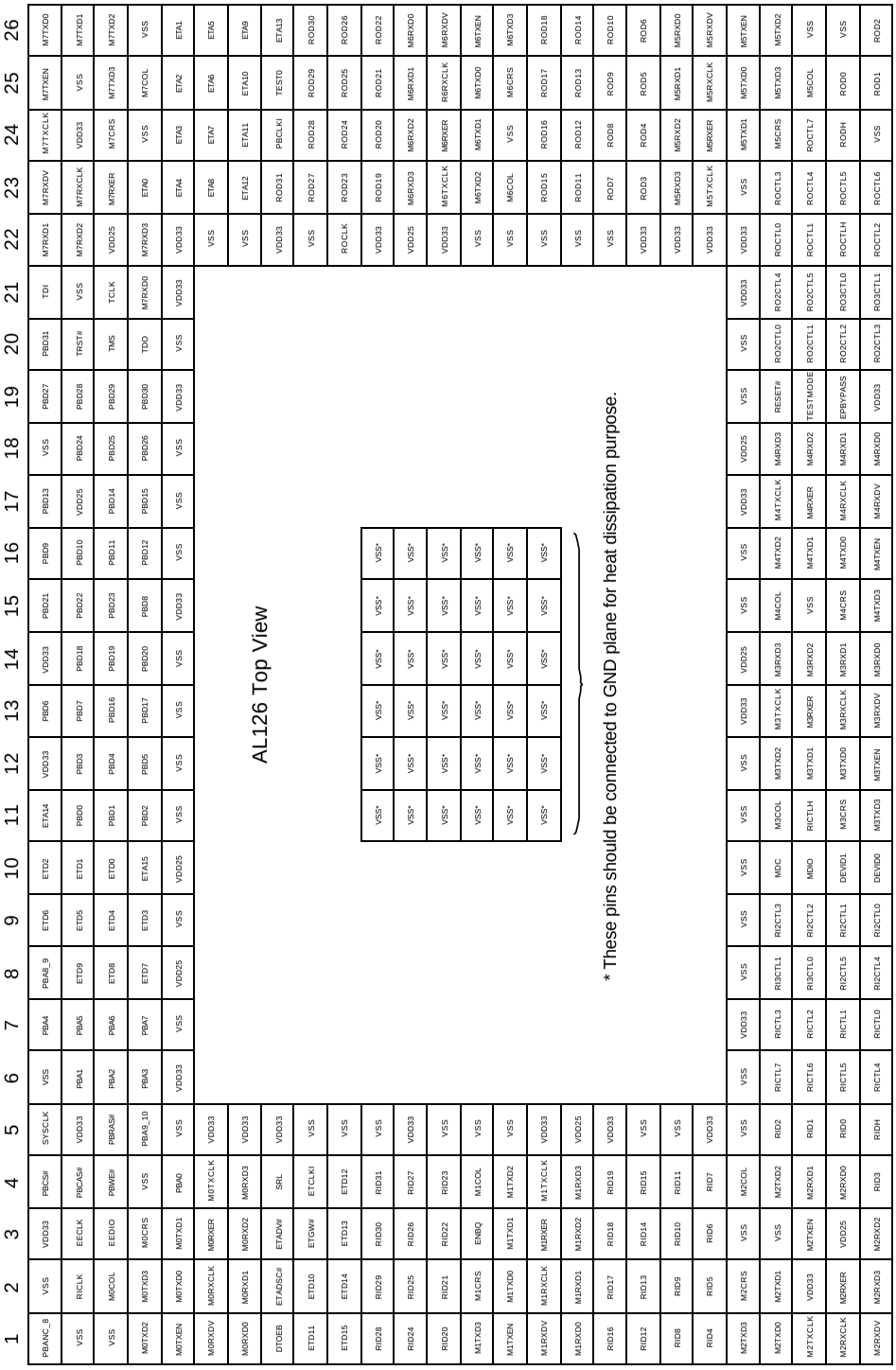

Figure 4 AL126 Pin Lay-out

2. Pin Descriptions

The AL126 supports MII/RMII interface. Ports 1 through 7 are globally programmed to be MII or RMII, and Port 0 is independently programmable as MII or RMII. When RMII interface is used; TXD3 and TXD2 should be left unconnected; RXD3, RXD2, TXCLK, RXDV, RXER, and COL can be left unconnected because they have internal pull ups. RXCLK0 and RXCLK3 should be connected to the 50 MHz reference clock. All date and control signals are clocked in/out on the rising edge of the reference clock in RMII mode.

Table 1: RMII/MII Interface (Port 0)

PIN NAME	PIN NO.	I/O	DESCRIPTION
M0TXD3 M0TXD2 M0TXD1 M0TXD0	D2 D1 E3 E2	O	Transmit Data - NRZ data to be transmitted to transceiver. For MII mode, signal M0TXEN and M0TXD0 through M0TXD3 are clocked out by the rising edge of M0TXCLK. For RMII mode, M0TXD1 and M0TXD0 are clocked out by the RMII reference clock M0RXCLK. During reset, these pins are set to input mode to read device existence information. Leave floating if not used.
M0TXEN	E1	O	Transmit Enable - Synchronous to the transmit clock in MII mode. For RMII mode, M0TXEN is synchronous to M0RXCLK.
M0TXCLK	F4	I	Transmit Clock Input. 25 MHz for 100 Mbit/s and 2.5 MHz for 10 Mbit/s. (Not used in RMII mode).
M0RXD3 M0RXD2 M0RXD1 M0RXD0	G4 G3 G2 G1	I	Receive Data - NRZ data from the transceiver. For MII mode, signal M0RXDV, M0RXER and M0RXD0 through RXD3 are sampled by the rising edge of M0RXCLK. For RMII mode, M0RXD3 and M0RXD2 are not used. M0RXD1and M0RXD0 are sampled by the rising edge of the RMII reference clock M0RXCLK.
M0RXDV	F1	I	Receive Data Valid. Active high.
M0RXCLK	F2	I	Receive Clock (MII mode). RMII clock for port 0.
M0RXER	F3	I	Receive Data Error. Active high. (Not used in RMII mode).
M0CRS	D3	I	Carrier Sense. Active high.
M0COL	C2	I	Collision Detect. Active high. (Not used in RMII mode).

Table 2: RMII/MII Interface (Port 1)

PIN NAME	PIN NO.	I/O	DESCRIPTION
M1TXD3 M1TXD2 M1TXD1 M1TXD0	P1 R4 R3 R2	O	Transmit Data - NRZ data to be transmitted to transceiver. For MII mode, signal M1TXEN and TXD0 through M1TXD3 are clocked out by the rising edge of TXCLK. For RMII mode, M1TXD1 and M1TXD0 are clocked out by the RMII reference clock M3RXCLK.
M1TXEN	R1	O	Transmit Enable - Synchronous to the transmit clock in MII mode. For RMII mode, M1TXEN is synchronous to M3RXCLK.
M1TXCLK	T4	I	Transmit Clock Input. 25 MHz for 100 Mbit/s and 2.5 MHz for 10 Mbit/s. (Not used in RMII mode).
M1RXD3 M1RXD2 M1RXD1 M1RXD0	U4 U3 U2 U1	I	Receive Data - NRZ data from the transceiver. For MII mode, signal M1RXDV, M1RXER and M1RXD0 through M1RXD3 are sampled by the rising edge of M1RXCLK. For RMII mode, M1RXD3 and M1RXD2 are not used. M1RXD1and M1RXD0 are sampled by the rising edge of the RMII reference clock M3RXCLK.
M1RXDV	T1	I	Receive Data Valid. Active high.
M1RXCLK	T2	I	Receive Clock (MII mode).
M1RXER	T3	I	Receive Data Error. Active high. (Not used in RMII mode).
M1CRS	P2	I	Carrier Sense. Active high.
M1COL	P4	I	Collision Detect. Active high. (Not used in RMII mode).

Table 3: RMII/MII Interface (Port 2)

PIN NAME	PIN NO.	I/O	DESCRIPTION
M2TXD3 M2TXD2 M2TXD1 M2TXD0	AB1 AC4 AC2 AC1	O	Transmit Data - NRZ data to be transmitted to transceiver. For MII mode, signal M2TXEN and M2TXD0 through M2TXD3 are clocked out by the rising edge of TXCLK. For RMII mode, M2TXD1 and M2TXD0 are clocked out by the RMII reference clock M3RXCLK.
M2TXEN	AD3	O	Transmit Enable - Synchronous to the transmit clock in MII mode. For RMII mode, M2TXEN is synchronous to M3RXCLK.
M2TXCLK	AD1	I	Transmit Clock Input. 25 MHz for 100 Mbit/s and 2.5 MHz for 10 Mbit/s. (Not used in RMII mode).
M2RXD3 M2RXD2 M2RXD1 M2RXD0	AF2 AF3 AD4 AE4	I	Receive Data - NRZ data from the transceiver. For MII mode, signal M2RXDV, M2RXER and M2RXD0 through M2RXD3 are sampled by the rising edge of M3RXCLK. For RMII mode, M2RXD3 and M2RXD2 are not used. M2RXD1and M2RXD0 are sampled by the rising edge of the RMII reference clock M3RXCLK.
M2RXDV	AF1	I	Receive Data Valid. Active high.
M2RXCLK	AE1	I	Receive Clock (MII mode).
M2RXER	AE2	I	Receive Data Error. Active high. (Not used in RMII mode).
M2CRS	AB2	I	Carrier Sense. Active high.
M2COL	AB4	I	Collision Detect. Active high. (Not used in RMII mode).

Table 4: RMII/MII Interface (Port 3)

PIN NAME	PIN NO.	I/O	DESCRIPTION
M3TXD3 M3TXD2 M3TXD1 M3TXD0	AF11 AC12 AD12 AE12	O	Transmit Data - NRZ data to be transmitted to transceiver. For MII mode, signal M3TXEN and M3TXD0 through M3TXD3 are clocked out by the rising edge of TXCLK. For RMII mode, M3TXD1 and M3TXD0 are clocked out by the RMII reference clock M3RXCLK.
M3TXEN	AF12	O	Transmit Enable - Synchronous to the transmit clock in MII mode. For RMII mode, M3TXEN is synchronous to M3RXCLK.
M3TXCLK	AC13	I	Transmit Clock Input. 25 MHz for 100 Mbit/s and 2.5 MHz for 10 Mbit/s. (Not used in RMII mode).
M3RXD3 M3RXD2 M3RXD1 M3RXD0	AC14 AD14 AE14 AF14	I	Receive Data - NRZ data from the transceiver. For MII mode, signal M3RXDV, M3RXER and RXD0 through RXD3 are sampled by the rising edge of M3RXCLK. For RMII mode, M3RXD3 and M3RXD2 are not used. M3RXD1and M3RXD0 are sampled by the rising edge of the RMII reference clock M3RXCLK.
M3RXDV	AF13	I	Receive Data Valid. Active high.
M3RXCLK	AE13	I	Receive Clock (MII mode). RMII clock for ports 1~7.
M3RXER	AD13	I	Receive Data Error. Active high. (Not used in RMII mode).
M3CRS	AE11	I	Carrier Sense. Active high.
M3COL	AC11	I	Collision Detect. Active high. (Not used in RMII mode).

Table 5: RMII/MII Interface (Port 4)

PIN NAME	PIN NO.	I/O	DESCRIPTION
M4TXD3 M4TXD2 M4TXD1 M4TXD0	AF15 AC16 AD16 AE16	O	Transmit Data - NRZ data to be transmitted to transceiver. For MII mode, signal M4TXEN and M4TXD0 through M4TXD3 are clocked out by the rising edge of TXCLK. For RMII mode, M4TXD1 and M4TXD0 are clocked out by the RMII reference clock M3RXCLK.
M4TXEN	AF16	O	Transmit Enable - Synchronous to the transmit clock in MII mode. For RMII mode, M4TXEN is synchronous to M3RXCLK.
M4TXCLK	AC17	I	Transmit Clock Input. 25 MHz for 100 Mbit/s and 2.5 MHz for 10 Mbit/s. (Not used in RMII mode).
M4RXD3 M4RXD2 M4RXD1 M4RXD0	AC18 AD18 AE18 AF18	I	Receive Data - NRZ data from the transceiver. For MII mode, signal RX_DV, RX_ER and RX_D0 through RX_D3 are sampled by the rising edge of M3RXCLK. For RMII mode, M4RXD3 and M4RXD2 are not used. M4RXD1and M4RXD0 are sampled by the rising edge of the RMII reference clock M3RXCLK.
M4RXDV	AF17	I	Receive Data Valid. Active high.
M4RXCLK	AE17	I	Receive Clock (MII mode).
M4RXER	AD17	I	Receive Data Error. Active high. (Not used in RMII mode).
M4CRS	AE15	I	Carrier Sense. Active high.
M4COL	AC15	I	Collision Detect. Active high. (Not used in RMII mode).

Table 6: RMII/MII Interface (Port 5)

PIN NAME	PIN NO.	I/O	DESCRIPTION
M5TXD3 M5TXD2 M5TXD1 M5TXD0	AC25 AC26 AB24 AB25	O	Transmit Data - NRZ data to be transmitted to transceiver. For MII mode, signal M5TXEN and M5TXD0 through M5TXD3 are clocked out by the rising edge of TXCLK. For RMII mode, M5TXD1 and M5TXD0 are clocked out by the RMII reference clock M3RXCLK.
M5TXEN	AB26	O	Transmit Enable - Synchronous to the transmit clock in MII mode. For RMII mode, M5TXEN is synchronous to M3RXCLK.
M5TXCLK	AA23	I	Transmit Clock Input. 25 MHz for 100 Mbit/s and 2.5 MHz for 10 Mbit/s. (Not used in RMII mode).
M5RXD3 M5RXD2 M5RXD1 M5RXD0	Y23 Y24 Y25 Y26	I	Receive Data - NRZ data from the transceiver. For MII mode, signal M5RXDV, M5RXER and M5RXD0 through M5RXD3 are sampled by the rising edge of M3RXCLK. For RMII mode, M5RXD3 and M5RXD2 are not used. M5RXD1and M5RXD0 are sampled by the rising edge of the RMII reference clock M3RXCLK.
M5RXDV	AA26	I	Receive Data Valid. Active high.
M5RXCLK	AA25	I	Receive Clock (MII mode).
M5RXER	AA24	I	Receive Data Error. Active high. (Not used in RMII mode).
M5CRS	AC24	I	Carrier Sense. Active high.
M5COL	AD25	I	Collision Detect. Active high. (Not used in RMII mode).

Table 7: RMII/MII Interface (Port 6)

PIN NAME	PIN NO.	I/O	DESCRIPTION
M6TXD3 M6TXD2 M6TXD1 M6TXD0	R26 P23 P24 P25	O	Transmit Data - NRZ data to be transmitted to transceiver. For MII mode, signal M6TXEN and M6TXD0 through M6TXD3 are clocked out by the rising edge of TXCLK. For RMII mode, M6TXD1 and M6TXD0 are clocked out by the RMII reference clock M3RXCLK.
M6TXEN	P26	O	Transmit Enable - Synchronous to the transmit clock in MII mode. For RMII mode, M6TXEN is synchronous to M3RXCLK.
M6TXCLK	N23	I	Transmit Clock Input. 25 MHz for 100 Mbit/s and 2.5 MHz for 10 Mbit/s. (Not used in RMII mode).
M6RXD3 M6RXD2 M6RXD1 M6RXD0	M23 M24 M25 M26	I	Receive Data - NRZ data from the transceiver. For MII mode, signal M6RXDV, M6RXER and M6RXD0 through M6RXD3 are sampled by the rising edge of M3RXCLK. For RMII mode, M6RXD3 and M6RXD2 are not used. M6RXD1and M6RXD0 are sampled by the rising edge of the RMII reference clock M3RXCLK.
M6RXDV	N26	I	Receive Data Valid. Active high.
M6RXCLK	N25	I	Receive Clock (MII mode).
M6RXER	N24	I	Receive Data Error. Active high. (Not used in RMII mode).
M6CRS	R25	I	Carrier Sense. Active high.
M6COL	R23	I	Collision Detect. Active high. (Not used in RMII mode).

Table 8: RMII/MII Interface (Port 7)

PIN NAME	PIN NO.	I/O	DESCRIPTION
M7TXD3 M7TXD2 M7TXD1 M7TXD0	C25 C26 B26 A26	O	Transmit Data - NRZ data to be transmitted to transceiver. For MII mode, signal M7TXEN and M7TXD0 through M7TXD3 are clocked out by the rising edge of TXCLK. For RMII mode, M7TXD1 and M7TXD0 are clocked out by the RMII reference clock M3RXCLK.
M7TXEN	A25	O	Transmit Enable - Synchronous to the transmit clock in MII mode. For RMII mode, M7TXEN is synchronous to M3RXCLK.
M7TXCLK	A24	I	Transmit Clock Input. 25 MHz for 100 Mbit/s and 2.5 MHz for 10 Mbit/s. (Not used in RMII mode).
M7RXD3 M7RXD2 M7RXD1 M7RXD0	D22 B22 A22 D21	I	Receive Data - NRZ data from the transceiver. For MII mode, signal M7RXDV, M7RXER and M7RXD0 through M7RXD3 are sampled by the rising edge of M3RXCLK. For RMII mode, M7RXD3 and M7RXD2 are not used. M7RXD1and M7RXD0 are sampled by the rising edge of the RMII reference clock M3RXCLK.
M7RXDV	A23	I	Receive Data Valid. Active high.
M7RXCLK	B23	I	Receive Clock (MII mode).
M7RXER	C23	I	Receive Data Error. Active high. (Not used in RMII mode).
M7CRS	C24	I	Carrier Sense. Active high.
M7COL	D25	I	Collision Detect. Active high. (Not used in RMII mode).

Table 9: RoX-II Input Interface

PIN NAME	PIN NO.	I/O	DESCRIPTION
RID31 RID30 RID29 RID28 RID27 RID26 RID25 RID24 RID23 RID22 RID21 RID20 RID19 RID18 RID17 RID16 RID15 RID14 RID13 RID12 RID11 RID10 RID9 RID8 RID7 RID6 RID5 RID4 RID3 RID2 RID1 RID0	L4 L3 L2 L1 M4 M3 M2 M1 N4 N3 N2 N1 V4 V3 V2 V1 W4 W3 W2 W1 Y4 Y3 Y2 Y1 AA4 AA3 AA2 AA1 AF4 AC5 AD5 AE5	I	Ring Data Input.
RIDH	AF5	I	Ring Data Header Input. High for duration of data, low when idle.
RICTL7 RICTL6 RICTL5 RICTL4 RICTL3 RICTL2 RICTL1 RICTL0	AC6 AD6 AE6 AF6 AC7 AD7 AE7 AF7	I	Ring Control Input.
RICTLH	AD11	I	Ring Control Header Input. Low/high for each part of control data word, high when idle.

Table 9: RoX-II Input Interface (Continued)

PIN NAME	PIN NO.	I/O	DESCRIPTION
RICLK	B2	I	Ring In Clock. RID [ ] and RICTL [ ] clocked in on the rising edge of RICLK.
RI2CTL5 RI2CTL4 RI2CTL3 RI2CTL2 RI2CTL1 RI2CTL0	AE8 AF8 AC9 AD9 AE9 AF9	I	Second Ring Control Input.
RI3CTL1 RI3CTL0	AC8 AD8	I	Reserved for Future Use.

Table 10: RoX-II Output Interface

PIN NAME	PIN NO.	I/O	DESCRIPTION
ROD31 ROD30 ROD29 ROD28 ROD27 ROD26 ROD25 ROD24 ROD23 ROD22 ROD21 ROD20 ROD19 ROD18 ROD17 ROD16 ROD15 ROD14 ROD13 ROD12 ROD11 ROD10 ROD9 ROD8 ROD7 ROD6 ROD5 ROD4 ROD3 ROD2 ROD1 ROD0	H23 J26 J25 J24 J23 K26 K25 K24 K23 L26 L25 L24 L23 T26 T25 T24 T23 U26 U25 U24 U23 V26 V25 V24 V23 W26 W25 W24 W23 AF26 AF25 AE25	O	Ring Data Output.
RODH	AE24	O	Ring Data Header Output. High for duration of data, low when idle.
ROCTL7 ROCTL6 ROCTL5 ROCTL4 ROCTL3 ROCTL2 ROCTL1 ROCTL0	AD24 AF23 AE23 AD23 AC23 AF22 AD22 AC22	O	Ring Control Output.
ROCTLH	AE22	O	Ring Control Header Output. Low/high for each part of control data word, keep high when idle.

Table 10: RoX-II Output Interface (Continued)

ROCLK	K22	O	Ring Out Clock. ROD [ ] and ROCTL [ ] are clocked out on the rising edge of SYSCLK. ROCLK is a delayed version of SYSCLK to drive RICLK of the next device.
RO2CTL5 RO2CTL4 RO2CTL3 RO2CTL2 RO2CTL1 RO2CTL0	AD21 AC21 AF20 AE20 AD20 AC20	O	Second Ring Control Output.
RO3CTL1 RO3CTL0	AF21 AE21	O	Reserved for Future Use.

Table 11: SGRAM Interface

PIN NAME	PIN NO.	I/O	DESCRIPTION
PBD31 PBD30 PBD29 PBD28 PBD27 PBD26 PBD25 PBD24 PBD23 PBD22 PBD21 PBD20 PBD19 PBD18 PBD17 PBD16 PBD15 PBD14 PBD13 PBD12 PBD11 PBD10 PBD9 PBD8 PBD7 PBD6 PBD5 PBD4 PBD3 PBD2 PBD1 PBD0	A20 D19 C19 B19 A19 D18 C18 B18 C15 B15 A15 D14 C14 B14 D13 C13 D17 C17 A17 D16 C16 B16 A16 D15 B13 A13 D12 C12 B12 D11 C11 B11	I/O	SGRAM Data Bus.
PBA9_10	D5	O	This pin is connected to address 10 when connected to a 16 Mbit SGRAM and address 9 when connected to a 8 Mbit SGRAM. This pin should be connected to Pin 29 of SGRAMs.
PBA8_9	A8	O	This pin is connected to address 9 when connected to a 16 Mbit SGRAM and address 8 when connected to a 8 Mbit SGRAM. This pin should be connected to Pin 51 of SGRAMs.
PBANC_8	A1	O	This pin is connected to address 8 when connected to a 16 Mbit SGRAM and unconnected when connected to a 8 Mbit SGRAM. This pin should be connected to Pin 31 of SGRAMs.

Table 11: SGRAM Interface (Continued)

PIN NAME	PIN NO.	I/O	DESCRIPTION
PBA7 PBA6 PBA5 PBA4 PBA3 PBA2 PBA1 PBA0	D7 C7 B7 A7 D6 C6 B6 E4	O	These pins are connected to SGRAM address 7 through 0 respectively.
PBCS#	A4	O	Chip Select. CS# enables and disables the command decoder of the SGRAM.
PBRAS#	C5	O	SGRAM Row Address Strobe.
PBCAS#	B4	O	SGRAM Column Address Strobe.
PBWE#	C4	O	Write Enable.
PBCLK	H24	O	System Clock Output to Drive the SGRAM.

Table 12: External Address Table SSRAM Interface

PIN NAME	PIN NO.	I/O	DESCRIPTION
ETD15 ETD14 ETD13 ETD12 ETD11 ETD10 ETD9 ETD8 ETD7 ETD6 ETD5 ETD4 ETD3 ETD2 ETD1 ETD0	K1 K2 K3 K4 J1 J2 B8 C8 D8 A9 B9 C9 D9 A10 B10 C10	I/O	SSRAM Data Bus.

Table 12: External Address Table SSRAM Interface (Continued)

PIN NAME	PIN NO.	I/O	DESCRIPTION
ETA15 ETA14 ETA13 ETA12 ETA11 ETA10 ETA9 ETA8 ETA7 ETA6 ETA5 ETA4 ETA3 ETA2 ETA1 ETA0	D10 A11 H26 G23 G24 G25 G26 F23 F24 F25 F26 E23 E24 E25 E26 D23	O	SSRAM Address Line.
ETADSC#	H2	O	Synchronous Address Status Controller.
ETADV#	H3	O	Synchronous Address Advance. Used to advance SRAMs internal burst counter.
ETGW#	J3	O	Global Write. Enables a full 32-bit write.
ETOE#	H1	O	Output Enable. Active low. This enables the I/O output driver.
ETCLK	J4	O	System Clock Output to Drive the SSRAM.

Table 13: EEPROM Interface

PIN NAME	PIN NUMBER	I/O	DESCRIPTION
EEDIO	C3	I/O	EEPROM Data Input and Output at boot-up. Data input and output for reverse EEDIO. Tri-stated after boot-up, use an external pull-up.
EECLK	B3	I/O	EEPROM Clock Output at boot-up. Clock input for reverse EEDIO. Tri-stated after boot-up, use an external pull-up.

Table 14: MDIO Interface

PIN NAME	PIN NUMBER	I/O	DESCRIPTION
MDC	AC10	O	PHY Management Clock.
MDIO	AD10	I/O	PHY Management Data Input and Output.

Table 15: Miscellaneous Pins

PIN NAME	PIN NUMBER	I/O	DESCRIPTION
DEVID1 DEVID0	AE10 AF10	I	Device ID Number. Should be connected to EEPROM A1 and A0. The AL126 will use <0, ID1, ID0> as EEPROM address and respond to <1, ID1, ID0> in reverse EEDIO.
RESET#	AC19	I	Reset
TESTMODE	AD19	I	Test Mode Pin. This pin should be grounded for normal operation.
SRL	H4	O	Status Serial Output (for testing).
EPBYPASS	AE19	I	This pin bypasses the EEPROM setup. This pin should be tied to ground.
SYSCLK	A5	I	100 MHz System Clock.
ENBQ	P3	I	Enable 802.1q Tag VLAN.
TEST0	H25	O	Reserved Test Output. Leave unconnected.
TRST	B20	O	Reserved for JTAG Scan. Testing output. Leave unconnected.
TMS	C20	O	Reserved for JTAG Scan. Testing output. Leave unconnected.
TDO	D20	O	Reserved for JTAG Scan. Testing output. Leave unconnected.
TDI	A21	O	Reserved for JTAG Scan. Testing output. Leave unconnected.
TCLK	C21	O	Reserved for JTAG Scan. Testing output. Leave unconnected.

Table 16: Power Interface

PIN NAME	PIN NUMBER	DESCRIPTION
VDD1	B17, C22, E8, E10, M22, U5, AB14, AB18, AE3	2.5 V Supply Voltage.
VDD2	A3, A12, A14, B5, B24, E6, E15, E19, E21, E22, F5, G5, H5, H22, L22, M5, N22, T5, V5, W22, Y22, AA5, AA22, AB7, AB13, AB17, AB21, AB22, AD2, AF19	3.3 V Supply Voltage.
VSS	A2, A6, A18, B1, B21, B25, C1, D4, D24, D26, E5, E7, E9, E11, E12, E13, E14, E16, E17, E18, E20, F22, G22, J5, J22, K5, L5, L11, L12, L13, L14, L15, L16, M11, M12, M13, M14, M15, M16, N5, N11, N12, N13, N14, N15, N16, P5, P11, P12, P13, P14, P15, P16, P22, R5, R11, R12, R13, R14, R15, R16, R22, R24, T11, T12, T13, T14, T15, T16, T22, U22, V22, W5, Y5, AB3, AB5, AB6, AB8, AB9, AB10, AB11, AB12, AB15, AB16, AB19, AB20, AB23, AC3, AD15, AD26, AE26, AF24	Ground

3. Functional Description

3.1 RoX-II Interface

The switch system is a 24-port 10/100 Mbit/s switch with two Gigabit Ethernet ports. This system utilizes Allayer's proprietary RoX-II architecture, which is an improved version of the original RoX-I Ring structure. The RoX-II has a higher bandwidth and built-in Layer 3 capabilities.

The RoX-II Ring is composed of a data ring and a control ring. The data ring is used to transfer frame data, MIB events, as well as system configuration and status report messages. The control ring is used to communicate RoX-II Ring protocol messages among the devices to set up switch backbone resources for the data transfer on the data ring. Each device on the ring has an input interface for receiving data frames and ring protocol messages from the upstream device, and an output interface for transmitting data frames and ring protocol messages to the downstream device.

The management device (MIB) AL300A, resides on the RoX-II ring. It provides the network management functions for all the devices in the ring. The MIB device collects the network statistics of the switch system as well as provides system configuration to the devices. The CPU interface is provided by the MIB device. This supporting chip, the AL300A, provides a full set of statistical counters to support both SNMP and RMON network management.

3.2 Data Reception

The port will go into the receive-state when RX_DV in the MII interface is asserted. The MII presents the received data in four-bit nibbles that are synchronous to the receive clock (25 MHz or 2.5 MHz). The AL126 will then attempt to detect the occurrence of the Start Frame Delimiter, (SFD / 10101011), pattern. All preamble data prior to SFD is discarded. Once SFD is detected, and the Frame Check Sequence (FCS) is verified, the frame data is forwarded and stored in the buffer of the switch.

3.2.1 Illegal Frame Length

During the receiving process, the MAC will monitor the length of the received frame. Legal Ethernet frames should have a length of no less than 64 bytes and no more than 1548 bytes. Any frames with illegal frame length are discarded.

3.2.2 Long Frames

The AL126 can handle frames up to 1548 bytes. All frames longer than 1548 bytes will be discarded. If the port continues to receive data after the 1548^{th} byte, the port's data will be filtered. If the port is in half-duplex mode, the port will no longer be able to transmit or receive data during the long frame reception.

3.2.3 False Carrier Events

If the Carrier Sense Signal (CRS) in the MII interface is asserted but the receive data valid (RX_DV) signal is not asserted within 16 bit-time (BT), the port is considered to have a false carrier event. The false carrier event is recorded for the MIB counter.

3.2.4 Frame Filtering

The AL126 will make filtering and forwarding decisions for each frame received, based on its frame routing table, VLAN mapping, port state, and the system configuration.

Under the following conditions, received frames are filtered.

1. The AL126 will check all received frames for errors such as symbol error, FCS error, short event, runt, long event, etc. Frames with any kind of error will not be forwarded to their destination port.
2. Any frame heading to its own source port will be filtered.
3. Frames heading to a disabled receiving port will be filtered.
4. If the input buffer of the port is full, the incoming frame will be discarded. It is recommended that flow control be used to prevent any loss of data. If the flow control option is enabled, this event will not occur. The remote station will transmit frames when the input buffer becomes available.
5. If the frame has any security violation, while the security option is enabled at the receiving port.

If the Spanning Tree Protocol is enabled, the AL126 will forward the frame as below.

1. If the port is in the Block-N-Listen state or the Learning state, the frame is forwarded to the CPU when it is a BPDU frame, the frame is discarded otherwise.
2. If the port is in the Forwarding State, the frame is forwarded to the CPU when it is a BPDU frame.

3.3 Frame Forwarding

After a frame is received, its Source Address (SA) and Destination Address (DA) are retrieved. The SA is used to update the port's address table as described previously and the DA is used to determine the frame's destination port.

The Address Lookup Engine will attempt to match the destination address with the addresses stored in the address table. If there is a match found, a link between the source port and the destination port is then established.

If the first bit of the destination address is a "0," the frame is regarded as an unicast frame. The destination address is passed to the Address Lookup Engine which returns a matched destination port number to identify which port the frame should be forwarded to. If the destination port is within the same VLAN of the receiving port, the frame will be forwarded. If the frame is tagged with the IEEE 802.3ac and IEEE 802.1q VLAN tag, and the AL126 is programmed to support tagged VLAN, then tagged VLAN membership is looked up from the VLAN table.

If the destination port does not belong to the VLANs specified at the receiving port, the frame will be discarded. The event will be recorded as a VLAN boundary violation. If a particular VLAN (whether port-based or tagged) has null membership, frames are discarded as well.

There are two ways that the AL126 handles frames with an unknown destination. The forwarding decision is controlled by the Flood Control Option (System Configuration Register 00). If Flood Control is disabled, the frame will be forwarded to all ports (except the receiving port) within the

same VLAN as the receiving port. If the Flood Control Option is enabled, the AL126 will forward the frame only to the uplink port specified at the receiving port.

Note: The AL126 defines a port as either a single port or a trunk, consistent with the IEEE 802.3ad Port Aggregation Standard.

If the port monitoring function is enabled, the frame forwarding decision is also subject to the port monitoring configurations.

If the first bit of the destination address is a "1," the frame will be handled as a multicast or broadcast frame. The AL126 does not differentiate multicast frames from broadcast frames, except with the following reserved bridge management group addresses, as specified in table 3.5 of the IEEE 802.1d standard; GARP, IGMP, ARP and IEEE 802.3ad Port Aggregation MAC control frames. Additionally, IEEE 802.3x Flow Control MAC frames are handled inside the AL126 and never forwarded to any other device, including the CPU. The destination ports of the broadcast frame are all ports within the same VLAN except the source port itself.

If Multicast/Broadcast frame trapping (MCtrap) is enabled, the multicast/broadcast frames will be forwarded to the CPU only.

3.3.1 Broadcast Storm Control

One of the unique features provided by the AL126 is Broadcast Storm Control. This option allows the user to limit the number of broadcast frames into the switch. This option can be implemented on a per-port basis. A threshold number of broadcast frames can be programmed in System Configuration Register, Register 1, MaxStorm.

When Storm Control is enabled and the number of cumulated non-unicast frames is over the programmed threshold, the broadcast frame is discarded. If the Storm Control is disabled or the number of non-unicast frames received at the port is not over the programmed threshold, the AL126 will forward the frame to all the ports (except the receiving port) within the VLANs specified at the receiving port. If the CPU port is within the specified VLAN, the frame will also be forwarded to the CPU.

If Broadcast-Storm-drop (System Configuration Register III, Register 2, FlowCtrlBC) is enabled, the AL126 only drops broadcast frames, but not the multicast frames.

3.3.2 Frame Transmission

The AL126 transmits all frames in accordance with the IEEE 802.3 standard. The AL126 sends the frames with a guaranteed minimum inter-packet (frame) gap (IPG) of 96BT, even when the received frames have an IPG less than the minimum requirement. The AL126 also supports transmission of frames with an IPG of 64BT (set in System Configuration Register III, Register 2, SIPG64).

3.3.3 Preamble Regeneration

During a transmit process, frame data is read out from the memory buffer and is forwarded to the destination port's PHY device in nibbles. Seven bytes of preamble signal (10101010) will be generated first before the SFD (10101011) and frame data is sent, which is then followed by four bytes of FCS. If a frame is sourced from the management engine (AL300A), or a frame is modified by VLAN tag/untag operation, a new FCS is calculated and sent.

Summary of Programmable Control for Transmit and Receive

The control for transmit and receive is on a per-port basis. All options are programmable in the Port Configuration Register (registers 0D to 1C).

- Data Rate and Duplex Mode - this option is a per-port option. Typically, data rate and duplex mode are auto-negotiated. To override these modes, set MDIOCfg[3:0] bits to forced-mode (^b0111), and set PrtCfgMode to the desired setting.
- Flow Control - the flow control option can be selected for full-duplex and half-duplex operations separately. The AL126 uses backpressure (either collision or carrier based) for half-duplex flow control and IEEE 802.3x for full-duplex flow control.

3.4 Half Duplex Mode Operation

For true CSMA/CD (half-duplex) operation, the MAC logic will abort the transmit-process if a collision is detected through the assertion of the collision (COL) signal by the MII. Re-transmission of the frame is scheduled in accordance to IEEE 802.3's truncated binary exponential backoff algorithm. If the transmit process has encountered 16 consecutive collisions, an excessive collision error is reported, and the resulting frame is dropped unless the retry-on-excessive-collision (UltraMAC) option is enabled.

The AL126 provides two non-standard options for collision handling. SuperMAC mode in Register I, System Configuration Register II, Bit 3 provides a more aggressive back-off where the back-off limit is three rather than ten. This will create a more aggressive channel capture behavior than the standard IEEE back-off algorithm.

There is a well-known anomaly channel capture effect, where a top-talker in a CSMA/CD (half-duplex operation) network can capture a significant percentage of available bandwidth. This is better known as "channel-capture" effect. The AL126 provides a non-standard mode Binary Exponential Backoff Select (BebSel, System Configuration Register III, Bit 2) that uses the binary back-off algorithm rather than the standard exponential back-off algorithm to reduce this channel-capture effect.

Please refer to the Flow Control section of this data sheet for the backpressure option in half-duplex mode operation.

3.5 Secure Mode Operation

The AL126 provides security support on a per-port basis. Whenever secure mode is enabled, (Security mode, Register 0D through 1C, Port Configuration Register I, Bit 6) the port will stop learning new addresses and the address table of each port will remain unchanged (i.e. any frame aging function, if enabled, and MAC address learning function, are disabled).

The AL126 provides two levels of security protection. The most severe intrusion protection is disabling a port experiencing an intrusion. AutoSec mode, Register 0, System Configuration Register I, Bit 13, when enabled, disables a port if a frame with an unlearned SA is received at a secured port (security violation). Once the port is disabled, it can only be enabled by network management. Security management is a global option.

An alternative is to enable security at the local port level without the security management. When the AL126 is configured this way, the device will only discard frames that have security violations which will prevent intruders from accessing the network.

Summary of Programmable Registers

- AutoSec (register 0) - this bit sets the global security management option. The AL126 will partition any port that experiences a security violation.
- Security (register 0D to 1C) - this is a port configuration option. When this option is enabled, the port is secured. When the port receives a security violation frame it will discard the frame and disable the port if security management is on.

3.6 Address Learning

The table lookup engine provides the switching information required to route the data frames. The address lookup table is set up through auto address learning (dynamic) or manual entry (static). The static addresses are assigned to the address table by the EEPROM or management device. All static address entries will not be aged or updated by the AL126.

After a frame is received by the AL126, the embedded source address (SA) and destination addresses (DA) are retrieved. The source address retrieved from the received frame is automatically stored in a SA buffer. The AL126 will then check for errors and security violations, and perform a SA search. If there is no error or security violation, the chip will store the source address in the address lookup table. If the SA has been previously stored in another port's SA table, the AL126 will delete the SA from the previously stored location.

The Individual MAC Address is a 48-bit unique MAC address to be programmed or learned. Bit 0 of a SA will be masked, i.e. no multicast SA.

The AL126 provides an on-chip MAC Address-To-PortID/TrunkID table with up to 1K entries for frame destination lookup operations. Optional external SRAM can be used to increase the number of MAC address lookups to 16K. (Note: When 802.1q Tag VLAN support is enabled via QEnable mode, the number of internal MAC address support is reduced to 0.5K, and the external table is reduced to 12K).

The AL126 address table contains both the static addresses input by the CPU or the EEPROM and dynamically learned addresses. It learns the individual MAC addresses from three different sources.

1. Frames received with no errors from the local ports.

2. Frames forwarded from other devices through the ring to the device.
3. The MAC Address Table Convergence message received from other switching devices on the ring. (TCNVG mode, Register 0, System Configuration Register I, Bit 11, controls this function. For IEEE 802.1d compliance, this mode should be enabled).

If a received frame contains a source address that has already been learned in another port's address table but not aged out (e.g. a station was moved from a port to another port of a switch), it will perform the following operation based on the switch's configuration.

- If the security option is selected for the port, the AL126 will consider this a security violation.
- If port is a non-protected port, the AL126 will delete the SA from the previous port's address table and update it to the current port's address table. However, if the SA is an static address entry, the address will not be updated.

3.6.1 Address Aging

A port's MAC address register is cleared on power-up, or hardware reset. If the SA aging option is enabled, the dynamically learned SA will be cleared if it is not refreshed in less than the programmed time. The AL126 MAC address aging is enabled by AgeEN, (Register 0, System Configuration Register, Bit 12).

Summary of Programmable Options for Address Learning

- Address Aging Time - the address aging and aging time can be programmed in the System Configuration II (MaxAge, bits 15~9, register 01). The resolution of the normal address aging is 5.36 seconds at 100 MHz and 6.7 seconds with a 80 MHz system clock. If the SlowAge (register 02, bit 10) bit is programmed to "1," the resolution is 10.72 seconds at 100 MHz and 13.4 seconds with a 80 MHz system clock.
- Static Programmed Addresses - up to twenty static addresses can be programmed in the EEPROM address 76 to FF. Further static addresses can be programmed via the AL300A management engine. See EEPROM section of this document, or the AL300A data sheet for more detail.

3.7 VLAN Support

The AL126 supports both Port Based VLAN, where VLAN membership is determined by the port assignment, and IEEE 802.1q (and IEEE 802.3ac) Tagged VLAN, where the VLAN membership is determined dynamically by the VLAN ID (or VID) embedded in the Tag. The IEEE 802.1q tagged VLAN mode is enabled by the QEnable Bit (Register 3, System Configuration IV).

3.7.1 Port Based VLAN

Each port of the AL126 can be assigned to one or multiple VLANs. Frames from the source port will only be forwarded to destination ports within the same VLAN domain. A broadcast/multicast frame will be forwarded to all ports within the VLAN(s) of the source port except the source port itself. An unicast frame will be forwarded to the destination port only if the destination port is in the same VLAN as the source port. If the destination port belongs to the another VLAN, the frame will be discarded and the event will be recorded as a VLAN boundary violation.

Each port should be assigned with a dedicated uplink port. Unicast frames with unknown destination addresses will be forwarded to the uplink port of the source port. An uplink port can either be a single port or a trunk.

The AL126 provides two VLAN register per ports (register 1D to 2C) for mapping to 32 ports (32-bits). Each register contains a 16-bits bit map (total of 32-bits) to indicate the VLAN group for the port.

The VLAN registers hold a broadcast destination mask for each source port. A “1” will indicate the broadcast frames will be forwarded from the source port to the specified port. Note that the source port bit must be set to “0” within the source port VLAN, because broadcast frames must not be forwarded to the source port.

A set of trunked ports (aggregated group) must belong to the same VLAN. For setting up VLAN for trunking, please see the section on trunking for detail.

Port VLAN Set Up Example

A VLAN set up worksheet is provided in Appendix I. Simply by marking the ports you wish to send broadcast frame to, you can complete the VLAN map easily.

Let’s assume we want to set up two VLAN groups in a sixteen port switch.

Group 1 consists of: 0, 1, 2, 5, 6, 8,10, 11, 12, and 15.

Group 2 consists of: 2, 3, 4, 7, 8, 9, 13, 14, and 15.

Note: It might be easier to mark the VLAN ports first and then delete the source ports that you don’t want the broadcast frames to be returned to.

3.7.2 Tagged VLAN

While port-based VLAN is widely used in the industry, there is no standard that governs its implementation. IEEE 802.1q/802.3ac standard specifies tag-based VLAN. The AL126 also supports this standard compliant tag-based VLAN.

The AL126 supports full 4K VID (VLAN Identification) in the tag, all eight of the user priority values in the tag, and preserves the state of the CFI bit. A ports membership to each VLAN value

is dynamically determined by the VID of the tag in a received frame. If frame is not tagged, then the default VLAN ID of the received port is used to determine the membership.

Each VLAN entry consist of: VID, bit map of VLAN membership of the ports in RoX-II Bus, and tag or untag behavior for each port. Please refer to the AL300A Data Sheet for more information.

VLAN searches are performed by AL126 hardware with external SSRAM, while the table entry for each of the active VID has to be pre-programmed through the indirect resource access registers (register 0x43 ~ 0x47), accessible from the AL300A or reverse EEDIO. The following table shows entry format and its mapping into the indirect access registers.

VID (12 bits)	CPU (1 bit)	Dev 3 (16 bits)	Dev 2 (16 bits)	Dev 1 (16 bits)	Dev 0 (16 bits)
IRAD5, R47		IRAD4, R46	IRAD3, R45	IRAD2, R44	IRAD1, R43
0000_0000_0000	Not Used (Priority-Only Tag)				
0000_0000_0001	M	TTTT_TTTT	TTTT_TTTT	TTTT_TTTT	TTTT_TTTT
0000_0000_0010	M	TTTT_TTTT	TTTT_TTTT	TTTT_TTTT	TTTT_TTTT
1111_1111_1111	M	TTTT_TTTT	TTTT_TTTT	TTTT_TTTT	TTTT_TTTT

In the VLAN tag entry, two bits (“T”) for each physical port (up to 32-ports) will define the “action” on a packet with that VID at that port. The corresponding actions are:

“00” to drop the packet,

“01” to pass the packet without change,

“10” to tag the packet (if not tagged, then tag with ingress port default VID),

“11” to untag the packet (if tagged, then untag).

One bit (“M”) will define whether the management port is in the VLAN; “1” will allow frame forwarding to the management CPU from that VLAN, “0” will not. No tagging/untagging is performed on the frame being sent to the management CPU.

VLAN entries can be set by the indirect resource access command, issued from the AL300A management device or reverse EEDIO interface. Five indirect access data registers should be set as in the diagram above, IRAD[4:1] contains the action bitmap for device[3:0], IRAD5= 2*(zzzzzzzzzzzz)+M, where “zzzzzzzzzzzz” is the 12-bit VID and “M” is the management bit. Indirect access command register, IRAC, should be 0x7000 for VLAN table writing. IRAC should be set after IRAD[5:1].

VID 0 is reserved for priority-only tagged frames, and is treated as if the frame is untagged for VLAN membership rules (the priority field is still used for selecting the proper priority queue). VID value of 0FFF is reserved by the IEEE 802.1 for future use, although the AL126 does not treat VID=0FFF in any special way.

A default priority and tag VID is assigned to each source port (up to 32 physical ports, plus the management port) as the default tag to all the incoming frames on that port. VID lookup is performed at input port and tag/untag operation is performed at the output port, all the 32+1 default tags have to be programmed to each AL126 device through the default tag registers (registers 0x4E ~ 0x6E).

3.8 Priority Queues and User Priority Support

The IEEE 802.1p user priority value in the tag is used to queue a frame to a particular priority queue. The AL126 supports a total of four priority queues and a complete set of controls to manage these queues.

User priority value of 0 ~ 7 in the tag is arbitrarily mapped to any of the four prioritized queues by programming register 7, the Priority Queue Assignment Register. This register maps each of the user priority numbers in the tag to one of the four AL126 priority queues. Even with tagged VLAN mode disabled (QEnable de-asserted), user priorities in the tag field are still used for priority queuing.

Four priority queues can be serviced in Weighted Round-Robin or Strict Priority mode. This mode is controlled by PQWRREn, (Register 2, System Configuration Register III, Bit 1).

When Strict Priority mode is enabled, frames in Queue 3 are serviced until the queue is empty, followed by Queue 2, and so on. While servicing lower priority queues, if a higher priority queue is not empty, the higher priority queue is serviced until empty. In a busy network, the lower priority queues could be starved.

When the Weighted Round-Robin mode is enabled, relative priority of each queue can be programmed in Register 0A, Priority Queue Weighted Round-Robin Control Register. Each queue is serviced, on the average, the relative integer value of each queue. A higher value means the queue is serviced in higher frequency than the lower value queue. A weight of zero has special meaning because the queue with zero value acts as the lowest priority queue even with Weighted Round-Robin mode enabled. This means that all other queues must be empty before a queue with zero weight is serviced.

3.9 Buffer Management and Queue Behavior

The AL126 offers a complete set of controls to manage congestion and real-time multimedia traffic. Each output port queue depth can be set to trigger a programmable threshold, and upon reaching this threshold, certain actions can be taken. This includes dropping frames destined to the congested port on a particular priority queue.

Queue depth control is by port and by queue. These modes of operation are controlled by register 8, Output Queue Management Register I. When both the Queue and the Port Maximum limit control is enabled, then selected action is taken when maximum queue depth is reached. For instance, if Queue 2 is used for voice traffic, where it is desirable to drop voice frames rather than deliver old ones in sustained congestion, Queue 2 would be programmed with Q2MaxLimEn as well as MaxLimEn for all the ports.

Maximum queue depth is programmable for each queue (that is used by all the ports) in Register 9, Output Queue Management Register II. The action taken is controlled by the MaxDrop, Register 8, Output Queue Management Register I, Bit 15. When MaxDrop is enabled, frames are dropped on the respective queue when MaxLim is reached. When MaxDrop is disabled, frames are kept in the input buffers and input port backpressures once the input buffer is full.

The AL126 also maintains a dedicated multicast queue for outgoing multicast frame parking. The transmit frame can be from one of two sources, local or from another device on the RoX-II ring. For an output queue, if the source selected is the multicast queue, the device will set up a channel to copy the frame in the head of the multicast queue to the output queue for transmission.

3.10 IP Multicast Group Support

With the management CPU, the AL126 can support IP multicast as specified in RFC1112. The AL126 will trap the IGMP (internet group management protocol) frames going to the CPU, and the CPU will setup the AL126 multicast forwarding table, based on the multicast group information resolved from the IGMP protocol. After table initialization, the AL126 will forward the IPMC frames to the related ports only, instead of all the ports. The AL126 supports all the possible IP multicast addresses, although only 64 active multicast groups are supported simultaneously by hardware. Since the AL126 performs a multicast DA search based on the full 48-bit address, it can also support private multicast groups other than standard IPMC.

Both the MAC table entry and the multicast group bitmap entry needs to be set in the AL126 to initialize a multicast group. The MAC entry is formatted as <IPMC address: 01-00-5e-xx-xx-xx><IPMC index>, and the IPMC table entry is formatted as <IPMC index><Port bitmap>. It's the CPU's responsibility to assign and maintain the IPMC index. The IPMC Port bitmap is defined the same way as tagged VLAN which allows the IPMC to be used in a tagged VLAN environment. Use only the "pass" and "drop" of the bitmap in a non-tagged application to avoid confusion. See the Tagged VLAN section for details on port bitmap definitions.

Both the MAC table and the IPMC table can be set by a indirect resource access command issued from the AL300A management device or reverse EEDIO interface. Setting the IPMC table is very similar to setting of VLAN tag, only set the IPMC index instead of VID to IRAD5 and use 0x6800 instead of 0x7000 as IRAC. Setting the IPMC address in the table is exactly the same way as setting any MAC entry, only set the IPMC index instead of port number into IRAD1.

3.11 Trunking (Port Aggregation)

The AL126 offers two alternative Port Aggregation methods. Port based trunking is backward compatible to Allayer's RoX-I family of switches (AL100 ~ AL116 series switches) and allows direct mapping of ingress traffic to a particular port in a trunk (aggregation) group. Layer 2 Trunking is an implementation of the IEEE 802.3ad Port Aggregation standard that offers enhanced automatic load balancing algorithm. These two mode of trunking methods are mutually exclusive, and are selected by L2Trunk, Register 0, System Configuration Register I, Bit 3.

3.11.1 Port Based Trunking (Port Aggregation)

The AL126 supports trunking/port aggregation. Port aggregation and trunking basically is a method to treat multiple physical links as a single logical link. The benefit of trunking is to be able to group multiple lower speed links into one higher speed link. For example, four full-duplex Fast Ethernet ports at 200 Mbit/s can be used as one single 800-Mbit/s link. This is very useful for switch to switch, switch to server, and switch to router applications.

The AL126 considers a trunk as a single port entity regardless of the trunk composition.

Two to four ports can be grouped together as a single trunk link in a port-based trunking. The grouping of the ports in the trunk must be from the ports of the same device. A total of two trunks per device can be supported.

In a multiple link trunk, the links within the trunk should have equal amount of traffic in order to achieve maximum efficiency. One of the requirements for transmission is that the frames being transmitted must not be out of order. Therefore, some sort of load balancing among the links of the trunk has to be deployed.

3.11.1.1 Load Balancing

The port-based load balancing method is an explicit port assignment scheme. It requires each individual port to be assigned to a specific link (trunk port) in the trunk. If the port is not assigned, frames might be forwarded to the trunk in random and this could cause the frames to go out of order. The port-based load balancing trunk can be a two, three, or four-port trunk.

During transmit, the frame will be forwarded from the source port to the assigned trunk port. When a frame is received from any one of the trunk ports, it is forwarded to the destination port within the VLAN. In essence, the AL126 treats a trunk as any single port within the same VLAN. If the traffic of the ports is evenly distributed among all the trunk ports, load balancing is achieved and the aggregate bandwidth of the trunk can be as high as 800 Mbit/s (full-duplex).

3.11.1.2 Trunk Configuration

Trunk group configuration is accomplished through programming the configuration registers. The AL126 also provide the capability to trap IEEE 802.3ad frames and allow the CPU to configure the aggregated links based on IEEE recommended protocol exchange.

3.11.1.3 Trunk Port Assignment

The maximum number of trunks for Allayer's RoX-II architecture is eight. The Port Configuration Registers (0D to 1C) provide the ability to designate a port to be a member of a trunk. The trunk can consist of up to four trunk ports. A trunk group must consist of either the top four ports or the bottom four ports. For example, a trunk can consist of either port 0, 1, 2, or 3, or port 4, 5, 6, or 7. Each trunk port's number is in sequence of 00, 01, 10, and 11 corresponding to the order of port of the devices. For example, port 1 and 5 are 01 (See Figure 5).

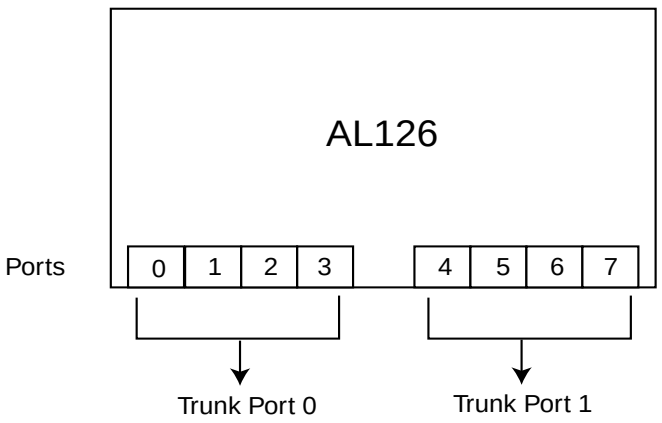

Figure 5 Trunk Port Numbering

3.11.1.4 Port Based Trunk Load Balancing

For port-based load balancing, a trunk port must be assigned to each port for all defined trunks. The port assignment is done by programming Port to Trunk Port Registers (2D to 34). A port assignment worksheet is provided in Appendix II. It is recommended that ports be evenly distributed among all trunk ports to prevent overloading any single trunk port. The following is a procedure to set up the trunk.

1. Select the trunk ports using Port Configuration Registers (0D to 1C) Bit 9.
2. Assign the ports to the Trunk Port Register (2F to 36).

   The port should be assigned to the appropriate trunk using this register. For the trunk port itself, the port assignment should be assigned to itself. A port to trunk port worksheet is provided in Appendix I.
3. Assign the port to a trunk port in the port to trunk port register.

   This is necessary because each port in the group to trunk must be assigned to a trunk port. By assigning the trunk port to itself, broadcast frames will not be sent back to the source port.
4. Assign the ports and the trunk port to the same VLAN using register 1D to 2C.

   The port VLAN grouping should only include the trunk port it is assigned to and no other trunk ports. This is to ensure that broadcast frames will only be forwarded to the assigned port.

Port Based Trunking Load Balancing Example

Note: The specific bits in the register are reference by a "X and Y" notation, where X is the register number and Y is the bit number.

The following is a procedure to design an 8-port switch with a 3-port trunk.

1. The desired trunk ports are 5, 6, and 7. Therefore, the port configuration register bits 17.9, 19.9, and 1B.9 are set to 1.
2. We want to assign port 0 to trunk port 5, port 1 and 3 to trunk port 6, and port 2 and 4 to trunk port 7. The trunk ports are 5, 6, and 7; therefore the trunk number is 1. The assignment of the port to trunk port register bits should therefore be;

   2F.3= 0, 2F.2= 1

   30.3= 1, 30.2= 0

   31.3= 1, 31.2= 1

   32.3= 1, 32.2= 0

   33.3= 1, 33.2= 1
3. For the trunk ports, trunk ports should be assigned with their own port number in the port to trunk port register. The port to trunk port bits should be;

   34.3= 0, 34.2= 1

   35.3= 1, 35.2= 0

   36.3= 1, 36.2= 1
4. Assigning VLAN. The VLAN map should be assigned as shown.

All bits are set to "1" while the bits 1E.6 and 1E.7 are set to "0" because port 0 is assigned to port 5. All the other ports are set up similarly. Bits 15 through 8 are reserved and should be set to "0" for all VLAN mapping registers.

Appendix I and II provide work sheets for port to trunk port and VLAN assignment.

Table 17: VLAN Mapping for Port Based Load Balancing Trunk

PORT	BIT	PORT 0/REG. 1E	PORT 1/REG. 20	PORT 2/REG. 22	PORT 3/REG. 24	PORT 4/REG. 26	PORT 5/REG. 28	PORT 6/REG. 2A	PORT 7/REG. 2C
7	**7**	0	0	1	0	1	0	0	0
6	**6**	0	1	0	1	0	0	0	0
5	**5**	1	0	0	0	0	0	0	0
4	**4**	1	1	1	1	0	1	1	1
3	**3**	1	1	1	0	1	1	1	1
2	**2**	1	1	0	1	1	1	1	1
1	**1**	1	0	1	1	1	1	1	1
0	**0**	0	1	1	1	1	1	1	1

3.11.2 L2 Trunking (Port Aggregation)

L2 Trunking automatically load-balances among its member ports through the use of unique and statistical methods, and provides link resiliency (link-fail-over function) when one or more of the links in a trunk group fails. L2 Trunking is selected by L2Trunk, Register 0, System Configuration Register I, Bit 3.

3.11.2.1 L2 Trunk Configuration

Trunk (Port Aggregation) configuration is accomplished through programming the configuration registers. The AL126 provides the capability to trap IEEE 802.3ad frames and allows the CPU to configure the aggregated links based on IEEE recommended protocol exchange.

3.11.2.2 L2 Trunk Port Assignment

Each device supports up to two trunks, and each trunk can have two through eight ports as its members. A total of eight trunk groups in four switching devices on the RoX-II are possible. Each device must be aware of other devices trunk configuration. These are configured in the Register 2E through Register 31, Layer 2 Trunking Assignment Registers I through IV. Unlike the port-based trunking groups, L2 Trunk group is programmed via a bit-map of member ports for each trunk.

3.11.2.3 L2 Trunk Load Balancing

The load balancing algorithm uses randomized seed based on the Destination MAC address, Source MAC Address, both Destination and Source MAC Addresses, or non-randomized DA and SA. Each trunk groups randomization method can be selected in Register 32, Layer 2 Trunking Protocol Register. This randomization sequence creates a 12-bit value, which is used as a random seed value for the load balancing algorithm. L2KeySel, Register 1, System Configuration Register II, bits 1~0, is used to select which 3-bit field to use for the random seed value. Normally this register doesn't need to be adjusted for normal operation.

The AL126 uses a robust and unique algorithm to ensure statistically equal loads whether a trunk group has 2, 3, 4,.. 8 member ports in the group.

3.11.2.4 Link Fail Over

The AL126 supports link fail-over when one or more of the member ports is in trunk fail. This feature can be enabled by L2FailEn in Register 3, System Configuration Register IV, Bit 6. If a member port in a trunk experiences a link failure, the AL126 detects this condition and divides the frame-flow that used to be assigned to the failed port to other member ports. The load balancing algorithm also applies in this case, which statistically ensures equal load on the rest of the member ports. If a link is healed, then only the frame-flow that was re-assigned to other member ports is restored back on the original link. When frame-flow is restored onto the original link, the queue needs to be flushed to avoid mis-ordered frames. This flushing mechanism can be selected by setting L2Timer value in Register 3, System Configuration Register IV, Bits 5~4. This Link Fail-Over feature is only available in L2 trunking mode.

3.12 Spanning Tree Support

The AL126 has the capability to support implementation of the Spanning Tree Protocol. All ports can be programmed to be in the port state as required by the Spanning Tree Protocol.

If the Spanning Tree Protocol option is enabled, the AL126 will forward the frame as below.

- If the port is in the Block-N-Listen State or the Learning State, the frame is forwarded to the CPU if it is a BPDU frame, the frame is discarded otherwise. All outgoing frames except outgoing BPDUs will be masked from the path to the PHY.
- If the port is in the Forwarding State, the frame is forwarded to the CPU if it is a BPDU frame. All source addresses of the incoming frames from the PHY will be learned and then forwarded based on the switch routing decision. All outgoing frames will be transmitted to the PHY.
- If the port is in the Learning State, all source addresses of the incoming frames from the PHY will be learned. All incoming frames except incoming BPDUs from the PHY will be discarded after being learned, all outgoing frames except outgoing BPDUs will be masked from the path to the PHY.

3.13 Flow Control

The AL126 can operate at two different modes, half- and full-duplex. Each port can operate at either full or half-duplex and be configured to have flow control enabled or no flow control independently on a per-port basis.

3.13.1 Half Duplex (Backpressure)

If the half-duplex flow control option is elected, backpressure will be used for flow control. Whenever the receive frame buffer of a port is full, the MAC of the port will start sending a JAM signal through the port. The remote station will defer transmission after sensing the JAM signal. Backpressure flow control is applied to ensure that there is no dropped frames. The AL126 supports two types of backpressure, collision based and carrier based.

Carrier based backpressure is generated by the AL126, when the switch port's frame buffer is full. The AL126 will cease to jam the line when the port has buffer space available for frame reception. The IPG of the jamming signal can be programmed to be either 64BT or 96BT.

Collision based backpressure is generated by the AL126 only when the switch port receives a frame and its frame buffer is full. The AL126 will cease to jam the line when the line is idle.

The carrier based backpressure has several advantages over collision based backpressure.

1. Collision based backpressure can cause late collisions.
2. After 16 consecutive collisions, the MAC could drop frames. The AL126 has an option not to drop frames after 16 collisions. However, the end terminal may still drop frames.

Therefore, we recommend the use of carrier based backpressure as the preferred method for half-duplex flow control. In this mode of operation, we also recommend that the IPG of the JAM signal should be set at 64BT. This is because if the IPG is at 96BT, the far end terminal might still be able to transmit frames and cause collisions. The excessive collisions can cause frames to be dropped.

The AL126 also supports collision based backpressure for customers that prefer that type of backpressure.

3.13.2 Full Duplex Flow Control (802.3x)

In the full-duplex mode, the AL126 will transmit and receive frames in accordance to IEEE 802.3x. The transmission channel and the receiving channel operate independently.

In the incoming direction, whenever the receive frame buffer of a port is full, the MAC of the port will send out a PAUSE frame with its delay value set to maximum. The PAUSE frame will deter any incoming frame from flowing into the port. After the occupancy of the receiving frame buffer is reduced below the FlowControlOff threshold, the MAC of the port will then send out a PAUSE frame with delay value set to zero, to resume receiving the incoming frame flow.

In the outgoing direction, whenever a incoming PAUSE frame with a non-zero delay value is received through a port, the MAC of the port will stop the next frame transmission after the ongoing frame transmission is finished, and start its pause timer. It will resume frame transmission either after the pause timer expired or when a PAUSE frame with a zero delay value is received. The PAUSE frame is defined by a special DA, type, and OP code.

When 802.3x flow control option is elected, the device will program the appropriate bit in the auto-negotiation capability field. When the AL126 is used in the full-duplex mode, it is recommended that flow control should be turned on to prevent the buffer from overflow and loss of frames. If the connected device has no 802.3x capability, then the link is recommended to be set at half-duplex.

3.13.3 Special Frame Identification and Trapping

The AL126 is capable of identifying special frames and forwards them to the CPU if required. The AL126 inspects the pay load of the incoming frames, and if it is one of the frame types selected (register 03), it will then forward the frame to the CPU. The following types of frame trapping are supported by the AL126 in addition to BPDU frames.

NAME	COMMENT
IPMC	IP Multicast Mapping Frames. The AL126 directly supports multicast addresses. All that is needed to support IP multicast is a procedure for mapping IP host addresses to an ethernet multicast address by placing the low-order 23 bits of the IP address into the low order 23 bits of the ethernet multicast address 01-00-5E-00-00-00 (hex). Because there are 28 significant bits, more than one host group address may be mapped to the same ethernet multicast address.
IGMP	Internet Group Management Protocol. This is for internet multicast support for bridges.
GARP	Generic Attribute Registration Protocol. This is required for 802.1p and 802.1q support.
ARP	Address Resolution Protocol. This is required for TCP/IP stack.
802.3ad	Controls Frames for 802.3ad Trunking Control.

3.14 Queue Management

The AL126 supports four priority queues on each port of the AL126. All frames that come into the AL126 are stored into the shared memory buffer and are lined up in the transmission queues of the corresponding destination port. The priority is assigned by the tag contained in the received frames. The definition of the priority can be programmed via register 07. The AL126 will transmit the frames based on the priority queue assigned and not on priority tag.

The AL126 provides two modes of priority scheduling (selectable by register 02); Strict Priority Scheduling and Weighted Priority Scheduling. Strict Priority Scheduling is a simple scheduling scheme that will schedule the highest priority frames to be transmitted first. The shortcoming of this method is low priority frames might be starved of bandwidth if there is very high traffic in the high priority frames.

The alternative is Weighted Priority Scheduling which assigns weight to different levels that provide low priority frames a fair chance of accessing the bandwidth. The weight of each priority can be programmed via register 09.

3.14.1 Congestion Control

The AL126 provides two options on congestion control. When a port is congested, the AL126 will backpressure or use flow control to deter further traffic from entering the switch. Although this is a good way to prevent frame loss, it may not be desirable for some applications. The AL126 therefore allows users to program any queue to be able to drop frames when the number of the frames reaches the watermark programmed in that queue.

For broadcast or multicast frames, the AL126 also provides the capability of dropping frames from the 10 Mbit/s multicast queue to keep the 100 Mbit/s forwarding speed.

3.15 Uplink Port

The uplink port provides a way to connect the switch with a repeater hub, a workgroup switch, a router, or any type of interconnecting device compliance with IEEE 802.3 standards. The CPU port can also be designated as an uplink port.

If flood control is enabled, the AL126 will send all frames with unmatched DA and multicast/ broadcast frames to the uplink port. It is very important that each port is assigned to an uplink port via the Port Configuration Register (0D to1C) if uplink is disabled, or data frames might be lost. The uplink port should be configured to be within the same VLAN as the source port. If the uplink port is not a member of the VLAN, the broadcast or multicast frames will not be forwarded to its designated uplink port. Multiple VLANs can share the same uplink port.

The AL126 will direct the following frames to the uplink port.

1. Frames with a unicast destination address that does not match with any MAC address stored in the switch.
2. Frames with a broadcast/multicast destination address if the uplink port is in the same VLAN.

When configuring an uplink port, the uplink port should designate itself as the uplink port.

Summary of Programmable Register

- Trunk Port Designation (register 0D to 1C) - this register provides the option of designating the uplink port as either a port, a trunk or a CPU. See details in register descriptions.

3.16 Port Monitoring

The AL126 supports port monitoring. This feature provides complete network monitoring capability at 100 Mbit/s. A copy of egress (TX) data and ingress (RX) data of the monitored port is sent to their respective snooping ports.

The monitored port is selected by register 06. The AL126 allows the transmit and receive data to be monitored by different snooping ports. The snooping ports are also selected by register 06.

Summary of Programmable Register

- Port Monitoring Register (register 06) - this register selects the target monitored port and the snooping port. A 5-bit Port_ID designates the port. The format of the Port_ID is [Dev_ID].[Port_ID]. [Dev_ID] is the device number and [Port_ID] is the port number.

3.17 Media Independent Interface (MII)

The MAC of each port of the AL126 is connected to the PHY through the standard MII interface. For reception, the received data (RXD) is sampled by the rising edge of the receive clock (RX_CLK). Assertion of the receive data valid (RX_DV) signal will cause the MAC to look for the start of SFD. For transmission, the transmit data enable (TX_EN) signal is asserted when the first preamble nibble is sent on the transmit data (TXD) lines. The transmit data is clocked out by the rising edge of the transmit clock (TX_CLK).

Prior to any transaction, the AL126 will output thirty-two bits of “1” as preamble signal. After the preamble, a “01” signal is used to indicate the start of the frame.

For a write operation, the device will send a ”01” to signal a write operation. Following the “01” write signal will be the five-bit ID address of the PHY device and the 5-bit register address. A “10” turn around signal is then used to avoid contention during a read transaction. After the turn around, the 16-bit of data will be written into the register. After the completion of the write transaction, the line will be put in a high impedance state.

For a read operation, the AL126 will output a “10” to indicate read operation after the start of frame indicator. Following the “10” read signal will be the 5-bit ID address of the PHY device and the 5-bit register address. Then, the AL126 will cease driving the MDIO line, and wait for 1-bit time. During this time, the MDIO should be in a high impedance state. The device will then synchronize with the next bit of “0” driven by the PHY device, and continue on to read 16-bits of data from the register. The detail timing requirements on PHY management signals are described in the section “Timing Requirements.”

The MDIO port can be disabled through the port configuration register. This allows the engineers to use the 100Base-TX transceiver without auto-negotiation capability or MII to MII interconnect. In this mode of operation, the PHY has no communication with the AL126. Therefore, the AL126 will assert the link status as soon as initialization is completed and assumes the connected PHY is operating at the specified operating duplex mode and speed.

3.18 PHY Management

The AL126 supports transceiver management through the serial MDIO and MDC signal lines. The device provides two modes of management, master and slave mode. In the master mode of operation, the AL126 controls the operation modes of the link while the PHY controls the operating mode in the slave mode.

3.18.1 PHY Management Master Mode

In this mode, the AL126 will continuously poll the status of the PHY devices through the serial management interface, without CPU intervention. The device will also configure the PHY capability fields to ensure proper operation of the link. The CPU can access any registers in the PHY devices through the CPU interface provided by the management device, the AL300A.

The configuration of the link is automatic. The link capability is programmed by the AL126 through the port configuration register. The AL126 reads from the standard IEEE PHY registers to determine the auto-negotiated operating speed and mode. If there is a need to manually set the operation mode because of flow control and cabling issues, the AL126 can set the port operation mode manually through the MDIO interface (see the EEPROM section for programming the AL126).

If a CPU is used to reprogram the PHY via the AL126, the operating mode is changed without reset or powered down. In order to ensure the link is operating in the desired mode, the PHY should renegotiate either through a command or by unplugging the RJ45.

3.18.2 PHY Management Slave Mode

In the slave mode, the PHY controls the programming of the operating mode. The AL126 will continuously poll the status of the PHY devices through the serial management interface, without CPU intervention to determine the operation mode of the link. The CPU can access any registers in the PHY devices through the CPU interface provided by the management device. This mode of PHY management is very useful for unmanaged switches. The operating mode of the link can be changed by programming the mode pin of the PHY through a jumper without any assists from the CPU.

The AL126 also supports 100Base-TX transceivers without a MDIO interface or MII to MII interface. When MDIO is disabled, the AL126 will operate in the operation mode specified in the Port Configuration Register (0D to 1C).

3.18.3 Non Auto-negotiation Mode

The AL126 can also turn off the auto-negotiation capability of the PHY. When auto-negotiation is turned off, the AL126 is in the slave mode and the transceiver will determine the link's operating mode.

3.18.4 Other PHY Options

Some Legacy Fast Ethernet devices and low cost devices have no auto-negotiation capability. In those cases, the transceiver will not be able to perform auto-negotiation. The switch transceiver will typically do a parallel detection and update the information in the transceiver's register. Unfortunately, such register addresses are vendor specific. The AL126 provides a register (register 05) to specify the register address of the PHY for the AL126 to read. The AL126 will read from that register and configure the port operation accordingly.

Register 05 also provides some additional flexibility's for some of the PHYs in the market. In general, the system designer should set the ID of the PHY devices as 0 for port 0, 1 for port 1, etc., and 7 for port 7. The Lucent Quad PHY, LU3X54FT, utilizes PHY address 00000 as a broadcast address. Bit 1 of register 05 allows the AL126 to start with PHY address 01000. This provision allows the engineers to work around PHYs that have problems handling address 00000.

Quad PHYs in the market today have 2-port ordering in the chip pinout, clockwise and counter clockwise. Register 05, Bit 2, programs the AL126 port order to go in either direction. This provision enables engineers to implement designs with any PHY easily.

There is also a slow MDIO clock (17 KHz) available for PHYs that are not capable of handling a high speed MDIO clock.

If for some reason, the transceiver is connected to a device and that device fails to auto-negotiate, the AL126 will default the data rate and duplex mode to the default setting in the port configuration register.

3.19 SGRAM Interface

All ports of the AL126 work in Store-And-Forward mode so that all ports can support both 10 Mbps and 100 Mbps data speed. The AL126 utilizes a central memory buffer pool which is shared by all ports within the same device. After a frame is received, it is passed across the SGRAM interface and stored in the buffer. During transmit, the frame is retrieved from the buffer pool and forwarded to the destination port.

The AL126 is designed to use 8-Mbit SGRAM or 16-Mbit SGRAM for cost and performance. SGRAM essentially is a SDRAM. Dynamic memories must be refreshed periodically to prevent data loss. The SGRAM has auto-refresh which it also uses to refresh the address counter. The SGRAM auto-refresh command generates a pre-charge command internally in the SGRAM. The AL126 will insert an auto-refresh command once every 15 us.

The SGRAM is accessed in page burst access mode for very high speed access. This burst mode is repeatedly accessing to the same column. If the burst mode reaches the end of the column address, then it wraps around to the first column address (=0) and continues to count until interrupted by a new read/write, pre-charge, or burst stop command.

The AL126 will initialize the SGRAM automatically. It pre-charges all banks and inserts eight auto-refresh commands. It will also program the mode registers for the AL126 read and write operations.

3.20 EEPROM Interface

The AL126 provides three functions with the EEPROM interface; system initialization, obtaining system status, and reconfiguration of the system in real time.

3.20.1 System Initialization

The EEPROM interface is provided so the manufacturer can provide a pre-configured system to their customers. Customers can change or reconfigure their system and retain their preferences. The EEPROM contains configuration and initialization information, which is accessed at power up and reset.

The AL126 uses the 24C02 serial EEPROM device (2048 bits organized as 256 bits x 8). The organization of EEPROM data is shown in Table 18.

During start up, the AL126 will try to detect the presence of the EEPROM. If no EEPROM is present, the AL126 will be initialized by the CPU attached to the management device on the RoX-II ring. If no initialization command is received, the device will not operate.

If the reset pin is held low, the AL126's EEPROM interface will go into a high impedance state. This feature is very useful for reprogramming the EEPROM during installation or reconfiguration.

There are two ways that the EEPROM can be reprogrammed, by an external parallel port or the CPU residing on the ring. For reprogramming using a parallel port, a signal is used to hold the RESET pin low; the EEPROM interface will then be in the high impedance state. An external device can then program the EEPROM through the EDIO and the ECLK pins. The EEPROM address should be set to be the same as the device ID with A2 (EEPROM) grounded. For example, EEPROM of device 0 has an address of 000 and device 1 has an address of 001.

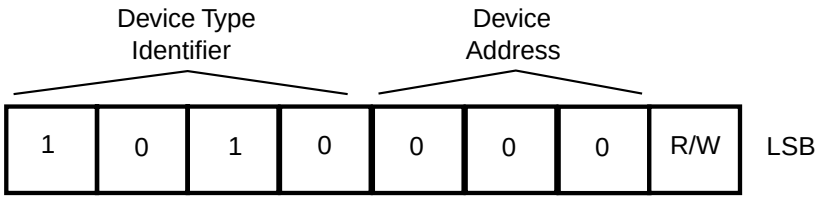

Figure 6 EEPROM Address Format

3.20.2 Start and Stop Bit

The write cycle is started by a start bit and ended by a stop bit. A start bit is a transition from high to low of EEDIO when EEC is high. The operation terminates when EEDIO goes from low to high when EEC is high (Figure 7). Following a start condition, the writing device must output the address of the EEPROM. The most significant four bits of the EEPROM address are the device type identifier. These four bits are 1010. The EEPROM device address should be set to the device ID number.

The EECLK is an output from the AL126. EEDIO is an input if the AL126 is reading the EEPROM or an output if it is writing to it. (See Figures 8 and 9).

When accessing the EEPROM, the reset pin has to be held low before the writing operation can begin.

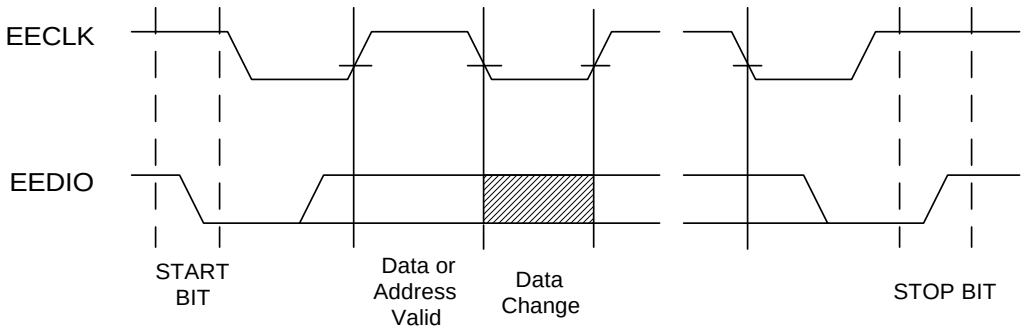

Figure 7 Start and Stop Bit

3.20.3 Write Cycle Timing

The EECLK is an output from the AL126 while EEDIO is a bi-directional signal. When accessing the EEPROM, the reset pin has to be held low or initialization of the AL126 must be finished before a write operation can begin. A typical write operation is shown in Figure 8.

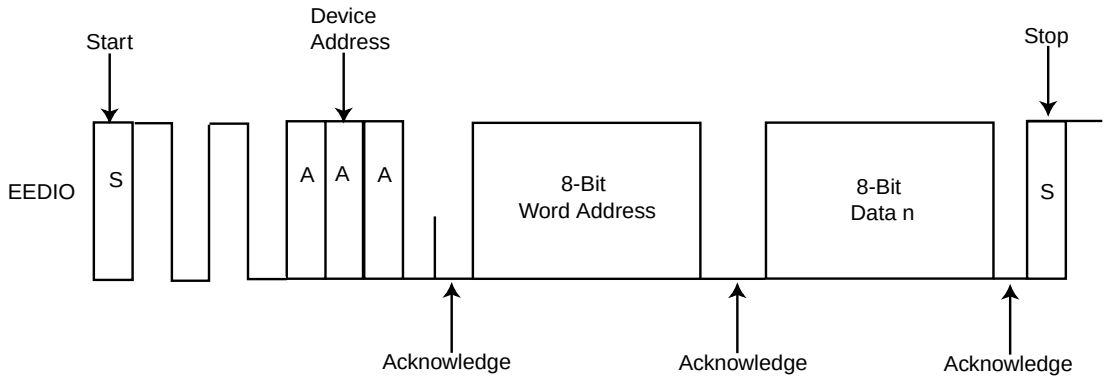

Figure 8 Typical Write Cycle

3.20.4 Read Cycle Timing

Read operations are initiated in the same manner as write operations, with the exception that the R/W bit of the EEPROM address is set to a “1.”

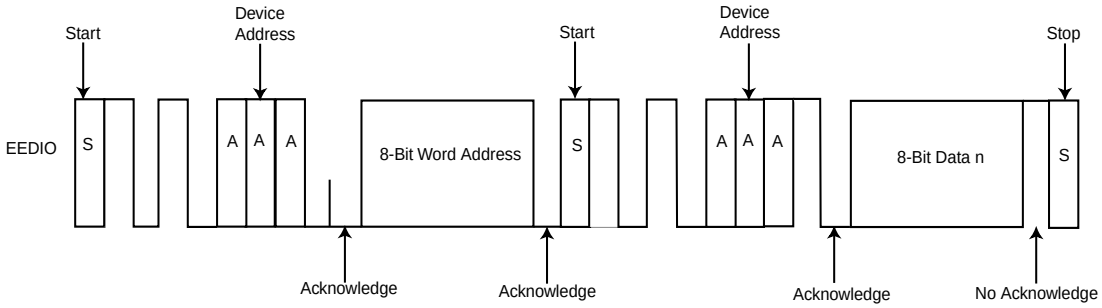

Figure 9 Typical Read Cycle

3.20.5 Reprogramming the EEPROM Configuration

There are two ways that the system can be reconfigured. Figure 10 shows an application using the parallel interface to reprogram the EEPROM. In this application, the parallel port holds the reset pins low, which forces the EEDIO pins to go in to high impedance. Once the pins are in high impedance, the EEPROM can now be programmed by the parallel port.

Once the parallel port releases the reset pins, the devices will start to download the EEPROM data and reconfigure the devices.

An alternate way of reconfiguring the system is to input the data directly into the AL126. After initialization, the EEPROM interface can act as a virtual EEPROM. In order for this method to work, the EEPROM's address must be 0XX, the AL126's address will be 1XX. The customer can now program the AL126 as an EEPROM. The read and write timing is the same as an EEPROM.

Because you read as well as write to the AL126, status of the register can be read from the AL126. This will serve as a very useful tool for diagnostic of an unmanaged switch.

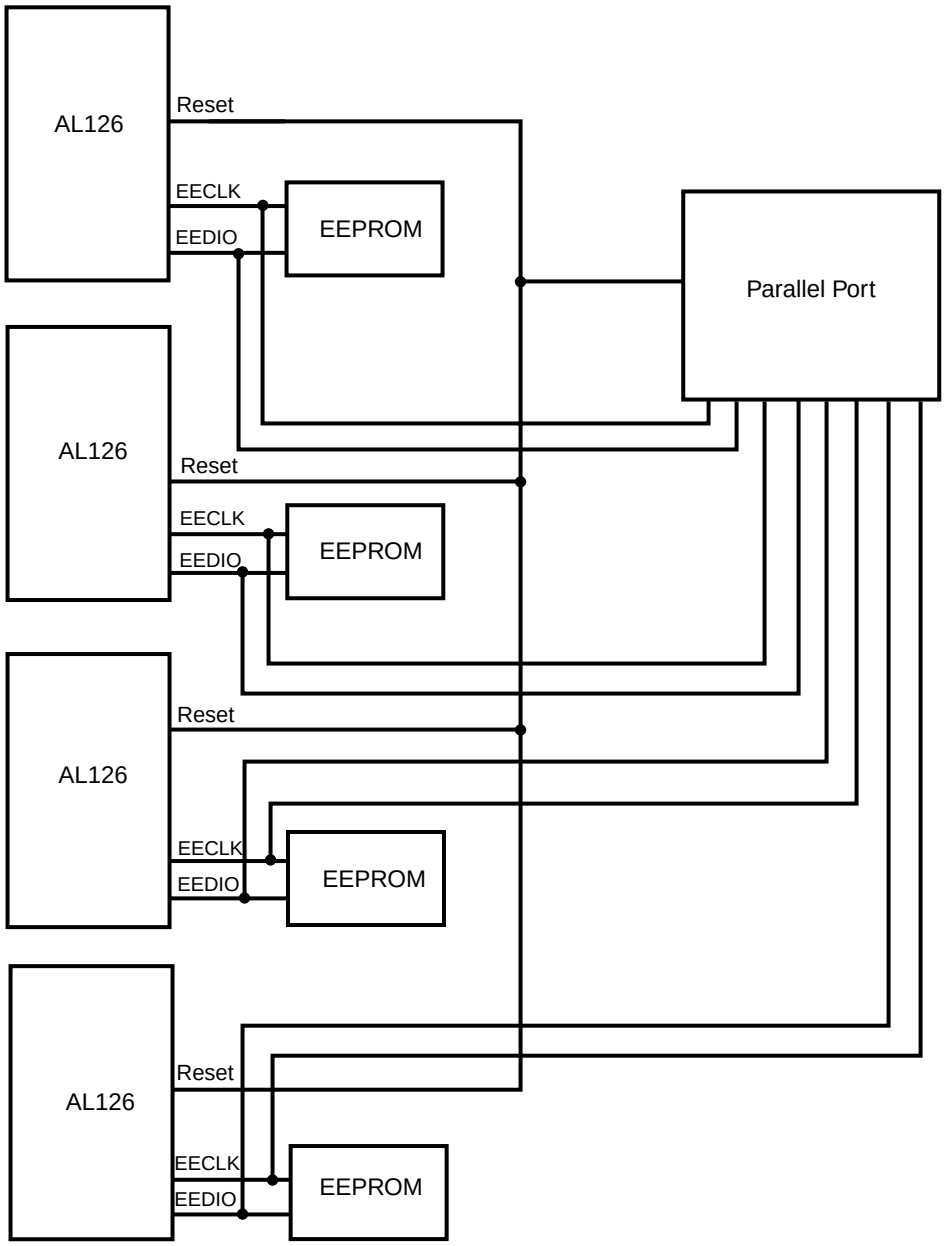

Figure 10 Programming the EEPROM with a Parallel Port

3.20.6 EEPROM Map

Note: The specific bits in the register are referenced by a "X and Y" notation, where X is the register number and Y is the bit number.

Table 18 shows the EEPROM addresses map cross-referenced to the register/bit set of the AL126.

- Addresses 00 through 73 are for configuring the device. They are downloaded by the AL126 during reset or power up.
- Address 75 indicates the last address entry. If no static address is used in the switch, the address 75 should be programmed.
- Addresses 76 to FF are used for programming the explicit address entry.

The format of the address is shown as follows; YXXXXX represents:

- If Y=0 then XXXXX is the 5-bit individual port ID number.
- If Y=1, then XXXXX can be either the trunk port represented by 00 followed by the 3-digit [trunk ID] number, or the CPU port represented by 11ZZZ where ZZZ is don't care.

Table 18: Static Address Entry Format for EEPROM

EEPROM ADDRESS	BIT							
	7	6	5	4	3	2	1	0
76	Reserved (Must be all zero)							
77	Reserved		Port ID YXXXXX or Trunk ID YXXYYY					
78	MAC Address [47:40]							
79	MAC Address [39:32]							
7A	MAC Address [31:24]							
7B	MAC Address [23:16]							
7C	MAC Address [15:8]							
7D	MAC Address [7:0]							

Table 19: AL126 EEPROM Mapping

EEPROM PHYSICAL ADDRESS	DESCRIPTION
00-01	System Configuration I
02-03	System Configuration II
04-05	System Configuration III
06-07	System Configuration IV
08-09	System Performance Tuning
0A-0B	Vendor Specific PHY
0C-0D	Port Monitoring Configuration
0E-0F	Priority Queue Assignment
10-11	Output Queue Management I
12-13	Output Queue Management II
14-15	Priority Queue Weight Round Robin
16-17	RoX-II Control I
18-19	RoX-II Control II
1A-1B	Port 0 Configuration I
1C-1D	Port 0 Configuration II
1E-1F	Port 1 Configuration I
20-21	Port 1 Configuration II
22-23	Port 2 Configuration I
24-25	Port 2 Configuration II
26-27	Port 3 Configuration I
28-29	Port 3 Configuration II
2A-2B	Port 4 Configuration I
2C-2D	Port 4 Configuration II
2E-2F	Port 5 Configuration I
30-31	Port 5 Configuration II
32-33	Port 6 Configuration I
34-35	Port 6 Configuration II
36-37	Port 7 Configuration I
38-39	Port 7 Configuration II

Table 19: AL126 EEPROM Mapping (Continued)

3A-3B	Port 0 VLAN Map I
3C-3D	Port 0 VLAN Map II
3E-3F	Port 1 VLAN Map I
40-41	Port 1 VLAN Map II
42-43	Port 2 VLAN Map I
44-45	Port 2 VLAN Map II
46-47	Port 3 VLAN Map I
48-49	Port 3 VLAN Map II
4A-4B	Port 4 VLAN Map I
4C-4D	Port 4 VLAN Map II
4E-4F	Port 5 VLAN Map I
50-51	Port 5 VLAN Map II
52-53	Port 6 VLAN Map I
54-55	Port 6 VLAN Map II
56-57	Port 7 VLAN Map I
58-59	Port 7 VLAN Map II
5A-5B	VLAN Map Extension I
5C-5D	CheckSum
5E-5F	VLAN Map Extension II
60-61	Port 0 to Trunk Port Assignment
62-63	Port 1 to Trunk Port Assignment
64-65	Port 2 to Trunk Port Assignment
66-67	Port 3 to Trunk Port Assignment
68-69	Port 4 to Trunk Port Assignment
6A-6B	Port 5 to Trunk Port Assignment
6C-6D	Port 6 to Trunk Port Assignment
6E-6F	Port 7 to Trunk Port Assignment
70-71	Testing Control I
72-73	Testing Control II
74-75	Last Entry Location
76-7D	Static Entry 0

Table 19: AL126 EEPROM Mapping (Continued)

7E-85	Static Entry 1
86-8D	Static Entry 2
8E-95	Static Entry 3
96-9D	Static Entry 4
9E-A5	Static Entry 5
A6-AD	Static Entry 6
AE-B5	Static Entry 7
B6-BD	Static Entry 8
BE-C5	Static Entry 9
C6-CD	Static Entry 10
CE-D5	Static Entry 11
D6-DD	Static Entry 12
DE-E5	Static Entry 13
E6-ED	Static Entry 14
EE-F5	Static Entry 15
F6-FD	Static Entry 16
FE-FF	Reserved

3.21 Register Descriptions

Table 20: Register Description

REGISTER ID	REGISTER NAME	REVEPADDR
00	System Configuration I	[00, 01]
01	System Configuration II	[02, 03]
02	System Configuration III	[04, 05]
03	System Configuration IV	[06, 07]
04	System Performance Tuning	[08, 09]
05	Vendor Specific PHY Status	[0a, 0b]
06	Port Monitoring Configuration	[0c, 0d]
07	Priority Queue Assignment	[0e, 0f]
08	Output Queue Management I	[10, 11]
09	Output Queue Management II	[12, 13]
0A	Priority Queue Weight Round-Robin	[14, 15]
0B	RoX-II Control I	[16, 17]
0C	RoX-II Control II	[18, 19]
0D	Port 0 Configuration I	[1a, 1b]
0E	Port 0 Configuration II	[1c, 1d]
0F	Port 1 Configuration I	[1e, 1f]
10	Port 1 Configuration II	[20, 21]
11	Port 2 Configuration I	[22, 23]
12	Port 2 Configuration II	[24, 25]
13	Port 3 Configuration I	[26, 27]
14	Port 3 Configuration II	[28, 29]
15	Port 4 Configuration I	[2a, 2b]
16	Port 4 Configuration II	[2c, 2d]
17	Port 5 Configuration I	[2e, 2f]
18	Port 5 Configuration II	[30, 31]
19	Port 6 Configuration I	[32, 33]
1A	Port 6 Configuration II	[34, 35]

Table 20: Register Description (Continued)

1B	Port 7 Configuration I	[36, 37]
1C	Port 7 Configuration II	[38, 39]
1D	Port 0 VLAN Map I	[3a, 3b]
1E	Port 0 VLAN Map II	[3c, 3d]
1F	Port 1 VLAN Map I	[3e, 3f]
20	Port 1 VLAN Map II	[40, 41]
21	Port 2 VLAN Map I	[42, 43]
22	Port 2 VLAN Map II	[44, 45]
23	Port 3 VLAN Map I	[46, 47]
24	Port 3 VLAN Map II	[48, 49]
25	Port 4 VLAN Map I	[4a, 4b]
26	Port 4 VLAN Map II	[4c, 4d]
27	Port 5 VLAN Map I	[4e, 4f]
28	Port 5 VLAN Map II	[50, 51]
29	Port 6 VLAN Map I	[52, 53]
2A	Port 6 VLAN Map II	[54, 55]
2B	Port 7 VLAN Map I	[56, 57]
2C	Port 7 VLAN Map II	[58, 59]
2D	VLAN Map Extension I	[5a, 5b]
2E	VLAN Map Extension II	[5c, 5d]
2F	Port 0 to Trunk Port Assignment/Layer 2 Trunking Assignment I	[5e, 5f]
30	Port 1 to Trunk Port Assignment/Layer 2 Trunking Assignment II	[60, 61]
31	Port 2 to Trunk Port Assignment/Layer 2 Trunking Assignment III	[62, 63]
32	Port 3 to Trunk Port Assignment/Layer 2 Trunking Assignment IV	[64, 65]
33	Port 4 to Trunk Port Assignment/Layer 2 Trunking Protocol Select	[66, 67]
34	Port 5 to Trunk Port Assignment	[68, 69]
35	Port 6 to Trunk Port Assignment	[6a, 6b]

Table 20: Register Description (Continued)

36	Port 7 to Trunk Port Assignment	[6c, 6d]
37	Testing Control I	[6e, 6f]
38	Testing Control II	[70, 71]
39	System Status Register	[72, 73]
3A	Port 0 Operation Status	[74, 75]
3B	Port 1 Operation Status	[76, 77]
3C	Port 2 Operation Status	[78, 79]
3D	Port 3 Operation Status	[7a, 7b]
3E	Port 4 Operation Status	[7c, 7d]
3F	Port 5 Operation Status	[7e, 7f]
40	Port 6 Operation Status	[80, 81]
41	Port 7 Operation Status	[82, 83]
42	Indirect Resource Access Command	[84, 85]
43	Indirect Resource Access Data I	[86, 87]
44	Indirect Resource Access Data II	[88, 89]
45	Indirect Resource Access Data III	[8a, 8b]
46	Indirect Resource Access Data IV	[8c, 8d]
47	Indirect Resource Access Data V	[8e, 8f]
48	Monitored Source Host I (MAC Address Bit [47:32])	[90, 91]
49	Monitored Source Host II (MAC Address Bit [31:16])	[92, 93]
4A	Monitored Source Host III (MAC Address Bit [15:0])	[94, 95]
4B	Monitored Destination Host I (MAC Address Bit [47:32])	[96, 97]
4C	Monitored Destination Host II (MAC Address Bit [31:16])	[98, 99]
4D	Monitored Destination Host III (MAC Address Bit [15:0])	[9a, 9b]
4E	Port 0 Default Priority/VLAN	[9c, 9d]
4F	Port 1 Default Priority/VLAN	[9e, 9f]
50	Port 2 Default Priority/VLAN	[a0, a1]
51	Port 3 Default Priority/VLAN	[a2, a3]
52	Port 4 Default Priority/VLAN	[a4, a5]
53	Port 5 Default Priority/VLAN	[a6, a7]

Table 20: Register Description (Continued)

54	Port 6 Default Priority/VLAN	[a8, a9]
55	Port 7 Default Priority/VLAN	[aa, ab]
56	Port 8 Default Priority/VLAN	[ac, ad]
57	Port 9 Default Priority/VLAN	[ae, af]
58	Port 10 Default Priority/VLAN	[b0, b1]
59	Port 11 Default Priority/VLAN	[b2, b3]
5A	Port 12 Default Priority/VLAN	[b4, b5]
5B	Port 13 Default Priority/VLAN	[b6, b7]
5C	Port 14 Default Priority/VLAN	[b8, b9]
5D	Port 15 Default Priority/VLAN	[ba, bb]
5E	Port 16 Default Priority/VLAN	[bc, bd]
5F	Port 17 Default Priority/VLAN	[be, bf]
60	Port 18 Default Priority/VLAN	[c0, c1]
61	Port 19 Default Priority/VLAN	[c2, c3]
62	Port 20 Default Priority/VLAN	[c4, c5]
63	Port 21 Default Priority/VLAN	[c6, c7]
64	Port 22 Default Priority/VLAN	[c8, c9]
65	Port 23 Default Priority/VLAN	[ca, cb]
66	Port 24 Default Priority/VLAN	[cc, cd]
67	Port 25 Default Priority/VLAN	[ce, cf]
68	Port 26 Default Priority/VLAN	[d0, d1]
69	Port 27 Default Priority/VLAN	[d2, d3]
6A	Port 28 Default Priority/VLAN	[d4, d5]
6B	Port 29 Default Priority/VLAN	[d6, d7]
6C	Port 30 Default Priority/VLAN	[d8, d9]
6D	Port 31 Default Priority/VLAN	[da, db]
6E	Local CPU Default Priority/VLAN	[dc, dd]
6F	Reserved	[de, df]
70	CheckSum	[e0, e1]

System Configuration Register I (Register 00)

The registers 01 to 03 are global system configuration registers. The option selected in this register affects the overall system operation.

Table 21: System Configuration Register I (Register 00)

BIT	NAME	DESCRIPTION
15	CPUprst	CPU Present. This bit is used to indicate if the AL126 is initialized from the EEPROM. This bit is set by the AL126 when it detects the EEPROM is not present and its configuration is not initialized. The device assumes that a CPU is present and waits for the CPU to initialize this device.
14	FloodCtl	Flooding Control. Controls the forwarding of unicast frames with unknown destinations received from the non-uplink ports. 0: Disable. Frames received with an unknown unicast destination MAC address will be forwarded to all the ports (excluding the receiving port) within the VLANs specified at the receiving port. (IEEE 802.1d compliant) 1: Enable. Frames received with an unknown unicast destination MAC address will be forwarded to the uplink port specified for the receiving port.
13	AutoSec	Auto Security Enforcement. 0: Auto security off. The security violation at a secured port will not change its port state. 1: Auto security on. The security violation at a secured port will cause the port to go into the DISABLE state.
12	AgeEN	Switch Table Entry Aging Control. Only the dynamically learned addresses will be aged. All explicit entries will not age. The aging time is programmed in register 01. 0: Disable. The table aging process is disabled. 1: Enable. The table aging process is enabled and a hardware process ages every dynamically learned table entry. (IEEE 802.1d compliant)
11	TCNVG	MAC Address Table Convergence Control. 0: Disable. The device will not share locally learned MAC addresses with other devices on the RoX-II Bus. 1: Enable. The device will run a background process to periodically transfer locally learned table entries for other devices to learn. (IEEE 802.1d compliant)
10	STPEN	Spanning Tree Protocol Enable Control. 0: Disable. The BPDU frames received from network ports will be treated as regular broadcast frames. 1: Enable. The BPDU frames received from network ports will be forwarded only to the CPU port. (IEEE 802.1d compliant, but use this setting if the system has network management).

Table 21: System Configuration Register I (Register 00) (Continued)

9	PinMon	Port Incoming Frame Flow Monitoring (port snooping) Enable Control. The monitored and snooping port configuration is in register 06. 0: Disable 1: Enable
8	PoutMon	Port Outgoing Frame Flow Monitoring (port snooping) Enable Control. The monitored and snooping port configuration is in register 06. 0: Disable 1: Enable
7	CPUcfgrdy	CPU Configuration Ready. This bit is set by the AL126 to provide an indication that the register file initialization is completed by the CPU. 0: Not initialized. 1: Register file initialization done.
6	NetMgmt	Network Management Enable Control. 0: Disable. The device will not generate MIB events to the management device (such as AL300A or AL3000). 1: Enable. The device will generate MIB events and propagate them to the management device.
5	CPUInitDone	System Initialization Done. Meaningful only when the AL126 is initialized by a CPU. The CPU sets this bit to one after all registers and static entries are programmed.
4	SelRMII	Select RMII for Ports 1 through 7. (See Register 2, Bit 15 for Port 0.) 0: Disable. The device will operate in MII mode. 1: Enable. The device will operate in RMII mode.
3	L2Trunk	Layer 2 Trunking Mode. Trunked (Port Aggregation) port selection for any given frame is based on either the Layer 2 MAC Source and Destination Address or based on the ports to trunk assignment. 0: Disable. Trunking decisions will be based on port-based trunk port assignment registers. 1: Enable. Trunking decisions will be based on source port L2 MAC addresses.
2	TimeoutEn	Frame Aging Time Out Enable. The MaxDelay bits in register 01 set the time-out limit. 0: Device will not time-out frames based on MaxDelay. 1: Device will time-out frames. (IEEE 802.1d compliant)
1~0	Reserved	Set to 0.

Table 22: System Configuration Register II (Register 01)

BIT	NAME	DESCRIPTION
15~9	MaxAge	MaxAge. This is a seven-bit register containing unsigned integer for determining the address-aging timer. The resolution of the normal address aging is 5.36 seconds at 100 MHz and 6.7 seconds with a 80 MHz system clock. If the SlowAge (register 02) bit is programmed to "1," the resolution is 10.72 seconds at 100 MHz and 13.4 seconds with a 80 MHz system clock.
8	PhyResetDis	PHY Reset Disable. 0: Reset PHY on link down. 1: Don't Reset PHY on link down.
7~6	MaxDelay	MaxDelay. This sets the timer for the maximum allowable frame aging through the switch if TimeoutDis (register 00) option is elected. This value can be slowed down by a factor of eight by setting Register 2, SlowAge bit. 00: 1 second. 01: 2 seconds. 10: 3 seconds. 11: 4 seconds.
5~4	MaxStorm	MaxStorm. This sets the threshold number of consecutive broadcast frames allowed from the port. The storm control option can be selected in the Port Configuration Registers (registers 0D to 1C). 00: 16 frames. 01: 32 frames. 10: 48 frames. 11: 64 frames.
3	SuperMAC	SuperMAC. When this option is selected, the AL126 MAC controller will use a more aggressive back off algorithm. This enables the switch to transmit frame earlier. (Meaningful only in half-duplex mode). 0: Disable. Device will perform the IEEE 802.3 standard exponential back off algorithm when a collision occurs. 1: Enable. When collision occurs, device will back off up to 3 slots.
2	Reserved	Set to 1.
1~0	L2KeySel	L2TKeySel. Selects the MAC address bits for MAC address based trunk port assignment. For most applications, this field does not need to be adjusted. 00: Use hashkey pattern 1. 01: Use hashkey pattern 2. 10: Use hashkey pattern 3. 11: Use hashkey pattern 4.

Table 23: System Configuration Register III (Register 02)

BIT	NAME	DESCRIPTION
15	SelRMIIP0	Selects RMII for Port 0. (See Register 0, Bit 4 for Ports 1 ~ 7) 0: Disable. Port 0 operates in MII mode. 1: Enable. Port 0 operates in RMII mode.
14	CPUOffL	Disables Unknown Frame Forwarding to the AL300A, thereby to the CPU.
13	ClkSel	Clock Select. 0: System clock is 100 MHz. 1: System clock is 80 MHz.
12	L2T0En	Layer 2 Trunk Group 0 Enable. 0: Disable 1: Enable
11	L2T1En	Layer 2 Trunk Group 1 Enable. 0: Disable 1: Enable
10	SlowAge	Slow Age Timing. Slows down the normal address aging timer specified in register 01, MaxAge field. 0: Normal aging. The resolution of the normal address aging is 5.36 seconds at 100 MHz and 6.7 seconds with a 80 MHz system clock. 1: Slow down. The resolution is 10.72 seconds at 100 MHz and 13.4 seconds with a 80 MHz system clock.
9	BpIPG64	Backpressure Inter-packet Gap. Used for half-duplex backpressure operation when carrier-based backpressure is selected. 0: BpIPG = 96BT. 1: BpIPG = 64BT.
8	SIPG	Standard Inter-packet Gap. Used for normal frame transmission. 0: IPG is 96BT. (IEEE 802.3 compliant) 1: IPG is 64BT.
7~6	BPRate	Backpressure Rate. Used when collision based backpressure operation is selected. 00: Collide with every frame. 01: Collide 7 out of every 8 frames. 10: Collide 3 out of every 4 frames. 11: Collide 1 out of every 2 frames.
5	SG16M	Frame Buffer SGRAM Size. 0: 8 Mbit SGRAM. 1: 16 Mbit SGRAM.
4	BPCOL	Backpressure Collision. Selects backpressure mechanism for half-duplex (CSMA/CD) operation. 0: CRS based. 1: Collision based.

Table 23: System Configuration Register III (Register 02) (Continued)

3	ETEnb	External MAC Table Enable. (Must have external SSRAM present). This table is also used for IEEE 802.1q tagged VLAN database. 0: Disable 1: Enable
2	BebSel	Binary Exponential Backoff Select for Half-duplex (CSMA/CD) Operation. 0: Standard (IEEE 802.3 compliant). 1: Avoid channel capture via binary back-off algorithm.
1	PQWRREn	Priority Queue Arbitration Method. Selects either weighted round-robin or strict priority. 0: Strict priority. 1: Weighted round-robin. Relative priority is set by register 0A.
0	FlowCtrlBC	Broadcast Storm Control Selection. 0: Flow control Multicast and Broadcast. 1: Flow control only Broadcast.

Table 24: System Configuration Register IV (Register 03)

BIT	NAME	DESCRIPTION
15	QEnable	Enables 802.1q VLAN Tagging. This requires an external MAC address table SSRAM and the corresponding control bit, register 2, External MAC Table, should be set. 0: Disable 1: Enable
14	AL300AEn	Supports AL300A Protocol. Must be set if the AL300A is present on the RoX-II Ring. 0: Disable 1: Enable
13	GWPrst	Gateway Device Present. Enables the support for the Ring Gateway device. 0: Disable 1: Enable
12	ALTGW	Enables Alternative Ring Gateway Device Support. 0: Disable 1: Enable
11	IPMCtrap	IPMC Frame Trap Enable. Enables the IP Multicast Frame Trap to the CPU via AL300A (management) or AL3000 (Router). 0: Disable 1: Enable
10	IGMPtrap	IGMP Frame Trap Enable. 0: Disable 1: Enable
9	GARPtrap	GARP-Type (e.g. GVRP, GMRP) Frame Trap Enable. 0: Disable 1: Enable
8	ARPtrap	ARP Frame Trap Enable. 0: Disable 1: Enable

Table 24: System Configuration Register IV (Register 03) (Continued)

7	802Xtrap	Trunking Control Frame Trap Enable. Enables IEEE 802.3ad Port Aggregation MAC Control Frame Trap. 0: Disable 1: Enable
6	L2FailEn	Layer 2 Trunk Link Fail Recovery Enable. Enables automatic link-fail over protection on trunks (Aggregated ports). This is only effective when Register 0, L2Trunk Bit is set. 0: Disable 1: Enable
5~4	L2Timer	Layer 2 Trunk Link Recover Timer Control. Selects the queue flushing timer to be used when a failed link on a trunk is healed and traffic is restored on the healed link. This field value is meaningful only when Register 0, L2Trunk Bit and Register 3, L2FailEn is set. 00: Disable 01: 1 ~ 2 sec 10: 1/4 ~ 1/2 sec 11: 1/8 ~ 1/16 sec
3	D3GigaOn	Device 3 is a Gigabit Device. To be set if a Gigabit device (such as AL1022) occupies the RoX-II Ring Device ID = 3. 0: Disable 1: Enable
2	D2GigaOn	Device 2 is a Gigabit Device. To be set if a Gigabit device (such as AL1022) occupies the RoX-II Ring Device ID = 2. 0: Disable 1: Enable
1	D1GigaOn	Device 1 is a Gigabit Device. To be set if a Gigabit device (such as AL1022) occupies the RoX-II Ring Device ID = 1. 0: Disable 1: Enable
0	D0GigaOn	Device 0 is a Gigabit Device. To be set if a Gigabit device (such as AL1022) occupies the RoX-II Ring Device ID = 0. 0: Disable 1: Enable

System Performance Tuning Control Register (Register 04)

The fields in this register set the performance characteristics of the RoX-II Ring. Set the register to the recommended value based on RoX-II Ring operating frequency.

Recommended Settings: 0001 1001 0101 1100 for 100 MHz with dual control ring enabled; or

0001 0001 0001 0100 for 80 MHz.

Table 25: System Performance Tuning Control Register (Register 04)

BIT	NAME	DESCRIPTION
15~14	SysPerf1	Refer to the Recommendation Above.
13	CasDelay	Sets the Frame Buffer Memory SGRAM/SDRAM CAS Latency. 0: CAS Latency 2. (Default) 1: CAS Latency 3.
12~0	SysPerf0	Refer to the Recommendation Above.

Vendor PHY Operating Mode (Register 05; PHY Configuration)

This register is used to program the vendor specific PHY option. It is also used for programming the Vendor Specific PHY register location and bit location of the operation status. Please refer to the respective 10/100 Fast Ethernet PHY data sheet (in MDIO programming section) connected to the AL126 for appropriate register settings.

Table 26: Vendor PHY Operating Mode (Register 05)

BIT	NAME	DESCRIPTION
15	MSBSel	Most Significant Bit Selection. 0: PHY address is 00xxx. 1: PHY address is 10xxx.
14	MIISlowClk	MDIO Clock Speed Selection. 0: Normal (RoX-II Ring Clock divided by 128, 781 KHz @100 MHz) 1: Select slow clock for MII. (RoX-II Ring Clock divided by 4096, 24 KHz @100 MHz)
13	RevOrder	Reverse Order. In multi-PHY IC package, some vendors PHY numbers ports clockwise and others counterclockwise. These can be re-mapped to be consistent with switch system's port numbering scheme by setting this register. 0: PHY address order is from 000 to 111; (normal). 1: PHY address order is from 111 to 000.
12~8	PHYOpReg	PHY Operating Mode Register. Address of the vendor specific PHY operating mode register that typically holds the results of parallel link capability detection.

Table 26: Vendor PHY Operating Mode (Register 05) (Continued)

7~4	PHYOpSp	PHY Operating Speed Location. Bit location within the register specified in PHYOpReg where attached PHY's operating speed is stored.
3~0	PHYOpMd	PHY Operating Mode Location. Bit location within the register specified in PHYOpReg where attached PHY's operating mode (full/ half-duplex) is stored.

Port Monitoring Configuration Register (Register 06)

This register configures port monitoring ("snooping" or "sniffer" port). It sets the monitored port and the TX and RX snooping ports.

Table 27: Port Monitoring Configuration Register (Register 06)

BIT	NAME	DESCRIPTION
15	Reserved	
14~10	MdPID	Device and Port ID of the Port Being Monitored. DeviceID[1:0]+PortID[2:0].
9~5	MgIPID	Device and Port ID of the Destination Port to Receive Monitored Port's Ingress Frames. This port can be the same port as MgOPID. DeviceID[1:0]+PortID[2:0].
4~0	MgOPID	Device and Port ID of the Destination Port to Receive Monitored Port's Egress Frames. This port can be the same port as MgIPID. DeviceID[1:0]+PortID[2:0].

Priority Queue Assignment Register (Register 07)

Recommended Setting: 1111 1010 0100 0001

The AL126 allows the tagged priority to be assigned to any of the four priority queues. The AL126 will transmit the frames based on the priority of the queue, not the priority tag.

Table 28: Priority Queue Assignment Register (Register 07)

BIT	NAME	DESCRIPTION
15~14	PL7QA	Select User Priority Value =7 in VLAN Tag Mapping to AL126's Priority Queue. 11 = Queue 3 10 = Queue 2 01 = Queue 1 00 = Queue 0
13~12	PL6QA	User Priority Value = 6 Queue Assignment.
11~10	PL5QA	User Priority Value = 5 Queue Assignment.
9~8	PL4QA	User Priority Value = 4 Queue Assignment.
7~6	PL3QA	User Priority Value = 3 Queue Assignment.
5~4	PL2QA	User Priority Value = 2 Queue Assignment.

Table 28: Priority Queue Assignment Register (Register 07) (Continued)

3~2	PL1QA	User Priority Value = 1 Queue Assignment.
1~0	PL0QA	User Priority Value = 0 Queue Assignment.

Output Queue Management Register I (Register 08)

Recommended Setting: 0011 1111 1111 1111

Table 29: Output Queue Management Register I (Register 08)

BIT	NAME	DESCRIPTION
15	MaxDrop	Output Over Drop Option. Selects the queue behavior when queue maximum depth limit is reached. 0: Flow control first. 1: Drop enable.
14	Reserved	
13	CPUMaxLimEn	AL300A Max Limit Enable. 0: Disable 1: Enable
12	M0MaxLimEn	10 Mbit/s Multicast Queue Max Limit Control Enable. 0: Disable 1: Enable
11	Q3MaxLimEn	Priority Queue 3 Max Limit Control Enable. For maximum limit control to be enabled, both the queue and the port maximum limit control must be enabled for the control to be enabled. 0: Disable 1: Enable
10	Q2MaxLimEn	Priority Queue 2 Max Limit Control Enable.
9	Q1MaxLimEn	Priority Queue 1 Max Limit Control Enable.
8	Q0MaxLimEn	Priority Queue 0 Max Limit Control Enable.
7	P7MaxLimEn	Output Port 7 Max Limit Control Enable. For the max limit control to be enabled, both the queue and the port max limit control must be enabled for the control to be enabled. 0: Disable 1: Enable
6	P6MaxLimEn	Output Port 6 Max Limit Control Enable.
5	P5MaxLimEn	Output Port 5 Max Limit Control Enable.
4	P4MaxLimEn	Output Port 4 Max Limit Control Enable.
3	P3MaxLimEn	Output Port 3 Max Limit Control Enable.
2	P2MaxLimEn	Output Port 2 Max Limit Control Enable.
1	P1MaxLimEn	Output Port 1 Max Limit Control Enable.
0	P0MaxLimEn	Output Port 0 Max Limit Control Enable.

Output Queue Management Register II (Register 09)

Recommended Setting: 0001 0001 0001 0001

Table 30: Output Queue Management Register II (Register 09)

BIT	NAME	DESCRIPTION
15~12	Q3MaxLim	Maximum # of buffer blocks priority queue 3 can hold if both priority queue and output port max limit controls are enabled. The AL126 uses this value to set its own buffer-full status in “Queue Status” registers for each of the output priority queues. When this threshold is reached, “Operation Status Communication Message” with <buffer full> is sent onto the RoX-II data ring. Any frame queue request must be honored regardless of this bit. The low water mark for sending <buffer available> is set for 16 less than the max limit, except for the limit of 4 (it’s low watermark is 2), which is used as a test mode. 0000: 32 0001: 64 0010: 96 0011: 128 0100: 160 0101: 192 0110: 224 0111: 256 1000: 320 1001: 384 1010: 448 1011: 512 1100: 640 1101: 768 1110: 896 1111: 4
11~8	Q2MaxLim	Maximum # of buffer blocks priority queue 2 can hold if both priority queue and output port max limit control for this queue is enabled.
7~4	Q1MaxLim	Maximum # of buffer blocks priority queue 1 can hold if both priority queue and output port max limit control for this queue is enabled.
3~0	Q0MaxLim	Maximum # of buffer blocks priority queue 0 can hold if both priority queue and output port max limit control for this queue is enabled.

Priority Queue Weight Round-Robin Control Register (Register 0A)

Recommended Setting: 1111 0111 0011 0001

This register controls the weight of each priority queue, when weight priority queuing is selected.

Note: Q3 weight should be bigger or equal to Q2, Q2 weight should be bigger or equal to Q1, Q1 weight should be bigger or equal to Q0.

Table 31: Priority Queue Weight Round-Robin Control Register (Register 0A)

BIT	NAME	DESCRIPTION
15~12	Q3RRWeight	Weight of Queue 3 in the Round-robin Scheme. 0000 = 1, 0001 = 1, ... , 1110 = 14, 1111 = 15. (Note that a “0” is not applicable for 0000.)
11~8	Q2RRWeight	Weight of Queue 2 in the Round-robin Scheme.
7~4	Q1RRWeight	Weight of Queue 1 in the Round-robin Scheme.
3~0	Q0RRWeight	Weight of Queue 0 in the Round-robin Scheme.

RoX-II Control Register I (Register 0B)

Recommended Setting: 0000 0000 0000 0000

This register, along with register 0C, sets the “route” bitmap from device x to this device. Each Dx Route has 5-bits representing the device to device physical connections. Set each respective bit that represents the path back to this device on the RoX-II ring. The least significant bit position is used for Device ID=0 while the most significant bit position is used for Device ID=4. RoX-II devices don’t have to be connected in Device ID sequence. A “1” in this bit-map means that data path from this Device ID to the bit-map device is active. If this Device ID =1, then D1Route is set to zero, since it does not use the RoX-II Ring to transfer data to itself. If the AL300A is present on the RoX-II ring, do not include the AL300A device for Route Field programming.

Example: Consider a RoX-II Ring where devices are connected in sequence of the Device ID, that is Device 0 ->Device 1 -> Device 2-> Device 3-> Device 4 (AL3000)->Device 0.

- For the device with Device ID=0, D0Route is set to ^b 00000, because it is its own device.
- D1Route is set to ^b 11110, because from Device ID=1 to Device ID=0, Device 1 through Device 4 are present.
- D2Route is set to ^b 11100, because from Device ID=2 to Device ID=0, Device 2 through Device 4 are present.
- D3Route is set to ^b 11000, because from Device ID=3 to Device ID=0, Device 3 through Device 4 are present.
- D4Route is set to ^b 10000, because from Device ID=4 to Device ID=0, Device 4 is the only one present to drive this device (Device 0).

Table 32: RoX-II Control Register I (Register 0B)

BIT	NAME	DESCRIPTION
15	DualREn	Dual Control Ring Enable. The RoX-II Ring has a separate data and control ring. The control ring can be either in 8-bit wide mode or 14-bit mode. Setting this bit enables the 14-bit mode, required for maximum RoX-II Ring performance. 0: Disable. Control ring is in 8-bit mode. 1: Enable. Control ring is in 14-bit mode.
14~10	D2Route	Route Selection from Device 2 to this Device. Refer to the example above in Register 0B description.
9~5	D1Route	Route Selection from Device 1 to this Device. Refer to the example above in Register 0B description.
4~0	D0Route	Route Selection from Device 0 to this Device. Refer to the example above in Register 0B description.

RoX-II Control Register II (Register 0C)

Recommended Setting: 0000 0000 0000 0000

Table 33: RoX-II Control Register II (Register 0C)

BIT	NAME	DESCRIPTION
15	OneDev	RoX-II Internal Loop Back Enable. If this device is the only device on the RoX-II Ring, the RoX signals can be internally closed when this bit is set. 0: Disable 1: Enable
14	HiMmode	Memory Mode Selection. Selects the Device ID=4, such as the AL3000. Select 0 for devices with one packet memory (such as the AL126 or AL3000), or select 1 for devices with dual packet memory (such as the AL1022). 0: Single buffer. 1: Dual buffers.
13	D3Mmode	Memory Mode Selection for the Device ID=3. Select 0 for devices with one packet memory (such as AL126 or AL3000), and select 1 for devices with dual packet memory (such as AL1022). 0: Single buffer (e.g. AL126) 1: Dual buffers (AL1022)
12	D2Mmode	Memory Mode Selection for Device 2.
11	D1Mmode	Memory Mode Selection for Device 1.
10	D0Mmode	Memory Mode Selection for Device 0.

Table 33: RoX-II Control Register II (Register 0C) (Continued)

BIT	NAME	DESCRIPTION
9~5	HiRoute	Route Selection from the AL3000 (always Device 4) to this Device. Refer to the example above in register 0B description.
4~0	D3Route	Route Selection from Device 3 to this Device. Refer to the example above in Register 0B description.

Port Configuration Registers I

Registers 0D to 1C are for local port configuration. There are two port configurations per port. Port 0 port configuration uses register 0D and 0E, Port 1 register 0F and 10, etc.

Uplink ID - this is a six-bit link ID which assigns an uplink to a port or a trunk.

- If the uplink is at local stack, the format is:

  Port: [0] [Dev_ID] [Port_ID]
  Trunk: [100] [Trunk_ID]
  CPU: [100000]
  Router: [100001]

- If the uplink is at remote stack, the ID is:

  Stack: [101] [Stack_ID] The remote stack will assign the final port/trunk ID.

Note: If the port/trunk is an uplink, the uplink ID should be its own port/trunk ID. Any frame with an unlearned SA will then be filtered.

Table 34: Port Configuration Registers I

BIT	NAME	DESCRIPTION
15~10	UpLinkID	Uplink ID Associated with the Port. Uplink is used when unknown MAC DA is received and the register 0, FloodCtl bit is set to enable this uplink feature. 0xxyyy: Local port ID with xx as the DEVID and yyy as the PID. 110xxx: Local trunk ID with xxx as the Trunk_ID. 100000: Local CPU. 100001: Local router. 101xxx: Remote stack uplink with xxx as the Stack_ID. Others: Reserved
9	Tmember	Trunk Member Port. 0: Individual port. 1: This port is a member of a trunk port.
8	Reserved	

Table 34: Port Configuration Registers I (Continued)

7	StormCTL	Broadcast Storm Control Enable. Global setting in register 2, FlowCtrlBC controls whether this storm control acts on multicast and broadcast, or just broadcast frames. At register 1, MaxStorm sets the maximum allowed multicast/broadcast frames at any given time. 0: Storm control disable. The broadcast frame will not be throttled. 1: Storm control enable. If the accumulated number of broadcast frames in the input buffer of the port is over the threshold specified in the system configuration register, new incoming broadcast frames will be discarded until the number has been reduced below the threshold.
6	Security	Intrusion Protection. Security control for the frames received from non-uplink ports. When Security is on, and AutoSec Bit (register 0) is set, this port will be disabled upon detection of unknown source MAC address. 0: Security off. The forwarding decision made about frames received from the port will not involve the source MAC address checking. 1: Security on. Frames received from the port with an unknown source MAC address or with source MAC address learned previously from another port will be discarded.
5	LCPUOn	Local CPU Port VLAN Membership. 0: Non-member. Multicast/Broadcast frames received from the port will not be forwarded to the local CPU port (AL300A or AL3000). 1: Member. Multicast/Broadcast frames received from the port will be forwarded to the local CPU port in addition to other member ports specified in the VLAN Map and VLAN Map Extension register of the port (excluding the source port).
4	LrnDis	Learning Disable. This is used to designate the port as an uplink port, since any unmatched frames will be forwarded to ports with no learned address. 0: Source address from this port will be learned. 1: Source address from this port will not be learned.
3~2	PortST	Spanning Tree Port State Control. 00: Disable. All incoming frames from the PHY will be discarded; all outgoing frames will be masked from the path to the PHY. 01: Blocking-N-Listening. All incoming frames except incoming BPDUs from the PHY will be discarded; all outgoing frames except outgoing BPDUs will be masked from the path to the PHY. 10: Learning. The source information of all incoming frames from the PHY will be learned, all incoming frames except incoming BPDUs from the PHY will be discarded after being learned; all outgoing frames except outgoing BPDUs will be masked from the path to the PHY. 11: Forwarding. The source information of all incoming frames from the PHY will be learned, all incoming frames will be forwarded based on the switch routing decision; all outing frames will be transmitted to the PHY.
1~0	Reserved	

Table 35: Port Configuration Registers II

BIT	NAME	DESCRIPTION
15	Reserved	
14	PHYR6Skip	Skip Check of PHY Register 6 in MDIO. 0: IEEE compliant operation. 1: Skips PHY register 6 in link auto-negotiation completion. After AN completes, MDIO logic skips checking the Expansion Register Link partner AN enable (register 6) and read the Link Partner Ability (register 5) immediately to determine the operation mode of the PHY.
13	PHYCTLAD	When this bit is set, the MDIO register is initialized to preserve control and ability advertisement before initiating auto-negotiation. 0: Control and ability is initialized to 0. 1: Previous value is preserved.
12	PHYACSkip	Ignore auto-complete for link up in MDIO flow. This mode is useful for interfacing some PHYs to 100BASE-FX (fiber). 0: IEEE compliant operation. 1: Skips PHY auto-complete.
11	FlowCtrlFdEn	Flow Control Full-Duplex (IEEE 802.3x) Enable.
10	FlowCtrlHdEn	Flow Control Half-Duplex Enable.
9~6	MDIOCfg[3:0]	MDIO Configuration. 0001: Selects master mode. When the AL126 is in this mode, it will set the PHY capability advertisement register. The link will auto-negotiate to the highest capability. 0010: Selects slave mode. When the AL126 is in this mode, the PHY will set the PHY capability advertisement register. The link will auto-negotiate to the highest capability. 0111: Selects forced mode. When the AL126 is in this mode, it will turn off auto-negotiation and the PHY will select the link's operating mode.
5	MDIODis	MDIO Disable. 0: MDIO enabled. 1: MDIO disabled.
4	LinkUp	Force Link Status. Effective only when MDIOCfg is set to master or forced mode, or when MDIODis is set to disable. 0: Link down. 1: Link up.

Table 35: Port Configuration Registers II

3~0	PrtCfgMode[3:0]	Force Port Operation Mode. Effective only when MDIOCfg is set to master or forced mode, or when MDIODis is set to disable. PrtCfgMode[3] = 100 full-duplex. PrtCfgMode[2] = 100 half-duplex. PrtCfgMode[1] = 10 full-duplex. PrtCfgMode[0] = 10 half-duplex.

Table 36: Port VLAN Map I Registers

BIT	NAME	DESCRIPTION
15~8	Dev3Map	Port VLAN Map corresponding to the port 7 ~ port 0 of the device with DEVID = 3. 0: Non-member port. 1: Member port.
7~0	Dev2Map	Port VLAN Map corresponding to the port 7 ~ port 0 of the device with DEVID = 2. Explanation is same as above.

Table 37: Port VLAN Map II Registers

BIT	NAME	DESCRIPTION
15~8	Dev1Map	Port VLAN Map corresponding to the port 7 ~ port 0 of the device with DEVID = 1. 0: Non-member port. 1: Member port.
7~0	Dev0Map	Port VLAN Map corresponding to the port 7 ~ port 0 of the device with DEVID = 0. 0: Non-member port. 1: Member port.

VLAN Map Extension Register I (Register 2D)

Recommended Setting: 0000 0000 0000 0000

Table 38: VLAN Map Extension Register I (Register 2D)

BIT	NAME	DESCRIPTION
15	P7GW7On	The RoX-II Ring Gateway Device 7 VLAN Membership for Port 7. 0: Non-member. Broadcast frames received from the port will not be forwarded to the Gateway Device 7. 1: Member. Broadcast frames received from the port will be forwarded to the Gateway Device 7 in addition to other member ports specified in the VLAN Map and LCPUOn in port configuration register, (excluding the source port).
14	P6GW7On	The Gateway Device 7 VLAN Membership for Port 6.
13	P5GW7On	The Gateway Device 7 VLAN Membership for Port 5.
12	P4GW7On	The Gateway Device 7 VLAN Membership for Port 4.
11	P3GW7On	The Gateway Device 7 VLAN Membership for Port 3.
10	P2GW7On	The Gateway Device 7 VLAN Membership for Port 2.
9	P1GW7On	The Gateway Device 7 VLAN Membership for Port 1.
8	P0GW7On	The Gateway Device 7 VLAN Membership for Port 0.
7~0	Reserved	Set to 0.

Table 39: VLAN Map Extension Register II (Register 2E)

BIT	NAME	DESCRIPTION
15~8	Reserved	
7	P7GW6On	The Gateway Device 6 VLAN Membership for Port 7.
6	P6GW6On	The Gateway Device 6 VLAN Membership for Port 6.
5	P5GW6On	The Gateway Device 6 VLAN Membership for Port 5.
4	P4GW6On	The Gateway Device 6 VLAN Membership for Port 4.
3	P3GW6On	The Gateway Device 6 VLAN Membership for Port 3.
2	P2GW6On	The Gateway Device 6 VLAN Membership for Port 2.
1	P1GW6On	The Gateway Device 6 VLAN Membership for Port 1.
0	P0GW6On	The Gateway Device 6 VLAN Membership for Port 0.

Register Group for Port Based Trunking Registers (Registers 2F ~ 36)

The Port to Trunk Port assignment register assigns a port to a trunk for port-based load balancing trunking. Please see example in the trunking section.

A port to trunk port work sheet is provided in Appendix II.

PORT NUMBER	REGISTER
0	2F
1	30
2	31
3	32
4	33
5	34
6	35
7	36

Table 40: Trunk Port Assignment Register (2F~36) x 8

BIT	NAME	DESCRIPTION
15~14	Port7TP	Trunk Link for Trunk Port 7. 00: PortID is represented by [DEVID, TID, 00]. 01: PortID is represented by [DEVID, TID, 01]. 10: PortID is represented by [DEVID, TID, 10]. 11: PortID is represented by [DEVID, TID, 11].
13~12	Port6TP	Trunk Link for Trunk Port 6. Explanation is same as above.
11~10	Port5TP	Trunk Link for Trunk Port 5. Explanation is same as above.
9~8	Port4TP	Trunk Link for Trunk Port 4. Explanation is same as above.
7~6	Port3TP	Trunk Link for Trunk Port 3. Explanation is same as above.
5~4	Port2TP	Trunk Link for Trunk Port 2. Explanation is same as above.
3~2	Port1TP	Trunk Link for Trunk Port 1. Explanation is same as above.
1~0	Port0TP	Trunk Link for Trunk Port 0. Explanation is same as above.

Register Grouping for Layer 2 Trunking (2F~33)

Using registers 2F~33 are defined by the selected trunking method in register 0, L2Trunk. If L2Trunk is set to zero (port-based trunking), then the table above is effective. If L2 Trunk is set to one (L2 or MAC Address based trunking), then the alternate table below is effective.

Layer 2 Trunking Assignment Register I (Register 2F)

Recommended Setting: 1111 0000 0000 1111

Table 41: Layer 2 Trunking Assignment Register I (Register 2F)

BIT	NAME	DESCRIPTION
15~8	T1Member	Assign Trunk Member for Trunk 1.
7~0	T0Member	Assign Trunk Member for Trunk 0.

Layer 2 Trunking Assignment Register II (Register 30)

Recommended Setting: 1111 0000 0000 1111

Table 42: Layer 2 Trunking Assignment Register II (Register 30)

BIT	NAME	DESCRIPTION
15~8	T3Member	Assign Trunk Member for Trunk 3.
7~0	T2Member	Assign Trunk Member for Trunk 2.

Layer 2 Trunking Assignment Register III (Register 31)

Recommended Setting: 1111 0000 0000 1111

Table 43: Layer 2 Trunking Assignment Register III (Register 31)

BIT	NAME	DESCRIPTION
15~8	T5Member	Assign Trunk Member for Trunk 5.
7~0	T4Member	Assign Trunk Member for Trunk 4.

Layer 2 Trunking Assignment Register IV (Register 32)

Recommended Setting: 1111 0000 0000 1111

Table 44: Layer 2 Trunking Assignment Register IV (Register 32)

BIT	NAME	DESCRIPTION
15~8	T7Member	Assign Trunk Member for Trunk 7.
7~0	T6Member	Assign Trunk Member for Trunk 6.

Layer 2 Trunking Protocol Register (Register 33)

Recommended Setting: 0000 0000 0000 0000

Table 45: Layer 2 Trunking Protocol Register (Register 33)

BIT	NAME	DESCRIPTION
15~14	T7Ptcl	Layer 2 Trunk 7 Protocol Control. 00=DA+SA crc. 01=SA crc. 10=DA crc. 11=DA+SA bits.
13~12	T6Ptcl	Layer 2 Trunk 6 Protocol Control.
11~10	T5Ptcl	Layer 2 Trunk 5 Protocol Control.
9~8	T4Ptcl	Layer 2 Trunk 4 Protocol Control.
7~6	T3Ptcl	Layer 2 Trunk 3 Protocol Control.
5~4	T2Ptcl	Layer 2 Trunk 2 Protocol Control.
3~2	T1Ptcl	Layer 2 Trunk 1 Protocol Control.
1~0	T0Ptcl	Layer 2 Trunk 0 Protocol Control.

Test Control Register I (Register 37) Reserved for Allayer's Use.

Recommended Setting: 0000 0000 0000 0000

Table 46: Testing Register I (Register 37)

BIT	NAME	DESCRIPTION
15~6	Reserved	
5	TypeOnly	802.3x Flow Control Frame Recognition Control. 0: Check for MAC control frame DA MAC address in addition to the MAC control type field. 1: Check only for the MAC control type field.
4~0	Reserved	

Test Control Register II (Register 38) Reserved for Allayer's Use.

This register is reserved for Allayer's use. The recommended setting is 0000 1000 0000 1100.

Table 47: Testing Register II (Register 38)

BIT	NAME	DESCRIPTION
15~12	Reserved	Reserved
11~10	WmarkSel	Backpressure Watermark Select. 00: Backpressure if available block count < 4. 01: Backpressure if available block count < 8. 10: Backpressure if available block count < 16. 11: Test mode. Each block is 2Kbyte.
9~0	Reserved	Reserved

Note: Most of the bits in this register are reserved of the factory testing except for the WmarkSel bits. These bits set the level of buffer to trigger backpressure to eliminate buffer overflow.

Table 48: System Status Register (Register 39)

BIT	NAME	DESCRIPTION
15	EPTimeOut	EEPROM Time Out. 0: EEPROM initializes the device. 1: Device is ready to be programmed by the CPU.
14	CheckSumErr	0: Checksum correct. 1: EEPROM checksum error.
13	Sgraminitdone	SGRAM Initialization Done.
12	Sraminitdone	SRAM Initialization Done.
11	Reginitdone	Register Initialization Done.
10~7	TrafCnt	Network Utilization Indicator Counter.
6~4	Reserved	
3~0	Device ID	The AL126's ID is 0011.

Table 49: Port Operation Status Registers (3A~41)

BIT	NAME	DESCRIPTION
15	LinkFail	Port Link Status. 0: Normal 1: Fail
14	PHYError	Port PHY Status. 0: Normal 1: Error
13	Sviolation	Port Security Status. 0: Normal 1: Violation
12	FlowCtrl	If port mode ([1:0]) is 2'b01 or 2'b11: 0: Pause disable. 1: Pause enable. If port mode ([1:0]) is 2'b00 or 2'b10: 0: Backpressure based on CRS. 1: Backpressure based on collision.
11	Stormed	Port Broadcast Storm Status. 0: Normal 1: Stormed
10	InBFull	Port Input Buffer Full Status. 0: Normal 1: Input buffer full experienced.
9	TblUNAVL	Table Entry Unavailability for MAC Learning. 0: Normal 1: Unavailability experienced.
8	Jabbered	Port Jabber Status. 0: Normal 1: Jabber experienced.
7	LateCOL	Port Late Collision Status. 0: Normal 1: Late collision experienced.
6	TxPaused	Port Transmit Pause Status. 0: No transmit pause experienced. 1: Transmit pause experienced.
5	CRSLoss	Port Carrier Sense Loss During Transmission Status. 0: No carrier sense loss experienced. 1: Carrier sense loss experienced.

Table 49: Port Operation Status Registers (3A~41) (Continued)

4	FalseCRS	False Carrier Status. 0: Normal 1: False carrier experienced.
3	Underflow	Transmit Queue Underflow Status. 0: Normal 1: Underflow experienced.
2	TimeOut	Frame Time Out. 0: Normal 1: Underflow experienced.
1~0	PortMode	Port Operating Mode. 00: 10 Mbit/s half-duplex. 01: 10 Mbit/s full-duplex. 10: 100 Mbit/s half-duplex. 11: 100 Mbit/s full-duplex.

Indirect Resource Access Command Register (Register 42)

This register is used for managing the resource of the switch.

Table 50: Indirect Resource Access Command Register (Register 42)

BIT	NAME	DESCRIPTION
15	CmdDone	Command Done. 0: New command. 1: Command finished.
14	Operation	Read/Write Operation Command. 0: Read operation. 1: Write operation.
13~11	ResType	Type of Accessed Resource. 000: PHY registers. 001: EEPROM 010: SGRAM 011: Address tables (I) Read: Sequential read. Write: MAC address learn. 100: Address tables (II) Read: MAC address search. Write: MAC address delete. 101: IPMC table. 110: VLAN table. 111: Reserved
10	ExtRD	If ResType = 011 and Operation = 0 0: On-chip address table sequential read. 1: Off-chip address table sequential read.

Table 50: Indirect Resource Access Command Register (Register 42) (Continued)

10~0	ResAddr	The Address of the Entry Within the Accessed Resource. For off-chip Address Table Sequential Read, iradata4 stores the address of the entry and will be overwritten by output data. For VLAN table access, iradata5[12:1] stores the address and iradata5[0] holds the MSB of data. For IPMC table access, iradata5[0] holds the MSB of data.

Table 51: Indirect Resource Access Data Register I (Register 43)

BIT	NAME	DESCRIPTION
15~0	IRAData	Indirect Resource Access Data I.

Table 52: Indirect Resource Access Data Register II (Register 44)

BIT	NAME	DESCRIPTION
15~0	IRAData	Indirect Resource Access Data II.

Table 53: Indirect Resource Access Data Register III (Register 45)

BIT	NAME	DESCRIPTION
15~0	IRAData	Indirect Resource Access Data III.

Table 54: Indirect Resource Access Data Register IV (Register 46)

BIT	NAME	DESCRIPTION
15~0	IRAData	Indirect Resource Access Address/Data IV.

Table 55: Indirect Resource Access Data Register V (Register 47)

BIT	NAME	DESCRIPTION
15~0	IRAData	Indirect Resource Access Address/Data V.

RMON Source and Destination Registers (Registers 48)

These registers are used by the RMON Host Group for frame counting. The AL126 supports hardware counter for one host. The RMON manager counts the frames to (destination) and from (source) these MAC addresses stored in the register.

The 48-bit MAC address is programmed in three separate registers. Source MAC Address is stored in Registers 07 to 09 and Destination MAC Address in Register 0A to 0C.

Table 56: Monitored Source Host Register I (Register 48)

BIT	NAME	DESCRIPTION
15~0	SRCMAC[47:32]	Monitored Source Host MAC Address [47:32].

Table 57: Monitored Source Host Register II (Register 49)

BIT	NAME	DESCRIPTION
15~0	SRCMAC[31:16]	Monitored Source Host MAC Address [31:16].

Table 58: Monitored Source Host Register III (Register 4A)

BIT	NAME	DESCRIPTION
15~0	SRCMAC[15:0]	Monitored Source Host MAC Address [15:0].

Table 59: Monitored Destination Host Register I (Register 4B)

BIT	NAME	DESCRIPTION
15~0	DSTMAC[47:32]	Monitored Destination Host MAC Address [47:32].

Table 60: Monitored Destination Host Register II (Register 4C)

BIT	NAME	DESCRIPTION
15~0	DSTMAC[31:16]	Monitored Destination Host MAC Address [31:16].

Table 61: Monitored Destination Host Register III (Register 4D)

BIT	NAME	DESCRIPTION
15~0	DSTMAC[15:0]	Monitored Destination Host MAC Address [15:0].

Table 62: Default Priority/VLAN Register (Register 4E~6E) x 33

BIT	NAME	DESCRIPTION
15	Reserved	
14~12	Priority	Default Port Priority.
11~0	VLAN	Default Port VLAN ID.

Table 63: Reserved (Register 6F)

BIT	NAME	DESCRIPTION
15~0	Reserved	Set to 0.

Table 64: Checksum (Register 70)

BIT	NAME	DESCRIPTION
15~8	CheckSum	EEPROM Checksum.
7~0	Reserved	

4. Timing Requirements

Table 65: MII Transmit Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{tdv}	TXCLK to TXD valid time.	4	-	12	ns
t_{txev}	TXCLK to TXEN valid time.	4	-	12	ns

Table 66: RMII Transmit Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{tdv}	TXCLK to TXD valid time.	3	-	9	ns
t_{txev}	TXCLK to TXEN valid time.	3	-	14	ns

Note: Delays are assuming 10pf loading on the output pins.

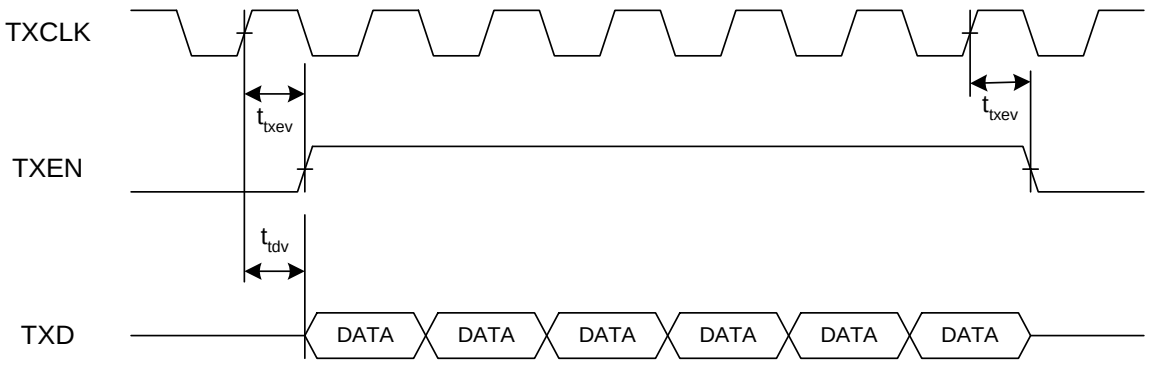

Figure 11 RMII/MII Transmit Timing Diagram

Table 67: MII Receive Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{rxds}	RX_DV, RXD, RX_ER, setup time.	10	-	-	ns
t_{rxdh}	RX_DV, RXD, RX_ER hold time.	5	-	-	ns

Table 68: RMII Receive Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{rxds}	RX_DV, RXD, RX_ER, setup time.	3	-	-	ns
t_{rxdh}	RX_DV, RXD, RX_ER hold time.	3	-	-	ns

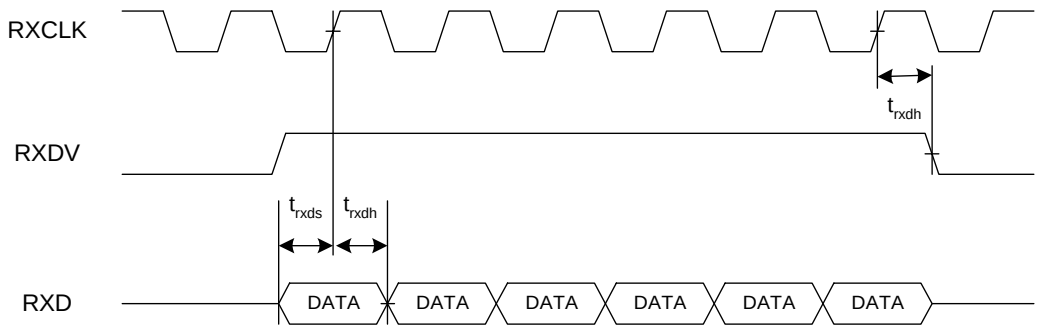

Figure 12 RMII/MII Receive Timing Diagram

Table 69: RoX-II Bus Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{roxs}	Setup time.	2	-	-	ns
t_{roxh}	Hold time.	2	-	-	ns

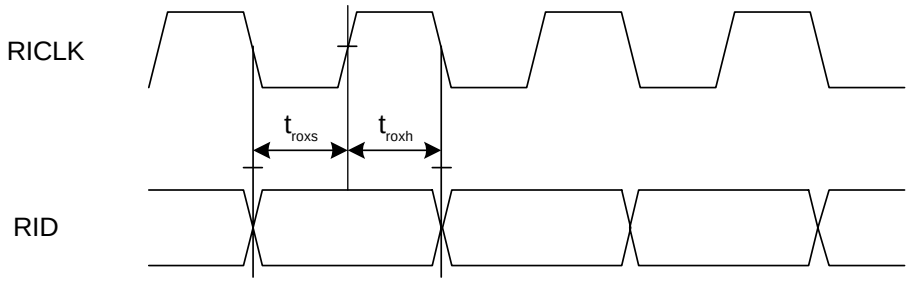

Figure 13 RoX-II Bus Timing

Table 70: PHY Management (MDIO) Read Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{ch}	MDC high time.	180	200	220	ns
t_{cl}	MDC low time.	180	200	220	ns
t_{mc}	MDC period.	-	400	-	ns
t_{d}	MDIO output delay.	10	-	300	ns

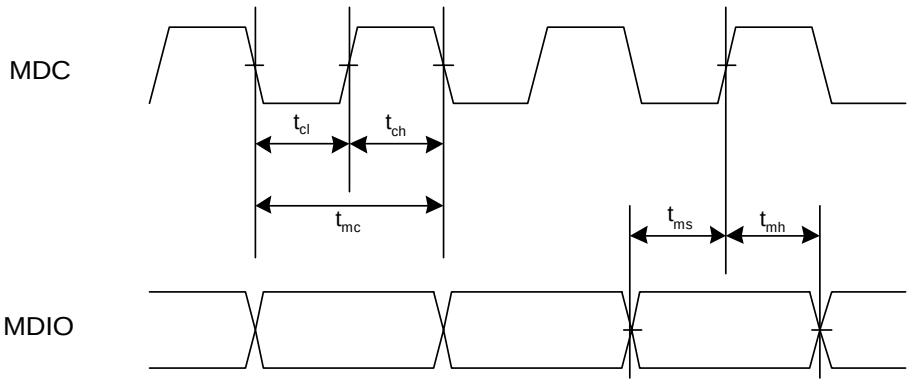

Figure 14 PHY Management Read Timing

Table 71: PHY Management (MDIO) Write Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{ch}	MDC high time.	180	200	220	ns
t_{cl}	MDC low time.	180	200	220	ns
t_{mc}	MDC period.	-	400	-	ns
t_{ms}	MDIO setup time.	10	-	-	ns
t_{mh}	MDIO hold time.	10	-	-	ns

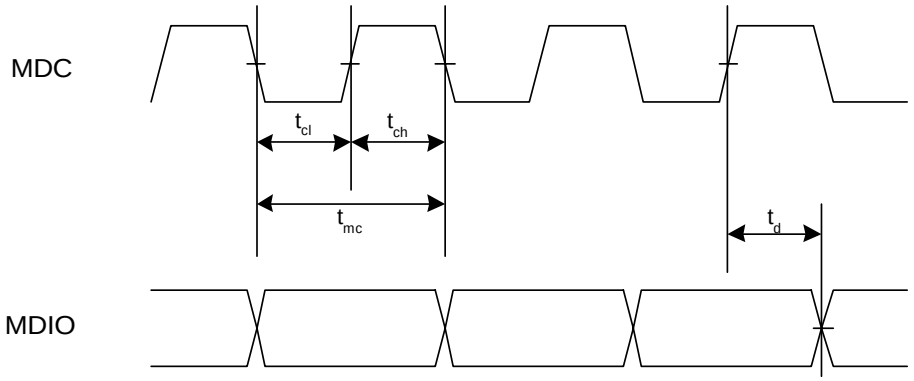

Figure 15 PHY Management Write Timing

Table 72: SGRAM Refresh Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{ah}	Access hold time.	1	-	-	ns
t_{as}	Access setup time.	3	-	-	ns
t_{ch}	PBCS#, PBRAS#, PBWE# hold time.	1	-	-	ns
t_{chi}	Clock high level width.	3.5	-	-	ns
t_{ck}	System clock cycle time.	10	-	-	ns
t_{ckh}	CKE hold time.	1	-	-	ns
t_{cks}	CKE setup time.	3	-	-	ns
t_{cl}	Clock low level width.	3.5	-	-	ns
t_{cs}	PBCS#, PBRAS#, PBWE# setup time.	3	-	-	ns

Table 72: SGRAM Refresh Timing (Continued)

t_{rp}	Precharge command period.	30	-	-	ns
t_{rc}	Auto-refresh to auto-refresh period.	90	-	-	ns

Table 73: SGRAM Read Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{ac}	Access time.	-	-	10	ns
t_{ah}	Access hold time.	2	-	-	ns
t_{as}	Access setup time.	2.5	-	-	ns
t_{ch}	PBCS#, PBRAS#, PBWE# hold time.	1	-	-	ns
t_{chi}	Clock high level width.	3	-	-	ns
t_{ck}	System clock cycle time.	13	-	-	ns
t_{ckh}	CKE hold time.	2	-	-	ns
t_{cks}	CKE setup time.	3	-	-	ns
t_{cl}	Clock low level width.	3	-	-	ns
t_{cs}	PBCS#, PBRAS#, PBWE# setup time.	2.5	-	-	ns
t_{hz}	Data out high impedance time.	-	-	8	ns
t_{lz}	Data out low impedance time.	2	-	-	ns
t_{oh}	Data out hold time.	2	-	-	ns
t_{ras}	Active to precharge command period.	48	-	-	ns
t_{rcd}	Active to read delay.	24	-	-	ns

Note: This timing requirement is for a SGRAM running at CAS Latency 2. Typically a -8 speed grade SGRAM needs to be used.

Table 74: SGRAM Write Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{ah}	Access hold time.	2	-	-	ns
t_{as}	Access setup time.	2.5	-	-	ns
t_{ch}	PBCS#, PBRAS#, PBWE# hold time.	1	-	-	ns
t_{chi}	Clock high level width.	3	-	-	ns
t_{ck}	System clock cycle time.	13	-	-	ns
t_{ckh}	CKE hold time.	2	-	-	ns
t_{cks}	CKE setup time.	3	-	-	ns
t_{cl}	Clock low level width.	3	-	-	ns
t_{cs}	PBCS#, PBRAS#, PBWE# setup time.	2.5	-	-	ns
t_{dh}	Data in hold time.	1	-	-	ns
t_{ds}	Data in setup time.	2.5	-	-	ns
t_{ras}	Active to precharge command period.	48	-	100,000	ns
t_{rcd}	Active to read delay.	24	-	-	ns

Note: This timing requirement is for a SGRAM running at CAS Latency 2. Typically a -8 speed grade SGRAM needs to be used.

5. Electrical Specifications

Note: Operation at absolute maximum ratings could cause permanent damage to the device.

Table 75: Maximum Ratings

DC Supply Voltage (VDD25) DC Supply Voltage (VDD33)	-0.3V ~ + 2.75V -0.3V ~ + 3.6V
DC Input Voltage	-0.3 ~ VDD33 + 0.3V
DC Output Voltage	-0.3 ~ VDD33 + 0.3V
DC Supply Voltage to MII	-0.6V to 6.0V
DC Input Voltage to MII	-0.6 to VDD33 + 0.3V
DC Output Voltage to MII	-0.6 to VDD33 + 0.3V
Storage Temperature	-55 ^{o}C to +150 ^{o}C

Table 76: Recommended Operation Conditions

Supply Voltage (VDD25) Supply Voltage (VDD33)	2.5V ± 0.25V 3.3V ± 0.3V
Operating Temperature	0 ^{o}C to 70 ^{o}C
Power Dissipation	1.7 W (typical)

Table 77: DC Electrical Characteristics

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
Voh	Output voltage-high, Ioh=4mA.	2.4	-	-	V
Vol	Output voltage-low, Ioh=4mA.	-	-	0.4	V
Ioz	High impedance state output current.	-10	-	10	uA
Iih	Input current-high. (With no pull-up or pull-down)	-10	-	10	uA
Iil	Input current-low. (With no pull-up or pull-down)	-10	-	10	uA
Vih	Input high voltage.	0.7*VDD33	-	-	V
Vil	Input low voltage.	-	-	0.3*VDD33	V
Icc	Supply current.	-	-	-	mA

6. AL126 Mechanical Data

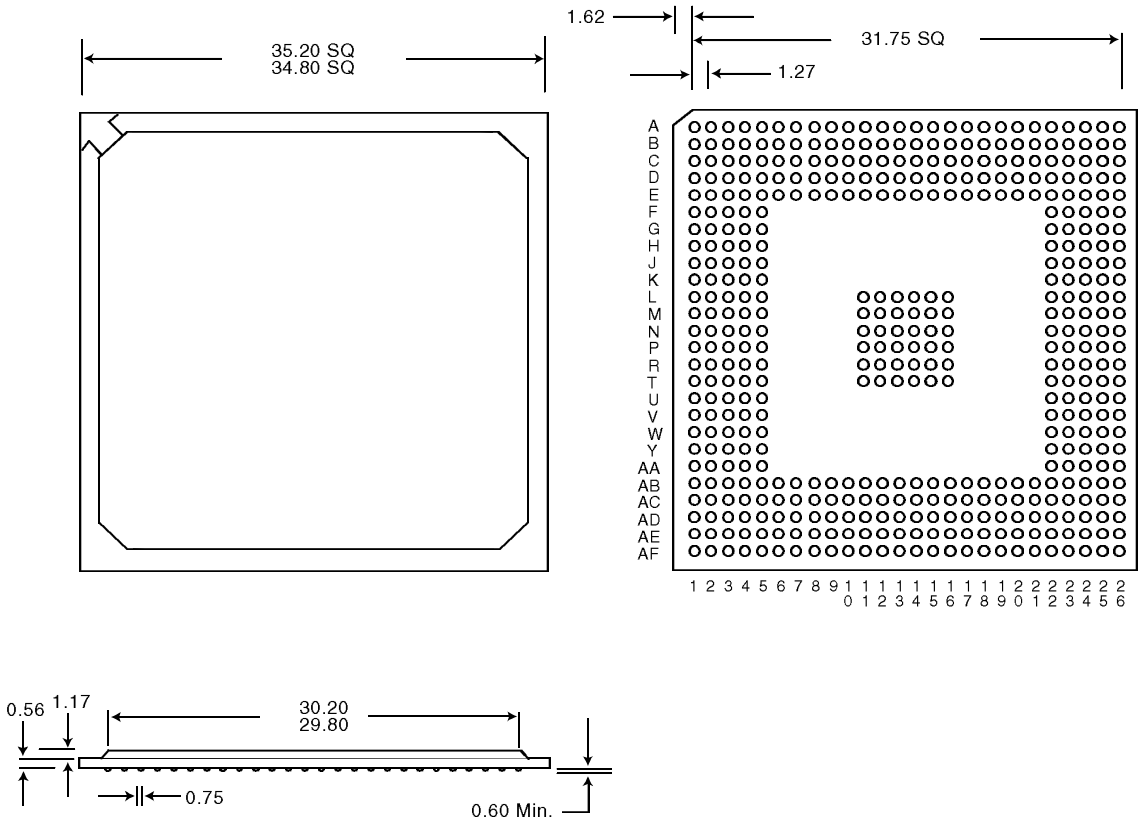

Figure 16 AL126 Mechanical Dimensions

7. Appendix I (VLAN Mapping Work Sheet)

PORT	BIT	PORT 0/REG. 1E	PORT 1/REG. 20	PORT 2/REG. 22	PORT 3/REG. 24	PORT 4/REG. 26	PORT 5/REG. 28	PORT 6/REG. 2A	PORT 7/REG. 2C
7	7								
6	6								
5	5								
4	4								
3	3								
2	2								
1	1								
0	0								

8. Appendix II (Port to Trunk Port Assignment Work Sheet)

	TRUNK / PORT	BIT/ VALUE	PORT 0/REG. 2F	PORT 1/REG. 30	PORT 2/REG. 31	PORT 3/REG. 32	PORT 4/REG. 33	PORT 5/REG. 34	PORT 6/REG. 35	PORT 7/REG. 36
TRUNK 1 BITS 3, 2	7	11								
	6	10								
	5	01								
	4	00								
TRUNK 0 BITS 1, 0	3	11								
	2	10								
	1	01								
	0	00								

9. Appendix III (Suggested Memory Components)

Note: This is only a partial list of memory components that can be used in Allayer devices.

The AL126 uses Frame Buffer SGRAM chips that require 32-bit wide SGRAM or SDRAM, that is 100 MHz or faster with CAS latency 2.

The AL126 uses MAC Table Memory SSRAM chips that require Sync Burst pipelined SSRAM, 100 MHz or faster.

The following lists some of the memory that can be used in the AL126.

DEVICE	FREQ.	8 Mbit SGRAM	16 Mbit SGRAM	SSRAM
AL126	100 MHz	N/A	MoSys - MG802C512L-10 Etron - EM636227Q-7 Oki - MS82V16520-7	Micron - MT58LC64K32D8LG-6.6 Micron - MT58L64L32PT-6.6 IDT - 71V632S4

10. Appendix IV (Memory Timing Requirements)

Note: These are the recommended timing requirements for 100 MHz systems.

Table 78: SSRAM Timing Requirements

SYMBOL	DESCRIPTION	MIN	MAX
t_{oehz}	OE# high to output high-Z.	-	-
t_{ds}	Data in setup time.	-	-
$t_{oehz} + t_{ds}$	OE# high to output high-Z + data in setup time.	-	5.9ns
t_{kq}	Clock to data output valid.	-	4.2ns

Table 79: SGRAM Timing Requirements

SYMBOL	DESCRIPTION	MIN	MAX
t_{ck}	System clock cycle time.	-	10ns
t_{rc}	Active to active delay.	-	70ns
t_{ras}	Active to precharge delay.	-	40ns
t_{co}	CLK to valid output delay.	-	7ns
t_{rcd}	Active to read/write delay.	-	20ns
t_{rp}	Precharge to active delay.	-	30ns

Revision History

Rev. 1.3 (7/18/99)

1. Added memory information in appendix III.

Rev. 1.3a (7/28/99)

1. Reformatted layout.

2. Added new PHY management timing diagrams.

3. Added new RMII and MII timing diagrams.

Rev. 1.4 (10/8/99)

1. Updated System Performance Tuning Control Register.

2. Updated electrical specifications section.

3. Corrected managed routing switch illustration.

Rev. 1.5 (10/25/99)

1. Added memory timing requirement tables in appendix IV.

2. Corrected tables 1-8 to reflect transmit signals are clocked out by the rising edge of the TX_CLK.

3. Updated MII transmit timing diagram and table.

4. Switched reserved bits 15~8 to 7~0 for VLAN Map Extension Register II (register 2E).

5. Removed testing control register tables. Updated default settings.

Rev. 1.6 (11/17/99)

1. Updated numbering for the port-based load balancing example.

2. Updated numbering for the port-based load balancing worksheet in appendix II.

3. Added RMII transmit timing table.

4. Changed the MII transmit timing diagram.

5. Added new Allayer logo.

6. Updated RMII/MII signal descriptions for ports 0 ~ port 7 in tables 1 through 8.

Rev. History (prelim. 1.7 to rev. 1.0)

1. Updated MaxAge information (table 22).

2. Updated SlowAge information (table 23).

3. Changed Testing Control Register (38) to reflect watermark information.

4. Updated uplink ID information in Port Config. Register I.

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