



# T-51-10-10 10-Bit 18 MSPS Monolithic A/D Converter

ANALOG DEVICES INC

AD773

## FEATURES

Monolithic 10-Bit 18 MSPS A/D Converter

Low Power Dissipation: 1.2 W

Signal-to-Noise Plus Distortion Ratio

$f_{IN} = 1 \text{ MHz}$ : 55 dB

$f_{IN} = 8 \text{ MHz}$ : 52 dB

Guaranteed No Missing Codes

On-Chip Track-and-Hold Amplifier

100 MHz Full Power Bandwidth

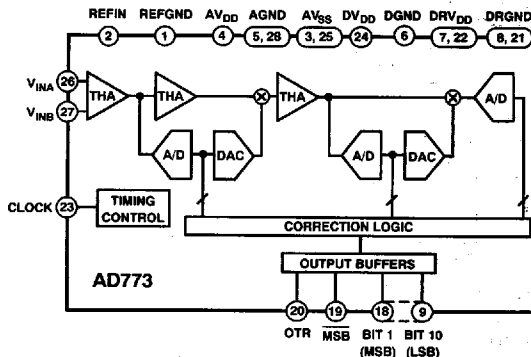
High Impedance Reference Input

Out of Range Output

Twos Complement and Binary Output Data

Available in Commercial and Military Temperature Ranges

## FUNCTIONAL BLOCK DIAGRAM



4

## PRODUCT DESCRIPTION

The AD773 is a monolithic 10-bit, 18 MSPS analog-to-digital converter incorporating an on-board, high performance track-and-hold amplifier (THA). The AD773 converts video bandwidth signals without the use of an external THA. The AD773 implements a multistage differential pipelined architecture with output error correction logic. The AD773 offers accurate performance and guarantees no missing codes over the full operating temperature range.

Output data is presented in binary and twos complement format. An out of range (OTR) signal indicates the analog input voltage is beyond the specified input range. OTR can be decoded with the MSB/MSB pins to signal an underflow or overflow condition. The high impedance reference input allows multiple AD773s to be driven in parallel from a single reference.

The combined dc precision and dynamic performance of the AD773 is useful in a variety of applications. Typical applications include: video enhancement, HDTV, ghost cancellation, ultrasound imaging, radar and high speed data acquisition.

The AD773 was designed using Analog Devices' ABCMOS-1 process which utilizes high speed bipolar and 2-micron CMOS transistors on a single chip. High speed, precision analog circuits are now combined with high density logic circuits. Laser trimmed thin film resistors are used to optimize accuracy and temperature stability.

The AD773 is packaged in a 28-pin ceramic DIP and is available in commercial (0°C to +70°C) and military (-55°C to +125°C) grades.

## PRODUCT HIGHLIGHTS

1. On-board THA  
The high impedance differential input THA eliminates the need for external buffering or sample and hold amplifiers. The THA offers the choice of differential or single-ended inputs. Input current is typically 5  $\mu$ A.
2. High Impedance Reference Input  
The high impedance reference input (200 k $\Omega$ ) allows direct connection with standard +2.5 V references, such as the AD680, AD580 and REF43.
3. Output Data Flexibility  
Output data is available in bipolar offset and bipolar twos complement binary format.
4. Out of Range (OTR)  
The OTR output bit indicates when the input signal is beyond the AD773's input range.

**AD773—SPECIFICATIONS**

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**DC SPECIFICATIONS** ( $T_{MIN}$  to  $T_{MAX}$  with  $AV_{DD} = +5\text{ V} \pm 5\%$ ,  $AV_{SS} = -5\text{ V} \pm 5\%$ ,  $DV_{DD} = +5\text{ V} \pm 5\%$ ,  $DRV_{DD} = +5\text{ V} \pm 5\%$ ,  $V_{REF} = +2.500\text{ V}$  unless otherwise indicated)

Parameter	AD773J			AD773K			Units
	Min	Typ	Max	Min	Typ	Max	
RESOLUTION	10			10			Bits
DC ACCURACY (+25°C)							
Integral Nonlinearity							LSB
$T_{MIN}$ to $T_{MAX}$	$\pm 1$			$\pm 0.75$ $\pm 2$			LSB
Differential Linearity Error							LSB
$T_{MIN}$ to $T_{MAX}$	$\pm 1$			$\pm 0.75$ $\pm 1$			LSB
Offset	0.5			0.5    3.5			% FSR
Gain Error	0.5			0.5    2.0			% FSR
No Missing Codes				GUARANTEED			
ANALOG INPUT							
Input Range	1			1			V p-p
Input Current	5    20			5    20			$\mu\text{A}$
Input Capacitance	10			10			pF
REFERENCE INPUT							
Reference Input Resistance	50			50			k $\Omega$
Reference Input	200			200			Volts
Reference Input	2.5			2.5			
LOGIC INPUT							
High Level Input Voltage	+3.5			+3.5			V
Low Level Input Voltage							V
High Level Input Current ( $V_{IN} = DV_{DD}$ )	-10			-10			$\mu\text{A}$
Low Level Input Current ( $V_{IN} = 0\text{ V}$ )	-10			-10			$\mu\text{A}$
Input Capacitance	10			10			pF
LOGIC OUTPUTS							
High Level Output Voltage ( $I_{OH} = 0.5\text{ mA}$ )	+2.4			+2.4			V
Low Level Output Voltage ( $I_{OL} = 1.6\text{ mA}$ )	+0.4			+0.4			V
POWER SUPPLIES							
Operating Voltages							
$AV_{DD}$	+4.75			+4.75			Volts
$AV_{SS}$	-5.25			-5.25			Volts
$DV_{DD}$ , $DRV_{DD}$	+4.75			+4.75			Volts
Operating Current							
$I_{AV_{DD}}$	85			85			mA
$I_{AV_{SS}}$	-140			-140			mA
$I_{DV_{DD}}$	20			20			mA
$I_{DRV_{DD}}^1$	15			15			mA
POWER CONSUMPTION <sup>2</sup>	1.2			1.2			W
POWER SUPPLY REJECTION	6			6			mV/V
TEMPERATURE RANGE							
Specified (J/K)	0			0			°C

## NOTES

<sup>1</sup> $C_L = 15\text{ pF}$  typical.<sup>2</sup>100% production tested.

Specifications subject to change without notice. See Definition of Specifications for additional information.

**AC SPECIFICATIONS** ( $T_{MIN}$  to  $T_{MAX}$  with  $AV_{DD} = +5V \pm 5\%$ ,  $AV_{SS} = -5V \pm 5\%$ ,  $DV_{DD} = +5V \pm 5\%$ ,  $DRV_{DD} = +5V \pm 5\%$ ,  $V_{REF} = +2.500V$  unless otherwise indicated,  $f_{SAMPLE} = 18$  MSPS,  $f_{IN}$  amplitude =  $-0.3$  dB)

Parameter	AD773J			AD773K			Units
	Min	Typ	Max	Min	Typ	Max	
<b>DYNAMIC PERFORMANCE<sup>1</sup></b>							
Signal-to-Noise plus Distortion (S/N+D) Ratio							
$f_{IN} = 1$ MHz	52	56		54	56		dB
$f_{IN} = 8.1$ MHz	45	53		47	53		dB
$f_{IN} = 9$ MHz		53			53		dB
Effective Number of Bits (ENOB)							
$f_{IN} = 1$ MHz		9.0			9.0		Bits
$f_{IN} = 8.1$ MHz		8.5			8.5		Bits
$f_{IN} = 9$ MHz		8.5			8.5		Bits
Total Harmonic Distortion (THD)							
$f_{IN} = 1$ MHz		-64	-57		-64	-59	dB
$f_{IN} = 8.1$ MHz		-55	-46		-55	-48	dB
$f_{IN} = 9$ MHz		-56			-56		dB
Spurious Free Dynamic Range <sup>2</sup>		-67			-67		dB
Full Power Bandwidth		100			100		MHz
Intermodulation Distortion (IMD) <sup>3</sup>							
Second Order Products		-69			-69		dB
Third Order Products		-63			-63		dB
Differential Phase		0.2			0.2		Degree
Differential Gain		0.8			0.8		%
Transient Response		25			25		ns
Overtolerance Recovery Time		25			25		ns

**NOTES**

<sup>1</sup>For typical dynamic performance curves at  $f_{SAMPLE} = 16.2$  MSPS and 18 MSPS, see Figures 2 through 13.

<sup>2</sup> $f_{IN} = 1$  MHz.

<sup>3</sup> $f_a = 1.0$  MHz,  $f_b = 1.05$  MHz.

Specifications subject to change without notice.

**TIMING SPECIFICATIONS** (for all grades  $T_{MIN}$  to  $T_{MAX}$  with  $AV_{DD} = +5V \pm 5\%$ ,  $AV_{SS} = -5V \pm 5\%$ ,  $DV_{DD} = +5V \pm 5\%$ ,  $DRV_{DD} = +5V \pm 5\%$ ,  $V_{REF} = +2.500V$  unless otherwise indicated,  $f_{SAMPLE} = 18$  MSPS)

	Symbol	Min	Typ	Max	Units
Conversion Rate				18	MSPS
Clock Period	$t_{CLK}$	55			ns
Clock High	$t_{CH}$	27			ns
Clock Low	$t_{CL}$	27			ns
Output Delay	$t_{OD}$		20		ns
Aperture Delay			7		ns
Aperture Jitter			9	32	ps
Pipeline Delay (Latency)				4	Clock Cycles

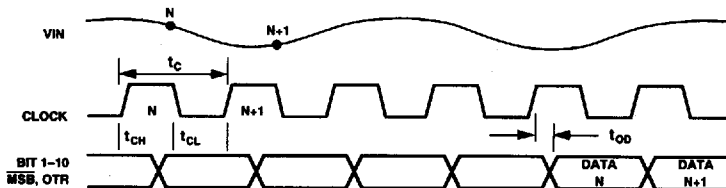


Figure 1. AD773 Timing Diagram

**CAUTION**

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

**ABSOLUTE MAXIMUM RATINGS\***

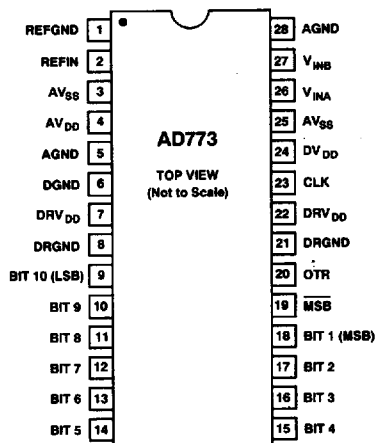
Parameter	With Respect to	Min	Max	Units
$V_{DD}$	AGND	-0.5	+6.5	V
$V_{SS}$	AGND	-6.5	+0.5	V
$DV_{DD}$ , $DRV_{DD}$	DGND, DRGND	-0.5	+6.5	V
AGND	DGND, DRGND	-1.0	+1.0	V
$V_{DD}$ , $V_{SS}$	$DV_{DD}$ , $DRV_{DD}$	-6.5	+0.5	V
CLK	$DV_{DD}$ , $DRV_{DD}$	-6.5	+0.5	V
REFIN	REFGND, AGND	-0.5	+6.5	V
Junction Temperature			+150	°C
Storage Temperature		-65	+150	°C
Lead Temperature (10 sec)			+300	°C

\*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

**ORDERING GUIDE**

Model	Temperature Range	Description	Package Option*
AD773JD	0°C to +70°C	28-Pin Ceramic DIP	D-28
AD773KD	0°C to +70°C	28-Pin Ceramic DIP	D-28

\*D = Ceramic DIP. For outline information see Package Information section.

**PIN CONFIGURATION****PIN DESCRIPTION**

Symbol	Pin No.	Type	Name and Function
AGND	5, 28	P	Analog Ground.
$V_{DD}$	4	P	+5 V Analog Supply.
$V_{SS}$	3, 25	P	-5 V Analog Supply.
BIT 1 (MSB)	18	DO	Most Significant Bit.
BIT 2-BIT 9	17-10	DO	Data Bit 2 through Data Bit 9.
BIT 10 (LSB)	9	DO	Least Significant Bit.
CLK	23	DI	Clock Input. The AD773 will initiate a conversion on the falling edge of the clock input. See the Timing Diagram for details.
$DV_{DD}$	24	P	+5 V Digital Supply.
$DRV_{DD}$	7, 22	P	+5 V Digital Supply for the output drivers.
DGND	6	P	Digital Ground.
DRGND	8, 21	P	Digital Ground for the output drivers.
MSB	19	DO	Inverted Most Significant Bit. Provides twos complement output data format.
OTR	20	DO	Out of Range is Active HIGH on the leading edge of Code 0 or the trailing edge of Code 1023. See Output Data Format Table II.
REF GND	1	AI	REF GND is connected to the ground of the external reference.
REF IN	2	AI	REF IN is the external 2.5 V reference input, taken with respect to REF GND.
$V_{INA}$	26	AI	(+) Analog input signal to the differential input THA.
$V_{INB}$	27	AI	(-) Analog input signal to the differential input THA.

Type: AI = Analog Input; DI = Digital Input; DO = Digital Output; P = Power.

**INTEGRAL NONLINEARITY (INL)**

Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale." The point used as "zero" occurs 1/2 LSB before the first code transition. "Full scale" is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line.

**DIFFERENTIAL LINEARITY ERROR (DNL, NO MISSING CODES)**

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value.

**OFFSET**

The first transition should occur at a level 1/2 LSB above "zero." Offset is defined as the deviation of the actual first code transition from that point.

**GAIN ERROR**

The last code transition should occur for an analog value 1 1/2 LSB below the nominal full scale. The gain error is the deviation of the actual level at the last transition from the ideal level.

**POWER SUPPLY REJECTION**

One of the effects of power supply variation on the performance of the device will be a change in gain error. The specification shows the maximum gain error deviation as the supplies are varied from their nominal values to their specified limits.

**SIGNAL-TO-NOISE PLUS DISTORTION (S/N+D) RATIO**

S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

**EFFECTIVE NUMBER OF BITS (ENOB)**

ENOB is calculated from the following expression:

$S/N+D = 6.02N + 1.76$ , where N is equal to the effective number of bits.

**TOTAL HARMONIC DISTORTION (THD)**

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

**SPURIOUS FREE DYNAMIC RANGE**

The peak spurious or peak harmonic component is the largest spectral component excluding the input signal and dc. This value is expressed in decibels relative to the rms value of a full-scale input signal.

**INTERMODULATION DISTORTION (IMD)**

With inputs consisting of sine waves at two frequencies,  $f_a$  and  $f_b$ , any device with nonlinearities will create distortion products, of order  $(m+n)$ , at sum and difference frequencies of  $m f_a \pm n f_b$ , where  $m, n = 0, 1, 2, 3 \dots$ . Intermodulation terms are those for which  $m$  or  $n$  is not equal to zero. For example, the second order terms are  $(f_a+f_b)$  and  $(f_a-f_b)$  and the third order terms are  $(2f_a+f_b)$ ,  $(2f_a-f_b)$ ,  $(f_a+2f_b)$  and  $(f_a-2f_b)$ . The IMD products are expressed as the decibel ratio of the rms sum of the measured input signals to the rms sum of the distortion terms. The two signals are of equal amplitude and the peak value of their sums is  $-0.5$  dB from full scale. The IMD products are normalized to a 0 dB input signal.

**DIFFERENTIAL GAIN**

The percentage difference between the output amplitudes of a small high frequency sine wave at two stated levels of a low frequency signal on which it is superimposed.

**DIFFERENTIAL PHASE**

The difference in the output phase of a small high frequency sine wave at two stated levels of a low frequency signal on which it is superimposed.

**TRANSIENT RESPONSE**

The time required for the AD773 to achieve its rated accuracy after a full-scale step function is applied to its input.

**OVERVOLTAGE RECOVERY TIME**

The time required for the ADC to recover to full accuracy after an analog input signal 150% of full scale is reduced to 50% of the full-scale value.

**APERTURE DELAY**

The difference between the switch delay and the analog delay of the THA. This effective delay represents the point in time, relative to the rising edge of the CLOCK input, that the analog input is sampled.

**APERTURE JITTER**

The variations in aperture delay for successive samples.

**PIPELINE DELAY (LATENCY)**

The number of clock cycles between conversion initiation and the associated output data being made available. New output data is provided every clock cycle.

**FULL POWER BANDWIDTH**

The input frequency at which the amplitude of the reconstructed fundamental is reduced by 3 dB for a full-scale input.

AD773—Dynamic Characteristics

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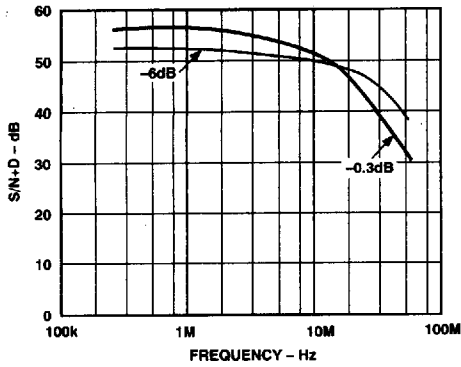


Figure 2. S/N+D vs. Input Frequency,  $f_{CLK} = 18$  MSPS

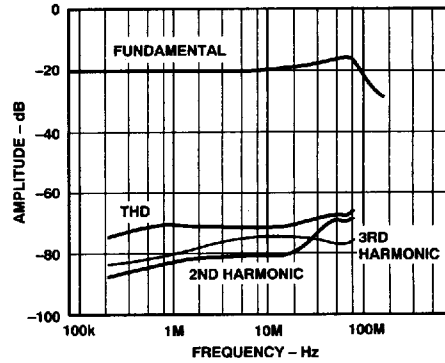


Figure 5. Harmonic Distortion vs. Input Frequency,  $f_{CLK} = 18$  MSPS: Small Signal

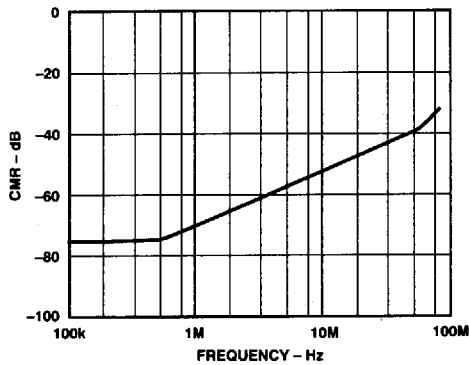


Figure 3. CMR vs. Input Frequency  $f_{CLK} = 18$  MSPS

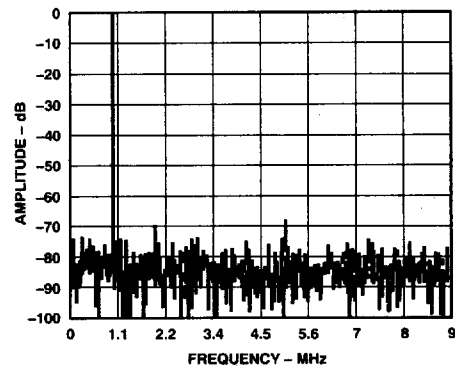


Figure 6. Typical FFT Plot of AD773,  $f_{CLK} = 18$  MSPS,  $f_{IN} = 1$  MHz at 1 V p-p

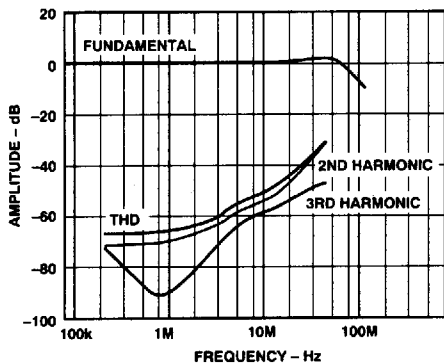


Figure 4. Harmonic Distortion vs. Input Frequency,  $f_{CLK} = 18$  MSPS: Full Power

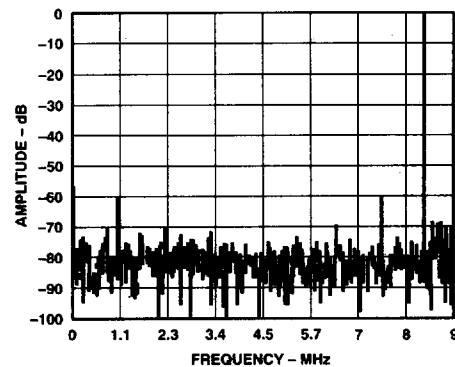


Figure 7. Typical FFT Plot of AD773,  $f_{CLK} = 18$  MSPS,  $f_{IN} = 8.5$  MHz at 1 V p-p

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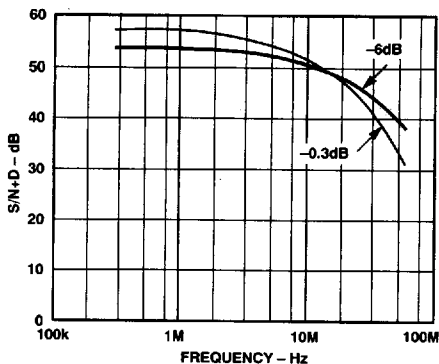


Figure 8. S/N+D vs. Input Frequency,  $f_{CLK} = 16.2$  MSPS

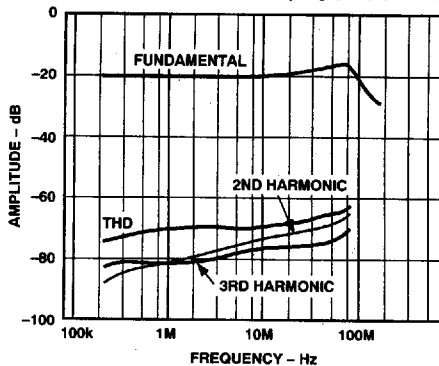


Figure 11. Harmonic Distortion vs. Input Frequency,  $f_{CLK} = 16.2$  MSPS: Small Signal

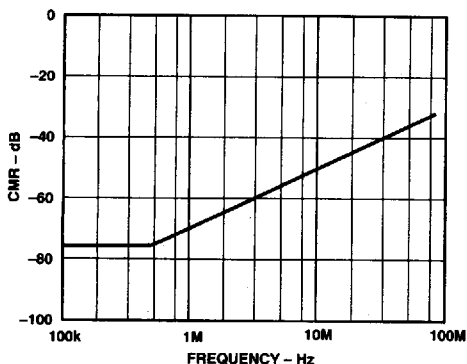


Figure 9. CMR vs. Input Frequency,  $f_{CLK} = 16.2$  MSPS

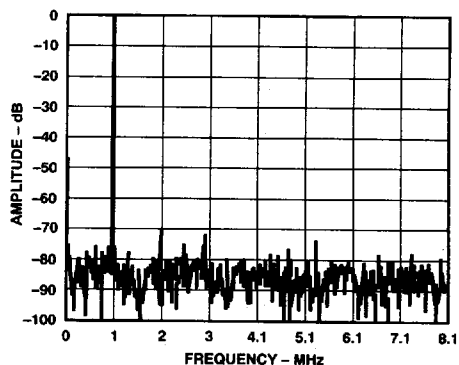


Figure 12. Typical FFT Plot of AD773,  $f_{CLK} = 16.2$  MHz,  $f_{IN} = 1$  MHz at 1 V p-p

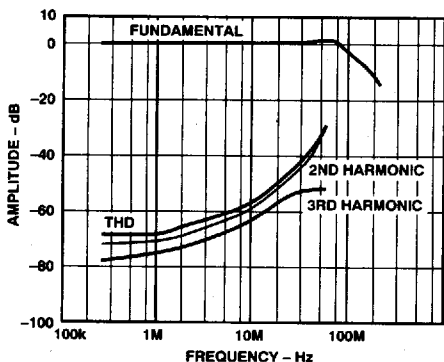


Figure 10. Harmonic Distortion vs. Input Frequency,  $f_{CLK} = 16.2$  MSPS: Full Power

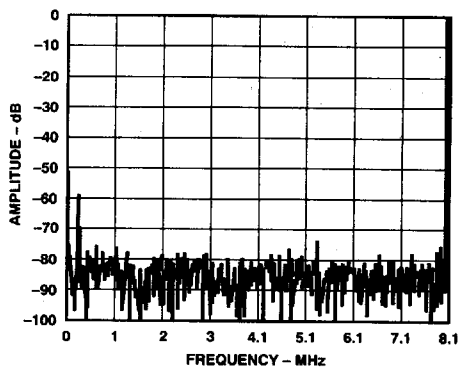


Figure 13. Typical FFT Plot of AD773,  $f_{CLK} = 16.2$  MHz,  $f_{IN} = 8.05$  MHz at 1 V p-p

AD773

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## Theory of Operation

The AD773 uses a pipelined multistage architecture with a differential input, fast settling track-and-hold amplifier (THA). Traditionally, high speed ADCs have used parallel, or flash architectures. When compared to flash converters, multistage architectures reduce the power dissipation and die size by reducing the number of comparators. For example, the AD773 uses 48 comparators compared to 1023 comparators for a 10-bit flash architecture.

The AD773's main signal path transmits differential current mode signals. Low impedance current summing techniques are employed, increasing speed by reducing sensitivity to parasitic capacitances. Pipelining allows the stages to operate concurrently and maximizes system throughput.

The input THA is followed by three 4-bit conversion stages. At any given time, the first stage operates on the most recent sample, while the second stage operates on a signal dependent on the previous sample. This process continues throughout all three stages. The twelve digital bits provided by the three 4-bit stages are combined in the correction logic to produce a 10-bit representation of the sampled analog input.

Pipeline delay, or latency, is four clock cycles. New output data is provided every clock cycle and is provided in both binary and twos complement format. The AD773 will flag an out-of-range condition when the analog input exceeds the specified analog input range.

## Applying the AD773

### DRIVING THE AD773 INPUT

The AD773 may be driven in a single-ended or differential fashion.  $V_{INA}$  is the positive input, and  $V_{INB}$  is the negative input. In the single-ended configuration either  $V_{INA}$  or  $V_{INB}$  is connected to Analog Ground (AGND) while the other input is driven with a full-scale input of  $\pm 500$  mV p-p. An inverted mode of operation can be achieved by simply interchanging the input connections.

Both inputs of the AD773,  $V_{INA}$  and  $V_{INB}$ , are high impedance and do not need to be driven by a low impedance source. Note, however, that as the source impedance increases, the input node becomes more susceptible to noise. The increased noise at the input will degrade performance. A 10 pF capacitor across  $V_{INA}$  and  $V_{INB}$  as shown in Figure 14 is recommended to bypass high frequency noise.

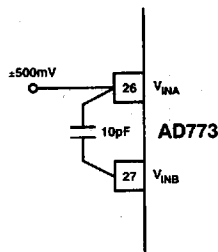


Figure 14. AD773 Single-Ended Input Connection

### INPUT CONDITIONING

In some cases, it may be appropriate to buffer the input source, add dc offset, or otherwise condition the input signal of the AD773. Choosing an appropriate op amp will vary with system requirements and the desired level of performance. Some suggested op amps are the AD9617, AD842, and AD827.

Figure 15 shows a typical application where a unipolar signal is level shifted to the bipolar input range of the AD773. Note that the reference used with the AD773 can also provide a noise-free voltage source to generate the dc offset.

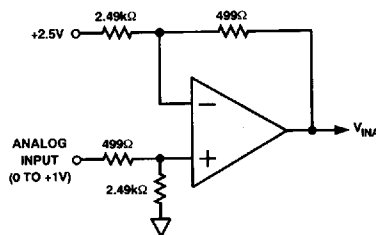


Figure 15. Unipolar to Bipolar Input Connection

### DIFFERENTIAL INPUT CONNECTIONS

Operating the AD773 with fully differential inputs offers the advantage of rejecting common-mode signals present on both  $V_{INA}$  and  $V_{INB}$ . The full-scale input range of  $V_{INA}$  and  $V_{INB}$  when driven differentially is  $\pm 250$  mV p-p as shown in Table I.

Table I. AD773's Maximum Differential Input Voltage

$V_{INA}$	$V_{INB}$	$V_{INA}-V_{INB}$
+250 mV	-250 mV	+500 mV
-250 mV	+250 mV	-500 mV

In some applications it may be desirable to convert a single-ended signal to a differential signal before being applied to the AD773. Figure 16 shows a single-ended to differential video line driver capable of driving doubly terminated cables.

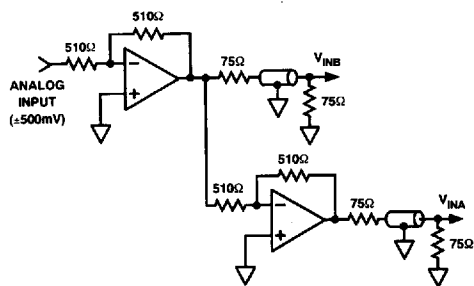


Figure 16. Single-Ended to Differential Connection



**REFERENCE INPUT**

The AD773's high impedance reference input allows direct connection with standard voltage references. Unlike the resistor ladder requirements of a flash converter the AD773's single pin, high impedance input can be driven from one low cost, low power reference. The high impedance input allows multiple AD773's to be driven from one reference thus minimizing drift errors.

Figure 17 shows the AD773 connected to the AD680. The AD680 is a single supply, low power, low cost 2.5 V reference with performance specifications ideally suited for the AD773. The low pass filter minimizes the AD680's wideband noise. Other recommended 2.5 V references are the AD580 and REF43.

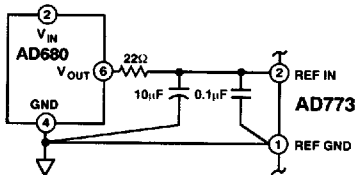


Figure 17. Recommended AD773 to AD680 Connection

**CLOCK INPUT**

The AD773's pipelined architecture operates on both the rising and falling edges of the clock input. A low jitter, symmetrical clock will provide the highest level of performance. The recommended logic families to drive the clock input are HC and F. The AD773's minimum clock half cycle may necessitate the use of an external divide-by-two circuit as shown in Figure 18. Power dissipation will vary with input clock frequency. Figure 19 shows the AD773's power dissipation vs. input clock frequency.

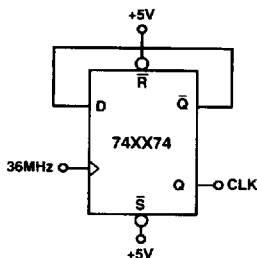


Figure 18. Divide-by-Two Clock Circuit

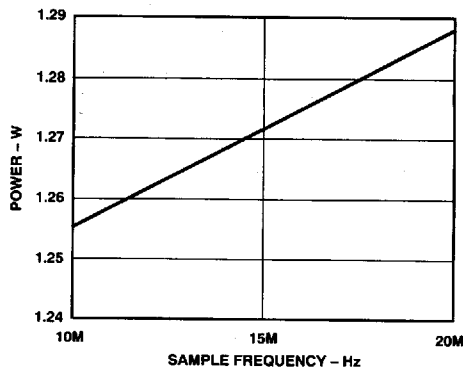


Figure 19. Power Dissipation vs. Sample Frequency

**EQUIVALENT ANALOG INPUT CIRCUIT**

The AD773 equivalent analog input circuit is shown in Figure 20. The typical input bias current is 5  $\mu$ A, while input capacitance is typically 5 pF. In the single-ended input configuration one input is connected to AGND while the second input is driven to full scale ( $\pm 500$  mV). Under nominal conditions the collector of the input transistor is at +1.15 V. This allows signals to be offset by up to +0.65 V without significantly degrading performance. In the negative direction, the emitter of the input transistor should not drop below -1.25 V. Therefore, signals can be offset by -0.65 V without significant performance degradation. Figure 21 shows signal-to-noise ratio vs. common-mode input voltage.

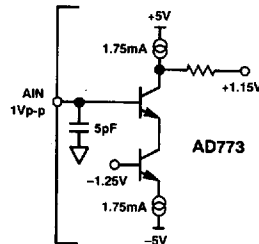


Figure 20. Equivalent Analog Input Circuit

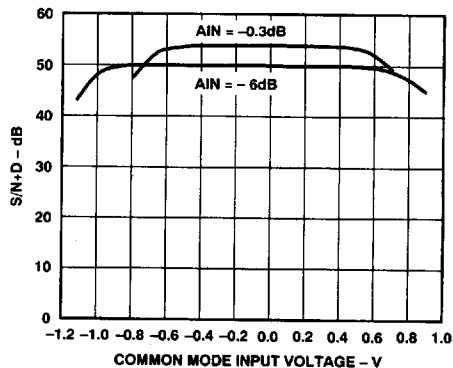


Figure 21. S/N+D vs. Common-Mode Input Voltage,  $f_{CLK} = 18$  MSPS

**EQUIVALENT REFERENCE INPUT CIRCUIT**

The AD773 is designed to have a reference to analog input voltage ratio of 2.5:1. When the AD773 is configured for single-ended operation a 2.5 volt reference input establishes a full-scale analog input voltage of 1 V p-p ( $\pm 500$  mV with respect to  $V_{INB}$ ). Although the AD773 is specified and tested with  $V_{REF}$  equal to 2.5 V and  $V_{IN}$  equal to  $\pm 500$  mV the reference input voltage and analog input voltages can be changed. To optimize the AD773's performance the 2.5:1 ratio should be maintained. The simplified model of the AD773's reference input circuit is shown in Figure 22.

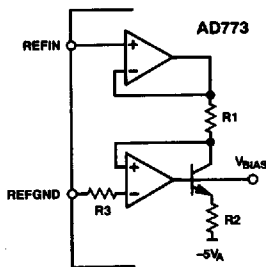


Figure 22. Typical Reference Input Circuit

The 2.5 V external reference is applied across resistor R1 producing a current which in turn generates a voltage  $V_{BIAS}$ . Multiple reference currents are generated from  $V_{BIAS}$  and are used throughout the converter. R3 is used to cancel errors induced by the input bias current of the REF GND buffer. Figure 23 shows the SNR performance as the reference voltage is varied from its nominal value of 2.5 V. The input full-scale voltage is defined by the following equation,

$$\text{Input Full-Scale Voltage} = \frac{\text{Reference Voltage}}{2.5}$$

The power dissipation is modulated by variations in the reference voltage. Figure 24 shows the variation in power dissipation versus reference voltage.

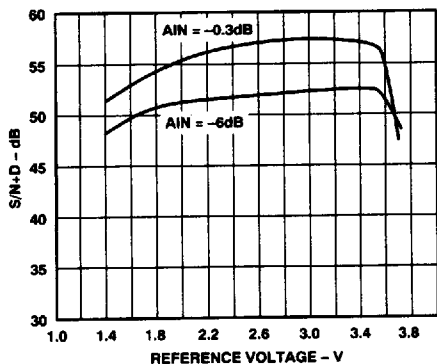


Figure 23. S/N+D vs. Reference Input Voltage,  $f_{CLK} = 18$  MSPS,  $f_{IN} = 1$  MHz

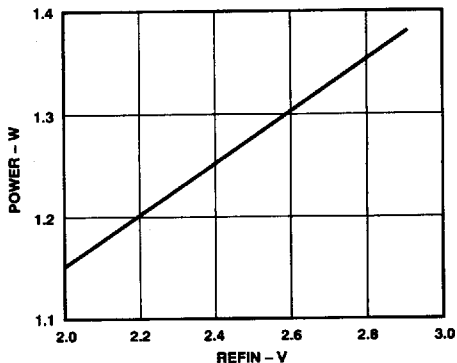


Figure 24. Power Dissipation vs. Reference Input Voltage

**TRANSIENT RESPONSE**

The fast settling input THA accurately converts full-scale input voltage swings in under one clock cycle. The THA's high impedance, fast slewing performance is critical in multiplexed or dc stepped (charge coupled devices, infrared detectors) systems. Figure 25 show the AD773's settling performance with an input signal stepped from  $-500$  mV to 0V. As can be seen, the output code settles to its final value in under one clock cycle.

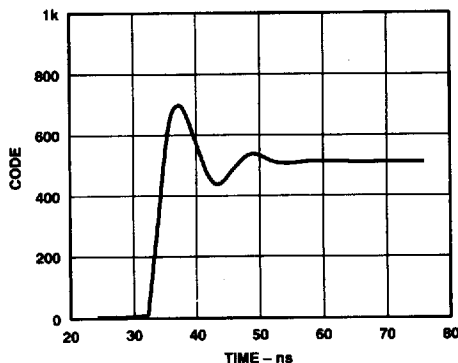


Figure 25. Typical AD773 Settling Time

**OUTPUT DATA FORMAT**

The AD773 provides both MSB and  $\overline{\text{MSB}}$  outputs, delivering positive true offset binary and twos complement output data. Table II shows the AD773's output data format.

Table II. Output Data Format

Analog Input	Digital Output		
	Offset Binary	Twos Complement	OTR
$V_{\text{INA}} - V_{\text{INB}}$			
$\geq 499.5 \text{ mV}$	11 1111 1111	01 1111 1111	1
499 mV	11 1111 1111	01 1111 1111	0
0 mV	10 0000 0000	00 0000 0000	0
-500 mV	00 0000 0000	10 0000 0000	0
$\leq -500.5 \text{ mV}$	00 0000 0000	10 0000 0000	1

**OUT OF RANGE**

An out-of-range condition exists when the analog input voltage is beyond the input range ( $\pm 500 \text{ mV}$ ) of the converter. [Note the AD773 has a 4 clock cycle latency rating.] OTR (Pin 20) is set low when the analog input voltage is within the analog input range. OTR is set HIGH and will remain HIGH when the analog input voltage exceeds the input range by 1/2 LSB from the center of the  $\pm$  full-scale output codes. OTR will remain HIGH until the analog input is within the input range. By logical ANDing OTR with the MSB and its complement, overrange high or underrange low conditions can be detected. Table III is a truth table for the over/under range circuit in Figure 26. Systems requiring programmable gain conditioning prior to the AD773 can immediately detect an out of range condition, thus eliminating gain selection iterations.

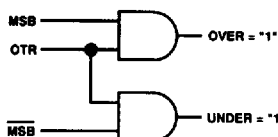


Figure 26. Overrange or Underrange Logic

Table III. Out-of-Range Truth Table

OTR	MSB	ANALOG INPUT IS
0	0	In Range
0	1	In Range
1	0	Underrange
1	1	Overrange

**GROUNDING AND LAYOUT RULES**

As is the case for any high performance device, proper grounding and layout techniques are essential in achieving optimal performance. The analog and digital grounds on the AD773 have been separated to optimize the management of return currents in a system. It is recommended that a 4-layer printed circuit board (PCB) which employs ground planes and power planes be used with the AD773. The use of ground and power planes offers distinct advantages:

1. The minimization of the loop area encompassed by a signal and its return path.
2. The minimization of the impedance associated with ground and power paths.
3. The inherent distributed capacitor formed by the power plane, PCB insulation, and ground plane.

These characteristics result in both a reduction of electromagnetic interference (EMI) and an overall improvement in performance.

It is important to design a layout which prevents noise from coupling onto the input signal. The wide input bandwidth of the AD773 permits noise outside the desired Nyquist bandwidth to be digitized along with the desired signal. This can result in a higher overall level of spurious noise in the digitized spectrum. Digital signals should not be run in parallel with the input signal traces and should be routed away from the input circuitry. It is also suggested that the traces associated with  $V_{\text{INA}}$  and  $V_{\text{INB}}$  be the same length.

Separate analog and digital ground should be joined together directly under the AD773 (see Figure 30). A solid ground plane under the AD773 is also acceptable if care is taken in the management of the power and ground return currents. A general "rule-of-thumb" for mixed signal layouts dictate that the return currents from digital circuitry should not pass through critical analog circuitry.

**POWER SUPPLY DECOUPLING**

The analog and digital supplies of the AD773 have been separated to prevent the typically large transients associated with digital circuitry from coupling into the analog supplies ( $AV_{\text{DD}}$ ,  $AV_{\text{SS}}$ ). Each power supply pin should be decoupled with a 0.1  $\mu\text{F}$  capacitor located as close to the pin as possible. Additional 0.1  $\mu\text{F}$  capacitors in parallel with the  $DRV_{\text{DD}}$  and  $DDV_{\text{DD}}$  bypass capacitors are required to adequately suppress high frequency noise. For optimal performance, surface-mount capacitors are recommended. The inductance associated with the leads of through-hole ceramic capacitors typically render them ineffective at higher frequencies. A complete system will also incorporate tantalum capacitors in the 10-100  $\mu\text{F}$  range to decouple low frequency noise and ferrite beads to limit high frequency noise.

The digital supplies have additionally been separated into  $DRV_{\text{DD}}$  and  $DV_{\text{DD}}$ . The  $DRV_{\text{DD}}$  pins provide power for the digital output drivers of the AD773 and are likely to contain high energy transients. Pin 22 should be decoupled directly to Pin 21 (DRGND) and Pin 7 should be decoupled directly to Pin 8 (DRGND) to minimize the length of the return path for these transients. A single +5 V supply is all that is required for  $DRV_{\text{DD}}$  and  $DV_{\text{DD}}$ , but decoupling  $DV_{\text{DD}}$  with an RC filter network is suggested (see Figure 27).

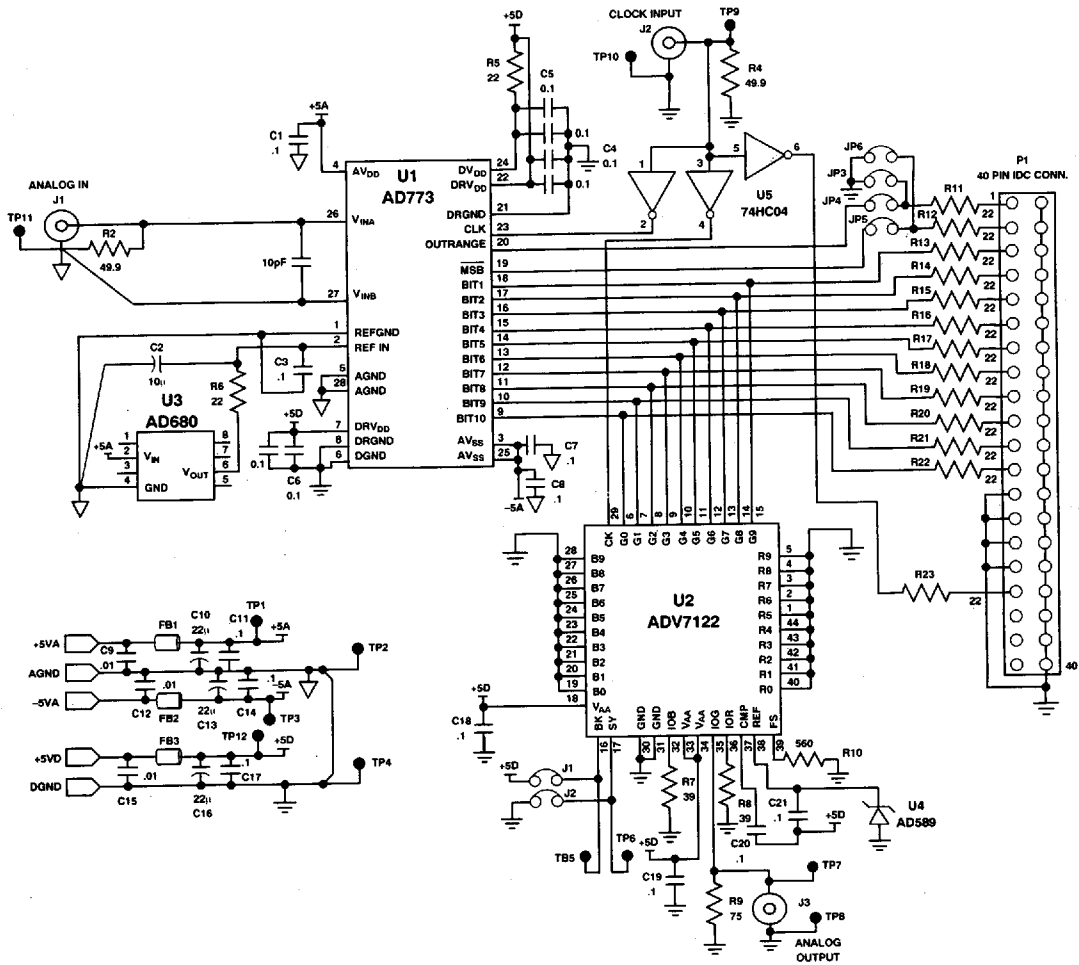


Figure 27. AD773 Evaluation Board Schematic

Table IV. Components List

Reference Designator	Description	Quantity
R2, R4	Resistor, 1%, 49.9 Ω	2
R5, R6, R11-R22	Resistor, 5%, 22 Ω	14
R7, R8	Resistor, 5%, 39 Ω	2
R9	Resistor, 5%, 75 Ω	1
R10	Resistor, 5%, 560 Ω	1
C1, C3-C8, C11, C14, C17-C21	Chip Cap, 0.1 μF	14
C2	Capacitor, Tantalum, 10 μF	1
C9, C12, C15	Chip Cap, 0.01 μF	3
C10, C13, C16	Capacitor, Tantalum, 22 μF	3
U1	AD773	1
U2	ADV7122	1
U3	AD680	1
U4	AD589	1
U5	74AS04	1
FB1-FB3	Ferrite Bead	3

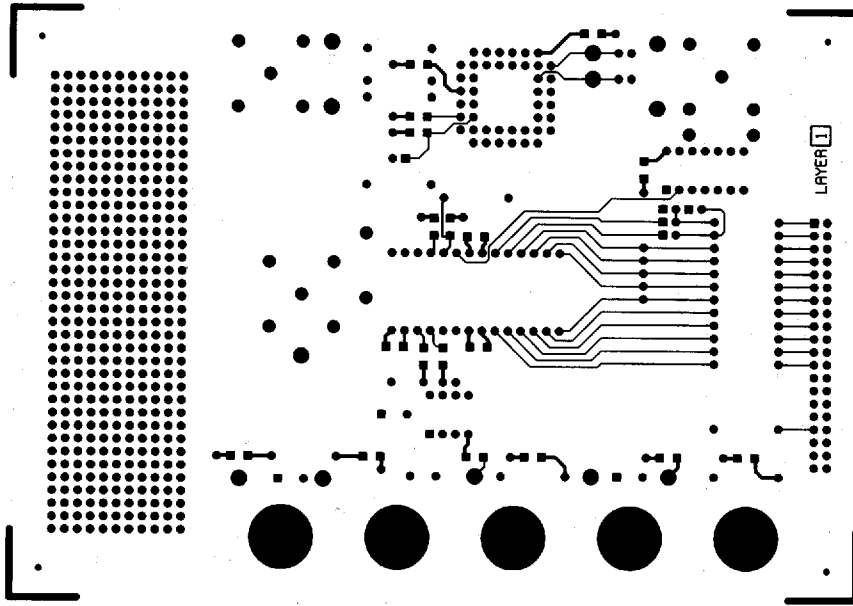


Figure 28. Component Side PCB Layout

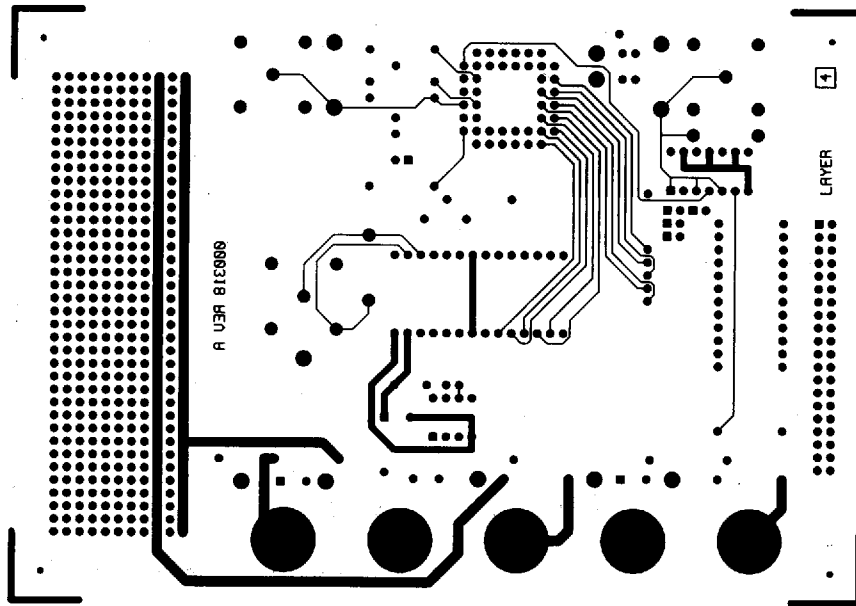


Figure 29. Solder Side PCB Layout

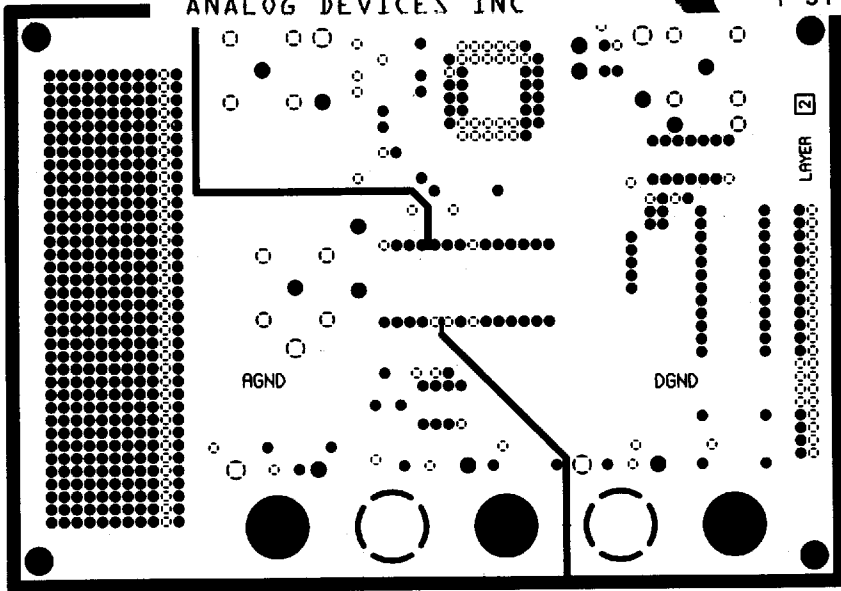


Figure 30. Ground Layer PCB Layout

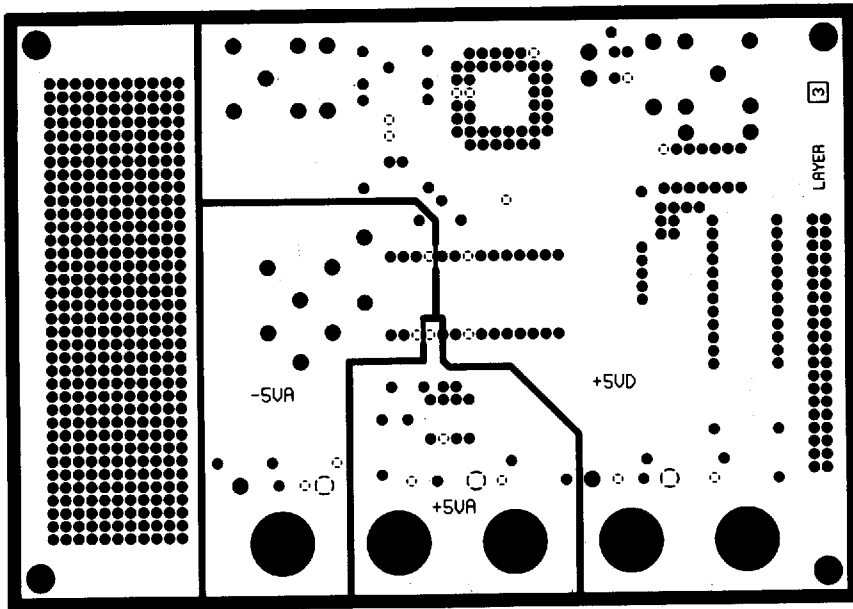


Figure 31. Power Layer PCB Layout

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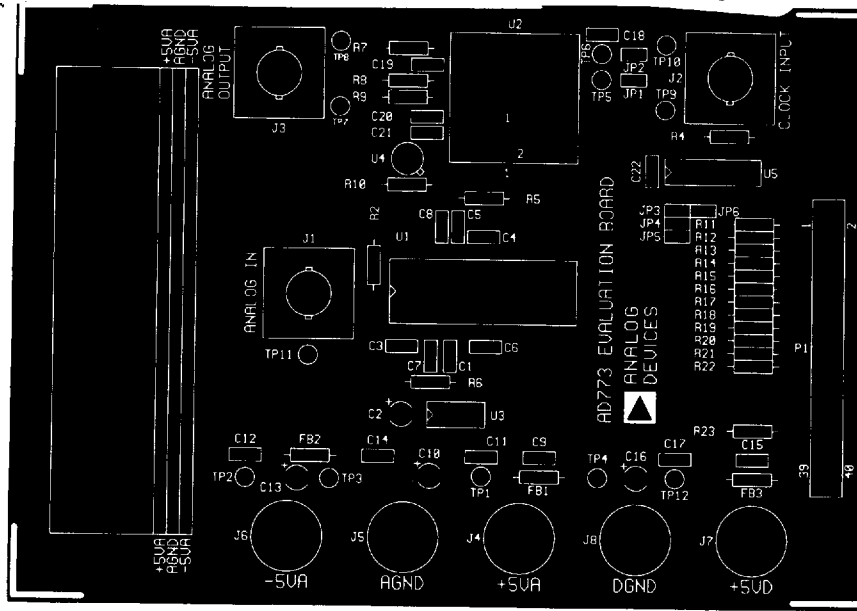


Figure 32. Silkscreen Layer PCB Layout