Multi-format Progressive Scan/HDTV Encoder with three 11-Bit DACs and Macrovision

Preliminary Technical Data **ADV7196**

INPUT FORMATS
- YCrCb in 2x10-Bit (4:2:2) or 3x10-Bit (4:4:4) format compliant to SMPTE-293M (525p), ITU-R.BT1358 (625p), SMPTE274M (1080i), SMPTE296M (720p) and any other High Definition standard using Async Timing Mode
- RGB in 3x10 Bit 4:4:4 format

OUTPUT FORMATS
- YPrPb Progressive Scan (EIA-770.1, EIA-770.2)
- YPrPb HDTV (EIA 770.3)
- RGB levels compliant to RS-170 and RS-343A

PROGRAMMABLE FEATURES
- Internal Testpattern Generator with Color Control
- Y/C delay (+/-)
- Gamma Correction
- Individual DAC on/off control
- 54MHz Output (2xOversampling)
- Sharpness filter with programmable gain/attenuation
- Programmable Adaptive Filter Control
- Undershoot Limiter
- VBI Open Control

Macrovision Rev 1.0 (525p)
CGMS-A (525p)
2 Wire Serial MPU Interface

Single Supply +5V/+3.3 V Operation
52-PQFP package

APPLICATIONS
- Progressive Scan / HDTV Display Devices
- DVD Players
- Progressive Scan/HDTV Projection Systems
- Digital Video Systems
- High Resolution Color Graphics
- Image Processing/ Instrumentation
- Digital Radio Modulation/ Video Signal Reconstruction

GENERAL DESCRIPTION

The ADV7196 is a triple high speed, digital-to-analog encoder on a single monolithic chip. It consists of three high speed video D/A converters with TTL compatible inputs.

The ADV7196 has three separate 10-Bit wide input ports which accept data in 4:4:4 10-Bit YCrCb or RGB or 4:2:2 10-Bit YCrCb. This data is accepted in progressive scan format at 27MHz or HDTV format at 74.25MHZ or 74.1758MHz. For any other High Definition standard but SMPTE 293M, ITU-R BT.1358, SMPTE274M or SMPTE296M the Async Timing Mode can be used to input data to the ADV7196. For all standards, external horizontal, vertical and blanking signals or EAV/SAV codes control the insertion of appropriate synchronisation signals into the digital data stream and therefore the output signals.

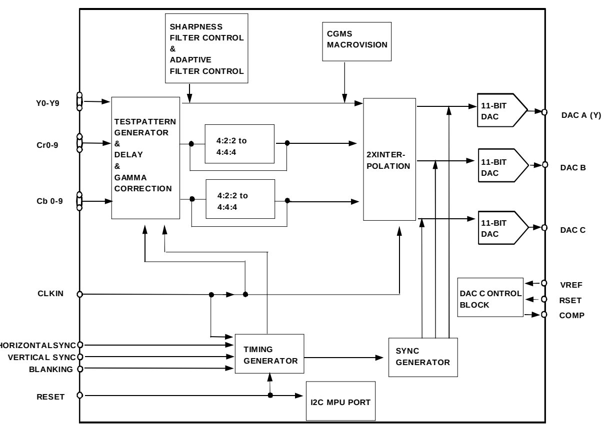
The ADV7196 outputs analog YPrPb progressive scan format complying to EIA770.1, EIA 770.2 or YPrPb HDTV complying to EIA 770.3 or RGB complying to RS-170/RS 343A.

The ADV7196 requires a single +5V/3.3V power supply, an optional external 1.235 V reference and a 27 MHz clock in Progressive Scan Mode or a 74.25MHz (or 74.1758MHz) clock in HDTV mode.

In Progressive Scan Mode, a Sharpness Filter with programmable gain allows high frequency enhancement on the luminance signal. Programmable Adaptive Filter Control which may be used, allows removal of ringing on the incoming Y data. The ADV7196 supports CGMS-A data control generation and the Macrovision Anticopy algorithm in 525p mode.

The ADV7196 is packaged in a 52-Pin PQFP package.

FUNCTIONAL BLOCK DIAGRAM



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5V SPECIFICATIONS

(V_{AA} = + 5V ± 5%, V_{REF} = 1.235 V, R_{SET} = 2470 Ω, R_{LOAD}=300 Ω. All specifications T_{MIN} to T_{MAX} (0 °C to 70°C) unless otherwise noted, Tj_{MAX} = 110°C.

Parameter	Min	Typ	Max	Units	Test Conditions[1]
STATIC PERFORMANCE					
Resolution (DAC A)		11		Bits	
Resolution (DAC B,C)		11		Bits	
Integral Nonlinearity DAC A[3]		1.3		LSB	
Differential Nonlinearity DAC A[3]		0.9		LSB	Guaranteed Monotonic
Integral Nonlinearity DAC B,C[3]		1.3		LSB	
Differential Nonlinearity DAC A[3]		0.9		LSB	Guaranteed Monotonic
DIGITAL OUTPUTS					
Output High Voltage, V_{OL}			0.4	V	
Output Low Voltage, V_{OH}	2.4			V	
Three State Leakage Current			0.05	μA	Vin = 0.4 V
Three State Output Capacitance		TBA		pF	
DIGITAL AND CONTROL INPUTS					
Input High Voltage, V_{IH}	2			V	
Input Low Voltage, V_{IL}			0.8	V	
Input Current, I_{IN}			TBA	μA	
Input Leakage Current			0.02	uA	Vin = 0.4V or 2.4V
Input Capacitance, C_{IN}		TBA		pF	
ANALOG OUTPUTS					
Output Current (DAC B, C)		2.66		mA	
Output Current (DAC A)		[illegible]		mA	
DAC to DAC Matching		[illegible]		%	DAC A,B,C
Output Compliance Range, V_{OC}		TBA		V	
Output Impedance, R_{OUT}		TBA		KΩ	
Output Capacitance, C_{OUT}		TBA		pF	I_{OUT} = 0 mA
VOLTAGE REFERENCE(Ext. and Int.)					
Reference Range, V_{REF}		1.235		V	
POWER REQUIREMENTS[4]					
Idd[1]		38		mA	1xInterpolation
Idd[1]		62		mA	2xInterpolation
Idd[1]		66		mA	HDTV mode
Iaa[2]		11.25		mA	1xInterpolation 2xInterpolation and HDTV mode
I_{PLL}		6.5		mA	1xInterpolation 2xInterpolation and HDTV mode
Power Supply Rejection Ratio		0.02		% / %	

Notes

1 Idd or the circuit current, is the continuous current required to drive the digital core without the I_{PLL}

2 Iaa is the total current required to supply all DACs including the Vref circuitry

3 Guraranteed by characterisation

4 All DACs on

Specifications subject to change without notice

3.3V SPECIFICATIONS[1]

(V_{AA} = + 3.3V ± 5%, V_{REF} = 1.235 V, R_{SET} = 2470 Ω, R_{LOAD}=300 Ω.
All specifications T_{MIN} to T_{MAX} (0 °C to 70°C) unless otherwise noted, Tj_{MAX} = 110°C.

Parameter	Min	Typ	Max	Units	Test Conditions
STATIC PERFORMANCE					
Resolution (DAC A)		11		Bits	
Resolution (DAC B,C)		11		Bits	
Integral Nonlinearity DAC A		1.3		LSB	
Differential Nonlinearity DAC A		0.9		LSB	
Integral Nonlinearity DAC B,C		1.3		LSB	
Differential Nonlinearity DAC B,C		0.9		LSB	
DIGITAL OUTPUTS					
Output High Voltage, V_{OL}		0.4		V	
Output Low Voltage, V_{OH}		2.4		V	
Three State Leakage Current			0.05	µA	Vin = 0.4 V
Three State Output Capacitance		TBA		pF	
DIGITAL AND CONTROL INPUTS					
Input High Voltage, V_{IH}		2		V	
Input Low Voltage, V_{IL}		0.8		V	
Input Current, I_{IN}			TBA	µA	
Input Leakage Current			0.0[illegible]	µA	Vin = 0.4 V or 2.4V
Input Capacitance, C_{IN}		TBA		pF	
ANALOG OUTPUTS					
Output Current		[illegible]		mA	
Output Current		4.33		mA	
DAC to DAC Matching		1.5		%	DAC A,B,C
Output Compliance Range, V_{OC}		TBA		V	
Output Impedance, R_{OUT}		TBA		KΩ	
Output Capacitance, C_{OUT}		TBA		pF	
VOLTAGE REFERENCE (Ext.)					
Reference Range, V_{REF}		1.235		V	
POWER REQUIREMENTS[4]					
Idd[2]		13		mA	1xInterpolation
Idd[2]		28		mA	2xInterpolation
Idd[2]		30		mA	HDTV mode
Iaa[3]		10.75		mA	1xInterpolation 2xInterpolation and HDTV mode
I_{PLL}		6.0		mA	1xInterpolation 2xInterpolation and HDTV mode
Power Supply Rejection Ratio		0.02		% / %	

Notes
1 Guaranteed by characteristation
2 Idd or the circuit current, is the continuous current required to drive the digital core without the I_{PLL}
3 Iaa is the total current required to supply all DACs including the Vref circuitry
4 All DACs on

Specifications subject to change without notice.

5V DYNAMIC-SPECIFICATIONS

(V_{AA} = + 5V ± 5%, V_{REF} = 1.235 V, R_{SET} = 2470 Ω, R_{LOAD}=300 Ω.
All specifications T_{MIN} to T_{MAX} (0 °C to 70°C) unless otherwise noted, Tj_{MAX} = 110°C.

Parameter	Min	Typ	Max	Units
Luma Bandwidth		TBA		MHz
Chroma Bandwidth		TBA		MHz
Signal to Noise Ratio		TBA		MHz
Chroma/Luma Delay Inequality		TBA		ns

3.3V DYNAMIC-SPECIFICATIONS

(V_{AA} = +3.3V ± 5%, V_{REF} = 1.235 V, R_{SET} = 2470 Ω, R_{LOAD}=300 Ω.
All specifications T_{MIN} to T_{MAX} (0 °C to 70°C) unless otherwise noted, Tj_{MAX} = 110°C.

Parameter	Min	Typ	Max	Units
Luma Bandwidth		TBA		MHz
Chroma Bandwidth		TBA		MHz
Signal to Noise Ratio		TBA		MHz
Chroma/Luma Delay Inequality		TBA		ns

5V TIMING–SPECIFICATIONS

(V_{AA} = + 5V ± 5%, V_{REF} = 1.235 V, R_{SET} = 2470 Ω, R_{LOAD}=300 Ω. All specifications T_{MIN} to T_{MAX} (0 °C to 70°C) unless otherwise noted, Tj_{MAX} = 110°C.

Parameter	Min	Typ	Max	Units	Condition
MPU PORT[1]					
SCLOCK Frequency	10		400	kHz	
SCLOCK High Pulse Width, t_1	0.6			µs	
SCLOCK Low Pulse Width, t_2	1.3			µs	
Hold Time (Start Condition), t_3	0.6			µs	After this period the 1st clock is generated
Setup Time (Start Condition), t_4	0.6			µs	Relevant for repeated Start Condition
Data Setup Time, t_5	100			ns	
SDATA, SCLOCK Rise Time, t_6			300	ns	
SDATA, SCLOCK Fall Time, t_7			300	ns	
Setup Time (Stop Condition) , t_8	0.6			µs	
ANALOG OUTPUTS[1]					
Analog Output Delay[2]			8	ns	
Analog Output Rise/Fall Time		TBA		ns	Analog
Output Transition Time		TBA		ns	Analog
Output Skew		0.5		ns	
CLOCK CONTROL AND PIXEL PORT					
f_{Clk}		27	MHz		
f_{Clk}		54	MHz		
f_{Clk}		74.25	MHz		
Clock High Time t_9		1.6		ns	
Clock Low Time t_{10}		1.6		ns	
Data Setup Time t_{11}		[illegible]		ns	
Data Hold Time t_{12}		[illegible]		ns	
Control Setup Time t_{11}		2.5		ns	
Control Hold Time t_{12}		2.0		ns	
Digital Output Access Time t_{13}		13		ns	
Digital Output Hold Time t_{14}		12		ns	
RESET Low Time[1]		1.6		ns	
Pipeline Delay [3]		16		Clock cycles	
Pipeline Delay [4]		29		Clock cycles	

Notes

1 Guaranteed by characterisation.
2 Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of DAC output full-scale transition.
3 For 4:4:4 pixel input format at 1xOversampling
4 For 4:4:4 pixel input format at 2xOversampling

Specifications subject to change without notice.

3.3V TIMING–SPECIFICATIONS[1]

(V_{AA} = +3.3V ± 5%, V_{REF} = 1.235 V, R_{SET} = 2470 Ω, R_{LOAD}=300 Ω. All specifications T_{MIN} to T_{MAX} (0 °C to 70°C) unless otherwise noted, Tj_{MAX} = 110°C.

Parameter	Min	Typ	Max	Units	Condition
MPU PORT					
SCLOCK Frequency	0		400	kHz	
SCLOCK High Pulse Width, t_1	0.6			µs	
SCLOCK Low Pulse Width, t_2	1.3			µs	
Hold Time (Start Condition), t_3	0.6			µs	After this period the 1st clock is generated
Setup Time (Start Condition), t_4	0.6			µs	Relevant for repeated Start Condition
Data Setup Time, t_5	100			ns	
SDATA, SCLOCK Rise Time, t_6			300	ns	
SDATA, SCLOCK Fall Time, t_7			300	ns	
Setup Time (Stop Condition) , t_8	0.6			µs	
ANALOG OUTPUTS					
Analog Output Delay[2]		8		ns	
Analog Output Rise/Fall Time		TBA		ns	Analog
Output Transition Time		TBA		ns	Analog
Output Skew		0.25		ns	
CLOCK CONTROL AND PIXEL PORT					
f_{Clk}		27		MHz	
f_{Clk}		54		MHz	
f_{Clk}		74.25		MHz	
Clock High Time t_9		1.5		ns	
Clock Low Time t_{10}		2.0		ns	
Data Setup Time t_{11}		0		ns	
Data Hold Time t_{12}		2.0		ns	
Control Setup Time t_{11}		3.5		ns	
Control Hold Time t_{12}		2.0		ns	
Digital Output Access Time t_{13}		15		ns	
Digital Output Hold Time t_{14}		1[illegible]		ns	
RESET Low Time		2.0		ns	
Pipeline Delay[3]		16		Clock cycles	
Pipeline Delay[4]		29		Clock cycles	

Notes

1 Guaranteed by characterisation.

2 Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of DAC output full-scale transition.

3 For 4:4:4 pixel input format at 1xOversampling

4 For 4:4:4 pixel input format at 2xOversampling

Specifications subject to change without notice.

ORDERING INFORMATION[1]

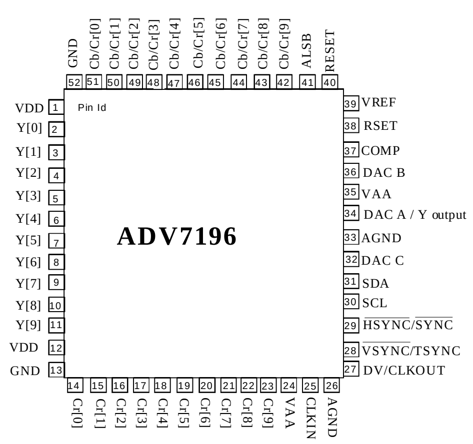
Package Description	Model	Package Option
Plastic Quad Flatpack	ADV7196KS	S-52

ABSOLUTE MAXIMUM RATINGS*

V_{AA} to GND...+7V
Voltage on any Digital Pin.............GND-0.5V to V_{AA}+0.5V
Ambient Operating Temperature (T_A)..........-40°C to +85°C
Storage Temperature (T_S).........................-65°C to +150°C
Junction Temperature (T_J)....................................+150°C
Lead Temperature (Soldering, 10 secs)....................300°C
Vapor Phase Soldering (1 minute))..........................220°C
I_{OUT} to GND[1]..0V to V_{AA}

NOTES
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[1]Analog Output Short Circuit to any Power Supply or Common can be of an indefinite duration.

PIN CONFIGURATION



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADV7127 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTIONS

Pin Mnemonic	Input/Output	Function
GND	G	Digital Ground
AGND	G	Analog Ground
ALSB	I	TTL Address Input. This signal sets up the LSB of the MPU address.
DV/CLKOUT	I/O	Video Blanking Control Signal Input or clock output signal.The clock output signal is only available in Progressive Scan Mode.
CLKIN	I	Pixel Clock Input. Requires a 27MHz reference clock for standard operation in Progressive Scan Mode or a 74.25MHz (74.1758MHz) reference clock in HDTV mode.
COMP	O	Compensation Pin for DACs. Connect 0.1µF Capacitor from COMP pin to V_{AA}.
DAC A	O	Y analog output.
DAC B	O	Color component analog output of input data on Cr 9-0 input pins.
DAC C	O	Color component analog output of input data on Cb/Cr 9-0 input pins.
$\overline{HSYNC}$/ $\overline{SYNC}$	I	$\overline{HSYNC}$, horizontal sync control signal input or $\overline{SYNC}$ input control signal in Async Timing Mode.
Cr 9-0	I	10-Bit Progressive scan/ HDTV input port for color data in 4:4:4 input mode. In 4:2:2 mode this input port is not used. Input port for R data when RGB data is input.
Cb/Cr 9-0	I	10-Bit Progressive scan/ HDTV input port for color data. In 4:2:2 mode the multiplexed CrCb data must be input on these pins. Input port for B data when RGB is input.
$\overline{RESET}$	I	This input resets the on chip timing generator and sets the ADV7196 into Default Register setting. Reset is an active low signal.
R_{SET}	I	A 2470 Ohm resistor (for input ranges 64-940 and 64-960, output standards EIA770.1-3)must be connected from this pin to AGND and is used to control the amplitudes of the DAC outputs. For input ranges 0 -1023 (RS-170,RS-343A) the R_{SET} value must be 2820 Ohms.
SCL	I	MPU Port Serial Interface Clock Input
SDA	I/O	MPU Port Serial Data Input/Output
$\overline{VSYNC}$/ TSYNC	I	$\overline{VSYNC}$, vertical sync control signal input or TSYNC input control signal in AsyncTiming Mode.
V_{DD}	P	Digital power supply
V_{AA}	P	Analog power supply
V_{REF}	I/O	Optional External Voltage Reference Input for DACs or Voltage Reference Output (1.235V).
Y9 -Y0	I	10-Bit Progressive scan/ HDTV input port for Y data. Input for G data when RGB data is input.

FUNCTIONAL DESCRIPTION

Digital Inputs

The digital inputs of the ADV7196 are TTL compatible. 30-Bit YCrCb or RGB pixel data in 4:4:4 format or 20-Bit YCrCb pixel data in 4:2:2 format is latched into the device on the rising edge of each clock cycle at 27 MHz in Progressive Scan mode, or 74.25MHz or 74.1785 in HDTV mode. It is also possible to input 3x10 Bit RGB data in 4:4:4 format to the ADV7196.

Control Signals

The ADV7196 accepts sync control signals accompanied by valid 4:2:2 or 4:4:4 data. These external horizontal, vertical and blanking pulses (or EAV/SAV codes) control the insertion of approriate sync information into the output signals.

Analog Outputs

The analog Y signal is output on DACs A, the color component analog signals on DAC B and DAC C conforming to EIA-770.1 or EIA 770.2 standards in PS mode or EIA-770.3 in HDTV mode. Rset has a value of 2470 Ohms (EIA-770.1, EIA-770.2, EIA 770.3), Rload has a value of 300Ohms. For RGB outputs conforming to RS-170/RS343A output standards Rset must have a value of 2820Ohms.

Undershoot Limiter

A limiter can be applied to the Y data before it is applied to the DACs. Available limit values are -1.5 IRE, -6IRE, -11IRE below blanking. This functionality is available in Progressive Scan mode only.

Internal Test Pattern Generator

The ADV7196 can generate a Cross Hatch pattern (white lines against a black background). Additionally the ADV7196 can output a uniform color pattern. The color of the lines or uniform field/frame can be programmed by the user.

Y/ CrCb delay

The Y output and the color component outputs can be delayed wrt the falling edge of the horizontal sync signal by up to 4 clock cycles.

Gamma Correction

Gamma correction may be performed on the luma data. The user has the choice to use either of two different gamma curves, A or B. At any one time one of these curves is operational if gamma corrrection is enabled. Gamma correction allows the mapping of the luma data to a user-defined function.

54MHz operation

In Progressive Scan mode, it is possible to operate the three output DACs at 54MHz or 27MHz. The ADV7196 is supplied with a 27MHz clock synced with the incoming data. If required, a second stage interpolation filter interpolates the data to 54MHz before it is applied to the 3 output DACs.

PROGRAMMABLE SHARPNESS FILTER

Sharpness Filter Mode is applicable to the Y data only in Progressive Scan mode.
The desired frequency response can be chosen by the user in programming the correct value via the I^2C.
The variation of frequency responses can be seen in the figures on the following pages.

PROGRAMMABLE ADAPTIVE FILTER CONTROL

If the Adaptive Filter Mode is enabled (Progressive Scan mode only) it is possible to compensate for large edge transitions on the incoming Y data. Sensitivity and attenuation are all programmable over the I2C. For further information refer to Sharpness Filter Control and Adaptive Filter Control section.

MPU PORT DESCRIPTION.

The ADV7196 support a two wire serial (I^2C compatible) microprocessor bus driving multiple peripherals. Two inputs Serial Data (SDA) and Serial Clock (SCL) carry information between any device connected to the bus. Each slave device is recognized by a unique address. The ADV7196 has four possible slave addresses for both read and write operations. These are unique addresses for each device and are illustrated in Figure xx. The LSB sets either a read or write operation. Logic level "1" corresponds to a read operation while logic level "0" corresponds to a write operation. A1 is set by setting the ALSB pin of the ADV7196 to logic level "0" or logic level "1". When ALSB is set to "0", there is greater input bandwidth on the I2C lines, which allows high speed data transfers on this bus. When ALSB is set to "1", there is reduced input bandwidth on the I2C lines, which means that pulses of less than 50ns will not pass into the I2C internal controller. This mode is recommended for noisy systems.

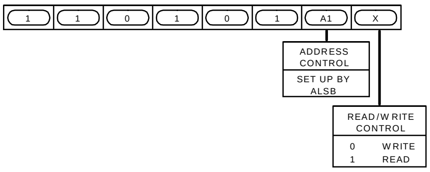


Fig xx. ADV7196 Slave Address

To control the various devices on the bus, the following protocol must be followed. First the master initiates a data transfer by establishing a Start condition, defined by a high to low transition on SDA whilst SCL remains high. This indicates that an address/data stream will follow. All peripherals respond to the Start condition and shift the next eight bits (7-Bit address + R/$\overline{W}$ bit). The bits are tranferred from MSB down to LSB. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as an acknowledge bit. All other devices withdraw from the bus at this point and maintain an idle condition. The idle condition is where the device monitors the SDA and SCL lines waiting for the Start condition and the correct transmitted address. The R/$\overline{W}$ bit determines the direction of the data.

A logic "0" on the LSB of the first byte means that the master will write information to the peripheral. A logic "1" on the LSB of the first byte means that the master will read information from the peripheral.

The ADV7196 acts as a standard slave device on the bus. The data on the SDA pin is 8 bits long supporting the 7-Bit addresses plus the R/$\overline{W}$ bit. It interprets the first byte as the device address and the second byte as the starting subaddress. The subaddresses auto-increment allowing data to be written to or read from from the starting subaddress. A data transfer is always terminated by a Stop condition. The user can also access any unique subaddress register on a one by one basis without having to update all the registers.

Stop and Start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, then these cause an immediate jump to the idle condition. During a given SCL high period the user should only issue one Start condition, one Stop condition or a single Stop condition followed by a single Start condition. If an invalid subaddress is issued by the user, the ADV7196 will not issue an acknowledge and will return to the idle condition. If in auto-increment mode, the user exceeds the highest subaddress then the following action will be taken:

1. In Read Mode, the highest subaddress register contents will continue to be output until the master device issues a no-acknowledge. This indicates the end of a read. A no-acknowledge condition is where the SDA line is not pulled low on the ninth pulse.

2. In Write Mode, the data for the invalid byte will be not be loaded into any subaddress register, a no-acknowledge will be issued by the ADV7196 and the part will return to the idle condition.

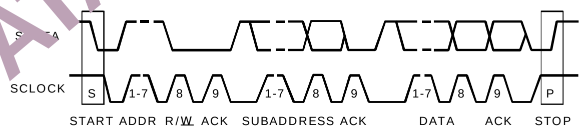


Figure xx. Bus Data Transfer

Figure 50 illustrates an example of data transfer for a read sequence and the Start and Stop conditions.

Figure 51 shows bus write and read sequences.

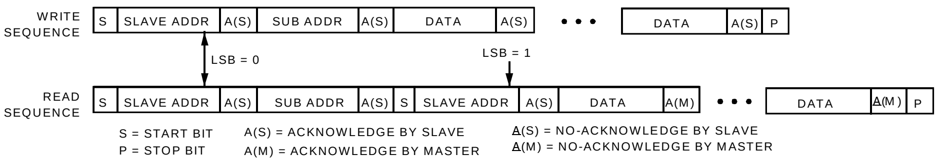


Figure xx. Write and Read Sequence

REGISTER ACCESSES

The MPU can write to or read from all of the registers of the ADV7196 except the Subaddress Registers which are write only registers. The Subaddress Register determines which register the next read or write operation accesses. All communications with the part through the bus start with an access to the Subaddress Register. Then a read/ write operation is performed from/to the target address which then increments to the next address until a Stop command on the bus is performed.

REGISTER PROGRAMMING

The following section describes the functionality of each register. All registers can be read from as well as written to unless otherwise stated.

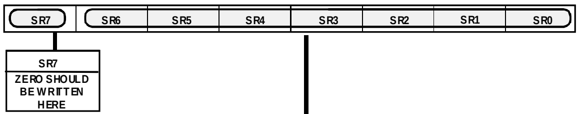
Subaddress Register (SR7-SR0)

The Communications Register is an eight bit write-only register. After the part has been accessed over the bus and a read/write operation is selected, the subaddress is set up. The Subaddress Register determines to/from which register the operation takes place.

Figure xx shows the various operations under the control of the Subaddress Register. "0" should always be written to SR7.

Register Select (SR6-SR0):

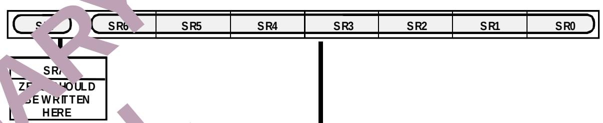
These bits are set up to point to the required starting address.



ADV7196 SUBADRESS REGISTER

Address	SR6	SR5	SR4	SR3	SR2	SR1	SR0	
00h	0	0	0	0	0	0	0	MODE REGISTER 0
01h	0	0	0	0	0	0	1	MODE REGISTER 1
02h	0	0	0	0	0	1	0	MODE REGISTER 2
03h	0	0	0	0	0	1	1	MODE REGISTER 3
04h	0	0	0	0	1	0	0	MODE REGISTER 4
05h	0	0	0	0	1	0	1	MODE REGISTER 5
06h	0	0	0	0	1	1	0	COLOR Y
07h	0	0	0	0	1	1	1	COLOR CR
08h	0	0	0	1	0	0	0	COLOR CB
09h	0	0	0	1	0	0	1	RESERVED
0Ah	0	0	0	1	0	1	0	RESERVED
0Bh	0	0	0	1	0	1	1	RESERVED
0Ch	0	0	0	1	1	0	0	RESERVED
0Dh	0	0	0	1	1	0	1	RESERVED
0Eh	0	0	0	1	1	1	0	RESERVED
0Fh	0	0	0	1	1	1	1	RESERVED
10h	0	0	1	0	0	0	0	FILTER GAIN
11h	0	0	1	0	0	0	1	CGMS DATA REGISTER 0
12h	0	0	1	0	0	1	0	CGMS DATA REGISTER 1
13h	0	0	1	0	0	1	1	CGMS DATA REGISTER 2
14h	0	0	1	0	1	0	0	GAMMA CORRECTION REGISTER 0
15h	0	0	1	0	1	0	1	GAMMA CORRECTION REGISTER 1
16h	0	0	1	0	1	1	0	GAMMA CORRECTION REGISTER 2
17h	0	0	1	0	1	1	1	GAMMA CORRECTION REGISTER 3
18h	0	0	1	1	0	0	0	GAMMA CORRECTION REGISTER 4
19h	0	0	1	1	0	0	1	GAMMA CORRECTION REGISTER 5
1Ah	0	0	1	1	0	1	0	GAMMA CORRECTION REGISTER 6
1Bh	0	0	1	1	0	1	1	GAMMA CORRECTION REGISTER 7
1Ch	0	0	1	1	1	0	0	GAMMA CORRECTION REGISTER 8
1Dh	0	0	1	1	1	0	1	GAMMA CORRECTION REGISTER 9
1Eh	0	0	1	1	1	1	0	GAMMA CORRECTION REGISTER 10
1Fh	0	0	1	1	1	1	1	GAMMA CORRECTION REGISTER 11
20h	0	1	0	0	0	0	0	GAMMA CORRECTION REGISTER 12
21h	0	1	0	0	0	0	1	GAMMA CORRECTION REGISTER 13
22h	0	1	0	0	0	1	0	ADAPTIVE FILTER GAIN 1
23h	0	1	0	0	0	1	1	ADAPTIVE FILTER GAIN 2
24h	0	1	0	0	1	0	0	ADAPTIVE FILTER GAIN 3
25h	0	1	0	0	1	0	1	ADAPTIVE FILTER THRESHOLD A
26h	0	1	0	0	1	1	0	ADAPTIVE FILTER THRESHOLD B
27h	0	1	0	0	1	1	1	ADAPTIVE FILTER THRESHOLD C

Fig xx. ADV7196 Subaddress Registers in Progressive Scan Mode



ADV7196 SUBADRESS REGISTER

Address	SR6	SR5	SR4	SR3	SR2	SR1	SR0	
00h	0	0	0	0	0	0	0	MODE REGISTER 0
01h	0	0	0	0	0	0	1	MODE REGISTER 1
02h	0	0	0	0	0	1	0	MODE REGISTER 2
03h	0	0	0	0	0	1	1	MODE REGISTER 3
04h	0	0	0	0	1	0	0	MODE REGISTER 4
05h	0	0	0	0	1	0	1	MODE REGISTER 5
06h	0	0	0	0	1	1	0	COLOR Y
07h	0	0	0	0	1	1	1	COLOR CR
08h	0	0	0	1	0	0	0	COLOR CB

Fig xx. ADV7196 Subaddress Registers in HDTV Mode

PROGRESSIVE SCAN MODE

PROGRESSIVE SCAN MODE

MODE REGISTER 0

MR0 (MR07-MR00)
(Address (SR4-SR0) = 00H)

Figure xx shows the various operations under the control of Mode Register 0.

MR0 BIT DESCRIPTION

Output Standard Selection (MR00-MR01):
These bits are used to select the output levels for the ADV7196.
If EIA-770.2 (MR01-00='00') is selected the output levels will be: 0mV for blanking level, 700mV for peak white for the Y channel, +/- 350 mV for Pr, Pb outputs and -300mV for Sync. Sync insertion on the Pr, Pb channels is optional.

If EIA-770.1 (MR01-00="01') is selected the output levels will be: 0mV for blanking level, 714mV for peak white for the Y channel, +/- 350 mV for Pr, Pb outputs and -286mV for Sync.Optional sync insertion on the Pr, Pb channels is not possible.

If Full I/P Range (MR01-00='10') is selected the output levels will be:0mV for blanking level, 700mV for peak white for the Y channel, +/- 350 mV for Pr, Pb outputs and -300mV for Sync. Sync insertion on the Pr, Pb channels is optional.This mode is used for RS-170, RS-343A standard output compatibility. Refer to Appendix for output level plots.

Input Control Signals (MR02-MR03):
These control bits are used to select whether data is input with external horizontal, vertical and blanking sync signals or if the data is input with embedded EAV/SAV codes.
An Asynchronous timing mode is also available using TSYNC, $\overline{SYNC}$ and DV as input control signals.These control signals have to be programmed by the user.

The figure on the next page shows an example of how to program the ADV7196 to accept a different high definition standard but SMPTE293M, SMPTE274M, SMPTE296M or ITU-R.BT1358 standard.

Input Standard (MR04):

Select between 525p progressive scan input or 625p progressive scan input .

Reserved (MR05):
A '0' must be written to this bit.

DV polarity (MR06):
This control bit allows to select the polarity of the DV input control signal to be either active high or active low.This is in order to facilitate interfacing from I to P Converters which use an active low blanking signal output.

Macrovision (MR07):
To enable Macrovision this bit must be set to '1'.

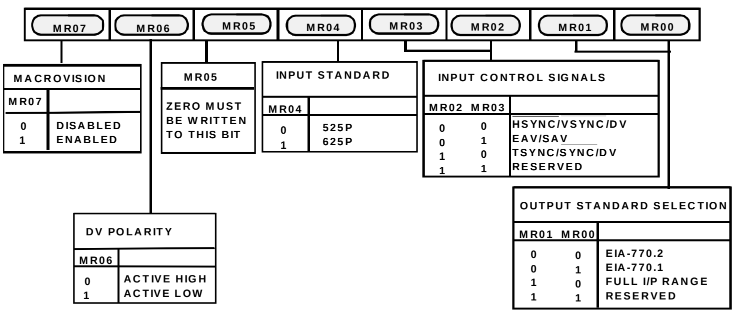


Figure xx: Mode Register 0

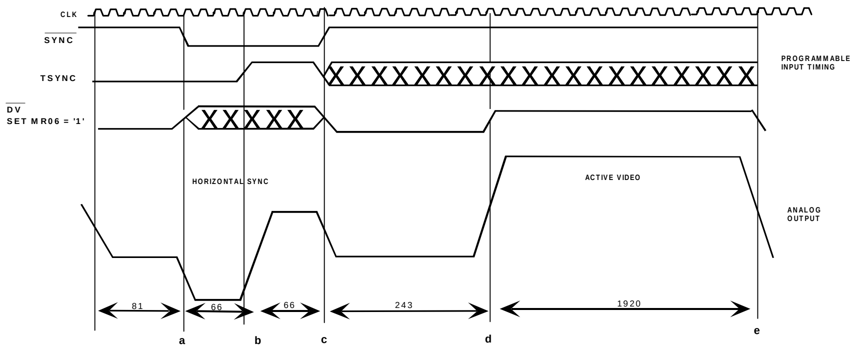


Figure xx: Async Timing Mode - Programming Input Control signals for SMPTE295M compatibility

The truth table below must be followed when programming the control signals in Async Timing Mode.

$\overline{SYNC}$	TSYNC	DV	
1 -> 0	0	0 or 1	50% point of falling edge of tri-level horizontal sync signal, a
0	0 -> 1	0 or 1	25% point of rising edge of tri-level horizontal sync signal, b
0 -> 1	0 or 1	0	50% point of falling edge of tri-level horizontal sync signal, c
1	0 or 1	0 -> 1	50% start of active video, d
1	0 or 1	1 -> 0	50% end of active video, e

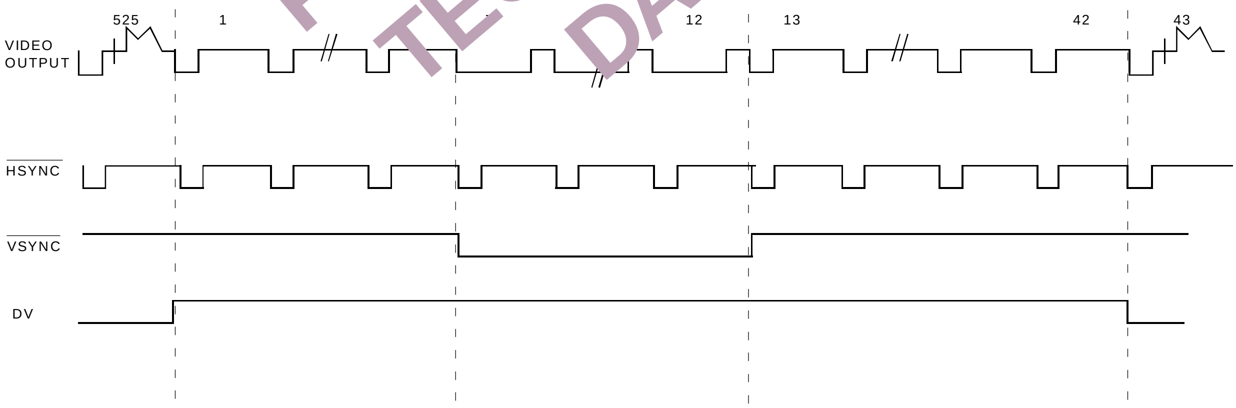


Figure xx: DV input control signal in relation to video output signal

MODE REGISTER 1
MR1 (MR17-MR10)
(Address (SR4-SR0) = 01H)

Figure xx shows the various operations under the control of Mode Register 1.

MR1 BIT DESCRIPTION

Pixel Data Enable (MR10):
When this bit is set to "0", the pixel data input to the ADV7196 is blanked such that a black screen is output from the DACs. When this bit is set to "1", pixel data is accepted at the input pins and the ADV7196 outputs the standard set in "Output Standard Selection" (MR01-00).

Input Format (MR11):
It is possible to input data in 4:2:2 format or at 4:4:4 format at 27MHz.

Testpattern Enable (MR12):
Enables or disables the internal test pattern generator.

Testpattern Hatch/Frame (MR13):
If this bit is set to '0', a cross hatch test pattern is output from the ADV7196 (for example, in SMPTE293M 11horizontal and 11vertical white lines, 4pixels wide are displayed against a black background). The cross hatch test pattern can be used to test monitor convergence.
If this bit is set to '1', a uniform colored frame/field test pattern is output from the ADV7196.

The color of the lines or the frame/field is by default white but can be programmed to be any color using the Color Y, Color Cr, Color Cb registers.

VBI open (MR14):
This bit enables or disables the facility of VBI data insertion during the Vertical Blanking Interval.
For this purpose lines 13 to 42 of each frame can be used for VBI when SMPTE293M standard is used, or lines 6 to 43 when ITU-R.BT1358 standard is used.

Undershoot Limiter (MR15 -MR16):
This control limits the Y signal to a programmable level in the active video region.
Available limit levels are - 1.5 IRE, -6 IRE, -11 IRE.

Note that this facility is only available when Interpolation is enabled (MR36="1").

Sharpness Filter (MR17):
This control bit enables or disables the Sharpness Filter mode. This bit must be set to "1" for any values programmed into the Filter Gain Register to take effect. It must also be set to "1" when Adaptive Filter mode is used. Refer to Sharpness Filter control and Adaptive Filter control section.

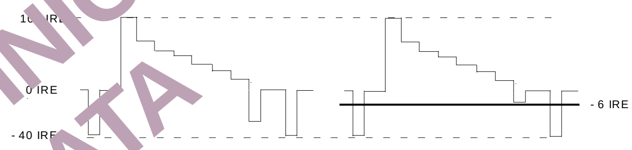


Figure xx Undershoot Limiter , programmed to -6 IRE

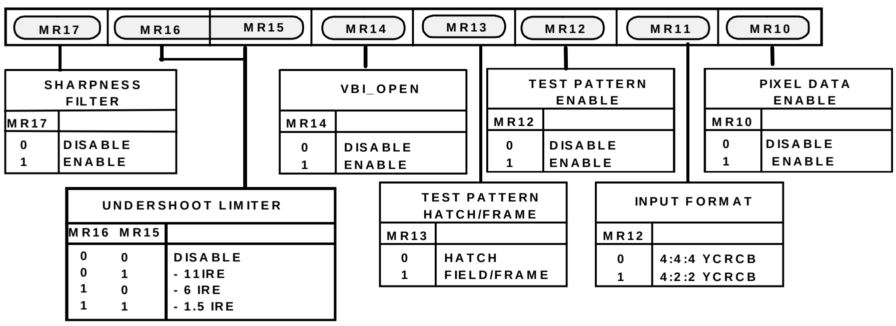


Figure xx: Mode Register 1

MODE REGISTER 2
MR1 (MR27-MR20)
(Address (SR4-SR0) = 02H)

Figure xx shows the various operations under the control of Mode Register 2.

MR2 BIT DESCRIPTION

Y Delay (MR20-22):
This control bit delays the Y signal with respect to the falling edge of the horizontal sync signal by up to 4 pixel clock cycles. Figure xx demonstrates this facility.

Color Delay (MR23-25):
This control allows to delay the color signals with respect to the falling edge of the horizontal sync signal by up to 4 pixel clock cycles. Figure xx demonstrates this facility.

CGMS Enable (MR26):
When this bit is set to "1" CGMS data is inserted on line 41 in 525p mode. The CGMS conforms to:

'CGMS-A EIA-J CPR1204-1, Transfer Method of Video ID information using vertical blanking interval (525p System), March 1998' and IEC61880, 1998, Video systems (525/60) - video and accompanied data using the vertical blanking interval - analogue interface.

The CGMS data bits are programmed into the CGMS Data Registers 0-2. For more information refer to CGMS Data Registers Section.

CGMS CRC (MR27):
This bit enables the automatic Cyclic Redundancy Check when CGMS is enabled.

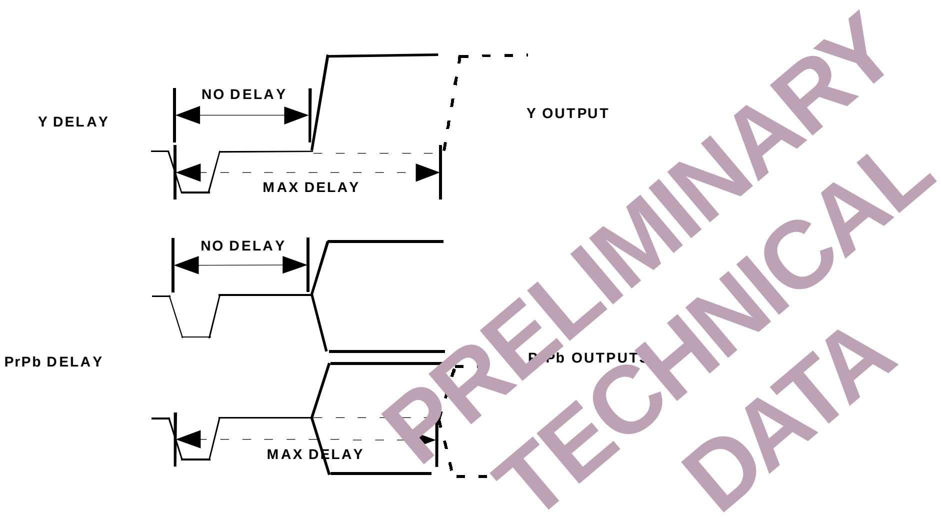


Fig xx. Y and Color Delay

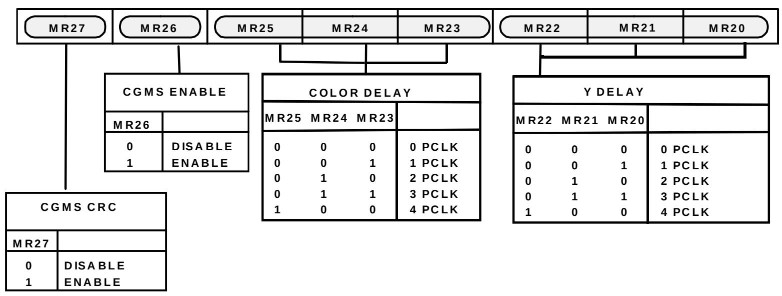


Figure xx: Mode Register 2

MODE REGISTER 3
MR3 (MR37-MR30)
(Address (SR4-SR0) = 03H)

Figure xx shows the various operations under the control of Mode Register 3.

MR3 BIT DESCRIPTION

HDTV Enable (MR30):
When this bit is set to '1' the ADV7196 reverts to HDTV mode (refer to HDTV mode section). When set to '0' the ADV7196 is set up in Progressive Scan Mode (PS mode).

Clkout Enable (MR31):
When this control is enabled (MR31="1"), the DV/CLKOUT pin functions as a clock output pin. In default setting (MR31="0") this pin is an input pin and accepts blank input signals.

Reserved(MR32):
A "0" must be written to this bit.

DAC A Control (MR33):
Setting this bit to "1" enables DAC A , otherwise this DAC is powered down.

DAC B Control (MR34):
Setting this bit to "1" enables DAC B , otherwise this DAC is powered down.

DAC C Control (MR35):
Setting this bit to "1" enables DAC C , otherwise this DAC is powered down.

Interpolation (MR36):
This bit enables the second stage interpolation filters. When this bit is enabled (MR36="1") data is send at 54MHz to the DAC output stage. After Reset it is recommended to toggle this bit
Before toggling this bit 1Ehex must be written to address 09hex. At 3.3V operation this values must be 3Ehex.

Reserved(MR37):
A zero must be written to this bit.

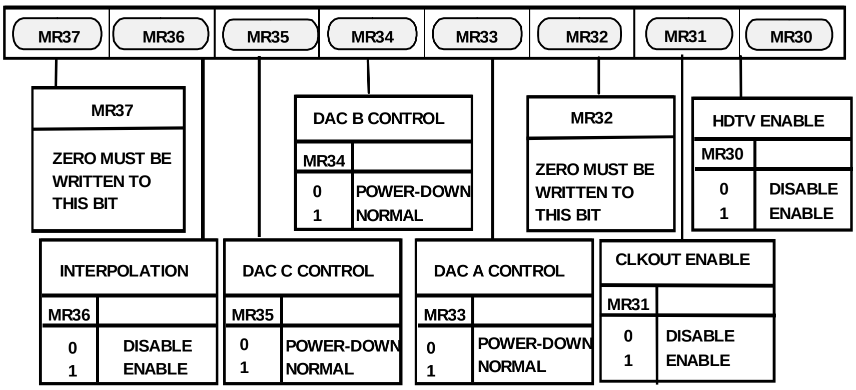


Figure xx. Mode Register 3

MODE REGISTER 4
MR4 (MR47-MR40)
(Address (SR4-SR0) = 04H)

Figure xx shows the various operations under the control of Mode Register 4.

MR4 BIT DESCRIPTION
Timing Reset (MR40):
Toggling MR40 from low to high and low again resets the internal horizontal and vertical timing counters.

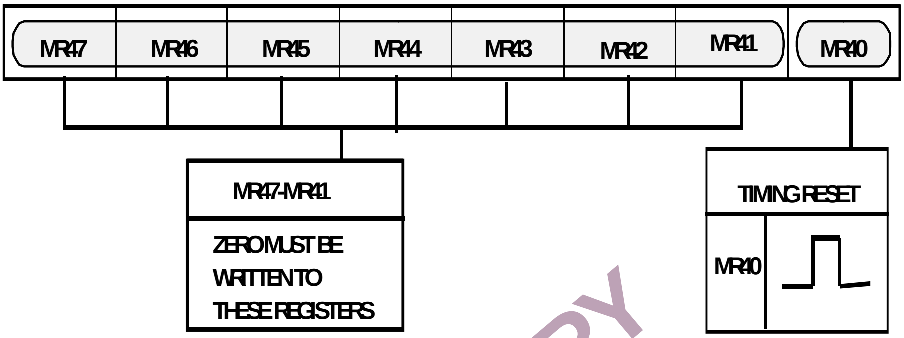


Figure xx. Mode Register 4

MODE REGISTER 5
MR5 (MR57-MR50)
(Address (SR4-SR0) = 05H)

Figure xx shows the various operations under the control of Mode Register 5.

MR5 BIT DESCRIPTION

Reserved (MR50):
This bit is reserved for the revision code.

RGB Mode (MR51):
When RGB mode is enabled (MR51="1") the ADV7196 accepts unsigned binary RGB data at its input port. This control is also available in Async Timing Mode.

Sync on PrPb (MR52):
By default the color component output signals Pr, Pb do not contain any horizontal sync pulses. They can be inserted when MR52="1". This facility is only available when Output Standard Selection has been set to EIA-770.2 (MR01-00 = "00") or Full Input Range (MR01-00= "10").
This control is not available in RGB mode.

Color data input on pins:	MR53	Analog Output signal:
In 4:4:4 input mode		
Cr 9-0	0	Dac B
Cb/Cr 9-0	0	Dac C
Cr 9-0	1	Dac C
Cb/Cr 9-0	1	Dac B
In 4:2:2 input mode		
Cr 9-0	0 or 1	not operational
Cb/Cr 9-0	0	Dac B (Pb)
Cb/Cr 9-0	1	Dac C (Pr)

Table xx Relationship between color input pixel port, MR53 and DAC B, DAC C outputs

Color Output Swap (MR53):
By default DAC B is configured as the Pr output and DAC C as the Pb output. In setting this bit to "1" the DAC outputs can be swapped around so that DAC B outputs Pb and DAC C outputs Pr. The table below demonstrates this in more detail. This control is also available in RGB mode.

Gamma Curve (MR54):
This bit selects which of the two programmable gamma curves is to be used. When setting MR54 to "0", the gamma correction curve selected is curve A. Otherwise curve B is selected. Each curve will have to be programmed by the user as explained in the Gamma Correction Registers section.

Gamma Corrrection (MR55):
To enable Gamma Correction and therefore activate the gamma curve programmed by the user, this bit must be set to "1". Otherwise the programmable Gamma Correction facility is bypassed. Programming of the gamma correction curves is explained in the Gamma Correction Registers section.

Adaptive Mode Control (MR56):
For this control to be effective, Adaptive Filter Control must be enabled (MR57="1") as well as the Sharpness Filter (MR17="1"). For Filter plots refer to Sharpness Filter Control and Adaptive Filter Control section.

Adaptive Filter Control (MR57):
This bit enables the Adaptive Filter Control when set to "1". Sharpness Filter must be enabled as well (MR17="1"). The Adaptive Filter Controls is explained in more detail under Sharpness Filter Control and Adaptive Filter Control section.

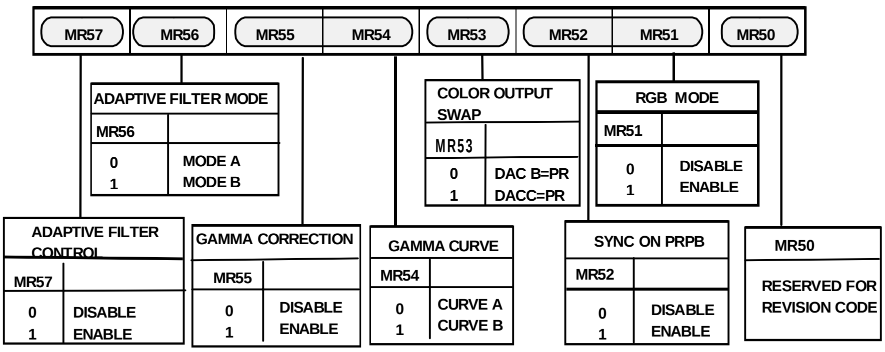


Figure xx. Mode Register 5

COLOR Y
CY (CY7-CY0)
(Address (SR4-SR0) = 06H)
COLOR CR
CCR (CCR7-CCR0)
(Address (SR4-SR0) = 07H)
COLOR CB
CCB (CCB7-CCB0)
(Address (SR4-SR0) = 08H)

These three 8-Bit wide registers are used to program the output color of the internal testpattern generator, be it the lines of the cross hatch pattern or the uniform field testpattern and are available in PS mode and HDTV mode. The standard used for the values for Y and the color difference signals to obtain white, black and the saturated primary and complementary colors conforms to the ITU-R BT 601-4 standard.
The table below shows sample color values to be programmed into the color registers when Output Standard Selection is set to EIA 770.2 (MR01-00 = "00").

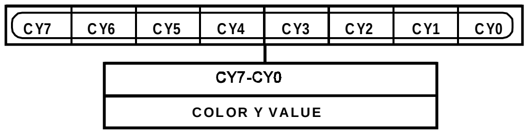


Figure xx. Color Y Register

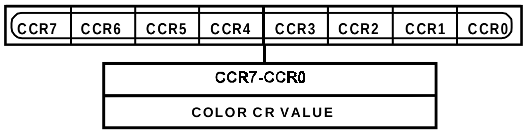


Figure xx. Color Cr Register

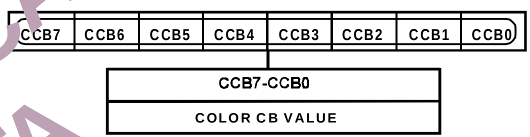


Figure xx. Color Cb Register

SAMPLE COLOR	COLOR Y VALUE	COLOR CR VALUE	COLOR CB VALUE
WHITE	235 (EB)	128 (80)	128 (80)
BLACK	16 (10)	128 (80)	128 (80)
RED	81 (51)	240 (F0)	90 (5A)
GREEN	145 (91)	34 (22)	54 (36)
BLUE	41 (29)	110 (6E)	240 (F0)
YELLOW	210 (D2)	146 (92)	16 (10)
CYAN	170 (AA)	16 (10)	166 (A6)
MAGENTA	106 (6A)	222 (DE)	202 (CA)

Figure xx Sample color values for EIA770.2 Output Standard Selection

FILTER GAIN
FG (FG7-FG0)
(Address (SR4-SR0) = 10H)

Figure xx shows the various operations under the control of the Filter Gain register.

In Sharpness Filter mode this control allows the filter coefficients to be changed so that the overall luma response can be varied. In this mode Filter A (BPF) and Filter B (LPF) are cascaded and therefore 256 possible responses can be chosen from.

FG BIT DESCRIPTION
Filter Gain A (FG3-FG0):
These bits are used to program the gain A value, which varies from response -8 to response +7 and are applied to Filter A.
Filter Gain B (FG4-FG7):
These bits are used to program the gain B value, which varies from response -8 to response +7 and are applied to Filter B.

Refer to Sharpness Filter Control and Adaptive Filter control section for more detail.

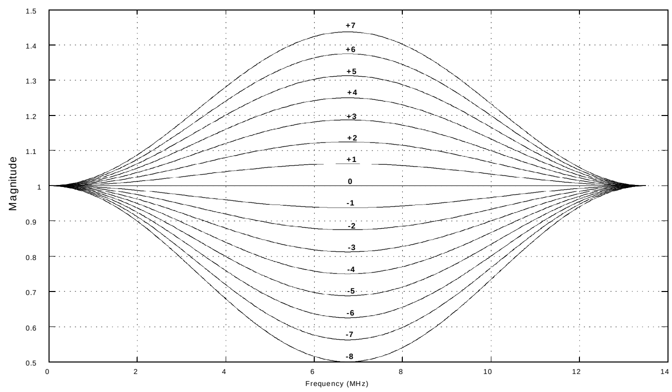


Figure xx Filter A Response

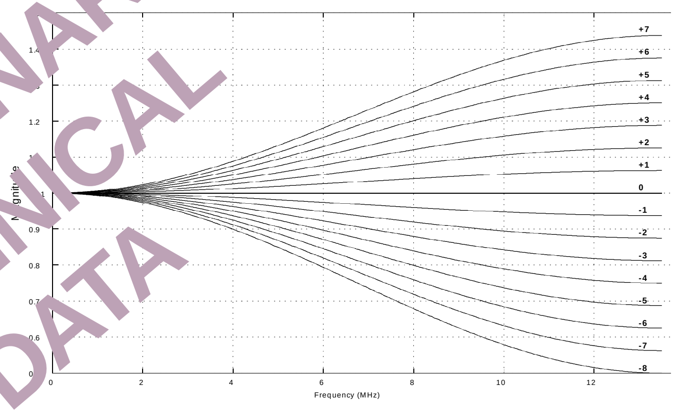


Figure xx Filter B Response

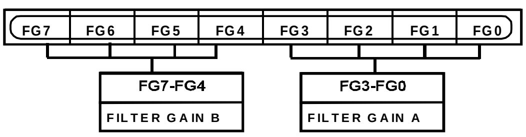


Figure xx. Filter Gain Register

CGMS DATA REGISTERS 2-0

CGMS2 (CGMS27-CGMS20)
(Address (SR4-SR0) = 13H)
This 8-bit wide register contains the first 4 CGMS data bits, Bit 1 to Bit 4 (C0-C3) of the CGMS data stream.

CGMS1 (CGMS17-CGMS10)
(Address (SR4-SR0) = 12H)
This 8-bit wide register contains Bit 5 to Bit 12 (C4-C11) of the CGMS data stream.

CGMS0 (CGMS07-CGMS00)
(Address (SR4-SR0) = 11H)
This 8-bit wide register contains the last 8 CGMS data bits, Bit 13 to Bit 20 (C12-C19) of the CGMS data stream.

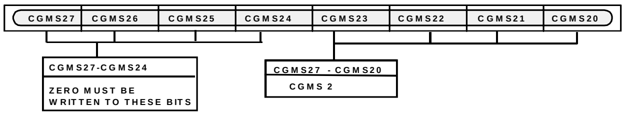


Figure xx. CGMS 2 Data Register

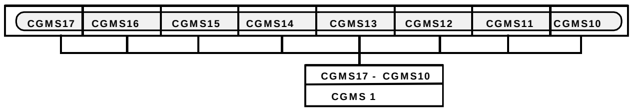


Figure xx. CGMS 1 Data Register

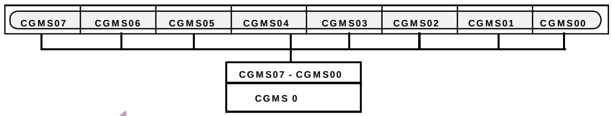


Figure xx. CGMS 0 Data Register

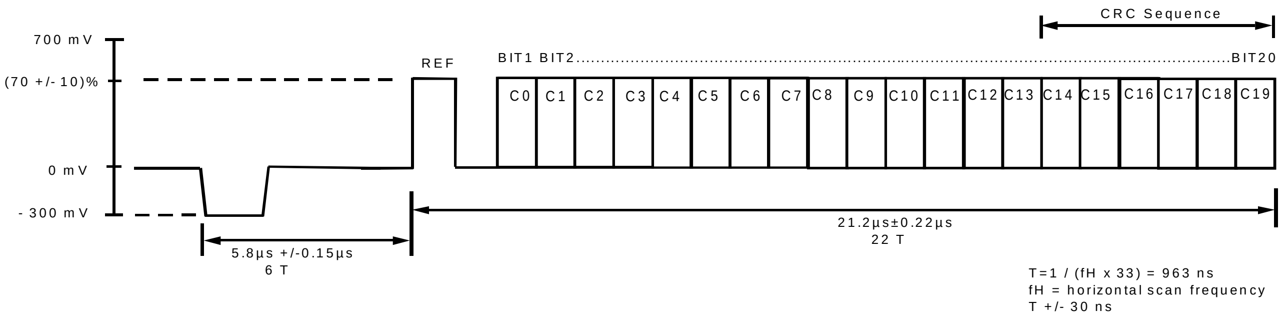


Fig xx. CGMS Waveform

GAMMA CORRECTION REGISTERS 0- 13
(GAMMA CORRECTION 0-13)
(Address (SR5-SR0) = 14H -21H)

The Gamma Correction Registers are fourteen 8-bit wide register. They are used to program the gamma correction curves A and B.
Generally gamma correction is applied to compensate for the non linear relationship between signal input and brightness level output (as perceived on the CRT). It can also be applied wherever non-linear processing is used.

Gamma correction uses the function :

$$Signal_{OUT} = (Signal_{IN})^{\gamma}$$

where γ = gamma power factor

Gamma correction is performed on the luma data only.
The user has the choice to use two different curves, curve A or curve B. At any one time only one of these curves can be used.
The response of the curve is programmed at 7 predefined locations. In changing the values at these locations the gamma curve can be modified. Between these points linear interpolation is used to generate intermediate values. Considering the curve to have a total length of 256 points, the seven locations are at 32, 64, 96, 128, 160, 192, 224.

Location 0, 16, 240 and 255 are fixed and can not be changed.

For the length of 16 to 240 the gamma correction curve has to be calculated as below:

$$y = x^{\gamma}$$

where y = gamma corrected output
x = linear input signal
γ = gamma power factor

To program the gamma correction registers, the 7 values for y have to be calculated using the following formulare:

$$y_n = [\, x_{(n-16)} / (240 - 16)\,]^{\gamma} \times (240-16) + 16$$

where
$x_{(n-16)}$ = Value for x along x-axis at points n = 32, 64, 96, 128, 160, 192 or 224
y_n = Value for y along the y-axis, which has to be written into the gamma correction register .

EXAMPLE:

$y_{32} = [\,(16 / 224)^{0.5} \times 224] + 16 = 76$*
$y_{64} = [\,(48 / 224)^{0.5} \times 224] + 16 = 120$*
$y_{96} = [\,(80 / 224)^{0.5} \times 224] + 16 = 150$*
$y_{128} = [\,(112 / 224)^{0.5} \times 224] + 16 = 174$*
* rounded to the nearest integer

The above will result in a gamma curve shown below, assuming a ramp signal as an input.

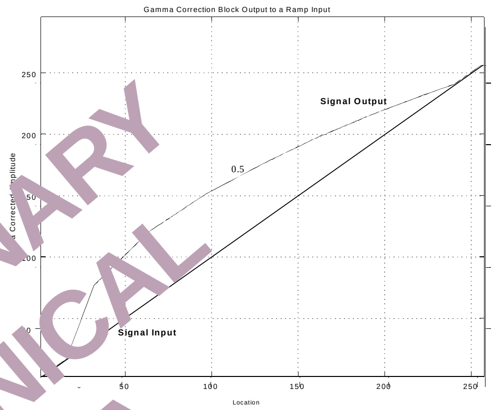


Figure 91 Signal Input (Ramp) and Signal Output for Gamma 0.5

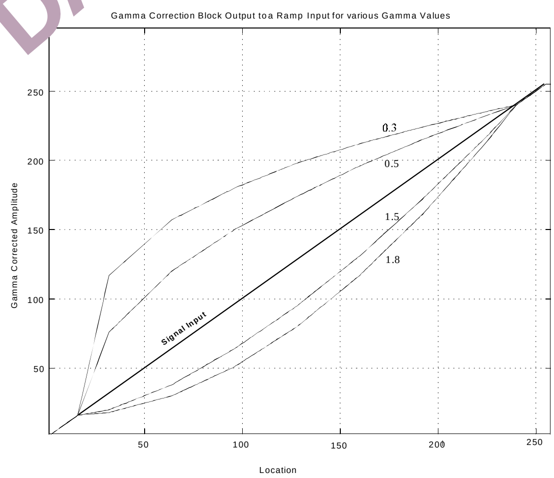


Figure 92 Signal Input (Ramp) and selectable Gamma Output curves

The gamma curves shown above are examples only, any user defined curve is acceptable in the range of 16 - 240.

SHARPNESS FILTER CONTROL AND ADAPTIVE FILTER CONTROL

There are three Filter modes available on the ADV7196: Sharpness Filter mode and two Adaptive Filter modes.

SHARPNESS FILTER MODE

To enhance or attenuate the Y signal in the frequency ranges shown in the figures below, the following register settings must be used:
Sharpness Filter must be enabled (MR17="1") and Adaptive Filter Control must be disabled (MR57="0").

To select one of the 256 individual responses, the according gain values for each filter, which range from -8 to +7 , must be programmed into the Filter Gain register.

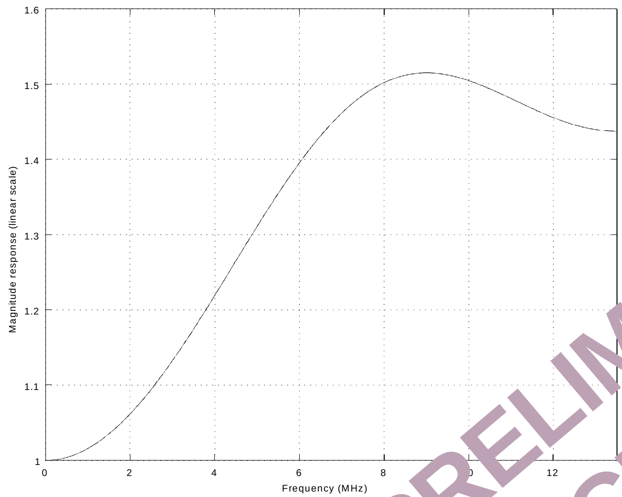


Figure xx Frequency response in Sharpness Filter mode with Ka=+3 and Kb=+7 when step input is applied

ADAPTIVE FILTER MODE

The Adaptive Filter Threshold A, B, C registers, the Adaptive Filter Gain 1, 2, 3 registers and the Filter Gain register are used in Adaptive Filter mode. To activate the Adaptive Filter control, Sharpness Filter must be enabled (MR17="1") and Adaptive Filter Control must be enabled (MR57="1").

The derivative of the incoming signal is compared to the three programmable threshold values: Adaptive Filter Threshold A, B, C.
In order to adapt to changes of the input signal, the Adaptive Filter Control block has a delay of 8T.

The edges can then be attenuated with the settings in Adaptive Filter Gain 1, 2, 3 registers and Filter Gain register.

According to the settings of the Adaptive Mode control (MR56), there are two Adaptive Filter Modes available:

1. Mode A: is used when Adaptive Filter Mode (MR56) is set to"0". In this case, Filter B (LPF) will be used in the adaptive filter block. Also, only the programmed values for Gain B in the Filter Gain, Adaptive Filter Gain 1, 2, 3 are applied when needed. The Gain A values are fixed and can not be changed.

2. Mode B: is used when Adaptive Filter Mode (MR56) is set to '1'. In this mode a cascade of Filter A and Filter B is used. Both settings for Gain A and Gain B in the Filter Gain, Adaptive Filter Gain 1, 2, 3 become active when needed.

The flowchart demonstrates the Adaptive Filter Control functionality.

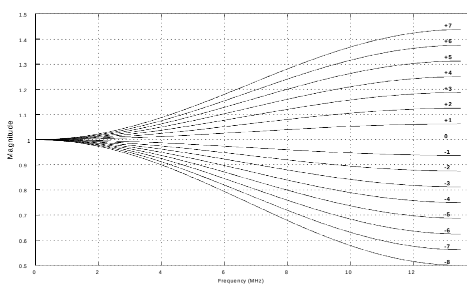


Figure xx Filter B Response

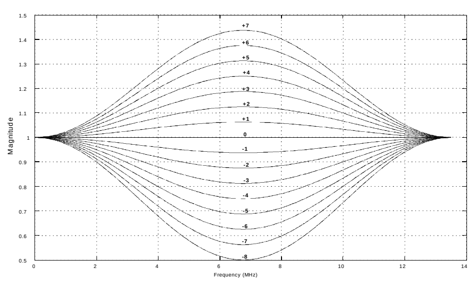


Figure xx Filter A Response

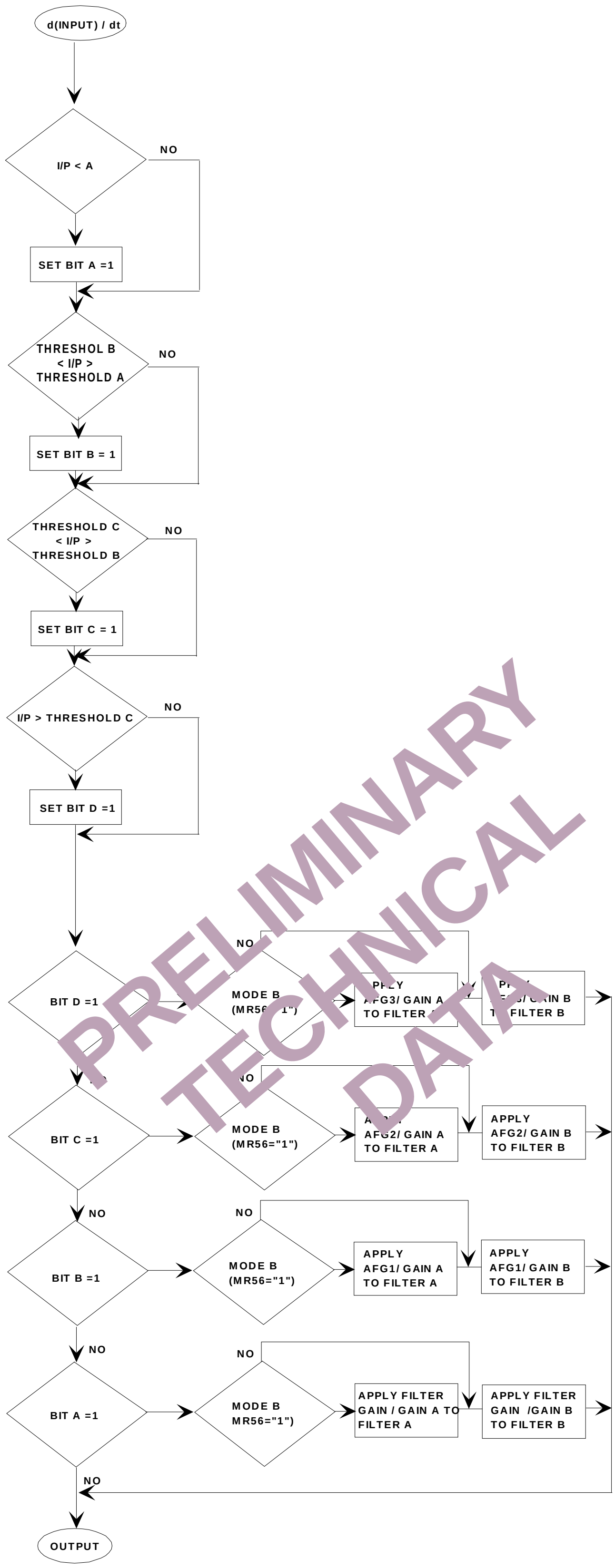


Figure xx Adaptive Filter Control Functionality

ADAPTIVE FILTER GAIN 1

AFG1 (AFG1)7-0

(Address (SR5-SR0) = 22H)

This 8-bit wide register is used to program the gain applied to signals which lie above Adaptive Filter Threshold A but are smaller than Adaptive Filter Threshold B.
Gain A and Gain B values vary from -8 to +7. Settings for (AFG1)3-0 have no effect unless Filter Selection is set to FilterA&B (MR56="1").

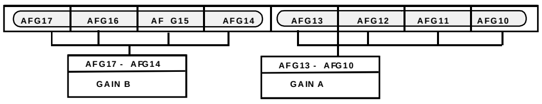


Figure xx. Adaptive Filter Gain 1 Register

ADAPTIVE FILTER GAIN 2

AFG2 (AFG2)7-0

(Address (SR5-SR0) = 23H)

This 8-bit wide register is used to program the gain applied to signals which lie above Adaptive Filter Threshold B but are smaller than Adaptive Filter Threshold C.
Gain A and Gain B values vary from -8 to +7. Settings for (AFG2)3-0 have no effect unless Filter Selection is set to FilterA&B (MR56="1").

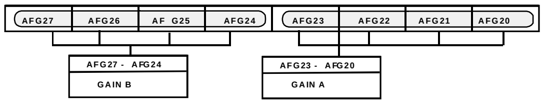


Figure xx. Adaptive Filter Gain 2 Register

ADAPTIVE FILTER GAIN 3

AFG3 (AFG3)7-0

(Address (SR5-SR0) = 24H)

This 8-bit wide register is used to program the gain applied to signals which lie above Adaptive Filter Threshold C.
Gain A and Gain B values vary from -8 to +7. Settings for (AFG3)3-0 have no effect unless Filter Selection is set to FilterA&B (MR56="1").

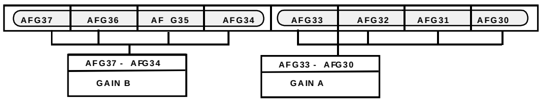


Figure xx. Adaptive Filter Gain 3 Register

The gain applied to signals which lie below Adaptive Threshold A are programmed in the Filter Gain register.
At any one time only one of the following registers is active: AFG1, AFG2, AFG3, FG. The gain values can be 'pre-programmed' and become active whenever the threshold conditions for the according register is met. As demonstrated in the flowchart on the previous page.

<u>ADAPTIVE FILTER THRESHOLD A</u>
AFTA AFTA7-0
(Address (SR5-SR0) = 25H)
This 8-bit wide register is used to program the threshold value for small edges. The recommended programmable threshold range is from 16-235, although any value in the range of 0 -255 can be used.

<u>ADAPTIVE FILTER THRESHOLD B</u>
AFTB AFTB7-0
(Address (SR5-SR0) = 26H)
This 8-bit wide register is used to program the threshold value for medium edges and has priority over Adaptive Threshold A. The recommended programmable threshold range is from 16-235, although any value in the range of 0-255 can be used.

<u>ADAPTIVE FILTER THRESHOLD C</u>
AFTC AFTC7-0
(Address (SR5-SR0) = 27H)
This 8-bit wide register is used to program the threshold value for large edges and has priority over Adaptive Threshold A and B. The recommended programmable threshold range is from 16-235, although any value in the range of 0-255 can be used.

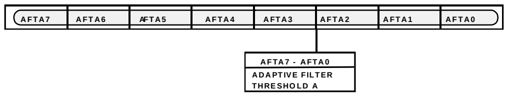


Figure xx. Adaptive Filter Threshold A Register

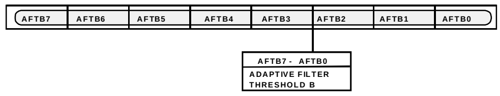


Figure xx. Adaptive Filter Threshold B Register

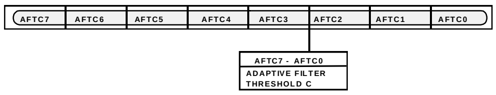


Figure xx. Adaptive Filter Threshold C Register

HDTV MODE

HDTV MODE

MODE REGISTER 0
MR0 (MR07-MR00)
(Address (SR4-SR0) = 00H)

Figure xx shows the various operations under the control of Mode Register 0.

MR0 BIT DESCRIPTION

Output Standard Selection (MR00-MR01):
These bits are used to select the output levels from the ADV7196.
If EIA 770.3 (MR01-00='00') is selected, the output levels will be: 0mV for blanking level, 700mV for peak white (Y channel),+/- 350mV for Pr,Pb outputs and -300 mV for tri-level sync.

If Full Input Range (MR01-00='10') is selected, the output levels will be 700mV for peak white for the Y channel, +/- 350 mV for Pr, Pb outputs and -300mV for Sync. This mode is used for RS-170, RS343A standard output compatibility.

Sync insertion on the Pr, Pb channels is optional.
For output levels refer to the Appendix.

Input Control Signals (MR02-MR03):
These control bits are used to select whether data is input with external horizontal, vertical and blanking sync signals or if the data is input with embedded EAV/SAV codes. An Asynchronous timing mode is also available using TSYNC, $\overline{SYNC}$ and DV as input control signals.
These timing control signals have to be programmed by the user.
The figure below shows an example of how to program the ADV7196 to accept a different high definition standard but SMPTE293M, SMPTE274M, SMPTE296M or ITU-R.BT1358 standard.

Reserved (MR04):
A '0' must be written to this bit.

Input Standard (MR05):
Select between 1080i or 720p input.

DV polarity (MR06):
This control bit allows to select the polarity of the DV input control signal to be either active high or active low.

Reserved (MR07):
A '0' must be written to this bit.

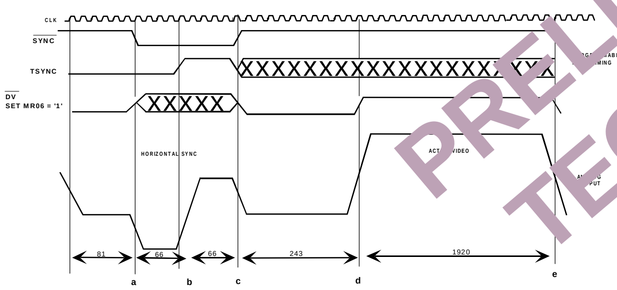


Figure xx: Async Timing Mode - Programming Input Control signals for SMPTE295M compatibility

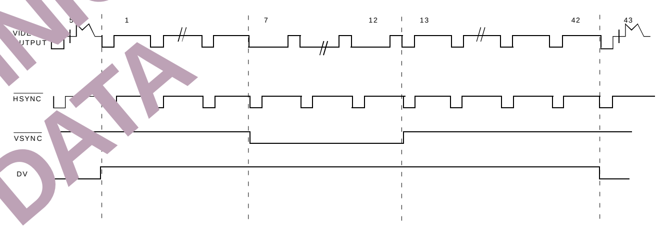


Figure xx: DV input control signal in relation to video output signal

The truth table below must be followed when programming the control signals in Async Timing Mode.

$\overline{SYNC}$	TSYNC	DV	
1 -> 0	0	0 or 1	50% point of falling edge of tri-level horizontal sync signal, a
0	0 -> 1	0 or 1	25% point of rising edge of tri-level horizontal sync signal, b
0 -> 1	0 or 1	0	50% point of falling edge of tri-level horizontal sync signal, c
1	0 or 1	0 -> 1	50% start of active video, d
1	0 or 1	1 -> 0	50% end of active video, e

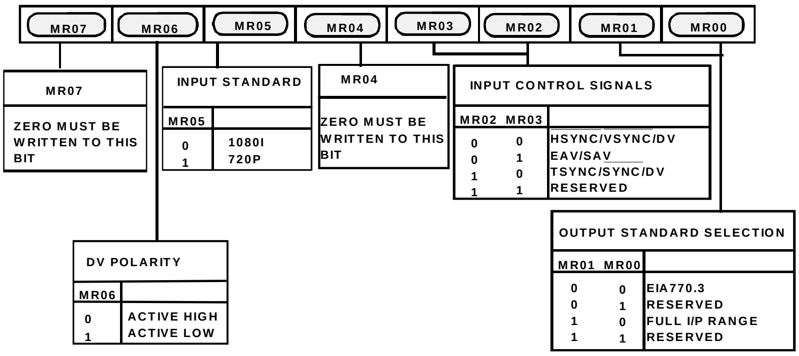


Figure xx: Mode Register 0

MODE REGISTER 1
MR1 (MR17-MR10)
(Address (SR4-SR0) = 01H)

Figure xx shows the various operations under the control of Mode Register 1.

MR1 BIT DESCRIPTION

Pixel Data Enable (MR10):
When this bit is set to "0", the pixel data input to the ADV7196 is blanked such that a black screen is output from the DACs. When this bit is set to "1", pixel data is accepted at the input pins and the ADV7196 outputs to the standard set in 'Output Standard Selection' (MR01-00).

Input Format (MR11):
It is possible to input data in 4:2:2 format or in 4:4:4 HDTV format.

Testpattern Enable (MR12):
Enables or disables the internal test pattern generator.

Testpattern Hatch/Frame (MR13):
If this bit is set to '0', a cross hatch test pattern is output from the ADV7196. The cross hatch test pattern can be used to test monitor convergence.
If this bit is set to '1', a uniform colored frame/field test pattern is output from the ADV7196.

The color of the lines or the frame/field is by default white but can be programmed to be any color using the Color Y, Color Cr, Color Cb registers.

VBI open (MR14):
This bit enables or disables the facility of VBI data insertion during the Vertical Blanking Interval.
For this purpose lines 7-20 in 1080i and lines 6-25 in 720p can be used for VBI data insertion.

Reserved (MR15 -MR17):
A '0' must be written to these bits.

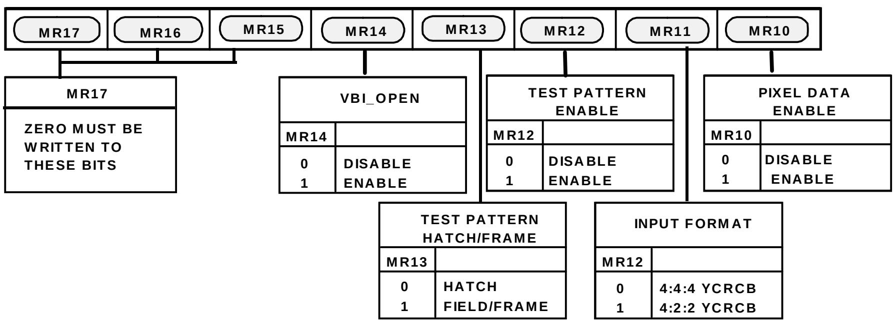


Figure xx: Mode Register 1

MODE REGISTER 2
MR1 (MR27-MR20)
(Address (SR4-SR0) = 02H)

Figure xx shows the various operations under the control of Mode Register 2.

MR2 BIT DESCRIPTION
Y Delay (MR20-22):
With theses bits it is possible to delay the Y signal with respect to the falling edge of the horizontal sync signal by up to
4 pixel clock cycles. Figure xx demonstrates this facility.

Color Delay (MR23-25):
With theses bits it is possible to delay the color signals with respect to the falling edge of the horizontal sync signal by up to 4 pixel clock cycles. Figure xx demonstrates this facility.

Reserved (MR26-27):
A '0' must be written to these bits.

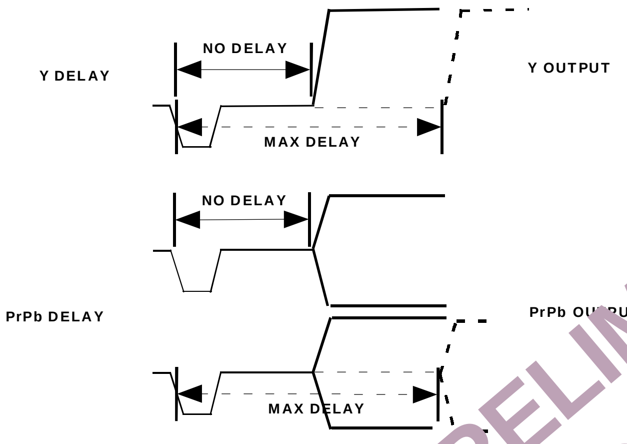


Figure xx: Y and Color Delay

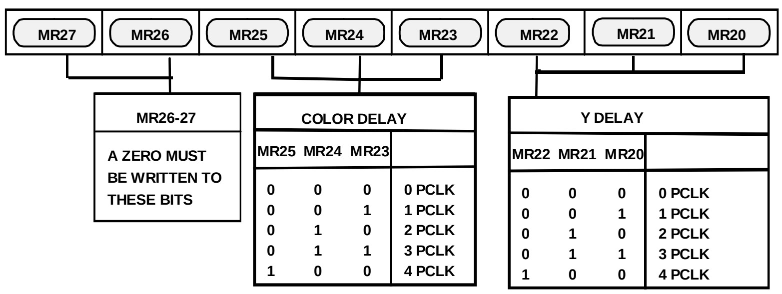


Figure xx: Mode Register 2

MODE REGISTER 3
MR3 (MR37-MR30)
(Address (SR4-SR0) = 03H)

Figure xx shows the various operations under the control of Mode Register 3.

MR3 BIT DESCRIPTION
HDTV Enable (MR30):
When this bit is set to '1' the ADV7196 reverts to HDTV mode. When set to '0' the ADV7196 reverts to Progressive Scan mode (PS mode).

Reserved(MR31-32):
A "0" must be written to these bits.

DAC A Control (MR33):
Setting this bit to "1" enables DAC A , otherwise this DAC is powered down.
DAC B Control (MR34):
Setting this bit to "1" enables DAC B , otherwise this DAC is powered down.
DAC C Control (MR35):
Setting this bit to "1" enables DAC C , otherwise this DAC is powered down.
Reserved (MR36-37):
A '0' must be written to these bits.

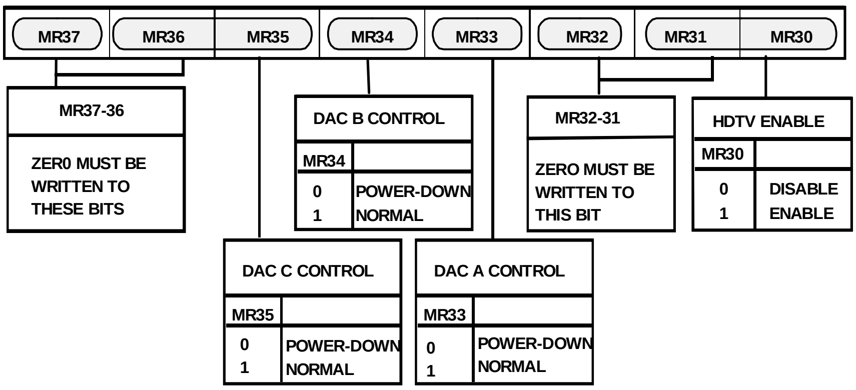


Figure xx: Mode Register 3

MODE REGISTER 4
MR4 (MR47-MR40)
(Address (SR4-SR0) = 04H)

Figure xx shows the various operations under the control of Mode Register 4.

MR4 BIT DESCRIPTION
Timing Reset (MR40):
Toggling MR40 from low to high and low again resests the internal horizontal and vertical timing counters.

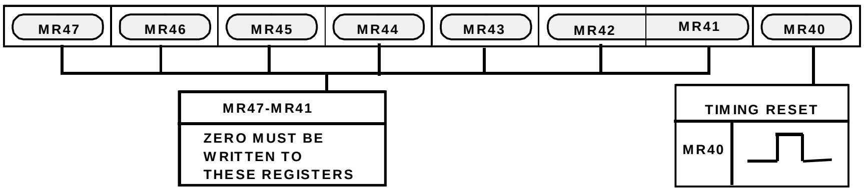


Figure xx: Mode Register 4

MODE REGISTER 5
MR5 (MR57-MR50)
(Address (SR4-SR0) = 05H)

Figure xx shows the various operations under the control of Mode Register 5.

MR5 BIT DESCRIPTION

Reserved (MR50):
These bit is reserved for the revision code.

RGB Mode (MR51):
When RGB mode is enabled (MR51='1') the ADV7196 accepts unsigned binary RGB data at its input port. This control is also available in Async Timing Mode.

Sync on PrPb (MR52):
By default the color component output signals Pr, Pb do not contain any horizontal sync pulses. If required they can be inserted when MR52="1". This control is not available in RGB mode.

Color Output Swap (MR53):
By default DAC B is configured as the Pr output and DAC C as the Pb output. In setting this bit to '1' the DAC outputs can be swapped around so that DAC B outputs Pb and DAC C outputs Pr. The table below demonstrates this in more detail.

Reserved (MR54-57):
"0' must be written to these bits.

In 4:4:4 input mode		
Color data input on pins:	**MR53**	**Analog Output signal:**
Cr 9-0	0	Dac B
Cb/Cr 9-0	0	Dac C
Cr 9-0	1	Dac C
Cb/Cr 9-0	1	Dac B
In 4:2:2 input mode		
Color data input on pins:	**MR53**	**Analog Output signal:**
Cr 9-0	0 or 1	not operational
Cb/Cr 9-0	0	Dac C (Pb)
Cb/Cr 9-0	1	Dac C (Pr)

Figure xx: Relationship between input pixel port, MR53 and DAC B, DAC C outputs

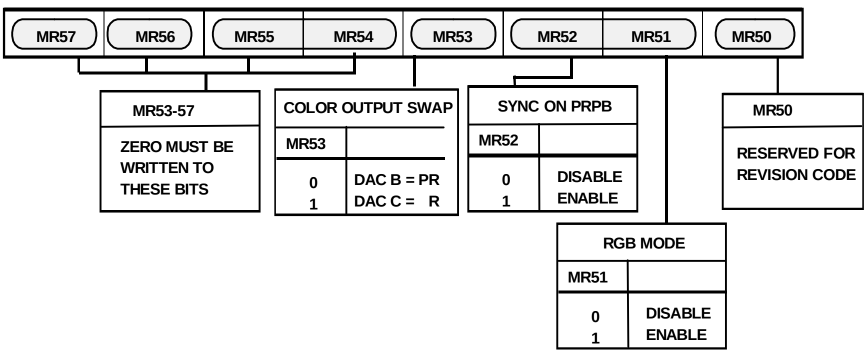


Figure xx: Mode Register 5

DAC termination and layout considerations

Voltage Reference

The ADV7196 contains an onboard voltage reference. The Vref pin is normally terminated to VAA throught a 0.1uF capacitor when the internal Vref is used. Alternatively, the ADV7196 can be used with an external Vref (AD589).

Resistor Rset is connected between the Rset pin and AGND and is used to control the full scale output current and therefore the DAC voltage output levels. For full scale output Rset must have a value of 2470Ohms. Rload has a value of 300Ohms. When an input range of 0-1023 is selected the value of Rset must be 2820Ohms.

The ADV7196 has three analog outputs, corresponding to Y, Pr, Pb video signals. Each one of the PrPb DACs is capable of an output current of 2.66mA, the Y DAC provides 4.33mA output current. The DACs must be used with external buffer circuits in order to provide sufficient current to drive an output device. Suitable op-amps are the AD8009, AD8002 or the AD8001current feedback amplifiers.

PC Board Layout Considerations

The ADV7196 is optimally designed for lowest noise performance, both radiated and conducted noise. To complement the excellent noise performance of the ADV7196, it is imperative that great care be given to the PC board layout.

The layout should be optimized for lowest noise on the ADV7196 power and ground lines. This can be achieved by shielding the digital inputs and providing good decoupling. The lead length between groups of VAA and AGND and VDD and DGND pins should be kept as short as possible to minimized inductive ringing.

It is recommended that a four-layer printed circit board is used. With power and ground planes separating the layer of the signal carrying traces of the components and solder side layer. Placement of components should consider to seperate noisy circuits, such as crystal clocks, high speed logic circuitry and analog circuitry.

There should be a seperate analog ground plane (AGND) and a seperate digital ground plane (GND).

Power planes should encompass a digital power plane (VDD) and a analog power plane (VAA). The analog power plane should contain the DACs and all associated circuitry, Vref circuitry.
The digital power plane should contain all logic circuitry.
The analog and digital power planes should be individually connected to the common power plane at one single point through a suitable filtering device, such as a ferrite bead.

DAC output traces on a PCB should be treated as transmission lines. It is recommended that the DACs be placed as close as possible to the output connector, with the analog output traces being as short as possible (less than 3 inches. The DAC termination resistors should be placed as close as possible to the DAC outputs and should overlay the PCB's ground plane. As well as minimizing reflectitons, short analog output traces will reduce noise pickup due to neighbouring digital circuitry.

Supply Decoupling

Noise on the analog power plane can be further reduced by the use of decoupling capacitors.
Optimum performance is achieved by the use of 0.1uF ceramic capacitors. Each of group of VAA or VDD pins should be individually decoupled to ground. This should be done by placing the capacitors as close as possible to the device with the capacitor leads as short as possible, thus minimizing lead inductance.

Digital Signal Interconnect

The digital signal lines should be isolated as much as possible from the analog outputs and other analog circuitry. Digital signal lines should not overlay the analog power plane.
Due to the high clock rates used, long clock lines to the ADV7196 should be avoided to minimize noise pickup.
Any active pull-up termination resistors for the digital inputs should be connected to the digital power plane and not the analog power plane.

Analog Signal Interconnect

The ADV7196 should be located as close as possible to the output connectors thus minimizing noise pickup and reflections due to impedance mismatch.
For optimum performance, the analog outputs should each be source and load terminated, as shown in the below figure.The termination resistors should be as close as possible to the ADV7196 to minimize reflections.

Any unused inputs should be tied to ground.

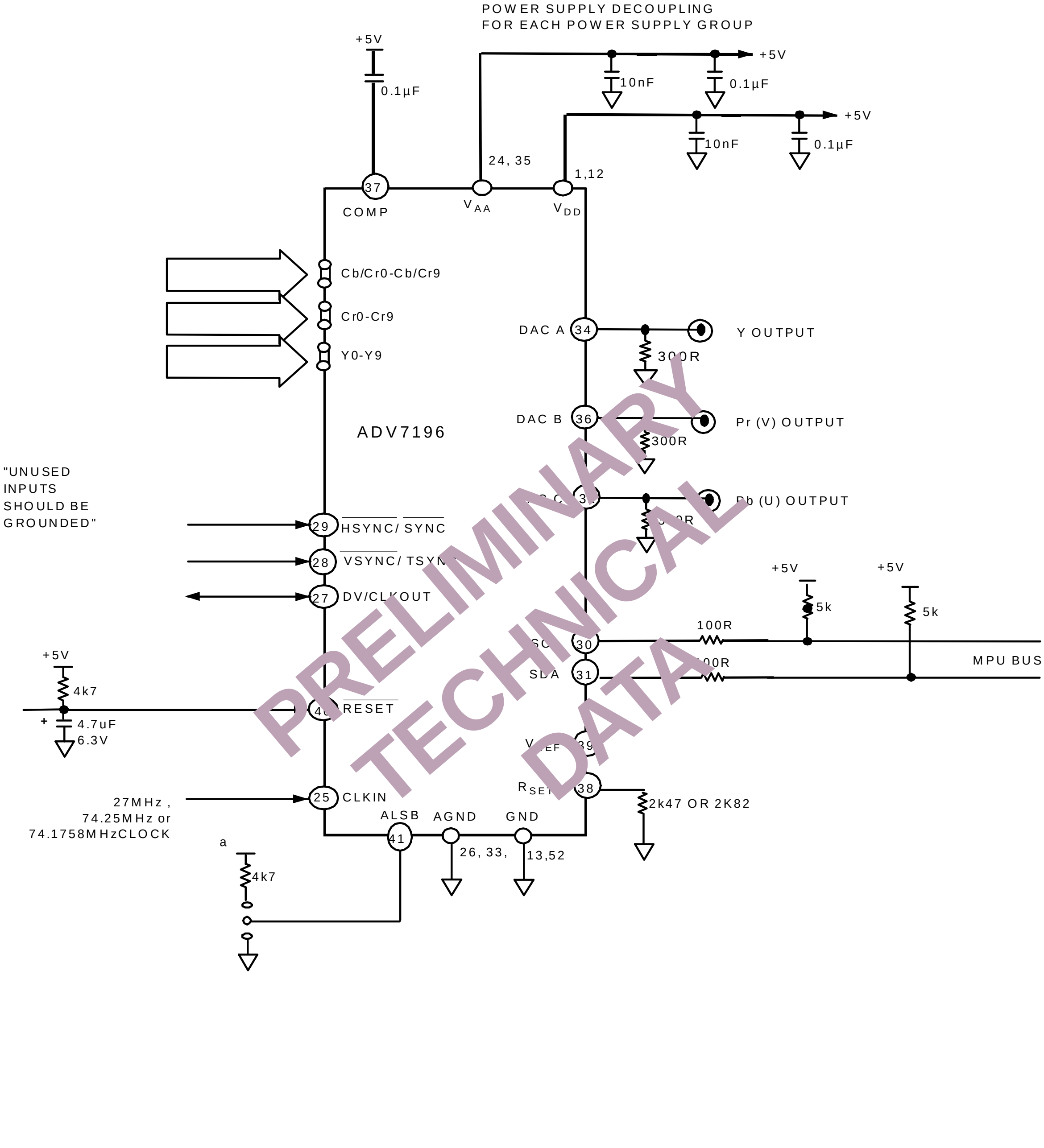


Figure xx: ADV7196 Circuit Layout

Video Output Buffer and optional Output Filter

Output buffering is necessary in order to drive output devices, such as progressive scan or HDTV monitors.
Analog Devides produces a range of suitable op ams for this application. Suitable op amps would be the AD8009,AD8002 or AD8001. More information on line driver buffering circuits is given in the relevant op amp datasheets.

An optional analog reconstruction LPF might be required as an antialias filter if the ADV7196 is connected to a device which requires this filtering.

The Eval ADV7196/7 EB evaluation board uses the ML6426 Microlinear IC, which provides buffering and Low-pass filtering for HDTV applications.

The Eval ADV7196/7EB RevA evaluation board uses the AD8009 as a buffer and a 6th order Chebychev Filter as a LPF.

The Application note, ANxxx, describes in detail these two designs and should be consulted when designing external filter and buffers for Analog Devices Video Encoders.

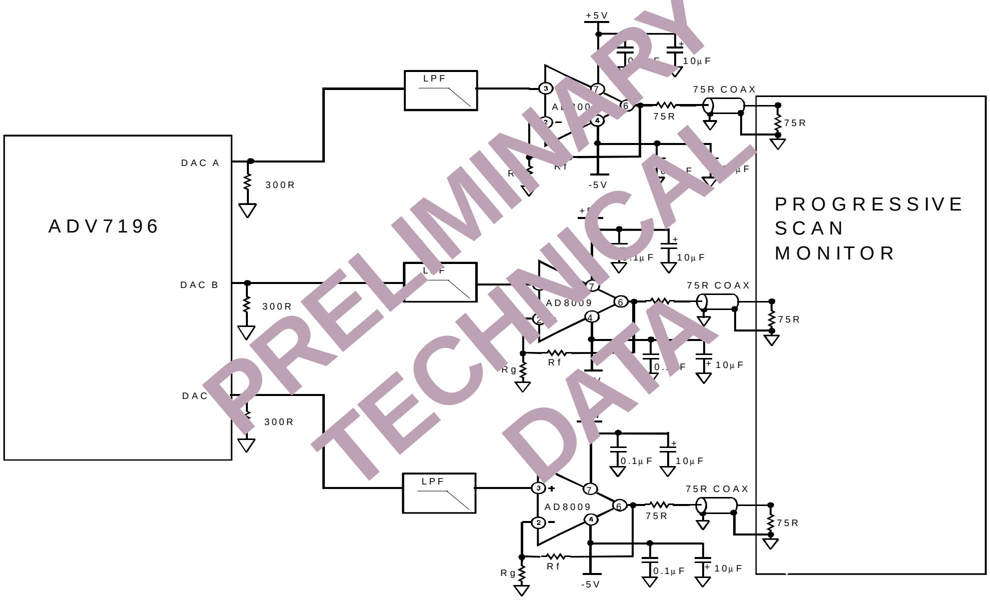


Figure xx Output Buffer and Optional Filter

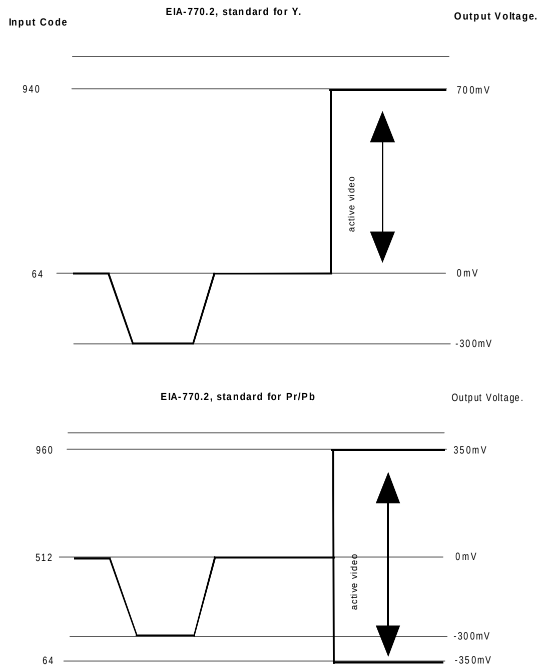


Figure xx EIA 770.2 Standard output signals (525p)

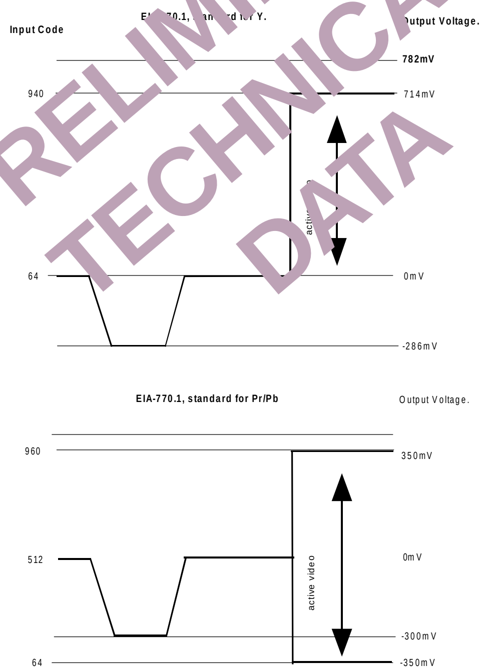


Figure xx EIA 770.1 Standard output signals(525p)

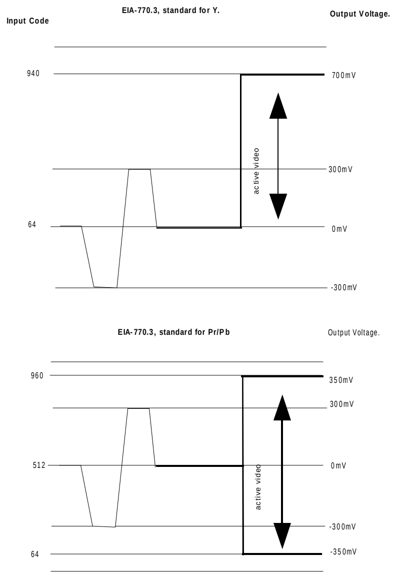


Figure xx EIA 770.3 Standard output signals(1080i, 720p)

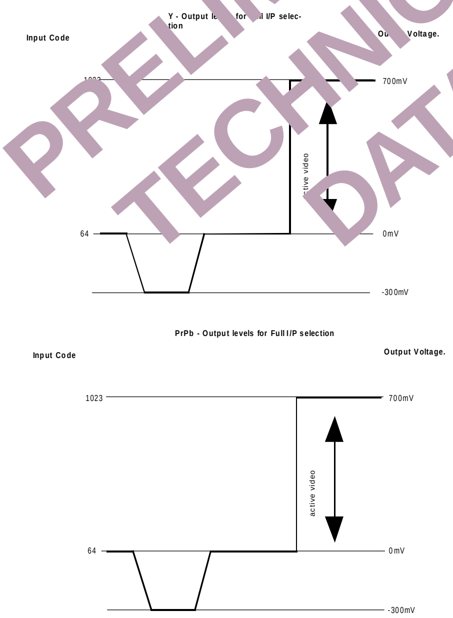


Figure xx Output levels for Full I/P selection

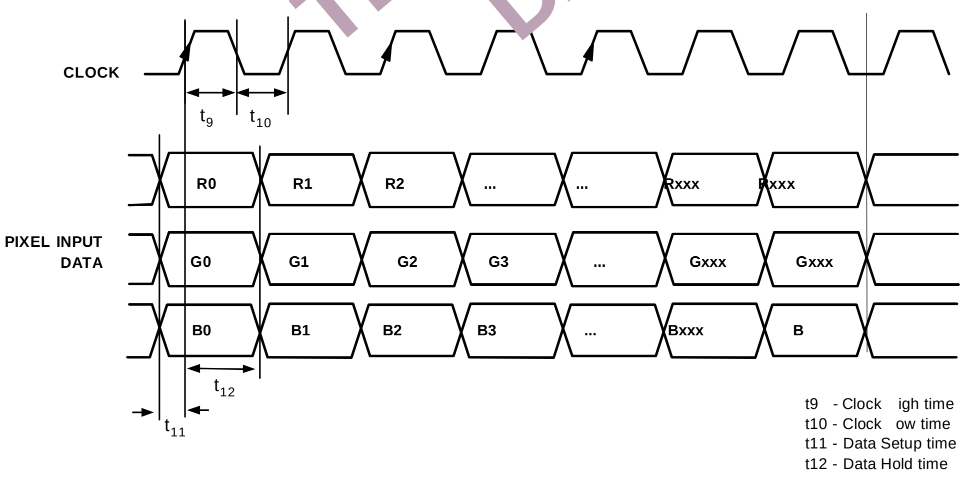


Figure xx 4:4:4 RGB input data format timing diagram

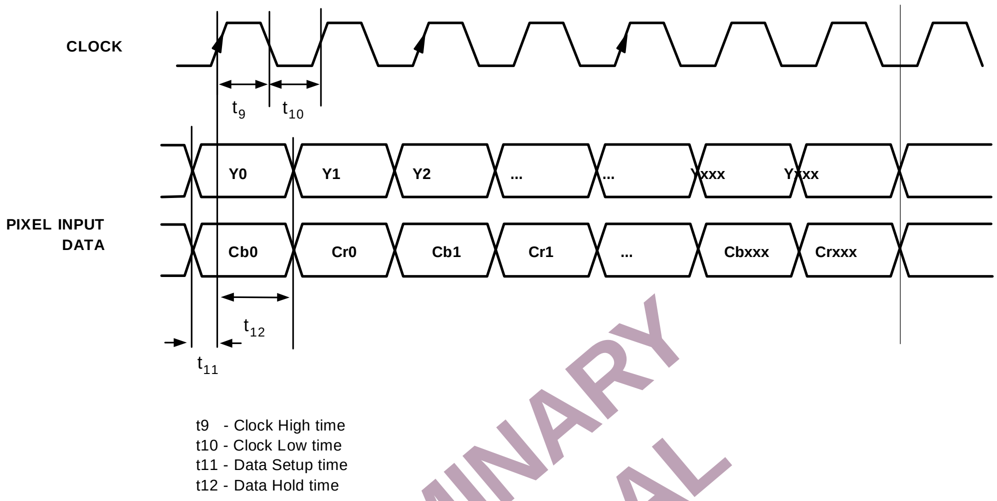


Figure xx 4:2:2 input data format timing diagram

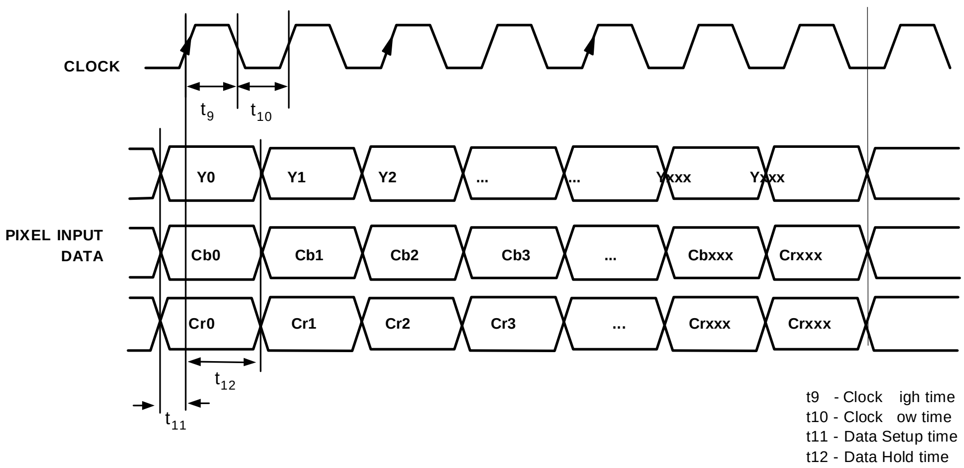


Figure xx 4:4:4 YCrCb input data format timing diagram

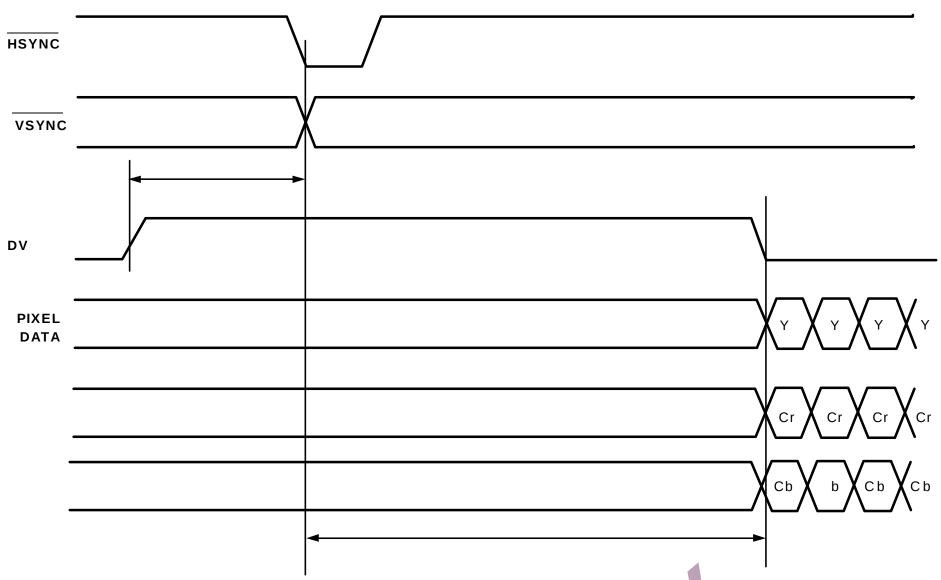
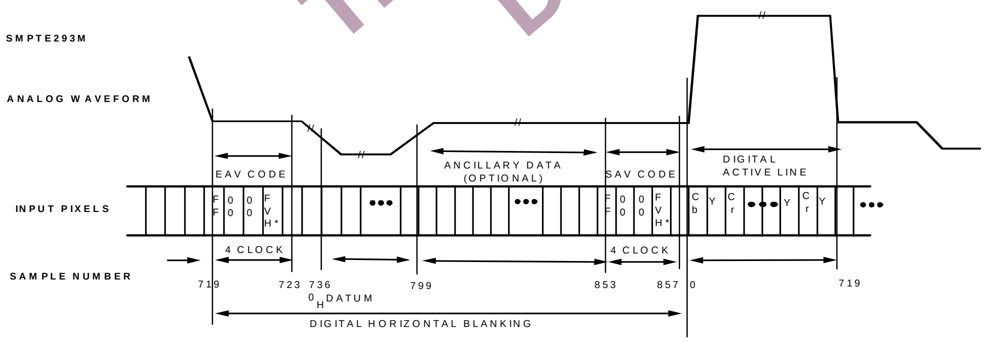
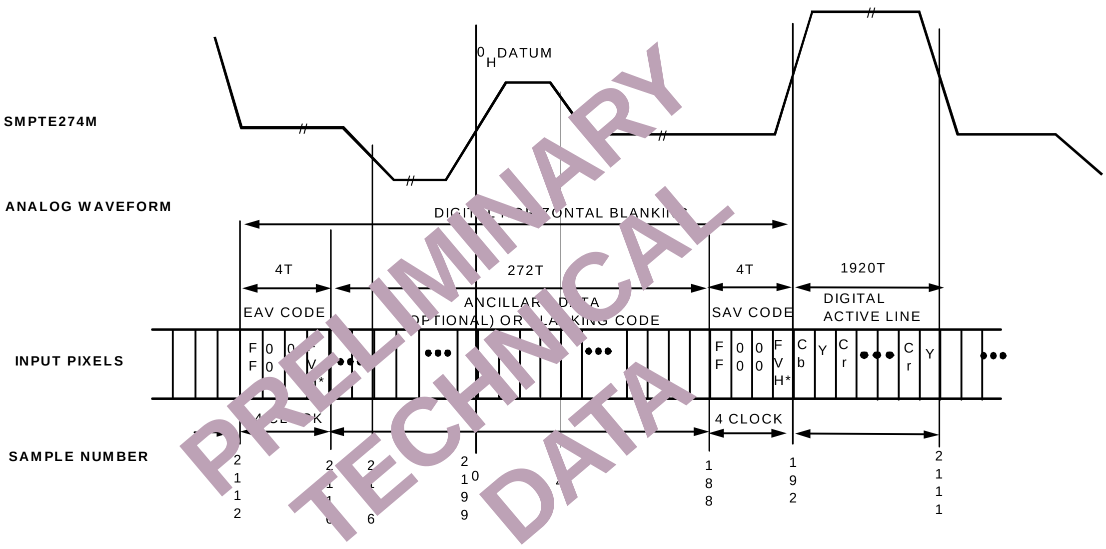


Figure xx Input timing diagram



FVH* = FVH and Parity Bits
SAV : Line 43 - 525 = 200H
SAV: Line 1 - 42 = 2AC
EAV: Line 43 - 525 = 274H
EAV: Line 1 - 42 = 2D8

Figure xx EAV/SAV input data timing diagram - SMPTE293M



FVH* = FVH and Parity Bits
SAV/EAV : Line 1 - 562 : F=0
SAV/EAV: Line 563 - 1125 : F=1
SAV/EAV: Line 1-20; 561-583;1124-1125: V=1
SAV/EAV: Line 21-560;584-1123: V=0

Figure xx EAV/SAV input data timing diagram - SMPTE 274M

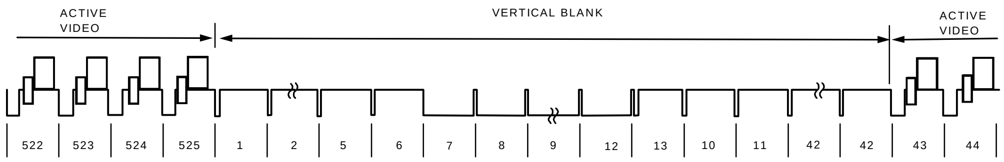


Figure xx SMPTE 293M (525p)

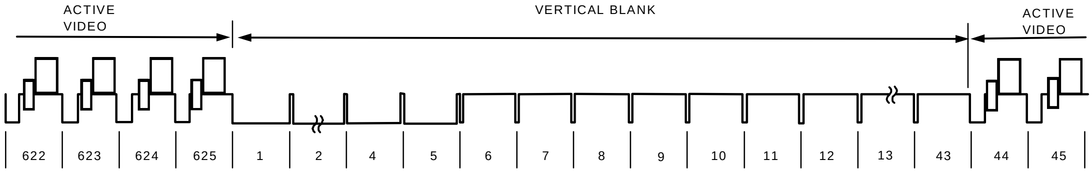


Figure xx ITU-R.BT1358 (625p)

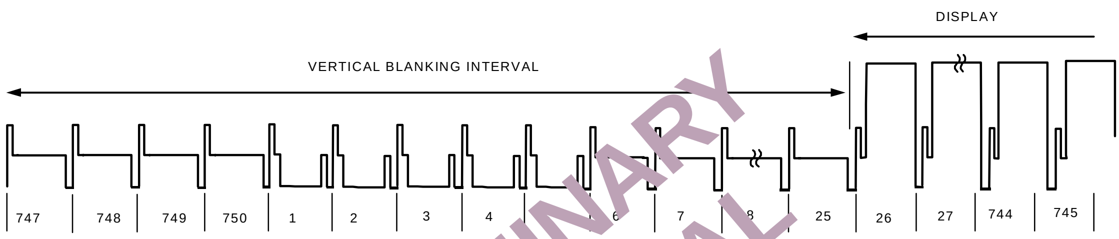


Figure xx SMPTE 296M (720p)

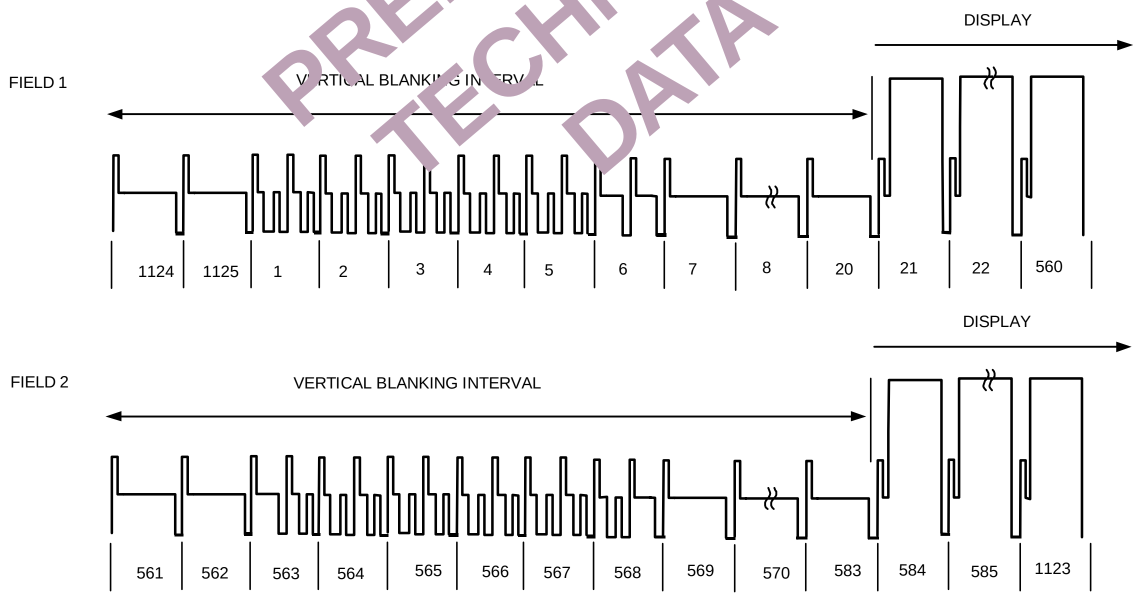


Figure xx SMPTE 274M (1080i)

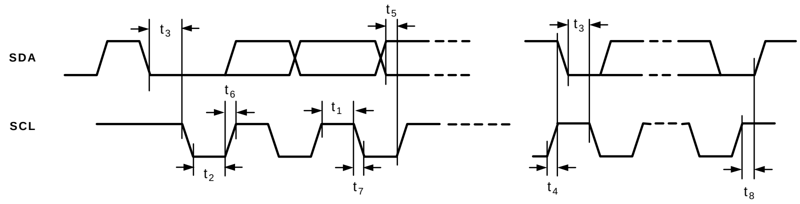


Figure 1. MPU Port Timing Diagram

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

52-Lead Plastic Quad Flatpack

(S-52)