



ULN2803

LINEAR INTEGRATED CIRCUIT

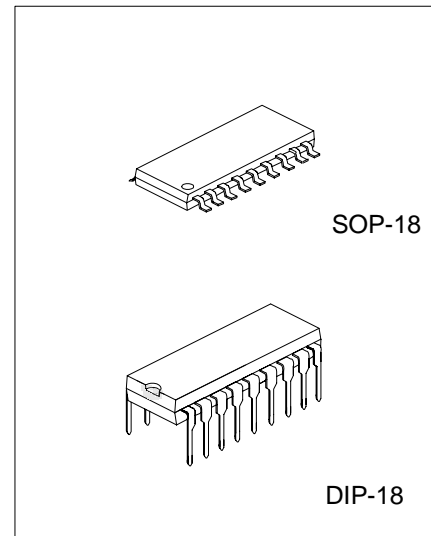
EIGHT DARLINGTON ARRAYS

DESCRIPTION

The UTC **ULN2803** is high-voltage, high-current Darlington drivers comprised of eight NPN Darlington pairs.

FEATURES

- *Output current (single output) 500mA MAX.
- *High sustaining voltage output 50V MIN.
- *Output clamp diodes
- *Inputs compatible with various types of logic



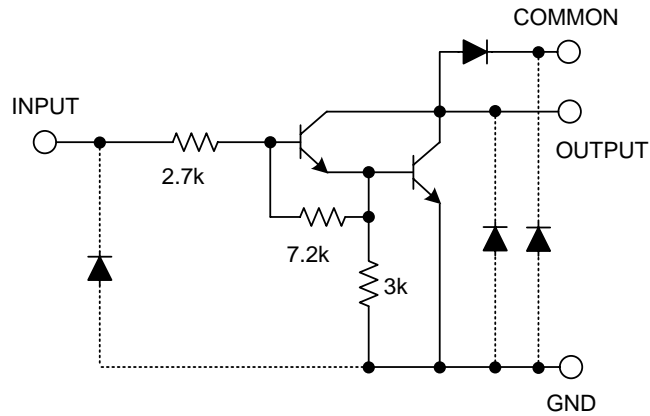
*Pb-free plating product number: ULN2803L

ORDERING INFORMATION

Ordering Number		Package	Packing
Normal	Lead Free Plating		
ULN2803-D18-T	ULN2803L-D18-T	DIP-18	Tube
ULN2803-S18-R	ULN2803L-S18-R	SOP-18	Tape Reel
ULN2803-S18-T	ULN2803L-S18-T	SOP-18	Tube

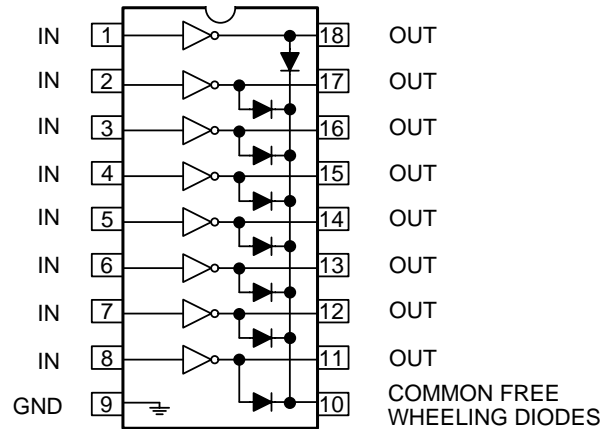
<p>ULN2803L-D18-T</p> <p>(1) Packing Type (2) Package Type (3) Lead Plating</p>	<p>(1) T: Tube, R: Tape Reel (2) D18: DIP-18, S18: SOP-18 (3) L: Lead Free Plating, Blank: Pb/Sn</p>
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■ SCHEMATICS (EACH DRIVER)



Note: The input and output parasitic diodes cannot be used as clamp diodes.

■ PIN CONFIGURATIONS



■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Input Voltage	V_{IN}	-0.5~30	V
Output Sustaining Voltage	$V_{CE(SUS)}$	-0.5~50	V
Output Current	I_{OUT}	500	mA/ch
Clamp Diode Reverse Voltage	V_R	50	V
Clamp Diode Forward Current	I_F	500	mA
Power Dissipation	DIP-18	P_D	W
	SOP-18		
		1.47	
		0.54/0.625(Note)	
Operating Temperature	T_{OPR}	-40 ~ +85	°C
Storage Temperature	T_{STG}	-40 ~ +150	°C

Note 1. On glass epoxy PCB (30x30x1.6mm Cu 50%)

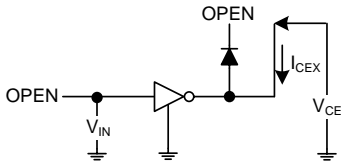
2. Absolute maximum ratings are stress ratings only and functional device operation is not implied. The device could be damaged beyond Absolute maximum ratings.

■ ELECTRICAL CHARACTERISTICS ($T_a=25^\circ\text{C}$, unless otherwise specified.)

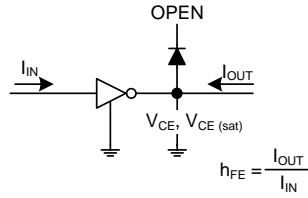
PARAMETER	SYMBOL	TEST CIRCUIT	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Output Leakage Current	I_{CEX}	1	$V_{CE}=50\text{V}, T_a=25^\circ\text{C}$ $V_{CE}=50\text{V}, T_a=85^\circ\text{C}$			50 100	μA	
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	2	$I_{OUT}=350\text{mA}, I_{IN}=500\mu\text{A}$ $I_{OUT}=200\text{mA}, I_{IN}=350\mu\text{A}$ $I_{OUT}=100\text{mA}, I_{IN}=250\mu\text{A}$		1.3 1.1 0.9	1.6 1.3 1.1	V	
Input Current	ON	$I_{IN(ON)}$	3	$V_{IN}=3.85\text{V}, I_{OUT}=350\text{mA}$		0.93	1.35	mA
	OFF	$I_{IN(OFF)}$	4	$I_{OUT}=500\mu\text{A}, T_a=85^\circ\text{C}$	50	65		μA
Input Voltage (output on)	$V_{IN(ON)}$	5	$V_{CE}=2.0\text{V}$ $I_{OUT}=200\text{mA}$ $I_{OUT}=250\text{mA}$ $I_{OUT}=300\text{mA}$			2.4 2.7 3.0	V	
Clamp Diode Reverse Current	I_R	6	$V_R=50\text{V}, T_a=25^\circ\text{C}$ $V_R=50\text{V}, T_a=85^\circ\text{C}$			50 100	μA	
Clamp Diode Forward Voltage	V_F	7	$I_F=350\text{mA}$			2.0	V	
Input Capacitance	C_{IN}				15	25	pF	
Turn-On Delay	t_{ON}	8	$V_{OUT}=50\text{V}, R_L=125\Omega, C_L=15\text{pF}$		0.1	1	μs	
Turn-Off Delay	t_{OFF}	8	$V_{OUT}=50\text{V}, R_L=125\Omega, C_L=15\text{pF}$		0.2	1	μs	

TEST CIRCUIT

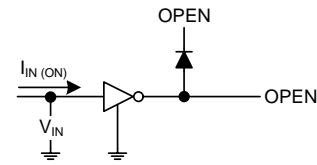
1. I_{CEX}



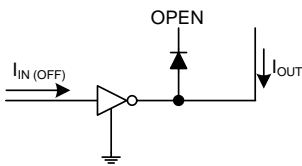
2. $V_{CE(sat)}$, h_{FE}



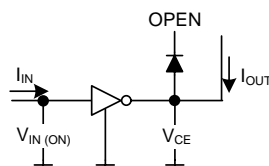
3. $I_{IN(ON)}$



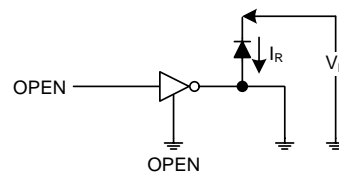
4. $I_{IN(OFF)}$



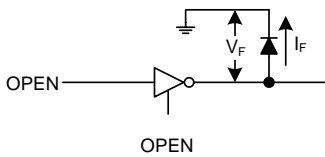
5. $V_{IN(ON)}$



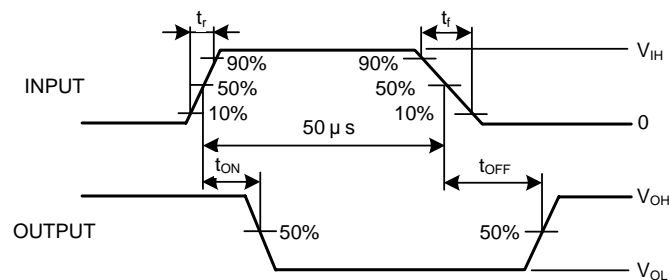
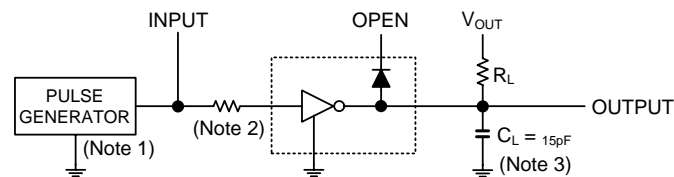
6. I_R



7. V_F

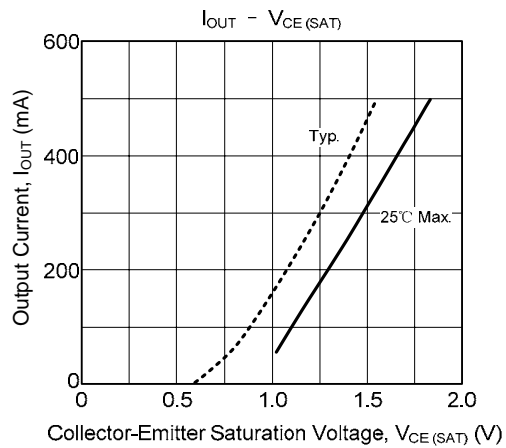
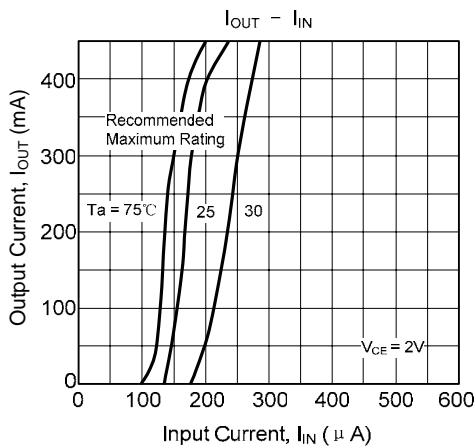
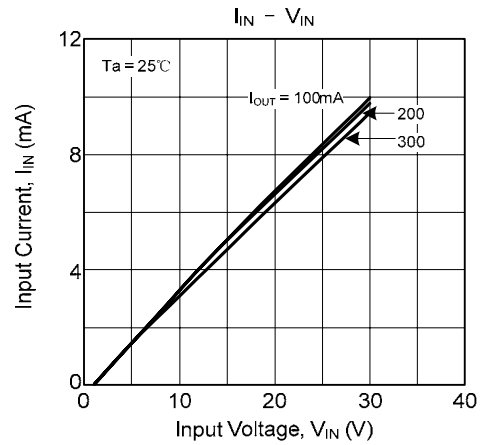
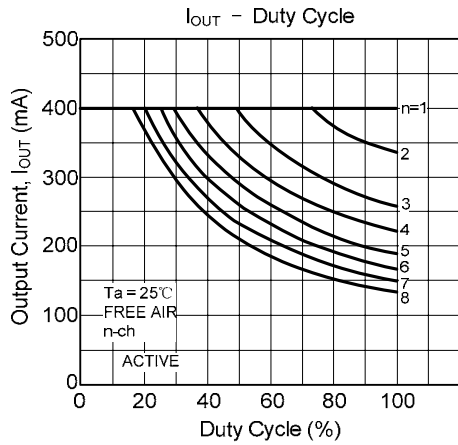
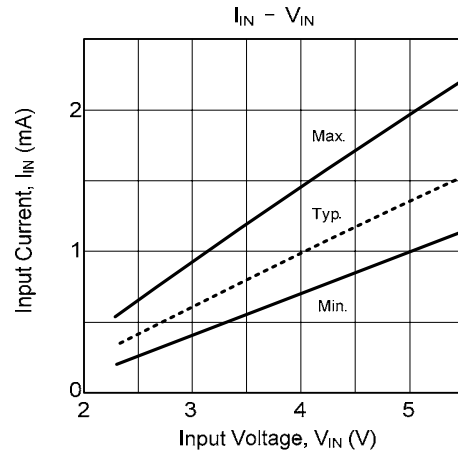
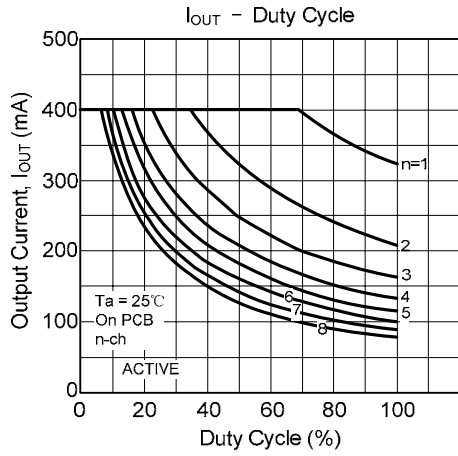


8. t_{ON} , t_{OFF}

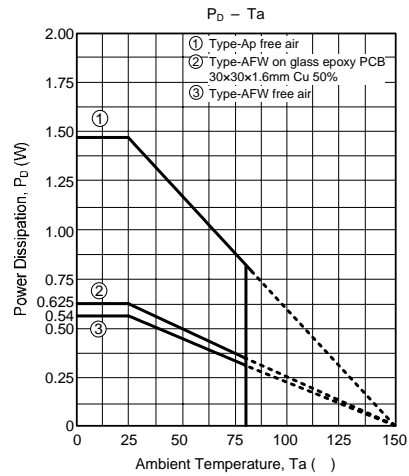
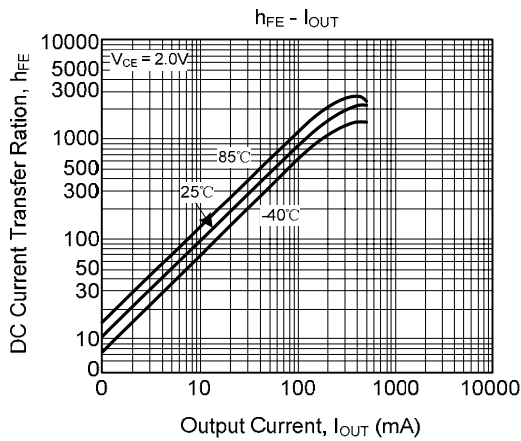
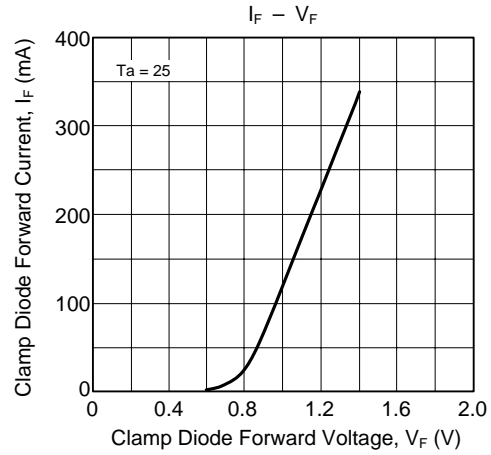
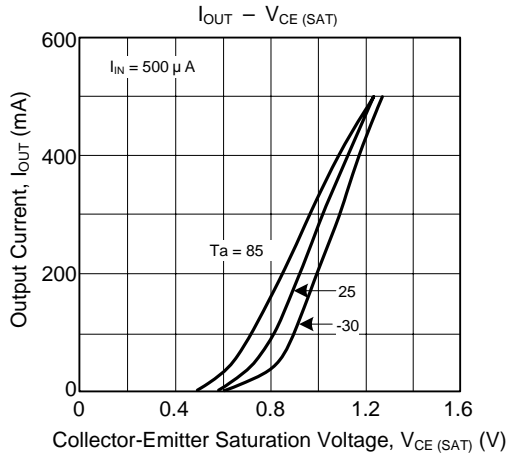


Note1: Pulse width $50\mu s$, duty cycle 10%
 Output impedance 50Ω , $t_r \leq 5ns$, $t_f \leq 10ns$
 Note2: $R_1: 0$, $V_{IH}: 3V$
 Note3: C_L includes probe and jig capacitance.

■ TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS(Cont.)



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