PRODUCT SPECIFICATION

Z86C27-ROM
Z86C97-ROMLESS
CMOS Z8® 8-BIT MICROCONTROLLER

FEATURES

- 8-bit CMOS microcontroller for consumer television applications, 64-pin DIP package.
- Low cost
- Low power consumption
- Fast instruction pointer-1.5 microseconds @ 4 MHz
- Two standby modes-STOP and HALT
- Low voltage detection/voltage sensitive reset
- 35 input/output lines
- On Screen Display Controller
- All digital CMOS levels Schmitt triggered
- 8 Kbytes of ROM
- 236 bytes of RAM
- Two programmable 8-bit Counter/Timers each with 6-bit programmable prescaler.
- Six vectored, priority interrupts from six different sources
- Clock speed up to 4 MHz
- Watch Dog/Power-On Reset Timer
- 4K x 6-bit character generator ROM
- 160 x 7-bit video RAM
- On-chip oscillator that accepts a crystal, ceramic resonator, LC or external clock drive.
- Mask programmable 128 character set displayed in an 8-row by 20-column format, 12 by 15 pixel character cell, capable of supporting English, Korean, Chinese and Japanese high resolution characters.
- Fully programmable color attributes including row character, row background/fringes, frame background/position, bar graph color change, and character size.
- Programmable display position and character size control.
- One Pulse Width Modulator (14-bit resolution) for voltage synthesis tuner control.
- Five Pulse Width Modulators (8-bit resolution) for picture control.
- Seven Pulse Width Modulators (6-bit resolution) for audio control.
- Port 2 (8-bit programmable I/O) and Port 3 (2-bit input, 3-bit output) register mapped ports.
- Port 4 (8-bit output), Port 5 (8-bit LED drive output) and Port 6 (6-bit input and tri-state comparator AFC input) memory mapped I/O ports.

GENERAL DESCRIPTION

The Z86C27 and Z86C97 Digital Television Controller (DTC) introduce a new level of sophistication to single-chip architecture. The Z86C27/C97 are members of the Z8 single-chip microcontroller family with 8 Kbytes of ROM (Z86C27), ROMless (Z86C97) and 236 bytes of RAM. Both devices are housed in a 64-pin DIP package, and are CMOS compatible. Having the ROM/ROMless selectivity, the DTC offers both external memory and pre-programmed ROM which enables the Z8 microcontroller to be used in a high volume production application device embedded with a custom program (customer supplied program). The Z86C97 ROMless offers the use of external memory rather

than a preprogrammed ROM. This enables the Z8 microcontroller to be used in prototyping, low volume applications or where code flexibility is required. Zilog's DTC offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption. The device provides an ideal performance and reliability solution for consumer and industrial television applications.

The Z86C27/C97 architecture is characterized by utilizing Zilog's advanced Superintegration™ design methodology. The devices have an 8-bit internal data path controlled by a Z8 microcontroller, and On Screen Display (OSD) logic circuits/Pulse Width Modulators (PWM). On-chip peripherals include two register mapped I/O ports (Ports 2 and Port 3), Interrupt control logic (1 software, 2 external and 3 internal interrupts) and a standby mode recovery input port (Port 3, pin P30).

The OSD control circuits support 8 rows by 20 columns for 128 kinds of characters. The character color is specified by row. One of the 8 rows is assigned to show two kinds of colors for bar type displays such as volume control. The OSD is capable of displaying either low resolution (5x7 dot pattern) or high resolution (11x15 dot pattern) characters. The Z86C97 currently supports high resolution characters only.

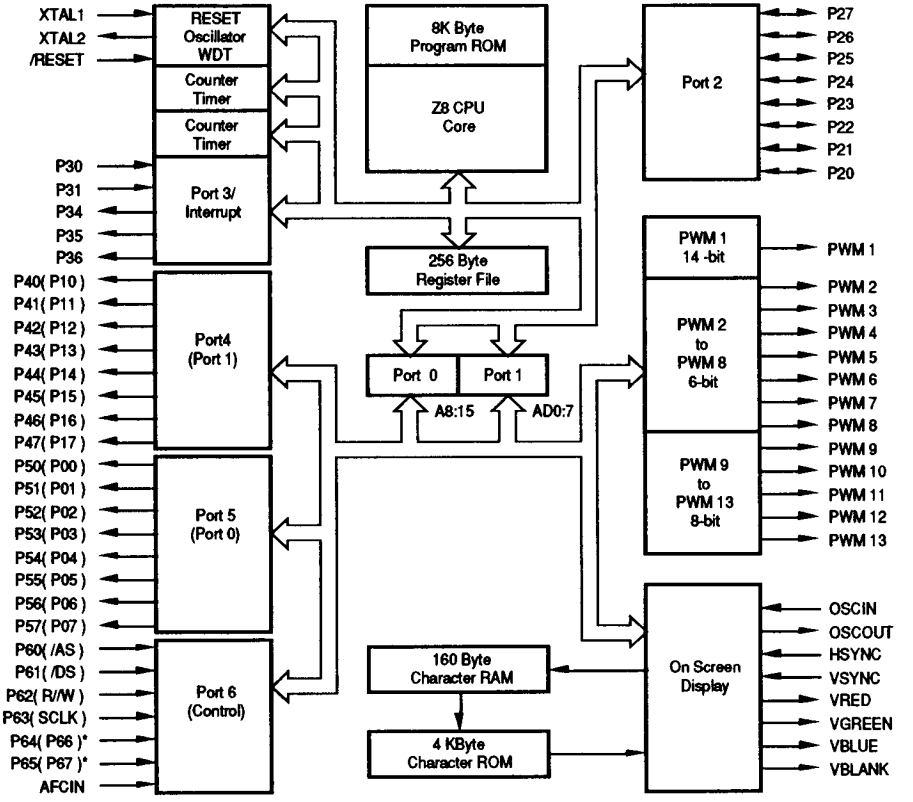
A 14-bit PWM port provides enough voltage resolution for a voltage synthesizer tuning system. Seven 6-bit PWM ports are used for controlling audio signal level. Five 8-bit PWM ports are used to vary picture levels.

The DTC applications demand powerful I/O capabilities. The Z86C27/C97 fulfills this with 35 I/O pins dedicated to input and output. These lines are grouped into five ports, and are configurable under software control to provide timing, status signals, parallel I/O and an address/data bus for interfacing to external memory.

There are three basic address spaces available to support this wide range of configurations: Program Memory, Register File and Data Memory. The Register File is composed of 236 bytes of general purpose register, two I/O Port registers and 15 control and status registers.

To unburden the program from coping with the real-time problems such as counting/timing and data communication, the DTC's offer two on-chip counter/timers with a large number of user selectable modes (Figure 1).

Note: All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only); /N//S (NORMAL and SYSTEM are both active Low).



* ( ) Denotes Z86C97 signal differences.

Figure 1. Functional Block Diagram

PIN CONFIGURATION

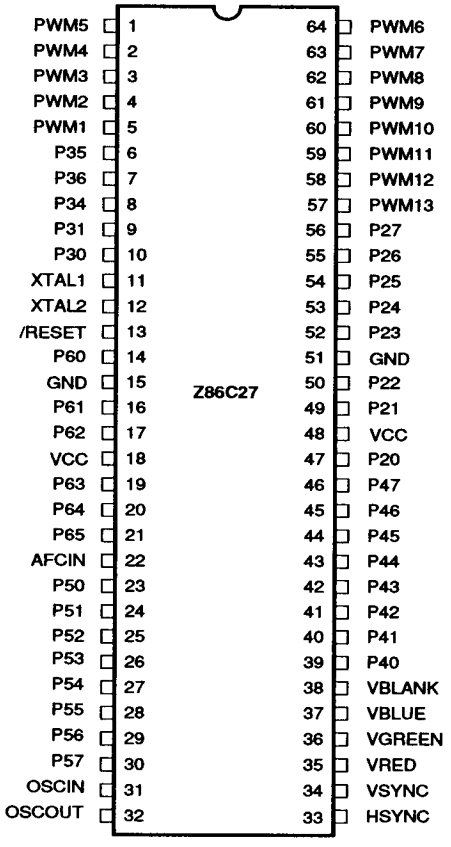


Figure 2. Z86C27 Mask-ROM Plastic DIP

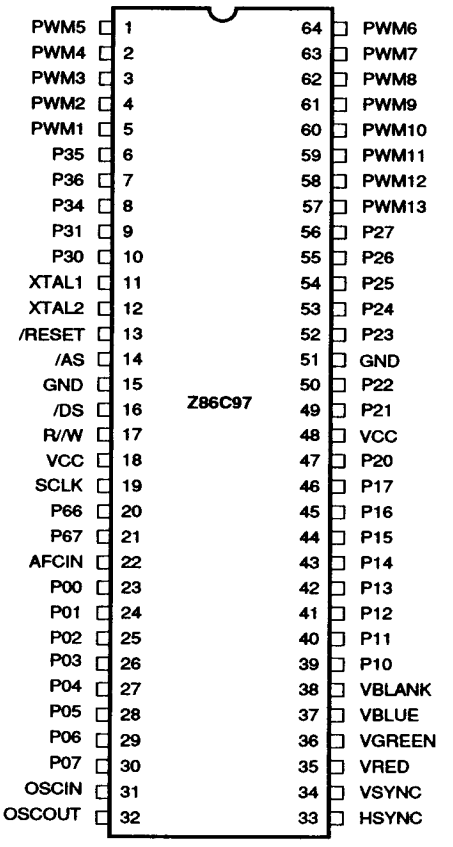


Figure 3. Z86C97 ROM-less Plastic DIP

PIN IDENTIFICATION
64-pin DIP Z86C27

Pin	Name	Function	Direction
1	PWM5	Pulse Width Modulator 5	Output
2	PWM4	Pulse Width Modulator 4	Output
3	PWM3	Pulse Width Modulator 3	Output
4	PWM2	Pulse Width Modulator 2	Output
5	PWM1	Pulse Width Modulator 1	Output
6, 7	P35-6	Port 3 pin 5, 6	Output
8	P34	Port 3 pin 4	Output
9	P31	Port 3 pin 1	Input
10	P30	Port 3 pin 0	Input
11	XTAL1	Crystal Oscillator	Input
12	XTAL2	Crystal Oscillator	Output
13	/RESET	System Reset	Input
14	P60	Port 6 pin 0	Input
15	GND	Ground,GND	Input
16	P61	Port 6 pin 1	Input
17	P62	Port 6 pin 2	Input
18	V_{cc}	Power Supply	Input
19-21	P63-5	Port 6 pin 3, 4, 5	Input
22	AFCIN	AFC Voltage Level	Input
23-30	P50-7	Port 5 pin 0, 1, 2, 3, 4, 5, 6, 7	Output
31	OSCIN	Video Dot Clock Osc	Input
32	OSCOUT	Video Dot Clock Osc	Output
33	HSYNC	Horizontal Sync	Input
34	VSYNC	Vertical Sync	Input
35	Vred	Video Red	Output
36	Vgreen	Video Green	Output
37	Vblue	Video Blue	Output
38	Vblank	Video Blank	Output
39-46	P40-7	Port 4 pin 0, 1, 2, 3, 4, 5, 6, 7	Output
47	P20	Port 2 pin 0	In/Output
48	V_{cc}	Power Supply	Input
49,50	P21-2	Port 2 pin 1, 2	In/Output
51	GND	Ground,GND	Input
52-56	P23-7	Port 2 pin 3, 4, 5, 6, 7	In/Output
57	PWM13	Pulse Width Modulator 13	Output
58	PWM12	Pulse Width Modulator 12	Output
59	PWM11	Pulse Width Modulator 11	Output
60	PWM10	Pulse Width Modulator 10	Output
61	PWM9	Pulse Width Modulator 9	Output
62	PWM8	Pulse Width Modulator 8	Output
63	PWM7	Pulse Width Modulator 7	Output
64	PWM6	Pulse Width Modulator 6	Output

PIN IDENTIFICATION (Continued)
64-pin DIP Z86C97

Pin	Name	Function	Direction
1	PWM5	Pulse Width Modulator 5	Output
2	PWM4	Pulse Width Modulator 4	Output
3	PWM3	Pulse Width Modulator 3	Output
4	PWM2	Pulse Width Modulator 2	Output
5	PWM1	Pulse Width Modulator 1	Output
6, 7	P35-6	Port 3 pin 5, 6	Output
8	P34	Port 3 pin 4	Output
9	P31	Port 3 pin 1	Input
10	P30	Port 3 pin 0	Input
11	XTAL1	Crystal Oscillator	Input
12	XTAL2	Crystal Oscillator	Output
13	/RESET	System Reset	Input
14	/AS	Address Strobe	Output
15	GND	Ground, GND	Input
16	/DS	Data Strobe	Output
17	R//W	Read/Write	Output
18	V_{cc}	Power Supply	Input
19	SCLK	System Clock	Output
20-21	P66-7	Port 6 pin 6, 7	Output
22	AFCIN	AFC Analog	Input
23-30	P00-7	Port 0 pin 0,1, 2, 3, 4, 5, 6, 7	Output
31	OSCIN	Video Dot Clock Oscillator	Input
32	OSCOUT	Video Dot Clock Oscillator	Output
33	Hsync	Horizontal Sync	Input
34	Vsync	Vertical Sync	Input
35	Vred	Video Red	Output
36	Vgreen	Video Green	Output
37	Vblue	Video Blue	Output
38	Vblank	Video Blank	Output
39-46	P10-7	Port 1 pin 0,1, 2, 3, 4, 5, 6, 7	Output
47	P20	Port 2 pin 0	In/Output
48	V_{cc}	Power Supply	Input
49-50	P21-2	Port 2 pin 1, 2	In/Output
51	GND	Ground,GND	Input
52-56	P23-7	Port 2 pin 3, 4, 5, 6, 7	In/Output
57	PWM13	Pulse Width Modulator 13	Output
58	PWM12	Pulse Width Modulator 12	Output
59	PWM11	Pulse Width Modulator 11	Output
60	PWM10	Pulse Width Modulator 10	Output
61	PWM9	Pulse Width Modulator 9	Output
62	PWM8	Pulse Width Modulator 8	Output
63	PWM7	Pulse Width Modulator 7	Output
64	PWM6	Pulse Width Modulator 6	Output

PIN DESCRIPTION

XTAL1, XTAL2. (Time-based input, output, respectively). These pins connect to the internal parallel-resonant clock crystal (4MHz max) oscillator circuit with 2 capacitors to GND. XTAL1 is also used as an external clock input.

/AS. *Address Strobe* (output, active Low) is pulsed once at the beginning of each machine cycle. Address output is via Port 0 and Port 1 for all external programs. Memory address transfers are valid at the trailing edge of /AS. Under program control, /AS can be placed in the high impedance state along with Port 0 and Port 1, Data Strobe and Read/Write.

/DS. *Data Strobe* (output, active Low) is active once for each external memory transfer. For READ operations, data must be available prior to the trailing edge of /DS. For WRITE operations, the falling edge of /DS indicates the output data is valid.

R/W. *Read/Write* (output, Write active Low) signal is low when the DTC is writing to the external program or data memory.

SCLK. *System Clock.* SCLK is the internal system clock. It can be used to clock external glue logic.

HSYNC. (input Schmitt triggered, CMOS level). Horizontal Sync is an input pin that accepts an externally generated Horizontal Sync signal of either negative or positive polarity.

VSYNC. (input Schmitt triggered, CMOS level). Vertical Sync is an input pin that accepts an externally generated Vertical Sync signal of either negative or positive polarity.

OSCIN, OSCOUT. (Video Oscillator input, output, respectively). Oscillator input and output pins for on-screen display circuits. These pins connect to an inductor and two capacitors to generate the character dot clock (typically around 6MHz). The dot clock frequency determines the character pixel width and phase synchronized to HSYNC.

Vblank. *Video Blank* (output). CMOS output, programmable polarity. Used as a superimpose control port to display characters from video RAM. The signal controls Y signal output of the CRT and turns off the incoming video display while the characters in video RAM are superimposed on the screen. The red, green, and blue outputs drive the three electron guns on the CRT directly, while the blank output turns off the Y signal.

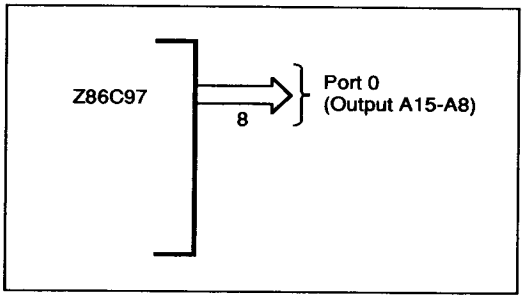
Vblue. *Video Blue* (output). CMOS Output of the Blue video signal (B-Y) and is programmable for either polarity.

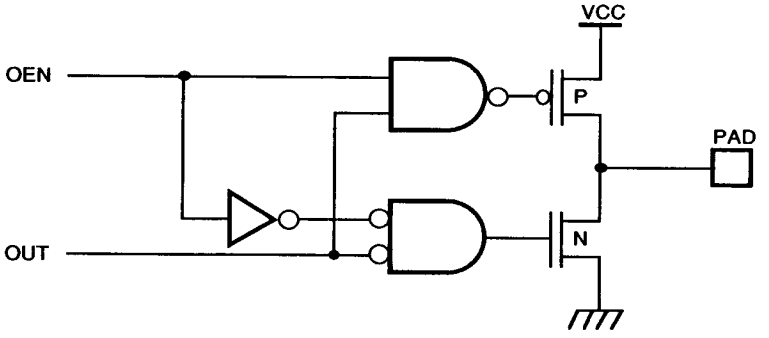
Vgreen. *Video Green* (output). CMOS Output of the Green video signal (G-Y) and is programmable for either polarity.

Vred. *Video Red* (output). CMOS Output of the Red video signal (R-Y) and is programmable for either polarity.

PIN DESCRIPTION (Continued)

Port 0 (P00-P07). Port 0 is an 8-bit, CMOS compatible, High Address Bus (A15-A8). In the ROMless mode this port is used to output the high order address (A15-A8) during an external memory cycle (Figure 4).





Note: Z86C97 Only

Figure 4. Port 0 Configuration

Port 1 (P10-P17). Port 1 is an 8-bit, CMOS compatible, Multiplexed Address/Data Bus (A7-A0)/(D7-D0). In the ROMless mode this port multiplexes the low order address (A7-A0 during /AS) and data (D7-D0 during /DS) for an external memory cycle (Figure 5).

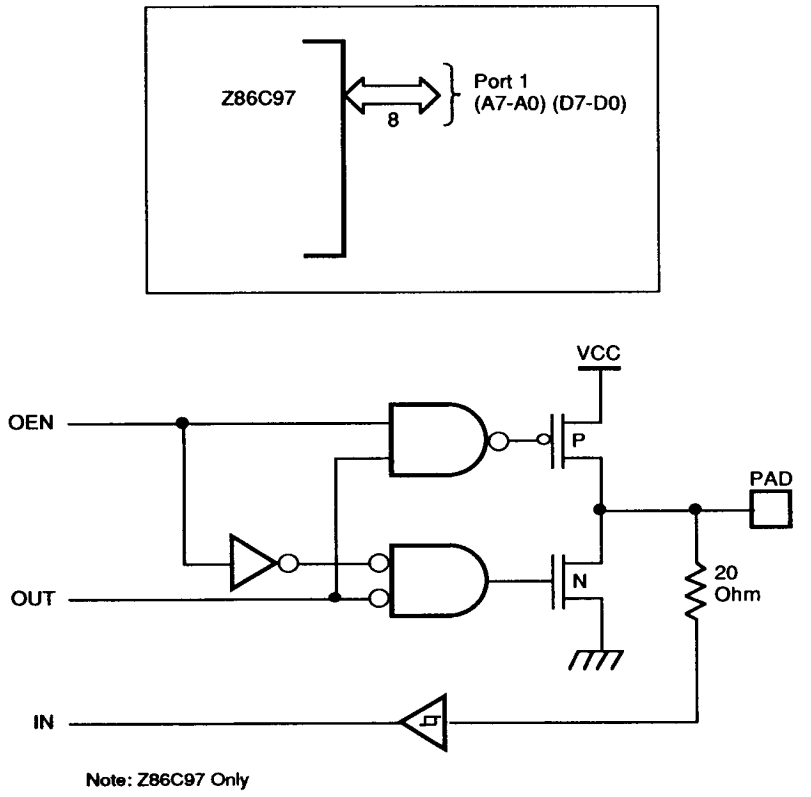
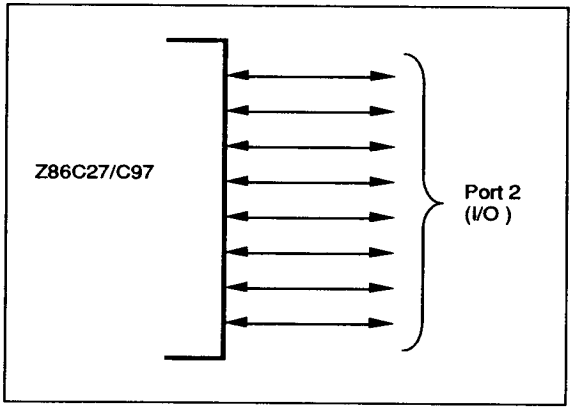
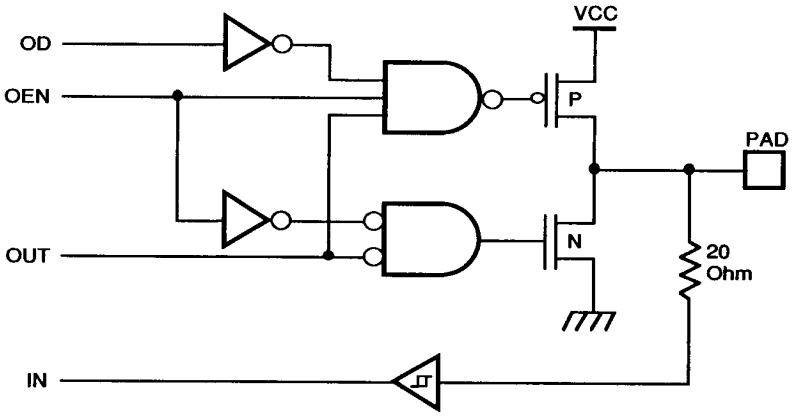


Figure 5. Port 1 Configuration

PIN DESCRIPTION (Continued)

Port 2 (P20-P27). Port 2 is an 8-bit port, CMOS compatible, bit programmable for either input or output. Input buffers are Schmitt triggered. Bits programmed as outputs may be globally programmed as either push-pull or open-drain (Figure 6).

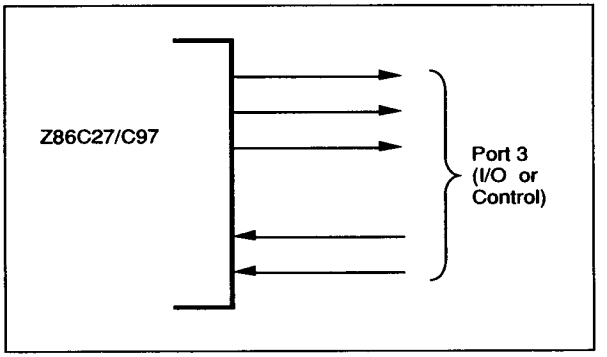


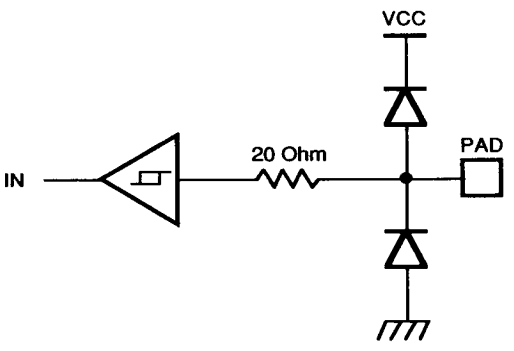


Note: Input/Output, 3-State, Open Drain, Pad Type 5

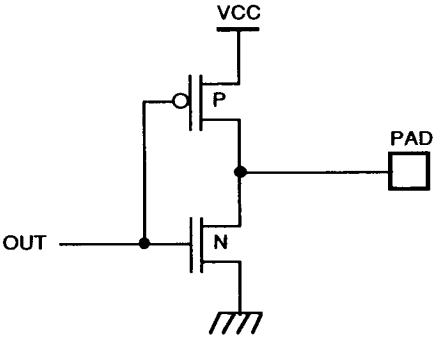
Figure 6. Port 2 Configuration

Port 3 (P30-1, P34-5 and P36). Port 3 Pin P30 input, is read directly. A negative edge event is latched in IRQ3 to initiate an IRQ3 vectored interrupt if appropriately enabled. An application could place the device in STOP mode when P30 goes low (in the IRQ3 interrupt routine). P30 initiates a STOP mode recovery when it subsequently goes high. Port 3, Pin P31 is read directly. A negative edge event is latched in IRQ2 to initiate an IRQ2 vectored interrupt if appropriately enabled. P31 high is signified as the T_{IN} signal to Timer1. Port 3, Pin P34 and Pin P35 are general purpose output lines. Port 3, Pin P36 can be used as a general purpose output or as an output for T_{OUT} (from Timer1 or Timer2) or SCLK (Figure 7).





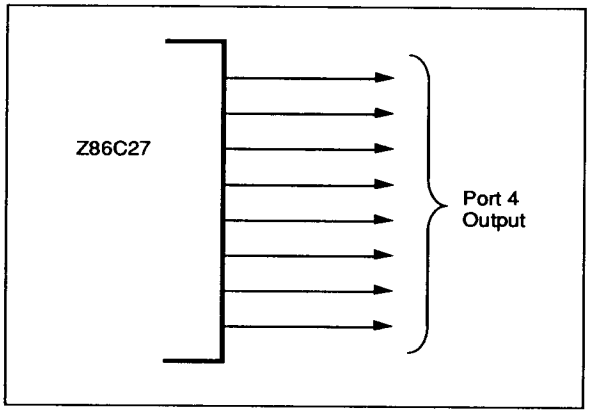
Note: Input Only, Schmitt-triggered, Pad Type 2

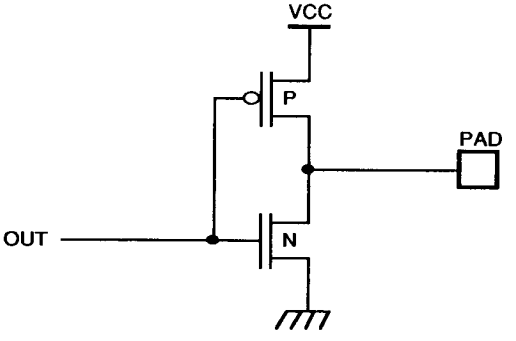


Note: Output Only, Pad Type 3

Figure 7. Port 3 Configuration

Port 4 (P40-P47). Port 4 is an 8-bit, CMOS compatible, Output Port (Figure 8).

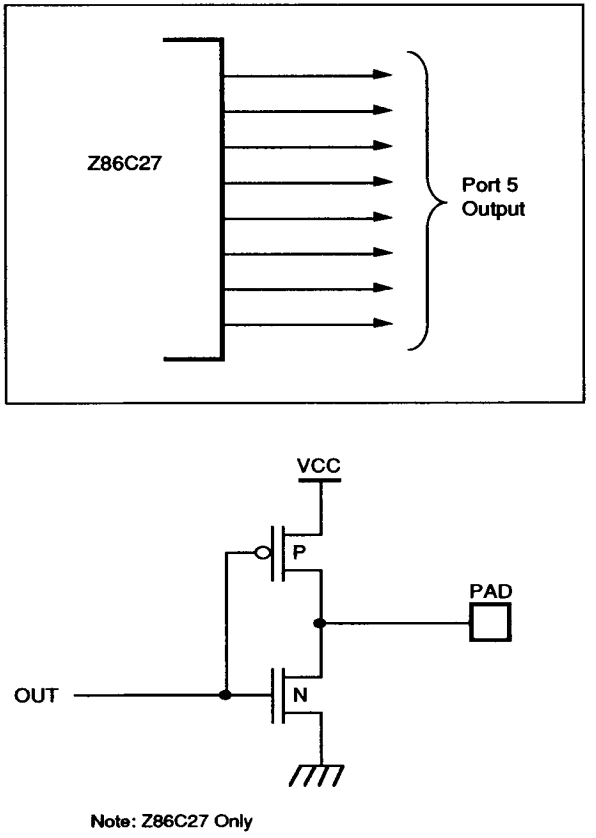




Note: Z86C27 Only

Figure 8. Port 4 Configuration

Port 5 (P50-P57). Port 5 is an 8-bit, CMOS compatible, Output Port. The output ports can directly sink 10 mA at 1.5 Volt V_{OL}. They are typically used to drive multiplexed LED displays (Figure 9).



Note: Z86C27 Only

Figure 9. Port 5 Configuration

Port 6 (P60-P65). Port 6 is a 6-bit, Schmitt triggered CMOS compatible, input port. The outputs of the AFC comparators internally feed into the Port 6, bit-6 and bit-7 inputs in ROM mode. In ROMless mode, pins 20 and 21 bring out the internal comparator outputs for Port 6, bit-6 and bit-7 emulation (Figure 10).

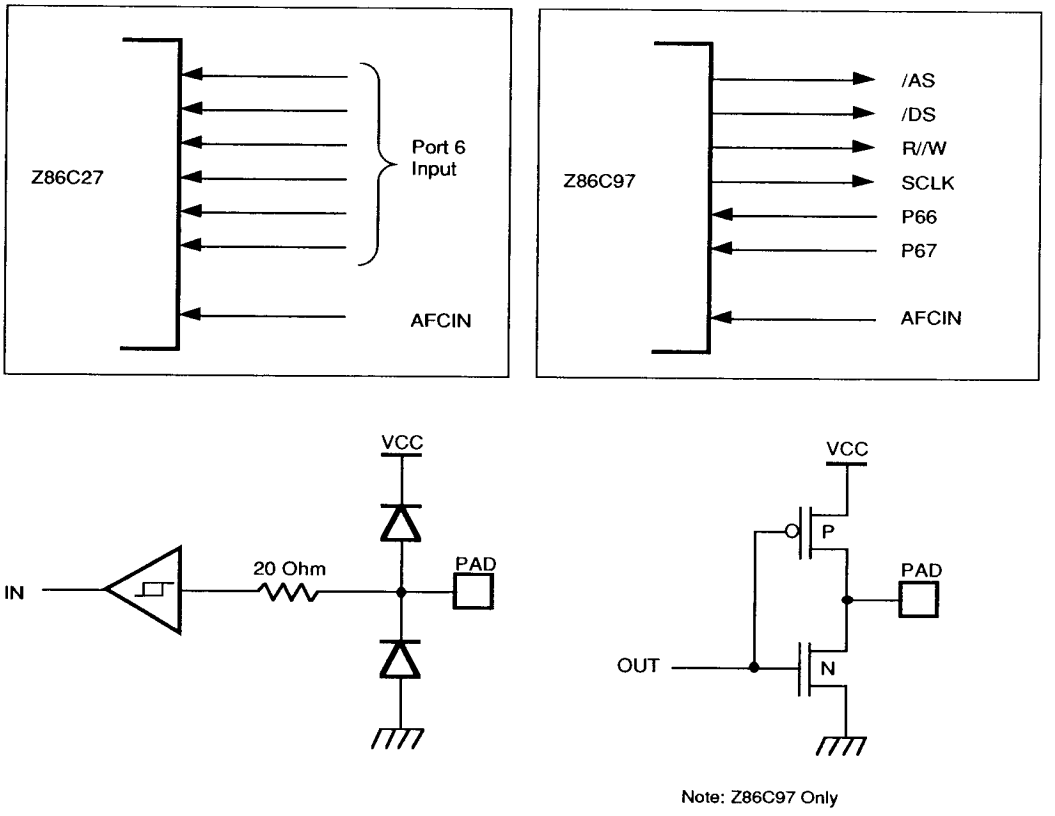


Figure 10. Port 6 Configuration

AFCIN. (Comparator input port, memory mapped). The input signal is supplied to two comparators with VTH1=2/5 V_{cc} and VTH2=3/5 V_{cc} typical threshold voltage. The comparator outputs are internally connected to Port 6, bit-6 and bit-7. AFCIN is typically used to detect AFC voltage level to accommodate digital automatic fine tuning functions. For Z86C97 Port 6, bit-6 and bit-7 are external outputs through pin 20 and pin 21 (Figure 11).

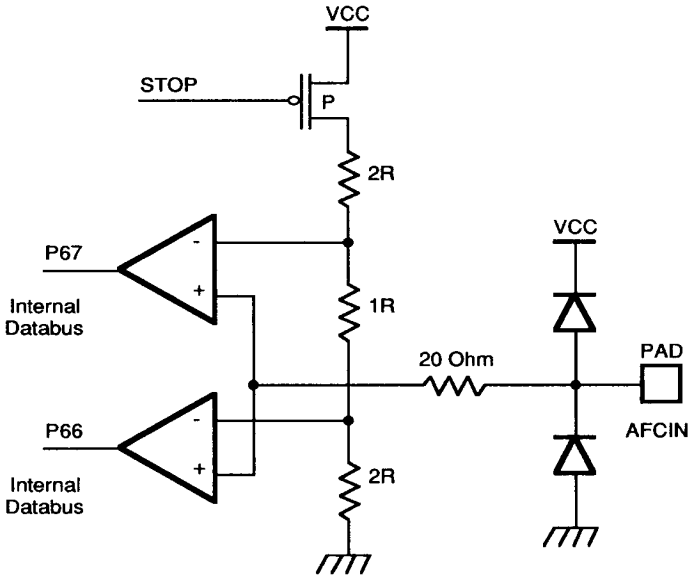


Figure 11. AFCIN Comparator Circuits

PIN DESCRIPTION (Continued)

Pulse Width Modulator 1 (PWM). PWM1 is typically used as the D/A converter for Voltage Synthesis Tuning systems.

Pulse Width Modulator 2-8 (PWM). PWM2-PWM8 are Pulse Width Modulators with 6-bit resolution.

Pulse Width Modulator 9-13 (PWM). PWM9-PWM13 are Pulse Width Modulator circuits with 8-bit resolution or individually programmed as general purpose outputs. In either case, the output drivers are 12-volt open-drain circuits.

/RESET. System Reset. Code is executed from memory address 000C (HEX) after the /RESET pin is set to a high level. The reset function is also carried out by detecting a V_{cc} transition state (automatic power on reset) so that the external reset pin can be permanently tied to V_{cc}. A low level on /RESET forces a restart of the device.

SPECIAL FUNCTIONS

The Z8 DTC incorporates special functions to enhance the Z8's application in consumer, industrial and television control applications.

Pulse Width Modulator (PWM). The DTC has thirteen PWM channels (Figure 12). There are three types of PWM circuits: PWM1 (1 channel of 14-bit resolution) typically used for Voltage Synthesis Tuning, PWM2-PWM8 (7 channels of 6-bit resolution) typically used for audio level control, and PWM9-PWM13 (5 channels of 8-bit resolution) typically used for picture level control. The PWM control registers are mapped into external memory and are accessed via LDE and LDEI instructions.

On Screen Display (OSD). The OSD has a capability of displaying 8 rows by 20 columns of 128 kinds of characters for either high resolution (11x15 dots) or low resolution (5x7 dots) pattern (Figure 13).

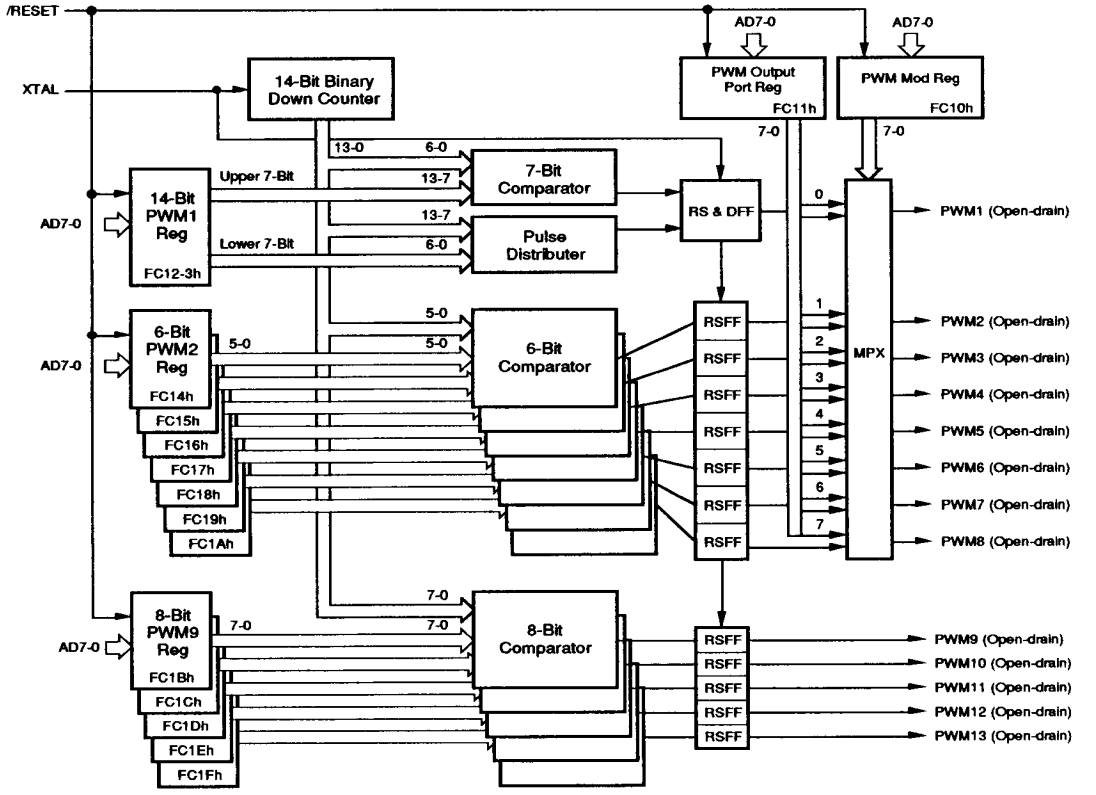


Figure 12. Pulse Width Modulator Block Diagram

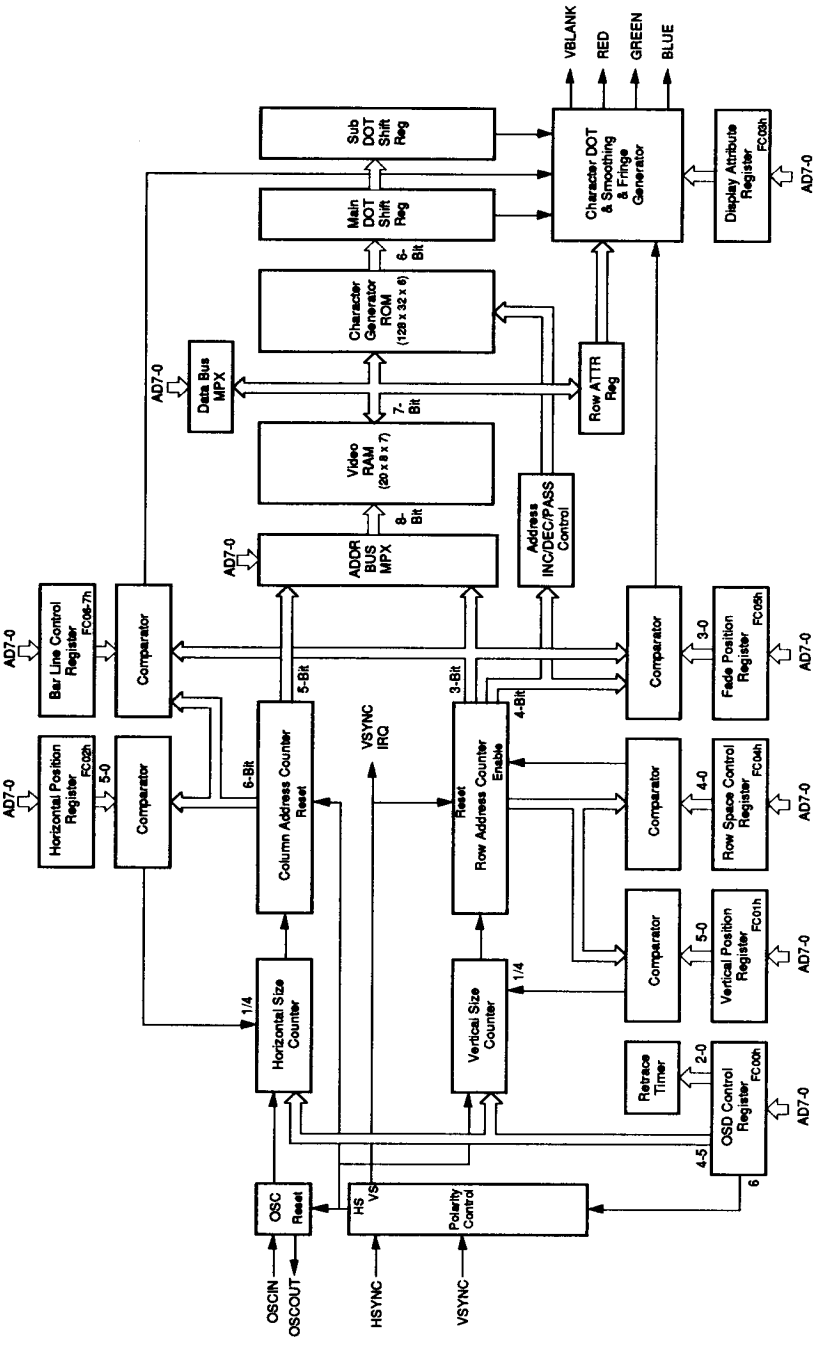


Figure 13. On-Screen-Display Block Diagram

The OSD features are as follows:

- Character Color: Seven kinds of color are specified on a row basis.
- Character Pixel Size: Four character pixel sizes are selected for a low resolution (2HL, 4HL, 6HL and 8HL) and high resolution (1HL, 2HL, 3HL and 4HL) Horizontal Line (HL).
- Polarity Selections: Can select active low or high for horizontal/vertical sync input and RGB outputs.
- Display Position: Can display 64 vertical positions by 4HL units and 64 horizontal positions by a 4 dot clock.
- Inter Row Spacing: Inter row vertical line spacing is set from 2HL to 25HL (17HL for high resolution).
- Fade In/Out Control: Fade position can be determined in vertical direction.
- Bar Line Type Display: One of the rows is selected to display an analog bar line every half column by setting second color with proper character set.
- Fringe Function: Fringe off/on and the color selected.
- Background Color: Eight kinds of color including black background color.
- ON/OFF Control: Character display, backgrounds are turned on and off.
- Number of Display Characters: 8 rows x 20 columns.
- Character Set: 128 (5x7 dots or 11x15 dots).

Character Generator ROM. The character generator ROM is organized as 4 Kbytes of 6 bits. The ROM defines either 11x15 dot (high resolution) or 5x7 (low resolution) characters (Figure 14).

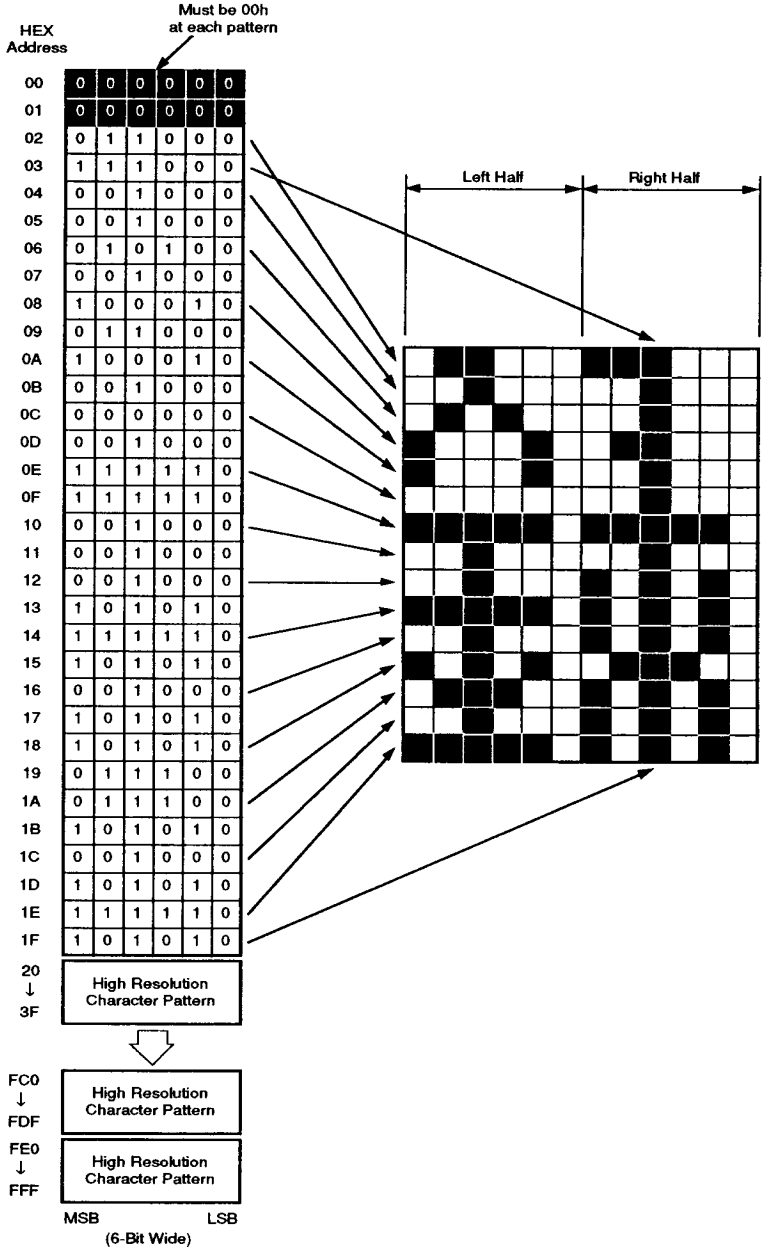


Figure 14a. High and Low Resolution Character ROM Configuration

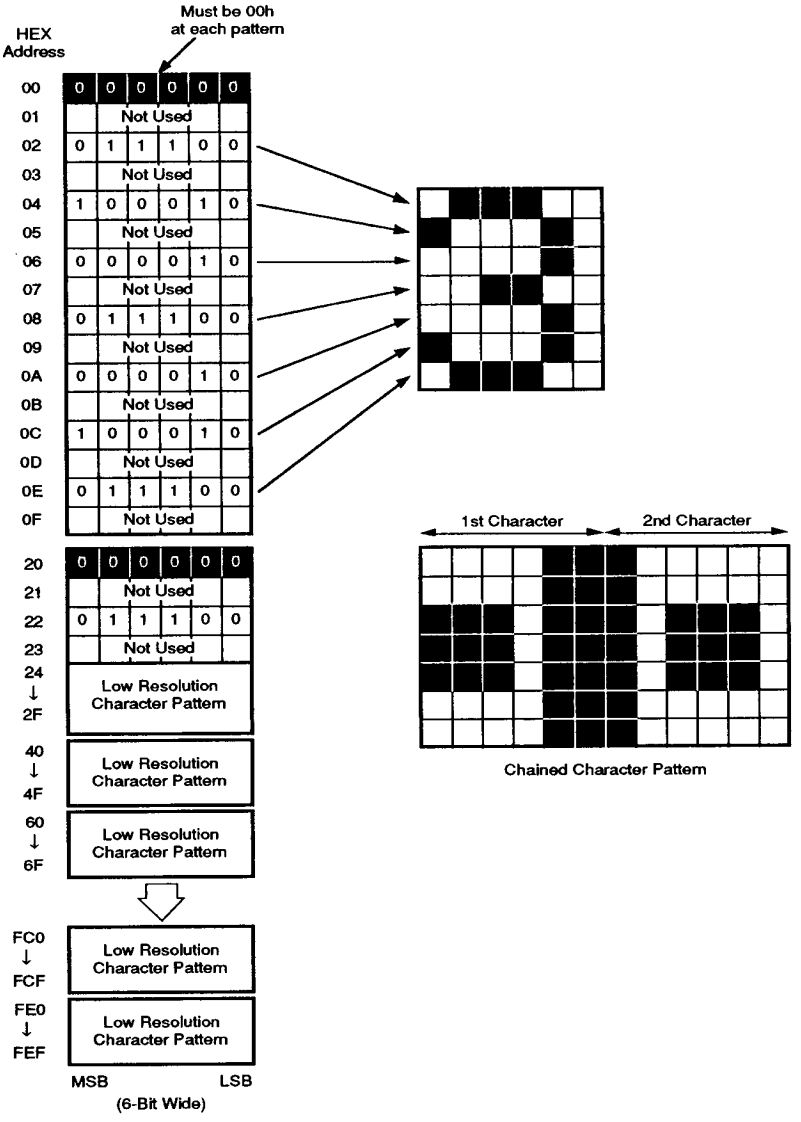


Figure 14b. High and Low Resolution Character ROM Configuration

SPECIAL FUNCTIONS (Continued)

Program Memory. The program ROM size is 8K bytes (Figure 15). The IRQ vector table is located in the lower address space. The vector address is fetched after the corresponding interrupt and program control is passed to the specified vector address. IRQ1 vector is fixed to VSYNC interrupt request and occurs at the leading edge of the filtered VSYNC input. Program memory start at address 000C (HEX) after reset.

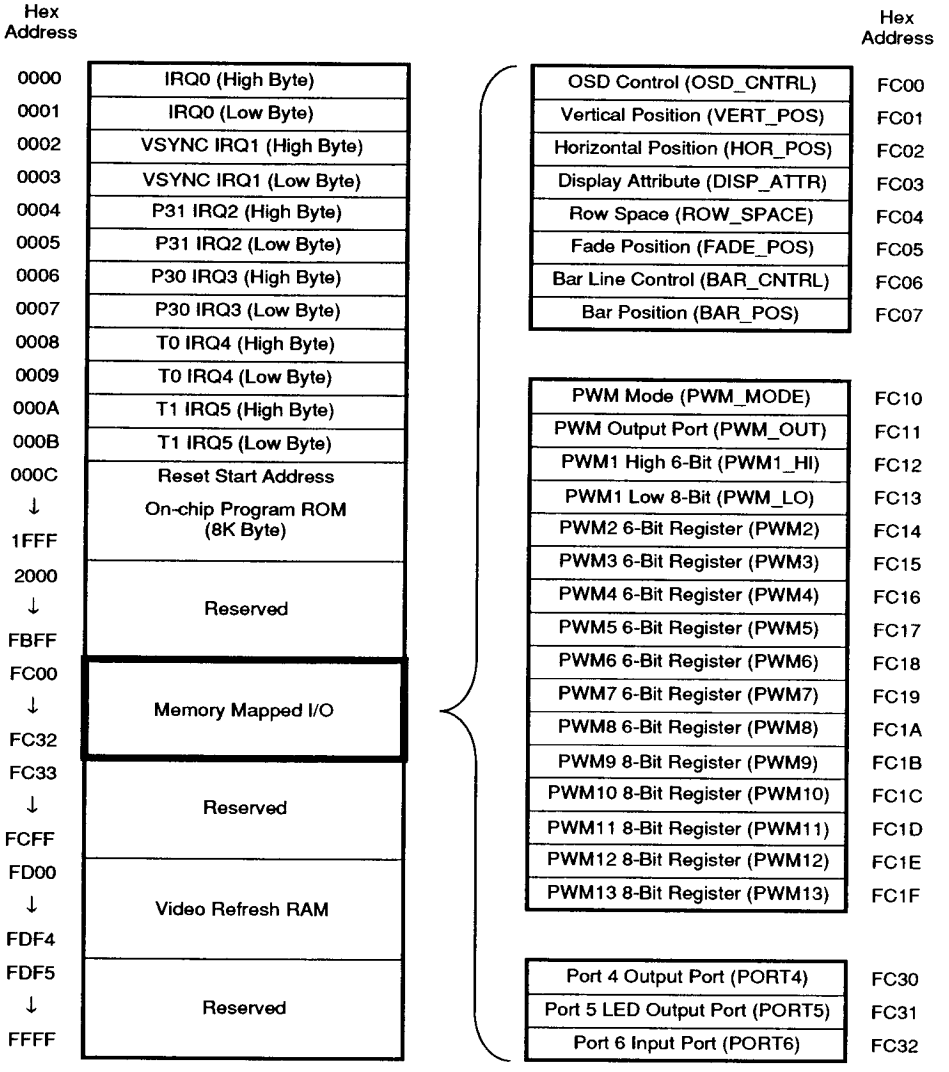


Figure 15. Program Memory

Memory Mapped Register. All control registers and I/O ports (except Port 2 and Port 3) are assigned to program memory space. Address space FC00 (HEX) contains OSD control registers, PWM output registers and Ports 4, 5 and 6 I/O registers. Two bits of the decoded AFCIN port are assigned to Port 6 input port. LDE and LDEI instructions are required to transfer data between the Register File and the Memory Mapped Registers.

Data Memory (/DM). The Z86C27/C97 can address up to 64K bytes of program memory, and 56K bytes of external data memory. External data memory may be included with or separated from the external program memory space. /DM, an optional I/O signal that can be programmed to appear on Port 3 Pin P34, distinguishes between data and program memory space.

Register File. A total of 253 byte registers are implemented in the Z8 core. Address 00 (HEX), 01 (HEX) and F0 (HEX) are reserved. The register file consists of 2 I/O Port registers, 236 general-purpose registers and 15 control and status registers (Figure 16). The instructions can access registers directly or indirectly with an 8-bit address field. This also allows short 4-bit register addressing using the Register Pointer. In the 4-bit mode, the register file is divided into sixteen working-register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group (Figure 17).

Note: Register Bank E0-EF is only accessed through a working register and indirect addressing modes.

Hex Address	
00	Port 0 (Internal)
01	Port 1 (Internal)
02	Port 2 (P2)
03	Port 3 (P3)
04	General - Purpose Registers
EF	
F0	Reserved
F1	Timer Mode (TMR)
F2	Timer/Counter1(T1)
F3	T1 Prescaler (PRE1)
F4	Timer/Counter0 (T0)
F5	T0 Prescaler (PRE0)
F6	Port 2 Mode (P2M)
F7	Port 3 Mode (P3M)
F8	Port 0-1 Mode (P01M)
F9	Interrupt Priority Reg (IPR)
FA	Interrupt Request Reg (IRQ)
FB	Interrupt Mask Reg (IMR)
FC	Condition Flag (FLAGS)
FD	Register Pointer (RP)
FE	Stack Pointer High (SPH)
FF	Stack Pointer Low (SPL)

Figure 16. Register File Configuration

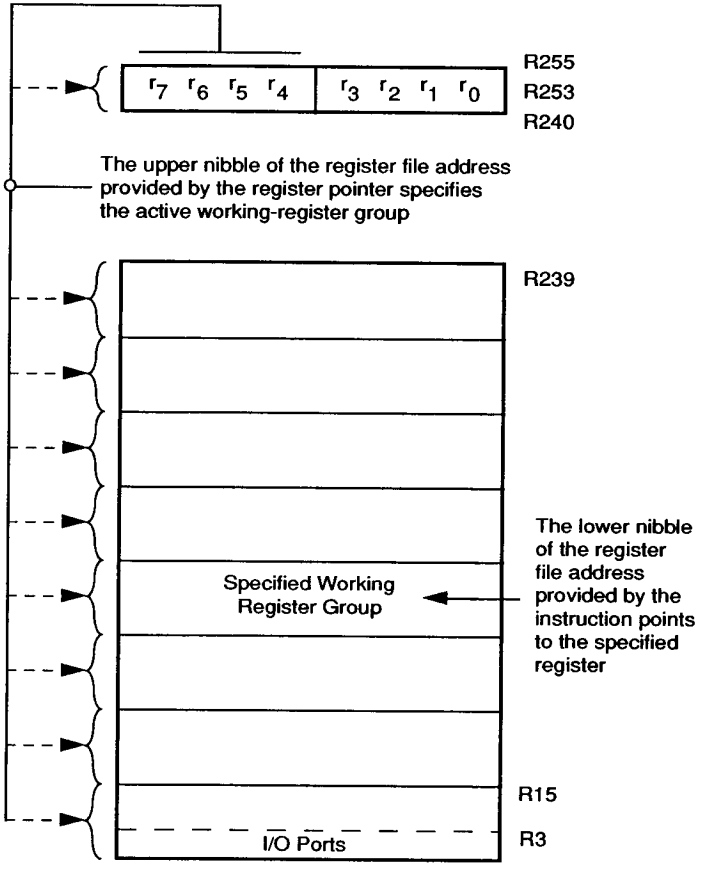


Figure 17. Register Pointer

Stack. Either the internal register file or the external data memory is used for the stack. A 16-bit Stack Pointer is used for the external stack, which can reside anywhere in data memory. An 8-bit Stack Pointer is used for the internal stack that resides within the 236 general-purpose registers.

Counter/Timers. There are two 8-bit programmable counter/timers (T0-T1), each driven by its own 6-bit programmable prescaler (PRE0 and PRE1). The T1 prescaler can be driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (Figure 18).

The counter, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is the internal microprocessor clock (XTAL clock/4), or an external signal input via Port 3, P31. The counter/timers are programmably cascaded by connecting the T0 output to the input of T1.

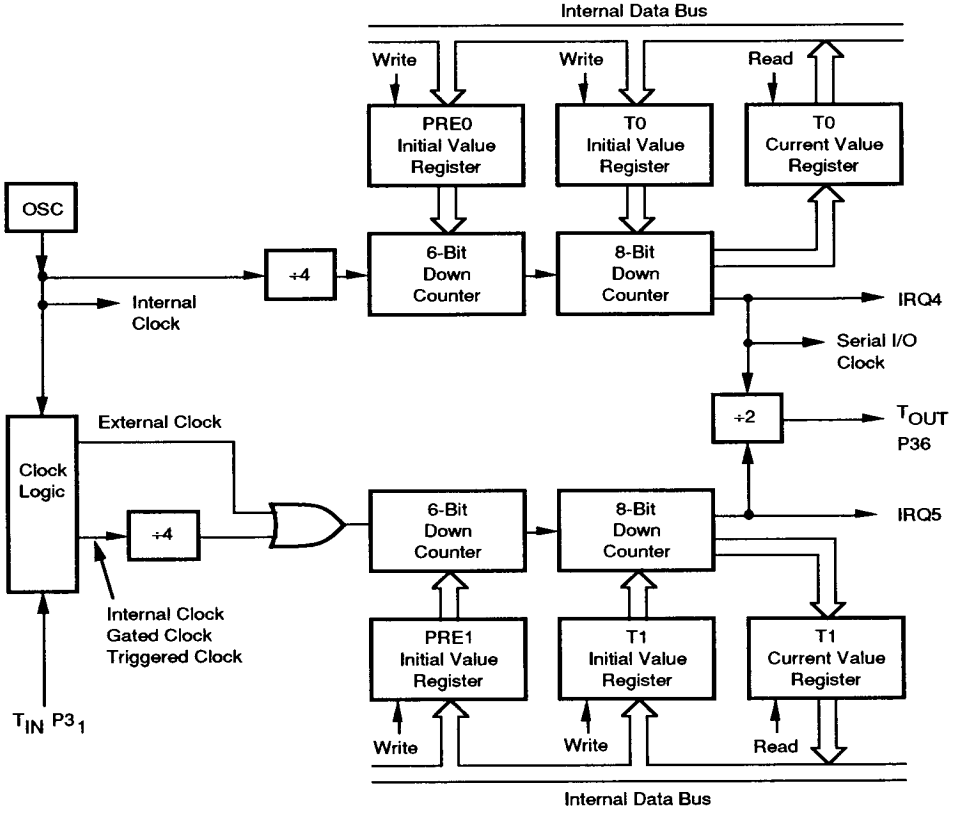


Figure 18. Counter/Timer Block Diagram

SPECIAL FUNCTIONS (Continued)

Interrupts. The DTC has six different interrupts from six different sources. These interrupts are maskable and prioritized (Figure 19). The six sources are divided as follows: two sources are claimed by Port 3 (P30, P31), one by VSYNC, two by the counter/timers, and one is software triggered only.

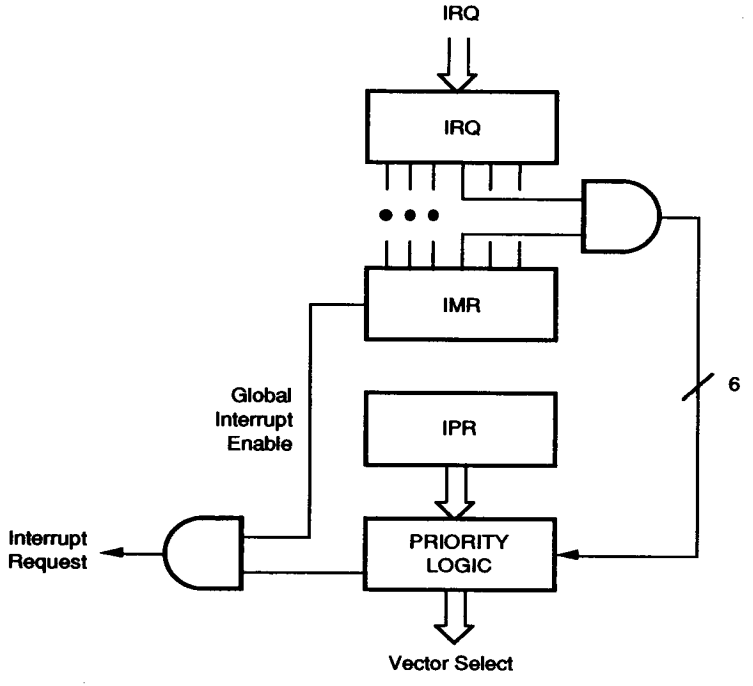


Figure 19. Interrupt Block Diagram

HALT Mode. The Z86C27/C97 is driven by two internal clocks, TCLK and SCLK, They both oscillate at the crystal frequency. TCLK provides the clock signal for the counter-timers and the interrupt block. SCLK provides the clock signal for all other CPU blocks. Halt mode turns off the internal CPU clock (SCLK), but not the XTAL oscillation. The counter/timers and external interrupts remain active. The device may be recovered by interrupts, either external or internally generated.

STOP Mode. The STOP instruction stops crystal oscillation, thereby stopping both SCLK and TCLK. The device ceases to operate. The STOP mode can be released by two methods. The first method is to reset the device. A high input condition on Port 3 Pin P30 is the second method. After releasing the STOP mode by using either one of the two methods, program execution begins at location %000C (HEX). To complete an instruction prior to entering the standby modes, a NOP instruction has to be placed before the HALT or STOP instructions. This is required because of instruction pipelining. i.e.:

```
FF NOP    ; clear the pipeline
6F STOP   ; enter STOP mode
          or
FF NOP    ; clear the pipeline
7F HALT   ; enter HALT mode
```

Notes:
In STOP mode, XTAL2 pin has an internal pull-up on it and OSCOUT has an internal pull-down.

Clock. The Z86C27/C97 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal is an AT cut, parallel resonant, 4 MHz max with a series resistance (RS) less than or equal to 100 Ohms.

The crystal source is connected across XTAL1 AND XTAL2 using the recommended capacitors (10 pF < CL < 300 pF, where C1=C2=CL) from each pin to ground (Figure 20).

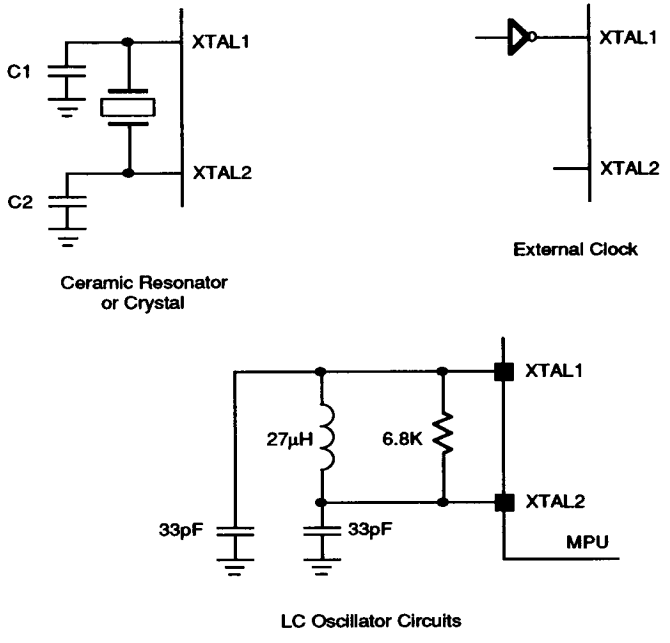


Figure 20. Oscillator Configuration

SPECIAL FUNCTIONS (Continued)

Watch Dog Timer (WDT). The Z86C27/C97 is equipped with a watch dog timer which should be refreshed within 12 ms. Failure to refresh the timer results in a reset of the device. The WDT is enabled the first time that a WDT 5F (HEX) instruction is executed. Every subsequent WDT instruction retriggers the timer. The watch dog timer may or may not be enabled during the HALT mode. The instruction WDH 4F (HEX) enables the timer during HALT mode. If the HALT mode is not released and the watch dog timer is not retriggered (by the WDT instruction) within 12 ms, a device reset occurs.

V_{cc} Voltage Sensitive Reset (VSR). Reset is globally driven if V_{cc} is below the specified voltage (Figure 21).

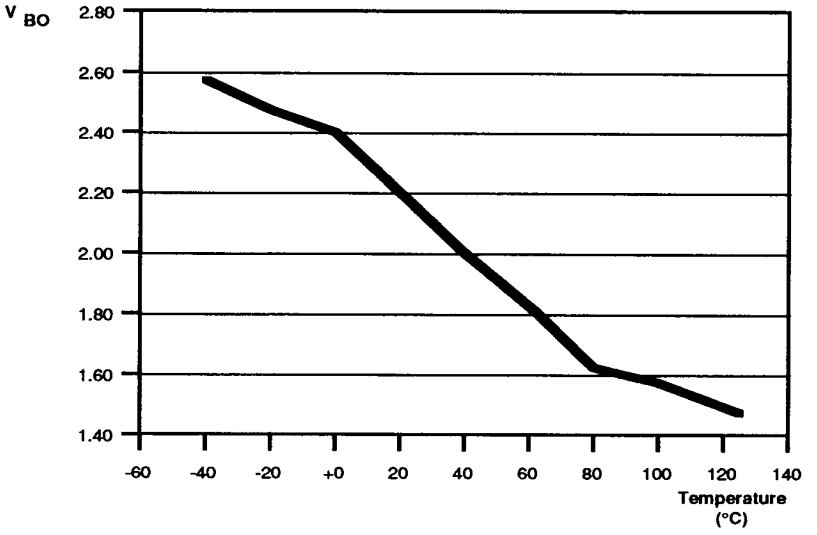


Figure 21. Voltage Sensitive Reset Vs Temperature

ABSOLUTE MAXIMUM RATINGS

Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameters	Min	Max	Units	Notes
V_{CC}	Power Supply Voltage †	-0.3	+7	V	
V_i	Input Voltage	-0.3	V_{CC}+0.3	V	
V_I	Input Voltage	-0.3	V_{CC}+0.3	V	[1]
V_O	Output Voltage	-0.3	V_{CC}+8.0	V	[2]
I_{OH}	Output Current High		-10	mA	1 pin
I_{OH}	Output Current High		-100	mA	all total
I_{OL}	Output Current Low		20	mA	1 pin
I_{OL}	Output Current Low		40	mA	[3] (1 pin)
I_{OL}	Output Current Low,all total		200	mA	
T_A	Operating Temperature	††			
T_{STG}	Storage Temperature	-65	+150	C	

Notes:
[1] Port 2 open-drain
[2] PWM open drain outputs
[3] Port 5

† Voltage on all pins with respect to GND.
†† See Ordering Information

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 22).

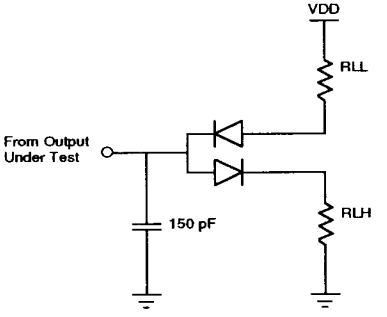


Figure 22. Test Load Diagram

CAPACITANCE

T_A=25°C, V_{CC}=GND=0V, Freq=1.0 MHz, unmeasured pins to GND.

Parameter	Max	Units
Input capacitance	10	pF
Output capacitance	20	pF
I/O capacitance	25	pF
AFCin input capacitance	10	pF

DC CHARACTERISTICS

T_A=0°C to +70°C; V_{CC}=+4.5V to +5.5V; F_{OSC}=4 MHz

Symbol	Parameter	T_A=0°C to 70°C Min	Max	Typical @ 25°C	Units	Conditions
V_{IL}	Input Voltage Low	0	0.2 V_{CC}	1.48	V	
V_{ILC}	Input XTAL/Osc In Low		0.07 V_{CC}	0.98	V	External Clock Generator Driven
V_{IH}	Input Voltage XTAL/Osc In High	0.7 V_{CC}	V_{CC}	3.2	V	External Clock Generator Driven
V_{IHC}	Input XTAL/Osc in High	0.8 V_{CC}	V_{CC}	3.0	V	External Clock Generator Driven
V_{HY}	Schmitt Hysteresis	0.1 V_{CC}		0.8	V	
V_{PU}	Maximum Pull-up Voltage		12		V	[2]
V_{OL}	Output Voltage Low		0.4	0.16	V	I_{OL}=1.00mA
			0.4	0.19	V	I_{OL}=3.2mA, [1]
			0.4	0.19	V	I_{OL}=0.75mA [2]
			1.5	1.00	V	I_{OL}=10mA [1]
V_{00-01}	AFC Level 01 In		0.45 V_{CC}	1.9	V	
V_{01-11}	AFC Level 11 In	0.5 V_{CC}	0.75 V_{CC}	3.12	V	
V_{OH}	Output Voltage High	V_{CC}-0.4		4.75	V	I_{OH}=-0.75mA
I_{IR}	Reset Input Current		-80	-46	µA	V_{RL}=0V
I_{IL}	Input Leakage	-3.0	3.0	0.01	µA	0V,V_{CC}
I_{OL}	Tri-State Leakage	-3.0	3.0	0.02	µA	0V,V_{CC}
I_{CC}	Supply Current		20	13.2	mA	All inputs at rail
I_{CC1}			6	3.2	mA	All inputs at rail
I_{CC2}			10	0	µA	All inputs at rail

Notes:
[1] Port 5
[2] PWM Open Drain

AC CHARACTERISTICS

Timing Diagrams

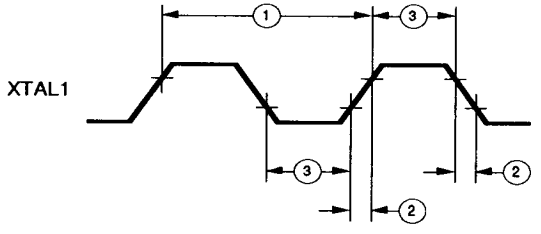


Figure 23. External Clock

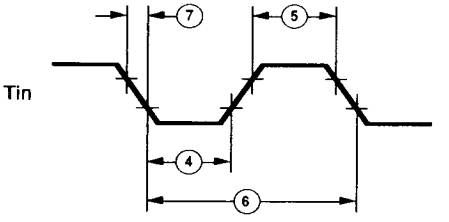


Figure 24. Counter Timer

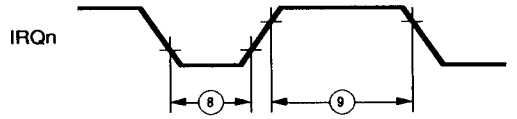


Figure 25. Interrupt Request

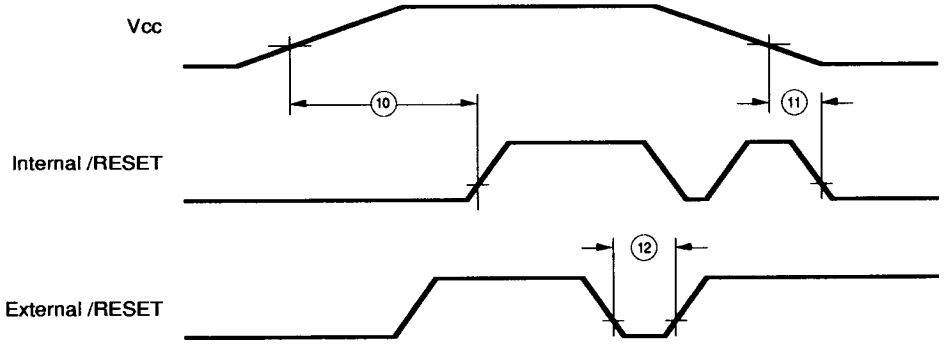


Figure 26. Power On Reset

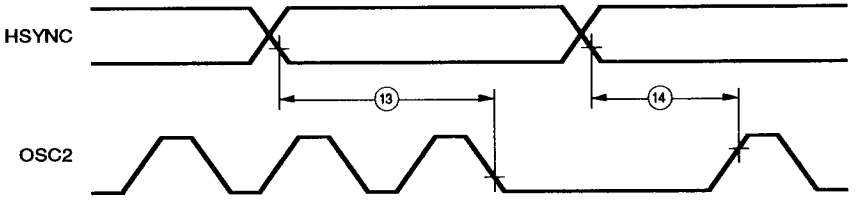


Figure 27. On Screen Display

AC CHARACTERISTICS

T_A=0° C to 70° C; V_{CC}=+4.5V to +5.5V; F_{OSC}=4 MHz,

No	Symbol	Parameter	Min	Max	Unit
1	TpC	Input clock period	250	1000	ns
2	TrC,TfC	Clock input raise and fall		15	ns
3	TwC	Input clock width	70		ns
4	TwTinL	Timer input low width	70		ns
5	TwTinH	Timer input high width	3TpC		
6	TpTin	Timer input period	8TpC		
7	TrTin,TfTin	Timer input raise and fall		100	ns
8A	TwIL	Int req input low	70		ns
8B	TwIL		3TpC		
9	TwIH	Int request input high	3TpC		
10	TdPOR	Power On Reset delay	25	100	ms
11	TdLVIRES	Low voltage detect to In-Internal RESET condition	200		ns
12	TwRES	Reset minimum width	5TpC		
13	TdHsOl	Hsync start to Vosc stop	2TpV	3TpV	
14	TdHsOh	Hsync end to Vosc start		1TpV	
15	TdWDT	WDT Refresh Time		12	ms

Notes:
[1] Refer to DC Characteristics for details on switching levels.

* Units in nanoseconds

AC CHARACTERISTICS

Unique to Z86C97 External Memory Read/Write Timing Diagram

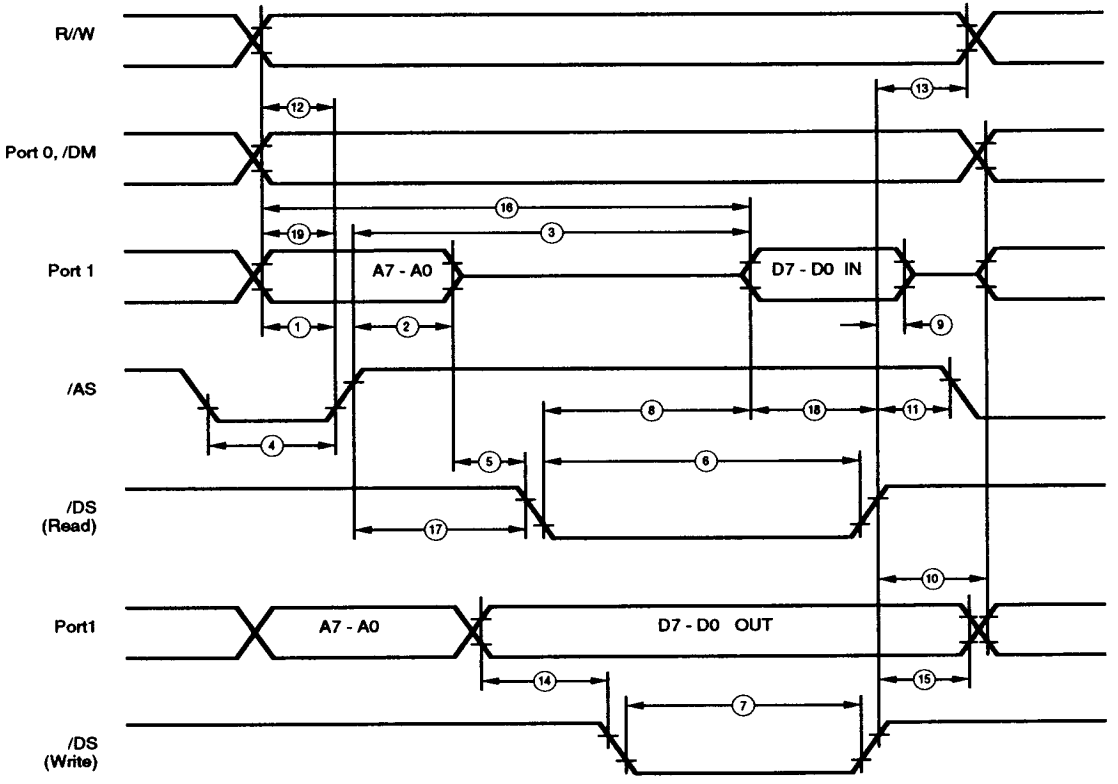


Figure 28. Z86C97 External Memory Read/Write Timing

AC CHARACTERISTICS

Unique to Z86C97, T_A=0°C to 70°C; V_{CC}=+4.5V to +5.5V; F_{OSC} = 4 MHz

No	Symbol	Parameter	Min	Max	Unit	Notes
1	TdA(AS)	Address Valid to /AS High Delay	35		ns	[2]
2	TdAS(AS)	/AS High to Address Float Delay	45		ns	[2]
3	TdAS(DR)	/AS High to Read Data Required Valid		250	ns	[1,2]
4	TwAS	/AS Low Width	55		ns	[2]
5	TdAZ(DS)	Address Float to /DS Low	0		ns	[2]
6	TwDSR	/DS (Read) Low Width	185		ns	[1,2]
7	TwDSW	DS (Write) Low Width	110		ns	[1,2]
8	TdDSR(DR)	/DS Low to Read Data Required Valid		130	ns	[1,2]
9	ThDR(DS)	Read Data to /DS High Hold		5	ns	
10	TdDS(A)	/DS High to Address Active Delay	55		ns	[2]
11	TdDS(AS)	/DS High to /AS Low Delay	55		ns	[2]
12	TdR/W(AS)	R//W Valid to /AS High Delay	35		ns	[2]
13	TdDS(R/W)	/DS High to R//W Not Valid	55		ns	[2]
14	TdDW(DSW)	Write Data Valid to /DS Low Delay	35		ns	[2]
15	TdDS(DW)	/DS High to Write Data Not Valid	55		ns	[2]
16	TdA(DR)	Address Valid to Read Data Required Valid		330	ns	[1,2]
17	TdAS(DS)	/AS High to /DS Low Delay	65		ns	[2]
18	TdDI(DS)	Data Input Setup to /DS High	75		ns	[1]

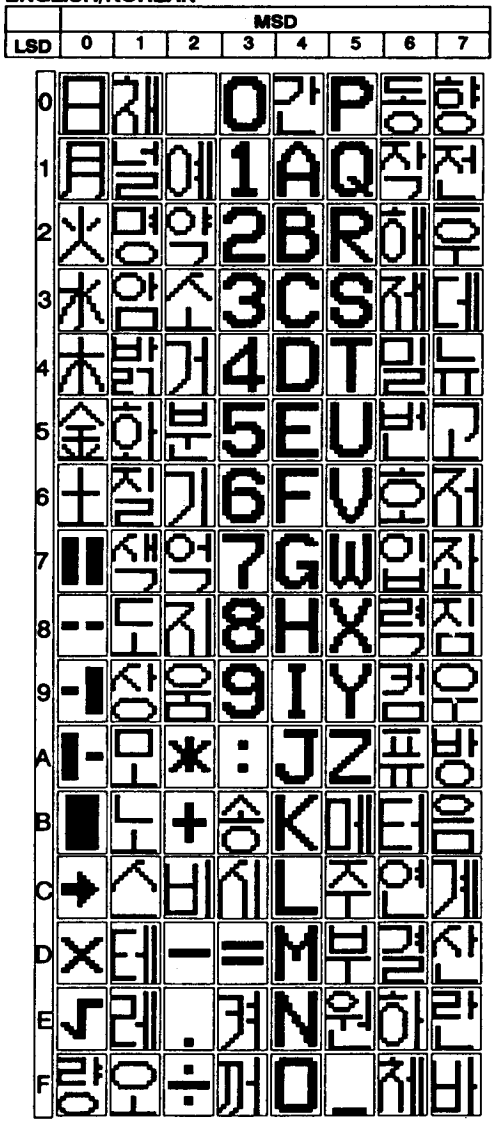
Notes:

[1] When using extended memory timing, for parameters 3, 6, 7, 8, and 16, add 2TpC (250 ns @ 4.0 MHz).

[2] Min and Max times are in nanoseconds unless otherwise noted.

STANDARD CHARACTER SETS

ENGLISH/KOREAN



SUMMARY

Input/Output Circuits

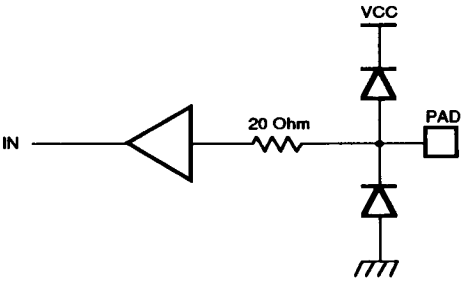


Figure 29. Input Only (Pad Type 1)

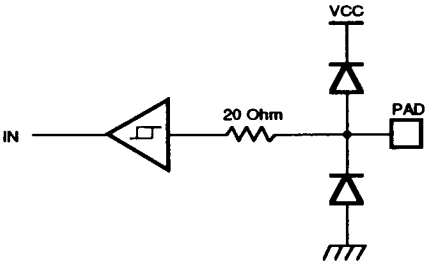


Figure 30. Input Only, Schmitt Triggered (Pad Type 2)

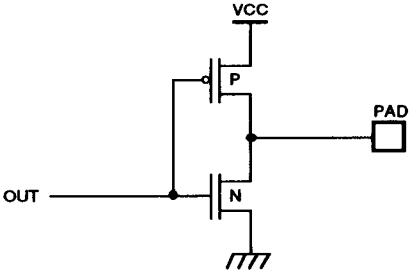


Figure 31. Output Only (Pad Type 3)

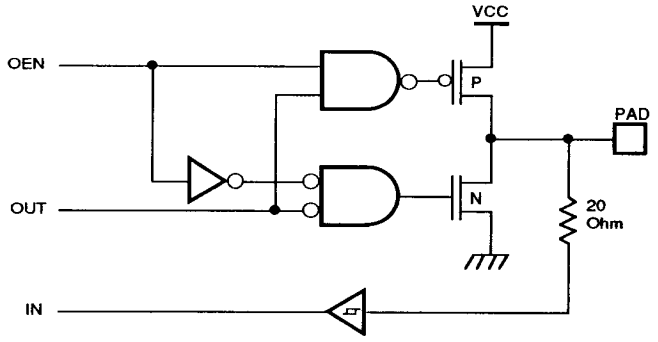


Figure 32. Input/Output 3-State (Pad Type 4)

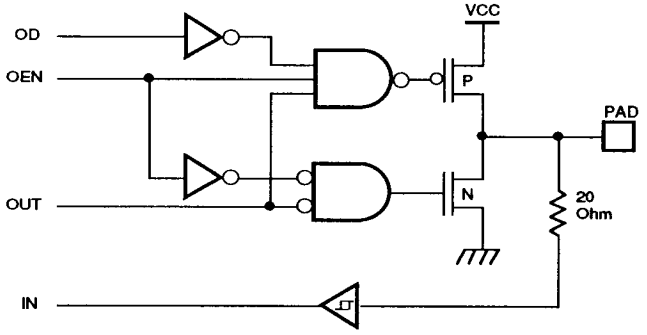


Figure 33. Input/Output, 3-state, Open Drain (Pad Type 5)

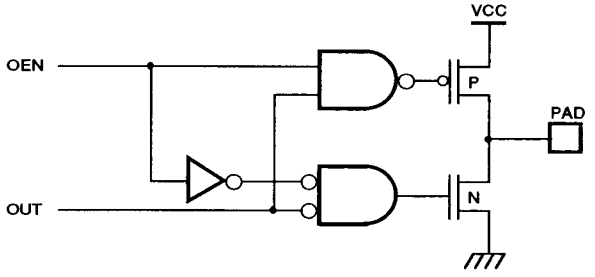


Figure 34. Output Only, 3-State (Pad Type 6)

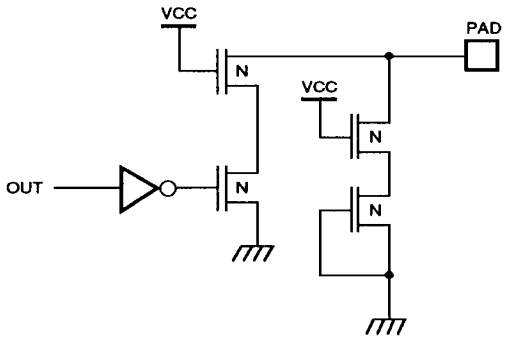


Figure 35. Output Only, 12-Volt Open Drain (Pad Type 7)

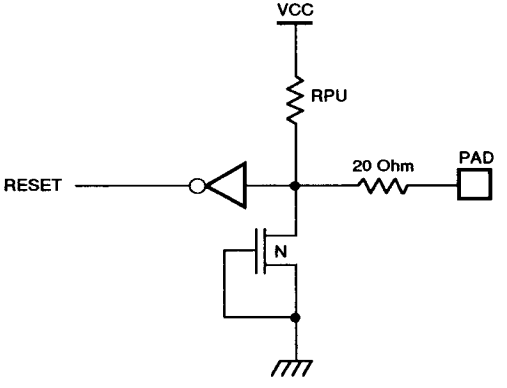


Figure 36. Reset Input Circuit (Pad Type 8)

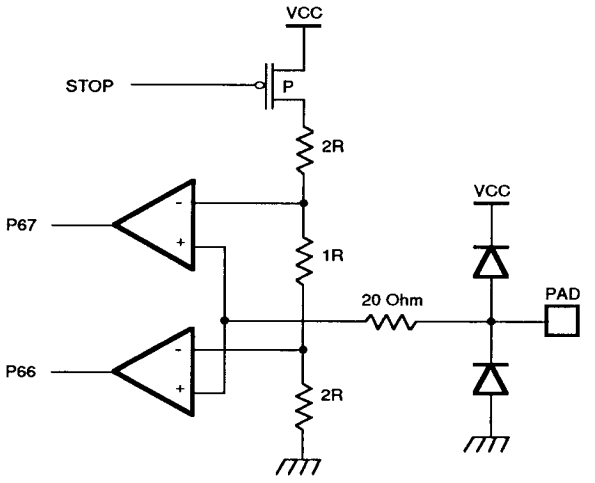


Figure 37. AFC Input Circuit (Pad Type 9)

Mapping of Symbolic Pad Types to Pin Functions

Pin Name	Pad Type	Notes
XTAL1, OSC_{IN} XTAL2, OSC_{OUT}	1	High gain start, low gain run amplifier circuit
/RESET	8	
P00-07	6	Z86C97 only
P10-17	4	Z86C97 only
P20-P27	5	
P30-P31	2	
P34-P36	3	
P40-P47	3	Z86C27 only
P50-P57	3	Z86C27 only
P60-P65	2	Z86C27 only
P66-P67	3	Z86C97 only
/AS, /DS, R/W, SCLK	3	Z86C97 only
AFCIN	9	
PWM1-PWM13	7	
HSYNC, VSYNC	2	
VRED, VBLUE, VGREEN, VBLANK	3	

DTC CONTROL REGISTER DIAGRAMS
Port Registers

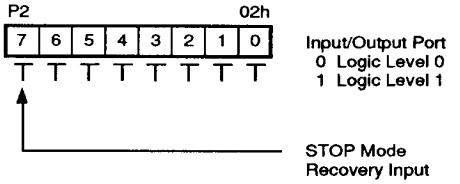


Figure 38. Port 2 Register

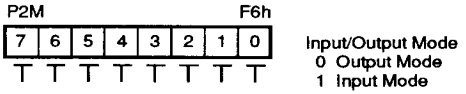


Figure 39. Port 2 Mode Register

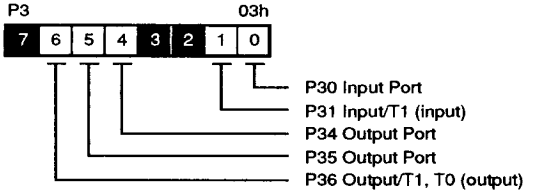


Figure 40. Port 3 Register

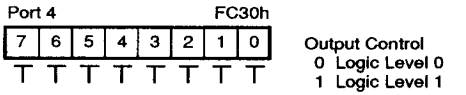


Figure 41. Port 4 Register

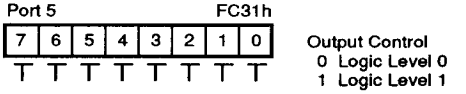


Figure 42. Port 5 Register

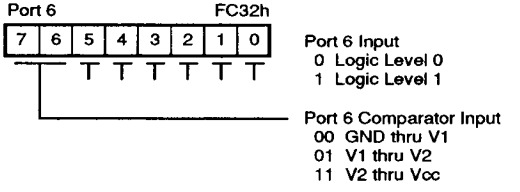


Figure 43. Port 6 Register

DTC CONTROL REGISTER DIAGRAMS
PWM Registers

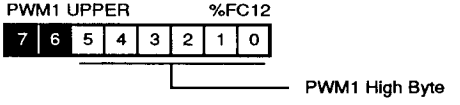


Figure 44. PWM 1 High Value

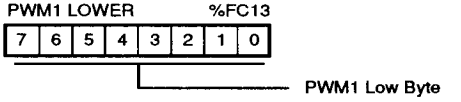


Figure 45. PWM 1 Low Value

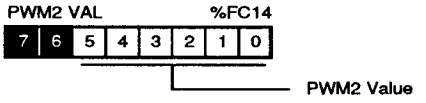


Figure 46. PWM 2 Value

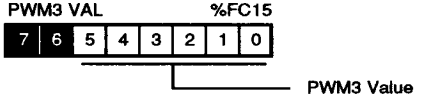


Figure 47. PWM 3 Value

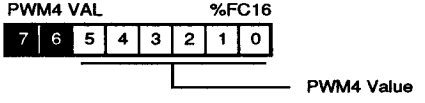


Figure 48. PWM 4 Value

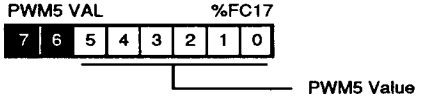


Figure 49. PWM 5 Value

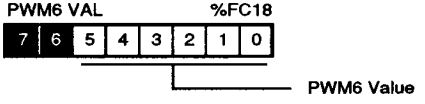


Figure 50. PWM 6 Value

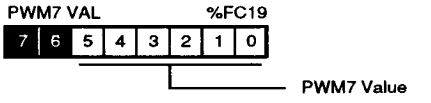


Figure 51. PWM 7 Value

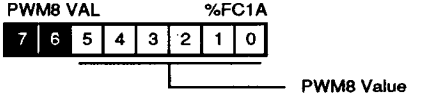


Figure 52. PWM 8 Value

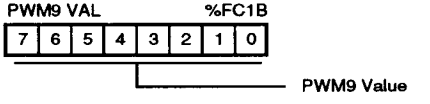


Figure 53. PWM 9 Value

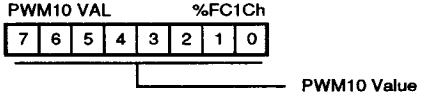


Figure 54. PWM 10 Value

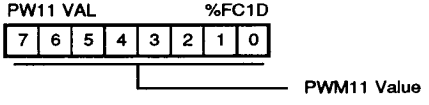


Figure 55. PWM 11 Value

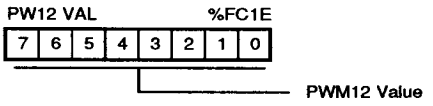


Figure 56. PWM 12 Value

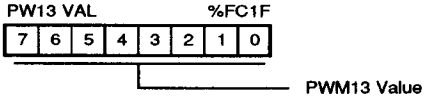


Figure 57. PWM 13 Value Register

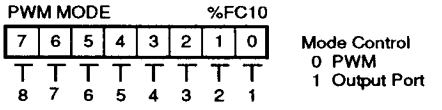


Figure 58. PWM Mode Register

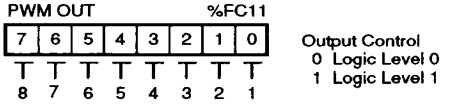


Figure 59. PWM Port Output Register

DTC CONTROL REGISTER DIAGRAMS

OSD Registers

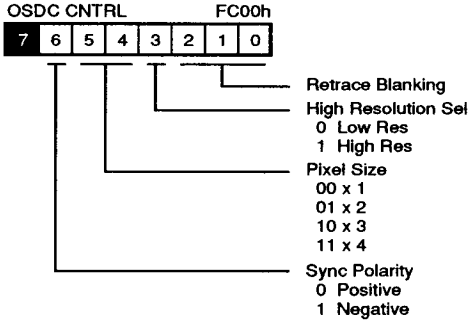


Figure 60. OSD Control Register

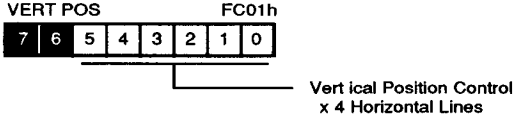


Figure 61. OSD Vertical Position Register

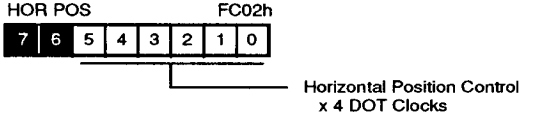


Figure 62. OSD Horizontal Position Register

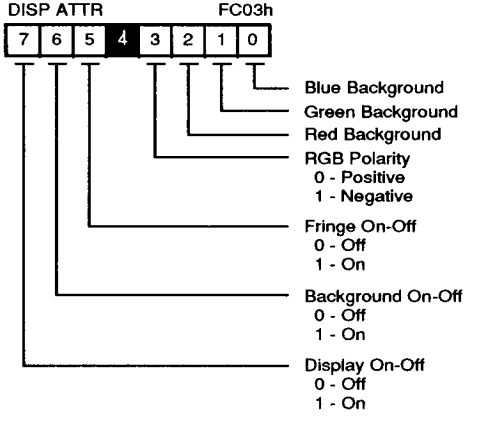


Figure 63. OSD Display Attribute Register

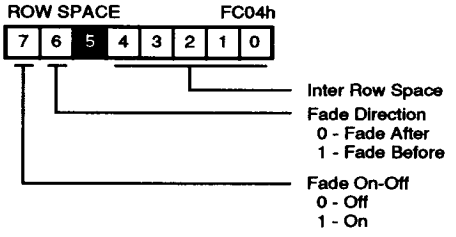


Figure 64. OSD Row Space Register

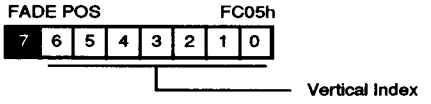


Figure 65. OSD Fade Position Register

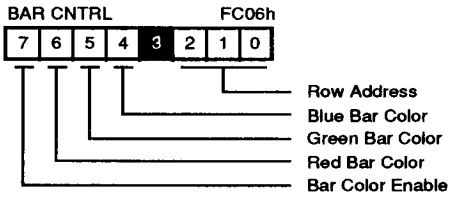


Figure 66. OSD Bar Control Register

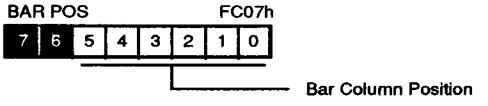


Figure 67. OSD Bar Position Register

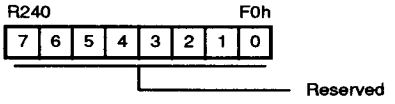


Figure 68. Reserved (F0H)

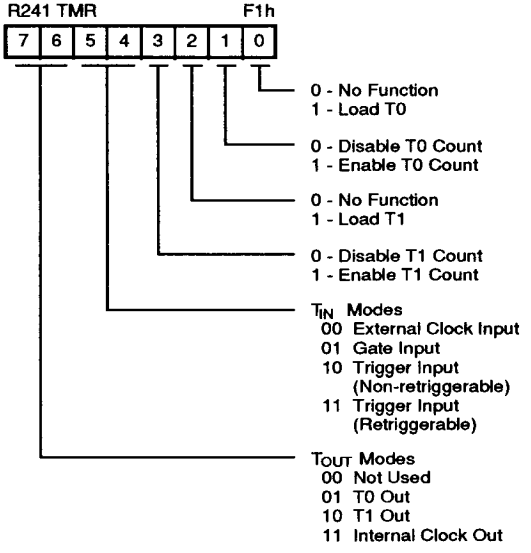


Figure 69. Timer Mode Register (F1H; Read/Write)

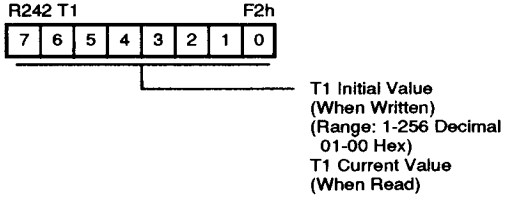


Figure 70. Counter Timer 1 Register (F1H; Read/Write)

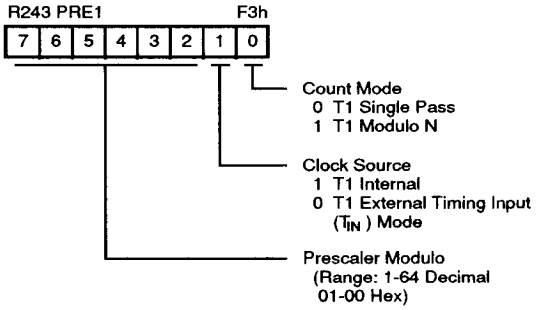


Figure 71. Prescaler 1 Register (F3H; Write Only)

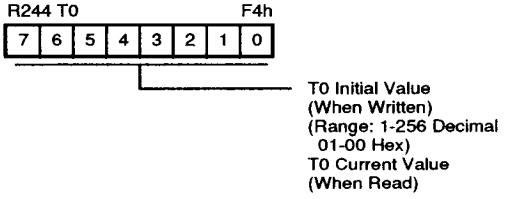


Figure 72. Counter/Timer 0 Register (F4H; Read/Write)

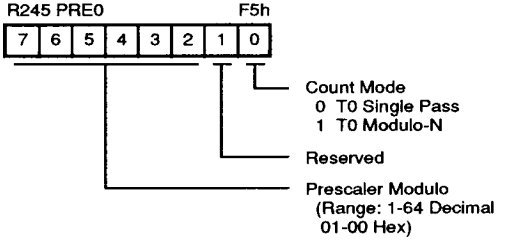


Figure 73 Prescaler 0 Register (F5H; Write Only)

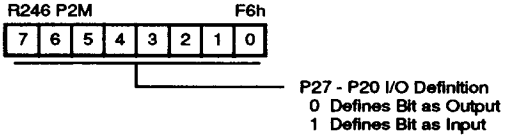


Figure 74. Port 2 Mode Register (F6H; Write Only)

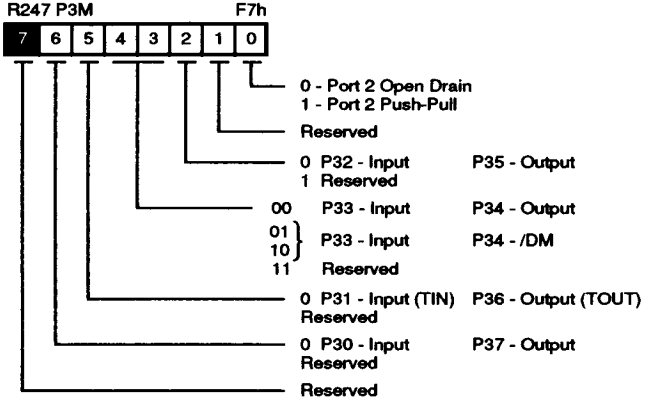


Figure 75. Port 3 Mode Register (F7H; Write Only)

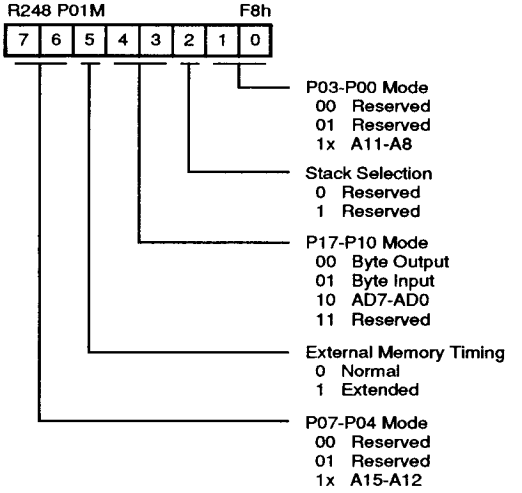


Figure 76. Port 0 and 1 Mode Register (F8H; Write Only)

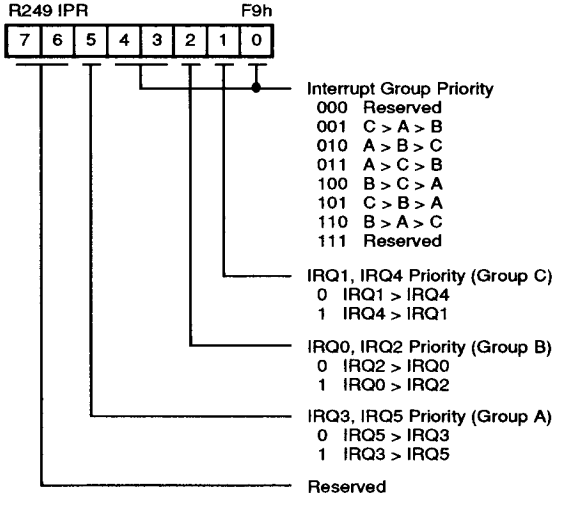


Figure 77. Interrupt Priority Register (F9H; Write Only)

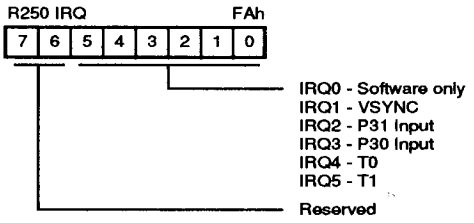


Figure 78. Interrupt Request Register (FAH; Read/Write)

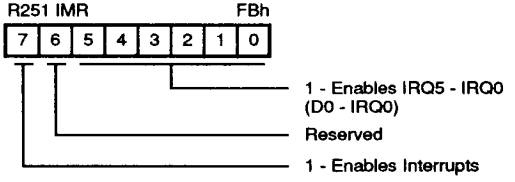


Figure 79. Interrupt Mask Register (FBH; Read/Write)

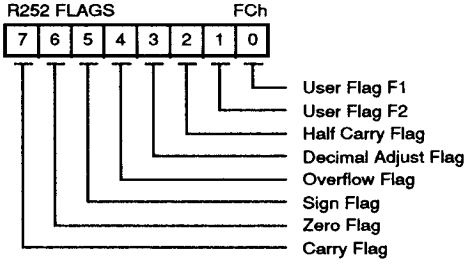


Figure 80. Flag Register (FCH; Read/Write)

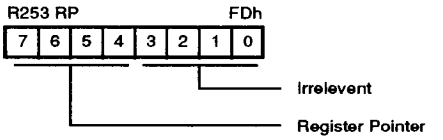


Figure 81. Register Pointer (FDH; Read/Write)

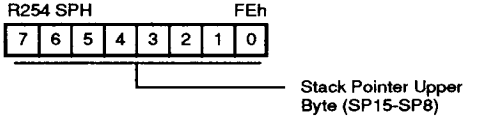


Figure 82. Stack Pointer (FEH; Read/Write)

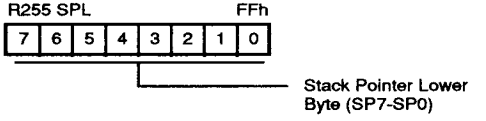


Figure 83. Stack Pointer (FFH; Read/Write)

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Irr	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working-register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack Pointer
PC	Program Counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags:

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

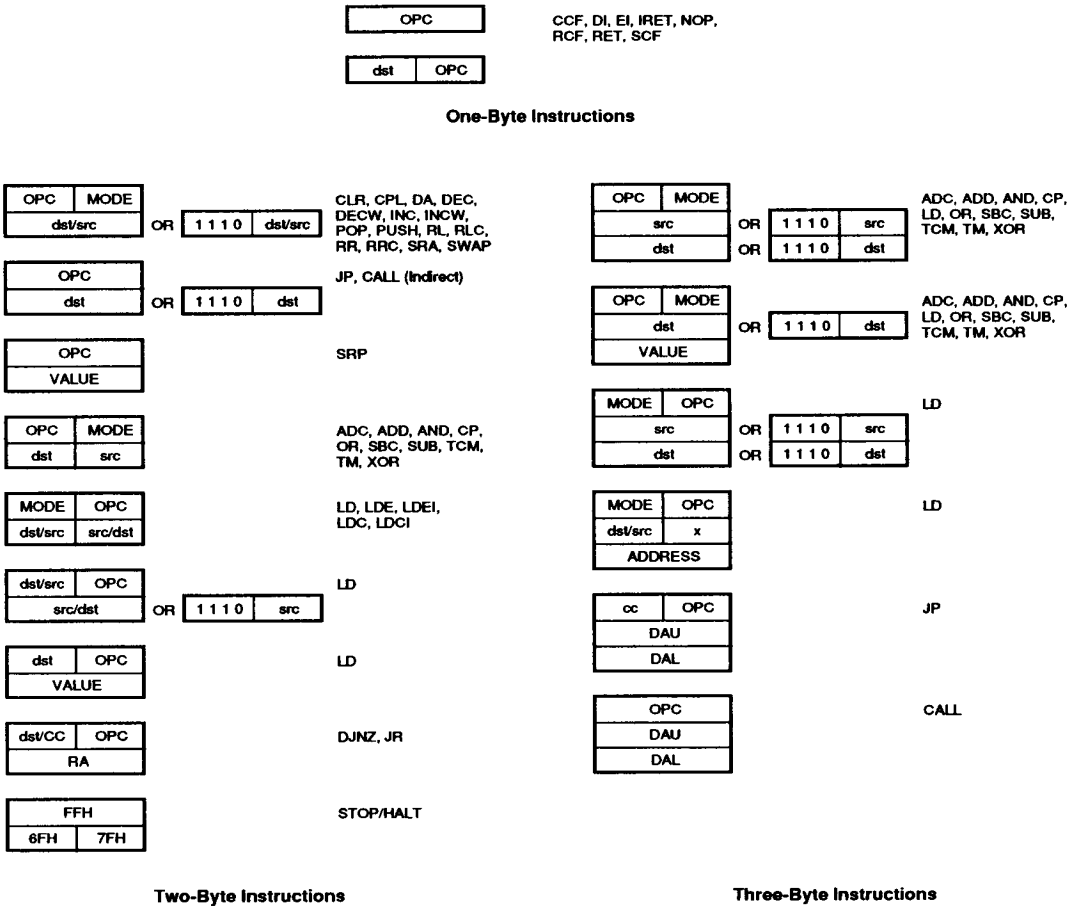
Affected flages are indicated by:

0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
x	Undefined

CONDITION CODES

Value	Mnemonic	Meaning	Flags Set
1000		Always True	
0111	C	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not Zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No Overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not Equal	Z = 0
1001	GE	Greater Than or Equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater Than	[Z OR (S XOR V)] = 0
0010	LE	Less Than or Equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned Greater Than or Equal	C = 0
0111	ULT	Unsigned Less Than	C = 1
1011	UGT	Unsigned Greater Than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned Less Than or Equal	(C OR Z) = 1
0000		Never True	

INSTRUCTION FORMATS



INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol " ← ". For example:

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

dst (7)

refers to bit 7 of the destination operand.

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
ADC dst, src dst←dst + src +C	†		1[ ]	*	*	*	*	0	*
ADD dst, src dst←dst + src	†		0[ ]	*	*	*	*	0	*
AND dst, src dst←dst AND src	†		5[ ]	-	*	*	0	-	-
CALL dst SP←SP - 2 @SP←PC, PC←dst	DA IRR		D6 D4	-	-	-	-	-	-
CCF C←NOT C			EF	*	-	-	-	-	-
CLR dst dst←0	R IR		B0 B1	-	-	-	-	-	-
COM dst dst←NOT dst	R IR		60 61	-	*	*	0	-	-
CP dst, src dst - src	†		A[ ]	*	*	*	*	-	-
DA dst dst←DA dst	R IR		40 41	*	*	*	X	-	-
DEC dst dst←dst - 1	R IR		00 01	-	*	*	*	-	-
DECW dst dst←dst - 1	RR IR		80 81	-	*	*	*	-	-
DI IMR(7)←0			8F	-	-	-	-	-	-
DJNZr, dst r←r - 1 if r ≠ 0 PC←PC + dst Range: +127, -128	RA		rA r = 0 - F	-	-	-	-	-	-
EI IMR(7)←1			9F	-	-	-	-	-	-
HALT			7F	-	-	-	-	-	-

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
INC dst dst←dst + 1	r R IR		rE r = 0 - F 20 21	-	*	*	*	-	-
INCW dst dst←dst + 1	RR IR		A0 A1	-	*	*	*	-	-
IRET FLAGS←@SP; SP←SP + 1 PC←@SP; SP←SP + 2; IMR(7)←1			BF	*	*	*	*	*	*
JP cc, dst if cc is true PC←dst	DA IRR		cD c = 0 - F 30	-	-	-	-	-	-
JR cc, dst if cc is true, PC←PC + dst Range: +127, -128	RA		cB c = 0 - F	-	-	-	-	-	-
LD dst, src dst←src	r r R r X r Ir R R IR IR	Im R r X r Ir r R IR IM IM R	rC r8 r9 r = 0 - F C7 D7 E3 F3 E4 E5 E6 E7 F5	-	-	-	-	-	-
LDC dst, src	r	Irr	C2	-	-	-	-	-	-
LDCI dst, src dst←src r←r +1; rr←rr + 1	Ir	Irr	C3	-	-	-	-	-	-

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
NOP			FF	-	-	-	-	-	-
OR dst, src dst←dst OR src	†		4[ ]	-	*	*	0	-	-
POP dst dst←@SP; SP←SP + 1	R IR		50 51	-	-	-	-	-	-
PUSH src SP←SP - 1; @SP←src		R IR	70 71	-	-	-	-	-	-
RCF C←0			CF	0	-	-	-	-	-
RET PC←@SP; SP←SP + 2			AF	-	-	-	-	-	-
RL dst	R IR		90 91	*	*	*	*	-	-
RLC dst	R IR		10 11	*	*	*	*	-	-
RR dst	R IR		E0 E1	*	*	*	*	-	-
RRC dst	R IR		C0 C1	*	*	*	*	-	-
SBC dst, src dst←dst←src←C	†		3[ ]	*	*	*	*	1	*
SCF C←1			DF	1	-	-	-	-	-
SRA dst	R IR		D0 D1	*	*	*	0	-	-
SRP src RP←src		Im	31	-	-	-	-	-	-

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
STOP			6F	-	-	-	-	-	-
SUB dst, src dst←dst←src	†		2[ ]	*	*	*	*	1	*
SWAP dst	R IR		F0 F1	X	*	*	X	-	-
TCM dst, src (NOT dst) AND src	†		6[ ]	-	*	*	0	-	-
TM dst, src dst AND src	†		7[ ]	-	*	*	0	-	-
XOR dst, src dst←dst XOR src	†		B[ ]	-	*	*	0	-	-

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

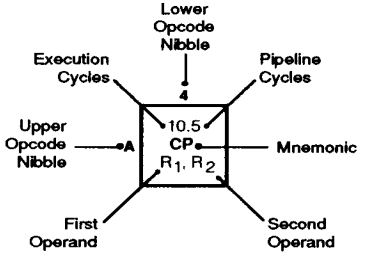
For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Address Mode dst	Address Mode src	Lower Opcode Nibble
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

OPCODE MAP

Lower Nibble (Hex)

Upper Nibble (Hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6.5 **DEC** R1	6.5 **DEC** IR1	6.5 **ADD** r1, r2	6.5 **ADD** r1, Ir2	10.5 **ADD** R2, R1	10.5 **ADD** IR2, R1	10.5 **ADD** R1, IM	10.5 **ADD** IR1, IM	6.5 **LD** r1, R2	6.5 **LD** r2, R1	12/10.5 **DJNZ** r1, RA	12/10.0 **JR** cc, RA	6.5 **LD** r1, IM	12.10.0 **JP** cc, DA	6.5 **INC** r1	
1	6.5 **RLC** R1	6.5 **RLC** IR1	6.5 **ADC** r1, r2	6.5 **ADC** r1, Ir2	10.5 **ADC** R2, R1	10.5 **ADC** IR2, R1	10.5 **ADC** R1, IM	10.5 **ADC** IR1, IM								
2	6.5 **INC** R1	6.5 **INC** IR1	6.5 **SUB** r1, r2	6.5 **SUB** r1, Ir2	10.5 **SUB** R2, R1	10.5 **SUB** IR2, R1	10.5 **SUB** R1, IM	10.5 **SUB** IR1, IM								
3	8.0 **JP** IRR1	6.1 **SRP** IM	6.5 **SBC** r1, r2	6.5 **SBC** r1, Ir2	10.5 **SBC** R2, R1	10.5 **SBC** IR2, R1	10.5 **SBC** R1, IM	10.5 **SBC** IR1, IM								
4	8.5 **DA** R1	8.5 **DA** IR1	6.5 **OR** r1, r2	6.5 **OR** r1, Ir2	10.5 **OR** R2, R1	10.5 **OR** IR2, R1	10.5 **OR** R1, IM	10.5 **OR** IR1, IM								6.0 **WDH**
5	10.5 **POP** R1	10.5 **POP** IR1	6.5 **AND** r1, r2	6.5 **AND** r1, Ir2	10.5 **AND** R2, R1	10.5 **AND** IR2, R1	10.5 **AND** R1, IM	10.5 **AND** IR1, IM								6.0 **WDT**
6	6.5 **COM** R1	6.5 **COM** IR1	6.5 **TCM** r1, r2	6.5 **TCM** r1, Ir2	10.5 **TCM** R2, R1	10.5 **TCM** IR2, R1	10.5 **TCM** R1, IM	10.5 **TCM** IR1, IM								6.0 **STOP**
7	10/12.1 **PUSH** R2	12/14.1 **PUSH** IR2	6.5 **TM** r1, r2	6.5 **TM** r1, Ir2	10.5 **TM** R2, R1	10.5 **TM** IR2, R1	10.5 **TM** R1, IM	10.5 **TM** IR1, IM								7.0 **HALT**
8	10.5 **DECW** RR1	10.5 **DECW** IR1	12.0 **LDE** r1, Irr2	18.0 **LDEI** Ir1, Irr2												6.1 **DI**
9	6.5 **RL** R1	6.5 **RL** IR1	12.0 **LDE** r2, Irr1	18.0 **LDEI** Ir2, Irr1												6.1 **EI**
A	10.5 **INCW** RR1	10.5 **INCW** IR1	6.5 **CP** r1, r2	6.5 **CP** r1, Ir2	10.5 **CP** R2, R1	10.5 **CP** IR2, R1	10.5 **CP** R1, IM	10.5 **CP** IR1, IM								14.0 **RET**
B	6.5 **CLR** R1	6.5 **CLR** IR1	6.5 **XOR** r1, r2	6.5 **XOR** r1, Ir2	10.5 **XOR** R2, R1	10.5 **XOR** IR2, R1	10.5 **XOR** R1, IM	10.5 **XOR** IR1, IM								16.0 **IRET**
C	6.5 **RRC** R1	6.5 **RRC** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2				10.5 **LD** r1,x,R2								6.5 **RCF**
D	6.5 **SRA** R1	6.5 **SRA** IR1	12.0 **LDC** r2, Irr1	18.0 **LDCI** Ir2, Irr1	20.0 **CALL*** IRR1		20.0 **CALL** DA	10.5 **LD** r2,x,R1								6.5 **SCF**
E	6.5 **RR** R1	6.5 **RR** IR1		6.5 **LD** r1, IR2	10.5 **LD** R2, R1	10.5 **LD** IR2, R1	10.5 **LD** R1, IM	10.5 **LD** IR1, IM								6.5 **CCF**
F	8.5 **SWAP** R1	8.5 **SWAP** IR1		6.5 **LD** Ir1, r2		10.5 **LD** R2, IR1										6.0 **NOP**
Bytes per Instruction	2			3					2					3	1	



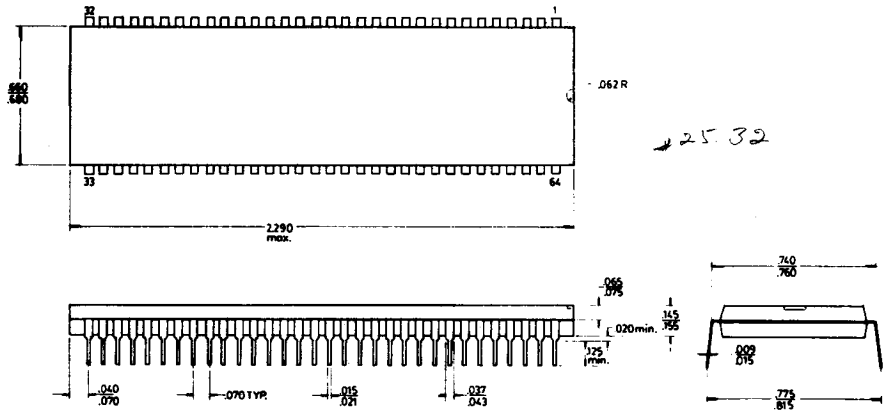
Legend:
R = 8-bit address
r = 4-bit address
R_1 or r_2 = Dst address
R_1 or r_2 = Src address

Sequence:
Opcode, First Operand, Second Operand

Note: The blank are not defined.

* 2-byte instruction appears as a 3-byte instruction

PACKAGE INFORMATION



64-Pin Dual In-Line Package (DIP)

ORDERING INFORMATION

Z86C27

4 MHz
64-pin DIP
Z86C2704PSC

Z86C97

4 MHz
Z86C9704PSC

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

Codes

Package
P = Plastic DIP

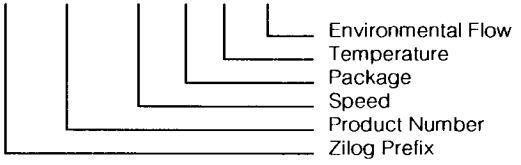
Temperature
S = 0°C to +70°C

Speed
04 = 4 MHz

Environmental
C = Plastic Standard

Example:

Z Z86C27 04 P S C is an 86C27 4 MHz, DIP, 0°C to 70°C, Plastic Standard Flow.



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