Data Sheet
January 1995

AT&T Microelectronics

T7256 Single-Chip NT1 (SCNT1) Transceiver

Features

- U- to S/T-interface conversion for ISDN basic rate (2B+D) systems
  - — Integrated U- and S/T-interfaces
  - — Operates in stand-alone mode to provide U- and S/T-interface activation, control, and maintenance functions
  - — Serial microprocessor and time-division multiplexed (TDM) bus interfaces for enhanced NT1 operation and voice/data ports
  - — Automatic embedded operations channel (eoc) processing for ANSI T1.601 systems
  - — Low power consumption (270 mW typical) supporting line-powered NT1
  - — Idle mode support (35 mW typical)
  - — Board-level testability support
- U-interface
  - — Conforms to ANSI T1.601 standard and ETSI DTR/TM 3002 technical report
  - — 2B1Q four-level line code
  - — Automatic ANSI maintenance functions (quiet mode and insertion loss mode)
- S/T-interface
  - — Conforms to ANSI T1.605 standard, ITU-T (formerly CCITT) I.430 recommendation, and ETSI ETS 300 012 for NT operation
  - — Supports point-to-point and point-to-multipoint (passive bus) arrangements
  - — Support of S and Q channel operations
- Serial microprocessor and TDM bus interfaces
  - — Supports inexpensive serial microprocessor
  - — Supports direct CODEC connection and voice/data ports
  - — Allows access to 2B+D data on TDM bus
- Other
  - — 0.9 µm linear CMOS technology
  - — Single +5 V (±5%) supply
  - — –40 °C to +85 °C
  - — 44-pin PLCC

Description

The AT&T T7256 Single-Chip NT1 (SCNT1) Transceiver integrated circuit provides data (2B+D) and control information conversion between 2-wire (U-interface) and 4-wire (S/T-interface) digital subscriber loops on the integrated services digital network (ISDN). The T7256 conforms to the ANSI T1.601 standard and ETSI DTR/TM 3002 technical report for the U-interface and the ITU-T I.430 recommendation, ANSI T1.605 standard, and ETSI ETS 300 012 for the S/T-interface. The T7256 also supports digital pair gain and terminal adapter applications. The single +5 V CMOS device is packaged in a 44-pin, plastic, leaded chip carrier (PLCC).

Table of Contents

Contents

Page

* *Motorola* is a registered trademark of Motorola, Inc.

Description (continued)

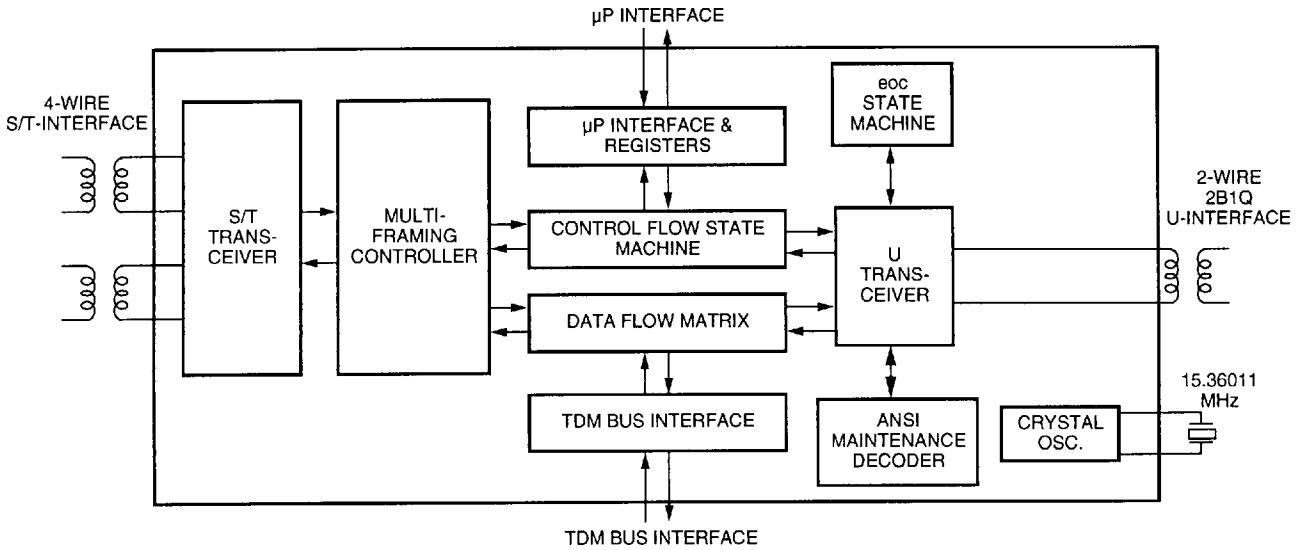
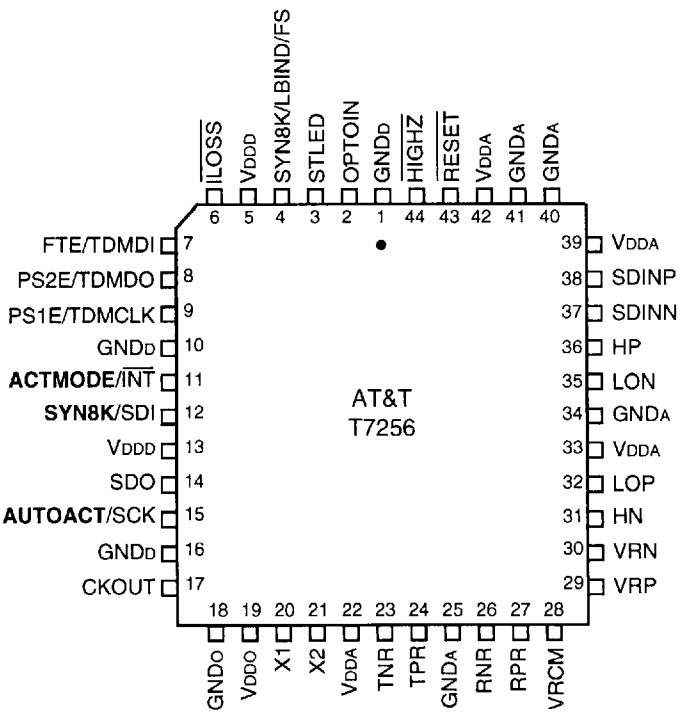


Figure 1. Block Diagram

Pin Information



Note: Controls shown in bold (pins 11, 12, and 15) are configured by the state of these pins when exiting $\overline{\text{RESET}}$.

Figure 2. Pin Diagram

Pin Information (continued)

Table 1. Pin Descriptions

Pin	Symbol	Type*	Name/Function
1, 10, 16	GNDD	—	**Digital Ground.** Ground leads for digital circuitry.
2	OPTOIN	I^U	**Optoisolator Input.** Pin accepts CMOS logic level maintenance pulse streams. These pulse streams typically are generated by an optoisolator that is monitoring the U loop. Pulse patterns on this pin are digitally filtered for 20 ms before being considered valid and are then decoded and interpreted using the ANSI maintenance state machine requirements. If AUTOCTL = 1 (register GR0, bit 3), the internal state machine decodes pulse trains and implements the required maintenance states automatically. If AUTOCTL = 0, the pulse trains are decoded internally, but the microprocessor must implement the maintenance state as indicated by the maintenance interrupts (register MIR0). If the OPTOIN pin is being used for implementing maintenance functions, the ILOSS pin should not be used. Instead, the ILOSS register bit should be used (register CFR0 bit 0). An internal 100 kΩ pull-up resistor is on this pin.
3	STLED	O	**Status LED Driver.** Output pin for driving an LED (source/sink 4.0 mA) that indicates the device status. The four defined states are low, high, 1 Hz flashing, and 8 Hz flashing (flashing occurs at 50% duty cycle). See the STLED Description section for a detailed explanation of these states. Also, this pin indicates device sanity upon poweron/RESET, as follows: ■ If SCK = 0 (pin 15) after a device RESET (which sets AUTOACT = 0 in register GR0 bit 6, turning on autoactivation), STLED will toggle at an 8 Hz rate for at least 0.5 s, signifying an activation attempt. If the activation attempt succeeds, it will continue to flash per the normal start-up sequence (see STLED Description section). ■ If SCK = 1 (pin 15) after a device RESET, STLED will go low for 1 s ("flash of life"), indicating that the device is operational, and no activation attempt will be made.
4	SYN8K/LBIND/FS	O	**Synchronous 8 kHz Clock or Loopback Indicator.** Pin function is selected via SDI pin state at end of external RESET . As SYN8K, this pin can be used as a reference clock or for synchronization in device performance testing (i.e., it reflects the recovered timing from the U-interface). As LBIND, this pin indicates a 2B+D loopback: 0 — No loopback. 1 — eoc requested 2B+D loopback in progress. **Frame Strobe.** If TDMEN = 0 (register GR2, bit 5), this pin is a programmable strobe output used to indicate appearance of B and/or D channel data on TDM bus. Polarity, offset, and duration are programmable through microprocessor interface.
5, 13	VDDD	—	**Digital Power.** 5 V ± 5% power supply pins for digital circuitry.

* I^U = input with internal pull-up.

Pin Information (continued)

Table 1. Pin Descriptions (continued)

Pin	Symbol	Type*	Name/Function
6	$\overline{\text{ILOSS}}$	I^u	**Insertion Loss Test Control (Active-Low).** The $\overline{\text{ILOSS}}$ pin is used to control SN1 tone transmission for maintenance. The OPTOIN and $\overline{\text{ILOSS}}$ pins should not be used at the same time (i.e., OPTOIN should be held high). This pin would typically be used if an external ANSI maintenance decoder is being used, in which case the decoder output drives the $\overline{\text{ILOSS}}$ pin. The $\overline{\text{ILOSS}}$ pin is ignored, and the functionality is controlled by the ILOSS bit (register CFR0, bit 0) if AUTOCTL = 0 (register GR0, bit 3). Internal 100 kΩ pull-up resistor on this pin. 0 — U transmitter sends SN1 tone continuously. 1 — No effect on device operation.
7	FTE/ TDMDI	I^u	**Fixed/Adaptive Timing Mode Select.** Selects S/T-interface timing recovery mode: 0 — Fixed timing recovery mode. 1 — Adaptive timing recovery mode. **TDM Data In.** If TDMEN = 0 (register GR2, bit 5), this pin is the TDM bus 2B+D data input synchronous with TDMCLK, and the S/T-interface timing mode is controlled via the FT bit (register GR2, bit 0). An internal 100 kΩ pull-up resistor is on this pin.
8	PS2E/ TDMDO	I^d/O	**Power Status #2.** If TDMEN = 1 (default), this is an input for the PS2 bit in transmit U-interface data stream. See PS2 bit description (register GR1, bit 1) for PS1 and PS2 message definition. If the PS2E functionality is not used, this input must be pulled up externally with a 10 kΩ or less resistor to set the U-interface PS2 bit to the inactive state. An internal 100 kΩ pull-down resistor is on this pin. **TDM Data Out.** If TDMEN = 0, this pin is the 2.048 MHz TDM bus 2B+D data output synchronous with TDMCLK, and PS2 is controlled via the PS2 (register GR1, bit 1) microprocessor register bit.
9	PS1E/ TDMCLK	I^d/O	**Power Status #1.** If TDMEN = 1 (default), this is an input for the PS1 bit in transmit U-interface data stream. See PS2 bit description (register GR1 bit 1) for PS1 and PS2 message definition. If the PS1E functionality is not used, this input must be pulled up externally with a 10 kΩ or less resistor to set the U-interface PS1 bit to the inactive state. An internal 100 kΩ pull-down resistor is on this pin. **TDM Clock.** If TDMEN = 0, this pin is the 2.048 MHz TDM clock output synchronous with U-interface (if active) or is free-running, and PS1 is controlled via the PS1 microprocessor register bit.

* I^u = input with internal pull-up; I^d = input with internal pull-down.

Pin Information (continued)

Table 1. Pin Descriptions (continued)

Pin	Symbol	Type*	Name/Function
11	ACTMODE/ $\overline{\text{INT}}$	I^u/O	**ACT Bit Mode.** Upon exiting $\overline{\text{RESET}}$, the state of $\overline{\text{INT}}$ is read and if $\overline{\text{INT}}$ = 1 (default), bit ACTSEL = 1 (register GR2, bit 6). If $\overline{\text{INT}}$ = 0 (externally pulled down), then ACTSEL = 0. An internal 100 kΩ pull-up resistor is on this pin. **Serial Interface Microprocessor Interrupt (Active-Low).** Interrupt output for microprocessor. Any active, unmaskable bit in interrupt registers UIR0, SIR0, or MIR0 will cause $\overline{\text{INT}}$ to go low. The bits in the interrupt registers UIR0, SIR0, and MIR0 will be set on a true condition, independent of the state of the corresponding mask bits. If a masked, active interrupt bit is subsequently unmasked, the $\overline{\text{INT}}$ pin will go low to indicate an interrupt for that condition. Reading UIR0, SIR0, or MIR0 clears the entire register and forces $\overline{\text{INT}}$ high for 50 µs. After this interval, $\overline{\text{INT}}$ will again reflect the state of any unmasked bit in these registers. The global interrupt register (GIR0) provides a summary status of the UIR0, SIR0, and MIR0 interrupt registers and indicates if one of the registers currently has an active, unmasked interrupt bit.
12	SYN8K/SDI	I^d	**Synchronous 8 kHz Clock.** If pin is held low during an external $\overline{\text{RESET}}$, the SYN8K/LBIND/FS pin performs the SYN8K function. If held high during an external $\overline{\text{RESET}}$, the pin performs the LBIND function. An internal 100 kΩ pull-down resistor is on this pin. **Serial Interface Data Input.** Data input for microprocessor interface.
14	SDO	O	**Serial Interface Data Output.** Data output for microprocessor interface.
15	AUTOACT/ SCK	I^d	**Automatic Activation.** If pin is held low during an external $\overline{\text{RESET}}$, the AUTOACT bit is written to 0, creating an activation attempt (see AUTOACT [register GR0, bit 6] description in Table 6). If pin is held high during external $\overline{\text{RESET}}$, no activation is attempted. An internal 100 kΩ pull-down resistor is on this pin. **Serial Interface Clock.** Clock input for microprocessor interface.
17	CKOUT	O	**Clock Output.** Clock output function to drive other board components. Powerup default state is high-impedance to minimize power consumption. Programmable via microprocessor register (register GR0, bits 1 and 2) to provide 15.36011 MHz output or 10.24 MHz output. If U-interface is active, the 10.24 MHz output is synchronous with U-interface timing.
18	GND_O	—	**Crystal Oscillator Ground.** Ground lead for crystal oscillator.
19	V_{DDO}	—	**Crystal Oscillator Power.** Power supply lead for crystal oscillator.
20	X1	I	**Crystal #1.** Crystal connection #1 for 15.36011 MHz oscillator.
21	X2	I	**Crystal #2.** Crystal connection #2 for 15.36011 MHz oscillator.
22, 33, 39, 42	V_{DDA}	—	**Analog Power.** 5 V ± 5% power supply leads for analog circuitry.
23	TNR	O	**Transmit Negative Rail for S/T-Interface.** Negative output of S/T-interface analog transmitter. Connect to transformer through a 121 Ω ± 1% resistor.
24	TPR	O	**Transmit Positive Rail for S/T-Interface.** Positive output of S/T-interface analog transmitter. Connect to transformer through a 121 Ω ± 1% resistor.

* I^u = input with internal pull-up; I^d = input with internal pull-down.

Pin Information (continued)

Table 1. Pin Description (continued)

Pin	Symbol	Type*	Name/Function
25, 34, 40, 41	GND_A	—	**Analog Ground.** Ground leads for analog circuitry.
26	RNR	I	**Receive Negative Rail for S/T-Interface.** Negative input of S/T-interface analog receiver. Connect to transformer through a 10 kΩ ± 10% resistor.
27	RPR	I	**Receive Positive Rail for S/T-Interface.** Positive input of S/T-interface analog receiver. Connect to transformer through a 10 kΩ ± 10% resistor.
28	VRCM	—	**Common-Mode Voltage Reference for U-Interface Circuits.** Connect a 0.1 µF ± 20% capacitor to GND_A (as close to the device pins as possible).
29	VRP	—	**Positive Voltage Reference for U-Interface Circuits.** Connect a 0.1 µF ± 20% capacitor to GND_A (as close to the device pins as possible).
30	VRN	—	**Negative Voltage Reference for U-Interface Circuits.** Connect a 0.1 µF ± 20% capacitor to GND_A (as close to the device pins as possible).
31	HN	I	**Hybrid Negative Input for U-Interface.** Connect directly to negative side of U-interface transformer.
32	LOP	O	**Line Driver Positive Output for U-Interface.** Connect to the U-interface transformer through a 16.9 Ω ± 1% resistor.
35	LON	O	**Line Driver Negative Output for U-Interface.** Connect to the U-interface transformer through a 16.9 Ω ± 1% resistor.
36	HP	I	**Hybrid Positive Input for U-Interface.** Connect directly to positive side of U-interface transformer.
37	SDINN	I	**Sigma Delta A/D Negative Input for U-Interface.** Connect via an 820 pF ± 5% capacitor to SDINP.
38	SDINP	I	**Sigma Delta A/D Positive Input for U-Interface.** Connect via an 820 pF ± 5% capacitor to SDINN.
43	$\overline{\text{RESET}}$	I^d	**Reset (Active-Low).** Asynchronous Schmitt trigger input. Reset halts data transmission, clears adaptive filter coefficients, resets the U transceiver timing recovery circuitry, resets the S/T-interface transceiver, and sets all microprocessor register bits to their default state. During reset, the U-interface transmitter produces 0 V and the output impedance is 135 Ω at tip and ring. The $\overline{\text{RESET}}$ pin can be used to implement quiet mode maintenance testing (refer to pin 2 description). The states of SCK, SDI, and $\overline{\text{INT}}$ are read upon exiting reset state. See SCK, SDI, and $\overline{\text{INT}}$ pin descriptions. An internal 100 kΩ pull-down resistor is on this pin. $\overline{\text{RESET}}$ must be held low for 1.5 ms after power on. Device is fully functional after an additional 1 ms.
44	$\overline{\text{HIGHZ}}$	I^u	**High-Impedance Control (Active-Low).** Control of the high-impedance function. An internal 100 kΩ pull-up resistor is on this pin. **Note:** This pin does not tristate the analog outputs. 0 — All digital outputs enter high-impedance state. 1 — No effect on device operation.

* I^u = input with internal pull-up; I^d = input with internal pull-down.

Application Overview

The T7256 is intended for use in ISDN networks as part of a 2-wire to 4-wire converter (NT1) or as part of a terminal adapter (TA), providing 2-wire termination of the network with available voice and/or data ports. Local switching of terminal voice/data is also supported by the T7256. Figure 3 shows the NT1 and TA applications. See Using the T7256 in a Combination TE/TA Environment in the Application Briefs section for a detailed explanation of an application which has both TE and TA functions.

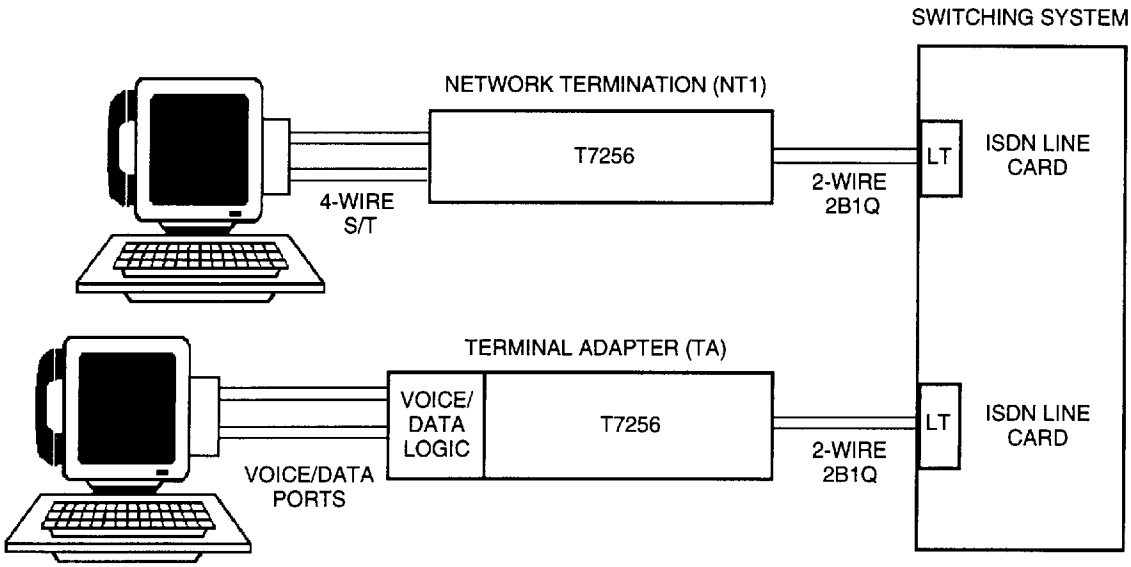


Figure 3. Applications of T7256

Functional Overview

The T7256 device provides four major interfaces for information transfer: the U-interface, the S/T-interface, the microprocessor interface, and the time-division multiplexed (TDM) bus interface. Use of the microprocessor and TDM bus interface is optional. Routing of data between the interfaces is controlled by the data flow matrix that uses register settings accessible via the microprocessor port. The data flow matrix circuitry routes 2B+D information between the appropriate interfaces, under direction of the microprocessor register settings. Routing between the T7256 interfaces allows configurations to support both NT1 and TA applications.

The architecture of the T7256 allows for a flexible combination of automatically and manually controlled functions. A control flow state machine, eoc state machine, and multiframing controller can be independently enabled or disabled. When enabled, these circuit blocks automatically perform their functions while ignoring the associated control bits in the microprocessor registers. When disabled, the control bits are made available to the microprocessor for manipulation. At all times, the status bits are available to the microprocessor and the 2B+D data can be routed via the data flow matrix.

At the U-interface, the T7256 conforms to ANSI T1.601 and ETSI DTR/TM 3002. The 2B1Q line code provides a four-level (quaternary) pulse amplitude modulation code with no redundancy. Data is grouped into pairs of bits for conversion to quaternary (quat) symbols. Figure 4 shows an example of this coding method.

The U-interface transceiver section provides the 2B1Q line coder (D/A conversion), pulse shaper, line driver, first-order line balance network, clock regeneration, and sigma-delta A/D conversion. The line driver, when connected to the proper transformer and interface circuitry, generates pulses which meet the required 2B1Q templates. The A/D converter is implemented by using a double-loop, sigma-delta modulator.

The U transceiver block also takes input from the data flow matrix and formats this information for the U-interface (see Figure 1). During this formatting, synchronization bits for U framing are added and a scrambling algorithm is applied. This data is then transferred to the 2B1Q encoder for transmission over the U-interface. Signals received from the U-interface are first passed through the sigma-delta A/D converter, and then sent to the digital signal processor for more extensive signal processing. The block provides decimation of the sigma-delta output, linear and non-linear echo cancellation, automatic gain control, signal detection, phase shift interpolation, decision feedback equalization, timing recovery, descrambling, and line-code polarity detection. The decision feedback equalizer circuit provides the functionality necessary for proper operation on subscriber loops with bridged taps.

A crystal oscillator provides the 15.36011 MHz master clock for the device. The on-chip phase-locked loop provides the ability to synchronize the chip to the line rate.

The U-interface provides rapid cold start and warm start operation. From a cold start, the device is typically operational within 3 seconds. The interface supports activation/deactivation, and when properly deactivated, it stores the adaptive filter coefficients permitting a warm start on the next activation request. A warm start typically requires 200 ms for the device to become operational.

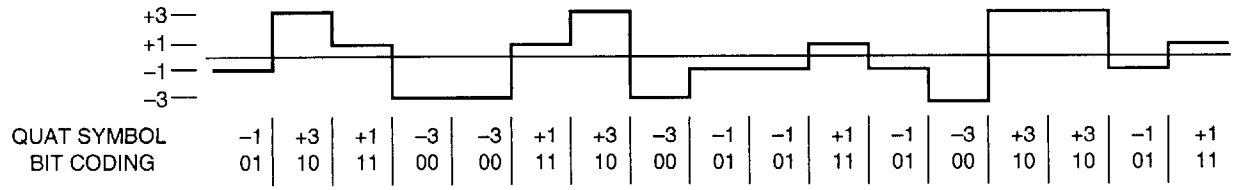


Figure 4. U-Interface Quat Example

Functional Overview (continued)

At the S/T-interface, the four-wire line transceiver meets the ANSI T1.605 standard, ITU-T I.430 recommendation, and ETSI ETS 300 012. At this interface, alternate space inversion (ASI) coding represents a logical 1 by the absence of a pulse and a logical 0 by alternating positive and negative pulses. Figure 5 illustrates the ASI coding method.

The S/T transceiver provides a voltage-limited current driver at the transmit interface, a self-adjusting voltage threshold comparator at the receive interface, and a digital timing recovery circuit employing either adaptive or fixed timing modes. Transmit pulses meeting the required templates can be achieved with the connection of appropriate transformers and interface components. In the adaptive timing mode, extended passive bus and point-to-point configurations are supported. The fixed timing mode supports the short passive bus configuration. The timing mode is programmed via the external FTE pin or by the FT bit (register GR2, bit 1) over the microprocessor interface.

The S/T transceiver also interprets the frames received from the line and generates frames to be transmitted onto the S/T link. It exchanges full-duplex 2B+D information with the data flow matrix.

The microprocessor interface is a serial communications port consisting of input data (SDI), output data (SDO), input clock (SCLK), and an output interrupt pin (INT). The microprocessor interface supports synchronous communication between the T7256 and an inexpensive microprocessor with a serial port. The interrupt is maskable via the on-board microprocessor interrupt mask registers. The internal register set controls various functions including information routing between interfaces, auto-eoc processing, maintenance testing, S/T-interface timing recovery mode, S and Q channel processing, microprocessor interrupt masks, activation of the TDM bus, and frame strobe timing.

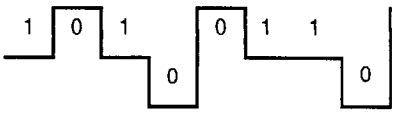


Figure 5. S/T-Interface ASI Example

The TDM interface consists of a TDM bus data clock (TDMCLK), input data (TDMDI), output data (TDMDO), and frame strobe (FS). The 2B+D data is transmitted and received in fixed time slots on the TDM bus; however, the frame strobe output lead is programmable to support a wide variety of devices (CODECs, HDLC processors, asynchronous interfaces) for direct connection on the TDM bus. The TDM bus exists as a selectable option via the microprocessor interface. When the TDM bus is activated, pins 4, 7, 8, and 9 are reconfigured to form the bus interface.

The eoc state machine, when enabled, automatically performs the eoc channel functions as described in the ANSI requirements. When disabled, control of the eoc channel is passed to the microprocessor via the appropriate microprocessor register bits.

The ANSI maintenance controller can operate in fully automatic or in fully manual mode. In automatic mode, the device decodes and responds to maintenance states according to the ANSI requirements. In manual mode, the device is controlled by an external maintenance decoder that drives the RESET and ILOSS pins to implement the required maintenance states.

The multiframing controller, when enabled, allows the S and Q channels on the S/T-interface to be manipulated by the microprocessor. When disabled, the S and Q channel bits are automatically loaded with their default values for applications not supporting multiframing.

Functional Overview (continued)

The control flow state machine performs the functions of reserved bit insertion, automatic implementation of the ANSI maintenance state machine, and automatic prioritization of multiple requests, such as reset, activation, maintenance, etc. Some bits which are normally controlled by the control flow state machine can be forced to their active state by writing the appropriate register (i.e., register GR1). When the control flow state machine is disabled (via the AUTOCTL bit in register GR0), the only change in the operation is that reserved bit control and ANSI maintenance control are passed directly to the microprocessor via register CFR0.

When the T7256 is powered on and there is no activity on the S/T or U-interfaces (i.e., no pending activation request), it automatically enters a low power IDLE mode in which it consumes an average of 35 mW. This mode is exited automatically when an activation or U maintenance request occurs from either the microprocessor or the S/T or U-interfaces.

The T7256 provides a board-level test capability that allows functional verification. Finally, an LED driver output indicates the status of the device during operation.

T7256 Reference Circuit

A reference circuit illustrating the T7256 in a stand-lone NT1 application is shown Figures 6 and 7. This depicts a complete stand-alone NT1 design with the exception of power supply circuitry and power status monitoring circuitry. A bill of materials for the schematic is shown in Table 2.

T7256 Reference Circuit (continued)

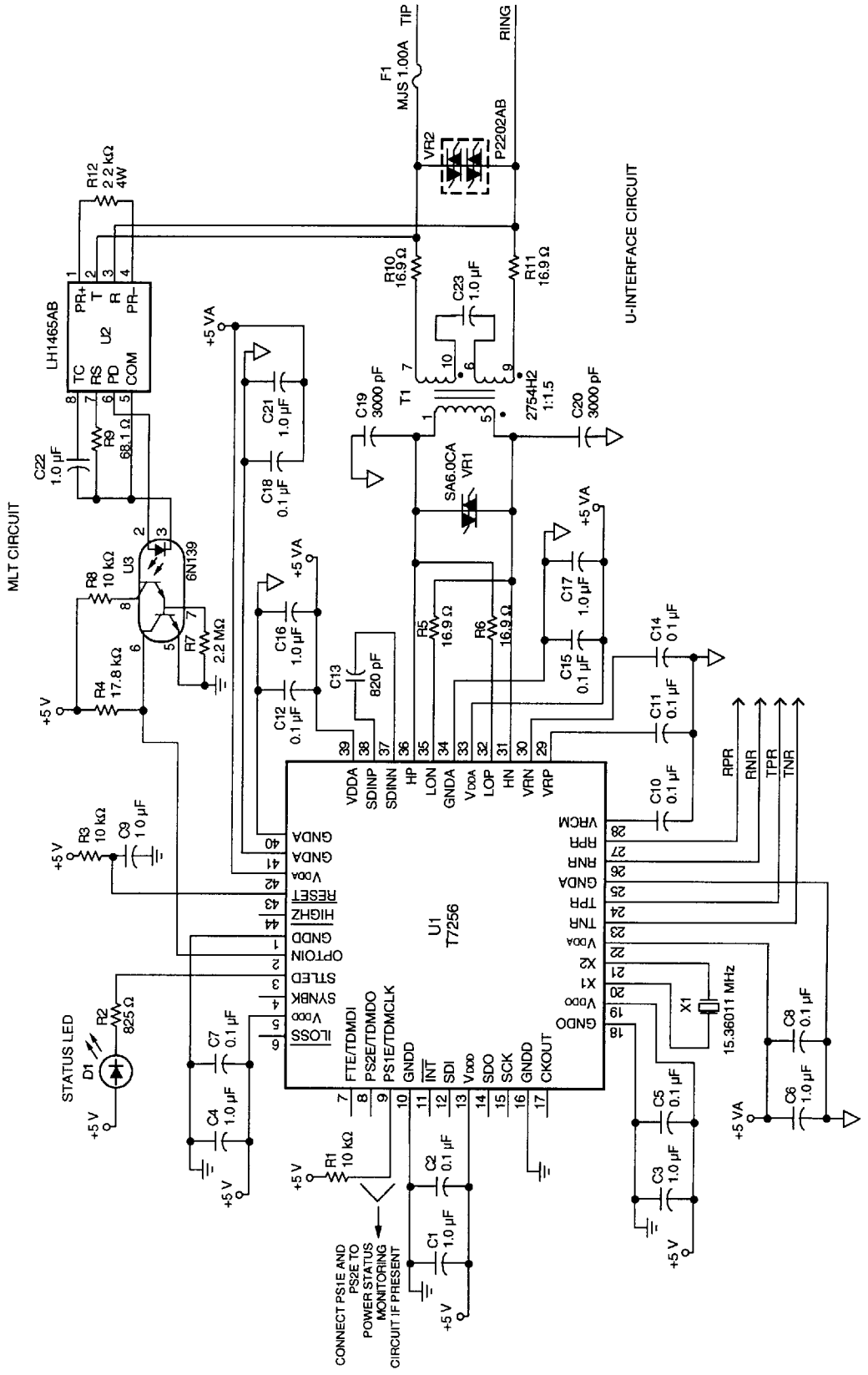


Figure 6. T7256 Stand-Alone Reference Circuit-A

T7256 Reference Circuit (continued)

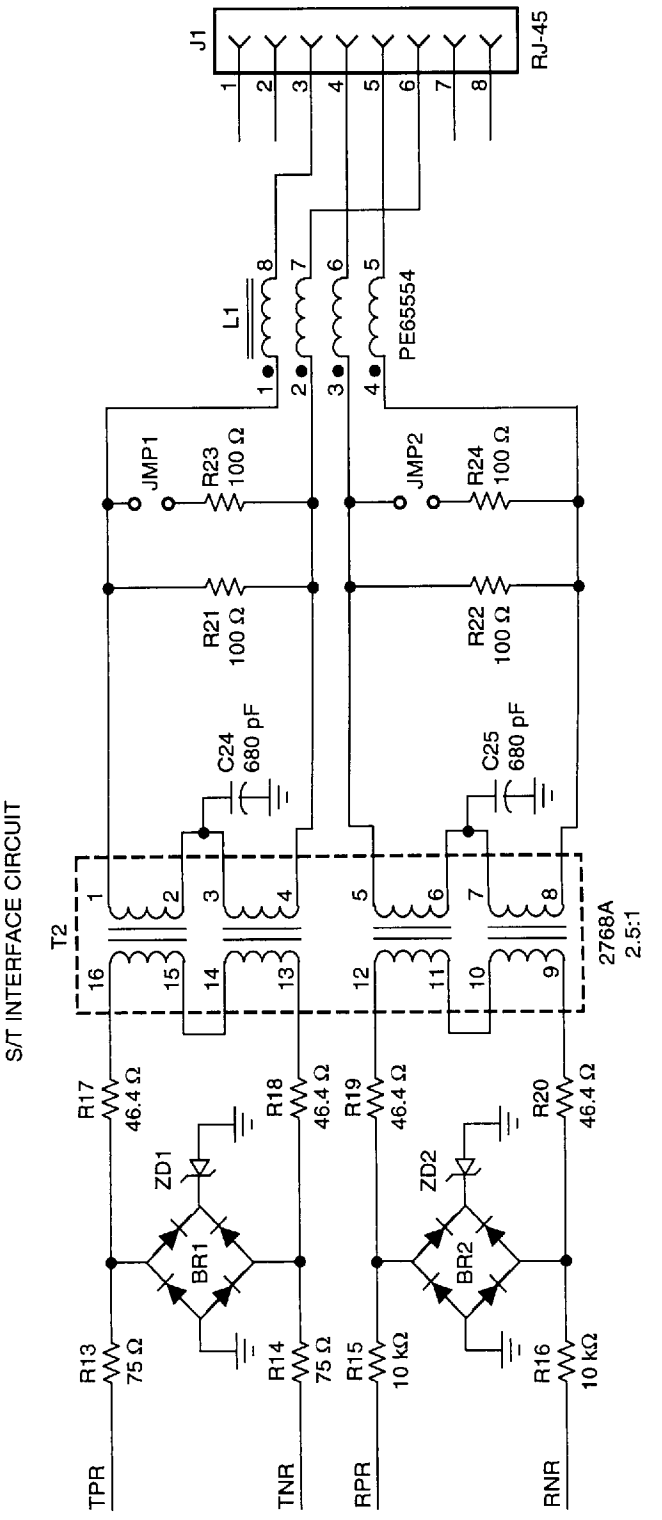


Figure 7. T7256 Stand-Alone Reference Circuit-B

T7256 Reference Circuit (continued)

Table 2. T7256 Reference Schematic Parts List

Reference Designator	Description	Source	Alternate Part
U1	T7256 IC	AT&T-ME	—
U2	LH1465AB dc termination IC	AT&T-ME	—
U3	6N139 opto isolator	Multiple	—
X1	crystal, 15.36011 MHz	Multiple	Examples: 2B Elettronica S.D.L. (Italy) P/N: TP0648 Tel: +39 6 6622432 Fax: +39 6 6632956 MTRON P/N: 4044-001 (605) 665-9321 SaRonix P/N: SRX5144 (415) 856-6900
T1	2754H2 transformer (1 kVRMS isolation)	AT&T-ME See notes at end of Table 2	AT&T 2754K2 (1.5 kVRMS) - pin compatible with 2754H2 Valor PT4084 (2 kVRMS) (619) 537-2500
T2	2768A transformer	AT&T-ME	Pulse Engineering, Inc. P/N: PE-65498 - pin compatible with 2754H2 (619) 674-8100 **For applications requiring reinforced insulation:** Advanced Power Components LTD (UK) P/N: APC2050S (single transformer) US Man Rep: Terry Manton Inc. (201) 447-8821 European office: 44 634 290588 VACUUMSCHMELZE (VAC) (Germany) P/N: T60403-L4097-X017-80 (single transformer) US: (908) 494-3530 Europe: 49 6181 38 2026 Pulse Engineering, Inc. P/N: PE-68998 (single transformer) (619) 674-8100

T7256 Reference Circuit (continued)

Table 2. T7256 Reference Schematic Parts List (continued)

Reference Designator	Description	Source	Alternate Part
F1	BEL MJS 1.00A fuse	BEL Fuse, Inc. (201) 432-0463 See notes at end of Table 2	Raychem TR600-150 PTC (800) 272-9243
VR1	SA6.0CA secondary protector (thru-hole)	*Motorola*	*SGS Thomson** 6T6V8CA (surface mount)
VR2	P2202AB *SIDACtor*† primary protector	Teccor (214) 580-1515	—
L1	PE65554 HF common-mode choke	Pulse Engineering (619) 674-8100	—
ZD1, ZD2	1.5SMC8.2AT3 8.2 V transient surge suppressor	*Motorola*	—
BR1, BR2	Diode bridge - use (x4) *Motorola* diodes 1N-4151	*Motorola*	—
D1	LED	multiple	—
J1	RJ45 connector	multiple	—
JMP1, JMP2	2-position jumper	multiple	—
C1, C3, C4, C6, C9, C16, C17, C21	1.0 µF decoupling capacitor	multiple	—
C2, C5, C7, C8, C10, C11, C12, C14, C15, C18	0.1 µF decoupling capacitor	multiple	—
C13	820 pF ± 5% capacitor (ceramic)	multiple	—
C19, C20	3000 pF ± 10% capacitors	multiple	
C22	1.0 µF 15 V ± 10% capacitor (**Note:** insulation resistance of this part must be > 10 GΩ)	multiple	—

* *SGS-Thomson* is a registered trademark of SGS-Thomson Microelectronics, Inc.
† *SIDACtor* is a trademark of Teccor, Inc.

T7256 Reference Circuit (continued)

Table 2. T7256 Reference Schematic Parts List (continued)

Reference Designator	Description	Source	Alternate Part
C23	1.0 µF 250 V ± 10% polyester capacitor	multiple	Example: Illinois Capacitor 105MWR250K1UF (708) 675-1760 ASC Capacitors Type X665 (818) 710-8555
C24, C25	680 pF ± 10% capacitors	multiple	—
R1, R3, R8, R15, R16	10 kΩ ± 10%, 1/8 W resistor	multiple	—
R2	825 Ω ± 10% , 1/4 W resistor	multiple	—
R4	17.8 kΩ ± 10%, 1/8 W resistor	multiple	—
R5, R6	16.9 Ω ± 1%, 1/4 W resistor	multiple	—
R7	2.2 MΩ ± 10%, 1/8 W resistor	multiple	—
R9	68.1 Ω ± 1% , 1/4 W resistor	multiple	—
R10, R11	16.9 Ω ± 1%, 1/4 W resistor	multiple	—
R12	2.2 kΩ ± 5%, 4 W resistor	multiple	—
R13, R14	75 Ω ± 1%, 1/8 W resistor	multiple	—
R17, R18, R19, R20	46.4 Ω ± 1%. 1/8 W resistor	multiple	—
R21, R22, R23, R24	100 Ω ± 1%, 1/8 W resistor	multiple	—

Note: The AT&T 2754K2 and the Valor PT4084 have different winding resistances than the AT&T 2754H2, and therefore require a change to the line side resistors (R10 and R11). In addition, if the Raychem TR600-150 PTC is used in place of the BEL fuse at location F1 to provide more robust protection (at a slightly higher cost), the line side resistors must be adjusted to compensate for the added PTC resistance of 12 Ω. The following table lists the necessary resistor values for these cases. Note that R10 and R11 are specified at 1%. This is due to the fact that the values were chosen from standard 1% resistor tables. When a PTC is used, the overall tolerance will be greater than 1% and R10 and R11 won't necessarily be matched. This is acceptable, as long as the total line side resistance is kept as close as possible to the ideal value. See Questions and Answers #11 for more details.

Table 3. Line Side Resistor Requirements

Transformer	When BEL Fuse Is Used	When TR600-150 Is Used	
	R10, R11	R10	R11
AT&T 2754H2	16.9 Ω	4.87 Ω	16.9 Ω
AT&T 2754K2	13.7 Ω	1.69 Ω	13.7 Ω
Valor PT4084	5.36 Ω	0 Ω	0 Ω

U-Interface Description

The T7256 U-interface transceiver circuitry is designed to allow systems to meet the loop-range requirements of ANSI standard T1.601 and ETSI technical report DTR/TM 3002 when the interface is used with the proper external circuitry.

Analog Interface

At the U-interface, proper line termination is required to meet the 2B1Q pulse templates and to achieve maximum loop range performance. Figures 6 and 7 show typical circuits for connecting the T7256 to the 2-wire loop; however, a specific application may vary depending on the system requirements.

The transmit outputs of the T7256 (LOP, LON) are connected to the interface transformer through 16.9 Ω ± 1% resistors, while the internal hybrid connections (HP, HN) are made directly to the device side of the transformer. A 1.5:1 turns ratio transformer, such as the AT&T 2754H2, is used to isolate the device from the loop plant. The center tap of the line side of the transformer is connected through a 1.0 µF ± 10% dc blocking capacitor.

The transformer line side is connected to the loop through 16.9 Ω ± 1% resistors. Secondary overvoltage protection is typically required on the device side of the transformer to protect the device. Primary overvoltage and overcurrent protection at the line interface is required for protecting the device and the equipment as well as providing safety to equipment users. The protection scheme shown in Figure 6 should be adequate for meeting *UL**1459 and FCC part 68 surge and safety requirements. For an in-depth discussion of surge protection issues when interfacing to the subscriber loop, the following application notes are available.

1. "Overvoltage Protection of Solid State Subscriber Loop Circuits", *AT&T Analog Line Card Components Data Book* (CA92-008TCOM) 800-372-2447.
2. *Protection of Telecommunications Customer Premises Equipment*, Raychem Corporation, 800-272-9243.

The ISDN termination circuitry (AT&T LH1465AB) is connected across tip and ring to provide the dc termination characteristics described in ANSI T1.601 section 7.5. Also, the LH1465AB, in conjunction with the 6N139 optoisolator, provides signal translation from the ac and dc signaling formats described in ANSI T1.601 section 6.5 (for NT maintenance testing) to a TTL-level format compatible with the T7256 OPTOIN input pin levels. The LH1465AB-based circuitry is for North American applications.

* *UL* is a registered trademark of Underwriters Laboratories, Inc.

U-Interface Description (continued)

Superframe Structure

Data is transmitted over the U-interface in 240-bit groups called U frames. Each U frame consists of an 18-bit synchronization word or inverted synchronization word (SW or ISW), 12 blocks of 2B+D data (216 bits), and six overhead bits (M bits). A U-interface superframe consists of eight U frames grouped together. The beginning of a U superframe is indicated by the inverted sync word (ISW). The six overhead bits (M1—M6) from each of the eight U frames, when taken together, form the 48 M bits. Figure 8 shows how U frames, superframes, and M bits are arranged.

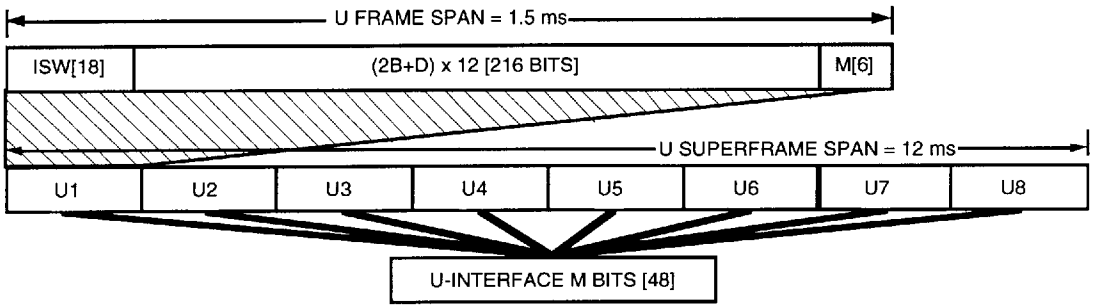


Figure 8. U-Interface Frame and Superframe

Of the 48 M bits, 24 bits form the embedded operations channel (eoc) for sending messages from the LT to the NT and responses from the NT to the LT. There are two eoc messages per superframe with 12 bits per eoc message (eoc1 and eoc2). Another 12 bits serve as U-interface control and status bits (UCS). The last 12 bits form the cyclic redundancy check (CRC) which is calculated over the 2B+D data and the M4 bits of the previous superframe. Figure 9 and Table 4 show the different groups of bits in the superframe.

U-Interface Description (continued)

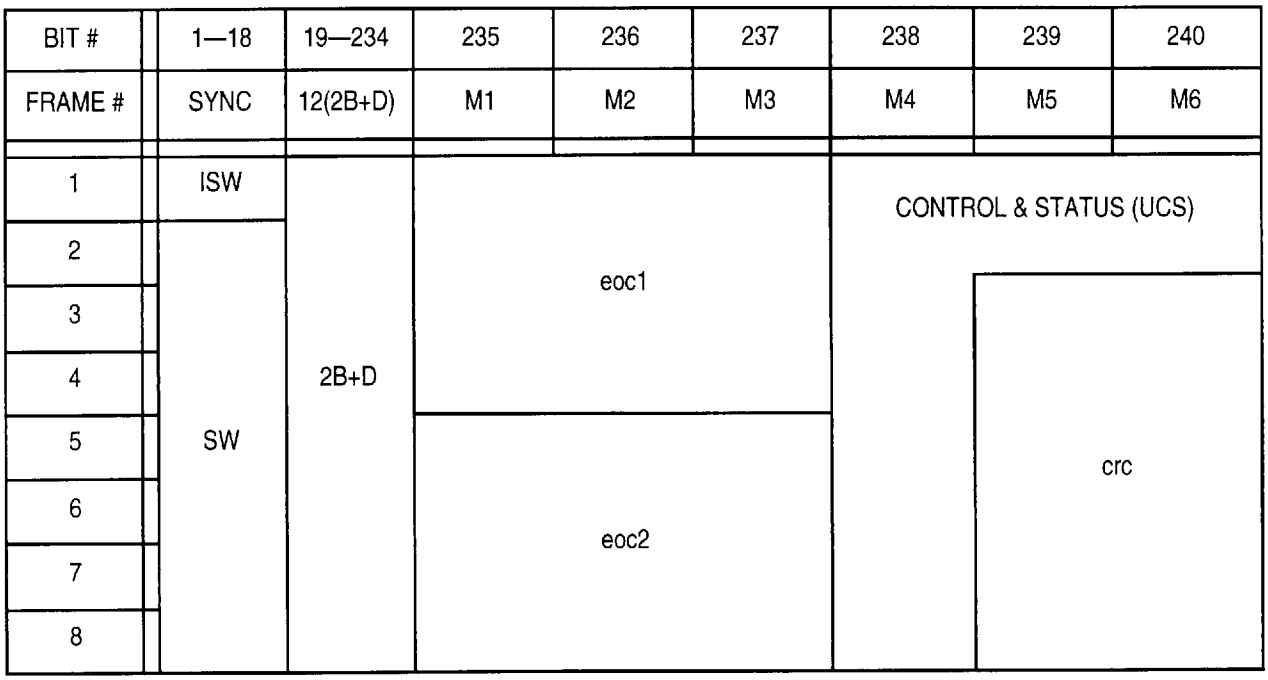


Figure 9. U-Interface Superframe Bit Groups

Bit Assignments

Table 4. U-Interface Bit Assignment

Bit #	1—18	19—234	235	236	237	238	239	240
Frame #	Sync	12(2B+D)	M1	M2	M3	M4	M5	M6
1	ISW	2B+D	eoc_{a1}	eoc_{a2}	eoc_{a3}	act	$R_{1,5}$	$R_{1,6}$
2	SW	2B+D	eoc_{dm}	eoc_{i1}	eoc_{i2}	dea (ps1)*	$R_{2,5}$	febe
3	SW	2B+D	eoc_{i3}	eoc_{i4}	eoc_{i5}	$R_{3,4}$ (ps2)*	crc_1	crc_2
4	SW	2B+D	eoc_{i6}	eoc_{i7}	eoc_{i8}	$R_{4,4}$ (ntm)*	crc_3	crc_4
5	SW	2B+D	eoc_{a1}	eoc_{a2}	eoc_{a3}	$R_{5,4}$ (cso)*,†	crc_5	crc_6
6	SW	2B+D	eoc_{dm}	eoc_{i1}	eoc_{i2}	$R_{6,4}$	crc_7	crc_8
7	SW	2B+D	eoc_{i3}	eoc_{i4}	eoc_{i5}	uoa (sai)*	crc_9	crc_{10}
8	SW	2B+D	eoc_{i6}	eoc_{i7}	eoc_{i8}	aib (nib)*,‡	crc_{11}	crc_{12}

* LT(NT). Values in parentheses () indicate meaning at the NT.
† cso is fixed at 0 by the device to indicate both cold and warm start capability.
‡ nib is fixed at 1 by the device to indicate the link is normal.

S/T-Interface Description

The T7256 S/T-interface is designed to allow systems to meet the requirements of the ANSI T1.605 standard, ITU-T I.430 recommendation, and ETSI ETS 300 012 when used with the proper external circuitry. The connection of a T7256 NT endpoint to a TE is shown in Figure 7. For an in-depth discussion of ISDN S/T line interface issues refer to the November 1993 *Design of ISDN S/T Line Interface Circuitry Using the T7250C/T7259* Application Note (AP93-008TCOM).

Analog Interface

The S/T-interface consists of two sections. The line transmitter and the line receiver are essentially stand-alone designs, except for limited sharing of timing and control circuits. The transmitter-receiver pair connects to 2.5:1 transformers. The transmitter connects to the transformer through 121 Ω ± 1% resistors. The receiver connects to the transformer through 10 kΩ ± 10% resistors.

The line transmitter is a voltage-limited current source that conforms to the I.430/T1.605 specifications. The transmitted bits are timed by an internal 192 kHz clock derived from the U-interface. Table 5 summarizes the mechanism used by the transmitter to send the alternate space inversion (ASI) code through the transmit transformer.

ASI is a differential strategy, with positive and negative rails connecting to the transformer. Current flows through the transformer only when there is a voltage difference on the two rails. When a logical one or mark is being sent, meaning no current is desired, both rails go to a high-impedance condition. When a positive logical zero (space) is transmitted, the positive rail forces current to the negative rail through the transformer. The reverse occurs for a negative zero.

The line receiver is more complex. Since the loop length to the subscriber(s) is variable, as is the number of TEs on the loop (1 to 8), the receiver must be sufficiently intelligent to adjust for widely varying input waveforms. The S/T receiver is designed to use a single adaptive timing mode to synchronize to all signals conforming to the I.430 templates. This mode can be used on any loop configuration (point-to-point, extended passive bus, short passive bus) in which round trip delays are between 0 µs and 42 µs and differential delays between TEs are between 0 µs and 3.1 µs. This means that if the line transmitter and the line receiver are directly connected externally in a loopback configuration, the receiver can extract the 2B+D information correctly from the transmitted stream.

A short passive bus configuration permits TEs to be connected anywhere along the full length of the cable, with the restriction that the total round trip delay must be between 10 µs and 14 µs for all TEs. Thus, worst-case differential delay between TEs can be as much as 4 µs. If the differential delay is more than 3.1 µs, adaptive timing mode cannot be used. A fixed timing mode is available for this case. The fixed timing mode is invoked through the FT microprocessor bit (if TDMEN = 0) or the FTE pin (if TDMEN = 1). When the T7256 uses fixed timing, the input stream is sampled 4.2 µs after the leading edge of each 192 kHz transmit bit interval.

The interval required for the receiver to synchronize to the received stream is 5 to 60 S/T frames (1.25 ms to 15 ms). The receiver can achieve framing only when the INFO 3 pattern appears on the loop. Three frames are required to recognize new INFO patterns.

Table 5. Line Transmission Code

Positive Rail	Negative Rail	Current	Logic
Z*	Z*	0	1
1	0	+1	0
0	1	−1	0

* Z = high impedance.

Frame and Multiframe Bit Assignments

The S/T-interface transfers its subscriber line 2B+D information as a 192 kbits/s full-duplex signal grouped into frames of 48 bits with a period of 250 µs, as specified in the ITU-T I.430/ANSI T1.605 standard. Thirty-six of the 48 bits sent in each direction convey user information (two 8-bit occurrences of each of the two B channels, and four D channel bits). The remaining 12 bits per frame are used for framing, control, dc balance, and maintenance. The frame structures are shown in each direction in Figure 10.

In the bit stream transmitted from the terminal endpoint (TE) to the network termination (NT), 4 bits are used for framing (F and FA, each with a dc balancing bit L), eight L bits are used to balance the 32 B channel bits, and 4 bits are D channel bits.

S/T-Interface Description (continued)

For the NT-to-TE transmission, 4 bits (F with dc balancing bit L, FA, and N) are used for framing, one M bit marks the start of a 20-frame multiframe, four E bits form an echo channel for retransmission of the D channel bits received from the TE, one L bit is used to balance the contents of the entire frame, and 1 bit (A) is set to one when bit synchronization is achieved between TE and NT as part of the INFO 4 state. One S bit is used for transmitting S subchannel messages in an NT-to-TE multiframe.

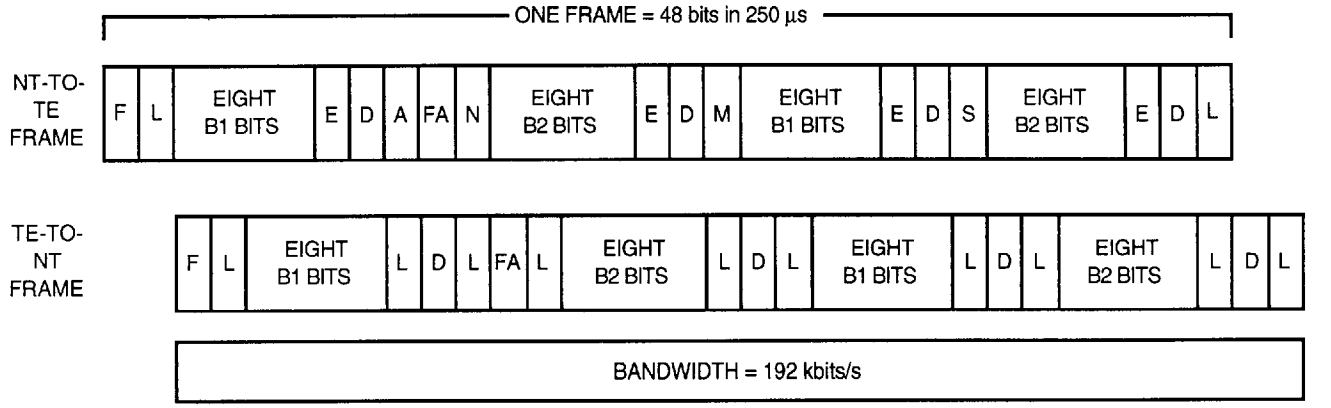
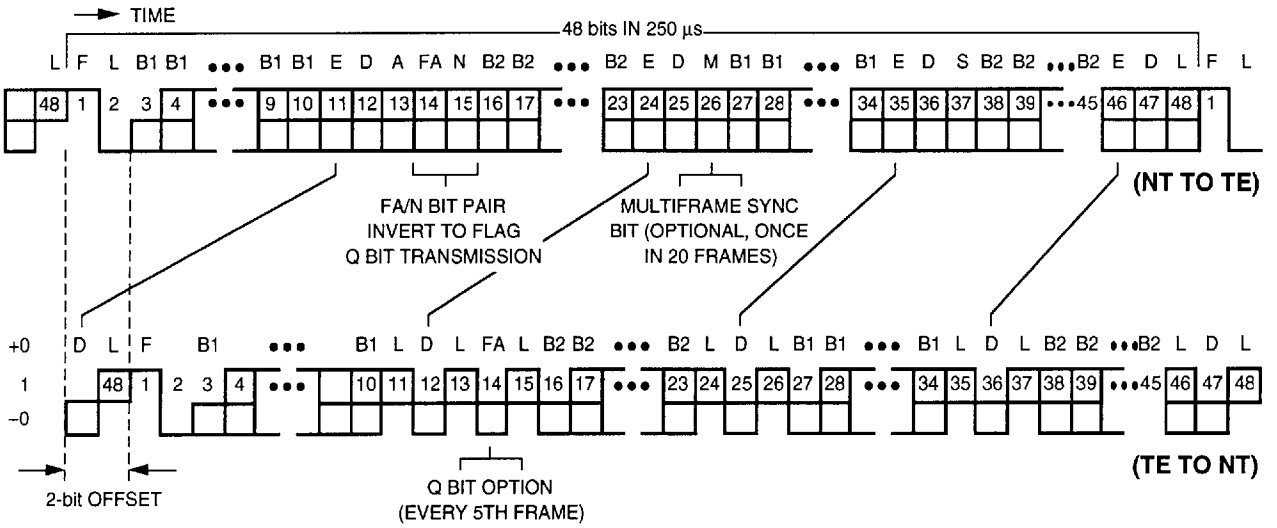


Figure 10. Frame Structures of NT and TE Frames

S/T-Interface Description (continued)

The framing procedure uses bipolar line-code violations to establish synchronization. Since the last binary 0 of any frame is a positive pulse and the F bit is also defined to be a positive pulse (see Figure 11), the first bit of each frame represents a coding violation. In addition, the second bit of each frame, a balance bit, is a negative pulse, and the next binary 0 in the frame is forced to be negative, causing another violation. Both bipolar violations allow framing and provide dc balance. All other pulses follow the alternating convention.

In the TE-to-NT direction, in at least four of five frames, this second violation occurs within 13 bits of the F bit. If this coding algorithm is not maintained, the receiver loses synchronization, but the T7256 continues transmitting.



F = Framing bit
L = DC balancing bit
D = D channel bit
E = Echo D channel bit
FA = Auxiliary framing bit or Q channel bit
N = Bit set to binary value N = FA
A = Activation bit
S = S channel bit
M = Multiframe synchronization bit
B1 = Bit within B channel 1
B2 = Bit within B channel 2

Signals from NT to TE		Signals from TE to NT	
INFO 0	No signal.	INFO 0	No signal.
INFO 2	Frame with all bits of B, D, and D echo (E) channels set to binary ZERO; bit A set to binary ZERO; N and L bits set according to the normal coding rules.	INFO 1	A continuous signal with the following pattern: positive ZERO, negative ZERO, six ONEs. 
INFO 4	Frames with operational data on B, D, and E channels; bit A set to binary ONE.	INFO 3	Synchronized frames with operational data on B and D channels.

Figure 11. Details of NT and TE Frames

S/T-Interface Description (continued)

If multiframing is enabled, the M bit in the NT-to-TE direction is set to a one every 20 frames and the FA bit is set to one every five frames. The TE recognizes these states and, in returned frames immediately corresponding to those in which the NT set the FA bit, replaces the FA bit it sends to the NT with a Q bit (Q1 through Q4). Q1 is returned for each frame in which both the M and FA bits were set to one by the NT, with Q2 through Q4 following at five-frame intervals. (See Figure 12.)

Microprocessor Interface Description

The microprocessor interface, used to control and monitor the device, is compatible with most general-purpose serial microprocessor interfaces using a synchronous mode of transmission. Transmission from the microprocessor to the T7256 occurs in a 2-byte format, the first byte representing read/write and register address command information and the second byte being write data or don't cares for a read operation. Transmission from the T7256 to the microprocessor carries register data only. The interrupt line to the microprocessor is maskable and can be used to signal the microprocessor to initiate a register read or write operation. A more detailed description of the operation is given below, and detailed timing information is given in the Timing Characteristics section.

Registers

The on-chip registers are divided by major circuit block and by status and control function. Microprocessor register control bits associated with the control flow state machine, eoc state machine, and multiframing controller are ignored when those blocks are enabled (the state machines affect the control automatically). When the blocks are disabled, the control bits are used to drive device operations. The functional summary of the registers and bits is shown in Figure 13 and Figure 14.

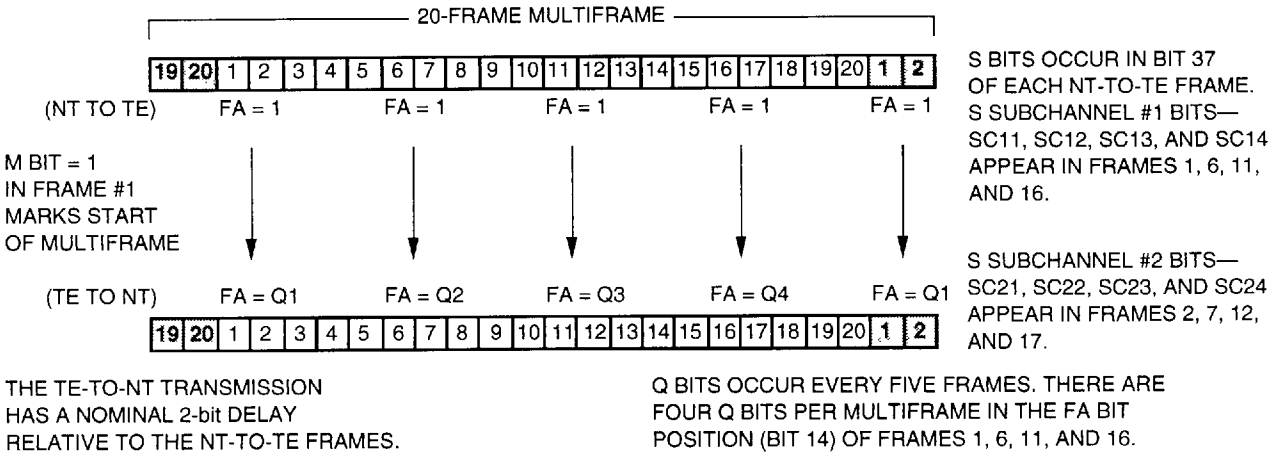


Figure 12. Multiframing—S Subchannels and Q Subchannels

Microprocessor Interface Description (continued)

ADDRESS			
00000	GR0	R/W	GLOBAL DEVICE CONTROL — DEVICE CONFIGURATION
00001	GR1	R/W	GLOBAL DEVICE CONTROL — U-INTERFACE
00010	GR2	R/W	GLOBAL DEVICE CONTROL — S/T-INTERFACE
00011	DFR0	R/W	DATA FLOW CONTROL — U & S/T B CHANNELS
00100	DFR1	R/W	DATA FLOW CONTROL — D CHANNELS & TDM BUS
00101	TDR0	R/W	TDM BUS TIMING CONTROL
00110	CFR0	R/W	CONTROL FLOW SM CONTROL — MAINTEN./RSV. BITS
00111	CFR1	R	CONTROL FLOW SM STATUS
01000	CFR2	R	CONTROL FLOW SM STATUS — RESERVED BITS
01001	ECR0	R/W	eoc STATE MACHINE CONTROL — ADDRESS
01010	ECR1	R/W	eoc STATE MACHINE CONTROL — INFORMATION
01011	ECR2	R	eoc STATE MACHINE STATUS — ADDRESS
01100	ECR3	R	eoc STATE MACHINE STATUS — INFORMATION
01101	MCR0	R	Q CHANNEL BITS
01110	MCR1	R/W	S SUBCHANNEL 1
01111	MCR2	R/W	S SUBCHANNEL 2
10000	MCR3	R/W	S SUBCHANNEL 3
10001	MCR4	R/W	S SUBCHANNEL 4
10010	MCR5	R/W	S SUBCHANNEL 5
10011	UIR0	R	U-INTERFACE INTERRUPT REGISTER
10100	UIR1	R/W	U-INTERFACE INTERRUPT MASK REGISTER
10101	SIR0	R	S/T-INTERFACE INTERRUPT REGISTER
10110	SIR1	R/W	S/T-INTERFACE INTERRUPT MASK REGISTER
10111	MIR0	R	MAINTENANCE INTERRUPT REGISTER
11000	MIR1	R/W	MAINTENANCE INTERRUPT MASK REGISTER
11001	GIR0	R	GLOBAL INTERRUPT REGISTER

Figure 13. Functional Register Map (Addresses)

Microprocessor Interface Description (continued)

REG	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
GR0	R/W	RESERVED	AUTOACT	MULTIF	AUTOEOC	AUTOCTL	CRATE1	CRATE0	RESET
GR1	R/W	SAI1	SAI0	XPCY	ACTT	NTM	PS1	PS2	LPBK
GR2	R/W	STOA	ACTSEL	TDMEN	U2BDLN	SXE	SRESET	SPWRUD	FT
DFR0	R/W	SXB21	SXB20	SXB11	SXB10	UXB21	UXB20	UXB11	UXB10
DFR1	R/W	TDMDU	TDMB2U	TDMB1U	TDMDS	TDMB2S	TDMB1S	SXD	UXD
TDR0	R/W	—	—	—	—	FSP	FSC2	FSC1	FSC0
CFR0	R/W	—	—	R64T	R25T	R16T	R15T	AFRST	ILOSS
CFR1	R	I4I	AIB	FEBE	NEBE	UOA	OOF	XACT	ACTR
CFR2	R	—	R64R	R54R	R44R	R34R	R15R	R16R	R15R
ECR0	R/W	CCRC	U2BDLT	UB2LP	UB1LP	DMT	A1T	A2T	A3T
ECR1	R/W	I1T	I2T	I3T	I4T	I5T	I6T	I7T	I8T
ECR2	R	—	—	—	—	DMR	A1R	A2R	A3R
ECR3	R	I1R	I2R	I3R	I4R	I5R	I6R	I7R	I8R
MCR0	R	—	—	—	—	Q1	Q2	Q3	Q4
MCR1	R/W	—	—	—	—	SC11	SC12	SC13	SC14
MCR2	R/W	—	—	—	—	SC21	SC22	SC23	SC24
MCR3	R/W	—	—	—	—	SC31	SC32	SC33	SC34
MCR4	R/W	—	—	—	—	SC41	SC42	SC43	SC44
MCR5	R/W	—	—	—	—	SC51	SC52	SC53	SC54
UIR0	R	—	—	TSFINT	RSFINT	OUSC	BERR	ACTSC	EOCSC
UIR1	R/W	—	—	TSFINTM	RSFINTM	OUSCM	BERRM	ACTSCM	EOCSCM
SIR0	R	—	—	—	—	I4C	SFECV	QSC	SOM
SIR1	R/W	—	—	—	—	I4CM	SFECVM	QSCM	SOMM
MIR0	R	—	—	—	—	—	EMINT	ILINT	QMINT
MIR1	R/W	—	—	—	—	—	EMINTM	ILINTM	QMINTM
GIR0	R	—	—	—	—	—	MINT	SINT	UINT

Figure 14. Functional Register Map (Bit Assignments)

Microprocessor Interface Description (continued)

Table 6. Global Device Control — Device Configuration (Address 00000)

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GR0	R/W	Rsv.	AUTOACT	MULTIF	AUTOEOC	AUTOCTL	CRATE1	CRATE0	RESET
Default State on $\overline{\text{RESET}}$		1	SCK	1	1	1	1	1	1

Register	Bit	Symbol	Name/Description
GR0	0	RESET	**Reset.** Same function as external $\overline{\text{RESET}}$ pin, except U-interface timing recovery is not reset and the state of the SCK, $\overline{\text{INT}}$, and SDI pins are not checked. Assertion of this bit halts data transmission, clears adaptive filter coefficients, resets the S/T-interface transceiver, and sets all microprocessor register bits (except itself) to their default state. The microprocessor must write this bit back to a 1 to bring the T7256 out of its RESET state. During reset, the U-interface transmitter produces 0 V and the output impedance is 135 Ω at tip and ring. 0 — Reset. 1 — No effect on device operation (default).
GR0	2—1	CRATE[1:0]	**CKOUT Rate Control.** 00 — Not used. 01 — 10.24 MHz synchronous with U-interface (if active); otherwise, free-running. 10 — 15.36011 MHz free-running. 11 — tristate (default).
GR0	3	AUTOCTL	**Auto Control Enable.** Enables automatic control of ANSI maintenance and reserved bit insertion. When AUTOCTL = 1, register CFR0 is ignored and the control flow state machine automatically controls ANSI maintenance functions and reserved bit insertion. When AUTOCTL = 0, the microprocessor controls ANSI maintenance functions and reserved bit insertion via register CFR0. 0 — CFR0 functions controlled manually by microprocessor. 1 — CFR0 functions controlled automatically.
GR0	4	AUTOEOC	**Automatic eoc Processor Enable.** Enables eoc state machine which implements eoc processing per the ANSI standard. When AUTOEOC = 1, registers ECR0—ECR1 are ignored. The eoc state machine only responds to addresses 000 and 111 as valid addresses. 0 — eoc state machine disabled. 1 — eoc state machine enabled (default).
GR0	5	MULTIF	**Multiframing Control.** Enables the multiframing controller and allows the microprocessor to access the S and Q channels. When disabled, multiframing is not implemented (the NT transmits all 0s in the F_A and M bit positions and all 1s in the S bit positions to the TE). Also, register bits 3—0 in MCR0 are forced to 1 and register bits 3—0 in MCR1—5 are forced to 0 when multiframing is disabled. 0 — Multiframing controller enabled. 1 — Multiframing controller disabled (default).
GR0	6	AUTOACT	**Automatic Activation Control.** Upon a 1-to-0 transition of the AUTOACT bit, the control flow state machine attempts one activation of the U-interface (if uoa = 0), or one activation of the S/T- and U-interfaces (if uoa = 1). If the U-interface is successfully activated, this bit is internally set to 1. If the SCK pin is held low during an external $\overline{\text{RESET}}$, AUTOACT is written to 0 and one activation attempt is made (see SCK pin description in Table 1). Multiple activation attempts can be made by toggling this bit. 0 — No effect on device operation. 1 — No activation attempt. 0 to 1 — No effect on device operation. 1 to 0 — One activation attempt.
GR0	7	—	**Reserved.** Set to 1. 1 — Default.

Microprocessor Interface Description (continued)

Table 7. Global Device Control — U-Interface (Address 00001)

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GR1	R/W	SAI1	SAI0	XPCY	ACTT	NTM	PS1	PS2	LPBK
Default State on $\overline{\text{RESET}}$		1	1	1	0	1	1	1	1

Register	Bit	Symbol	Name/Description
GR1	0	LPBK	**U-Interface Analog Loopback.** Controls analog loopback of U-interface data stream from transmit to receive. Loopback turns off the echo canceler and reconfigures the scrambler. U transceiver should be reset using AFRST, and the line should be disconnected before loopback test. The ISTP bit should be set to 1 during loopback. 0 — U-interface analog loopback. 1 — No effect on device operation (default).
GR1	1	PS2	**Power Status #2.** Controls PS2 bit in transmit U-interface data stream if TDMEN = 0. If TDMEN = 1, PS2 bit is ignored. For ANSI T1.601 applications, PS1 and PS2 indicate the NT power status via the following messages: **PS1 PS2 Power Status** 0 0 Dying gasp. 0 1 Primary power out. 1 0 Secondary power out. 1 1 All power normal (default).
GR1	2	PS1	**Power Status #1.** Controls PS1 bit in transmit U-interface data stream if TDMEN = 0. If TDMEN = 1, PS1 bit is ignored. See PS2 bit definition.
GR1	3	NTM	**NT Test Mode.** Controls ntm bit in transmit U-interface data stream and indicates if the NT is in a customer-initiated test mode. 0 — NT is currently in a customer-initiated test mode. 1 — No effect on device operation (default).
GR1	4	ACTT	**Transmit Activation.** Controls act bit in transmit U-interface data stream. 0 — No effect on device operation (default). 1 — Ready to transmit.
GR1	5	XPCY	**Transparency.** Controls data being transmitted at U-interface. 0 — Enable data transparency. 1 — No effect on device operation (default).
GR1	7—6	SAI[1:0]	**S/T-Interface Activity Indicator Control.** Controls sai bit in transmit U-interface data stream. For ANSI T1.601 applications, the sai bit is set to 1 to indicate to the network that there is activity (INFO 1 or INFO 3) at the S/T reference point. Otherwise, it is set to 0. The SAI[1:0] bits provide the following options for controlling the sai bit: 00 — Forces sai to 0 on the U-interface. 01 — Forces sai to 1 on the U-interface. 10 — sai is set internally according to S-interface activity. 11 — sai is set internally according to S-interface activity (default).

Microprocessor Interface Description (continued)

Table 8. Global Device Control — S/T-Interface (Address 00010)

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GR2	R/W	STOA	ACTSEL	TDMEN	U2BDLN	SXE	SRESET	SPWRUD	FT
Default State on $\overline{\text{RESET}}$		1	$\overline{\text{INT}}$	1	1	1	1	1	1

Register	Bit	Symbol	Name/Description
GR2	0	FT	**Fixed/Adaptive Timing Control.** Controls mode of timing recovery on S/T-interface if TDMEN = 0. If TDMEN = 1, FT is ignored. 0 — Fixed timing. 1 — Adaptive timing (default).
GR2	1	SPWRUD	**S/T-Interface Powerdown Control.** When 0, this bit forces the S/T-interface to remain in a powerdown mode. This is the same low-power mode the S/T-interface is in when the T7256 is in its IDLE state with no activity on the U- or S/T-interfaces. In this mode, all S/T-interface circuits are powered down, except for circuits required to detect an activation request from a TE. 0 — Powerdown. 1 — Normal (default).
GR2	2	SRESET	**S/T-Interface Reset.** While 0, this bit causes a reset of the S/T-interface, initializing the interface in the same manner as the external $\overline{\text{RESET}}$ pin. Must be set to 1 for normal operation. 0 — Reset. 1 — Normal (default).
GR2	3	SXE	**S/T-Interface D Channel Echo Bit Control.** Controls data in E channel from NT to TE on S/T-interface. This bit must be cleared during 2B+D loopbacks to meet ITU-T I.430 requirements. 0 — All 0s. 1 — Echoes D channel from S/T receive path (default).
GR2	4	U2BDLN	**Nontransparent 2B+D Loopback Control.** When 0, this bit causes a non-transparent loopback of 2B+D data from U receiver to U transmitter upstream of the data flow matrix. Note that this loopback path is not as close to the S/T-interface as the transparent loopback initiated by U2BDLT (register ECR0, bit 6). This loopback may be useful for test purposes. When this bit is set, the upstream data (NT to LT direction) will be forced to all 1s until either ACTR = 1 (register CFR1, bit 0) or XPCY = 0 (register GR1, bit 5). 0 — 2B+D loopback. All 1s 2B+D data is automatically generated towards the TE. 1 — No loopback (default).
GR2	5	TDMEN	**TDM Bus Select.** Selects functions of pins 4, 7, 8, and 9. 0 — TDM bus functions. Pins 4, 7, 8, and 9 configured as FS, TDMDI, TDMDO, and TDMCLK, respectively. See DFR1 and TDR0 registers for TDM bus programming details. Microprocessor register bits GR11, GR12, and GR20 control the PS2, PS1, and FT functions. 1 — No TDM bus. Pins 4, 7, 8, and 9 configured as SYN8K/LBIND, FTE, PS2E, and PS1E, respectively (default).

Microprocessor Interface Description (continued)

Table 8. Global Device Control — S/T-Interface (Address 00010) (continued)

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GR2	R/W	STOA	ACTSEL	TDMEN	U2BDLN	SXE	SRESET	SPWRUD	FT
Default State on $\overline{\text{RESET}}$		1	$\overline{\text{INT}}$	1	1	1	1	1	1

Register	Bit	Symbol	Name/Description
GR2	6	ACTSEL	**ACT Mode Select.** Controls the state of the transmitted ACT bit when an eoc loopback 2 (2B+D loopback) is requested. The loopback 2 occurs automatically if AUTOEOC = 1 (register GR0, bit 4). Otherwise, bit U2BDLT (register ECR0, bit 6) must be set to 0. The loopback is accomplished in the device by looping the output of the S/T transmitter back to the input of the S/T receiver at the device pins (i.e., as close to the S/T-interface as possible). The S/T transceiver will ignore any signals transmitted by the TE, and the T7256 will synchronize to its own transmit signal causing INFO 3 to be reported. The initial state of ACTSEL is determined by the state of the $\overline{\text{INT}}$ pin on the rising edge of $\overline{\text{RESET}}$. 0 — act = 0 during loopback 2 (per ANSI T1.601). The data received at the NT is looped back towards the LT as soon as the 2B+D loopback is enabled. 1 — act = 1 during loopback 2 after INFO 3 is recognized at the S/T-interface (per ETSI DTR/TM 3002). The data received by the NT is not looped back towards the LT until after ACT = 1 is received from the LT. Prior to this time, 2B+D data toward the LT is all 1s.
GR2	7	STOA	**S/T Only Activation.** Set to 0 to force an S/T activation when the U-interface is inactive. When the U-interface is active, this bit is ignored. STOA is reset to 1 upon the receipt of a U-interface tone or a 1-to-0 transition of AUTOACT. 0 — Attempt an S/T only activation. 1 — No effect on device operation (default).

Microprocessor Interface Description (continued)

Table 9. Data Flow Control — U and S/T B Channels (Address 00011)

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DFR0	R/W	SXB21	SXB20	SXB11	SXB10	UXB21	UXB20	UXB11	UXB10
Default State on $\overline{\text{RESET}}$		1	1	1	1	1	1	1	1

Register	Bit	Symbol	Name/Description
DFR0	1—0	UXB1[1:0]	**U-Interface Transmit Path Source for B1 Channel.** Refer to point #1 in Figure 19. 00 — Not used. 01 — TDM bus. 10 — All 1s. 11 — S/T-interface receive (default).
DFR0	3—2	UXB2[1:0]	**U-Interface Transmit Path Source for B2 Channel.** Refer to point #1 in Figure 19. 00 — Not used. 01 — TDM bus. 10 — All 1s. 11 — S/T-interface receive (default).
DFR0	5—4	SXB1[1:0]	**S/T-Interface Transmit Path Source for B1 Channel.** Refer to point #2 in Figure 19. 00 — Not used. 01 — TDM bus. 10 — S/T-interface receive (ITU-T I.430 LoopC for B1 channel). 11 — U-interface receive (default).
DFR0	7—6	SXB2[1:0]	**S/T-Interface Transmit Path Source for B2 Channel.** Refer to point #2 in Figure 19. 00 — Not used. 01 — TDM bus. 10 — S/T-interface receive (ITU-T I.430 LoopC for B2 channel). 11 — U-Interface receive (default).

Microprocessor Interface Description (continued)

Table 10. Data Flow Control — D Channels and TDM Bus (Address 00100)

Bits 2—7 are enabled only if TDMEN = 0 (register GR2, bit 5). The TDMCLK and FS outputs are activated if any one of bits 2—7 are enabled. The TDMDO output is activated during time slots enabled by programming bits 2—7.

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DFR1	R/W	TDMDU	TDMB2U	TDMB1U	TDMDS	TDMB2S	TDMB1S	SXD	UXD
Default State on $\overline{\text{RESET}}$		1	1	1	1	1	1	1	1

Register	Bit	Symbol	Name/Description
DFR1	0	UXD	**U-Interface Transmit Path Source for D Channel.** Refer to point #1 in Figure 19. 0 — TDM bus. 1 — S/T-interface receive (default).
DFR1	1	SXD	**S/T-Interface Transmit Path Source for D Channel.** Refer to point #2 in Figure 19. 0 — TDM bus. 1 — U-interface receive (default).
DFR1	2	TDMB1S	**TDM Bus Transmit Control for B1 Channel from S/T-Interface.** Refer to point #3 in Figure 19. Controls transmit time slot allocated on TDM bus for B1 channel derived from S/T-interface receiver. 0 — Time slot enabled. 1 — Time slot disabled (high impedance) (default).
DFR1	3	TDMB2S	**TDM Bus Transmit Control for B2 Channel from S/T-Interface.** Refer to point #3 in Figure 19. Controls transmit time slot allocated on TDM bus for B2 channel derived from S/T-interface receiver. 0 — Time slot enabled. 1 — Time slot disabled (high impedance) (default).
DFR1	4	TDMDS	**TDM Bus Transmit Control for D Channel from S/T-Interface.** Refer to point #3 in Figure 19. Controls transmit time slot allocated on TDM bus for D channel derived from S/T-interface receiver. 0 — Time slot enabled. 1 — Time slot disabled (high impedance) (default).
DFR1	5	TDMB1U	**TDM Bus Transmit Control for B1 Channel from U-Interface.** Refer to point #3 in Figure 19. Controls transmit time slot allocated on TDM bus for B1 channel derived from U-interface receiver. 0 — Time slot enabled. 1 — Time slot disabled (high impedance) (default).
DFR1	6	TDMB2U	**TDM Bus Transmit Control for B2 Channel from U-Interface.** Refer to point #3 in Figure 19. Controls transmit time slot allocated on TDM bus for B2 channel derived from U-interface receiver. 0 — Time slot enabled. 1 — Time slot disabled (high impedance) (default).
DFR1	7	TDMDU	**TDM Bus Transmit Control for D Channel from U-Interface.** Refer to point #3 in Figure 19. Controls transmit time slot allocated on TDM bus for D channel derived from U-interface receiver. 0 — Time slot enabled. 1 — Time slot disabled (high impedance) (default).

Microprocessor Interface Description (continued)

Table 11. TDM Bus Timing Control (Address 00101)

Bits 0—4 are enabled only if TDMEN = 0 and one or more of bits DFR1[2:7] are set to 0.

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TDR0	R/W	—	—	—	—	FSP	FSC2	FSC1	FSC0
Default State on $\overline{\text{RESET}}$		—	—	—	—	1	1	1	1

Register	Bit	Symbol	Name/Description
TDR0	2—0	FSC[2:0]	**Frame Strobe (FS) Control.** Selects location of strobe envelope within TDM bus time slots. 000 — S/T-interface 2B+D channel strobe (18-bit envelope). 001 — U-interface 2B+D channel strobe (18-bit envelope). 010 — S/T-interface B2 channel strobe. 011 — U-interface B2 channel strobe. 100 — S/T-interface D channel strobe (2-bit envelope). 101 — U-interface D channel strobe (2-bit envelope). 110 — S/T-interface B1 channel strobe. 111 — U-interface B1 channel strobe (default).
TDR0	3	FSP	**Frame Strobe (FS) Polarity.** 0 — Active-low envelope. 1 — Active-high envelope (default).

Microprocessor Interface Description (continued)

Table 12. Control Flow State Machine Control — Maintenance/Reserved Bits (Address 00110)

This register has no effect on device operation if AUTOCTL = 1.

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CFR0	R/W	—	—	R64T	R25T	R16T	R15T	AFRST	ILOSS
Default State on $\overline{\text{RESET}}$		—	—	1	1	1	1	1	1

Register	Bit	Symbol	Name/Description
CFR0	0	ILOSS	**Insertion Loss Test Control.** The insertion loss test mode is initiated by setting AFRST = 0 and ILOSS = 0, and then setting AFRST = 1. When enabled, the U-interface transmitter continuously transmits the sequence SN1. The U-interface receiver remains reset. The U-interface transceiver performs an internal reset when the ILOSS bit returns to its inactive state. 0 — U-transmitter sends SN1 tone continuously. 1 — No effect on device operation (default).
CFR0	1	AFRST	**Adaptive Filter Reset.** U transceiver reset. Assertion of this bit halts U-interface data transmission and clears adaptive filter coefficients. During AFRST, the U transmitter produces 0 V and has an output impedance of 135 Ω. If the microprocessor interface is being used, the AFRST bit should be used to place the device in quiet mode for U-interface maintenance procedures. Assertion of AFRST does not reset the S/T transceiver, microprocessor register bits, or the U-interface timing recovery. 0 — U transceiver reset. 1 — No effect on device operation (default).
CFR0	3—2	R[16:15]T	**Transmit Reserved Bits.** Control R1,6 and R1,5 in transmit U-interface data stream. 11 — (default.)
CFR0	4	R25T	**Transmit Reserved Bit.** Controls R2,5 in transmit U-interface data stream. 1 — (default.)
CFR0	5	R64T	**Transmit Reserved Bit.** Controls R6,4 in transmit U-interface data stream. 1 — (default.)

Microprocessor Interface Description (continued)

Table 13. Control Flow State Machine Status (Address 00111)

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CFR1	R	I4I	AIB	FEBE	NEBE	UOA	OOF	XACT	ACTR

Register	Bit	Symbol	Name/Description
CFR1	0	ACTR	**Receive Activation.** Follows act bit in receive U-interface data stream. 0 — Pending activation. 1 — Ready to transmit.
CFR1	1	XACT	**U Transceiver Active.** 0 — Transceiver not active. 1 — Transceiver starting up or active.
CFR1	2	OOF	**Out of Frame.** 0 — U-interface out of frame. 1 — Normal.
CFR1	3	UOA	**U-Interface Only Activation.** Follows uoa bit in receive U-interface data stream. 0 — U-interface only for activation. 1 — U-interface and S/T-interface for activation.
CFR1	4	NEBE	**Near-End Block Error.** Follows nebe bit in receive U-interface data stream. 0 — CRC error detected in previously received U frame. 1 — No error.
CFR1	5	FEBE	**Far-End Block Error.** Follows febe bit in receive U-interface data stream. 0 — Error detected at LT. 1 — No error.
CFR1	6	AIB	**Alarm Indication Bit.** Follows aib in receive U-interface data stream. 0 — Failure of intermediate 2B+D transparent element. 1 — Transmission path established between LT and NT.
CFR1	7	I4I	**INFO 4 Indicator.** 0 — non-INFO 4. 1 — INFO 4.

Microprocessor Interface Description (continued)

Table 14. Control Flow State Machine Status — Reserved Bits (Address 01000)

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CFR2	R	—	R64R	R54R	R44R	R34R	R25R	R16R	R15R

Register	Bit	Symbol	Name/Description
CFR2	1—0	R[16:15]R	**Receive Reserved Bits.** Follow R1,5 and R1,6 in receive U-interface data stream.
CFR2	2	R25R	**Receive Reserved Bits.** Follows R2,5 in receive U-interface data stream.
CFR2	6—3	R[64:54:44:34]R	**Receive Reserved Bits.** Follow R3,4; R4,4; R5,4; and R6,4 in receive U-interface data stream.

Microprocessor Interface Description (continued)

Table 15. eoc State Machine Control — Address (Address 01001)

This register has no effect on device operation if AUTOEOC = 1.

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ECR0	R/W	CCRC	U2BDLT	UB2LP	UB1LP	DMT	A1T	A2T	A3T
Default State on $\overline{\text{RESET}}$		1	1	1	1	1	0	0	0

Register	Bit	Symbol	Name/Description
ECR0	0—2	A[3:1]T	**Transmit eoc Address.** 000 — NT address (default). 111 — Broadcast address.
ECR0	3	DMT	**Transmit eoc Data or Message Indicator.** 0 — Data. 1 — Message (default).
ECR0	4	UB1LP	**U-Interface Loopback of B1 Channel Control.** Control for U-interface transparent B1 loopback. UB1LP and UB2LP may be enabled concurrently. 0 — B1 channel loopback from U-interface receive to U-interface transmit upstream of data flow matrix. 1 — No loopback (default).
ECR0	5	UB2LP	**U-Interface Loopback of B2 Channel Control.** Control for U-interface transparent B2 loopback. UB1LP and UB2LP may be enabled concurrently. 0 — B2 channel loopback from U-interface receive to U-interface transmit upstream of data flow matrix. 1 — No loopback (default).
ECR0	6	U2BDLT	**Transparent 2B+D Loopback Control.** When activated, this bit causes a transparent 2B+D loopback from S/T transmitter to S/T receiver at the device pins (i.e., as close as possible to the S/T-interface) according to ITU-T I.430 Loop2. Any signals from the TE are ignored during this loopback. 0 — Transparent 2B+D loopback: The microprocessor must clear the D channel echo bit control (SXE = 0) and data flow matrix (SXB10 = SXB11 = SXB20 = SXB21 = SXD = UXB10 = UXB11 = UXB20 = UXB21 = UXD = 1) for proper operation of the loopback. 1 — No loopback (default).
ECR0	7	CCRC	**Corrupt Cyclic Redundancy Check.** Used to corrupt the CRC information transmitted at the U-interface. 0 — Corrupt CRC generation. 1 — Generate correct CRC (default).

Microprocessor Interface Description (continued)

Table 16. eoc State Machine Control — Information (Address 01010)

This register has no effect on device operation if AUTOEOC = 1.

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ECR1	R/W	I1T	I2T	I3T	I4T	I5T	I6T	I7T	I8T
Default State on $\overline{\text{RESET}}$		1	1	1	1	1	1	1	1

Register	Bit	Symbol	Name/Description
ECR1	0—7	I[8:1]T	**Transmit eoc Information.** These bits are transmitted as the eoc channel message when in manual eoc mode. See eoc State Machine Description section for a list of possible eoc messages.

Microprocessor Interface Description (continued)

Table 17. eoc State Machine Status — Address (Address 01011)

This register contains the currently received eoc address and data/message indicator bits independent of the state of AUTOEOC (register GR0, bit 4).

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ECR2	R	—	—	—	—	DMR	A1R	A2R	A3R

Register	Bit	Symbol	Name/Description
ECR2	0—2	A[3:1]R	**Receive eoc Address.** These bits store the received eoc address. 000 = NT address. 001—110 = Intermediate element addresses. 111 = Broadcast address.
ECR2	3	DMR	**Receive eoc Data or Message Indicator.** 0 — Data. 1 — Message.

Microprocessor Interface Description (continued)

Table 18. eoc State Machine Status — Information (Address 01100)

This register contains the currently received eoc information bits independent of the state of AUTOEOC (register GR0, bit 4).

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ECR3	R	I1R	I2R	I3R	I4R	I5R	I6R	I7R	I8R

Register	Bit	Symbol	Name/Description
ECR3	0—7	I[8:1]R	**Receive eoc Information.** Receive eoc channel message or data.

Microprocessor Interface Description (continued)

Table 19. Q Channel Bits (Address 01101)

These register bits are forced to 1 if MULTIF = 1 and during $\overline{\text{RESET}}$.

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MCR0	R	—	—	—	—	Q1	Q2	Q3	Q4

Register	Bit	Symbol	Name/Description
MCR0	0—3	Q[4:1]	**Q Channel Bits.** Four bits reflecting the four Q bits (Q1—Q4) received in the last completed multiframe. Bits are loaded at the end of the multiframe.

Microprocessor Interface Description (continued)

Table 20. S Subchannels 1—5 (Address 01110—10010)

These register bits have no effect on device operation and are set to 0 if MULTIF = 1. Refer to the Multiframing Controller Description section for more detail on using S and Q channels.

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MCR1	R/W	—	—	—	—	SC11	SC12	SC13	SC14
MCR2	R/W	—	—	—	—	SC21	SC22	SC23	SC24
MCR3	R/W	—	—	—	—	SC31	SC32	SC33	SC34
MCR4	R/W	—	—	—	—	SC41	SC42	SC43	SC44
MCR5	R/W	—	—	—	—	SC51	SC52	SC53	SC54
Default State on $\overline{\text{RESET}}$		—	—	—	—	0	0	0	0

Register	Bit	Symbol	Name/Description
MCR1	0—3	SC1[4:1]	**S Subchannel 1.**
MCR2	0—3	SC2[4:1]	**S Subchannel 2.**
MCR3	0—3	SC3[4:1]	**S Subchannel 3.**
MCR4	0—3	SC4[4:1]	**S Subchannel 4.**
MCR5	0—3	SC5[4:1]	**S Subchannel 5.**

Microprocessor Interface Description (continued)

Table 21. U-Interface Interrupt Register (Address 10011)

These bits are cleared during $\overline{\text{RESET}}$.

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
UIR0	R	—	—	TSFINT	RSFINT	OUSC	BERR	ACTSC	EOCSC

Register	Bit	Symbol	Name/Description
UIR0	0	EOCSC	**eoc State Change on U-Interface.** Activates (set to 1) when the received eoc message changes state. Bit is cleared on read. See eoc State Machine Description section for details. 0 — No change in eoc state. 1 — eoc state change.
UIR0	1	ACTSC	**Activation/Deactivation State Change on U-Interface.** Activates (set to 1) during changes in the status bits monitoring U-interface activation and deactivation (ACTR, XACT). Bit cleared on read. 0 — No activation/deactivation activity. 1 — Change in state of activation/deactivation bits.
UIR0	2	BERR	**Block Error on U-Interface.** Activates (set to 1) when received signal contains either a near-end (NEBE = 0) or a far-end (FEBE = 0) block error. Bit cleared on read. 0 — No block errors. 1 — Block error.
UIR0	3	OUSC	**Other U-Interface State Change.** Activates (set to 1) when any of the following bits change state: OOF, UOA, AIB, and Rx,y (all reserved U-interface status bits). Bit cleared on read. 0 — No state change. 1 — State change.
UIR0	4	RSFINT	**Receive Superframe Interrupt.** Activates (set to 1) when the receive superframe boundary occurs. Bit cleared on read. 0 to 1 — First 2B+D data of the receive U superframe.
UIR0	5	TSFINT	**Transmit Superframe Interrupt.** Activates (set to 1) when the transmit superframe boundary occurs. Bit cleared on read. 0 to 1 — First 2B+D data of the transmit U superframe.

Microprocessor Interface Description (continued)

Table 22. U-Interface Interrupt Mask Register (Address 10100)

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
UIR1	R/W	—	—	TSFINTM	RSFINTM	OUSCM	BERRM	ACTSCM	EOCSCM
Default State on $\overline{\text{RESET}}$		—	—	1	1	1	1	1	1

Register	Bit	Symbol	Name/Description
UIR1	0	EOCSCM	**eoc State Change on U-Interface Mask.** 0 — EOCSC interrupt enabled. 1 — EOCSC interrupt disabled (default).
UIR1	1	ACTSCM	**Activation/Deactivation State Change on U-Interface Mask.** 0 — ACTSC interrupt enabled. 1 — ATCSC interrupt disabled (default).
UIR1	2	BERRM	**Block Error on U-Interface Mask.** 0 — BERR interrupt enabled. 1 — BERR interrupt disabled (default).
UIR1	3	OUSCM	**Other U-Interface State Change Mask.** 0 — OUSC interrupt enabled. 1 — OUSC interrupt disabled (default).
UIR1	4	RSFINTM	**Receive Superframe Interrupt Mask.** 0 — RSFINT interrupt enabled. 1 — RSFINT interrupt disabled (default).
UIR1	5	TSFINTM	**Transmit Superframe Interrupt Mask.** 0 — TSFINT interrupt enabled. 1 — TSFINT interrupt disabled (default).

Microprocessor Interface Description (continued)

Table 23. S/T-Interface Interrupt Register (Address 10101)

These bits are cleared during $\overline{\text{RESET}}$.

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SIR0	R	—	—	—	—	I4C	SFECV	QSC	SOM

Register	Bit	Symbol	Name/Description
SIR0	0	SOM	**Start of Multiframe.** Activates (set to 1) upon transmission of the F bit that begins a multiframing interval toward the TE. Bit is cleared on read. 0 to 1 — Start of multiframe.
SIR0	1	QSC	**Q Bits State Change.** Activates (set to 1) when the set of four Q bits received in a multiframe differs from the set of Q bits received in the previous multiframe. Bit is cleared on read. 0 — No state change. 1 — State change.
SIR0	2	SFECV	**S Channel Far-End Code Violation.** Activates when an illegal line code violation or extra/missing bipolar violations are detected in the S/T-interface data stream. Changes on multiframe boundary. Only active if MULTIF = 0 and a transparent Loop2 is not in effect. Bit is cleared on read. 0 — No code violations. 1 — At least one code violation.
SIR0	3	I4C	**INFO 4 Change.** 0 — No INFO 4 state change. 1 — INFO 4 state change.

Microprocessor Interface Description (continued)

Table 24. S/T-Interface Interrupt Mask Register (Address 10110)

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SIR1	R/W	—	—	—	—	I4CM	SFECVM	QSCM	SOMM
Default State on $\overline{\text{RESET}}$		—	—	—	—	1	1	1	1

Register	Bit	Symbol	Name/Description
SIR1	0	SOMM	**Start of Multiframe Mask.** 0 — SOM interrupt enabled. 1 — SOM interrupt disabled (default).
SIR1	1	QSCM	**Q Bits State Change Mask.** 0 — QSC interrupt enabled. 1 — QSC interrupt disabled (default).
SIR1	2	SFECVM	**S Subchannel Far-End Code Violation Mask.** 0 — SFECVM interrupt enabled. 1 — SFECVM interrupt disabled (default).
SIR1	3	I4CM	**INFO 4 Change Mask.** 0 — I4C interrupt enabled. 1 — I4C interrupt disabled (default).

Microprocessor Interface Description (continued)

Table 25. Maintenance Interrupt Register (Address 10111)

These bits are cleared during $\overline{\text{RESET}}$.

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MIR0	R	—	—	—	—	—	EMINT	ILINT	QMINT

Register	Bit	Symbol	Name/Description
MIR0	0	QMINT	**Quiet Mode Interrupt.** Activates (set to 1) when the ANSI maintenance state machine detects a request on the OPTOIN pin for the device to enter the quiet mode. Bit is cleared on read. 0 — No quiet mode request. 1 — Quiet mode requested.
MIR0	1	ILINT	**Insertion Loss Interrupt.** Activates (set to 1) when the ANSI maintenance state machine has detected a request on the OPTOIN pin for the device to transmit the SN1 tone on the U-interface. Bit is cleared on read. 0 — No SN1 tone request. 1 — SN1 tone requested.
MIR0	2	EMINT	**Exit Maintenance Mode Interrupt.** Activates (set to 1) when the ANSI maintenance state machine detects a request on the OPTOIN pin for the device to exit the current maintenance mode. Bit is cleared on read. 0 — No exit request. 1 — Exit requested.

Microprocessor Interface Description (continued)

Table 26. Maintenance Interrupt Mask Register (Address 11000)

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MIR1	R/W	—	—	—	—	—	EMINTM	ILINTM	QMINTM
Default State on $\overline{\text{RESET}}$		—	—	—	—	—	1	1	1

Register	Bit	Symbol	Name/Description
MIR1	0	QMINTM	**Quiet Mode Interrupt Mask.** 0 — QMINT interrupt enabled. 1 — QMINT interrupt disabled (default).
MIR1	1	ILINTM	**Insertion Loss Interrupt Mask.** 0 — ILINT interrupt enabled. 1 — ILINT interrupt disabled (default).
MIR1	2	EMINTM	**Exit Maintenance Mode Interrupt Mask.** 0 — EMINT interrupt enabled. 1 — EMINT interrupt disabled (default).

Microprocessor Interface Description (continued)

Table 27. Global Interrupt Register (Address 11001)

These bits are cleared during $\overline{\text{RESET}}$.

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GIR0	R	—	—	—	—	—	MINT	SINT	UINT

Register	Bit	Symbol	Name/Description
GIR0	0	UINT	**U Transceiver Interrupt.** Activates (set to 1) when any of the unmasked U transceiver interrupt bits (register UIR0) activate. 0 — No U transceiver interrupts. 1 — U transceiver interrupt active.
GIR0	1	SINT	**S/T Transceiver Interrupt.** Activates (set to 1) when any of the unmasked S/T transceiver interrupt bits (register SIR0) activate. 0 — No S/T transceiver interrupts. 1 — S/T transceiver interrupt active.
GIR0	2	MINT	**Maintenance Interrupt.** Activates (set to 1) when any of the unmasked maintenance interrupt bits (register MIR0) activate. 0 — No maintenance interrupts. 1 — Maintenance interrupt active.

Microprocessor Interface Description (continued)

Timing

The microprocessor interface is compatible with any microprocessor that supports a synchronous serial microprocessor port such as the following:

- *NEC** 75402
- *Motorola* MC68HC05 and MC68302 SCP port
- *Intel*† 80C51

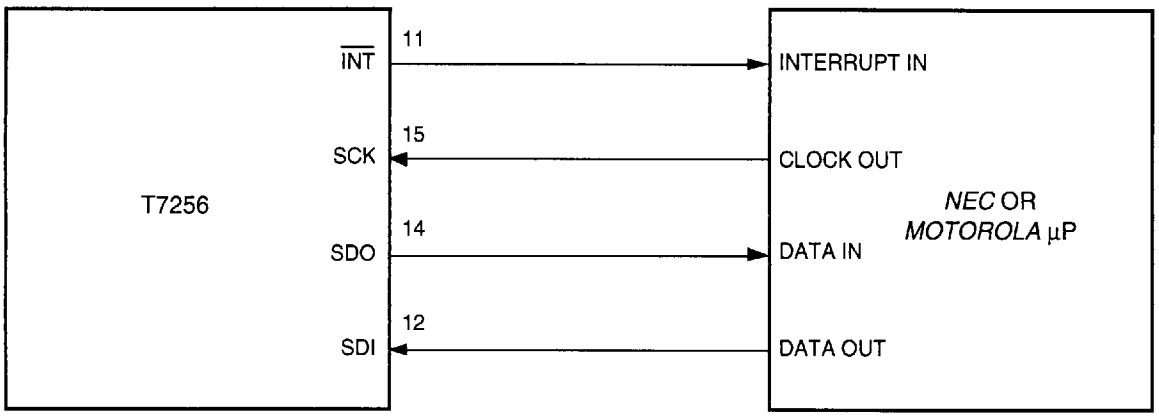


Figure 15. *NEC* and *Motorola* Microprocessor Port Connections

The synchronous interface consists of the microprocessor input clock (SCK), serial data input (SDI), and serial data output (SDO). A microprocessor interrupt lead ($\overline{\text{INT}}$) is also included. These connections are shown in Figure 15 for applications using either *NEC* or *Motorola* microprocessors. Figure 16 shows the connections for applications using the *Intel* 80C51 or equivalents.

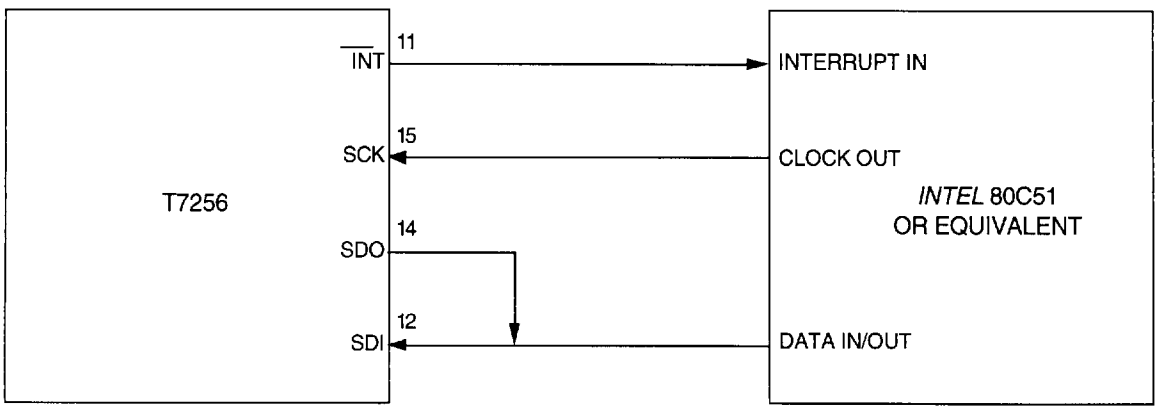


Figure 16. *Intel* Microprocessor Port Connections

* *NEC* is a registered trademark of NEC Electronics, Inc.
† *Intel* is a registered trademark of Intel Corporation.

Microprocessor Interface Description (continued)

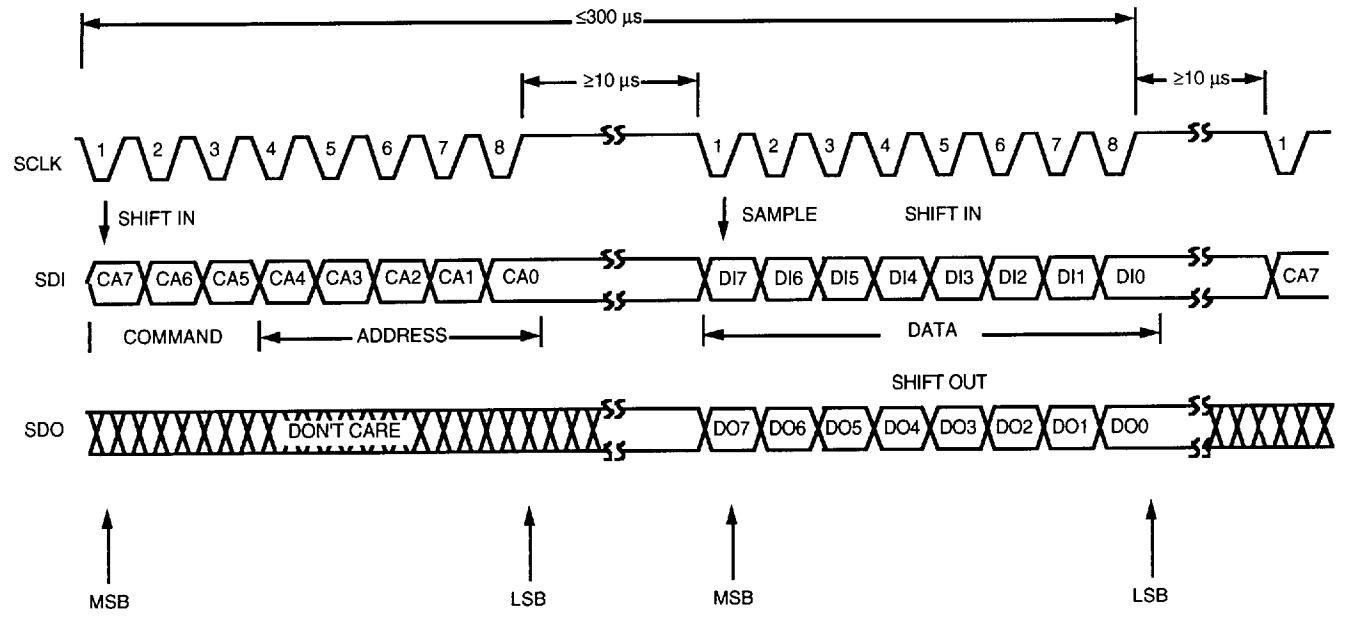


Figure 17. Synchronous Microprocessor Port Interface Format

Figure 17 shows the basic transfer format. All data transfers are initiated by the microprocessor, although the interrupt may indicate to the microprocessor that a register read or write is required. The microprocessor holds the SCK pin high during inactive periods and only makes transitions during register transfers. The maximum clock rate of SCK is 960 kHz. Data changes on the falling edge of SCK and is latched on the rising edge of SCK.

Each complete serial transfer consists of 2 bytes (8 bits/byte). The first byte of data received over the SDI pin from the microprocessor consists of command/address information that includes a 5-bit register address in the least significant bit positions (CA4—CA0) and a 3-bit command field in the most significant bit positions (CA7—CA5). The byte is defined as follows:

- Bits CA7—CA5: 001 = read, 010 = write, all other bit patterns will be ignored.
- Bits CA4—CA0: 00000 = register address 0, 00001 = register address 1, etc.

The second byte of data received over the SDI pin consists of write data for CA7—CA5 = 010 (write) or don't care information for CA7—CA5 = 001 (read).

The data transmitted over the SDO pin to the microprocessor during the first byte transfer is a don't care for both read and write operations. The second byte transmitted over the SDO pin consists of read data for CA7—CA5 = 001 (read) or don't care information for CA7—CA5 = 010 (write).

In order for the T7256 to recognize the identity (command/address or data) of the byte being received, it is required that the time allowed to transfer an entire instruction (time from the receipt of the first bit of the command/address byte to the last bit of the data byte) be limited to less than 300 µs. This limits the minimum SCK rate to 60 kHz. If the complete instruction is received in less than 300 µs, the T7256 accepts the instruction immediately and is ready to receive the next instruction after a 10 µs delay. If the complete instruction is not received within 300 µs, the bits received in the previous 300 µs are discarded and the interface is prepared to receive a new instruction after a 10 µs delay. In addition, a minimum 10 µs delay must exist between the command/address and data bytes.

Microprocessor Interface Description (continued)

For microprocessors using a multiplexed data out/in pin to drive SDI and SDO (as shown in Figure 16), a read instruction to T7256 will require that the microprocessor data in/out pin be an output during the command/address byte written to T7256, then switch to an input to read the data byte T7256 presents on the SDO pin in response to the read command. In this case, the microprocessor data in/out pin must tristate within 1.46 µs of the final SCK rising edge of the command/address byte to ensure that there is no contention between the microprocessor data out pin and the T7256 SDO pin.

Time-Division Multiplexed (TDM) Bus Description

The TDM bus facilitates B1, B2, and D channel communication between the T7256 and peripheral devices such as CODECs, HDLC processors, time-slot interchangers, synchronous data interfaces, etc. The following list is a subset of the devices that can connect directly to the T7256 TDM bus:

- AT&T T7570 Codec
- AT&T T7270 Time-Slot Interchanger
- AT&T T7121 HDLC Formatter
- *National Semiconductor** 3070 Codec

The bus can be used to extract data from S/T- or U-interface receivers, process the data externally, and source data to the appropriate transmitters with the processed data. The bus can also be used to simply monitor 2B+D channel data flow within the T7256 without modifying it. The bus also supports board-level testing procedures using in-circuit techniques (see the Board-Level Testing section for more details). Upon powerup, the TDM bus is not selected. Pins 4, 7, 8, and 9 form the TDM bus when TDMEN is set to 0.

The TDM bus consists of a 2.048 MHz output clock (TDMCLK), data in (TDMDI), data out (TDMDO), and a programmable frame strobe lead (FS). The frame strobe timing can be configured via the microprocessor register bits FSC and FSP in register TDR0. Data appearing and expected on the bus is controlled via the B1, B2, and D channel data flow register bits (registers DFR0 and DFR1). The TDMCLK and FS outputs only become active if one or more of the TDM time slots is enabled (See register DFR1,Table 10).

Clock and Data Format

The clock and data signals for the TDM bus are TDMCLK, TDMDO, and TDMDI (see Figure 18). TDMCLK is a 2.048 MHz output clock. TDMDO is the 2B+D data output for data derived from either the S/T-interface receiver, U-interface receiver, or both. The TDMDO output driver is only active during a time slot when it is driving data off-chip; otherwise, the output driver is tristated (this includes the 6-bit interval in the D channel octet). TDMDI is the 2B+D data input for data used to drive either the S/T-interface transmitter, U-interface transmitter, or both.

On both the TDMDO and TDMDI leads, six time slots are reserved for the B1, B2, and D channels associated with the S/T- and U-interfaces. The relative locations of the time slots are fixed; however, the frame strobe is programmable. The number of total time slots is 32. During unused time slots, data on TDMDI is ignored and TDMDO is tristated.

Frame Strobe

The FS frame strobe is a programmable output associated with the TDM bus. FS can be configured to serve as an envelope strobe for any of the six reserved time slots available on the bus: U-interface B1, B2, and D and S/T-interface B1, B2, and D. FS can also be programmed as a 2B+D envelope for either the U-interface or S/T-interface time slots. FS can be used to directly drive a CODEC for voice applications or can be used to control other external devices such as HDLC controllers.

Figure 18 shows the relationship between the TDMCLK, TDMDO, and TDMDI time slots, and the FS strobe for some example programmable settings. Detailed descriptions of TDM bus interface timing are given in the Timing Characteristics section of this document.

* *National Semiconductor* is a registered trademark of National Semiconductor Corporation.

Time-Division Multiplexed (TDM) Bus Description (continued)

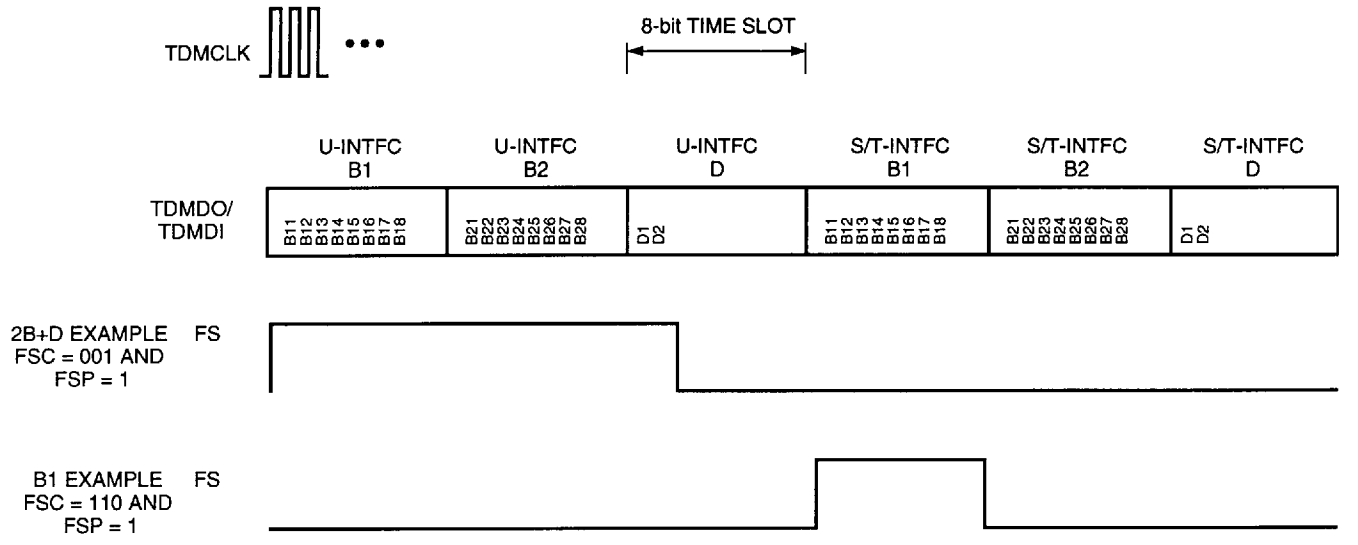


Figure 18. TDM Bus Time-Slot Format

Data Flow Matrix Description

B1, B2, D Channel Routing

The T7256 supports extremely flexible B1, B2, and D channel routing among major circuit blocks in order to accommodate multiple applications. Channel routing is controlled via the data flow control registers. Figure 19 below shows a block diagram of the device and the channel paths to and from the U transceiver, S/T transceiver, and TDM bus interface. Channel flow is determined by specifying the source of channel data at the three points shown in the figure: (1) U transceiver transmit input, (2) S/T transceiver transmit input, and (3) TDM bus transmit input. Channel flow at the TDM bus receive input is determined, by default, from the settings at the other three points. A switch matrix within the data flow matrix block routes channels to and from the specified points.

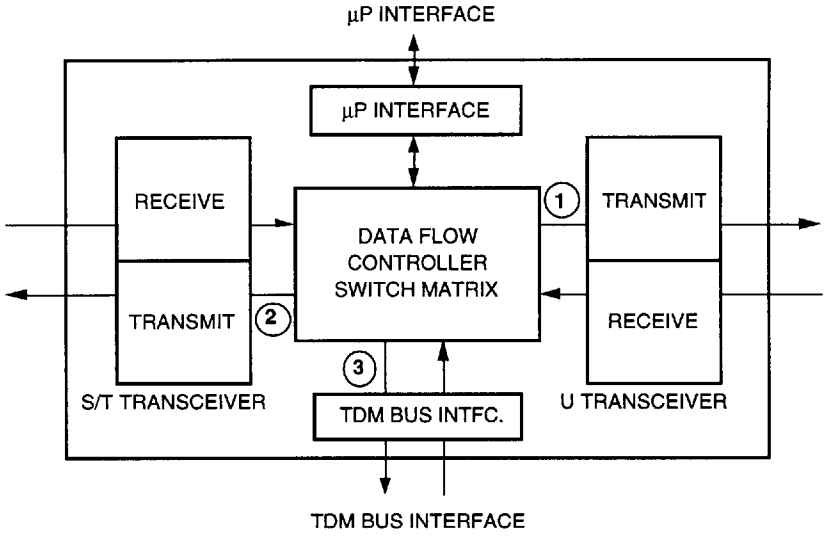


Figure 19. B1, B2, D Channel Routing

Data Flow Matrix Description (continued)

As an example, below are the register settings required to configure the device as an NT1, with the B1 and B2 channels in both the U- to S/T- and S/T- to U-interface directions made available on the TDM bus for monitoring:

- UXB1 = 11, UXB2 = 11, UXD = 1 (routes S/T-interface receive channels to U-interface transmitter).
- SXB1 = 11, SXB2 = 11, SXD = 1 (routes U-interface receive channels to S/T-interface transmitter).
- TDMB1S = TDMB2S = 0 (brings out B1 and B2 channels in S/T- to U-interface direction to TDM bus).
- TDMDS = 1 (D channel in S/T- to U-interface direction not brought out on TDM bus).
- TDMB1U = TDMB2U = 0 (brings out B1 and B2 channels in U- to S/T-interface direction to TDM bus).
- TDMDU = 1 (D channel in U- to S/T-interface direction not brought out on TDM bus).

Loopbacks

The figure below shows the Layer-1 loopbacks that are defined in ITU-T I.430, Appendix I and ANSI Specification T1.605, Appendix G. A complete discussion of these loopbacks is presented in ITU-T I.430, Appendix I.

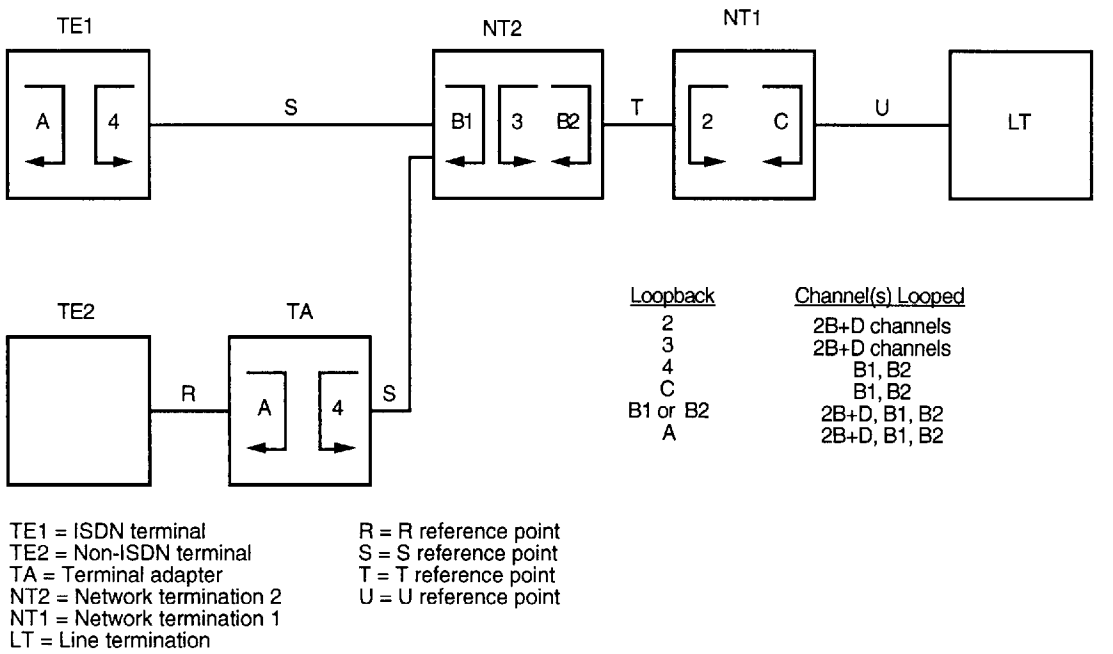


Figure 20. Location of the Loopback Configurations (Reference ITU-T I.430 Appendix I)

If a U-interface transparent B1 or B2 loopback is requested via an eoc message, the proper channel is looped upstream of the data flow matrix. All other device functions are unaffected. Nontransparent B1 or B2 loopbacks towards the S/T-interface (loop C in Figure 20) are supported via the DFR0 register, bits 4—7.

If a U-interface transparent 2B+D loopback is requested via an eoc message (loop 2 in Figure 20), the 2B+D data will be looped as close to the S/T-interface as possible. In stand-alone mode, the device overrides the SXE bit to force all 0s in the echo channel and also overrides the SXB1, SXB2, SXD, UXB10, UXB11, UXB21, UXB20, and UXD data flow matrix bits to force a U- to S/T-interface data path. In microprocessor mode, the user must clear these bits via software for proper operation of the transparent 2B+D loopback (see register ECR0, bit 6). Note that the actual register bits are unaffected.

Modes of Operation

To provide flexibility in the system architecture, the T7256 transceiver can operate in stand-alone mode (no microprocessor) to provide basic NT1 functionality or it can operate under microprocessor control through the serial interface to provide enhanced NT1 operation. In stand-alone mode, the T7256 automatically handles U- and S/T-interface activation, control, and maintenance according to the ANSI T1.601 and ITU-T I.430/ANSI T1.605 standards. The device is configured for this mode via internal pull-ups and pull-downs and microprocessor register default values during an external $\overline{\text{RESET}}$. Table 28 shows the transceiver control pins that may be relevant in stand-alone mode.

Table 28. Stand-Alone Mode

Pin	Symbol	Function
2	OPTOIN	Maintenance pulse streams are decoded and automatically implemented using the ANSI state machine requirements.
4	SYN8K/LBIND/FS	Performs the SYN8K or LBIND depending on the state of SDI (pin 12) during an external $\overline{\text{RESET}}$.
7	FTE/TDMI	Performs the FTE function. Selects the S/T-interface timing recovery mode.
8	PS2E/TDMDO	Performs the PS2E function. Controls the PS2 bit in the transmit U-interface data stream.
9	PS1E/TDMCLK	Performs the PS1E function. Controls the PS1 bit in the transmit U-interface data stream.
11	ACTMODE/ $\overline{\text{INT}}$	Performs the ACTMODE function. Controls the act bit in the transmit U-interface data stream during 2B+D loopbacks.
12	SYN8K/SDI	Held high or low on powerup or RESET to control SYN8K/LBIND/FS (pin 4).
15	AUTOACT/SCK	Held high or low on powerup or RESET to control automatic activation attempt.
43	$\overline{\text{RESET}}$	Resets the device. The states of SCK, SDI, and $\overline{\text{INT}}$ are read upon exiting reset state.

In microprocessor mode, the T7256 supports all the features of stand-alone mode, plus allows enhanced control including S/Q channel support, TDM highway access, and manual eoc and U overhead bit manipulation. The microprocessor port can be accessed at any time via the SDI, SDO, and SCK pins (see Microprocessor Interface Description and Timing Characteristics sections for details). Table 29 shows the transceiver control pins that may be relevant in microprocessor mode, or whose operation may change based on register settings.

Table 29. Microprocessor Mode

Pin	Symbol	Comment
2	OPTOIN	Controlled by microprocessor bit AUTOCTL (register GR0).
4	SYN8K/LBIND/FS	Controlled by microprocessor bit TDMEN (register GR2).
6	$\overline{\text{ILOSS}}$	Controlled by microprocessor bit AUTOCTL (register GR0).
7	FTE/TDMDI	Controlled by microprocessor bit TDMEN (register GR2).
8	PS2E/TDMDO	Controlled by microprocessor bit TDMEN (register GR2).
9	PS1E/TDMCLK	Controlled by microprocessor bit TDMEN (register GR2).
11	ACTMODE/ $\overline{\text{INT}}$	Interrupt output for the microprocessor interface.
12	SYN8K/SDI	Serial data input for the microprocessor interface.
14	SDO	Serial data output for the microprocessor interface.
15	AUTOACT/SCK	Master clock input for the microprocessor interface.

STLED Description

The STLED pin is used to drive an LED and provides a visual indication of the current state of the T7256. The STLED control is typically configured to illuminate the LED when STLED is LOW. This convention will be assumed throughout this section.

The following table describes the four states of STLED, the list of system conditions that produce the state, and the corresponding ANSI states, as defined in ANSI T1.601-1992 (Tables C1 and C4) and ETSI DTR/TM 3002-1992 (Tables A3 and I2).

Note: The ETSI state names begin with the letters NT instead of H. Also, the ETSI state tables do not include a state NT11 because it is considered identical to state NT6. Table A3 of the ETSI standard contains the additional states NT6A, NT7A, and NT8A to describe states related to the eoc loopback 2 (2B+D loopback). The most likely ANSI state for each STLED state is shown in bold typeface.

Table 30. STLED States

STLED State	List of System Conditions that Can Cause STLED State	Corresponding ANSI States
High (LED off)	RESET (pin 43) = 0 AUTOCTL = 0 (register GR0, bit 3), or AUTOEOC = 0 (register GR0, bit 4), or STOA = 0 (register GR2, bit 7)	NA
	U and S/T not active	H0, **H1**, H10, H12
8 Hz Flashing	RESET = 0 (register GR0, bit 0) Quiet mode active, or ILOSS mode active	NA
	U activation attempt in progress	H2, H3, H4
	AIB = 0 (register CFR1, bit 6)	H7, **H8**
	eoc-initiated 2B+D loopback active	NT6A*, NT7A*, **NT8A***
1 Hz Flashing	U active, S/T not fully active	H6, H6(a), **H7**, H11, H8(a)†, H8(b), H8(c)
Low (LED on)	U and S/T fully active	**H8**

* These are ETSI DTR/TM-3002 states not yet defined in ANSI T1.601, although they are defined in revised ANSI tables which are currently on the living list (i.e., not yet an official part of the standards document).
† State H8(a) is most likely when U-interface bit uoa = 0.

The flow chart in Figure 21 illustrates the priority of the logic signals which control the STLED pin. In the decision diamonds, those names in all capital letters denote T7256 register bit names. The RESET, AUTOCTL, AUTOEOC, and STOA are R/W bits controlled by the user via the microprocessor interface. The XACT, OOF, and AIB bits are read-only bits determined by the internal logic based on system events and can be monitored by the user via the microprocessor interface. Other names in the decision diamonds (quiet mode, ILOSS mode, Loop2, INFO 2, INFO 4) represent system conditions that cannot be directly monitored or controlled by the microprocessor interface.

STLED Description (continued)

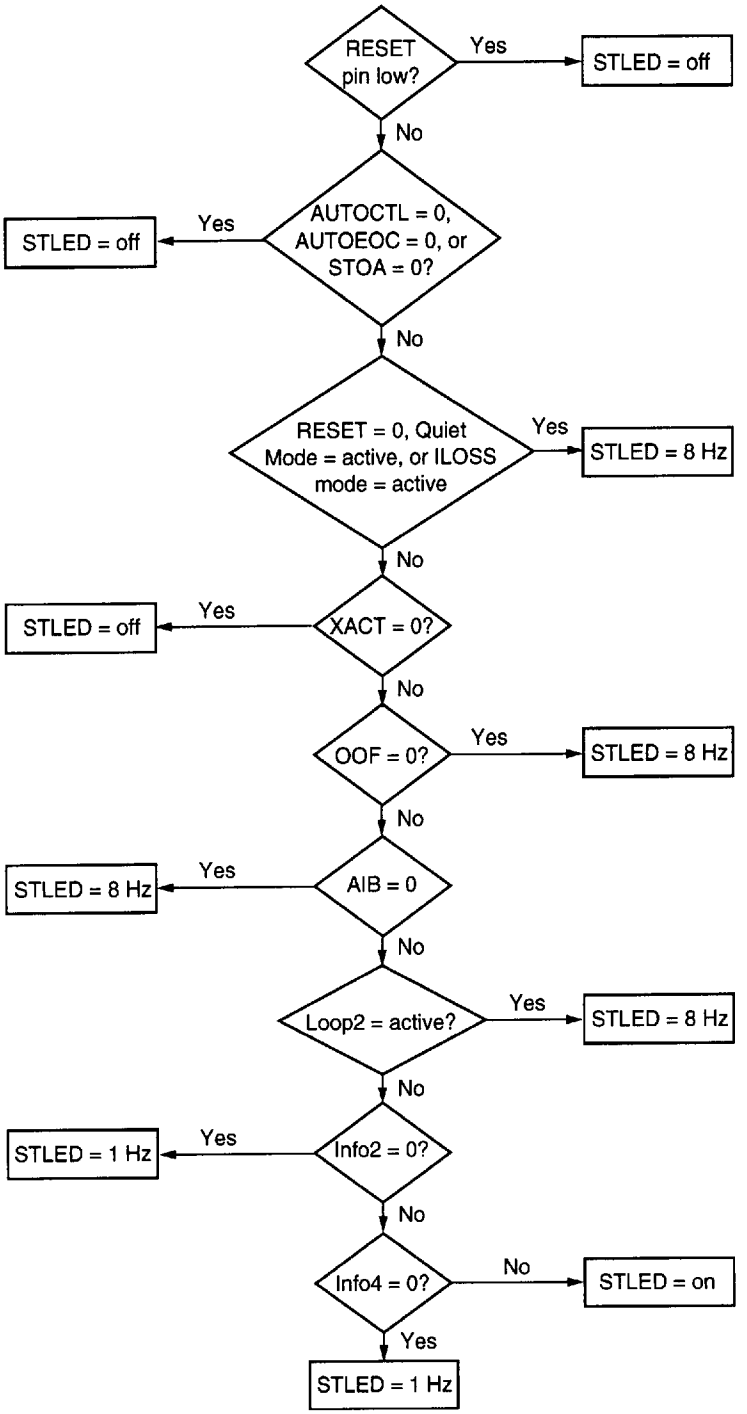


Figure 21. STLED Control Flow Diagram

eoc State Machine Description

The following list shows the eight eoc states defined in ANSI T1.601 and ETSI DTR/TM 3002.

01010000 — Operate 2B+D loopback.
01010001 — Operate B1 channel loopback.
01010010 — Operate B2 channel loopback.
01010011 — Request corrupt CRC.
01010100 — Notify of corrupted CRC.
11111111 — Return to normal (default).
00000000 — Hold state.
10101010 — Unable to comply.

Normally, the T7256 automatically handles the eoc channel processing per the ANSI and ETSI standards. There may be some applications where manual control of the eoc channel is desired (e.g., equipment that is meant to test the eoc processing of upstream elements by writing incorrect or delayed eoc data). This can be accomplished by setting AUTOEOC = 0 (register GR0, bit 4). The eoc state change interrupt is enabled by setting EOCSCM = 0 (register UIR1, bit 0). This allows state changes in the received eoc messages (registers ECR2 and ECR3) to be indicated to the microprocessor by the assertion of UINT = 1 (register GIR0, bit 0) and EOCSC = 1 (register UIR0, bit 0). The microprocessor reads registers ECR2 and ECR3 to determine which received eoc bits changed. Then, it updates the transmit eoc values by writing registers ECR0 and ECR1 and takes appropriate action (e.g., enable a requested loopback). The total manual eoc procedure consists of the following steps:

1. Microprocessor detects $\overline{\text{INT}}$ pin going low.
2. Microprocessor reads GIR0 and determines that the UINT bit is set.
3. Microprocessor reads UIR0 and determines that the EOCSC bit is set.
4. Microprocessor reads ECR2.
5. Microprocessor reads ECR3.
6. Microprocessor interrupts newly received eoc message and determines the appropriate response.
7. Microprocessor writes ECR0 based on results of step 6.
8. Microprocessor writes ECR1 based on results of step 6.

The maximum time allowed from the assertion of the $\overline{\text{INT}}$ pin (step 1) until the completion of the last write cycle to the eoc registers (step 8) is 1.5 ms.

ANSI Maintenance Control Description

The ANSI maintenance controller of the T7256 can operate in fully automatic or in fully manual mode. Automatic mode can be used in applications where autonomous control of the metallic loop termination (MLT) maintenance is desired. The MLT capability implemented with the AT&T LH1465AB and an optocoupler provides a dc signature, sealing current sink, and maintenance pulse level translation for the testing facilities. Maintenance pulses from the U-interface MLT circuit are received by the OPTOIN pin and digitally filtered for 20 ms. The device decodes these pulses according to ANSI maintenance state machine requirements and responds to each request automatically.

For example, the T7256 will place itself in the quiet mode if six pulses are received from the MLT circuitry. Microprocessor interrupts in register MIR0 are available for tracking maintenance events if desired.

Manual mode can be used in applications where an external maintenance decoder is used to drive the $\overline{\text{RESET}}$ and ILOSS pins of the T7256. In this mode, the $\overline{\text{RESET}}$ pin places the device in quiet mode and the ILOSS pin controls SN1 tone transmission. Maintenance events are not available in register MIR0 when in manual mode.

S/T-Interface Multiframing Controller Description

The T7256 provides the capability of supporting multiframing as defined in ITU-T I.430 section 6.3.3 and ANSI T1.605 Section 7.3.3. Multiframing provides layer-1 signaling capability between the TEs and the NT in both directions through the use of extra channels referred to as the S channel for the NT-to-TE direction and the Q channel for the TE-to-NT direction (see Figure 12 in this data sheet for the location of the S and Q bits in the NT and TE frames). This signaling capability is similar to the eoc channel between the LT and NT on the U-interface. The S and Q channels exist only between the TE and NT, and there is no requirement that the NT transfer this information to the U-interface.

The requirement for multiframing capability is treated somewhat different in ANSI T1.605, ITU-T I.430 and ETSI ETS 300 012. The ANSI standard states that the use of the S and Q channels is optional. NTs that do not support these channels are not required to encode the FA and M bits as required for multiframing. TEs that do not support these channels still must provide for identification of the Q bit positions and, if identified, must set each Q bit to a binary one. ANSI defines a set of Q channel messages, and divides the S channel into five subchannels, defining messages for S subchannels 1 and 2 (see T1.605 Tables 8 and 9).

ITU-T I.430 contains essentially the same requirements for the S and Q channels with the following exceptions:

1. There is no "far-end code violation" message for S subchannel 1 (see ITU-T I.430, Table 9).
2. S subchannel 2 is not defined.

ETSI ETS 300 012 deviates slightly from ITU-T I.430. It states that the NT1 shall not provide multiframing, and therefore the FA bit from NT-to-TE must be set to zero. An NT2, however, may optionally provide multiframing in accordance with ITU-T I.430. In either case, the TEs must provide for identification of the Q bit positions.

The multiframing mechanism in the T7256 is controlled by the microprocessor. Normally, multiframing is disabled (the NT transmits all zeros in the F_A and M bit positions and all ones in the S bit positions). To enable multiframing, set the MULTIF = 0 in bit 5 of register GR0. This allows the microprocessor to read the Q channel data that is received and control the S subchannel data that is transmitted via registers MCR0-MCR5. The reception of a new Q channel message is indicated to the microprocessor when interrupt bit QBSC = 1 (Q Bits State Change bit, register SIR0 bit 1). The microprocessor is informed that a new S subchannel message may be transmitted when interrupt bit SOM = 1 (Start of Multiframe bit, register SIR0 bit 0). To enable the SOM and QBSC interrupts, set SOMM = 0 and QSCM = 0 (register SIR1 bits 0 and 1). When an interrupt occurs, the global interrupt bits (register GR0) can be read by the microprocessor to determine the source of the interrupt (register UINT, SINT, or MINT). An interrupt asserted in the SIR0 register is indicated by SINT = 1. Reading the SIR0 interrupt register clears the SOM and QSC interrupt bits in preparation for the next occurrence. It should be noted that the SOM interrupt is asserted 27 µs after the start of a multiframe and the S subchannel bits are latched in the MCR1—MCR5 registers 3 µs prior to the start of the next multiframe. Since 30 µs (27 µs + 3 µs) of time is used by the device, the microprocessor has 4.97 ms of a total 5 ms multiframe to load the next value of S subchannel bits. The Q channel bits in the MCR0 register are updated every multiframe at the same time that SOM is asserted. Changes in any of the Q bits are indicated to the microprocessor by QSC = 1.

Board-Level Testing

In order to reduce board-level test cost and development time, and to simplify field diagnostic procedures, the T7256 supports board-level testability. The configuration is described below. For board-level testing during manufacturing, the $\overline{\text{HIGHZ}}$ pin tristates all digital outputs.

External Stimulus/Response Testing

External data transparency of the B1, B2, and D channels can be verified by the combined use of the TDM bus and microprocessor port. Data flow within the device can be configured by the external test machine through the microprocessor port, and B1, B2, and D channel data can be entered into and extracted from the device via the TDM bus. Using this method, arbitrary data patterns can be used to stimulate the device and all possible combinations of loopbacks can be exercised to help detect and isolate faults. Figure 22 illustrates this general-purpose testing configuration.

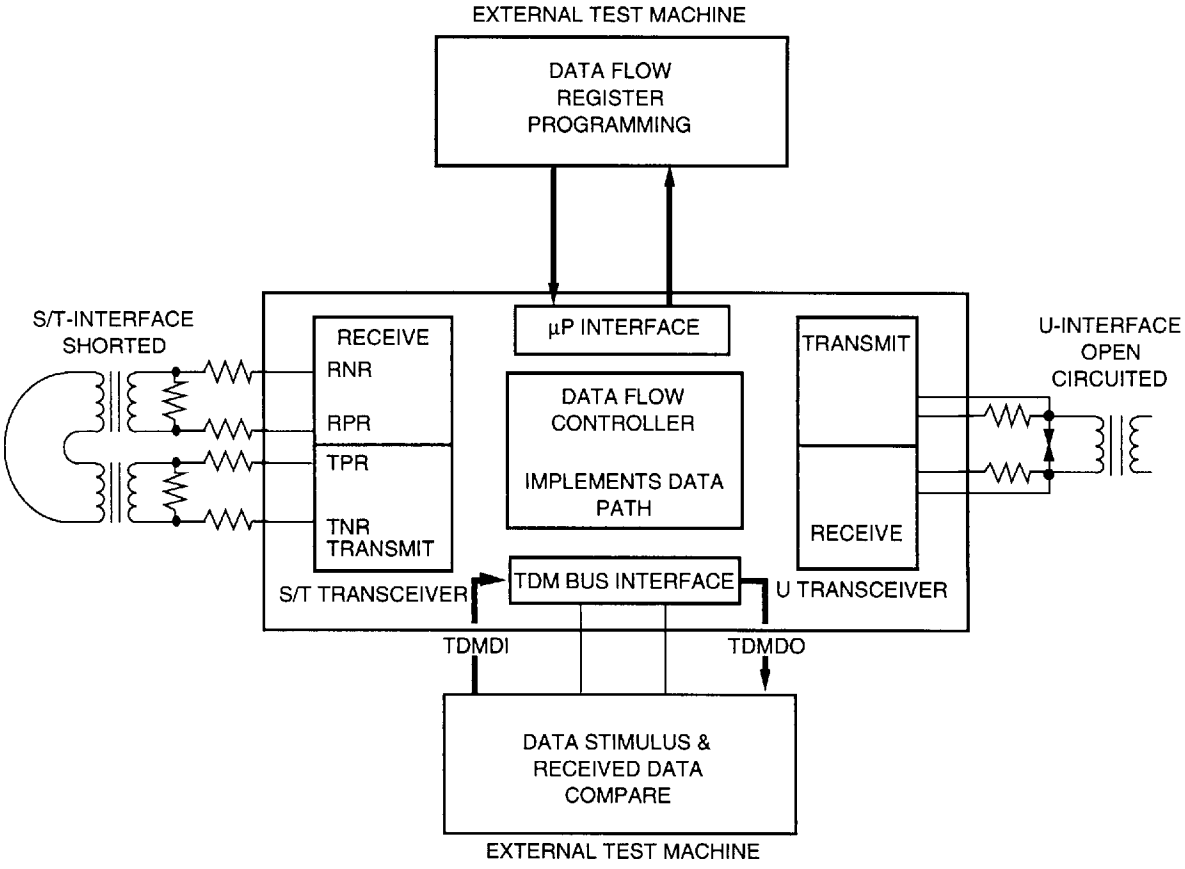


Figure 22. External Stimulus/Response Configuration

Application Briefs

Using the T7256 in a Combination TE/TA Environment (NT1/TA)

The T7256 can be used in applications requiring NT1 and terminal adapter (TA) functionality (NT1/TA). This application brief describes an NT1/TA that supports conventional POTS (plain old telephone service) in addition to ISDN service. A block diagram of this application is shown in Figure 23.

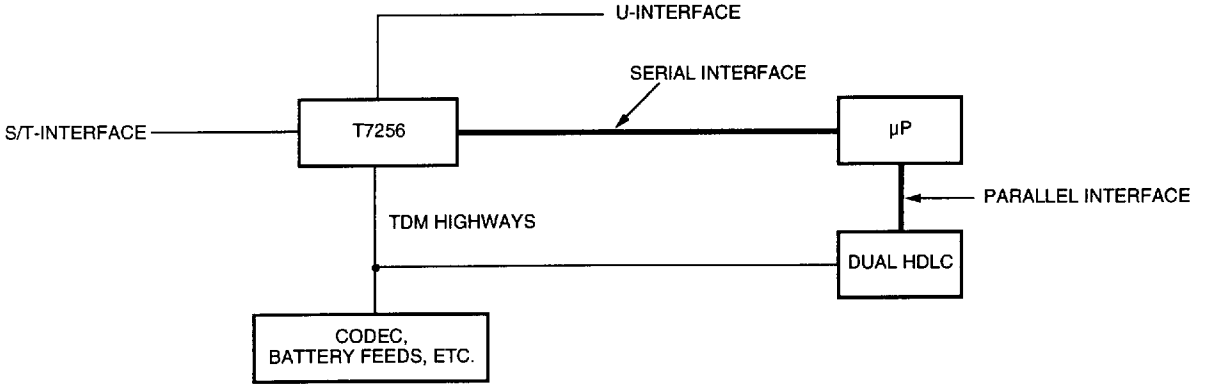


Figure 23. T7256 NT1/TA Application Block Diagram

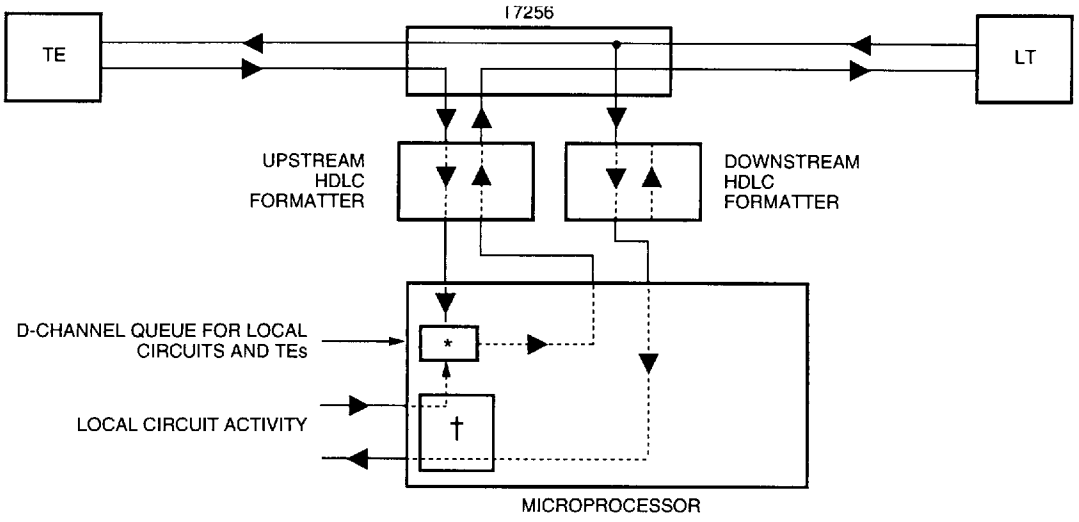
One issue in this application concerns the D channel priority mechanism because the D channel must not only be shared among any TEs, but must also be shared with the TA circuitry. Below are two approaches to implementing the D channel priority mechanism:

1. As illustrated in Figure 24, the microprocessor can queue all upstream D channel messages. This includes those messages received from the TEs via the upstream HDLC formatter and those generated locally by the D message generator software in the microprocessor. The D messages are transmitted to the switch in the order they are queued. This implements the D channel priority control in software.

   In the downstream direction (LT to TE), the D channel messages from the LT are passed directly to the TE and monitored locally via the downstream HDLC formatter. The microprocessor's D message decoder determines if the D message is for the local circuits and if so, exercises the appropriate local signals (for example, it may enable a CODEC frame strobe signal to establish a POTS voice call). Any required D channel response from the local circuits is generated by the D message generator and queued in the upstream HDLC formatter.

   If the D channel message is for the TE, the TE will respond and any D channel response from the TE will be received locally via the upstream HDLC formatter where it will be queued for transmission. The D channel message flow is illustrated in Figure 24.

Application Briefs (continued)

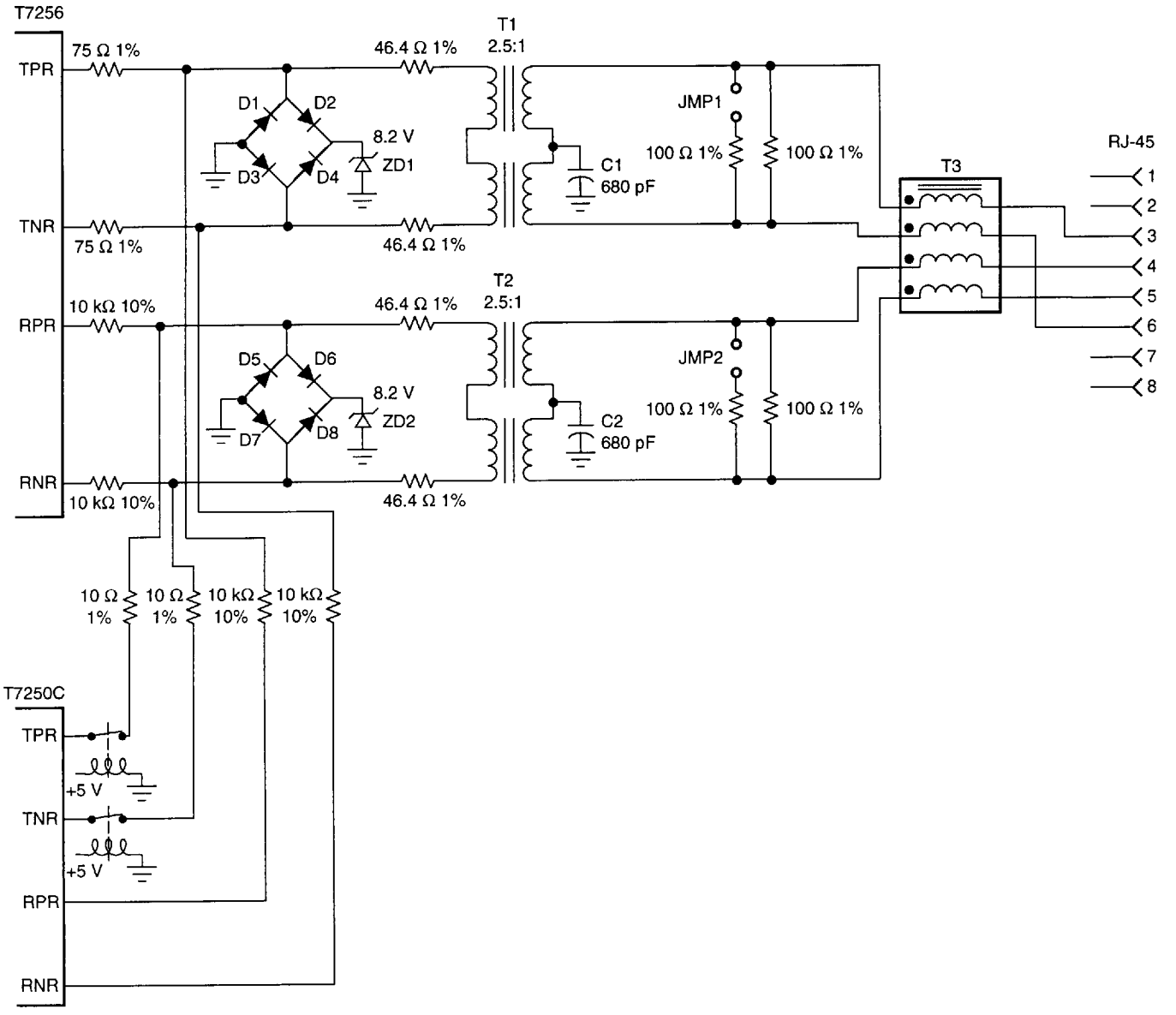


* D message queue.
† D message generator/decoder for local analog phones.

Figure 24. D Channel Message Flow, Option #1

2. The second approach is to use the AT&T T7250C TE chip as a local TE on the NT1/TA and connect it to the T7256 S/T-interface as shown in Figure 25. A standard short passive bus connection can be used for external TEs (the bus configuration is by definition a short passive bus, since there is a TE connected locally). The analog phone circuitry (CODECs, battery feeds, etc.) connects to the system side of the T7250C using the TDM interface to transfer 2B+D data. A microprocessor interface on the T7250C provides access to the internal HDLC formatter (see the T7250C data sheet, DS93-022TCOM). This solution is ideal if a terminal adapter based on the T7250C already exists because the hardware and software are identical. The external HDLC formatters are eliminated in this solution because the T7250C internal HDLC formatter provides this function.

Application Briefs (continued)



Notes:
Install JMP1 and JMP2 if no external TE is a attached.
Remove JMP1 and JMP2 if external TE with 100 Ω termination is attached.

Figure 25. Local TE Connection, Option #2

Application Briefs (continued)

T7256 Configuration

When option #1 is used in the NT1/TA application, the T7256 TDM highway must be used in conjunction with the data flow control registers (DFR0 and DFR1) to control the B and D channel data flow.

1. The TDM highway should be enabled immediately on powerup by setting TDMEN = 0 (register GR2, bit 5). In this case, the PS1/PS2 functions must be controlled via the microprocessor (register GR1, bits 1 and 2) because pins 8 and 9 are used for TDMDO and TDMCLK.
2. The D channels need to be monitored via the TDM bus in both the upstream (TE to LT) and downstream (LT to TE) directions. This is accomplished by setting TDMDS = 0 for the upstream direction and TDMDU = 0 for the downstream direction (register DFR1, bits 4 and 7, respectively). To queue the D channel messages from the TE before sending them to the LT, the upstream D channel data path needs to be sourced from the TDM highway by setting UXD = 0 (register DFR1, bit 0). This has the effect of a drop/insert function on the upstream D channel.
3. The frame strobe pulse envelope and polarity must be configured for correct operation with the HDLC controllers and CODECs using register TDR0. For example, to set an active-high FS pulse that envelopes the U-interface B1 channel data (see Figure 18), register TDR0 bits 0—3 should be set to all 1s (default on powerup). This setting can be used with the AT&T T7121 HDLC controller because the T7121 can be programmed for any time-slot and bit offset from the rising or falling edge of FS.

   The CODECs may require the FS pulse be in a particular position relative to the B channel data. For example, the AT&T T7570 CODEC is typically used in variable timing mode and require an FS pulse that envelopes the appropriate B channel data. The configuration described here is adequate for sourcing or sinking B1 channel data to the U-interface, but there is no separate FS pulse available for the B2 channel data. Therefore, external glue logic is necessary to generate an FS pulse for the B2 channel data that is similar to the FS pulse for the B1 channel data.
4. The upstream B channel source will be either the S/T-interface (if a TE has a call active) or the TDM highway TDMDI pin (if an analog phone has a call active). The source of the upstream B channels is controlled by register DFR0, bits 1 and 0 (for B1) and bits 3 and 2 (for B2). These bits must be controlled dynamically depending if an analog phone or a TE is requesting the B channel. One approach to B channel control is to default to the S/T-interface (i.e., the TEs) and switch to the TDM highway after it is determined a call is being placed/received on the analog phone. For example, if a B1 call is placed on an analog phone, DFR0, bit 1 would be changed from a 1 to a 0. All the remaining bits in DFR0 would remain set to 1.

   Register DFR1, bits 5 and 6 control B1 and B2 channel data (respectively) from the U-interface to the TDM highway TDMDO pin. It may be necessary to keep the B1 and B2 time slots disabled (tristated) when the analog phones are not in use to keep the CODECs quiet. A 5.1 kΩ pull-up resistor on the TDMDO pin should be used to ensure that the TDM data is all 1s or the CODEC frame strobe signals should be disabled when the CODECs are not in use.
5. When the TDM highway is enabled by setting TDMEN = 0, TDMCLK and FS will not active until at least one of the bits 2—7 in register DFR1 are enabled (set to 0).

Application Briefs (continued)

Activation Control

Because there is no guarantee that a TE will be connected in this application, the local microprocessor must perform a layer 1 activation request as follows:

1. Write AUTOACT = 0 (register GR0, bit 6) if the local analog phone initiates a call. This will initiate start-up on the U-interface, causing XACT = 1 (register CFR1, bit 1). The AUTOACT bit will be set to a 1 automatically after the start-up request is made. This permits another activation attempt by writing AUTOACT = 0 again (without first writing it back to 1) if the start-up attempt fails.

   A switch-initiated start-up is detected by the local microprocessor when XACT = 1 (register CFR1, bit 1). This event can be indicated by an interrupt ($\overline{\text{INT}}$, pin 11) by writing the interrupt mask bit OUSCM = 0 (register UIR1, bit 3) and writing UINT = 1 (register GR0, bit 0, default). The OUSC interrupt (register UIR0, bit 3) will then indicate a bit change in either CFR1 or CFR2. Read these registers to determine the current state of these bits.

2. Look for XACT = 0 or OOF = 1 (register CFR1 bits 1 and 2). These events can be indicated by an interrupt ($\overline{\text{INT}}$, pin 11) in a similar manner as described in (1) above.

3. If XACT = 0, the start-up attempt has failed and appropriate action should be taken depending on the system requirements (it may be desirable to attempt another start-up).

4. If OOF = 1, U-interface synchronization is complete and set ACTT = 1 (register GR1, bit 4). This will set the upstream ACT = 1 on the U-interface independently of actions on the S/T-interface. It may be required to delay several tens of milliseconds between detecting OOF and setting ACTT = 1 to allow the S/T-interface time to activate if there is a TE present. If this is the case, the upstream act bit will automatically be set, but manually setting ACTT = 1 is permissible.

5. After setting ACTT = 1, wait for ACTR = 1 (register CFR1, bit 0). This event can be indicated by an interrupt ($\overline{\text{INT}}$, pin 11) in a similar manner as described in (1) above. After ACTR = 1 is detected, enable U-interface transparency by setting XPCY = 0 (register GR1, bit 5).

   At this point, layer 1 activation is complete. Note that the above steps 1—5 occur automatically if there is a TE connected or if the LT starts up and sends an eoc loopback-2 request (2B+D loopback). However, having the microprocessor perform these steps ensures layer 1 activation independently of the presence of a TE. After layer 1 activation is complete, the XACT bit (register CFR1, bit 1) can be monitored for a state change to 0. This provides an indication to the local microprocessor that layer 1 has deactivated. When this occurs, set XPCY = 1 (register GR1, bit 5) and ACTT = 0 (register GR1, bit 4) to prepare for the next start-up attempt.

Application Briefs (continued)

Information on Interfacing the T7256 to the *Motorola* 68302

Introduction

The *Motorola* MC68302 integrated multiprotocol processor (IMP) contains a 68000 core integrated with a flexible communications architecture. It has three serial communications controllers (SCCs) that can be independently programmed to support the following protocols and physical interfaces.

Table 31. *Motorola* MC68302 SCC Options

Protocols	Physical Interfaces
HDLC/SDLC	*Motorola* IDL
UART	GCI
BISYNC	PCM highway
DDCMP	NMSI (nonmultiplexed serial interface)
V.110 rate adaption	
Transparent	

The PCM interface option of the SCCs is appropriate for interfacing to the T7256 TDM highway to provide access to B and D channel data. The SCCs allow ISDN B channel transfers that support applications such as V.120 rate adaption (synchronous HDLC mode) and voice storage (transparent mode). However, the T7256 does not output all signals that are required to connect directly to the SCC and some external circuitry (e.g., a PAL) is required in order to interface the T7256 TDM highway to the MC68302 SCC PCM highway.

The MC68302 contains a three-wire serial interface called an SCP (serial communications port). The SCP may be directly connected to the T7256 serial microprocessor interface to control the T7256 register configuration. The MC68302 also has programmable ports A (16 bits) and B (12 bits) that are bitwise programmable and can be used as an alternative to the SCP to drive the T7256 serial microprocessor interface.

Figure 26 illustrates the interface connections between the MC68302 and the T7256. A discussion of the TDM and microprocessor interfaces follows.

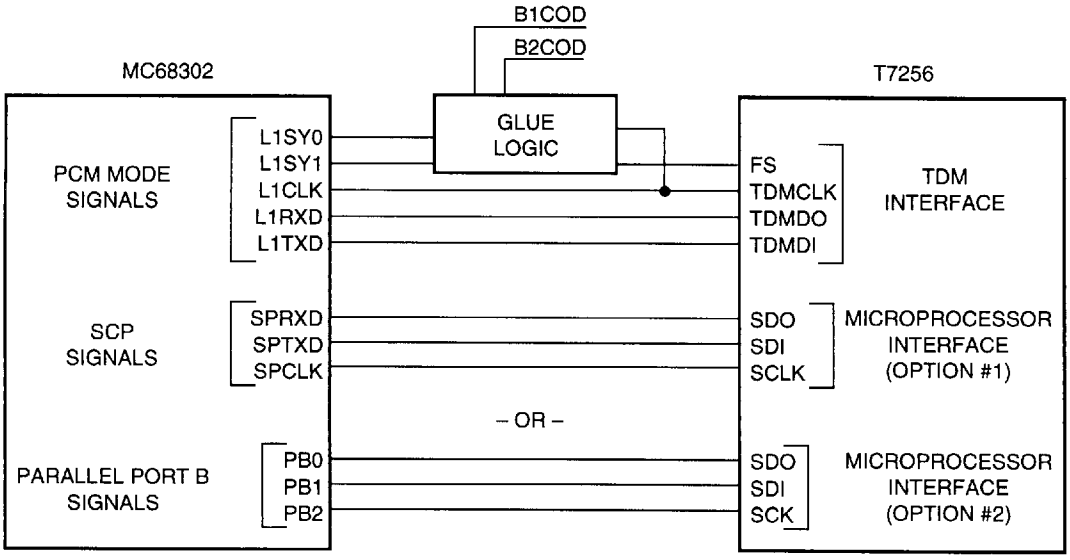


Figure 26. M68302 to T7256 Interface Diagram

Application Briefs (continued)

Using the *Motorola* MC68302 PCM Mode to Interface to the T7256 TDM Highway

In PCM mode, any number of the MC68302 internal SCCs can be multiplexed to support a TDM type of interface (see Section 4.4.3, PCM Highway Mode in the MC68302 data book). The SCCs in PCM mode require a data-in lead (L1RXD) for receive data, a data-out lead (L1TXD) for transmit data, a common receive and transmit data clock to clock data into and out of the SCCs (L1CLK). These signals are directly compatible with the T7256 TDM highway. In addition, the PCM-mode SCCs require two data synchronization signals, L1SY1 and L1SY0, which route specific TDM time slots to the SCCs. These signals are not directly supported by T7256 and some glue logic is required to generate them.

To interface to the T7256 TDM highway B and D channel time slots, the L1SY1 and L1SY0 signals must be 8 bits in length for the B1 and B2 channels, and 2 bits in length for the D channel. The MC68302 PCM channel selection criteria for the L1SY0 and L1SY1 signals are presented in the following table.

Table 32. Channel Selection Criteria

L1SY0	L1SY1	Channel Accessed
0	0	None
1	0	U-interface B1 Channel — active for 8 bits
0	1	U-interface B2 Channel — active for 8 bits
1	1	U-interface D Channel — active for 2 bits

Figures 27 and 28 illustrate a circuit and the corresponding timing diagram for generating the L1SY0 and L1SY1 signals. This circuit can be implemented on an EPLD such as an Altera EP610 or an ICTPA7024. The T7256 TDM signals FS and TDMCLK are used as inputs to the circuit, and the outputs are L1SY0 and L1SY1. In addition, two optional CODEC frame strobe outputs for B1 and B2 channel data are shown that allows one or two CODECs to share the TDM highway with the MC68302 PCM interface. The CODEC frame strobes are enabled only when the CODECs are in use to prevent them from interfering with data transmission on the TDM highway when the CODECs are not in use.

To enable the TDMCLK and FS signals and generate the FS signal in the proper time slot, the following T7256 register bits must be programmed:

Register GR2 bit 2 (TDMEN) = 0

Register DFR0 bits 3:0 (UXB2[1:0] and UXB1[1:0]) = 0101

Register DFR1 bit 0 (UXD) = 0

Register DFR1 bits 7:5 (TDMDU, TDMB2U, TDMB1U) = 000

Register TDR0 bit 3:0 (FSP, FSC[2:0]) = 1111 (default)

Detailed information on T7256 activation control and configuration of the microprocessor registers can be found in the Application Brief, Using the T7256 in a Combination NT1/TA Environment section in this document.

As an example of programming the MC68302 SIMODE register bits for PCM mode, the following settings will enable PCM mode and route the B2 channel to SCC1, the B1 channel to SCC2, and the D channel to SCC3. The ISDN signaling protocol stack (Q.931 and LAPD) would communicate via SCC3, and any higher-layer data protocol such as V.120 or V.110 would communicate via SCC1 and SCC2 as required.

SETZ = 0, SYNC = 1, SDIAG1:SDIAG0 = 00, SDC2 = 0, SDC1 = 0, B2RB:B2RA = 01, B1RB:B1RA = 10, DRB:DRA = 11, MSC3 = 0, MSC2 = 0, and MS1:MS0 = 01.

Application Briefs (continued)

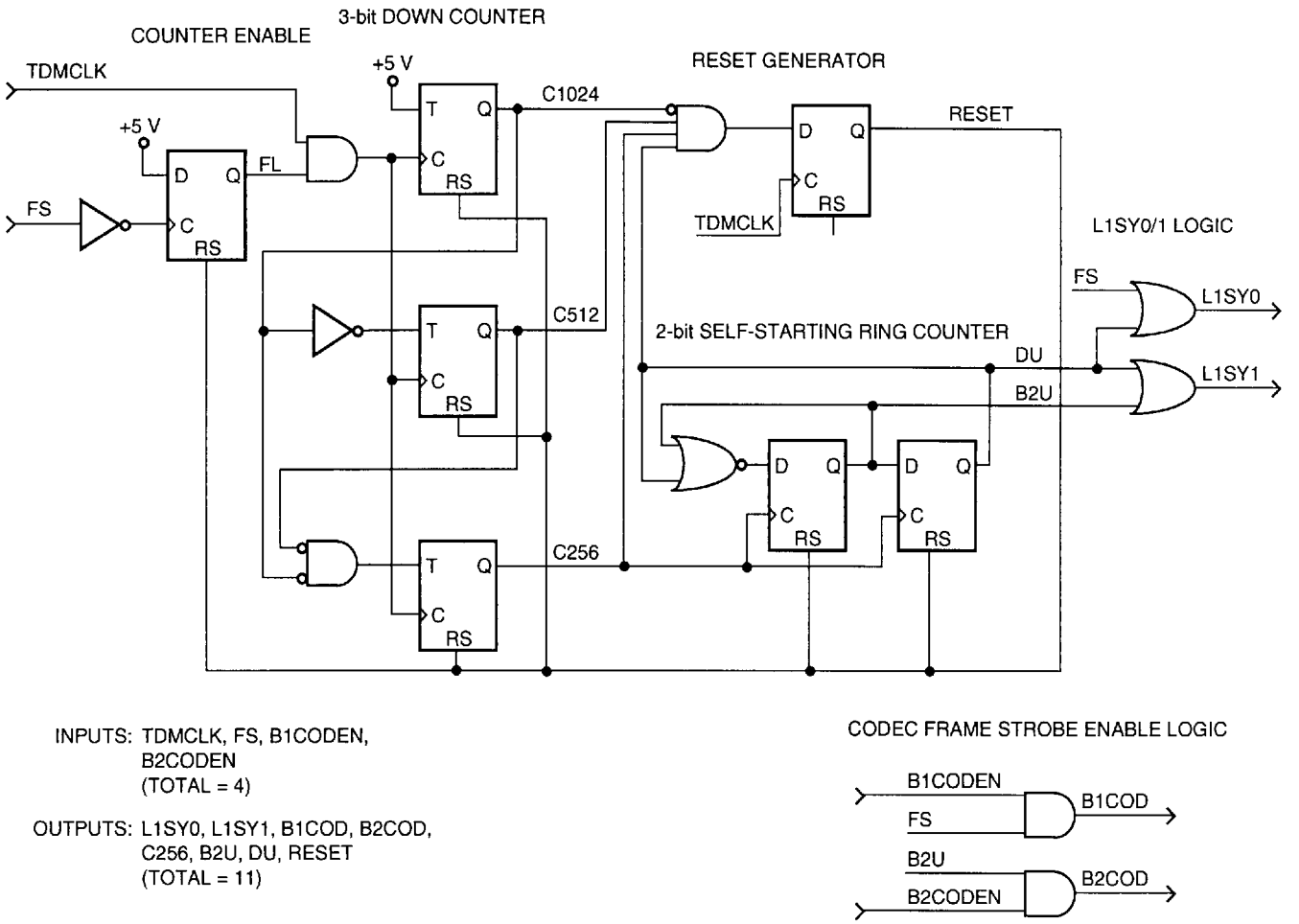


Figure 27. T7256/MC68302 Interface Circuit

Application Briefs (continued)

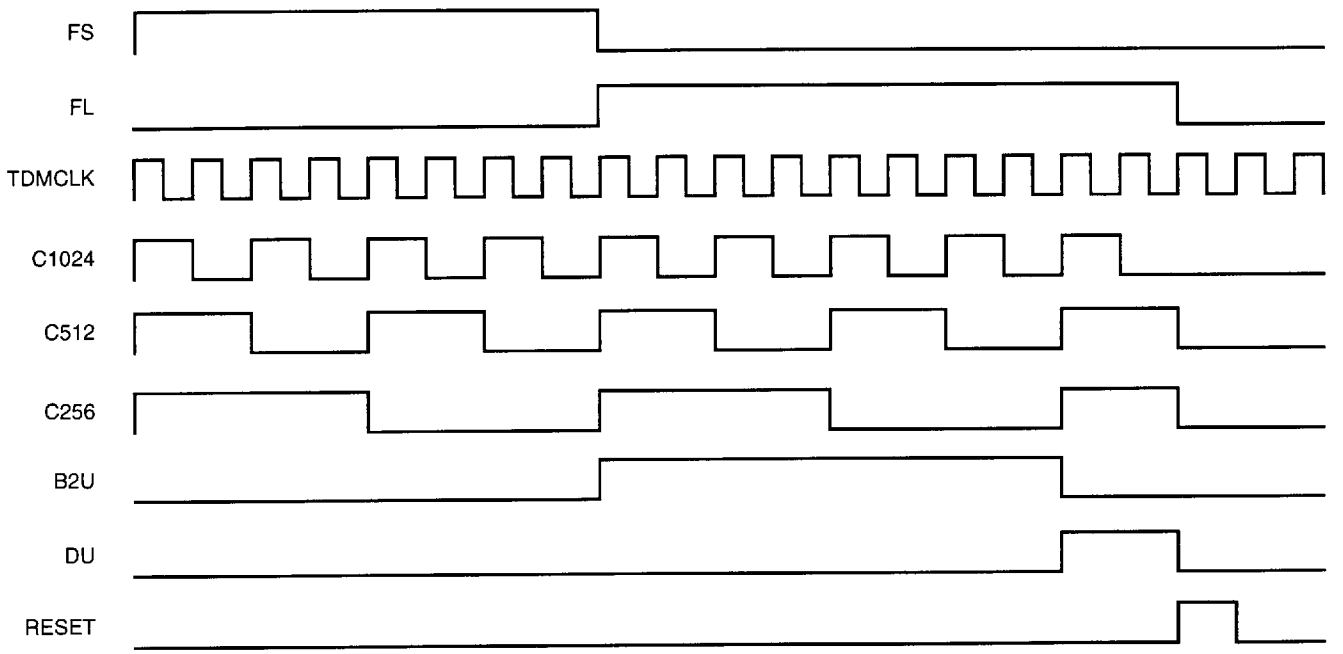


Figure 28. T7256/MC68302 Interface Timing

Application Briefs (continued)

T7256 Serial Microprocessor Interface Support

The MC68302 SCP interface is a three-wire serial interface that may be directly connected to the T7256 microprocessor interface. The SCP interface is implemented in the MC68302 hardware, and the only software interaction required is to set up the SCP interface, to transmit/receive SCP bytes, and to respond to SCP events (the SCP interrupt).

There are several points to note when interfacing the T7256 to the MC68302 microprocessor interface.

1. Register bit CI (Clock Invert) in the MC68302 should be set to 1 to invert the MC68302 SCP clock in order to meet the T7256 microprocessor timing specifications.
2. The MC68302 SCP clock, SPCLK, may be programmed to run as high as 4.096 MHz. The minimum rate of the SCP SPCLK, assuming the slower 16.384 MHz version of the MC68302 with a maximum divide-down pre-scale of 64, is 256 kHz. The minimum and maximum rates of the T7256 SCK are 60 kHz and 960 kHz, respectively and care should be taken to ensure that the MC68302 is programmed to a clock rate that is compatible with T7256.
3. Every T7256 access consists of two 8-bit transfers, where the first is the command/address byte and the second is the data byte. There must be a delay of 10 µs between every 8-bit register access to meet the T7256 microprocessor timing specifications. The back-to-back byte transmit delay of the MC68302 SCP at the slowest SPCLK rate of 256 kHz can be anywhere from 2 to 8 clocks, or 7.8 µs to 31.25 µs. To ensure that the 10 µs delay requirement is met, the MC68302 software must not send the second byte of the two-byte sequence for at least 10 µs after the SCP processor clears the DONE bit in the SCP transmit/receive buffer descriptor (refer to Section 4.6.2 of the *Motorola MC68302 User's Manual* for further information).
4. During 2-byte data transfer over the MC68302 SCP, 8 bits will be shifted into the SCP receive buffer for every 8 bits shifted out. For a T7256 read, the first byte in the receive buffer should be discarded and the second byte will contain the read data from the T7256. For a write, both bytes should be discarded from the SCP receive buffer.
5. The T7256 microprocessor interface lacks an enable pin to permit multiple device communication on a single MC68302 SCP. In these applications, the T7256 microprocessor interface can be enabled/disabled using a microprocessor parallel port pin to control a tristate buffer at SCK (pin 15).

An alternative method of interfacing the MC68302 to the T7256 microprocessor interface is to use three MC68302 parallel port pins (e.g., PB0, PB1, and PB2 in Figure 26) programmed as outputs and supporting the T7256 microprocessor interface in software. The timing of the SCK, SDI, and SDO signals can be implemented in software with a minimum amount of code instructions.

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent or latent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

External leads can be soldered safely at temperatures up to 300 °C

Parameter	Symbol	Min	Max	Unit
dc Supply Voltage Range	V_{DD}	–0.5	6.5	V
Power Dissipation (package limit)	P_D	—	800	mW
Storage Temperature	T_{stg}	–55	150	°C
Voltage (any pin) with Respect to GND	—	–0.5	6.5	V

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. AT&T employs a human-body model (HBM) and charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to defined the model. No industry-wide standard has been adopted for the CDM. However, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and, therefore, can be used for comparison. The HBM ESD threshold presented here was obtained by using these circuit parameters:

ESD Threshold Voltage

Device	Voltage
T7256-ML2	>1000

Recommended Operating Conditions

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Ambient Temperature	T_A	V_{DD} = 5 V ± 5%	–40	—	85	°C
Any V_{DD}	V_{DD}	—	4.75	5.0	5.25	V
GND to GND	V_{GG}	—	–10	—	10	mV

Electrical Characteristics

All characteristics are for a 15.36011 MHz crystal, 135 Ω line load, random 2B+D data, T_A = –40 °C to +85 °C, V_{DD} = 5 V ± 5%, GND = 0 V, and output capacitance = 50 pF.

Power Consumption

Table 33. Power Consumption

Parameter	Test Conditions	Min	Typ	Max	Unit
Power Consumption	Operating, Random Data	—	270	350	mW
Power Consumption	Powerdown Mode	—	35	50	mW

Pin Electrical Characteristics

Table 34. Digital dc Characteristics (over operating ranges)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Input Leakage Current					
Low	I_{ILPU}	V_{IL} = 0 (Pins 2, 6, 7, 11, 44)	–52	–10	µA
High	I_{IHPU}	V_{IH} = V_{DD} (Pins 2, 6, 7, 11, 44)	—	–10	µA
Low	I_{ILPD}	V_{IL} = 0 (Pins 8, 9, 12, 15, 43)	–10	—	µA
High	I_{IHPD}	V_{IH} = V_{DD} (Pins 8, 9, 12, 15, 43)	–10	–52	µA
Input Voltage					
Low	V_{IL}	All pins except 2, 6, 43	—	0.8	V
High	V_{IH}	All pins except 2, 6, 43	2.0	—	V
Low-to-High Threshold	V_{ILS}	Pin 43	V_{DD} – 0.5	—	V
High-to-Low Threshold	V_{IHS}	Pin 43	—	0.5	V
Low	V_{ILC}	Pins 2, 6	—	0.2 V_{DD}	V
High	V_{IHC}	Pins 2, 6	0.7 V_{DD}	—	V
Output Leakage					
Low	I_{OZL}	V_{OL} = 0, Pin 44 = 0 (Pins 3, 14)	—	10	µA
High	I_{OZH}	V_{OH} = V_{DD}, Pin 44 = 0 (Pins 3, 14)	–10	—	µA
Low	I_{OZLPU}	V_{OL} = 0, Pin 44 = 0 (Pins 11)	–52	–10	µA
High	I_{OZHPU}	V_{OH} = V_{DD}, Pin 44 = 0 (Pins 11)	—	10	µA
Low	I_{OZLPD}	V_{OL} = 0, Pin 44 = 0 (Pins 4, 8, 9, 17)	–10	—	µA
High	I_{OZHPD}	V_{OH} = V_{DD}, Pin 44 = 0 (Pins 4, 8, 9, 17)	10	52	µA
Output Voltage					
Low, TTL	V_{OL}	I_{OL} = 4.5 mA (Pin 3)	—	0.4	V
		I_{OL} = 19.5 mA (Pins 4, 9)	—	0.4	V
		I_{OL} = 8.2 mA (Pins 8, 17)	—	0.4	V
		I_{OL} = 6.5 mA (Pin 14)	—	0.4	V
		I_{OL} = 3.3 mA (Pin 11)	—	0.4	V
High, TTL	V_{OH}	I_{OH} = 32.2 mA (Pins 4, 9)	2.4	—	V
		I_{OH} = 13.5 mA (Pins 8, 17)	2.4	—	V
		I_{OH} = 10.4 mA (Pins 3, 14)	2.4	—	V
		I_{OH} = 5.1 mA (Pin 11)	2.4	—	V

Electrical Characteristics (continued)

S/T-Interface Receiver Common-Mode Rejection

Table 35. S/T-Interface Receiver Common-Mode Rejection

Parameter	Symbol	Specifications	Unit
Common-Mode Rejection (at device pins)	CMR	400	mV

Crystal Characteristics

Table 36. Fundamental Mode Crystal Characteristics

These are the characteristics of a crystal for meeting the ±100 ppm requirements of T1.601 for NT operation. The parasitic capacitance of the PC board to which the T7256 crystal is mounted must be kept within the range of 0.6 pF ± 0.4 pF.

Parameter	Symbol	Test Conditions	Specifications	Unit
Center Frequency	Fo	With 25.0 pF of loading	15.36011	MHz
Tolerance Including Calibration, Temperature Stability, and Aging	TOL	—	±60	ppm
Drive Level	DL	Maximum	0.5	mW
Series Resistance	Rs	Maximum	20	Ω
Shunt Capacitance	Co	—	3.0 ± 20%	pF
Motional Capacitance	Cm	—	12 ± 20%	fF

Electrical Characteristics (continued)

Crystal Characteristics (continued)

Table 37. Internal PLL Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit
Total Pull Range	—	±250	—	—	ppm
Jitter Transfer Function	–3 dB point (NT), 18 kft 26 AWG	—	5*	—	Hz
Jitter Peaking	1.5 Hz typical	—	1.0*	—	dB

* Set by digital PLL; therefore, variations track U-interface line rate.

Timing Characteristics

T_A = –40 °C to +85 °C, V_{DD} = 5 V ± 5%, GND = 0 V, Crystal Frequency = 15.36011 MHz.

Table 38. TDM Bus Timing

Symbol	Parameter	Min	Typ	Max	Unit
t_{CDC}	TDMCLK Duty Cycle	39	47	54	%
t_{CHFS}	TDMCLK High to FS (high or low)	—	—	15	ns
t_{CHDOV}	TDMCLK High to TDMO Valid	—	—	50	ns
t_{DIVCL}	Receive Data (TDMI) Setup	25	—	—	ns
t_{CLDIX}	Receive Data (TDMI) Hold	25	—	—	ns
t_{CHDOZ}	TDMCLK High to Tristate TDMO	—	—	45 *	ns
t_{CR}/t_{CF}	TDMCLK Rise/Fall Time	—	—	20	ns
t_{FSR}/t_{FSF}	FS Rise/Fall Time	—	—	20	ns

* Devices connecting to the CHI must be able to withstand 45 ns of bus contention. At this time, the output current is less than 10% of the output high and output low currents. The TDMD pin on the T7256 was designed to withstand 80 ns of bus contention.

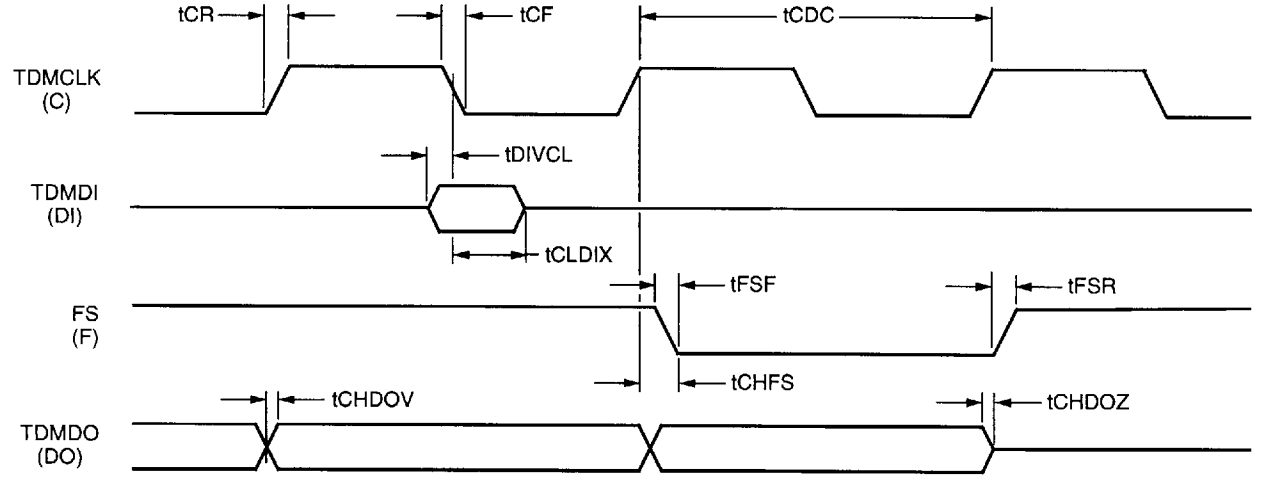


Figure 29. TDM Bus Timing

Timing Characteristics (continued)

Table 39. Clock Timing (See Figure 30.)

Symbol	Parameter	Min	Typ	Max	Unit
SYN8K	8 kHz Duty Cycle	49.8	—	50.2	%
CKOUT	Duty Cycle:				
	In 15.36011 MHz Mode	40	—	60	%
	In 10.24 MHz Mode	23*	—	52*	%
tR1, tF1	Rise or Fall Time	—	30	—	ns
tCOLFH	CKOUT Clock to Frame Sync (SYN8K)	—	—	50	ns
tR2, tF2	CKOUT Clock Rise or Fall	—	15	—	ns

* Includes the effect of phase steps generated by the digital phase-locked loop.

Figure 30. Timing Diagram Referenced to F

Table 40. RESET Timing

Parameter	Description	Min	Max	Unit
tRSLFL, tFLRSH	RESET Setup and Hold Time	60	—	ns
tRSLRSH	RESET Low Time:			
	From Idle Mode or Normal Operation	375	—	µs
	From Power-on	1.5	—	ms

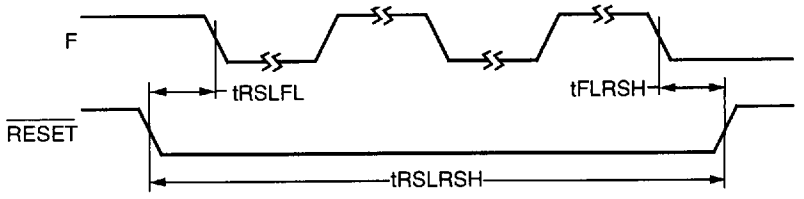


Figure 31. RESET Timing Diagram

Switching Test Input/Output Waveform

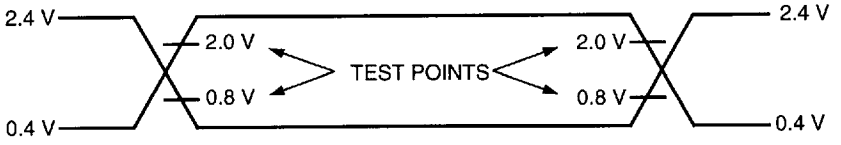


Figure 32. Switching Test Waveform for RESET Timing

Timing Characteristics (continued)

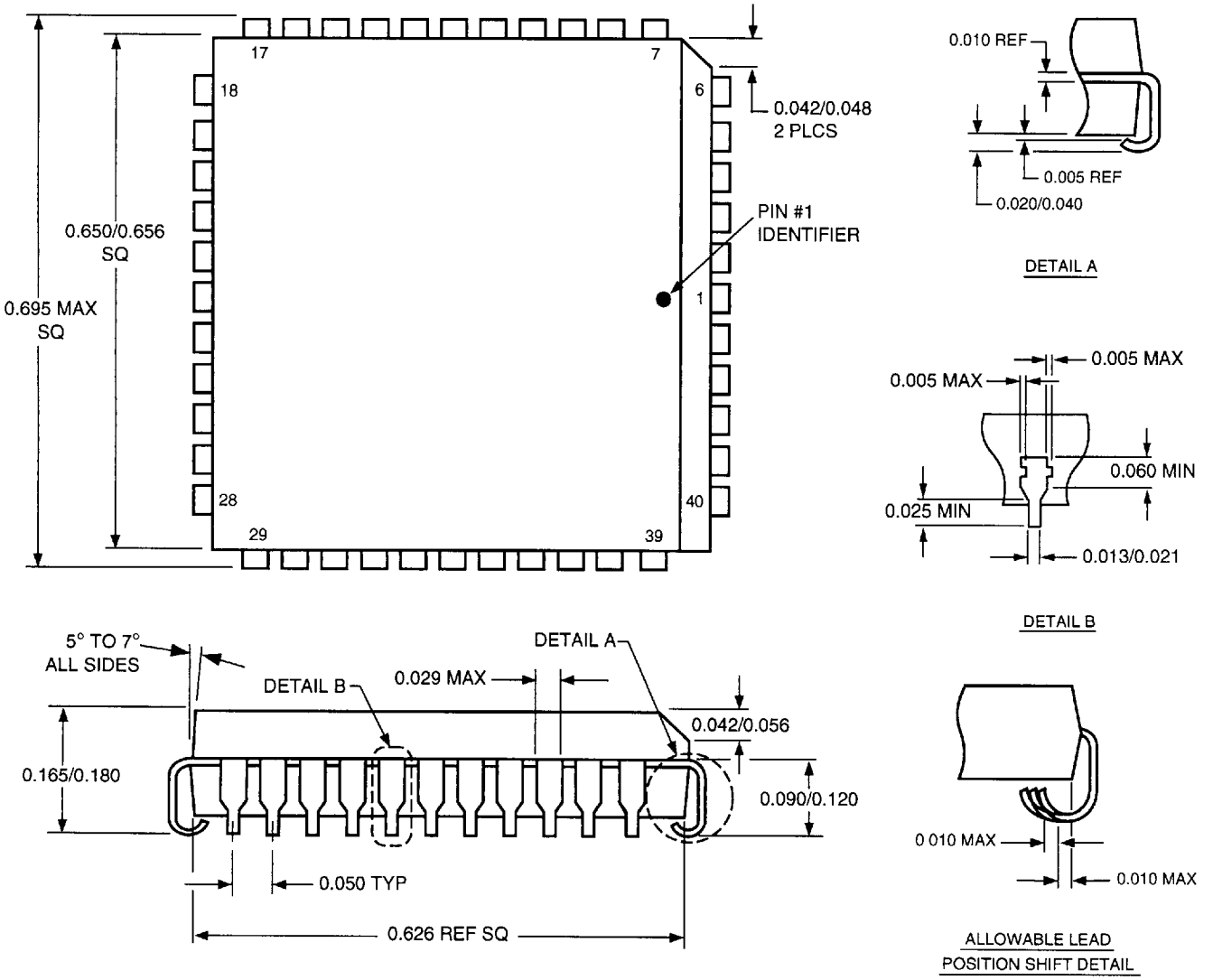
Propagation Delay

The maximum propagation delay from the S/T-interface to the U-interface (upstream direction) is 750 µs. The maximum propagation delay from the U-interface to the S/T-interface (downstream direction) is 550 µs.

Outline Diagram

44-Pin, PLCC

Controlling dimensions are in inches.



Ordering Information

Device Code	Package	Temperature
T-7256- - -ML2	44-Pin PLCC	–40 °C to +85 °C

Questions and Answers

Introduction

This section is intended to answer questions that may arise when using the T7256 Single-Chip NT1 Transceiver.

The questions and answers are divided into three categories: U-interface, S/T-interface, and miscellaneous.

U-Interface

Q1: Is the line interface for the T7256 the same as for the T7264?

A1: Yes. The U-interface section on these chips is identical, so their line interfaces are also identical.

Q2: Why is a higher transformer magnetizing inductance used (as compared to other vendors)?

A2: It has been determined that a higher inductance provides better linearity. Furthermore, it has been found that a higher inductance at the far end provides better receiver performance at the near end and better probability of start-up at long loop lengths.

Q3: Can the T7256 be used with a transformer that has a magnetizing inductance of 20 mH?

A3: The echo canceler and tail canceler are optimized for a transformer inductance of approximately 80 mH and will not work with lower inductance transformers.

Q4: Are the AT&T U-interface transformers available as surface-mount components?

A4: Not at this time.

Q5: Are there any future plans to make a smaller height 2-wire transformer?

A5: Due to the rigid design specifications for the transformer, vendors have found it difficult to make the transformer any smaller. We are continuing to work with transformer vendors to see if we can come up with a smaller solution.

Q6: The line interface components' specifications require 16.9 Ω resistors on the line side of the transformer when using the 2754H2. For our application, we would like to change this value. Can the U-interface line-side circuit be redesigned to change the value of the line-side resistors?

A6: Yes. For example, the line-side resistances can be reflected back to the device side of the transformer so that, instead of having 16.9 Ω on each side of the transformer, there are no resistors on the line side of the transformer and 24.4 Ω resistors on the device side ($16.9 + 16.9/N^2$, where N is the turns ratio of the transformer). However, there may be a slight performance penalty in this case since the on-chip hybrid network is optimized for 16.9 Ω of resistance on the device side of the transformer.

Q7: Table 2, T7256 Reference Schematic Parts List, states the 1 µF capacitor that is used with the LH1465 (C22) must have an insulation resistance of >10 GΩ. Why?

A7: This capacitor is used to set the gate/source voltage for the main transistor in the device. The charging currents for this capacitor are on the order of microamps. Since the currents are so small, it is important to keep the capacitor leakage to a minimum.

Q8: The dc blocking capacitor specified is 1 µF. Can it be increased to at least 2 µF?

A8: This value can be increased to 2 µF without an effect on performance. However, for an NT1 to be compliant with T1.601-1992 Section 7.5.2.3, the dc blocking capacitor must be 1.0 µF ± 10%.

Questions and Answers (continued)

Q9: What is the purpose of the 3000 pF capacitors in the U-line interface figure in the data sheet?

A9: The capacitors are for common-mode noise rejection. The ANSI T1.601 specification contains no requirements on longitudinal noise immunity. Therefore, these capacitors are not required in order to meet the specification. However, there are guidelines in IEC 801-6 which suggest a noise immunity of up to 10 Vrms between 150 kHz and 250 MHz. At these levels, the 10 kHz tone detector in the T7256 may be desensitized such that tone detection is not guaranteed on long loops. The 3000 pF was selected to provide attenuation of this common-mode noise so that tone detector sensitivity is not adversely affected. Since the 3000 pF capacitor was selected based only on guidelines, it is not mandatory, but it is recommended in applications which may be susceptible to high levels of common-mode noise. The final decision depends on the specific application.

As for the size of the capacitors, lab tests indicate the following:

1. The performance of the system suffers no degradation until the values are increased to about 0.1 µF.
2. The return loss at 25 kHz increases with increasing capacitor value.
3. The capacitor value has no effect on longitudinal balance.
4. A large unbalance in the capacitor values did not effect return loss, longitudinal balance, or performance.

Q10: Are there any recommended common filtering parts for the U-interface? I suspect that our product may have emissions problems, and I want to include a provision for common-mode filtering on the U-interface.

A10: The only common-mode filtering parts we have any data on are two common-mode chokes from Pulse Engineering (619) 674-8100 that are intended to help protect against external common-mode noise. The part numbers are PE-68654 (12.5 mH) and PE-68635 (4.7 mH), and in lab experiments, no noticeable degradation in transmission performance was observed. These chokes are typically effective in the frequency range 100 kHz—1 MHz.

As far as emissions are concerned, we don't have a lot of data. We have seen some success with the use of RJ-45 connectors that have integral ferrite beads such as those from Corcom, Inc., (708) 680-7400. These provide some flexibility in that they have the same footprint as some standard RJ-45 connectors.

Q11: I am planning on using a Raychem PTC (p/n TR600-150) on the U-interface of the T7256. The device is rated at 6 Ω—12 Ω. I plan on using this resistor and a 4.87 Ω resistor in place of one of the 16.9 Ω line side resistors. I am concerned about the loose tolerance on the PTC resistance. Will I be able to pass the return loss requirements in ANSI T1.601 Section 7.1?

A11: The NT1 impedance limits looking into tip/ring are derived from the T1.601 return loss requirements (Figure 19 in T1.601). At the narrowest point in the templates, the permissable range is between 111 Ω to 165 Ω. The tolerance on the PTC will reduce the impedance margin somewhat, but should still be acceptable.

Questions and Answers (continued)

A11: (continued)

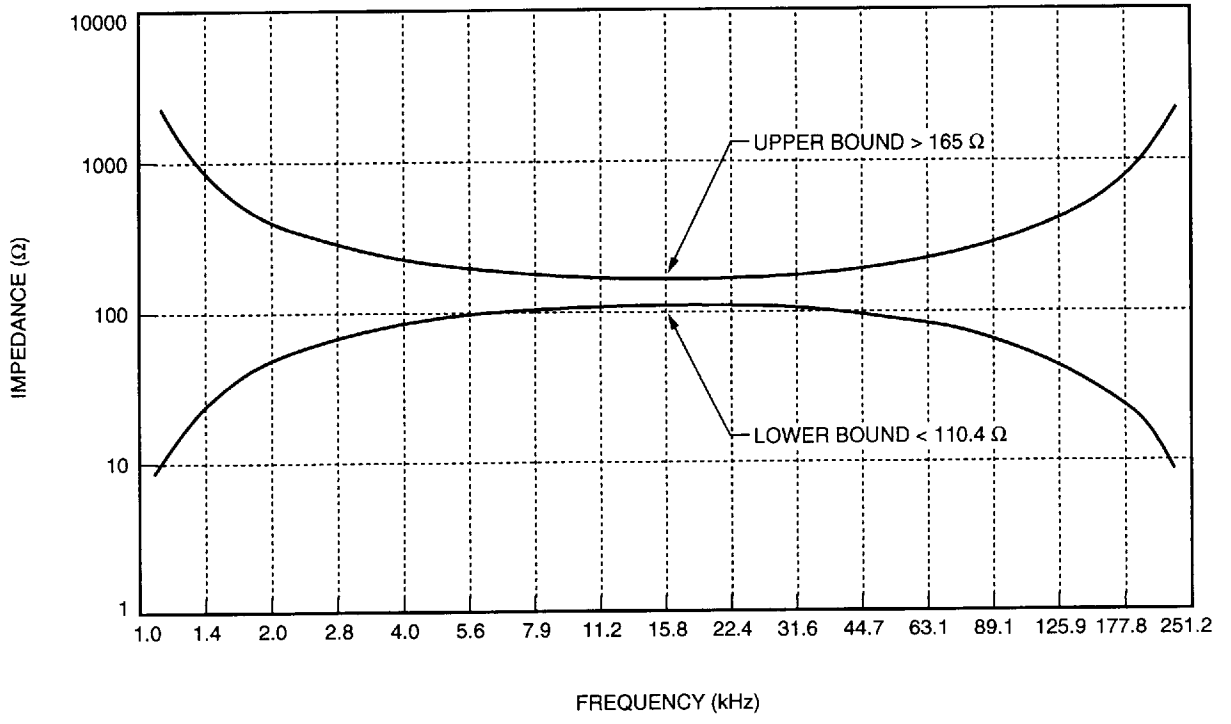


Figure 33. Transceiver Impedance Limits

Figure 33 is derived from the return loss template in ANSI T1.601. Return loss is a measure of the match between two impedances on either side of a junction point. The following equation is an expression of return loss in terms of the complex impedances of the two halves of the circuit Z_1, Z_2.

$$RL\ (dB) = 20 \log \left| \frac{Z1 + Z2}{Z1 - Z2} \right|$$

When the impedances are not matched the junction becomes a reflection point. For a perfectly matched load, the return loss is infinite, whereas for an open or short circuit, the return loss is zero. The return loss expresses the ratio of incident to reflected signal power and should consequently be fairly high.

Questions and Answers (continued)

A11: (continued)

It is desirable to express the return loss in terms of impedance bounds, since an impedance measurement is relatively simple to make. From the above equation, upper and lower bounds on impedance magnitude can be derived as follows:

Z_O = Return Loss Reference Impedance = 135 Ω

Z_U = Upper Impedance Curve

Z_L = Lower Impedance Curve

Upper Bound ($Z_U > Z_O$):

$$RL\ (dB) = 20 \log \left| \frac{Z_O + Z_U}{Z_U - Z_O} \right|$$

Lower Bound ($Z_L < Z_O$):

$$RL\ (dB) = 20 \log \left| \frac{Z_O + Z_L}{Z_U - Z_L} \right|$$

Note that, the higher the minimum return loss requirement, the tighter the impedance limits will be around Z_O, and conversely.

So, for the upper bound, solve for Z_U:

$$Z_U = Z_O \frac{10^{\frac{RL}{20}} + 1}{10^{\frac{RL}{20}} - 1} = |Z_O| \frac{1 + 10^{\frac{-RL}{20}}}{1 - 10^{\frac{-RL}{20}}}$$

For the lower bound, solve for Z_L:

$$Z_L = Z_O \frac{10^{\frac{RL}{20}} - 1}{10^{\frac{RL}{20}} + 1} = |Z_O| \frac{1 - 10^{\frac{-RL}{20}}}{1 + 10^{\frac{-RL}{20}}}$$

Plotting the above equations (using 135 for Zo and Figure 19 in T1.601 for the RL values) results in the graph shown in Figure 33, which shows the return loss expressed in terms of impedance upper and lower bounds.

Questions and Answers (continued)

Q12: Why must secondary protection, such as a *Motorola* SA6.0CA protection diode, be used?

A12: The purpose of the diode is to protect against metallic surges below the breakdown level of the primary protector.

Such metallic surges can be coupled through the transformer and could cause device damage if the currents are high. The protector does not provide absolute protection for the device, but it works in conjunction with the built-in protection on the device leads.

The breakdown voltage level for secondary protection devices must be chosen to be above the normal working voltage of the signal and typically below the breakdown voltage level of the next stage of protection. The SA6.0CA has a minimum breakdown voltage level of 6.7 V and a maximum breakdown voltage of 7.4 V (for detailed information, refer to the *Motorola TVS/Zener Device Data Book*, # DL150/D, 1994).

The chip pins that the SA6.0CA protects are pins 36 (HP), 31 (HN), 32 (LOP), and 35 (LON). The 16.0 Ω resistors will help to protect pins 32 and 35, but pins 31 and 36 will be directly exposed to the voltage across the SA6.0CA. The on-chip protection on these pins consists of output diodes and a pair of polysilicon resistors. These pins have been thoroughly tested to ensure that an 7.4 V level will not damage them; therefore, no third level of protection is needed between the SA6.0CA and the HP and HN pins.

The SA6.0CA has a maximum reverse surge voltage level of 10.3 V at 48.5 A. Sustained currents this large on the device side of the transformer are not a concern in this application.

Thus, there should never be more than 7.4 V across the SA6.0CA, except for possibly an ESD or lightning hit. In these cases, the T7256 is able to withstand at least ±1000 V (human-body model) on its pins.

Q13: Where can information be obtained on lightning and surge protection requirements for 2B1Q products?

A13: Requirements vary among applications and between countries. ANSI T1.601, Appendix B, provides a list of applicable specifications to which you may refer. Also, there are many manufacturers of overvoltage protection devices who are familiar with the specifications and would be willing to assist in surge protection design. The ITU-T K series recommendations are also a good source of information on protection, especially recommendation K.11, "Principles of Protection Against Overvoltages and Overcurrents," which presents an overview of protection principles. Also refer to the application notes mentioned in the U-interface Description section of this data sheet.

Q14: ITU-T specification K.21 describes a lightning surge test for NT1s (see Figure 1/K.21 and Table 1/K.21, Test #1) in which both Tip and Ring are connected to the source and a 1.5 kV voltage surge is applied between this point and the GND of the NT1. What are the protection considerations for this test? Are the HP and HN pins susceptible to damage?

A14: The critical component in this test is the transformer since its breakdown voltage must be greater than 1.5 kV. Assuming this is the case, the only voltage that will make it through to the secondary side of the transformer will be primarily due to the interwinding capacitance of the transformer coils. This capacitance will look like an impedance to the common-mode surge and will therefore limit current on the device side of the transformer. The device-side voltage will be clamped by the SA6.0CA device. The maximum breakdown voltage of the SA6.0CA is 7.4 V. The 16.9 Ω resistors will help protect the LOP and LON pins on the T7256 from this voltage. However, this voltage will be seen directly on pins 36 and 31 (HP and HN) on the T7256. The on-chip protection on these pins consists of output diodes and a pair of polysilicon resistors. These pins have been thoroughly tested to ensure that an 7.4 V level will not damage them; therefore, no third level of protection is needed between the SA6.0CA and the HP and HN pins.

Questions and Answers (continued)

Q15: Can the range of the T7256 on the U-interface be specified in terms of loss? What is the range over straight 24 awg wire?

A15: ANSI Standard T1.601, Section 5.1, states that transceivers meeting the U-interface standard are intended to operate over cables up to the limits of 18 kft (5.5 km) 1300 Ω resistance design. Resistance design rules specify that a loop (of single- or mixed-gauge cable; e.g., 22 awg, 24 awg, and 26 awg) should have a maximum dc resistance of 1300 Ω, a maximum working length of 18 kft, and a maximum total bridged tap length of 6 kft.

The standard states that, in terms of loss, this is equivalent to a maximum insertion loss of 42 dB @ 40 kHz. AT&T has found that, for assessing the condition of actual loops in the field in a 2B1Q system, specifying insertion loss as 33.4 dB @ 20 kHz more closely models ANSI circuit operation. This is equivalent to a straight 26 awg cable with 1300 Ω dc resistance (15.6 kft).

The above goals are for actual loops in the outside loop plant. These loops may be subjected to noise and jitter. In addition, as mentioned above, there may be bridge taps at various points on the loop. The T1.601 standard defines 15 loops, plus the null, or 0 length loop, which are intended to represent a generic cross section of the actual loop plant.

A 2B1Q system must perform over all of these loops in the presence of impairments with an error rate of <1E-7. Loop #1 (18 kft, where 16.5 kft is 26 awg cable and 1.5 kft is 24 awg cable) is the longest, so it has the most loss (37.6 dB @ 20 kHz and 47.5 dB @ 40 kHz). Note that this is more loss than discussed in the preceding paragraph. The difference is based on test requirements vs. field deployment. The test requirements are somewhat more stringent than the field goal in order to provide some margin against severe impairments, complex bridged taps, etc.

If a transceiver can operate over Loop #1 error-free, it should have adequate range to meet all the other loops specified in T1.601. Loop #1 has no bridged taps, so passing Loop #1 does not guarantee that a transceiver will successfully start up on every loop. Also, due to the complex nature of 2B1Q transceiver start-up algorithms, there may be shorter loops which could cause start-up problems if the transceiver algorithm is not robust. The T7256 has been tested on all of the ANSI loops per the T1.601 standard and passes them all successfully. Two loops commonly used in the lab to evaluate the performance of the T7256 silicon are as follows:

Loop Configuration	Bridge Taps (BT)	Loss @ 20 kHz (dB)	Loss @ 40 kHz (dB)
18 kft 26 awg	None	38.7	49.5
15 kft 26 awg	2 at near end, each 3 kft 22 awg	37.1	46.5

The T7256 is able to start up and operate error-free on both of these loops. Neither of these loops is specified in the ANSI standard, but both are useful for evaluation purposes. The first loop is used because it is simple to construct and easy to emulate using a lumped parameter cable model, and it is very similar to ANSI Loop #1, but the loss is slightly worse. Thus, if a transceiver can start up on this loop and operate error-free, its range will be adequate to meet the longest ANSI loop. The second loop is used because, due to its difficult bridge tap structure and its length, it stresses the transceiver start-up algorithms more than any of the ANSI-defined loops. Therefore, if a transceiver can start up on this loop, it should be able to meet any of the ANSI-defined loops which have bridge taps. Also, on a straight 26 awg loop, the T7256 can successfully start up at lengths up to 21 kft. This fact, combined with reliable start-up on the 15 kft 2BT loop above, illustrates that the T7256 provides ample start-up sensitivity, loop range, and robustness on all ANSI loops.

Another parameter of interest is pulse height loss (PHL). PHL can be defined as the loss in dB of the peak of a 2B1Q pulse relative to a 0 length loop. For an 18 kft 26 awg loop, the PHL is about 36 dB, which is 2 dB worse than on ANSI Loop #1. A signal-to-noise ratio (SNR) measurement can be performed on the received signal after all the signal processing is complete (i.e., at the input to the slicer in the decision feedback equalizer). This is a measure of the ratio of the recovered 2B1Q pulse height vs. the noise remaining on the signal. The SNR must be greater than 22 dB in order to operate with a bit error rate of <1E-7. With no impairments, the T7256 SNR is typically 32 dB on the 18 kft/26 awg loop. When all ANSI-specified impairments are added, the SNR is about 22.7 dB, still leaving adequate margin to guarantee error-free operation over all ANSI loops.

Questions and Answers (continued)

A15: (continued)

Finally, to estimate range over straight 24 awg cable, the 18 kft loop loss can be used as a limit (since the T7256 can operate successfully with that amount of loss) and the following calculations can be made:

Loss of 18 kft 26 awg loop @ 20 kHz	38.7 dB
Loss per kft of 24 awg cable @ 20 kHz	1.6 dB

$$\frac{38.7\ \text{dB}}{1.6\ \text{dB/kft}} = 24\ \text{kft}$$

Thus, the operating range over 24 awg cable is expected to be about 24 kft.

Q16: What cable simulator is used for evaluating the T7256 U-interface?

A16: Real cable is used for ANSI loop performance measurements. We have evaluated several commercial cable simulators, but were not satisfied with their accuracy in loop emulation and impairments generation.

Q17: What does the energy spectrum of a 2B1Q signal look like?

A17 Figure A1 (curve P1) in the ANSI T1.601 standard illustrates what this spectrum looks like.

Q18: Please clarify the meaning of ANSI Standard T1.601, Section 7.4.2, Jitter Requirement #3.

A18: The intent of this requirement is to ensure that after a deactivation and subsequent activation attempt (warm start), the phase of the receive and transmit signals at the NT will be within the specified limits relative to what they were prior to deactivation. This is needed so that the LT, upon a warm-start attempt, can make an accurate assumption about the phase of the incoming NT signal with respect to its transmit signal. Note that the T7256 meets this requirement by design because the NT phase offset from transmit to receive is always fixed.

Q19: I need a way to generate a scrambled 2B1Q data stream from the T7256 for test purposes (e.g., ANSI T1.601 section 5.3.2.2, total power and section 7.2, longitudinal output voltage). How can I do this?

A19: A scrambled 2B1Q data stream (the "SN1" signal described in ANSI T1.601 Table 5) can be generated by pulling ILOSS (pin 6) low on the T7256.

Q20: We are trying to do a return loss measurement on the U-interface of the T7256 per ANSI T1.601 section 7.1. We are using a circuit similar to the one you recommend in the data sheet. We have observed the following. When the chip is in IDLE mode (powered on but no activity on the U- or S/T-interfaces), the return loss is very low, i.e., the termination impedance appears to be very large relative to 135 Ω and falls outside the boundaries of Figure 19 of ANSI T1.601. However, if we inject a 10 kHz tone before making a measurement, the return loss falls within the template. Why is it necessary to inject the 10 kHz tone in order to get this test to pass? Shouldn't a 135 Ω impedance be presented to the network regardless of the state of the T7256 once it is powered on?

A20: The return loss is only relevant when the transmitter section is powered on. When the transmitter is powered, it presents a low-impedance output to the U-interface. The transmitter must be held in this low-impedance state when the return loss *and* longitudinal balance tests are performed. This can be accomplished by pulling RESET low (pin 43). In the RESET state, the transmitter is held in a low impedance state and not able to transmit, and won't respond to any incoming wakeup tones. This is different than the IDLE state that the chip enters after power on or deactivation. In IDLE, the transmitter is powered down and in a high-impedance state, with only the tone detector powered on and looking for a far-end wakeup tone. The transmitter powers down when in IDLE state to save power and maximize the tone detector sensitivity. The reason that the chip behaves as it does in your tests is that your test begins with the transmitter in its IDLE state, causing the return loss to be very low. If a 10 kHz signal is applied, the tone detector senses the applied signal and triggers. This causes the transmitter to enter its low-impedance state, where it will remain until the T7256 start-up state machine times out (typically 480 ms for this case due to Loss of Signal > 480 ms, see Table C1 State H4 in ANSI T1.601).

Questions and Answers (continued)

Q21: Is there some way to generate single U-interface pulses from the T7256 for pulse template testing?

A21: This is possible, but only with an external test board that AT&T-ME is willing to lend to customers for conformance test purposes. This board is called the SPEC (Single Pulse Eye Control) board, and supports several test modes. It will produce a single U-interface pulse of programmable magnitude and polarity every 125 µs. On the S/T-interface, it will allow activation of the S/T-interface without a U-interface connected, and will place the S/T-interface in loopback C so that data sent by a test set configured for TE operation can be looped back to the test set (this is what is typically required for S/T testers such as the Siemens K1403 to perform S/T pulse template measurements). The SPEC board also supports reading and writing of T7256 registers and can display the eye pattern of the received data. If you intend to use this board, please request a copy of the SPEC manual. It explains which T7256 signals must be made available on your product in order to interface to this board, and which signals should not be tied directly to ground or Vcc. The SPEC manual also contains enough schematic and software information to allow you to produce your own version of this board.

Q22: What are the average cold start and warm start times?

A22: Lab measurements have shown the average cold start time to be about 3.3 s—4.2 s over all loop lengths, and the average warm start time to be around 125 ms—190 ms over all loop lengths.

Q23: What is the U-interface's response time to an incoming wakeup tone from the LT?

A23: Response time is about 1 ms.

Q24: What is the minimum time for a U-interface reframe after a momentary (<480 ms) loss of synchronization?

A24: Five superframes (60 ms).

Q25: Where is the U-interface loopback 2 (i.e., eoc 2B+D loopback) performed in the T7256?

A25: It is performed just inside the chip at the S/T-interface. The S/T receiver is disconnected internally from the chip pins, and the S/T transmit signal is looped back to the receiver inputs so the S/T section synchronizes to its own signal. This ensures that as much of the data path as possible is being tested during the 2B+D loopback.

Q26: Are the embedded operations channel (EOC) initiated B1 and B2 channel loopbacks transparent?

A26: Yes, the B1 and B2 channel loopbacks are transparent, as is the 2B+D loopback.

Q27: How can proprietary messages be passed across the U-interface?

A27: The embedded operations channel (EOC) provides one way of doing this. ANSI standard T1.601 defines 64 8-bit messages which can be used for nonstandard applications. They range in value from binary 00010000 to 01000000.

There is also a provision for sending bulk data over the EOC. Setting the data/message indicator bit to 0 indicates the current 8-bit EOC word contains data that is to be passed transparently without being acted on. Note that there is no response time requirement placed on the NT in this case (i.e., the NT does not have to echo the message back to the LT). Also note that this is currently only an ANSI provision and is not an ANSI requirement. The T7256 does support this provision.

Q28: What is the value of the ANSI T1.601 cso and nib bits in the 2B1Q frame?

A28: cso and nib are fixed at 0 and 1, respectively, by the device. This is because the device always has warm start capability (CSO = 0), and NT1s are required to have nib = 1 per T1.601-1992.

Q29: Are the PS bits controllable from outside the chip?

A29: Yes, the bits are controlled by two pins (8 and 9) on the chip. When the T7256 TDM highway is enabled, these pins change function and become part of the TDM highway and PS1 and PS2 are controlled by registered GR1, bits 1 and 2.

Questions and Answers (continued)

Q30: It looks like the U-interface sai and act bits that the T7256 transmits towards the LT always track one another. If this is the case, I don't understand why they are both needed. Can you explain the purpose of the sai bit and how it relates to the act bit?

A30: The sai bit is equal to 1 when there is activity (INFO 1 or INFO 3) on the S/T-interface. The act bit is 1 whenever layer 1 transparency is established. Most of the time these bits are the same, but there are two situations where they will be different.

1. The sai bit can be used in conjunction with the uoa bit from the LT to support DSL-only activation as described in the ANSI and ETSI standards. The LT can request a U-only activation by setting uoa =0, which will cause the S/T-interface to remain in a deactivated state. If the TE requests an activation under these conditions by transmitting INFO 1 to the T7256, the sai bit will change from 0 to 1, indicating to the LT that there is activity on the S/T-interface so that the LT can respond accordingly. Typically, this means that LT will set uoa = 1 to exit the DSL-only condition so that layer 1 transparency can be established from TE to LT. Thus, in the case of a DSL-only activation, the T7256's sai bit is 1 and its act bit is 0 from the time a TE requests an activation until the following events occur:

   A. LT sets uoa = 1 towards the NT.

   B. The T7256 detects uoa = 1 and transmits INFO 2 on the S/T-interface.

   C. The TE synchronizes and transmits INFO 3 on the S/T-interface.

   D. Upon reception of the INFO 3 signal, the T7256 sets act = 1.

2. If a link is fully active, then the LT detects a transition of the NT act bit from 1 to 0, it is an indication of loss of layer-1 transparency. This can be caused by either a) S/T loss of sync or b) NT1 received INFO 0. Case a) will result in an act = 0 / sai = 1 combination, i.e., S/T sync is lost but there is still activity on the S/T-interface, meaning the TE is having trouble staying synchronized. Case b) will result in an act = 0 / sai = 0 combination, i.e., no activity on the S/T-interface (INFO 0), meaning the TE has been disconnected (there is no way the TE can legally send INFO 0 when the link is fully active because the TE is not allowed to initiate deactivation—only the LT is—so the only other possibility is that it has been disconnected or has failed). Note that this procedure allows the CO to determine whether the cause of loss of layer 1 transparency is a TE that is having synchronization problems or a TE that has been disconnected, based on the state of the sai bit when act = 0.

   The ANSI T1.601 and ETSI DTR/TM 3002 standards contain finite state matrices that describe DSL-only operation. The T7256 follows the behavior described in the matrices. Refer to those tables for detailed information on each of the states.

Questions and Answers (continued)

S/T-Interface

Q31: What is the S/T transformer's inductance?

A31: For AT&T transformers 2768A or 2776, a minimum inductance of 22 mH is guaranteed.

Q32: Can the S/T-interface leads be short-circuited together without harming the device?

A32: Yes, this will not cause any harm to the device.

Q33: What is the common-mode rejection of the S/T receiver?

A33: The common-mode rejection of the S/T receiver is 400 mV. Refer to the Electrical Characteristics described in the data sheet.

Q34: I notice that the Application Note entitled *Design an S/T Line Interface Circuitry Using the T7250C/T7259* recommends relays on both the transmitter and receiver outputs that disconnect the device when power is removed from the chip. Is this necessary for an NT using the T7256?

A34: The relay on the TE transmitter output is necessary to pass the peak current test (ITU-T I.430 Section 8.5.1.2 and ANSI T1.605-1991, section 9.5.1.2) when the TE is powered down. For the NT, there is no equivalent test, so the relay is not necessary. The relay on the TE receiver input is also necessary to pass the peak current test (ITU-T I.430 sections 8.5.1.2 and 8.6.1.1, and ANSI T1.605-1991 sections 9.5.1.2 and 9.6.1.1). For the NT, however, there is enough margin in the line interface capacitance circuitry such that the peak current requirement (ITU-T I.430 section 8.6.1.2 and ANSI T1.605-1991 section 9.6.1.2) can be met without using relays. This assumes, of course, that sound layout practices have been applied to keep parasitic capacitance of the line interface circuitry to a minimum (of primary importance is making sure there is no ground plane under the S/T line interface). The reason the TE needs a relay on its receiver is that the TE tests assume a 350 pF cord connected to the line, and this extra capacitance can cause the peak current requirement to be exceeded. So even though the NT peak current requirement is slightly more stringent (0.5 mA as opposed to 0.6 mA), the TE peak current test is the most difficult to meet due to the 350 pF cord capacitance.

Q35: The T7256 reference design in Figure 6 shows 100 Ω termination resistors in parallel with a second pair of optional 100 Ω resistors that can be inserted or removed by installing/removing jumpers from JMP1 and JMP2. What is the purpose of this second pair of resistors?

A35: Typically, a TE or group of TEs connected to an NT1 will have a 100 Ω termination located at the interface point of the TE farthest from the NT1 (refer to ITU-T I.430 Figure 2 and section 4 or T1.605 Figure 2 and section 5). However, in some cases it may be desirable to operate an NT1 with a TE that does not provide the 100 Ω termination impedance. In this case, the provisional 100 Ω resistors shown in Figure 6 may be installed to provide the extra termination impedance required.

Q36: I would like to integrate an NT1 onto my T7250C-based 4-wire ISDN product. Is there a way I can avoid having to use two sets of S/T transformers, protection diodes, etc. to convert the S/T-interface (i.e., one set on the T7250C and one set on the T7256)?

A36: If no external S/T-interface connection is required, the T7250C and T7256 can be directly connected as shown in the following diagram. If it is required to be able to connect an external TE, the circuit shown in Figure 34 can be used.

Questions and Answers (continued)

A36: (continued)

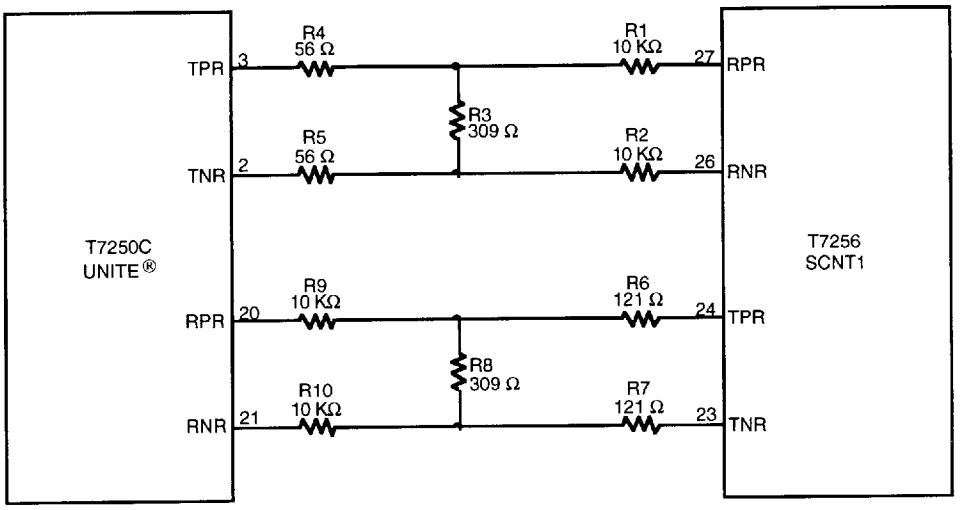


Figure 34. T7256 to T7250C Direct Connection

Questions and Answers (continued)

Q37: What is the state of the D-echo bit during an EOC 2B+D loopback?

A37: The D-echo bit (SXE, GR2, bit 3) should be set to zero to meet the ITU-T I.430 requirement in Appendix I, Note 4, which states that during a loopback 2 (eoc 2B+D loopback), the NT1 should send INFO 4 frames toward the TE with the D-echo channel bits set binary zero. If AUTOEOC = 1 (register GRO, bit 4), SXE is internally overridden to 0 by the T7256. If AUTOEOC = 0, SXE must be set to 0 by the user.

Q38: Is it possible to make a nontransparent single B channel loopback toward the S/T-interface via the microprocessor?

A38: Yes. Refer to the data sheet for a description of the ITU-T I.430 Loop C loopback control bits (register DFRO).

Q39: What is the purpose of the SFECV bit in register SIR0?

A39: ANSI T1 T1.605 Table 8, "Codes for Q-Channel and SC1-Subchannel Messages," defines an SC1-Subchannel message, "Far-End Code Violation" (SC11, SC12, SC13, SC14 = 1110). This is an S channel message that the NT can send to the TE to indicate that a previous multiframe received by the NT contains one or more illegal S/T line code violations. In an NT1 that supports multiframing, the SFECV bit can be used to generate an interrupt to the T7256 microprocessor indicating that it should transmit the "Far-End Code Violation" message to the TE in S-Subchannel one. This subchannel is accessed via register MCR1 bits 0—3.

Q40: In the Analog Interface section of the S/T-interface Description in the data sheet, where does the value of 0—3.1 ms max. differential delay in adaptive timing mode come from?

A40: The minimum value of 0 ms is necessary so that the NT's transmitter and receiver can be directly connected in a loopback and still synchronize. The maximum value of 3.1 ms comes about because the "window" size needed in the adaptive timing algorithm is 2.1 ms. The window size is the time during each bit period in which no transitions may occur. Since a period is 5.2 ms, the time during which there may be transitions is 5.2 – 2.1 ms, or 3.1 ms. This is the same as the maximum differential delay, since the earliest and latest bit transitions represent the nearest and farthest TEs relative to the NT receiver.

Miscellaneous

Q41: Is the ±100 ppm free-run frequency recommendation met in the T7256?

A41: In the free-run mode, the output frequency is primarily dependent on the crystal, not the silicon design. For low-cost crystals, initial tolerance, temperature, and aging effects may account for two-thirds of this budget, and just a couple of pF of variation in load capacitance will use up the rest; therefore, the ±100 ppm goal can be met if the crystal parameters are well controlled. See the Crystal Characteristics section in the data sheet.

Q42: It has been noted in some other designs that the crystal has a capacitor from each pin to ground. Changing these capacitances allows the frequency to be adjusted to compensate for board parasitics. Can this be done with the T7256 crystal? Also, can we use a crystal from our own manufacturer?

A42: The crystal for the T7256 is tuned to a particular load capacitance that does not include external capacitors. The advantage to this is that no external components are required. The disadvantage is that board parasitics must be very small. The crystal characteristics section of the data sheet notes that the board parasitics must be within the range of 0.6 pF ± 0.4 pF. AT&T does not require that a particular crystal be used, but we strongly recommend adhering to the crystal parameters specified in the data sheet. A crystal which deviates from these parameters may work under most conditions, but we cannot guarantee that it will start up and/or meet the ±100 ppm requirement under all operating conditions.

Questions and Answers (continued)

Q43: What clocks are available on the T7256?

A43: The following clocks are available:

1. SYN8K, pin 4 (8 kHz clock) is enabled by holding SDI (pin 12) low during an external RESET.
2. TDMCLK, pin 9 (2.048 MHz clock) is enabled by writing TDMEN = 0 (register GR2, bit 5).
3. CKOUT, pin 17 (10.24 MHz or 15.36011 MHz clock) is enabled by writing register GRO bit 2 or 1, respectively, to 0. Normally tristated.

Note that using clocks 2 or 3 above requires a microprocessor for setting the appropriate configuration.

Q44: I plan to program the T7256 to output 15.36 MHz from its CKOUT pin. Is this clock a buffered version of the 15.36 MHz oscillator clock? I am concerned that if it is not buffered, the capacitive loading on this pin could affect the system clock frequency.

A44: The 15.36 MHz output is a buffered version of the XTAL clock and therefore hanging capacitance on it will not affect the T7256's system clock frequency.

Q45: How does the filtering at the OPTOIN input work?

A45: The signals applied to OPTOIN are digitally filtered for 20 ms. Any transitions under 20 ms will be ignored.

Q46: Can the T7256 operate with an external 15.36011 MHz clock source instead of using a crystal?

A46: No.

Q47: What is the effect of ramping down the power supply voltage on the device? When will it provide a valid reset? This condition can occur when a line-powered NT1's line cord is repeatedly plugged-in and removed and plugged-in again before the power supply has had enough time to fully ramp-up.

A47: The device's reset is more dependent on the RESET pin than the power supply to the device. As long as the proper input conditions on the RESET pin (see Table 40) are met, the device will have a valid reset. Note that this input is a Schmitt-trigger input.

Q48: Is there a recommended method for powering the T7256? For example, is it desirable to separate the power supplies, etc.?

A48: The T7256 is not extremely sensitive to power supply schemes. Following standard practices of decoupling power supplies close to the chip and, if power and ground planes are not used, keeping power traces away from high-frequency signals, etc., should yield acceptable results. Separating the T7256 analog power supplies from the digital power supplies near the chip may yield a small improvement, and the same holds true for using power and ground planes vs. discrete traces.

Note that if analog and digital power supplies are separated, the crystal power supply (V_{DDO}) should be tied to the digital supplies (V_{DDD}).

Q49: What are the filter characteristics of the PLL at the NT?

A49: The –3 dB frequency is approximately 5 Hz, peaking is about 1.2 dB.

Q50: Can the T7256 operate in the LT mode?

A50: No, the T7256 is optimized for the NT side of the loop and cannot operate in the LT mode.

Q51: Can you provide detailed information on the active and idle power consumption of the T7256?

A51: The IDLE power of the T7256 is typically 35 mW. The IDLE power will be increased if CKOUT or the TDM highway are active. The discussion below presents accurate numbers for adding in the effects of CKOUT and the TDM highway.

When considering active power measurement figures, it is important to note that the conditions under which power measurements are made are not always completely stated by 2B1Q IC vendors. For example, loop length is not typically mentioned in the context of power dissipation, yet power dissipation on a short loop is noticeably greater than on a long loop. There are two reasons for the increased power dissipation at shorter loop lengths:

1. The overall loop impedance is smaller, requiring a higher current to drive the loop.
2. The far-end transceiver is closer, requiring the near-end transceiver to sink more far-end current in order to maintain a virtual ground at its transmitter outputs.

Questions and Answers (continued)

A51: (continued)

The following lab measurements provide an example of how power dissipation varies with loop length for a specific T7256 with its 15.36011 MHz CKOUT output disabled (see the following table for information on CKOUT). Note that power dissipation on a 0 length loop (the worst-case loop) is about 35 mW higher than on a loop of >3 kft length—a significant difference. Thus, loop length needs to be considered when determining worst-case power numbers.

Loop Configuration	Power (mW)
18 kft/26 awg	270
6 kft/26 awg	270
3 kft/26 awg	274
2 kft/26 awg	277
1 kft/26 awg	285
0.5 kft/26 awg	293
0 kft	305
135 Ω load, ILOSS or lpbk active, no far-end transceiver*	278

* This is the configuration used by some IC manufacturers.

Also, in the case of the T7256, the use of the output clock CKOUT (pin 17) needs to be considered since its influence on power dissipation is significant. Some applications may make use of this clock, while others may leave it tristated. The power dissipation of CKOUT is as follows:

CKOUT Frequency (MHz)	Power Due to CKOUT 40 pF Load (mW)	Power Due to CKOUT No Load (mW)
15.36011	21.3	11.0
10.24	17.7	9.1

Another factor influencing power consumption is the S/T-interface data pattern. For example, when transmitting an INFO 4 pattern with all 1s data in the B and D channels, the power consumption is 25 mW lower than it is when transmitting INFO 2, because INFO 2 is worst-case in terms of the amount of +0 and –0 transitions, and INFO 4 is best-case if the data is all 1s. A typical number would lie about midway between these two. The T7256 TDM highway, when active, can add another 3 mW of power.

Therefore, it is apparent that the conditions under which power is measured must be clearly specified. The methods AT&T has used to evaluate typical and worst-case power consumption are based on our commitment to provide our customers with accurate and reliable data. Measurements are performed as part of the factory test procedure using automated test equipment. Bench top tests are performed in actual T7256-based systems to correlate the automated test data with an actual implementation. A conservative margin is then added to the test results for publication in our data sheets.

The following table provides power consumption data for several scenarios so that knowledgeable customers can fairly compare transceiver solutions. A baseline scenario is presented in the Case 1 column, and then adders are listed in the Cases 2—6 columns to account for the worst-case condition listed in each column so that an accurate worst-case figure can be determined based on the conditions that are present in a particular application. Note that the tests were run at 5 V, so changes in the supply voltage will change the power accordingly.

Questions and Answers (continued)

A51: (continued)

Table 41. Power Consumption

Variables	Case 1	Case 2	Case 3	Case 4	Case 5	Case 6
Loop Configuration	>3 kft, 26 awg	0 kft*	—	—	—	—
S/T State	INFO 4 with all 1s data	—	INFO 2†	—	—	—
CKOUT, MHz (40 pF load)‡	Tristated	—	—	15.36011	—	—
Temperature (°C)	25	—	—	—	85	—
TDM Highway	Inactive	—	—	—	—	Active
Max. Power Consumption (mW)	277	35	25	22	5	3

* Some 2B1Q silicon vendors specify power using a configuration in which the IC is active and transmitting into a 135 Ω termination, with no far-end transmitter attached. This configuration would cause an increase of 9 mW over the Case 1 column, instead of the 35 mW shown here. This highlights the importance of specifying measurement conditions accurately when making comparisons between chip vendors' power numbers.

† This is a worst-case number representing the state of the S/T-interface where the most +0/–0 transitions occur. In a real application, this will be a transient state, as INFO 4 will occur as soon as synchronization is achieved. The average power consumed during a typical INFO 4, assuming a 50% mix of 1s and 0s in the B and D channels, would be approximately half this number, or 12.5 mW.

‡ See the preceding table for a comparison of power dissipation with negligible capacitive loading on CKOUT. The 40 pF figure chosen here is intended to represent a worst-case condition.

Q52: What would cause the STLED indicator to flash sporadically at an 11 Hz rate?

A52: If the T7256 S/T-interface is operating over a long loop that is outside the range specified in the I.430/T1.605 standard, the T7256 may go into a state where it is constantly going in and out of synchronization. This causes it to cycle between ANSI states H7 and H8, producing STLED state changes between 1Hz flashing and always on. When the S/T-interface loses synchronization, it takes about 96 ms before synchronization can be reacquired. This 96 ms cycle, coupled with the STLED switching from always on to 1 Hz flashing, can appear as 11 Hz or sporadic flashing, depending on how frequently S/T synchronization is being lost.

Either of these states could cause potential confusion to maintenance personnel in the event that a T7256-based NT1 is connected to an S/T loop that is longer than permitted by the standards. For example, an 11 Hz rate is difficult to visually distinguish from the 8 Hz rate, but the 11 Hz case indicates a problem on the S/T-interface and the 8 Hz case indicates a problem on the U-interface. To troubleshoot the STLED indication, unplug the S/T connector and repower the T7256 and initiate a start-up on the U-interface. If there is no problem on the U-interface, the STLED will reach a 1 Hz flashing state and remain there, indicating that the fast flashing was a result of S/T-interface problems.

Questions and Answers (continued)

Q53: What is the state of the T7256 TDM bus output when the unused bits of the D channel octet are transmitted?

A53: The T7256 tristates the TDM bus output when B and D channel information is not transmitted to the TDM bus. This includes the 6-bit interval in the D channel octet.

Q54: The STLED on my T7256-based NT1 behaves in an unexpected way. When a start up attempt is received, it flashes at an 8 Hz rate. Then it flashes briefly at 1 Hz, indicating synchronization on the U-interface. This is expected. However, after this, it starts flashing at 8 Hz, and yet it appears as though the system is operating fine (data is being passed end to end, etc.). Shouldn't the STLED signal be always low (i.e., ON) at this point?

A54: Yes it should. Referring to the STLED Control Flow diagram in Figure 21 of the data sheet, it appears as though you may be receiving aib = 0 from the upstream U-interface element. This will cause the behavior you are seeing. If you have access to the microprocessor registers, you can check this by monitoring register CFR1 bit 6 to see if it ever goes to 0.

Q55: When I try to activate our T7256-based NT1, it appears as though the U-interface is synchronizing (i.e., STLED flashes at 1 Hz), but the S/T-interface won't activate, and there is not even any signal activity on the S/T-interface (i.e., no INFO 1 or INFO 2). What might the problem be?

A55: The behavior you have observed can be caused if the uoa bit received on the U-interface from the network is set to 0. This causes the T7256 to activate the U-interface only, keeping the S/T-interface quiet, per the ANSI and ETSI standards. We have heard of some network equipment that incorrectly sets this bit low. If you have access to the microprocessor registers, you can check this by monitoring register CFR1 bit 3 to see if it is low. If it is, the problem is in the network equipment, not your NT1.

Q56: Can the T7513 CODEC interface to the T7256 TDM bus?

A56: We recommend against using the T7513B with the T7256. The typical way to use the T7513 in this application is in variable-rate mode with TDMCLK as both the master and data clocks. The internal data shift registers will not be properly clocked when data clock duty cycle is outside the 45%—55% range. The T7256 TDMCLK duty cycle can vary in the range 39% to 54%, which violates this specification (note that the CODEC master clock can tolerate this variation).

The reason for the variation in the T7256 TDMCLK is as follows: The T7256 TDMCLK is derived from the internal 10.24 MHz clock. The 10.24 MHz clock is generated by doubling the 15.36 MHz system clock, and dividing by 3 (nominally), or 2 (negative phase step), or 4 (positive phase step). The phase steps occur in order to keep the 10.24 MHz clock phase locked to the U-interface line rate. The maximum rate of occurrence of these phase steps is 4 kHz (this worst-case phase step frequency implies that the line rate and crystal center frequency are at the maximum permissible distance from one another). The nominal 10.24 MHz clock is a 33% duty cycle. When a positive phase step is taken, the duty cycle is 50% (15.36 MHz) for two clock periods, and when a negative phase step is taken, it is a 25% (7.68 MHz) rate for two clock periods.

Since TDMCLK is derived by dividing the 10.24 MHz clock by 5, its duty cycle will change when phase steps occur. The nominal duty cycle of the TDMCLK is 53%. When phase steps occur, the duty cycle can drop to as low as 39% for one clock period (during a positive phase step) or increase to as high as 54% for one clock period (during a negative phase step). How much the duty cycle changes during these phase steps depends on the relative phase of TDMCLK with the 10.24 MHz clock edges on which the phase steps occur. It turns out that there is a 20% chance that the duty cycle will fall outside the 45%—55% range for either positive or negative phase steps. Thus, we recommend against using the T7513B with the T7256.

Questions and Answers (continued)

Miscellaneous (continued)

Q57: What is the purpose of the ACTSEL bit in register GR2 bit 6?

A57: This bit is to provide compatibility with the ANSI T1.601 and ETSI DTR/TM 3002 standards. The 1992 version of T1.601 (the most recent as of this writing) specifies that, upon a loopback 2 eoc request, the NT1's 2B+D data should be looped back immediately and the upstream (NT-to-LT) act bit should be set to 0. ANSI specified that the upstream act bit should be set to 0 to indicate to the LT that end-to-end data transparency (TE-to-LT) is interrupted during a loopback 2. The fact that 2B+D data is looped back immediately means that upstream data transparency at the NT is established independent of the status of the act bit from the LT. Normally, upstream data transparency at the NT is dependent on act = 1 being received from the LT. The reason that loopback 2 transparency criteria differ is that there is no guarantee that the NT1 will receive act = 1 from the LT. Consider the case where an LT wants to activate the U-interface and perform a loopback 2 test on an NT1 with no TE connected. In this case, the LT will never receive act = 1 since, prior to the loopback 2 request, act = 0 because there is no TE attached, and after the loopback 2 request, act = 0 because layer 1 transparency is interrupted. Since the LT will never receive act = 1 from the NT1, it will never send act = 1 back to the NT1. Since the NT1 receipt of act = 1 normally enables upstream transparency, ANSI chose to make an exception to the data transparency requirements in this case and enable upstream transparency immediately upon receipt of the loopback 2 eoc command at the NT1.

The major difference between the ANSI and ETSI standards with regard to how the NT1 handles a loopback 2 request lies in what happens to the upstream act bit. ANSI's position is that act should be set to 0 because a loopback 2 is an interruption to layer 1 transparency. ETSI's position is that the state of the act bit should only be dependent on whether or not the NT1 is receiving INFO 3 from the TE (this is consistent with ANSI T1.601 paragraph 6.4.6.4 and ETSI DTR/TM 3002 paragraph A.10.1.5.1). During a loopback 2, the T7256 will always receive INFO 3 at the S/T-interface (even if there is no TE attached) because it loops back its S/T transmit signal and synchronizes itself to that signal. Therefore, the possibility that LT will never receive act = 1 from the NT does not exist under these rules. As a result, no special exceptions need to be applied to the case of loopback 2 in ETSI. For example, again consider the case where an LT wants to activate the U-interface and perform a loopback-2 test on an NT1 with no TE connected. The NT1 will synchronize to its own S/T signal and detect INFO 3. This will cause act = 1 to be transmitted upstream. The LT will detect act = 1 and set its downstream act = 1. When the NT detects the downstream act = 1, it will enable upstream data transparency. The handling of the act bit and transparency in this case is the same as for a normal activation.

In the ETSI standard, transparency at the NT during loopback 2 is dependent upon the reception of the act bit from the LT, i.e., if act = 1, loopback transparency is established, and if act = 0, loopback data is forced to all 1s. The LT won't send act = 1 until it receives act = 1 from the NT. The NT will not send act = 1 to the LT until it receives an INFO 3 indication (i.e., until its S/T-interface is synchronized as described in the register GR2 ACTSEL bit definition). Thus, data transparency requires that the NT1 set its upstream act bit to 1.

There is a contribution that has been voted onto the ANSI T1E1.4 living list that changes the act bit behavior during loopback 2 to match that specified for ETSI (contribution #T1E1.4/92-089). Thus, the next issue of the T1.601 standard will bring the ANSI and ETSI standards into harmony as pertains to handling of the act bit during a loopback 2.

Glossary

ACTMODE/ $\overline{\text{INT}}$: Act bit mode, serial interface microprocessor interrupt.

ACTR: Receive activation (register CFR1, bit 0.)

ACTSC: Activation/deactivation state change on U-interface (register UIR0, bit 1).

ACTSCM: Activation/deactivation state change on U-interface interrupt mask (register UIR1, bit 1).

ACTSEL: Act mode select (register GR2, bit 6).

ACTT: Transmit activation (register GR1, bit 4).

AFRST: Adaptive filter reset (register CFR0, bit 1).

AIB: Alarm indication bit (register CFR1, bit 6).

ANSI: American National Standards Institute.

ASI: Alternate space inversion.

AUTOACT: Automatic activation control (register GR0, bit 6).

AUTOCTL: Auto control enable (register GR0, bit 3).

AUTOEOC: Automatic eoc processor enable (register GR0, bit 4).

A[3:1]R: Receive eoc address (register ECR2, bits 0—2).

A[3:1]T: Transmit eoc address (register ECR0, bits 0—2).

BERR: Block error on U-interface (register UIR0, bit 2).

BERRM: Block error on U-interface interrupt mask (register UIR1, bit 2).

CCRC Corrupt cyclic redundancy check (register ECR0, bit 7).

CDM: Charged-device model.

CFR0: Control flow state machine control—maintenance / reserved bits register.

CFR1: Control flow state machine status register.

CFR2: Control flow state machine status—reserved bits register.

CKOUT: Clock output.

CODEC: Coder/decoder, typically used for analog-to-digital conversions or digital-to-analog conversions.

CRATE[1:0] CKOUT rate control (register GR0, bits 2—1).

CRC: Cyclic redundancy check.

DFR0: Data flow control—U and S/T B channels register.

DFR1: Data flow control—D channels and TDM bus register.

Digital power.

DMR: Receive eoc data or message indicator (register ECR2, bit 3).

DMT: Transmit eoc data or message indicator (register ECR0, bit 3).

DPGS: Digital pair gain system.

ECR0: eoc state machine control—address register.

ECR2: eoc state machine status—address register.

ECR3: eoc state machine status—information register.

EMINT: Exit maintenance mode interrupt (register MIR0, bit 2).

EMINTM: Exit maintenance mode interrupt mask (register MIR1, bit 2).

EOC: Embedded operations channel.

EOCSC: eoc state change on U-interface (register UIR0, bit 0).

Glossary (continued)

EOCSCM: eoc state change on U-interface mask (register UIR1, bit 0).

ERC1: eoc state machine control—information register.

ESD: Electrostatic discharge.

ETSI: European Telecommunications Standards Institute.

FEBE: Far-end block error (register CFR1, bit 5).

FSC[2:0]: Frame strobe (FS) control, (register TDR0, bits 2—0).

FSP: Frame strobe (FS) polarity (register TDR0, bit 3).

FT: Fixed/adaptive timing control (register GR2, bit 0).

FTE/TDMDI: Fixed/adaptive timing mode select.

GIR0: Global interrupt register.

GND_A: Analog ground.

GND_O: Crystal oscillator ground.

GR0: Global device control—device configuration register.

GR1: Global device control—U-interface register.

GR2: Global device control—S/T-interface register.

HBM: Human-body model.

HDLC: High-level data link control.

$\overline{\text{HIGHZ}}$: High impedance control.

HN: Hybrid negative input for U-interface.

HP: Hybrid positive input for U-interface.

I4C: INFO 4 change (register SIR0, bit 3).

I4CM: INFO 4 change mask (register SIR1, bit 3).

I4I: INFO 4 indicator (register CFR1, bit 7).

ILINT: Insertion loss interrupt (register MIR0, bit 1).

ILINTM: Insertion loss interrupt mask (register MIR1, bit 1).

ILOSS: Insertion loss test control (register CFR0, bit 0).

$\overline{\text{ILOSS}}$: Insertion loss test control.

ISDN: Integrated services digital network.

ITU-T: International Telecommunication Union-Telecommunication Sector.

I[8:1]R: Receive eoc information (register ECR3, bits 0—7).

I[8:1]T: Transmit eoc information (register ERC1, bits 0—7).

LON: Line driver negative output for U-interface.

LOP: Line driver positive output for U-interface.

LPBK: U-interface analog loopback (register GR1, bit 0).

MCR0: Q channel bits register.

MCR1: S subchannel 1 register.

MCR2: S subchannel 2 register.

MCR3: S subchannel 3 register.

MCR4: S subchannel 4 register.

MCR5: S subchannel 5 register.

MINT: Maintenance interrupt (register GIR0, bit 2).

MIR0: Maintenance interrupt register.

MIR1: Maintenance interrupt mask register.

MLT: Metallic Loop Termination.

MULTIF: Multiframing control (register GR0, bit 5).

NEBE: Near-end block error (register CFR1, bit 4).

NTM: NT test mode (register GR1, bit 3).

OOF: Out of frame (register CFR1, bit 2).

OPTOIN: Optoisolator input.

OUSC: Other U-interface state change (register UIR0, bit 3).

Glossary (continued)

OUSCM: Other U-interface state change mask (register UIR1, bit 3).

PS1: Power status #1 (register GR1, bit 2).

PS1E/TDMDO: Power status #1, TDM clock.

PS2: Power status #2 (register GR1, bit 1).

PS2E/TDMCLK: Power status #2, TDM data out.

QMINT: Quiet mode interrupt (register MIR0, bit 0).

QMINTM: Quiet mode interrupt mask (register MIR1, bit 0).

QSC: Q bits state change (register SIR0, bit 1).

QSCM: Q bits state change mask (register SIR1, bit 1).

Q[4:1]: Q channel bits (register MCR0, bits 0—3).

R25R: Receive reserved bits (register CFR2, bit 2).

R25T: Transmit reserved bit (register CFR0, bit 4).

R64T: Transmit reserved bit (register CFR0, bit 5).

$\overline{\text{RESET}}$: Reset.

RNR: Receive negative rail for S/T-interface.

RPR: Receive positive rail for S/T-interface.

RSFINT: Receive superframe interrupt (register UIR0, bit 4).

RSFINTM: Receive superframe interrupt mask (register UIR1, bit 4).

R[16:15]R: Receive reserved bits (register CFR2, bits 1—0).

R[16:15]T: Transmit reserved bits (register CFR0, bits 3—2).

R[64:54:44:34]R: Receive reserved bits (register CFR2, bits 6—3).

SAI[1:0]: S/T-interface activity indicator control (register GR1, bits 6—7).

SC1[4:1]: S subchannel 1 (register MCR1, bits 0—3).

SC2[4:1]: S subchannel 2 (register MCR2, bits 0—3).

SC3[4:1]: S subchannel 3 (register MCR3, bits 0—3).

SC4[4:1]: S subchannel 4 (register MCR4, bits 0—3).

SC5[4:1]: S subchannel 5 (register MCR5, bits 0—3).

SCK: Serial interface clock.

SDI: Serial interface data input.

SDINN: Sigma delta A/D negative input for U-interface.

SDINP: Sigma delta A/D positive input for U-interface.

SDO: Serial interface data output.

SFECV: S channel far-end code violation (register SIR0, bit 2).

SFECVM: S subchannel far-end code violation mask (register SIR1, bit 2).

SINT: S/T transceiver interrupt (register GIR0, bit 1).

SIR0: S/T-interface interrupt register.

SIR1: S/T-interface interrupt mask register.

SOM: Start of multiframe (register SIR0, bit 0).

SOMM: Start of multiframe mask (register SIR1, bit 0).

SPWRUD: S/T-interface powerdown control (register GR2, bit 1).

SRESET: S/T-interface reset (register GR2, bit 2).

STLED Status LED driver.

STOA: S/T only activation (register GR2, bit 7).

Superframe: Eight U frames grouped together.

Glossary (continued)

SXB1[1:0]: S/T-interface transmit path source for B1 channel (register DFR0, bits 5—4).

SXB2[1:0]: S/T-interface transmit path source for B2 channel (register DFR0, bits 7—6).

SXD: S/T-interface transmit path source for D channel (register DFR1, bit 1).

SXE: S/T-interface D channel echo bit control (register GR2, bit 3).

SYN8K/LBIND/FS: Synchronous 8 kHz clock or loopback indicator, frame strobe.

TDM: Time-division multiplexed.

TDMB1S: TDM bus transmit control for B1 channel from S/T-interface (register DFR1, bit 2).

TDMB1U: TDM bus transmit control for B1 channel from U-interface (register DFR1, bit 5).

TDMB2S: TDM bus transmit control for B2 channel from S/T-interface (register DFR1, bit 3).

TDMB2U: TDM bus transmit control for B2 channel from U-interface (register DFR1, bit 6).

TDMDS: TDM bus transmit control for D channel from S/T-interface (register DFR1, bit 4).

TDMDU: TDM bus transmit control for D channel from U-interface (register DFR1, bit 7).

TDMEN: TDM bus select (register GR2, bit 5).

TDR0: TDM bus timing control register.

TNR: Transmit negative rail for S/T-interface.

TPR: Transmit positive rail for S/T-interface.

TSFINT: Transmit superframe interrupt (register UIR0, bit 5).

TSFINTM: Transmit superframe interrupt mask (register UIR1, bit 5).

U frame: An 18-bit synchronous word.

U2BDLN: Nontransparent 2B+D loopback control (register GR2, bit 4).

U2BDLT: Transparent 2B+D loopback control (register ECR0, bit 6).

UB1LP: U-interface loopback of B1 channel control (register ECR0, bit 4).

UB2LP: U-interface loopback of B2 channel control (register ECR0, bit 5).

UINT: U transceiver interrupt (register GIR0, bit 0).

UIR0: U-interface interrupt register.

UIR1: U-interface Interrupt mask register.

UOA: U-interface only activation, (register CFR1, bit 3).

UXB1[1:0]: U-interface transmit path source for B1 channel (register DFR0, bits 1—0).

UXB2[1:0]: U-interface transmit path source for B2 channel (register DFR0, bits 3—2).

UXD: U-interface transmit path source for D channel (register DFR1, bit 0).

V_{DDA}: Analog power.

V_{DDO}: Crystal oscillator power.

VRCM: Common-mode voltage reference for U-interface circuits.

VRN: Negative voltage reference for U-interface circuits

VRP: Positive voltage reference for U-interface circuits.

X1: Crystal #1.

X2: Crystal #2.

XACT: U transceiver active (register CFR1, bit 1).

XPCY: Transparency (register GR1, bit 5).

Standards Documentation

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.)

American National Standards Institute (ANSI)
11 West 42nd Street
New York, New York 10036

Tel: 212-642-4900
FAX: 212-302-1286

AT&T Publications

AT&T Customer Information Center (CIC)

Tel: 800-432-6600
FAX: 800-566-9568 (In U.S.A.)
FAX: 317-322-6484 (Outside U.S.A.)

Bellcore (U.S.A.)

Bellcore Customer Service
8 Corporate Plaza
Piscataway, New Jersey 08854

Tel: 800-521-CORE (In U.S.A.)
Tel: 908-699-5800
FAX: 212-302-1286

ITU-T

International Telecommunication Union-Telecommunication Sector
Place des Nations
CH 1211
Geneve 20, Switzerland

Tel: 41-22-730-5285
FAX: 41-22-730-5991

ETSI

European Telecommunications Standards Institute
BP 152
F-06561 Valbonne Cedex, France

Tel: 33-92-94-42-00
FAX: 33-93-65-47-16

TTC (Japan)

TTC Standard Publishing Group of the Telecommunications Technology Committee
2nd Floor, Hamamatsucho-Suzuki Building,
1 2-11, Hamamatsu-cho, Minato-ku, Tokyo

Tel: 81-3-3432-1551
FAX: 81-3-3432-1553