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THE I/O INTERCONNECT SOLUTION

PCI 9050-1 Data Book

PCI 9050-1 Data Book

Version 2.0

June 2001

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PREFACE

The information contained in this document is subject to change without notice. Although an effort has been made to keep the information accurate, there may be misleading or even incorrect statements made herein.

SUPPLEMENTAL DOCUMENTATION

The following is a list of additional documentation to provide the reader with further information:

- *PCI Local Bus Specification, Revision 2.1*, June 1, 1995
  PCI Special Interest Group (PCI SIG)
  5440 SW Westgate Drive #217, Portland, OR 97221 USA
  Tel: 800 433-5177 (domestic only) or 503 693-6232, Fax: 503 693-8344, http://www.pcisig.com
- *PCI Local Bus Specification, Revision 2.2*, December 18, 1998
  PCI Special Interest Group (PCI SIG)
  5440 SW Westgate Drive #217, Portland, OR 97221 USA
  Tel: 800 433-5177 (domestic only) or 503 693-6232, Fax: 503 693-8344, http://www.pcisig.com
- *PCI Hot-Plug Specification, Revision 1.0*
  PCI Special Interest Group (PCI SIG)
  5440 SW Westgate Drive #217, Portland, OR 97221 USA
  Tel: 800 433-5177 (domestic only) or 503 693-6232, Fax: 503 693-8344, http://www.pcisig.com

Note: *In this data book, shortened titles are given to the works listed above. The following table lists these abbreviations.*

Supplemental Documentation Abbreviations

Abbreviation	Document
PCI r2.1	*PCI Local Bus Specification, Revision 2.1*
PCI r2.2	*PCI Local Bus Specification, Revision 2.2*
Hot-Plug r1.0	*PCI Hot-Plug Specification, Revision 1.0*

TERMS AND DEFINITIONS

For other unfamiliar terms, refer to the index for text references.

- **Direct Slave**—External PCI Bus Master initiates Data write/read to/from the C or J mode Local Bus.

Data Assignment Conventions

Data Width	PCI 9050-1 Convention
1 byte (8 bits)	Byte
2 bytes (16 bits)	Word
4 bytes (32 bits)	Lword

REVISION HISTORY

Date	Revision	Comments
1996	1.0	Initial release
4/1996	1.01	Information not available.
12/1999	1.02	Applied minor format changes and corrected minor typographical errors. Changed title from “Data Sheet” to “Data Book”. Added 800 phone number. Changed copyright date to 1999. Added primary title page, disclaimer and trademarks, part number, and list of Figures, Tables, and Timing Diagrams. Changed “negate” to “de-assert.” Changed “field” to “bit” in register-related tables. Reorganized timing diagrams (Section 8) by type. Correct Figure 3-1 to state Spaces 0-3 for Local Base Address (Remap) for PCI-to-Local Address Space. Table 4-15, PCIBAR3[3], corrected reference to LAS1BRD. Section 7, resequenced content and added section headings.
6/2001	2.0	Initial release of Version 2.0. Applied updates, including major revisions to “Bus Operation” section and adding two new sections, “Local Chip Selects” and “Interrupts.” Deleted the “Functional Description” section and used its content (including major revisions) to create two new sections—“Reset and Serial EEPROM Initialization” and “Direct Slave Operation.” Edited for readability. PCISR[11] renamed from “Target Abort” to “Signaled Target Abort.” CNTRL[14] renamed from “PCI Read Mode” to “PCI Delayed Read Mode.” Cached Read Mode renamed to Read Ahead Mode (CNTRL[16]). CNTRL[18] renamed from “PCI Write Mode” to “PCI Write Release Bus Mode Enable.” Notation added to timing diagrams and pin descriptions to indicate that in J mode, LAD[1:0] are valid address bits during the Address phase. Added pull-up resistor and EEPROM requirements to Section 8.1.

PLX TECHNOLOGY
THE I/O INTERCONNECT SOLUTION

PCI 9050-1

June 2001
Version 2.0

PCI Bus Target Interface Chip
for Low Cost Adapters

1 INTRODUCTION

1.1 COMPANY AND PRODUCT BACKGROUND

PLX Technology, Inc., is the leading supplier of high-speed, interconnect silicon and software solutions for the networking and communications industry. These include high-speed silicon, reference design tools that minimize design risk, and software for managing data throughout the PCI Bus, as well as third-party development tool support through the PLX Partner Program, further extending our complete solution.

The PLX solution enables hardware designers and software developers to maximize system input/output (I/O), lower development costs, minimize system design risk, and accelerate time to market.

PLX PCI I/O Accelerator chips and I/O Processor devices are designed in a wide variety of embedded PCI communication systems, including switches, routers, media gateways, base stations, access multiplexors, and remote access concentrators. PLX customers include many of the leading communications equipment companies, including 3Com, Cisco Systems, Compaq Computer, Ericsson, Hewlett-Packard, Intel, IBM, Lucent Technologies, Marconi, Nortel Networks, and Siemens.

Founded in 1986, PLX has developed products based on the PCI industry standard since 1994.

PLX is publicly-traded (NASDAQ: PLXT) and headquartered in Sunnyvale, California, USA, with operations in the United Kingdom, Japan, and China.

1.2 GENERAL DESCRIPTION

The PCI 9050-1 provides a compact high performance PCI Bus Slave interface for adapter boards. The PCI 9050-1 is designed to connect a wide variety of Local Bus designs to the PCI Bus and allow relatively slow Local Bus designs to achieve 132 MB/s burst transfers on the PCI Bus.

The PCI 9050-1 can be programmed to connect directly to the non-multiplexed (C mode) or multiplexed (J mode) 8, 16, or 32-bit Local Bus. The 8-and 16-bit modes allow easy conversion of ISA designs to PCI. (Refer to Figure 1-1.)

The PCI 9050-1 contains Read and Write FIFOs to speed match the 32-bit wide, 33 MHz PCI Bus to a Local Bus, which may be narrower or slower. Up to five local address spaces and four Chip Select outputs are supported.

1.3 PCI 9050-1 MAJOR FEATURES

***PCI Local Bus Specification, Revision 2.1*-Compliant.** The PCI 9050-1 is compliant with *PCI r2.1*, supporting low cost slave adapters. This allows simple conversion of ISA adapters to PCI.

Direct Slave (Target) Data Transfer Mode. The PCI 9050-1 supports Burst Memory-Mapped and single I/O-mapped accesses from the PCI-to-Local Bus. Read and Write FIFOs enable high-performance bursting on the Local and PCI Buses. The PCI Bus is always bursting; however, the Local Bus can be set to bursting or continuous single cycle.

Interrupt Generator. The PCI 9050-1 can generate a PCI interrupt from two Local Bus interrupt inputs, or by software writing to an internal register bit.

Clock. The PCI 9050-1 Local Bus interface runs from a local TTL clock and generates the necessary internal clocks. This clock runs asynchronously to the PCI clock, allowing the Local Bus to run at an independent rate from the PCI clock. The buffered PCI Bus clock (BCLKO) may be connected to the Local Bus clock (LCLK).

Programmable Local Bus Configurations. The PCI 9050-1 supports 8-, 16-, or 32-bit Local Buses, which may be non-multiplexed (C mode) or multiplexed (J mode).

In C mode, the PCI 9050-1 has four byte enables (LBE[3:0]#), 26 address lines (LA[27:2]), and 32, 16, or 8 data lines (LAD[31:0]).

In J mode, the PCI 9050-1 has four byte enables (LBE[3:0]#), and 28 address lines (LAD[27:0]), multiplexed with 32, 16, or 8 data lines (LAD[31:0]).

Read Ahead Mode. The PCI PCI 9050-1 supports Read Ahead mode, where prefetched data can be read from the PCI 9050-1 internal FIFO instead of the Local Bus. The address must be subsequent to the previous address and be 32-bit aligned (next address = current address + 4).

Bus Drivers. All control, address, and data signals generated by the PCI 9050-1 directly drive the PCI and Local buses, without external drivers.

Serial EEPROM Interface. The PCI 9050-1 contains a serial EEPROM interface used to load configuration information. This is useful for loading information unique to a particular adapter (*such as* Vendor ID and chip selects).

Four Local Chip Selects. The PCI 9050-1 provides up to four local chip selects. The base address and range of each chip select are independently programmable from the serial EEPROM or host.

Five Local Address Spaces. The base address and range of each local address space are independently programmable from the serial EEPROM or host.

Big/Little Endian Byte Swapping. The PCI 9050-1 supports Big and Little Endian byte ordering. The PCI 9050-1 also supports Big Endian Byte Lane mode to redirect the current word or byte lane during 16- or 8-bit Local Bus operation.

Read/Write Strobe Delay and Write Cycle Hold. The Read and Write (RD# and WR#) signals can be delayed from the beginning of the cycle for legacy interfaces (*such as* an ISA Bus). Write Cycle Hold allows the Data phase to be extended beyond WR# strobe de-assertion, to increase the time Write data remains valid on the Local Bus to accommodate slower Local Bus devices.

Local Bus Wait States. In addition to the LRDYi# (local ready input) handshake signal for variable wait state generation, the PCI 9050-1 has an internal wait state generator (Read and Write address-to-data, data-to-data, and data-to-address).

Programmable Prefetch Counter. The Local Bus Prefetch counter can be programmed to 0 (no prefetch), 4, 8, 16, or Continuous (prefetch counter turned off) Prefetch mode. The prefetched data can be used as cached data if a consecutive address is used (must be Lword-aligned).

Delayed Read Mode. The PCI 9050-1 supports *PCI r2.1* Delayed Read with:

- PCI Read with Write Flush mode
- PCI Read No Flush mode
- PCI Read No Write mode
- PCI Write Release Bus mode

PCI Read/Write Retry Delay Timer. The PCI 9050-1 has a programmable Direct Slave (PCI Target) Retry Delay timer, which, when expired, generates a RETRY to the PCI Bus.

PCI LOCK Mechanism. The PCI 9050-1 supports Direct Slave LOCK sequences. A PCI Master can obtain exclusive access to the PCI 9050-1 device by locking to the PCI 9050-1.

PCI Bus Transfers up to 132 MB/s.

Low-Power CMOS in 160-pin Plastic QFP Package (PQFP).

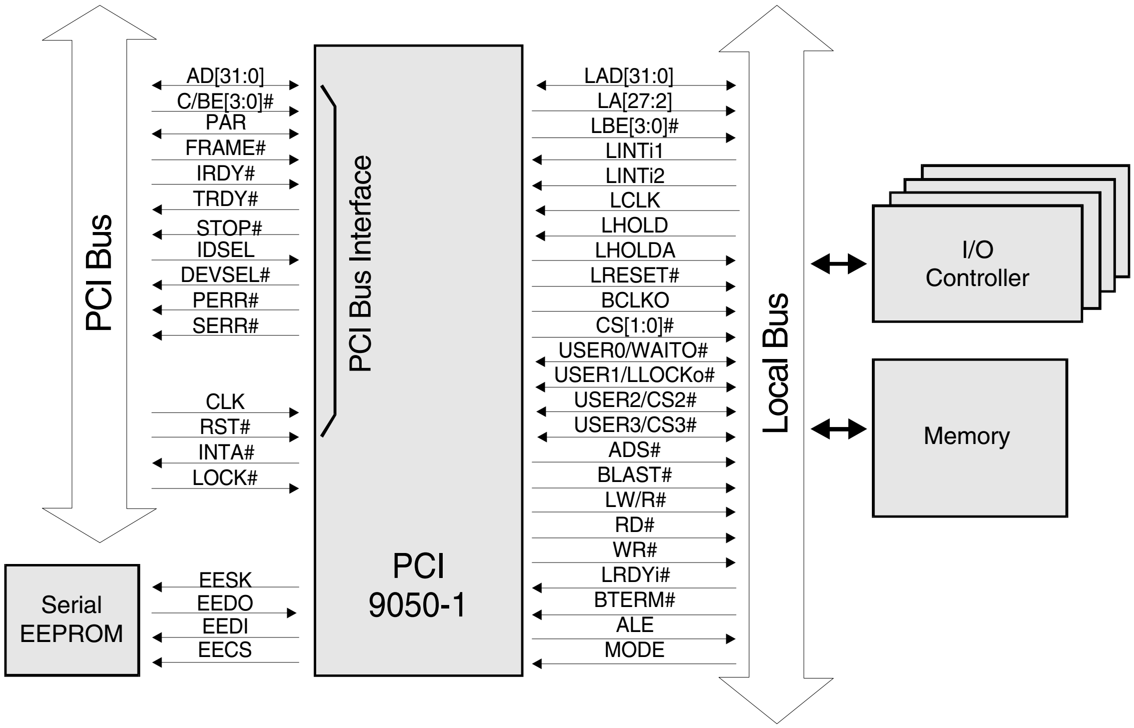


Figure 1-1. PCI 9050-1 Block Diagram

2 BUS OPERATION

This section discusses PCI and Local Bus operation.

2.1 PCI BUS

2.1.1 PCI Bus Interface and Bus Cycles

The PCI 9050-1 is compliant with *PCI r2.1*. Refer to it for specific PCI Bus functions as a Direct Slave Interface chip.

2.1.1.1 PCI Target (Direct Slave) Command Codes

As a Target, the PCI 9050-1 allows access to the PCI 9050-1 internal registers and the Local Bus, using the commands listed in Table 2-1.

All Read or Write accesses to the PCI 9050-1 can be Byte, Word, or Lword (32-bit data). All Memory commands are aliased to basic Memory commands. All PCI 9050-1 I/O accesses are decoded to an Lword boundary.

Table 2-1. Direct Slave Command Codes

Command Type	Code (C/BE[3:0]#)
I/O Read	0010 (2h)
I/O Write	0011 (3h)
Memory Read	0110 (6h)
Memory Write	0111 (7h)
Configuration Read	1010 (Ah)
Configuration Write	1011 (Bh)
Memory Read Multiple	1100 (Ch)
Memory Read Line	1110 (Eh)
Memory Write and Invalidate	1111 (Fh)

2.1.1.2 Wait States—PCI Bus

The PCI Bus Master throttles IRDY# and the PCI Bus Slave throttles TRDY# to insert PCI Bus wait state(s).

2.1.1.3 PCI Bus Little Endian Mode

The PCI Bus is a Little Endian Bus (*that is*, the address is invariant and data is Lword-aligned to the lowermost byte lane).

Table 2-2. PCI Bus Little Endian Byte Lanes

Byte Number	Byte Lane
0	AD[7:0]
1	AD[15:8]
2	AD[23:16]
3	AD[31:24]

2.1.1.4 PCI Prefetchable Memory Mapping

PCI Memory Address spaces assigned to the PCI 9050-1 for its Local Address spaces can be mapped as either prefetchable or non-prefetchable memory within the system. Configuration software (PCI BIOS) checks the PCI 9050-1 PCI Configuration register Prefetchable bit(s) (PCIBAR0[3], PCIBAR1[3], PCIBAR2[3], PCIBAR3[3], PCIBAR4[3], and/or PCIBAR5[3]) to determine whether the Target memory is prefetchable. This value of this bit(s) is set according to Local Configuration register settings (as configured by serial EEPROM values) at boot time.

When set to 1, the Prefetchable bit(s) signals that the Memory space can operate under a prefetching protocol, for improved performance. If a PCI Master initiates a read to a location that is mapped in the prefetchable address range, a Host-to-PCI or PCI-to-PCI bridge is permitted to extend the Read Transaction burst length in anticipation of the Master consuming the additional data. The Prefetchable bit(s) should normally be set if all the following conditions are met:

- Multiple Memory reads of an Lword result in the same data
- If Read data is discarded by the PCI Master, no negative side effects occur
- Address space is not mapped as I/O.
- Local Target must be able to operate with byte merging

Byte merging is an optional function of a Host-to-PCI or PCI-to-PCI bridge in which bytes or combinations of bytes written in any order by multiple individual Memory Write cycles to one Lword address can be merged within the bridge's Posted Memory Write buffer into a single Lword Write cycle. Byte merging is possible when any of the bytes to be merged are written only once, and the Prefetchable bit(s) is set to 1.

The Prefetchable bit(s) setting has no effect on prefetching initiated by the PCI 9050-1. PCI 9050-1 prefetching is disabled, by default, in the Local Configuration registers, and should be enabled to support highest performance with Direct Slave burst reads and Read Ahead mode. (Refer to Section 4.2.1.)

2.1.1.5 PCI Target (Direct Slave) Accesses to an 8- or 16-Bit Local Bus Device

Direct PCI access to an 8- or 16-bit Local Bus device results in the PCI Bus Lword being broken into multiple Local Bus transfers. For each 8-bit transfer, byte enables are encoded to provide Local Address bits LA1 and LA0. For each 16-bit transfer, byte enables are encoded to provide BLE#, BHE# and LA1.

Do not use direct PCI access to an 8-bit bus with nonadjacent byte enables in a PCI Lword. Nonadjacent byte enables cause an incorrect LA[1:0] address sequence when bursting to memory. Therefore, for each Lword written to an 8-bit bus, the PCI 9050-1 does not write data after the first gap. Direct PCI accesses to an 8-bit bus with nonadjacent byte enables are not terminated with a Target Abort. Therefore, for nonadjacent bytes (illegal byte enables), the PCI Master must perform single cycles.

2.2 LOCAL BUS

2.2.1 Introduction

The Local Bus provides a data path between the PCI Bus and non-PCI devices, including Memory devices and peripherals. The Local Bus is a 32-bit Non-Multiplexed (C mode) or Multiplexed (J mode) mode bus, with Bus Memory regions that can be programmed for 8-, 16-, or 32-bit widths.

The PCI 9050-1 is the Local Bus Master. The PCI 9050-1 can transfer data between the Local Bus, internal registers and FIFOs. Burst lengths are not limited. The bus width depends upon the Local Address Space register setting. There are four address spaces and one default space (the Expansion ROM that can be used as another address space). Each space contains a set of Configuration registers that determine all Local Bus characteristics when that space is accessed.

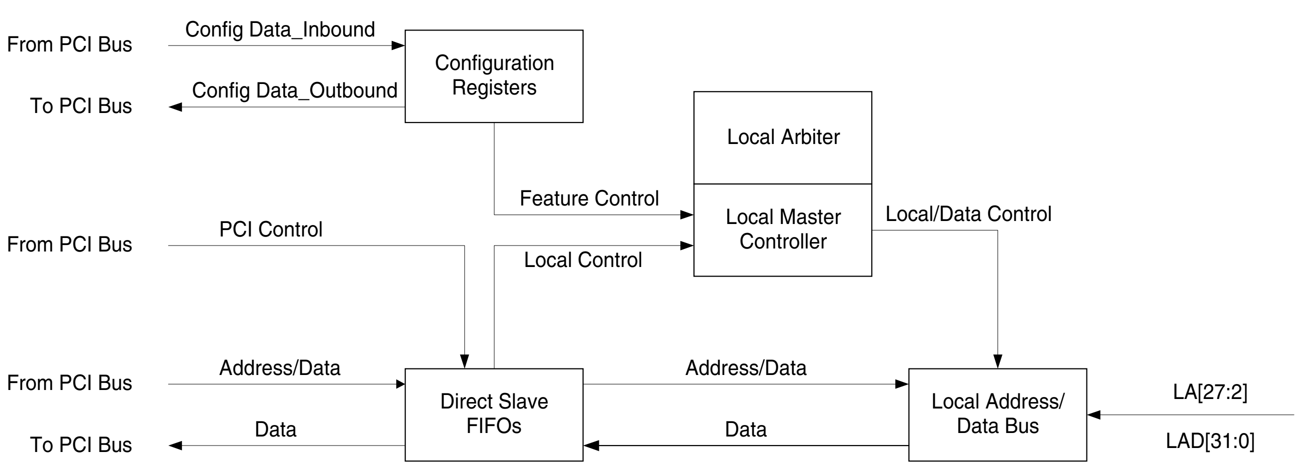


Figure 2-1. Local Bus Block Diagram

2.2.1.1 Transactions

Four types of transactions can occur on a Local Bus:

- Read
- Write
- Read Burst
- Write Burst

A Bus access is a transaction which is bounded by the assertion of ADS# at the beginning and de-assertion of BLAST# at the end. A Bus access consists of an address cycle followed by one or more data transfers. During each clock cycle of an access, the Local Bus is in one of four basic states defined in Section 2.2.1.2. A clock cycle consists of one Local Bus clock period.

2.2.1.2 Basic Bus States

The four basic bus states are *idle*, *address*, *data/wait*, and *recovery*. Once the Local Bus Master owns the Bus and needs to start a Bus access, the address state is entered, ADS# or ALE is asserted, and a valid address is presented on the Address/Data Bus. Data is then transferred while in a data/wait state. LRDYi# or the internal wait state generator is used to insert wait states. BLAST# is asserted during the last data/wait state to signify the last transfer of the access. In J mode only, after all data is transferred, the Bus enters the recovery state to allow the Bus devices to recover. The Bus then enters the idle state and waits for another access.

2.2.2 Local Signals

The key Local Bus control signals shown in most timing diagram examples are as follows:

- ADS# or ALE indicates the start of an access
- LRDYi#, WAITO#, and BTERM# are used to insert wait states and terminate Burst cycles during Data transfers
- LW/R#, direction of Data transfer
- BLAST#, BTERM# indicate the end of an access

The key data signals are:

- LA Address Bus
- LAD Address, Data Bus
- LBE# Local byte enables, indicating valid byte lanes

2.2.3 Local Bus Signals

Signal usage varies upon application. There are four groups of Local Bus signals:

- Clock
- Address/Data
- Control/Status
- Arbitration

2.2.3.1 Clock

LCLK, the Local Bus clock, operates at frequencies up to 40 MHz, and is asynchronous to the PCI Bus clock. Most Local Bus signals are driven and sampled on the rising edge of LCLK. Setup and hold times, with respect to LCLK, must be observed. (Refer to Section 9.2, “Local Inputs,” on page 9-2 for setup and hold timing requirements.)

2.2.3.2 Address/Data

2.2.3.2.1 LA[27:2]

LA[27:2] contains the transfer word address.

2.2.3.2.2 LAD[31:0]

In C mode, the LAD[31:0] Bus is a 32-bit non-multiplexed data bus. During Data phases, LAD[31:0], LAD[15:0], or LAD[7:0] contain transfer data for a 32-, 16-, or 8-bit bus, respectively. If the bus is 8 or 16 bits wide, data supplied by the PCI 9050-1 is replicated across the entire 32-bit wide bus.

In J mode, the LAD[31:0] Bus is a 32-bit Multiplexed Address/Data Bus. During an Address phase, LAD[27:0] contains the transfer word address. LAD[1:0] have the same address value as LBE[1:0]#, for use with 8- or 16-bit bus width addressing.

Note: *Dedicated address pins are available.*

During Data phases, LAD[31:0], LAD[15:0], or LAD[7:0] contain transfer data for a 32-, 16-, or 8-bit bus, respectively. If the bus is 8 or 16 bits wide, data supplied by the PCI 9050-1 is replicated across the entire 32-bit wide bus.

2.2.3.3 Control/Status

The control/status signals control the address latches and flow of data across the Local Bus.

2.2.3.3.1 ADS#, ALE

A Local Bus access starts when ADS# (address strobe) is asserted during an address state by the PCI 9050-1 as the Local Bus Master. ALE is used to strobe the LA/LAD Bus into an external address latch. Refer to Figure 9-3 and Table 9-7 on page 9-4 for ALE timing specifications.

2.2.3.3.2 LBE[3:0]#

During an Address phase, the LBE[3:0]# byte enables denote which byte lanes are being used during access of a 32-bit bus. They remain asserted until the end of the Data transfer.

2.2.3.3.3 LRDYi#

The LRDYi# input pin has a corresponding Enable bit in the Bus Region Descriptor register for each Local address space. If LRDYi# is enabled, this indicates that Write data is being accepted or Read data is being provided by the Bus Slave. If a Bus Slave needs to insert wait states, it can de-assert LRDYi# until it is ready to accept or provide data. If LRDYi# is disabled, then the Local Bus transfer length can be determined by internal wait state generators. LRDYi# is not sampled until address-to-data or data-to-data wait states have expired. (Refer to Table 2-3.)

When BTERM# input is enabled for a Local Address space in the corresponding Bus Region Descriptor register, BTERM# can be used to complete an access in place of LRDYi#. When BTERM# is enabled and asserted, LRDYi# input is ignored. Further information regarding BTERM# is provided in Section 2.2.4.3.

2.2.3.3.4 LW/R#

During an Address phase, LW/R# is driven to a valid state, and signifies the data transfer direction. Because the PCI 9050-1 is the Local Bus Master, LW/R# is driven high when the PCI 9050-1 is writing data to the Local Bus, and low when it is reading the bus.

2.2.3.3.5 WAITO#

WAITO# is an output that provides status of the internal wait state generators. It is asserted while internal wait states are being inserted. LRDYi# input is not sampled until WAITO# is de-asserted.

2.2.3.3.6 LLOCKo#

When the PCI 9050-1 owns the Local Bus, LLOCKo# is asserted to indicate that an atomic operation for a Direct Slave access may require multiple transactions to complete. LLOCKo# is asserted during the Address phase of the first transaction of the atomic operation, and de-asserted one clock after the last transaction of the atomic operation completes. If enabled, the Local Bus arbiter does not grant the Bus to another Master until the atomic operation is complete.

2.2.3.3.7 WR#

WR# is a general purpose write output strobe. The timing is controlled by the current Bus Region Descriptor register. The WR# strobe is asserted during the entire Data transfer. WR# is normally asserted during NWAD wait states, unless Write Strobe Delay clocks are programmed in bits [29:28]. WR# remains asserted throughout Burst and NWDD wait states. The LAD data bus hold time can be extended beyond WR# de-assertion if Write Cycle Hold clocks are programmed in bits [31:30].

Table 2-3. LRDYi# Data Transfers, with PCI 9050-1 as Master Device

Slave Device	LRDYi#		Description
	Input Enable	Signal	
Address Spaces	0	Ignored	LRDYi# is not sampled by the PCI 9050-1. Data transfers determined by the internal wait state generator. LRDYi# is ignored and the Data transfer occurs after the internal wait state counter expires.
	1	Sampled	LRDYi# is sampled by the PCI 9050-1. Data transfers are determined by an external device, which asserts LRDYi# to indicate a Data transfer is occurring. LRDYi# is not sampled until address-to-data or data-to-data wait states have expired.

2.2.3.3.8 RD#

RD# is a general purpose read output strobe. The timing is controlled by the current Bus Region Descriptor register. The RD# strobe is asserted during the entire Data transfer. Normally, it is also asserted during NRAD wait states, unless Read Strobe Delay clocks are programmed in bits [27:26]. RD# remains asserted throughout Burst and NRDD wait states.

2.2.3.3.9 LHOLD

LHOLD is asserted by a Local Bus Master to request Local Bus use. The PCI 9050-1 can be made sole master of the Local Bus by pulling LHOLD low or leaving LHOLD unterminated (internal pull-down resistor).

2.2.3.3.10 LHOLDA

LHOLDA is asserted by the PCI 9050-1 to grant Local Bus control to a Local Bus Master. When the PCI 9050-1 requires the Local Bus, it signals a preempt by de-asserting LHOLDA.

2.2.4 Local Bus Interface and Bus Cycles

The PCI 9050-1 is the Local Bus Master. The PCI 9050-1 interfaces a PCI Host Bus to two Local Bus types, as listed in Table 2-4. It operates in one of two modes, selected through the MODE pin, corresponding to the bus type.

Notes: *No PCI Initiator (Direct Master) capability.*

Internal registers are not readable/writable from the Local Bus. The internal registers are accessible from the Host CPU on the PCI Bus or from the serial EEPROM.

Table 2-4. Local Bus Types

MODE Pin	Mode	Bus Type
0	C	32-Bit Non-Multiplexed
1	J	32-Bit Multiplexed

2.2.4.1 Local Bus Arbitration

The PCI 9050-1 is the Local Bus Master. When the PCI Bus initiates a new transfer request, the PCI 9050-1 takes control of the Local Bus. Another device can gain control of the Local Bus by asserting LHOLD. If the PCI 9050-1 has no cycles to run, it asserts LHOLDA, transferring control to the external Master. If the PCI 9050-1 requires the Local Bus before the external Master completes, LHOLDA is de-asserted (preempt condition).

LHOLD can be left unterminated to provide permanent Local Bus ownership to the PCI 9050-1.

2.2.4.2 Wait State Control

The following figure illustrates wait state control.

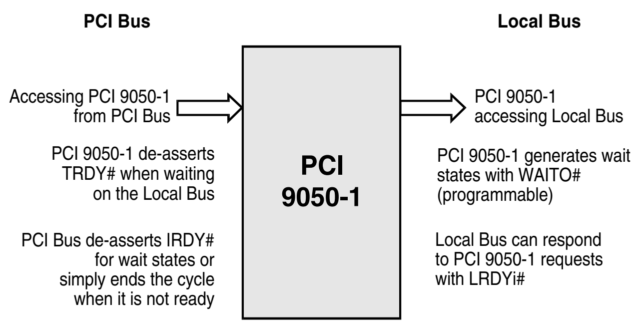


Figure 2-2. Wait States

Note: *The figure represents a sequence of Bus cycles.*

If LRDYi# mode is disabled, the external LRDYi# input signal has no effect on wait states for a Local access. Wait states between Data cycles are inserted internally by a wait state counter. The wait state counter is initialized with its Configuration register value at the start of each data access.

If LRDYi# mode is enabled and the internal wait state counter is zero (default value), the LRDYi# input controls the number of additional wait states.

If LRDYi# mode is enabled and the internal wait state counter is programmed to a non-zero value, LRDYi# has no effect until the wait state counter reaches 0. When it reaches 0, the LRDYi# input controls the number of additional wait states.

If the internal wait state counter is programmed to a non-zero value and BTERM# is enabled, BTERM# input is not sampled until the wait state counter reaches 0.

2.2.4.2.1 Wait States—Local Bus

In Direct Slave mode, the PCI 9050-1 as a Local Bus Master signals internal wait states with WAITO#. A Local Bus device can insert external wait states by delaying LRDYi# input assertion. (Refer to Figure 2-3 and Figure 2-4.)

The following Internal Wait State bit(s) can be used to program the number of internal wait states between the first address-to-data state (and subsequent data-to-data in Burst mode):

- LAS0BRD[21:15, 12:6],
- LAS1BRD1[21:15, 12:6],
- LAS2BRD[21:15, 12:6], and/or
- LAS3BRD[21:15, 12:6]

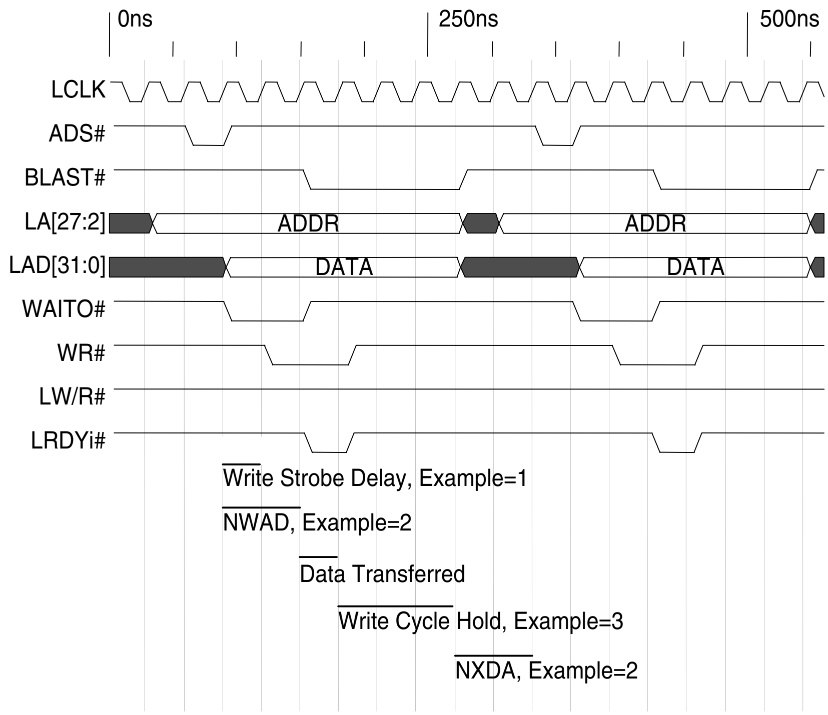


Figure 2-3. PCI 9050-1 Single Cycle Write

Note: *NWDD is relevant only in a Burst cycle, where it determines the wait state between successive Data cycles.*

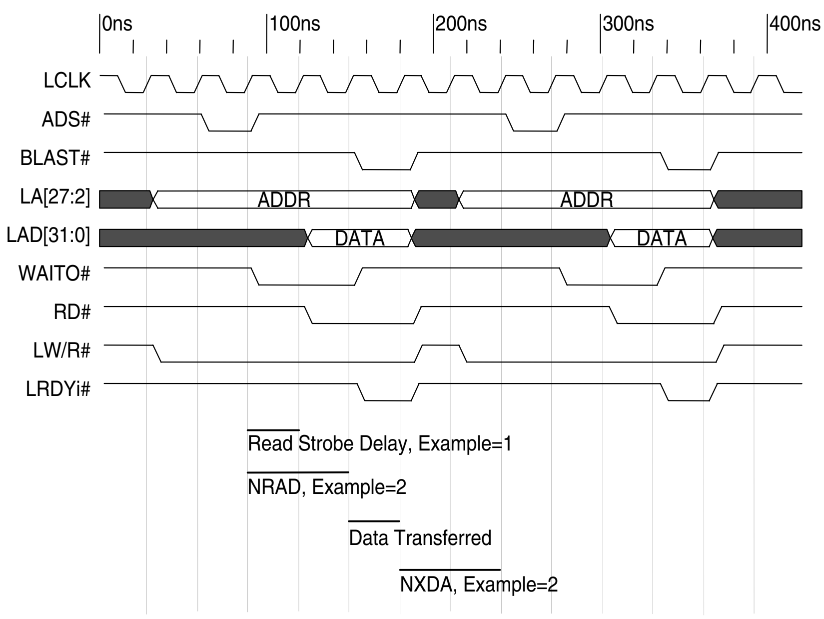


Figure 2-4. PCI 9050-1 Single Cycle Read

Note: *NRDD is relevant only in a Burst cycle, where it determines the wait state between successive Data cycles.*

2.2.4.3 Burst Mode and Continuous Burst Mode (Bterm "Burst Terminate" Mode)

Note: *In the following sections, Bterm refers to the PCI 9050-1 internal register bit and BTERM# refers to the PCI 9050-1 external signal.*

2.2.4.3.1 Burst and Bterm Modes

As an input, BTERM# is asserted by external logic. It instructs the PCI 9050-1 to break up a Burst cycle.

Table 2-5. Burst and Bterm on the Local Bus

Mode	Burst	Bterm	Result
Single Cycle	0	0	One ADS# per data (default)
	0	1	One ADS# per data
Burst-4 Lword	1	0	One ADS# per four data
Continuous Burst	1	1	One ADS# per BTERM# (refer to Section 2.2.4.3.2.1)

On the Local Bus, BLAST# and BTERM# perform the following:

- If the Burst Mode bit is enabled, but the Bterm Mode bit is disabled, the PCI 9050-1 bursts (up to four Data phases). BLAST# is asserted at the beginning of the fourth Lword Data phase (LA[3:2]=11) and a new ADS# is asserted at the first Lword (LA[3:2]=00) of the next burst.
- If BTERM# is enabled and asserted, the PCI 9050-1 terminates the Burst cycle at the end of the current Data phase without generating BLAST#. The PCI 9050-1 generates a new burst transfer, starting with a new ADS#, terminating it normally using BLAST#.
- The BTERM# input is valid only when the PCI 9050-1 is performing a Direct Slave transaction.
- BTERM# is used to indicate a Memory access is crossing a page boundary or requires a new Address cycle.
- If the internal wait state counter is programmed to a non-zero value and BTERM# is enabled, the BTERM# input is not sampled until the wait state counter reaches 0.
- BTERM# always overrides LRDYi#, even if both signals are asserted. BTERM# executes the ongoing transaction and causes the PCI 9050-1 to initiate a new Address/Data cycle for Burst transactions.

Note: *If the Bterm Mode bit is disabled, the PCI 9050-1 performs the following:*

- ***32-bit Local Bus****—Bursts up to four Lwords*
- ***16-bit Local Bus****—Bursts up to two Lwords*
- ***8-bit Local Bus****—Bursts up to one Lword*

In every case, it performs four data beats.

2.2.4.3.2 Burst-4 Lword Mode

If the Burst mode bit is enabled and the Bterm mode bit is disabled, bursting can start on any Lword boundary and continue up to a 16-byte address boundary. After data up to the boundary is transferred, the PCI 9050-1 asserts a new Address cycle (ADS#).

Table 2-6. Burst-4 Lword Mode

Bus Width	Burst
32 bit	Four Lwords or up to a quad-Lword boundary (LA[3:2] = 11)
16 bit	Four words or up to a quad-word boundary (LA[2:1] = 11)
8 bit	Four bytes or up to a quad-byte boundary (LA[1:0] = 11)

2.2.4.3.2.1 Continuous Burst Mode (Bterm "Burst Terminate" Mode)

If both the Burst and Bterm Mode bits are enabled, the PCI 9050-1 can operate beyond the Burst-4 Lword mode.

Bterm mode enables the PCI 9050-1 to perform long bursts to devices that can accept bursts of longer than four Lwords. The PCI 9050-1 asserts one Address cycle and continues to burst data. If a device requires a new Address cycle (ADS#), it can assert the BTERM# input to cause the PCI 9050-1 to assert a new Address cycle. The BTERM# input acknowledges the current Data transfer (replacing LRDYi#) and requests that a new Address cycle be asserted (ADS#). The new address is for the next Data transfer. If the Bterm mode bit is enabled and the BTERM# signal is asserted, the PCI 9050-1 asserts BLAST# only if its Read FIFO is full, its Write FIFO is empty, or a transfer is complete.

2.2.4.3.3 Partial Lword Accesses

Partial Lword accesses are Lword accesses in which not all byte enables are asserted.

Table 2-7. Direct Slave Single and Burst Reads

Bus	Direct Slave Single Reads	Direct Slave Burst Reads
32-, 16-, or 8-bit Local Bus	Passes the byte enables	Ignores the byte enables and all 32-bit data is passed

Burst Start addresses can be any Lword boundary. If the Burst Start address in a Direct Slave transfer is not aligned to an Lword boundary, the PCI 9050-1 first performs a single cycle. It then starts to burst on the Lword boundary.

2.2.4.4 Recovery States

In C mode, the PCI 9050-1 uses the NXDA (data-to-address wait states) value in the Bus Region Descriptor register to determine the number of recovery states to insert between the last data transfer and next address cycle. This value can be programmed between 0 and 3 clock cycles (default value is 0).

In J mode, the PCI 9050-1 inserts a minimum of one recovery state between the last data transfer and the next address cycle. Add recovery states by programming values greater than one into the NXDA bits of the Bus Region Descriptor register.

Note: *The PCI 9050-1 does not support the i960J function that uses the LRDYi# input to add recovery states. No additional recovery states are added if the LRDYi# input remains asserted during the last Data cycle.*

2.2.4.5 Local Bus Read Accesses

For all single cycle Local Bus Read accesses, the PCI 9050-1 reads only bytes corresponding to byte enables requested by a PCI Master. For all Burst Read cycles, the PCI 9050-1 can be programmed to:

- Perform Direct Slave Delayed Reads
- Perform Direct Slave Read Ahead
- Generate internal wait states
- Enable external wait control (LRDYi# input)
- Enable type of Burst mode to perform

2.2.4.6 Local Bus Write Accesses

For Local Bus writes, only bytes specified by a PCI Bus Master are written. For all Burst Write cycles, the PCI 9050-1 can be programmed to:

- Generate internal wait states
- Enable external wait control (LRDYi# input)

2.2.5 Local Bus Big/Little Endian Mode

The PCI 9050-1 Local Bus can be independently programmed to operate in Little or Big Endian mode for each of the following transfer types:

- Direct Slave accesses to Local Address Space 0
- Direct Slave accesses to Local Address Space 1
- Direct Slave accesses to Local Address Space 2
- Direct Slave accesses to Local Address Space 3
- Direct Slave accesses to Expansion ROM

Notes: *The PCI Bus is always Little Endian.*
Only byte lanes are swapped, not individual bits.

The PCI 9050-1 Local Bus can be programmed to operate in Big or Little Endian mode, as shown in Table 2-8.

Table 2-8. Big/Little Endian Byte Number and Lane Cross-Reference

Byte Number		
Big Endian	Little Endian	Byte Lane
3	0	LAD[7:0]
2	1	LAD[15:8]
1	2	LAD[23:16]
0	3	LAD[31:24]

Big/Little Endian Control bits are as follows:

- LAS0BRD[24]—Space 0
- LAS1BRD[24]—Space 1
- LAS2BRD[24]—Space 2
- LAS3BRD[24]—Space 3
- EROMBRD[24]—Expansion ROM

In Big Endian mode, the PCI 9050-1 transposes data byte lanes. Data is transferred as listed in Table 2-9 through Table 2-13.

2.2.5.1 32-Bit Local Bus—Big Endian Mode

Data is Lword-aligned to the uppermost byte lane (Address Invariance).

Table 2-9. Upper Lword Lane Transfer—32-Bit Local Bus

Burst Order	Byte Lane
First Transfer	PCI Byte 0 appears on Local Data [31:24]
	PCI Byte 1 appears on Local Data [23:16]
	PCI Byte 2 appears on Local Data [15:8]
	PCI Byte 3 appears on Local Data [7:0]

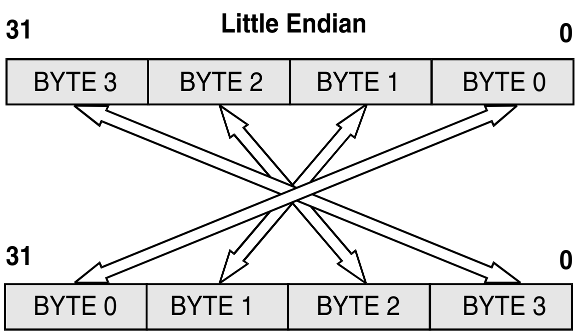


Figure 2-5. Big/Little Endian—32-Bit Local Bus

2.2.5.2 16-Bit Local Bus—Big Endian Mode

For a 16-bit Local Bus, the PCI 9050-1 can be programmed to use upper or lower word lanes.

Table 2-10. Upper Word Lane Transfer—16-Bit Local Bus

Burst Order	Byte Lane
First Transfer	Byte 0 appears on Local Data [31:24]
	Byte 1 appears on Local Data [23:16]
Second Transfer	Byte 2 appears on Local Data [31:24]
	Byte 3 appears on Local Data [23:16]

Table 2-11. Lower Word Lane Transfer—16-Bit Local Bus

Burst Order	Byte Lane
First Transfer	Byte 0 appears on Local Data [15:8]
	Byte 1 appears on Local Data [7:0]
Second Transfer	Byte 2 appears on Local Data [15:8]
	Byte 3 appears on Local Data [7:0]

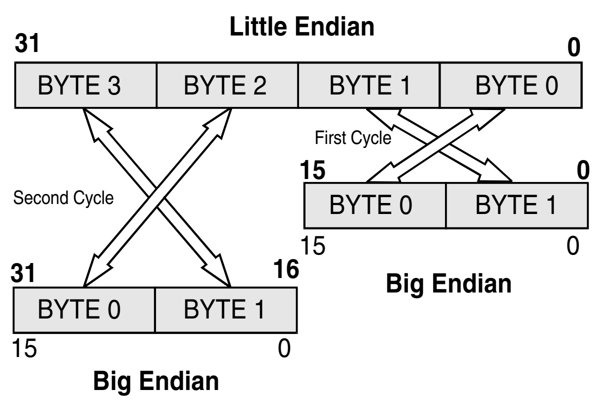


Figure 2-6. Big/Little Endian—16-Bit Local Bus

2.2.5.3 8-Bit Local Bus—Big Endian Mode

For an 8-bit Local Bus, the PCI 9050-1 can be programmed to use upper or lower byte lanes.

Table 2-12. Upper Byte Lane Transfer—8-Bit Local Bus

Burst Order	Byte Lane
First transfer	Byte 0 appears on Local Data [31:24]
Second transfer	Byte 1 appears on Local Data [31:24]
Third transfer	Byte 2 appears on Local Data [31:24]
Fourth transfer	Byte 3 appears on Local Data [31:24]

Table 2-13. Lower Byte Lane Transfer—8-Bit Local Bus

Burst Order	Byte Lane
First Transfer	Byte 0 appears on Local Data [7:0]
Second Transfer	Byte 1 appears on Local Data [7:0]
Third Transfer	Byte 2 appears on Local Data [7:0]
Fourth Transfer	Byte 3 appears on Local Data [7:0]

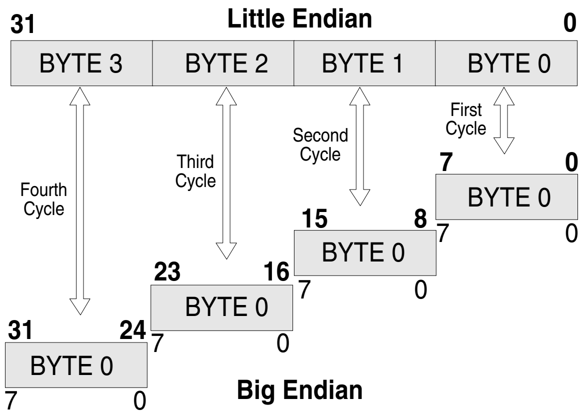


Figure 2-7. Big/Little Endian—8-Bit Local Bus

3 RESET AND SERIAL EEPROM INITIALIZATION

3.1 INITIALIZATION

During power-on, the PCI RST# signal resets the default values of the PCI 9050-1 internal registers. In return, the PCI 9050-1 outputs the local LRESET# signal and checks for a serial EEPROM. If a serial EEPROM exists, and the first 48 bits are not all ones (1), the PCI 9050-1 loads the internal registers from the serial EEPROM. Otherwise, default values are used. The PCI 9050-1 Configuration registers can be written only by the optional serial EEPROM or PCI Host processor. During serial EEPROM initialization, the PCI 9050-1 response to Direct Slave accesses is RETRYs.

3.2 RESET

3.2.1 PCI Bus Input RST#

PCI Bus RST# input assertion causes all PCI Bus outputs to float, resets the entire PCI 9050-1, asserts local reset output LRESET#, and floats all other Local Bus output and I/O pins.

3.2.2 Software Reset

A PCI Host can set the software reset bit in the Miscellaneous Control register (CNTRL) to reset the PCI 9050-1, assert LRESET# output, and float all other Local Bus output and I/O pins. The PCI and Local Configuration registers contents are not reset. When the Software Reset bit is set, the PCI 9050-1 responds only to Configuration register accesses, and not to Local Bus accesses. The PCI 9050-1 remains in this reset condition until the PCI Host clears the Software Reset bit.

3.2.3 Local Bus Output LRESET#

LRESET# is asserted when the PCI Bus RST# input is asserted (4 to 10 ns delay) or the Software Reset bit is set (CNTRL[30]=1).

3.3 SERIAL EEPROM

After reset, the PCI 9050-1 attempts to read the serial EEPROM to determine its presence. An active low start bit indicates the serial EEPROM is present. (Refer to the manufacturer's data sheet for the particular serial EEPROM being used.) If the first 48 bits in the serial EEPROM are not all ones (1), then the PCI 9050-1 assumes the device is not blank, and continues reading.

For blank serial EEPROM conditions, the PCI 9050-1 reverts to the default values (refer to Table 3-1). When the Serial EEPROM Valid bit is set to 1 (CNTRL[28]=1), if programmed, real or random data is detected in the serial EEPROM.

A serial data start bit set to 1 indicates that a serial EEPROM is not present. For missing serial EEPROM conditions, the PCI 9050-1 stops the serial EEPROM load and reverts to the default values. If no serial EEPROM is present, pull EEDO low to prevent false detection of a low Start bit.

However, the PCI 9050-1 requires a programmed serial EEPROM to set the PCI Direct Slave Retry Delay Clock (CNTRL[22:19]) value to 3h or greater, or to enable PCI Delayed Read mode (CNTRL[14] = 1).

The 5V serial EEPROM clock is derived from the PCI clock. The PCI 9050-1 generates the serial EEPROM clock by internally dividing the PCI clock by 32.

Table 3-1. Serial EEPROM Guidelines

Serial EEPROM	PCI 9050-1 System Boot Condition
None	Uses default values (Start bit is 1).
Programmed	Boots with serial EEPROM values (Start bit is 0).
Blank	Detects a blank device and reverts to default values (Start bit is 0).

Notes: *2K-bit devices, such as the FM93CS56, are not compatible.*

The PCI 9050-1 does not support serial EEPROMs that do not support sequential reads and writes (such as the FM93C46L).

3—Reset & Serial EEPROM

A PCI Bus Host can read or program the serial EEPROM. Register bits CNTRL[29:24] control the PCI 9050-1 pins, enabling reading or writing of the serial EEPROM bits. (Refer to the manufacturer's data sheet for the particular serial EEPROM being used.)

To reload serial EEPROM data into the PCI 9050-1 internal registers, write 1 to the Reload Configuration Registers bit (CNTRL[29]=1).

The following steps are necessary, to read or write to the serial EEPROM:

1. Enable the serial EEPROM Chip Select, EECS, by writing 1 to the Miscellaneous Control register (CNTRL[25]=1).
2. Generate the serial EEPROM clock by writing 0 and then 1. The data is read or written during the zero-to-one transition (refer to CNTRL[24).
3. Send the command code to the serial EEPROM.
4. If the serial EEPROM is present, 0 is returned as a start bit after the command code.
5. Read or write the data.
6. Write 0 to CNTRL[25] to end serial EEPROM access (the serial EEPROM EECS pin goes low).

3.3.1 Serial EEPROM Load Sequence

The serial EEPROM load sequence, listed in Table 3-2, uses the following abbreviations:

- **MSW** = Most Significant Word Bits [31:16]
- **LSW** = Least Significant Word Bits [15:0]

Note: *Serial EEPROM values shown are register values for the PCI 9050RDK.*

3.3.1.1 Serial EEPROM Load

The registers listed in Table 3-2 are loaded from the serial EEPROM after a PCI Reset is de-asserted. The serial EEPROM is organized in words (16-bit). The PCI 9050-1 first loads the Most Significant Word bits (MSW[31:16]), starting from the most significant bit ([31]). The PCI 9050-1 then loads the Least Significant Word bits (LSW[15:0]), starting again from the most significant bit ([15]). Therefore, the PCI 9050-1 loads the Device ID, Vendor ID, class code, and so forth.

The serial EEPROM values can be programmed using a serial EEPROM programmer or PLXMon™ software.

The CNTRL register allows programming of the serial EEPROM, one bit at a time. Values should be programmed in the order listed in Table 3-2. The 50, 16-bit words listed in the table are stored sequentially in the serial EEPROM.

3.3.1.2 Recommended Serial EEPROMs

The PCI 9050-1 is designed to use a 1K-bit, 1 MHz serial EEPROM, powered at 5V:

- Fairchild Semiconductor FM93CS46L
- Holtek HT93LC46 (tie ORG pin high for 16 bit)
- Integrated Silicon Solution IS93C46-3
- Microchip Technology 93C46B, 93LC46B, or 93AA46 (tie ORG pin high for 16 bit)
- Rohm BR93LC46
- Seiko S-93C46A
- ST Microelectronics M93C46 or M93S46

or other compatible serial EEPROM.

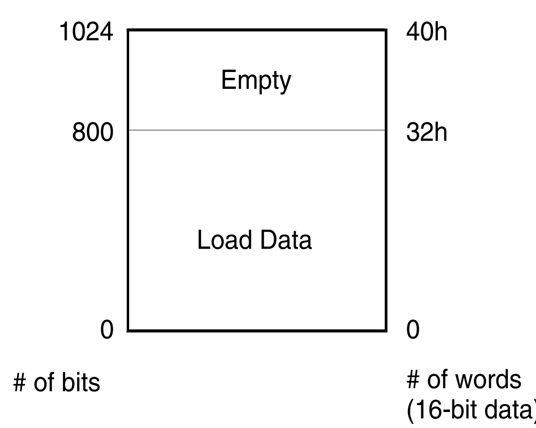


Figure 3-1. Serial EEPROM Memory Map

Note: *Serial EEPROM data values shown in Table 3-2 are from the PCI 9050RDK Hardware Reference Manual.*

Table 3-2. Serial EEPROM Register Load Sequence

Serial EEPROM Offset	Register Offset	Serial EEPROM Value	Description
0h	PCI 02h	9050	Device ID.
2h	PCI 00h	10B5	Vendor ID.
4h	PCI 0Ah	0680	Class Code.
6h	PCI 08h	000x	Class Code (revision is not loadable).
8h	PCI 2Eh	9050	Subsystem ID.
Ah	PCI 2Ch	10B5	Subsystem Vendor ID.
Ch	PCI 3Eh	xxxx	(Maximum Latency and Minimum Grant are not loadable.)
Eh	PCI 3Ch	01xx	Interrupt Pin (Interrupt Line Routing is not loadable).
10h	LOCAL 02h	FFF0	MSW of Range for PCI-to-Local Address Space 0 (1 MB).
12h	LOCAL 00h	0000	LSW of Range for PCI-to-Local Address Space 0 (1 MB).
14h	LOCAL 06h	FFFF	MSW of Range for PCI-to-Local Address Space 1.
16h	LOCAL 04h	FFF1	LSW of Range for PCI-to-Local Address Space 1.
18h	LOCAL 0Ah	FFF0	MSW of Range for PCI-to-Local Address Space 2.
1Ah	LOCAL 08h	0000	LSW of Range for PCI-to-Local Address Space 2.
1Ch	LOCAL 0Eh	FFF0	MSW of Range for PCI-to-Local Address Space 3.
1Eh	LOCAL 0Ch	0000	LSW of Range for PCI-to-Local Address Space 3.
20h	LOCAL 12h	0000	MSW of Range for PCI-to-Local Expansion ROM (64 KB).
22h	LOCAL 10h	0000	LSW of Range for PCI-to-Local Expansion ROM (64 KB).
24h	LOCAL 16h	0200	MSW of Local Base Address (Remap) for PCI-to-Local Address Space 0.
26h	LOCAL 14h	0001	LSW of Local Base Address (Remap) for PCI-to-Local Address Space 0.
28h	LOCAL 1Ah	0300	MSW of Local Base Address (Remap) for PCI-to-Local Address Space 1.
2Ah	LOCAL 18h	0001	LSW of Local Base Address (Remap) for PCI-to-Local Address Space 1.
2Ch	LOCAL 1Eh	0100	MSW of Local Base Address (Remap) for PCI-to-Local Address Space 2.
2Eh	LOCAL 1Ch	0001	LSW of Local Base Address (Remap) for PCI-to-Local Address Space 2.
30h	LOCAL 22h	0400	MSW of Local Base Address (Remap) for PCI-to-Local Address Space 3.
32h	LOCAL 20h	0001	LSW of Local Base Address (Remap) for PCI-to-Local Address Space 3.
34h	LOCAL 26h	0000	MSW of Local Base Address (Remap) for PCI-to-Local Expansion ROM.
36h	LOCAL 24h	0000	LSW of Local Base Address (Remap) for PCI-to-Local Expansion ROM.
38h	LOCAL 2Ah	4000	MSW of Bus Region Descriptors for Local Address Space 0.
3Ah	LOCAL 28h	0022	LSW of Bus Region Descriptors for Local Address Space 0.
3Ch	LOCAL 2Eh	4000	MSW of Bus Region Descriptors for Local Address Space 1.
3Eh	LOCAL 2Ch	0022	LSW of Bus Region Descriptors for Local Address Space 1.
40h	LOCAL 32h	0080	MSW of Bus Region Descriptors for Local Address Space 2.
42h	LOCAL 30h	0005	LSW of Bus Region Descriptors for Local Address Space 2.
44h	LOCAL 36h	5421	MSW of Bus Region Descriptors for Local Address Space 3.
46h	LOCAL 34h	38E9	LSW of Bus Region Descriptors for Local Address Space 3.
48h	LOCAL 3Ah	0000	MSW of Bus Region Descriptors for Expansion ROM Space.
4Ah	LOCAL 38h	0000	LSW of Bus Region Descriptors for Expansion ROM Space.
4Ch	LOCAL 3Eh	0208	MSW of Chip Select (CS) 0 Base and Range.
4Eh	LOCAL 3Ch	0001	LSW of Chip Select (CS) 0 Base and Range.
50h	LOCAL 42h	0300	MSW of Chip Select (CS) 1 Base and Range.
52h	LOCAL 40h	0009	LSW of Chip Select (CS) 1 Base and Range.
54h	LOCAL 46h	0101	MSW of Chip Select (CS) 2 Base and Range.

Table 3-2. Serial EEPROM Register Load Sequence (Continued)

Serial EEPROM Offset	Register Offset	Serial EEPROM Value	Description
56h	LOCAL 44h	0001	LSW of Chip Select (CS) 2 Base and Range.
58h	LOCAL 4Ah	0408	MSW of Chip Select (CS) 3 Base and Range.
5Ah	LOCAL 48h	0001	LSW of Chip Select (CS) 3 Base and Range.
5Ch	LOCAL 4Eh	0000	MSW of Interrupt Control/Status.
5Eh	LOCAL 4Ch	0041	LSW of Interrupt Control/Status.
60h	LOCAL 52h	007C	MSW of Serial EEPROM Control and Miscellaneous Control.
62h	LOCAL 50h	4B76	LSW of Serial EEPROM Control and Miscellaneous Control.

3.4 INTERNAL REGISTERS

The PCI 9050-1 chip provides several internal registers, allowing maximum flexibility in bus interface design and performance. The register types are as follows:

- **PCI Configuration Registers** (accessible from the PCI Bus and serial EEPROM)
- **Local Configuration Registers** (accessible from the PCI Bus and serial EEPROM)

Note: *Local Configuration register access can be limited to Memory- or I/O-Mapped. Access can also be disabled by way of the PCIBAR Enable bits (CNTRL[13:12]). These bits should not be disabled for the PC platform.*

3.4.1 PCI Configuration Registers

Device and Vendor IDs. There are two sets of Device and Vendor IDs. The Device ID and Vendor ID are located at offset 00h of the PCI Configuration registers (PCIIDR[31:16] and PCIIDR[15:0], respectively). The Subsystem ID and Subsystem Vendor ID are located at offsets 2Eh and 2Ch, respectively, of the PCI Configuration registers (PCISID[15:0] and PCISVID[15:0], respectively). The Device ID and Vendor ID identify the particular device and its manufacturer. The Subsystem Vendor ID and Subsystem ID provide a way to distinguish between PCI interface chip vendors and add-in board manufacturers, using a PCI chip.

Status. This register contains PCI Bus-related events information.

Command. This register controls the ability of a device to respond to PCI accesses. It controls whether the device responds to I/O or Memory Space accesses.

Class Code. This register identifies the general function of the device. (Refer to *PCI r2.2* for further details.)

Revision ID. The value read from this register represents the PCI 9050-1 current silicon revision.

Header Type. This register defines the device configuration header format and whether the device is single function or multifunction.

Note: *Multiple functions are not supported.*

Cache Line Size. This register defines the system cache line size in units of 32-bit Lwords.

PCI Base Address for Memory Accesses to Local Configuration Registers. The system BIOS uses this register to assign a PCI Address space segment for Memory accesses to the PCI 9050-1 Local Configuration registers. The PCI Address Range occupied by these Configuration registers is fixed at 128 bytes. During initialization, the host writes FFFFFFFF to this register, then reads back FFFFFF80, determining the required Memory space of 128 bytes. The host then writes the base address to PCIBAR0[31:7].

PCI Base Address for I/O Accesses to Local Configuration Registers. The system BIOS uses this register to assign a PCI address space segment for I/O accesses to the PCI 9050-1 Local Configuration registers. The PCI address range occupied by these Configuration registers is fixed at 128 bytes. During initialization, the host writes FFFFFFFF to this register, then reads back FFFFFF81, determining a required 128 bytes of I/O space. The host then writes the base address to PCIBAR1[31:7].

PCI Base Address for Accesses to Local Address Spaces 0, 1, 2, and 3. The system BIOS uses these registers to assign a PCI address space segment for accesses to Local Address Space 0, 1, 2, and 3. The PCI address range occupied by this space is determined by the Local Address Space Range registers. During initialization, the host writes FFFFFFFF to these registers, then reads back a value determined by the range. The host then writes the base address to the upper bits of these registers.

PCI Expansion ROM Base Address. The system BIOS uses this register to assign a PCI address space segment for accesses to the Expansion ROM. The PCI address range occupied by this space is determined by the Expansion ROM Range register. During initialization, the host writes FFFFFFFF to this register, then reads back a value determined by the range. The host then writes the base address to the upper bits of this register.

PCI Interrupt Line. This register identifies where the device interrupt line connects on the system interrupt controller(s).

PCI Interrupt Pin. This register specifies the interrupt request pin (if any) to be used.

3.4.2 PCI Bus Access to Internal Registers

The PCI 9050-1 PCI Configuration registers are accessed from the PCI Bus with a Type 0 Configuration cycle.

The PCI 9050-1 Local Configuration registers are accessed by one of the following:

- A Memory cycle, with the PCI Bus address matching the base address specified in the PCI Base Address register for Memory Accesses to Local Configuration registers (PCIBAR0)
- An I/O cycle, with the PCI Bus address matching the base address specified in the PCI Base Address register for I/O Accesses to Local Configuration registers (PCIBAR1)

All PCI Read or Write accesses to the PCI 9050-1 registers can be Byte, Word, or Lword accesses. Memory accesses to the PCI 9050-1 registers can be burst or non-burst. The PCI 9050-1 responds with a PCI Bus disconnect for all Burst I/O accesses to the PCI 9050-1 registers.

4 DIRECT SLAVE OPERATION

The functional operation described can be modified through the PCI 9050-1 programmable internal registers.

4.1 OVERVIEW

Direct Slave operations originate on the PCI Bus, go through the PCI 9050-1, and finally access the Local Bus. The PCI 9050-1 is a PCI Bus Slave and a Local Bus master.

4.2 DIRECT DATA TRANSFER MODE

The PCI 9050-1 supports Direct Slave accesses to Local Memory by way of Memory or I/O transfers.

4.2.1 Direct Slave Operation (PCI Master-to-Local Bus Access)

The PCI 9050-1 supports Burst Memory-Mapped Transfer accesses and single Memory- or I/O-Mapped Transfer accesses to the Local Bus from the PCI Bus through an 8-Lword (32-byte) Direct Slave Read FIFO and a 16-Lword (64-byte) Direct Slave Write FIFO. The PCI Base Address registers are provided to set up the adapter location in the PCI Memory and I/O space. In addition, Local Mapping registers allow address translation from the PCI Address Space to the Local Address Space. The following five spaces are available:

- Space 0
- Space 1
- Space 2
- Space 3
- Expansion ROM

Expansion ROM is intended to support a bootable ROM device for the Host.

For single cycle Direct Slave reads, the PCI 9050-1 reads a single Local Bus Lword or partial Lword. The PCI 9050-1 disconnects after one transfer for all Direct Slave I/O accesses.

For higher data transfer rates, the PCI 9050-1 can be programmed to prefetch data during a PCI Burst Read. The Prefetch size, when enabled, can be 4, 8, or 16 Lwords, or until the PCI Bus stops requesting. When the PCI 9050-1 prefetches, if enabled, it drops the Local Bus read after reaching the prefetch count. In Continuous Prefetch mode, the PCI 9050-1 prefetches as long as FIFO space is available and stops prefetching when the PCI Bus terminates the request. If Read prefetching is disabled, the PCI 9050-1 stops after one Read transfer.

In addition to Prefetch mode, the PCI 9050-1 supports Direct Slave Read Ahead mode. (Refer to Section 4.2.1.3.)

Each Local space can be programmed to operate in an 8-, 16-, or 32-bit Local Bus width. The PCI 9050-1 contains an internal wait state generator and external wait state input, LRDYi#. LRDYi# can be disabled or enabled by way of the Internal Configuration registers.

With or without wait state(s), the Local Bus, independent of the PCI Bus, can:

- Burst as long as data is available (Continuous Burst mode)
- Burst four Lwords at a time
- Perform continuous single cycles

4.2.1.1 Direct Slave Lock

The PCI 9050-1 supports direct PCI-to-Local Bus Exclusive accesses (locked atomic operations). A PCI-locked operation to the Local Bus results in the entire address Spaces 0, 1, 2, and 3, and Expansion ROM space being locked until they are released by the PCI Bus Master. Locked operations are enabled or disabled with the Direct Slave LOCK# Enable bit (CNTRL[23]) for PCI-to-Local accesses.

It is the responsibility of external arbitration logic to monitor the LLOCKo# pin and enforce the meaning for an atomic operation. *For example*, if a local master initiates a locked operation, the local arbiter may choose to not grant use of the Local Bus to other masters until the locked operation is complete

4.2.1.2 Direct Slave Delayed Read Mode

The PCI 9050-1 can be programmed to perform Direct Slave Delayed reads (CNTRL[14]). (Refer to Figure 4-1.)

In addition to delayed reads, the PCI 9050-1 supports the following *PCI r2.1* functions:

- No write while a read is pending (PCI Retry for writes)
- Write and flush pending read

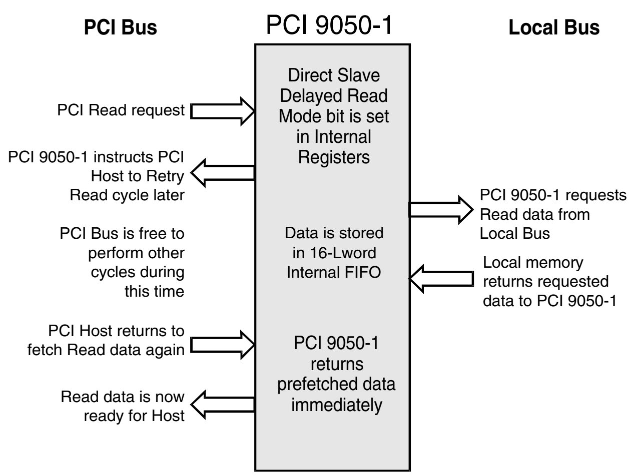


Figure 4-1. Direct Slave Delayed Reads

Note: *The figure represents a sequence of Bus cycles.*

4.2.1.3 Direct Slave Read Ahead Mode

The PCI 9050-1 also supports Direct Slave Read Ahead mode (CNTRL[16]), where prefetched data can be read from the PCI 9050-1 internal FIFO instead of the Local Bus. The address must be subsequent to the previous address and 32-bit aligned (next address = current address + 4). The Direct Slave Read Ahead mode functions can be used with or without the Direct Slave Delayed Read mode. (Refer to Figure 4-2.)

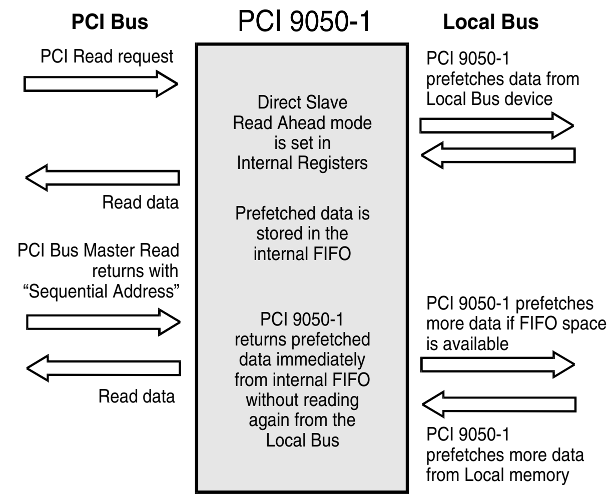


Figure 4-2. Direct Slave Read Ahead Mode

Note: *The figure represents a sequence of Bus cycles.*

4.2.1.4 Direct Slave Transfer

A PCI Bus Master addressing the Memory space decoded for the Local Bus initiates transactions. Upon a PCI Read/Write, the PCI 9050-1 being a Local Bus Master executes a transfer, at which time it reads data into the Direct Slave Read FIFO or writes data to the Local Bus.

For a PCI Direct access to the Local Bus, the PCI 9050-1 has a 16-Lword (64-byte) Write FIFO and an 8-Lword (32-byte) Read FIFO. The FIFOs enable the Local Bus to operate independently of the PCI Bus.

For Write transfers, the PCI 9050-1 is programmable to disconnect or retain the PCI Bus by generating a wait state(s) and de-asserting TRDY# if the Write FIFO becomes full (CNTRL[18]).

For PCI Read transactions from the Local Bus, the PCI 9050-1 holds off TRDY# while gathering data from the Local Bus. For Read accesses mapped to PCI Memory space, the PCI 9050-1 prefetches up to 16 Lwords (in Continuous Prefetch mode) from the Local Bus. Unused Read data is flushed from the FIFO. For Read accesses mapped to PCI I/O space, the PCI 9050-1 does not prefetch Read data. Rather, it breaks each read of a Burst cycle into a single Address/Data cycle on the Local Bus.

The Direct Slave Retry Delay Clocks bits (CNTRL[22:19]) can be used to program the period of time in which the PCI 9050-1 holds off TRDY#. The PCI 9050-1 issues a Retry to the PCI Bus Transaction Master when the programmed time period expires. This occurs when the PCI 9050-1 cannot gain Local Bus control and return TRDY# within the programmed time period or the Local Bus is slowly emptying the Write FIFO, and filling the Read FIFO.

The PCI 9050-1 supports on-the-fly Endian conversion for Spaces 0, 1, 2, and 3, and Expansion ROM. The Local Bus can be Big/Little Endian by using the programmable internal register configuration.

Note: *The PCI Bus is always Little Endian.*

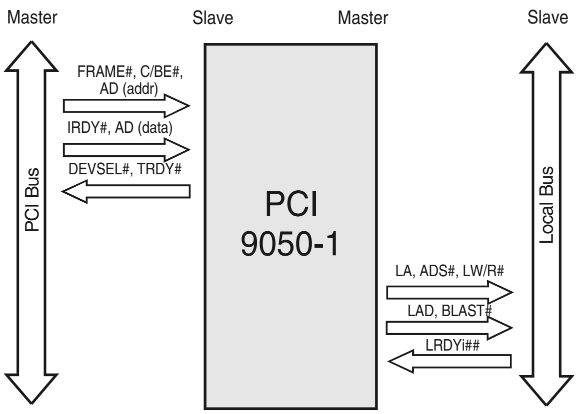


Figure 4-3. Direct Slave Write

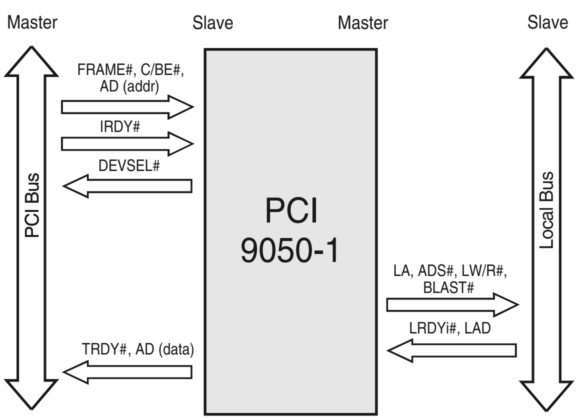


Figure 4-4. Direct Slave Read

Note: *The figures represent a sequence of Bus cycles.*

4.2.1.5 Direct Slave PCI-to-Local Address Mapping

Five Local Address spaces—Space 0, Space 1, Space 2, Space 3, and Expansion ROM—are accessible from the PCI Bus. Each is defined by a set of three registers:

- **Local Address Range**—LAS0RR, LAS1RR, LAS2RR, LAS3RR, and/or EROMRR
- **Local Base Address**—LAS0BA, LAS1BA, LAS2BA, LAS3BA, and/or EROMBA
- **PCI Base Address**—PCIBAR2, PCIBAR3, PCIBAR4, PCIBAR5, and/or PCIERBAR

A fourth register, the Bus Region Descriptor register for PCI-to-Local Accesses (LAS0BRD, LAS1BRD, LAS2BRD, LAS3BRD, and/or EROMBRD), defines the Local Bus characteristics for the Direct Slave regions. (Refer to Figure 4-5.)

Each PCI-to-Local Address space is defined as part of reset initialization. (Refer to Section 4.2.1.5.1.) These Local Bus characteristics can be modified at any time before actual data transactions.

4.2.1.5.1 Direct Slave Local Bus Initialization

Range—Specifies the PCI Address bits to use for decoding a PCI access to Local Bus space. Each bit corresponds to a PCI Address bit. Bit 31 corresponds to address bit 31. Write 1 to all bits required to be included in decode, and 0 to all others.

Remap PCI-to-Local Addresses into a Local Address Space—Bits in this register remap (replace) the PCI Address bits used in decode as the Local Address bits.

Local Bus Region Descriptor—Specifies the Local Bus characteristics.

4.2.1.5.2 Direct Slave Initialization

After a PCI reset and serial EEPROM load, the software determines the amount of required address space by writing all ones (1) to a PCI Base Address register and then reading back the value. The PCI 9050-1 returns zeros (0) in the Don't Care Address bits, effectively specifying the address space required, at which time the PCI software maps the Local Address space into the PCI Address space by programming the PCI Base Address register.

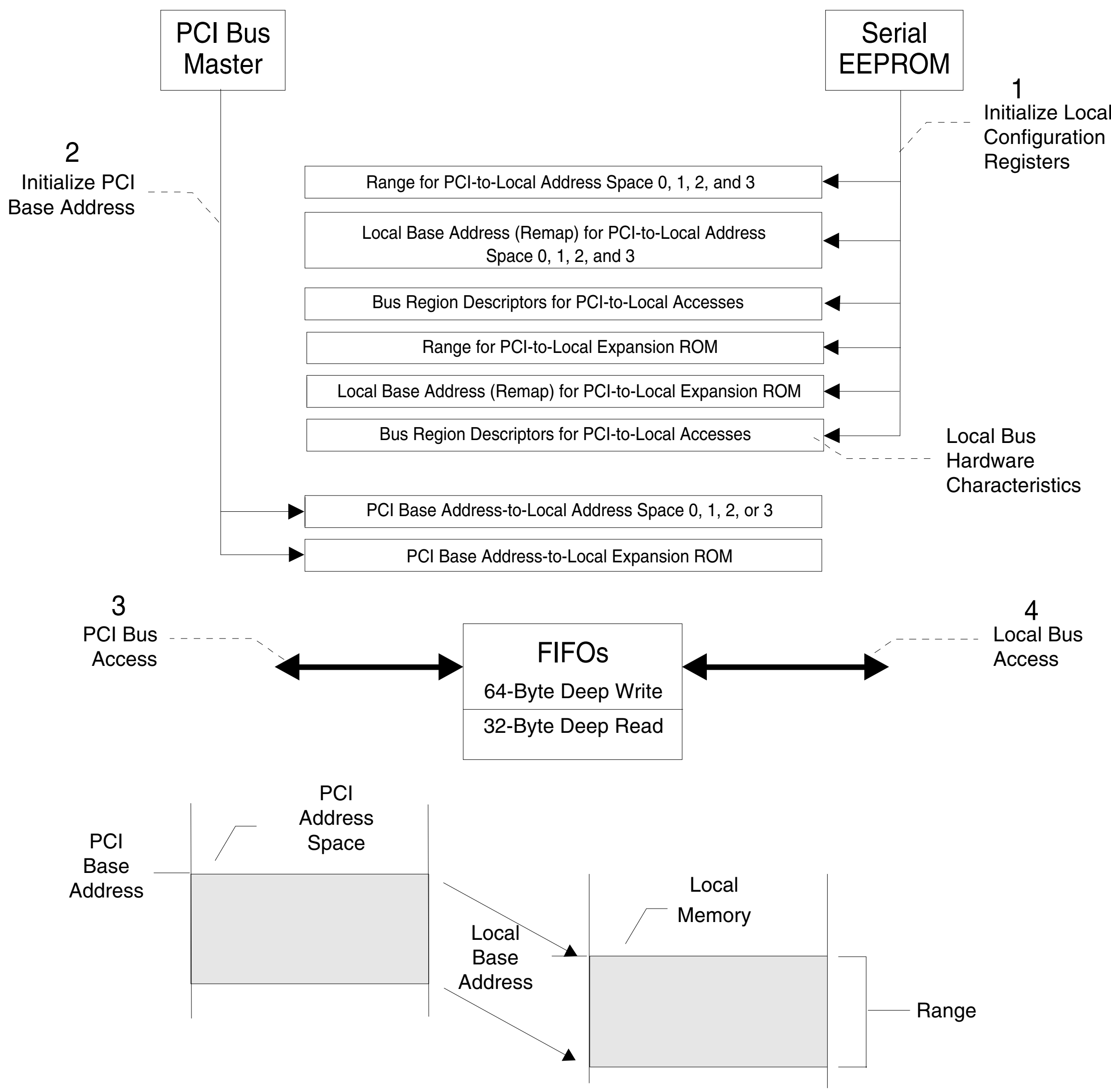


Figure 4-5. Local Bus Direct Slave Access

4.2.1.5.3 Direct Slave Example

A 1 MB Local Address Space, 12300000h through 123FFFFFh, is accessible from the PCI Bus at PCI addresses 78900000h through 789FFFFFh.

a. Local initialization software sets the Range and Local Base Address registers as follows:
   - **Range**—FFF00000h (1 MB, decode the upper 12 PCI Address bits)
   - **Local Base Address (Remap)**—123XXXXXh, (Local Base Address for PCI-to-Local accesses) [Space Enable bit(s) must be set to be recognized by the PCI Host (LAS0BA[0]=1and/or LAS1BA[0]=1)]

b. PCI Initialization software writes all ones to the PCI Base Address, then reads it back.
   - The PCI 9050-1 returns a value of FFF00000h, at which time the PCI software writes to the PCI Base Address register(s).
   - **PCI Base Address**—789XXXXXh (PCI Base Address for Access to the Local Address Space registers, PCIBAR2 and PCIBAR3).

4.2.1.5.4 Direct Slave Byte Enables (C Mode)

During a Direct Slave transfer, each of five spaces (Space 0, Space 1, Space 2, Space 3, and Expansion ROM space) can be programmed to operate in an 8-, 16-, or 32-bit Local Bus width by encoding the Local byte enables (LBE[3:0]#).

LBE[3:0]# are encoded, based on the configured Bus width, as follows.

32-Bit Bus—The four byte enables indicate which of the four bytes are active during a Data cycle:

- LBE3# Byte Enable 3—LAD[31:24]
- LBE2# Byte Enable 2—LAD[23:16]
- LBE1# Byte Enable 1—LAD[15:8]
- LBE0# Byte Enable 0—LAD[7:0]

16-Bit Bus—LBE[3, 1:0]# are encoded to provide BHE#, LA1, and BLE#, respectively:

- LBE3# Byte High Enable (BHE#)—LAD[15:8]
- LBE2# ***not used***
- LBE1# Address bit 1 (LA1)
- LBE0# Byte Low Enable (BLE#)—LAD[7:0]

8-Bit Bus—LBE[1:0]# are encoded to provide LA1 and LA0, respectively:

- LBE3# ***not used***
- LBE2# ***not used***
- LBE1# Address bit 1 (LA1)
- LBE0# Address bit 0 (LA0)

4.2.1.5.5 Direct Slave Byte Enables (J Mode)

During a Direct Slave transfer, each of five spaces (Space 0, Space 1, Space 2, Space 3, and Expansion ROM space) can be programmed to operate in an 8-, 16-, or 32-bit Local Bus width by encoding the Local byte enables (LBE[3:0]#).

LBE[3:0]# are encoded, based on the configured Bus width, as follows.

32-Bit Bus—The four byte enables indicate which of the four bytes are active during a Data cycle:

- LBE3# Byte Enable 3—LAD[31:24]
- LBE2# Byte Enable 2—LAD[23:16]
- LBE1# Byte Enable 1—LAD[15:8]
- LBE0# Byte Enable 0—LAD[7:0]

16-Bit Bus—LBE[3, 1:0]# are encoded to provide BHE#, LAD1, and BLE#, respectively:

- LBE3# Byte High Enable (BHE#)—LAD[15:8]
- LBE2# ***not used***
- LBE1# Address bit 1 (LAD1)
- LBE0# Byte Low Enable (BLE#)—LAD[7:0]

8-Bit Bus—LBE[1:0]# are encoded to provide LAD[1:0], respectively:

- LBE3# ***not used***
- LBE2# ***not used***
- LBE1# Address bit 1 (LAD1)
- LBE0# Address bit 0 (LAD0)

During the address phase, LAD[1:0] are valid address bits with the same value as LBE[1:0]#.

4.3 RESPONSE TO FIFO FULL OR EMPTY

Table 4-1 lists the PCI 9050-1 response to full or empty FIFOs.

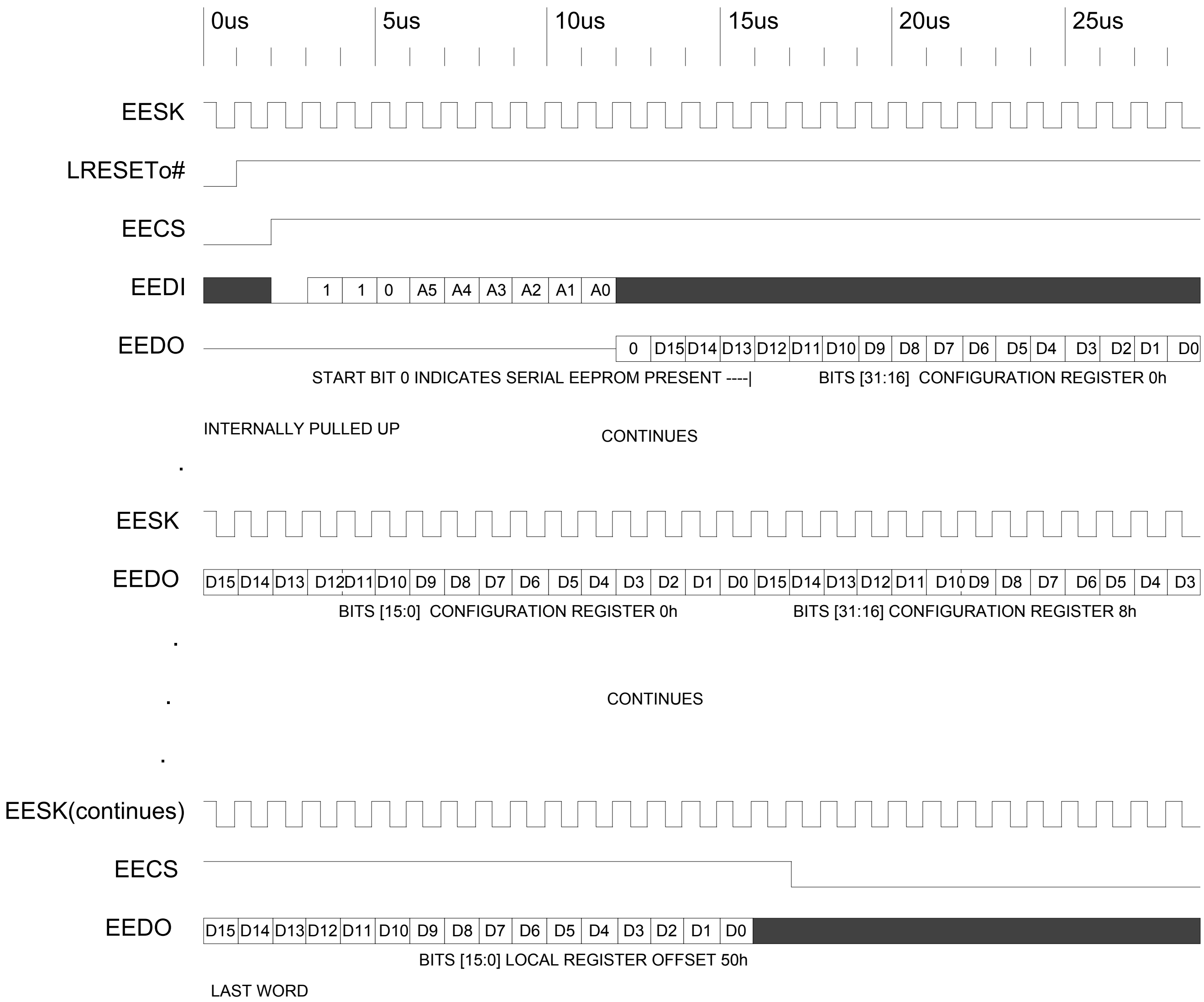
Table 4-1. Response to FIFO Full or Empty

Mode	Direction	FIFO	PCI Bus	Local Bus
Direct Slave Write	PCI-to-Local	Full	Disconnect or Throttle TRDY#[1]	De-assert LHOLDA if Local Bus is busy and wait for LHOLD to be de-asserted
		Empty	Normal	Normal, assert BLAST#
Direct Slave Read	Local-to-PCI	Full	Normal	Normal, assert BLAST#
		Empty	Disconnect or Throttle TRDY#[1]	Normal

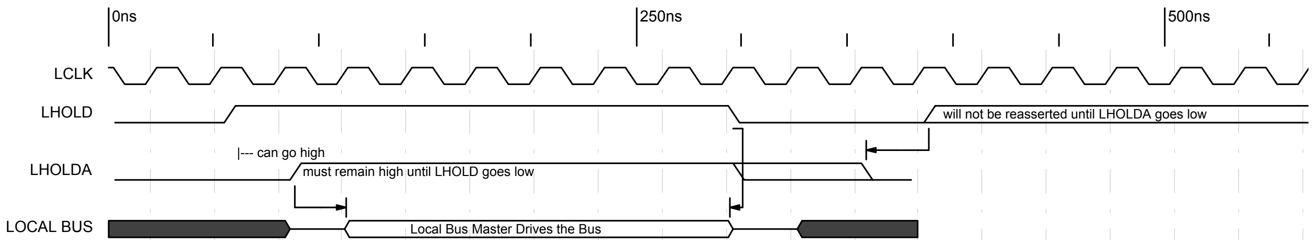
1. Throttle TRDY# depends on the Direct Slave Retry Delay Clocks (CNTRL[22:19]).

4.4 TIMING DIAGRAMS

4.4.1 Serial EEPROM and Configuration Initialization

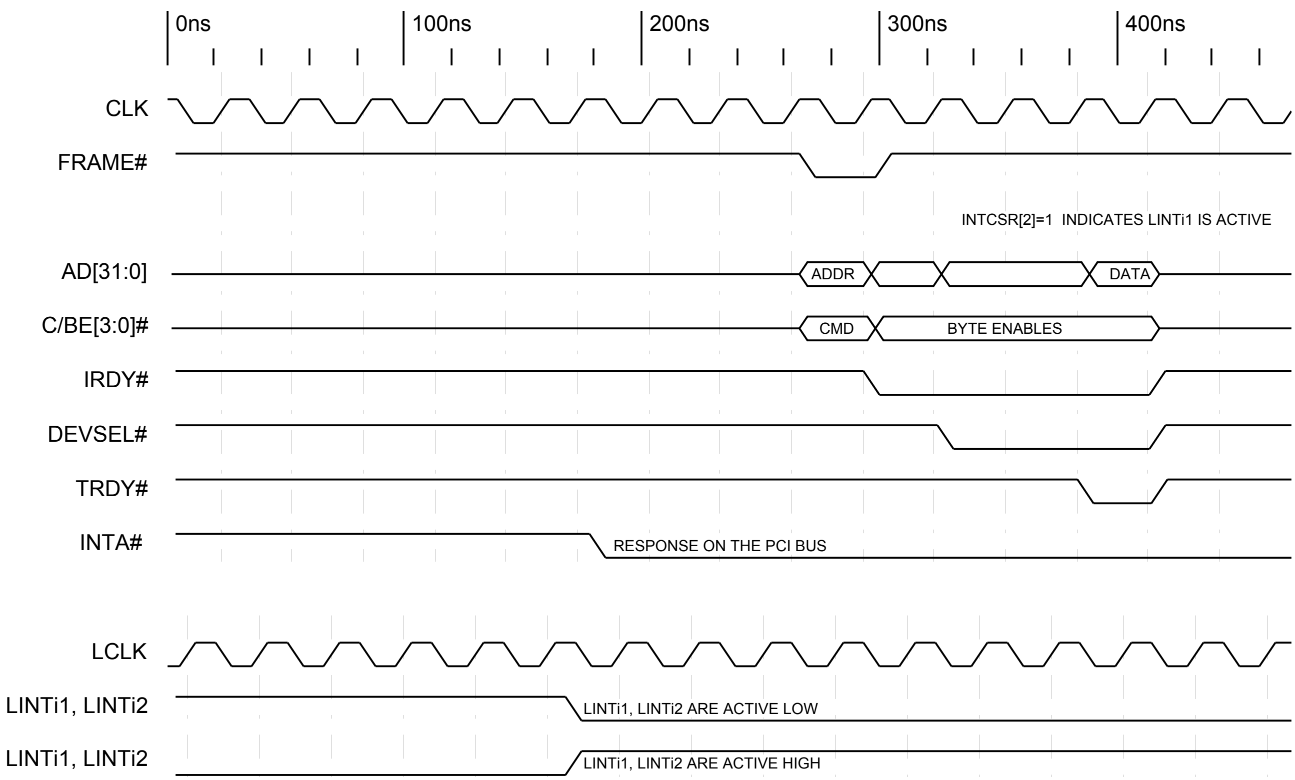


Timing Diagram 4-1. Initialization from Serial EEPROM

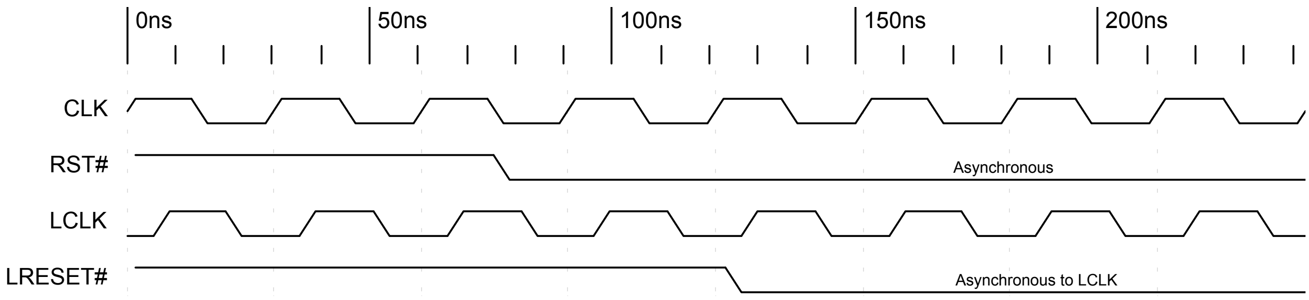


Note: The PCI 9050-1 always releases Local Bus between different Direct Slave accesses.

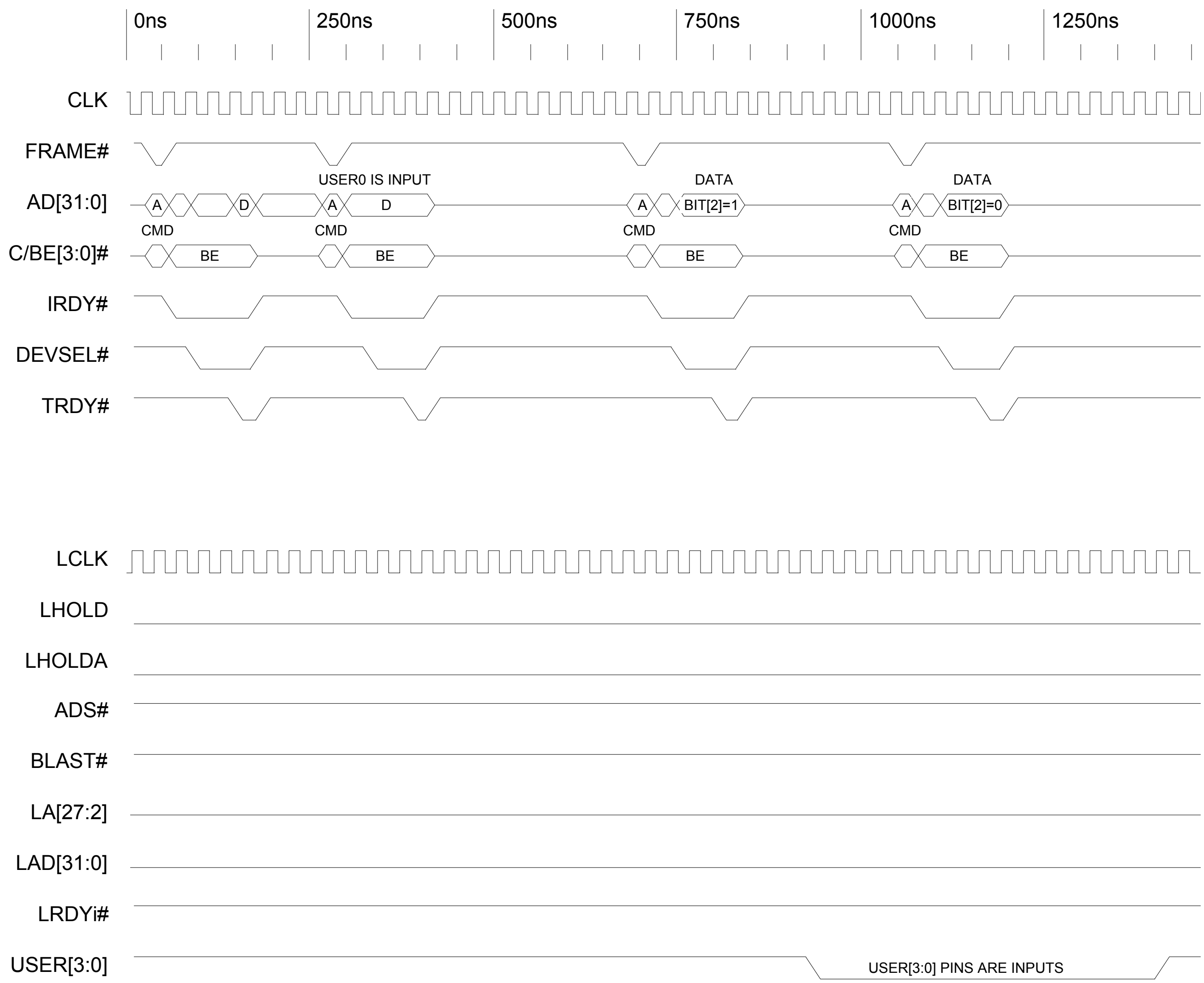
Timing Diagram 4-2. PCI 9050-1 Local Bus Arbitration



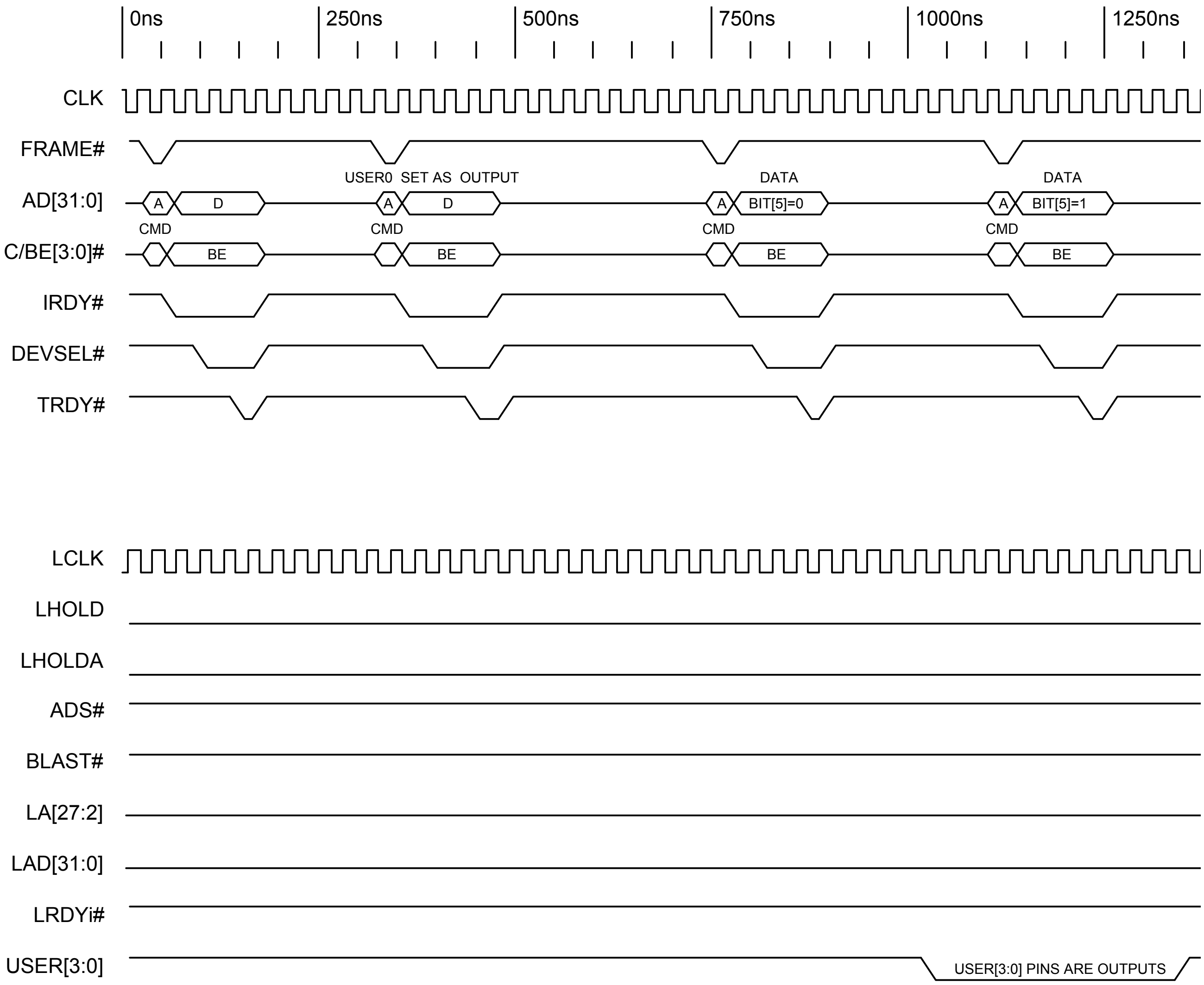
Timing Diagram 4-3. Local LINTi1 Asserting PCI Output INTA#



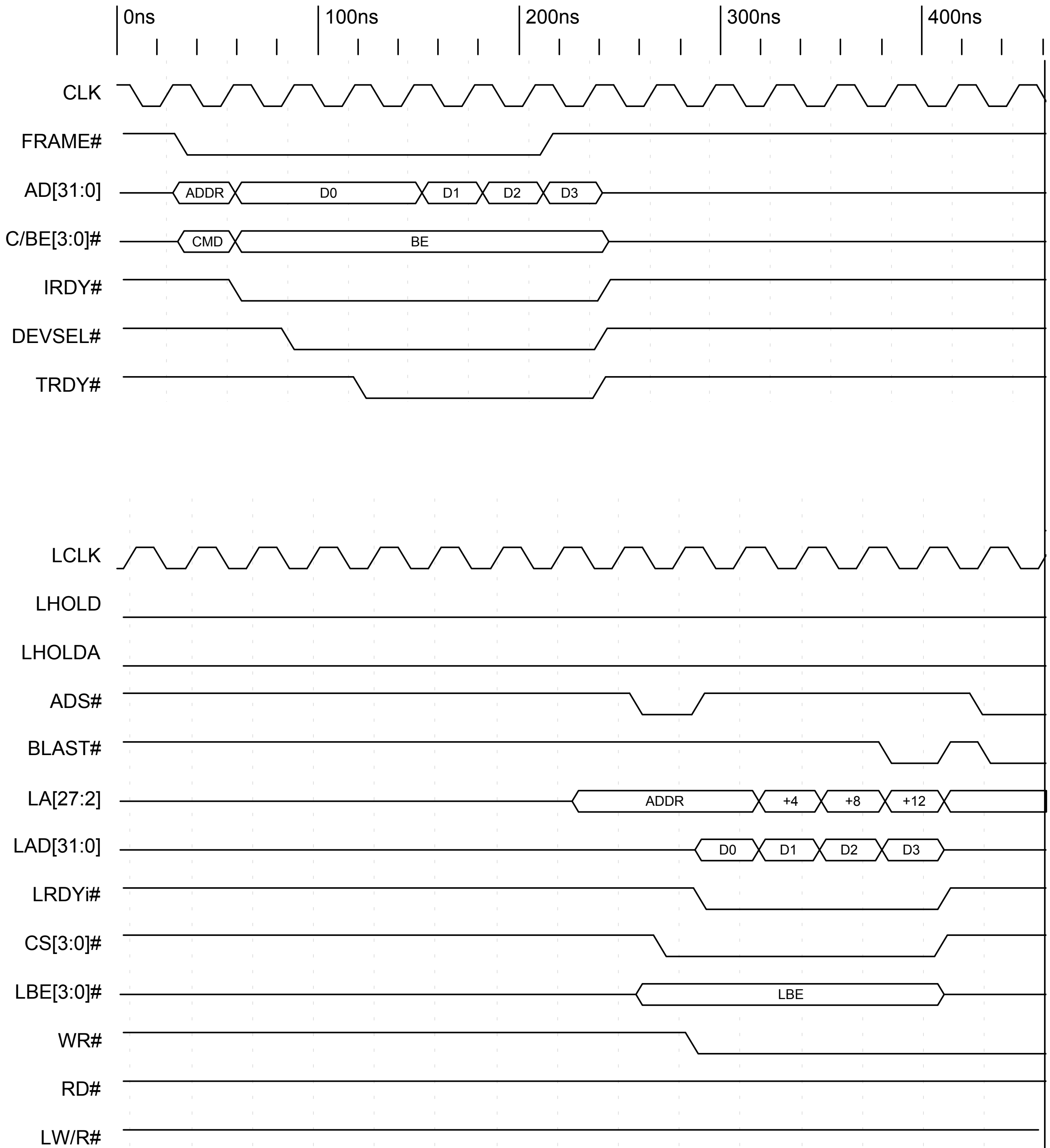
Timing Diagram 4-4. PCI RST# Asserting Local Output LRESET#



Timing Diagram 4-5. USER[3:0] as Inputs



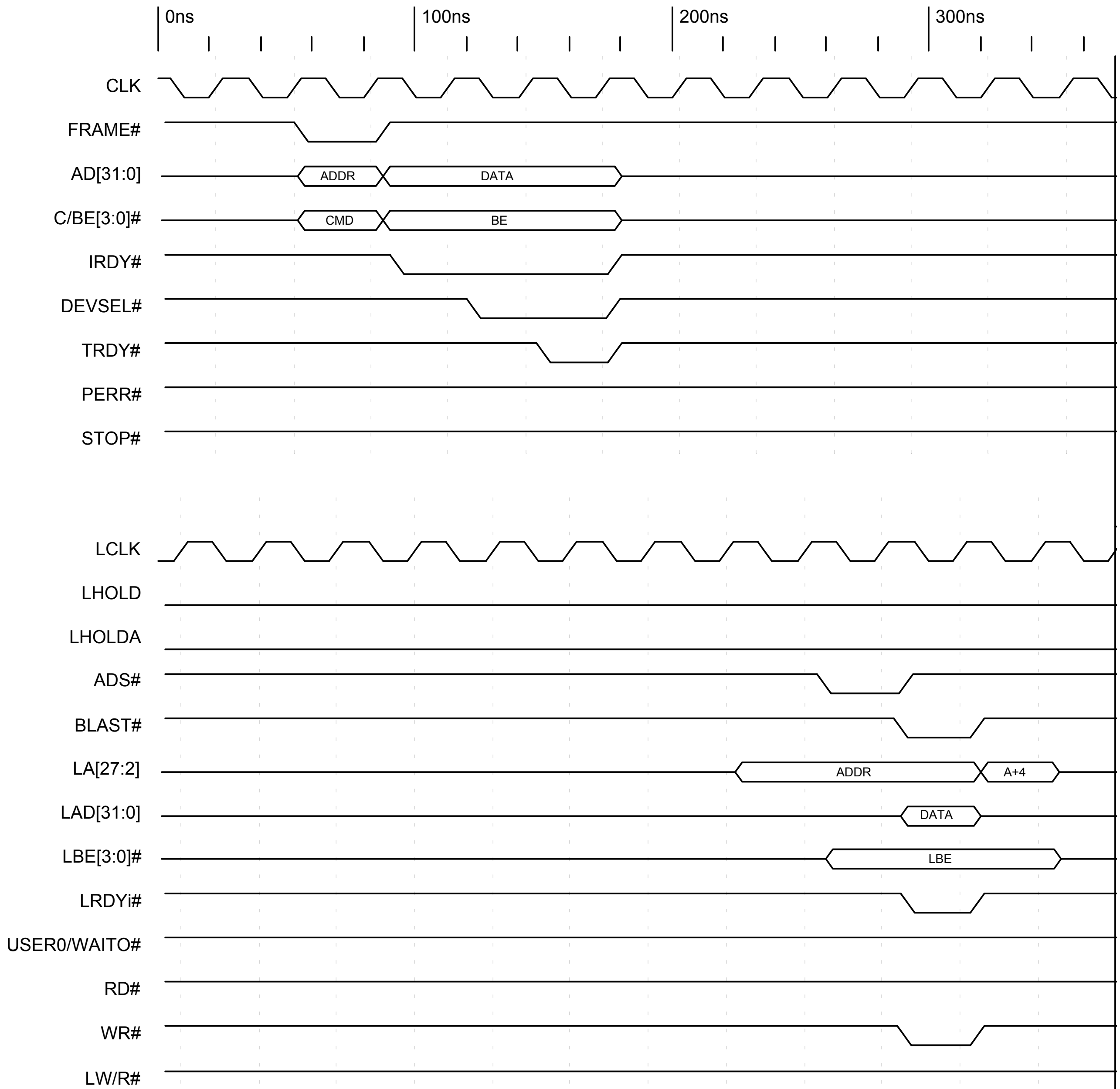
Timing Diagram 4-6. USER[3:0] as Outputs



Note: CS[3:0]# Base Address is in the range of Spaces 3 through 0

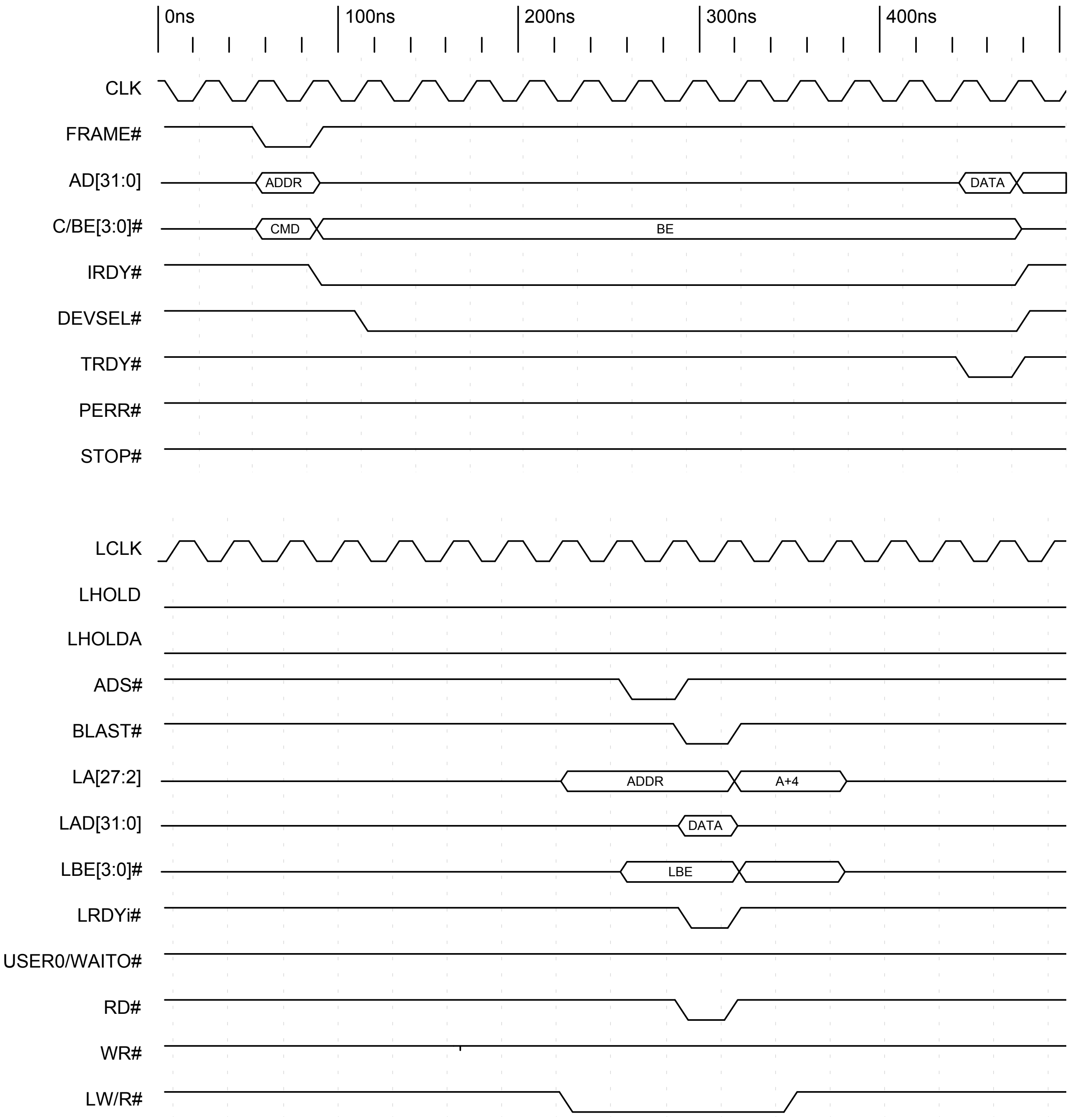
Timing Diagram 4-7. Chip Select [3:0]#

4.4.2 C Mode Local Bus



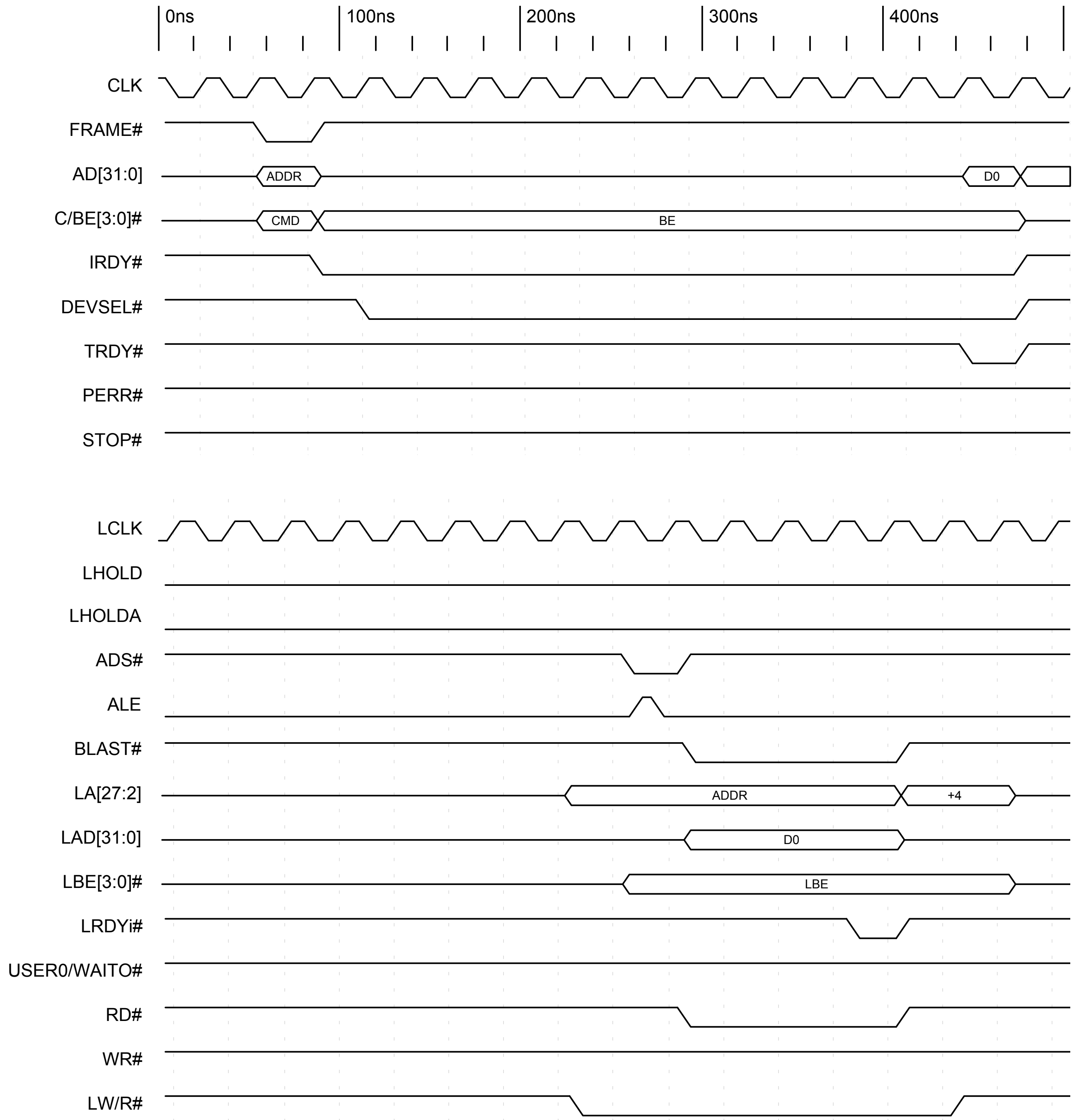
Note: Single write, 32-bit Local Bus, without wait states
Space 0 is mapped to I/O
Address-to-data = zero wait states
Data-to-data = zero wait states
Read strobe delay = zero wait states

Timing Diagram 4-8. C Mode, Direct Slave Single Write without Wait States (32-Bit Local Bus)



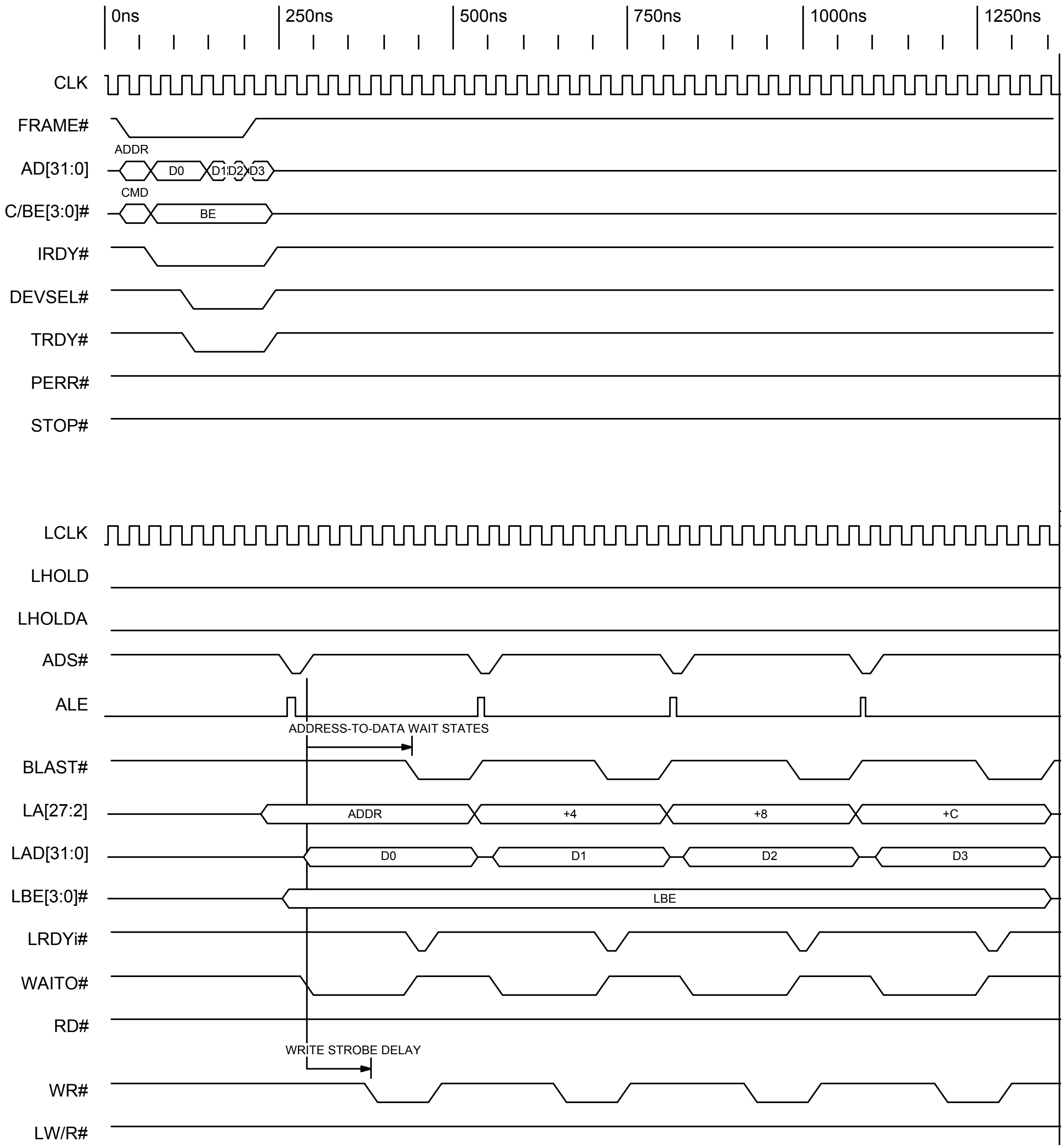
Note: Single read, 32-bit Local Bus, without wait states
Space 0 is mapped to I/O
Address-to-data = zero wait states
Data-to-data = zero wait states
Read strobe delay = zero wait states

Timing Diagram 4-9. C Mode, Direct Slave Single Read without Wait States (32-Bit Local Bus)



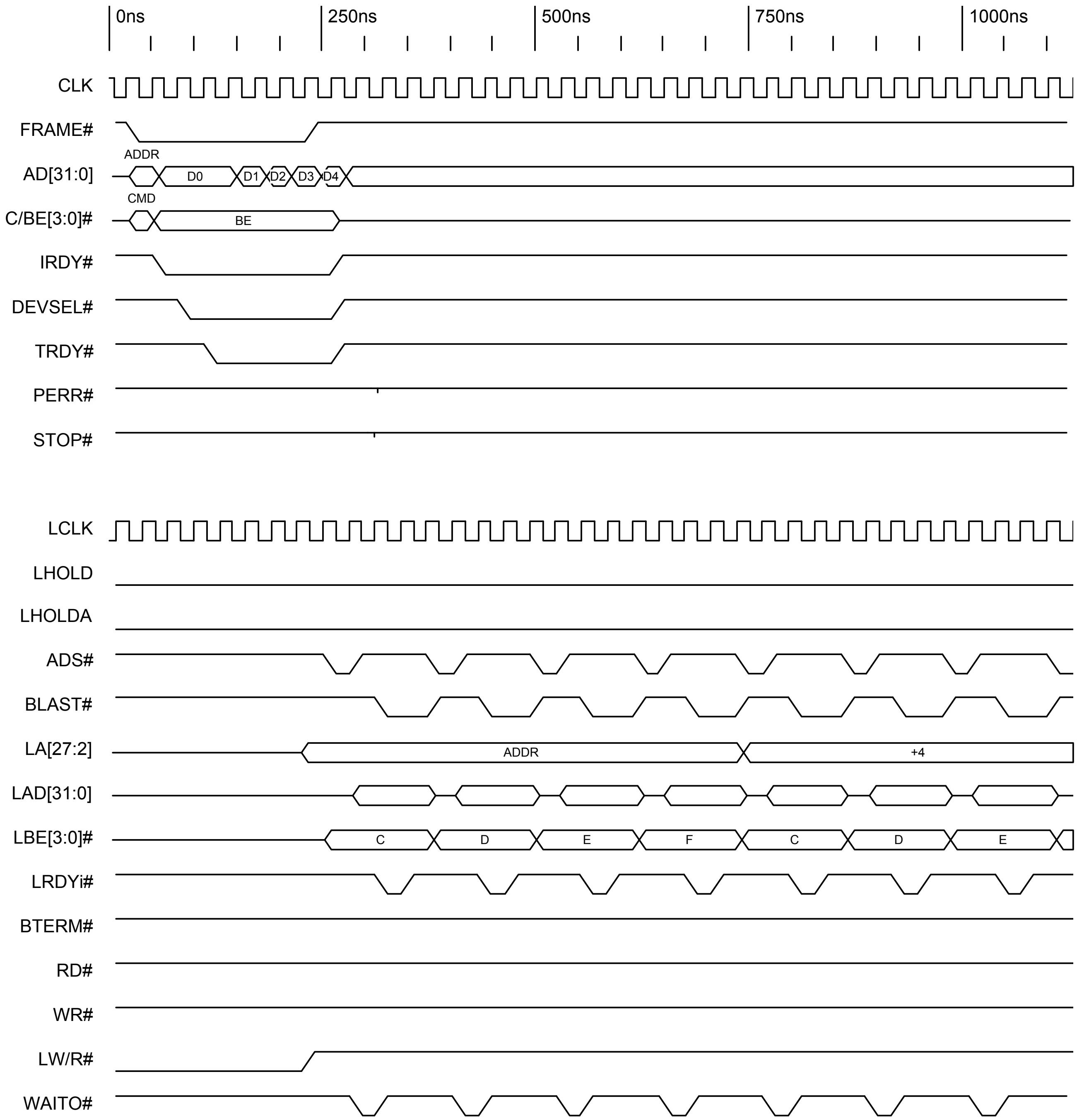
Note: Single read, 32-bit Local Bus, with wait states
Space 0 is mapped to I/O
Address-to-data = zero wait states (NRAD)
Data-to-data = zero wait states (NRDD)
Read strobe delay = zero wait states

Timing Diagram 4-10. C Mode, Direct Slave Single Read with External (LRDYi#) Wait States (32-Bit Local Bus)



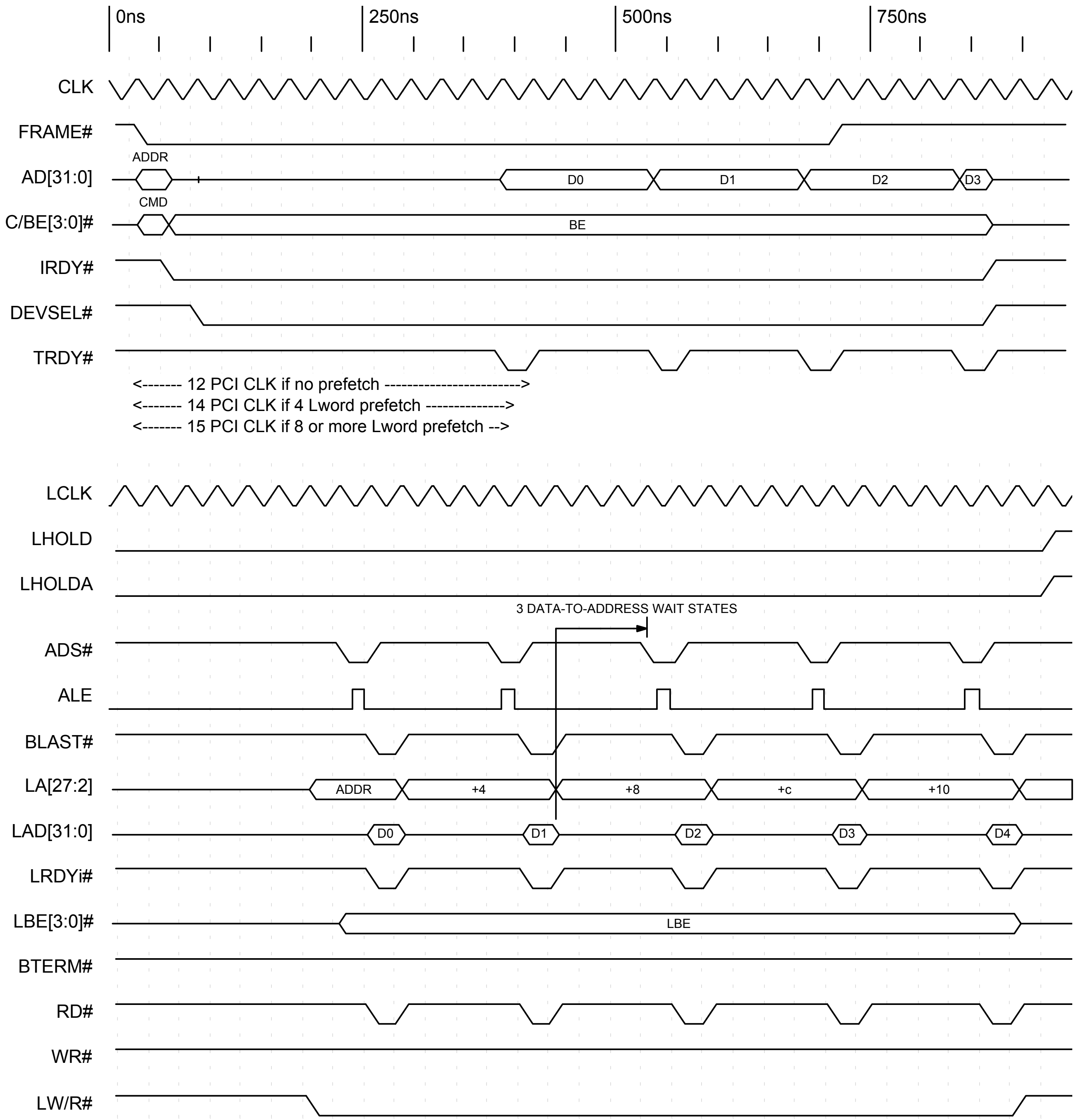
Note: Non-Burst write of four Lwords
32-bit Local Bus, BTERM# is disabled
Address-to-data = five NWAD wait states
Data-to-data = one NWDD wait state
Write strobe delay = three wait states
Write cycle hold = two wait states

Timing Diagram 4-11. C Mode, Direct Slave Non-Burst Write with Wait States (32-Bit Local Bus)



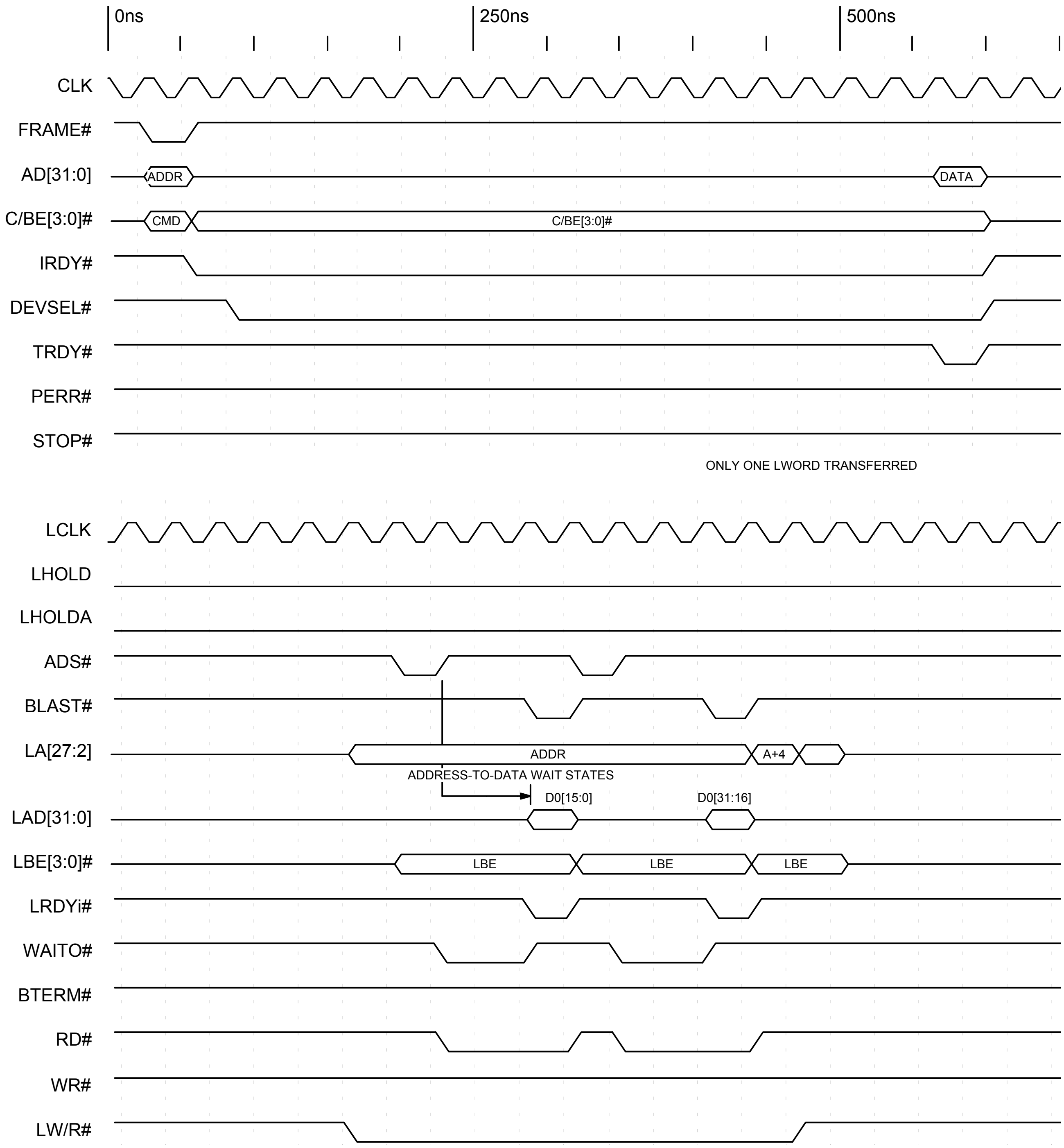
Note: Non-Burst write of five Lwords
8-bit Local Bus
Address-to-data = one NWAD wait state
Data-to-data = zero NWDD wait states
Write strobe delay = two wait states, WR# not asserted because the delay is not $\leq$ NWAD
Write hold cycle = one wait state

Timing Diagram 4-12. C Mode, Direct Slave Non-Burst Write (8-Bit Local Bus)



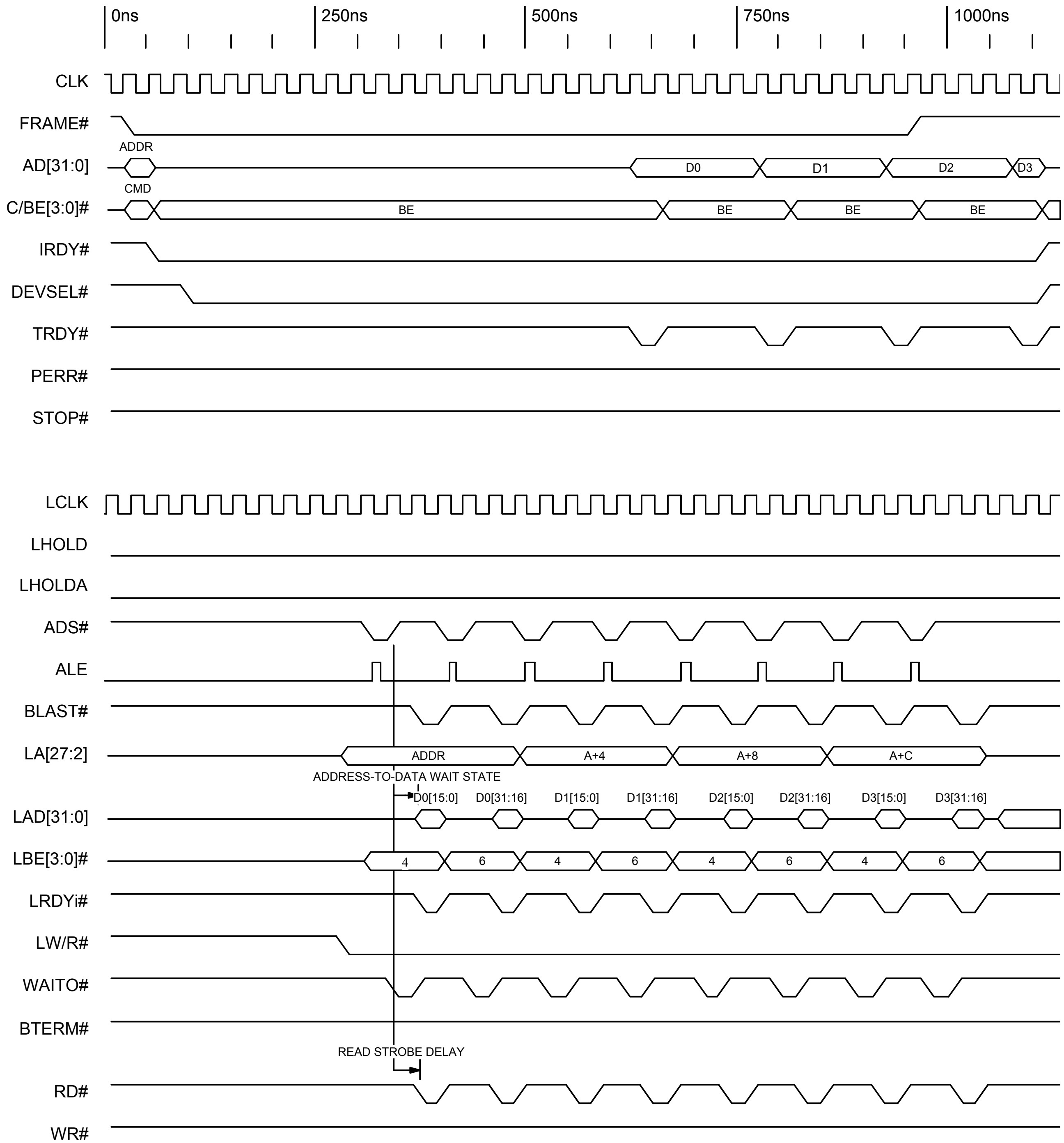
Note: Direct Slave read from Space 1
Burst disabled, BTERM# enabled
Local Bus: Little Endian, 32-bit
Data-to-address = three NXDA wait states
Write strobe delay = zero wait states
Write cycle hold = zero wait states

Timing Diagram 4-13. C Mode, Direct Slave Non-Burst Read with BTERM# Enabled (32-Bit Local Bus)



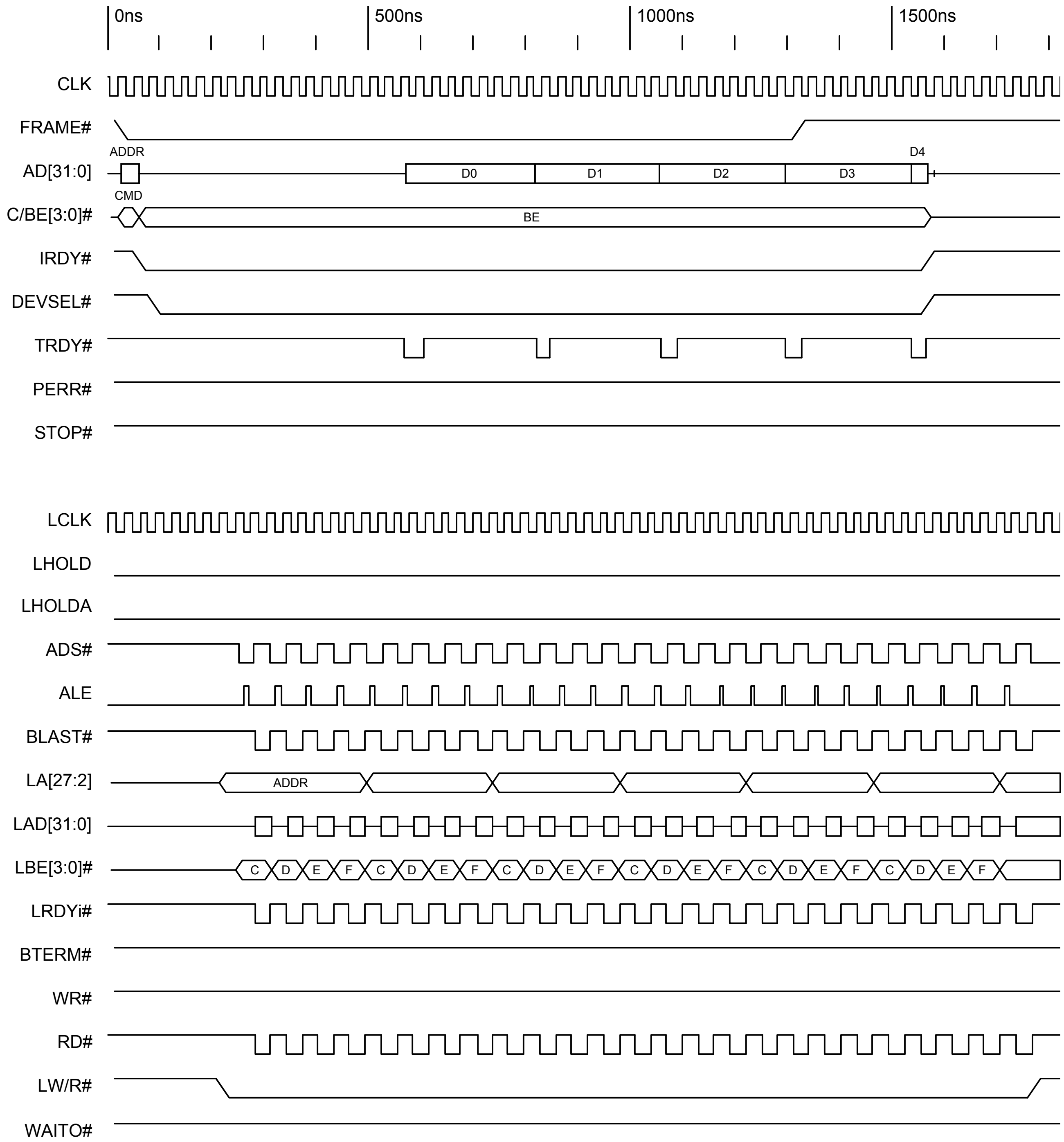
Note: Address-to-data = two NRAD wait states
Data-to-data = zero wait states
Read strobe delay = zero wait states

Timing Diagram 4-14. C Mode, Direct Slave Non-Burst Read with Unaligned PCI Address (32-Bit Local Bus)

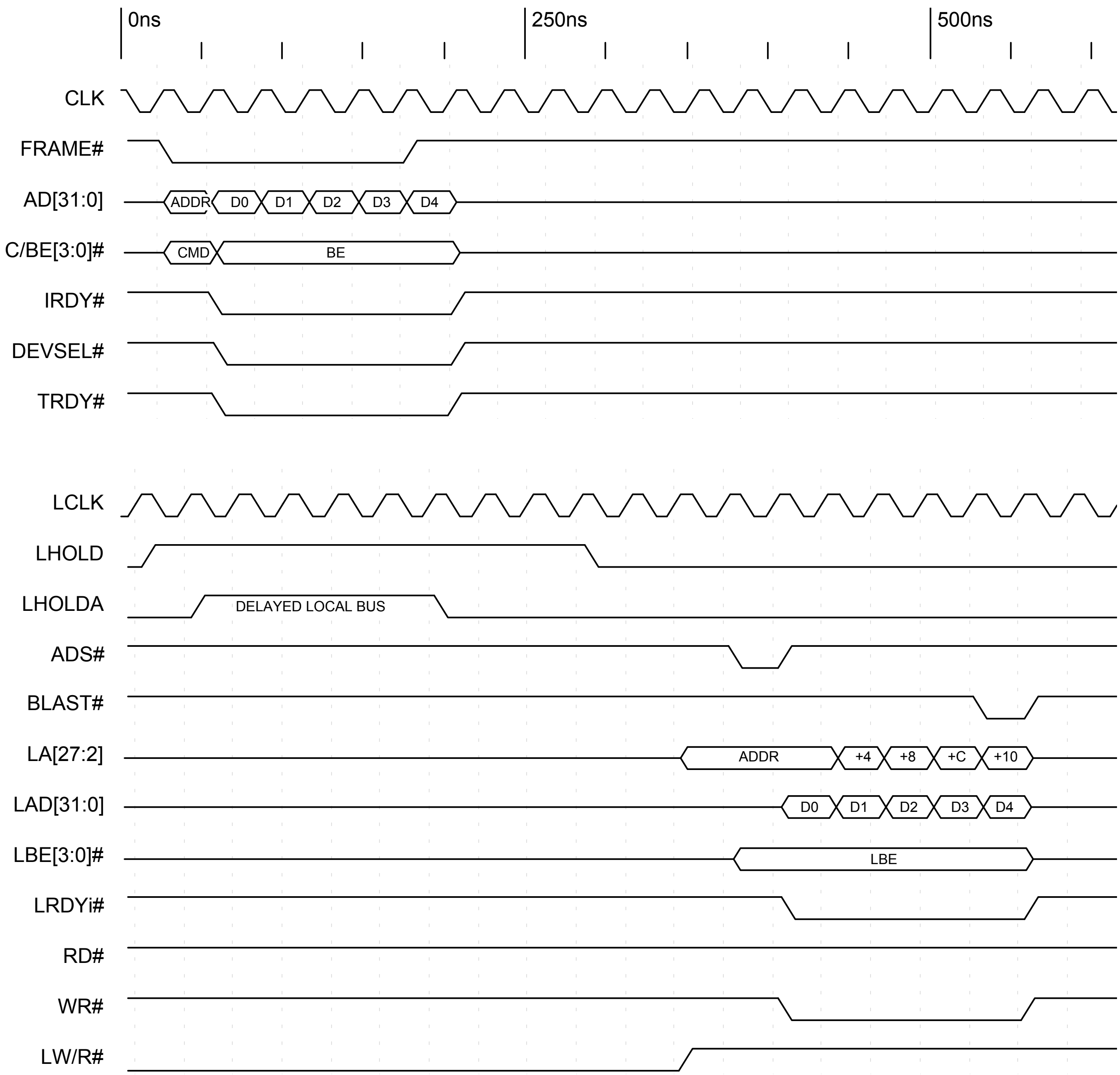


Note: 16-bit Local Bus
Non-burst read of four Lwords
Prefetch four Lwords
Address-to-data = one NRAD wait state
Data-to-data = one NRDD wait state
Read strobe delay = one wait state

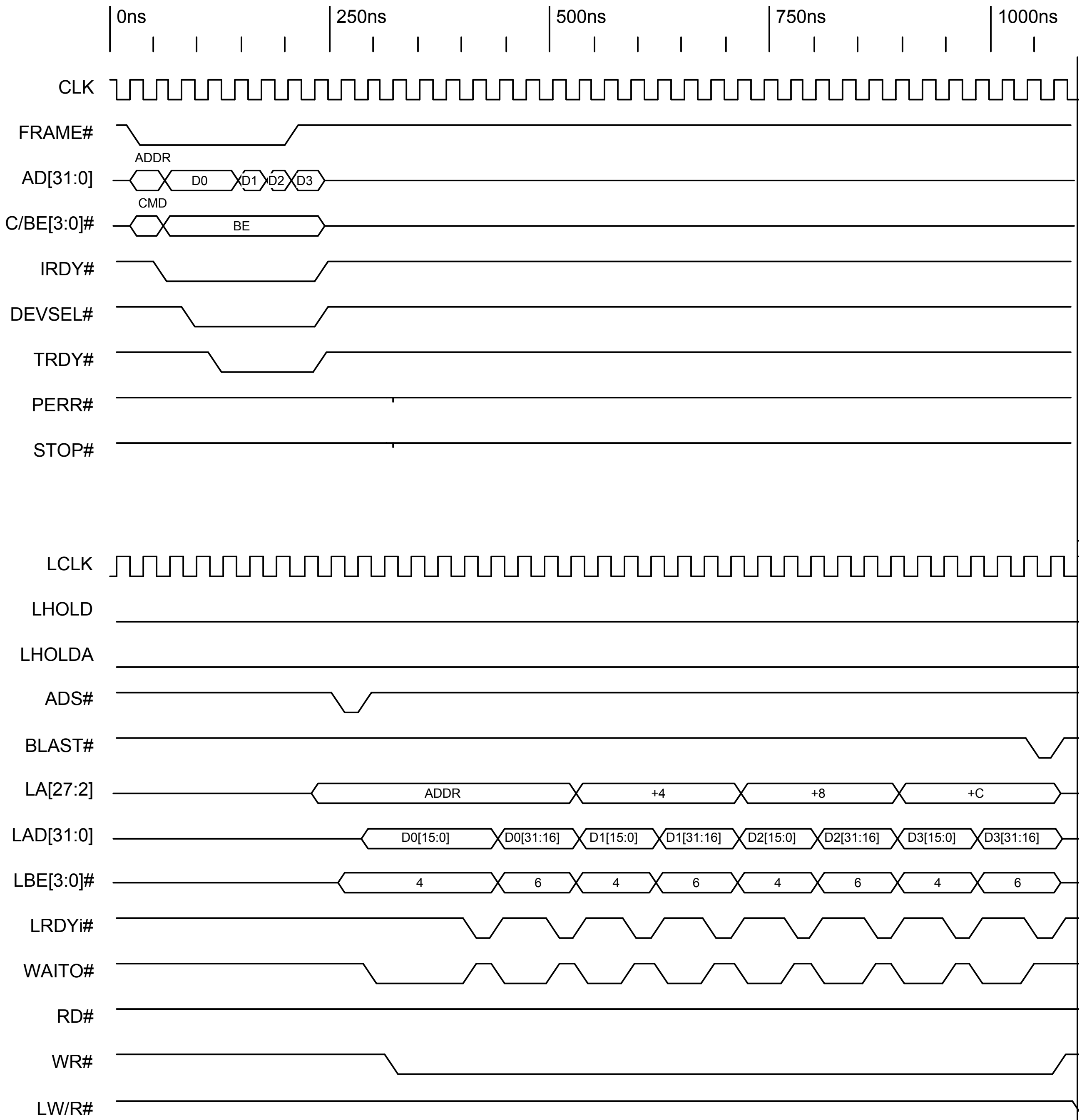
Timing Diagram 4-15. C Mode, Direct Slave Non-Burst Read with Prefetch (16-Bit Local Bus)



Timing Diagram 4-16. C Mode, Direct Slave Non-Burst Read with Continuous Prefetch (8-Bit Local Bus)

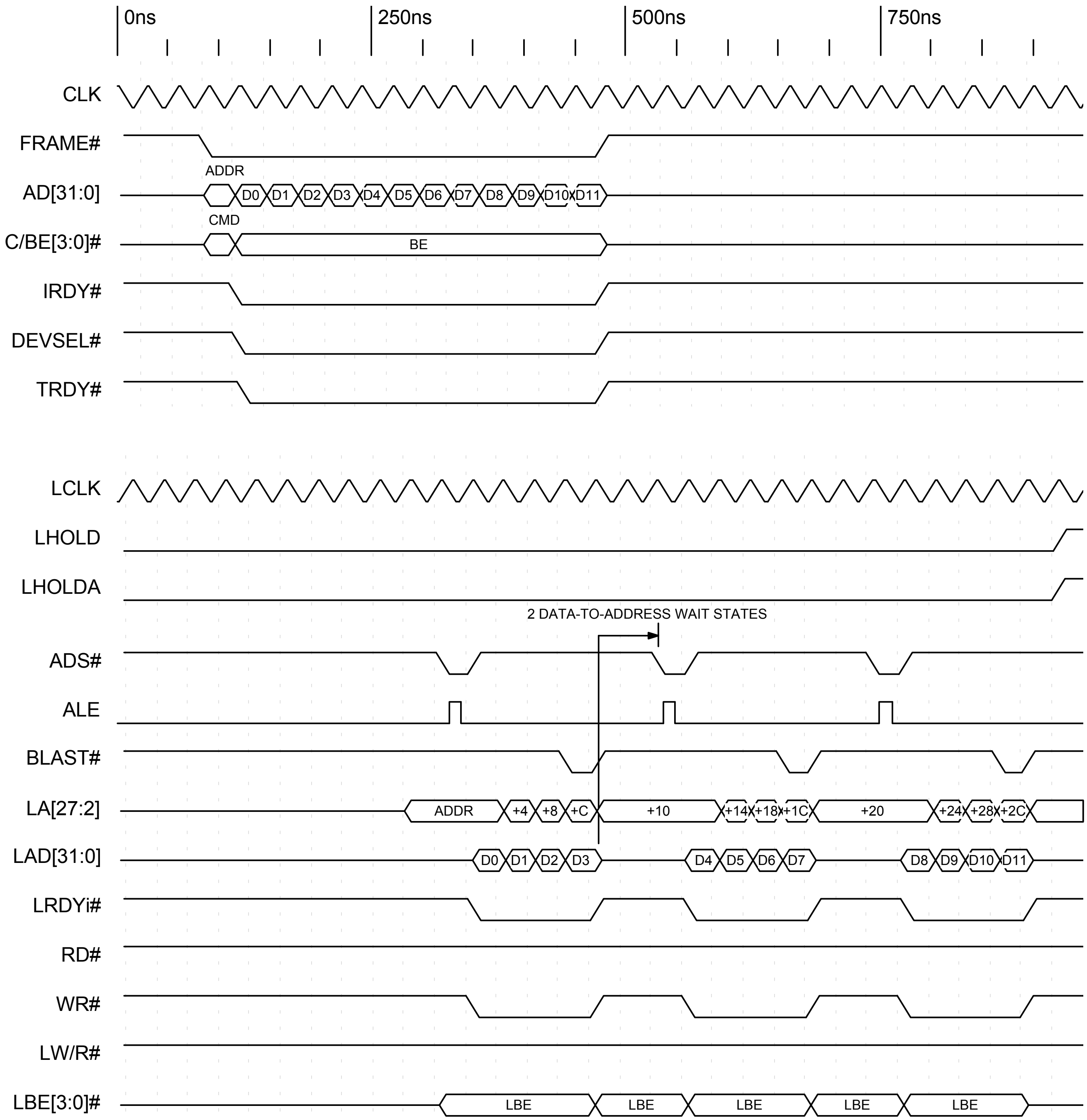


Timing Diagram 4-17. C Mode, Direct Slave Burst Write with Delayed Local Bus (32-Bit Local Bus)



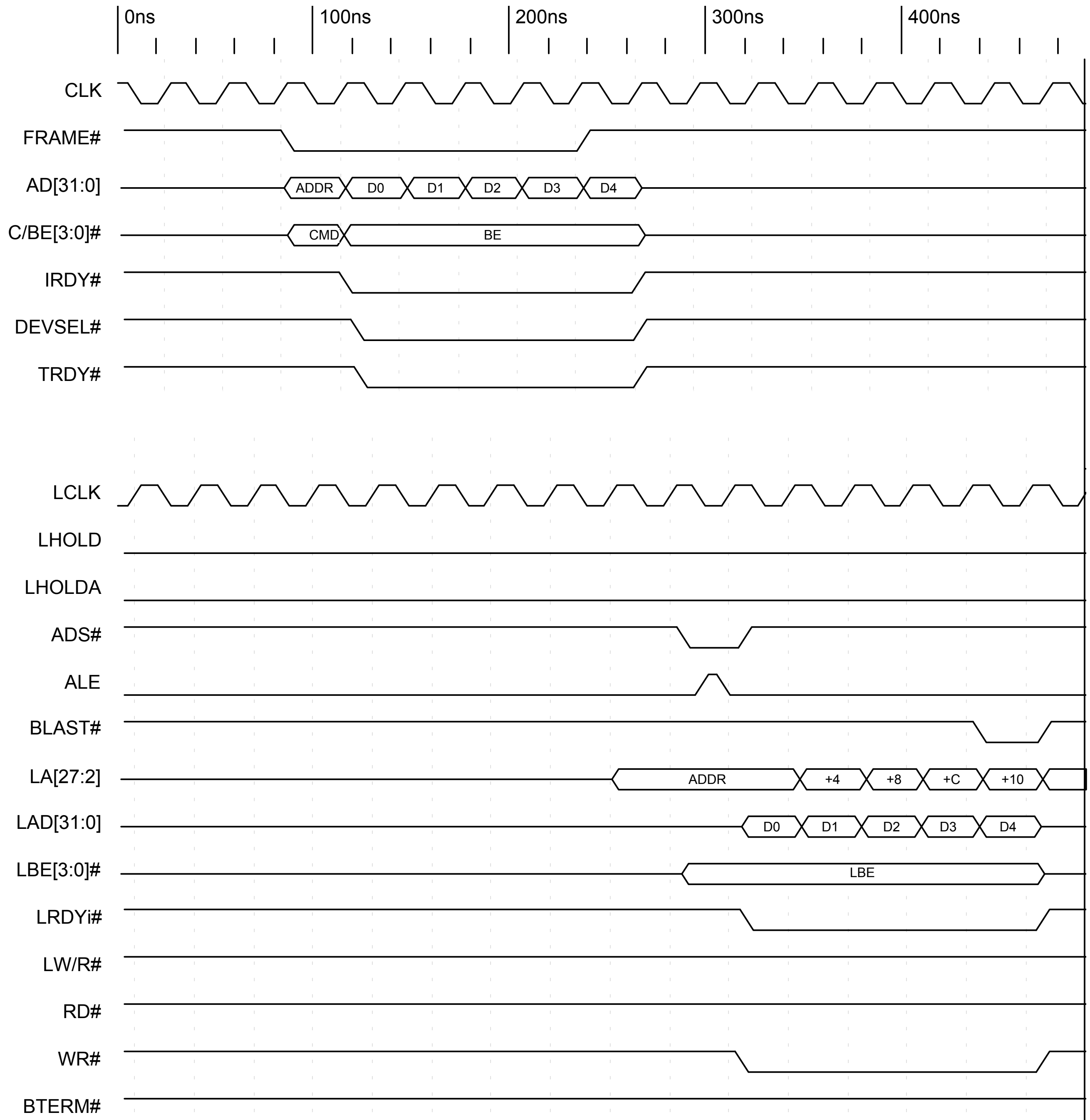
Note: Burst enabled (Burst write of four Lwords)
Address-to-data = four NWAD wait states
Data-to-data = two NWDD wait states
Write strobe delay = one wait state
Write cycle hold = zero wait states

Timing Diagram 4-18. C Mode, Direct Slave Burst Write with Wait States (16-Bit Local Bus)



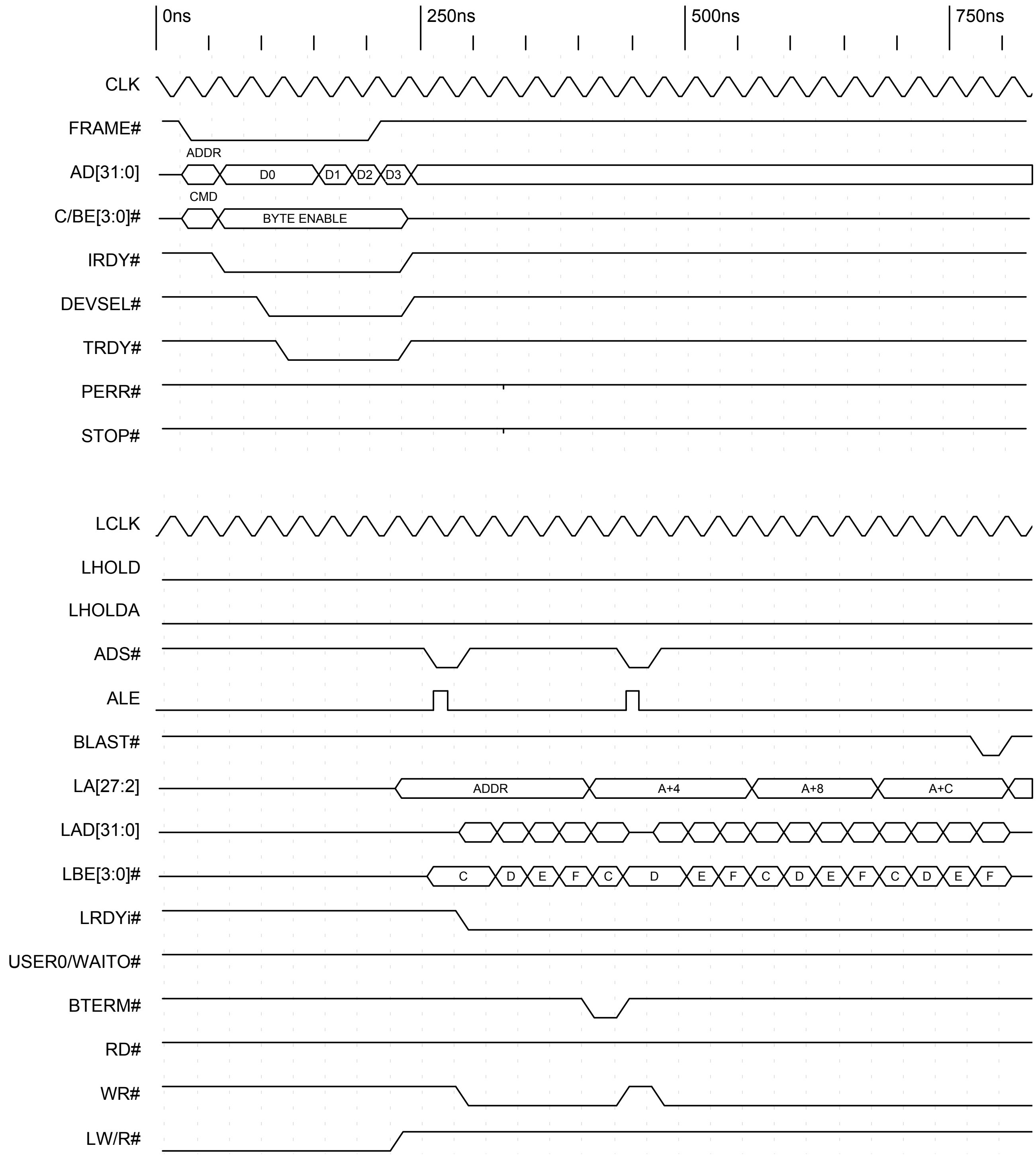
Note: Local Bus: Little Endian, 32-bit
Burst enabled (Burst write of four Lwords)
BTERM# disabled
Data-to-address = two NXDA wait states

Timing Diagram 4-19. C Mode, Direct Slave Burst Write with BTERM# Disabled and Wait States (32-Bit Local Bus)



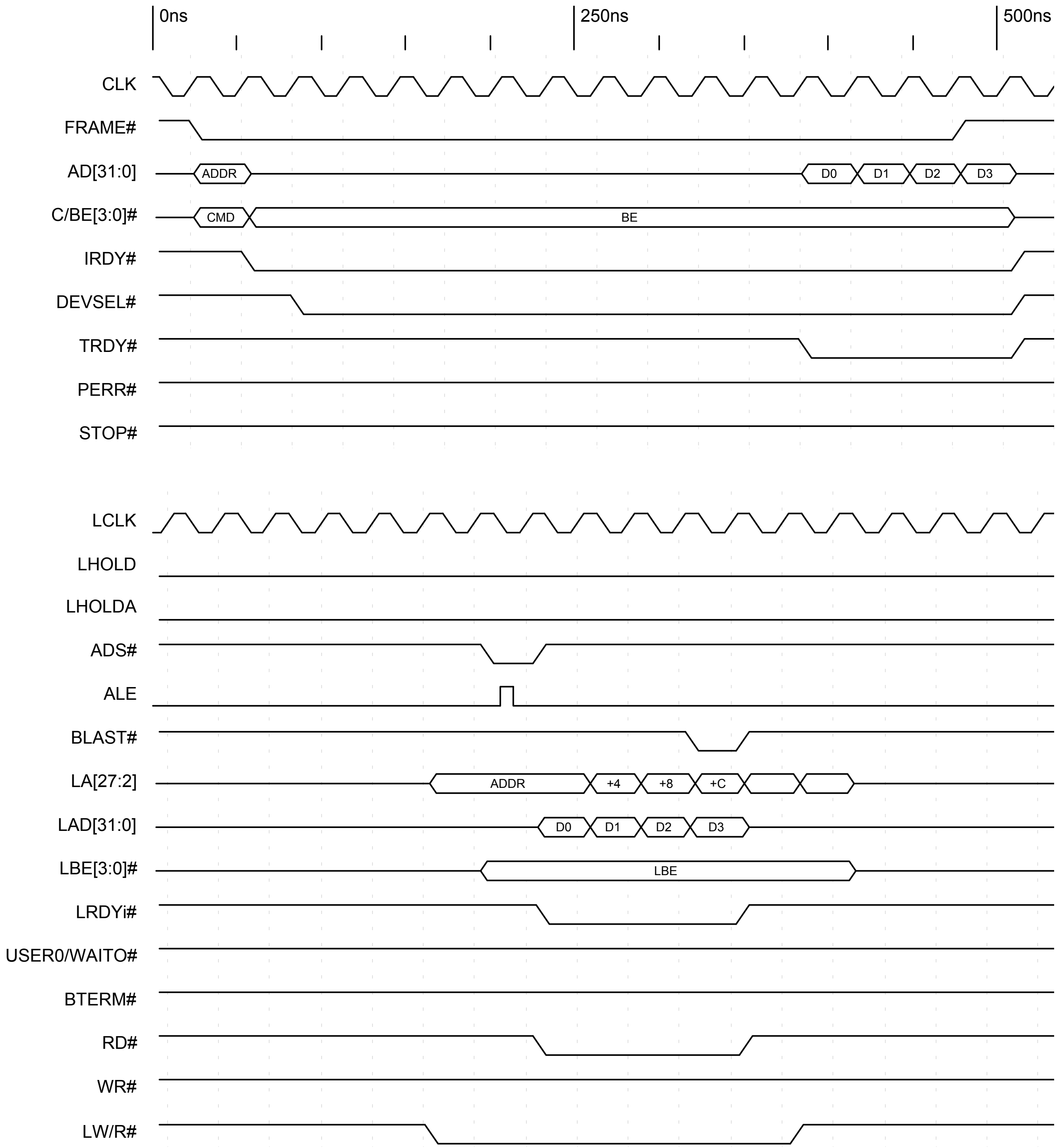
Note: Local Bus: Little Endian, 32-bit
Burst enabled (Burst write of five Lwords), BTERM# enabled
Address-to-data = zero wait states
Data-to-data = zero wait states
Write strobe delay = zero wait states
Write cycle hold = zero wait states

Timing Diagram 4-20. C Mode, Direct Slave Burst Write with BTERM# Enabled (32-Bit Local Bus)



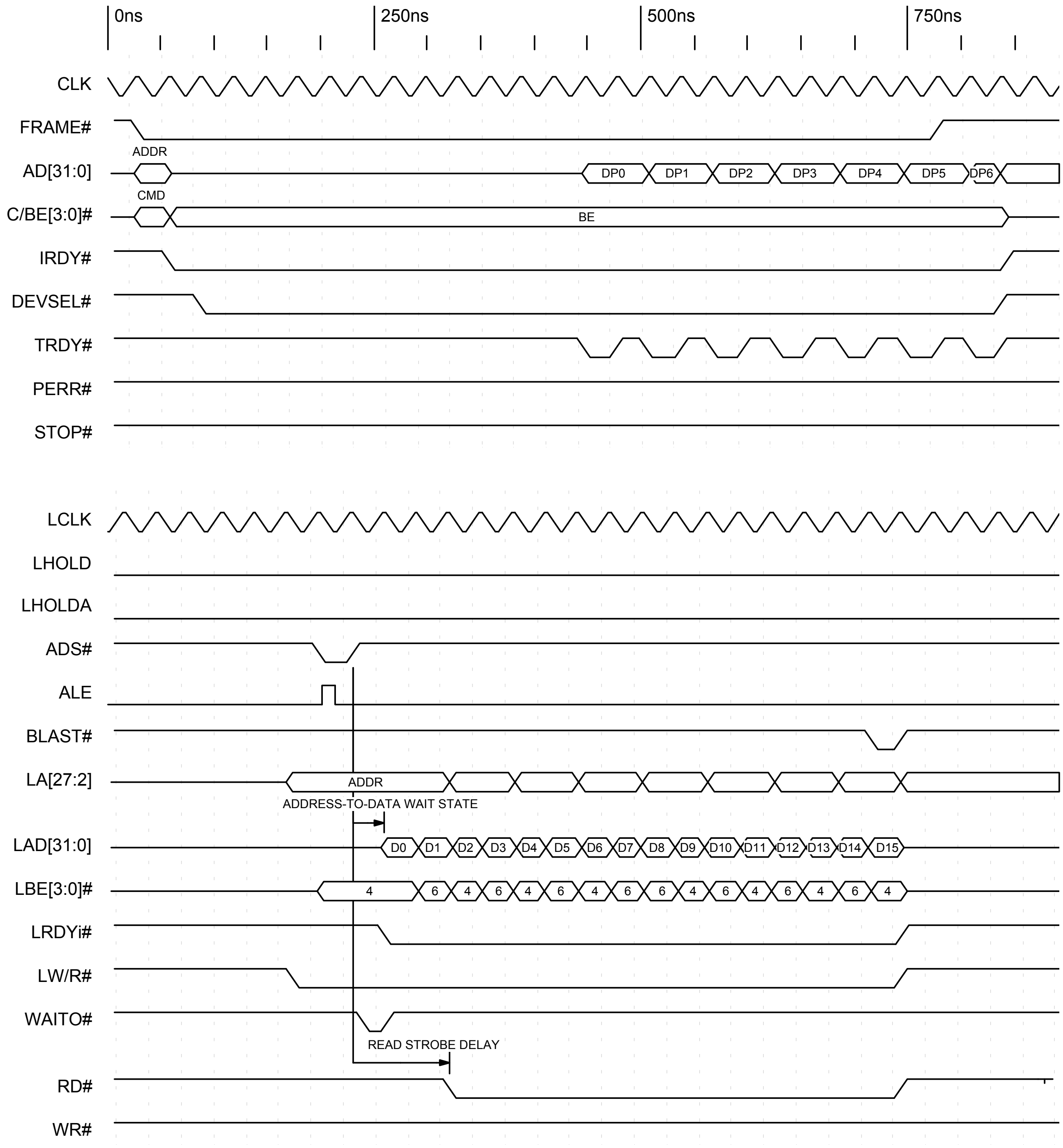
Note: Burst enabled (Burst write of four Lwords)
BTERM# enabled

Timing Diagram 4-21. C Mode, Direct Slave Burst Write with BTERM# Enabled (8-Bit Local Bus)



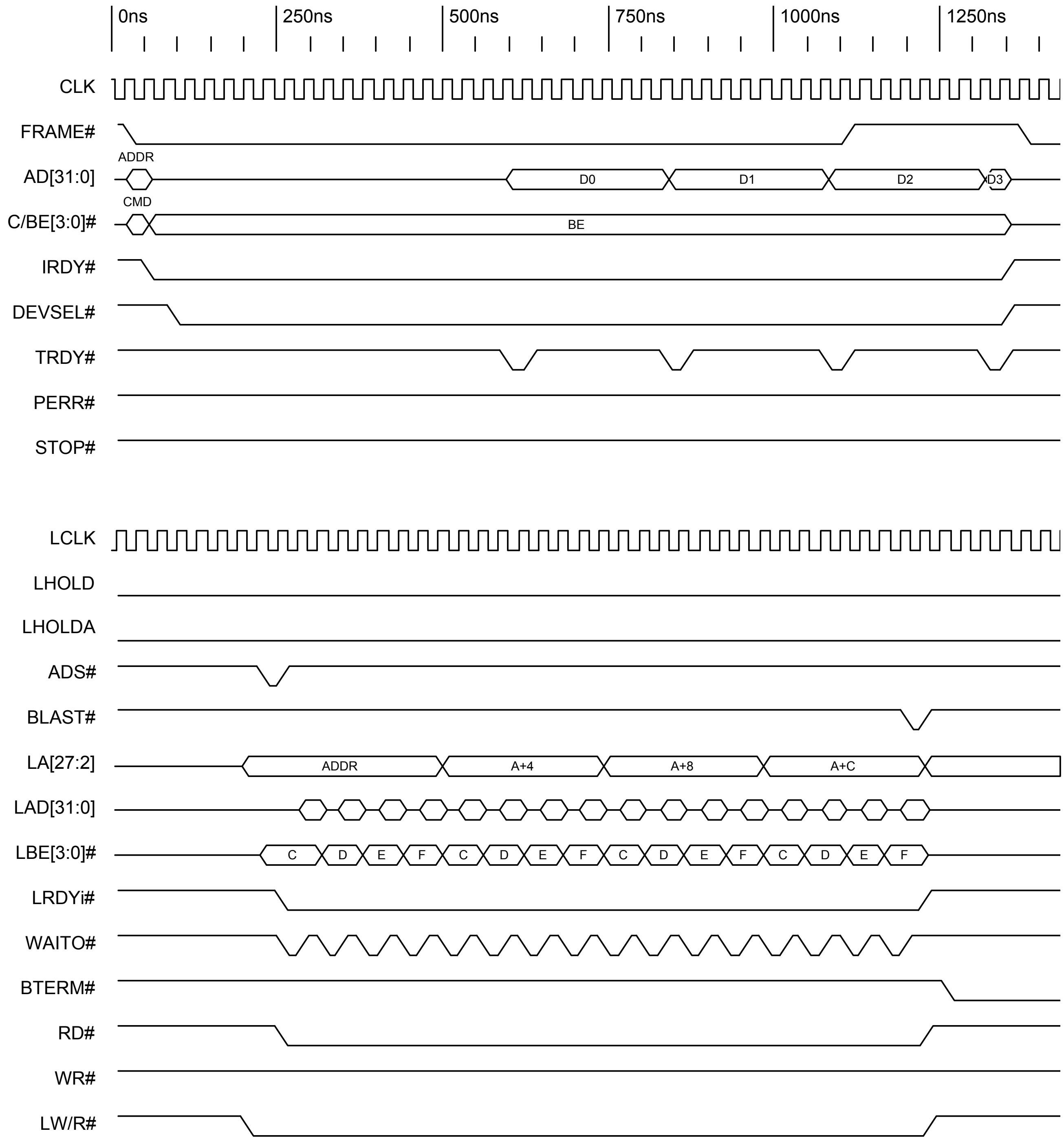
Note: Local burst
Address-to-data = zero wait states
Data-to-data = zero wait states
Read strobe delays = zero wait states

Timing Diagram 4-22. C Mode, Direct Slave Burst Read with Prefetch of Four Lwords (32-Bit Local Bus)



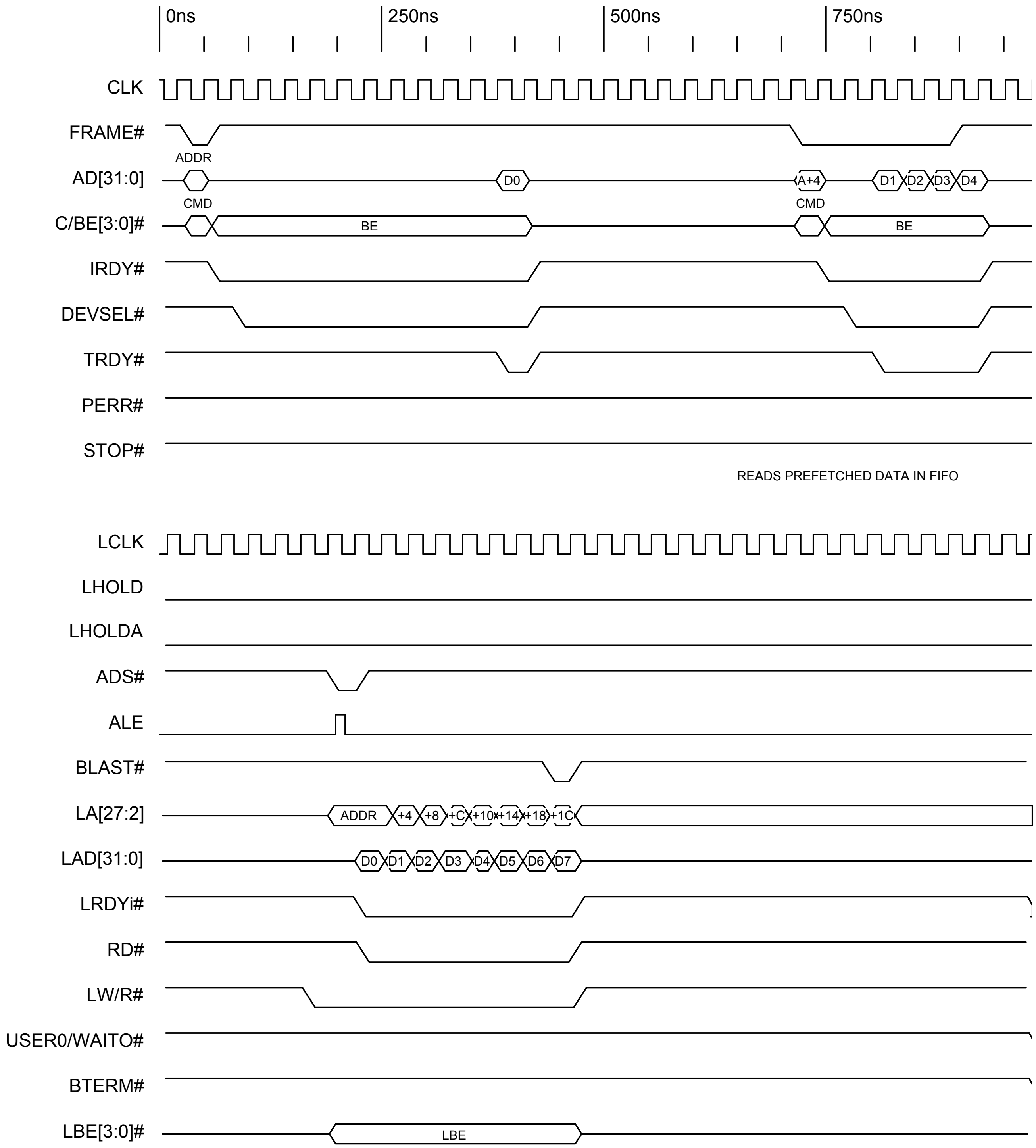
Note: Burst read eight Lwords
Address-to-data = one NRAD wait state
Data-to-data = zero wait states
Read strobe delay = three wait states

Timing Diagram 4-23. C Mode, Direct Slave Burst Read with Prefetch of Eight Lwords (16-Bit Local Bus)



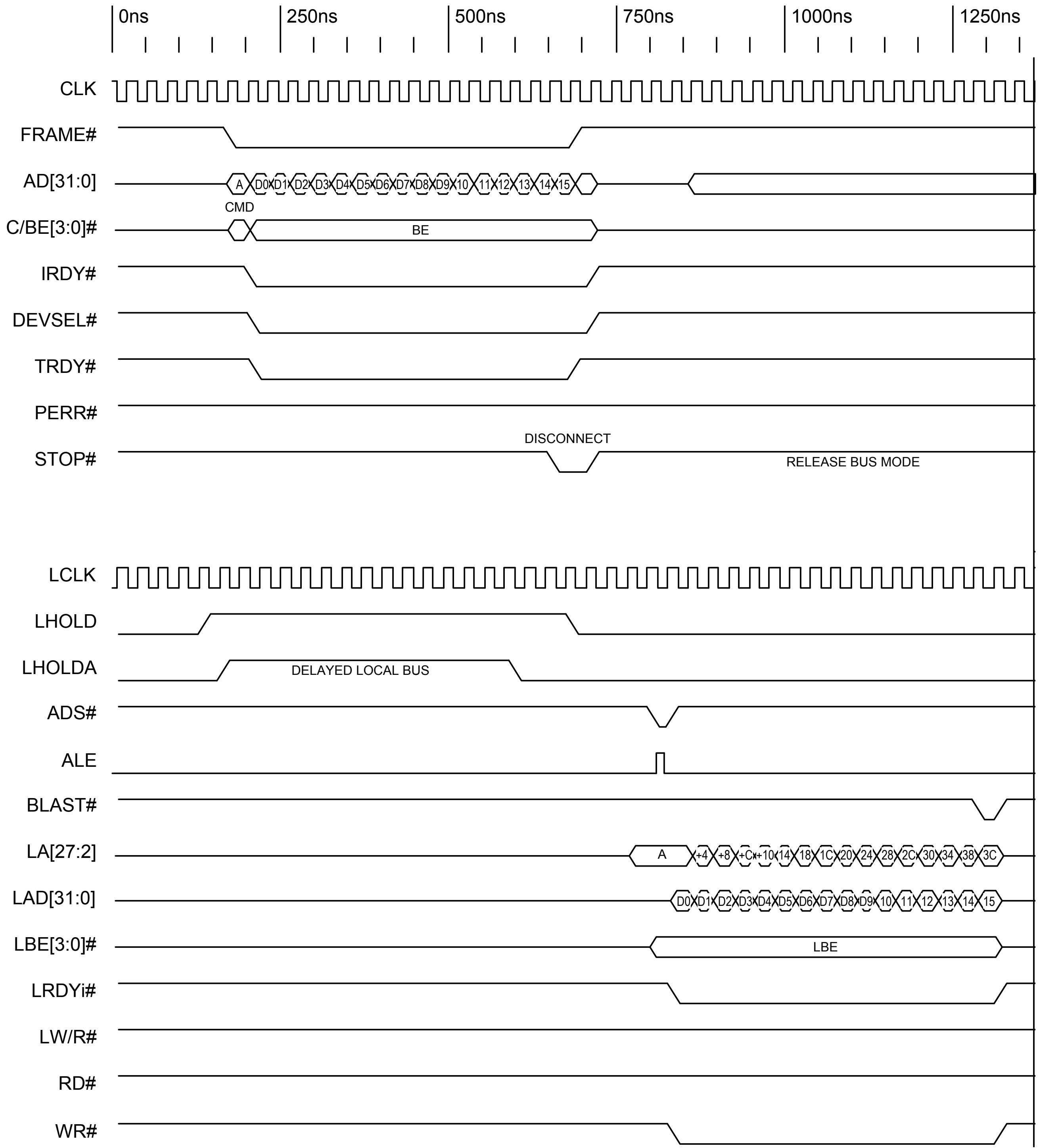
Note: Burst read four Lwords
Address-to-data = one NRAD wait state
Data-to-data = one NRDD wait state
Read strobe delay = zero wait states

Timing Diagram 4-24. C Mode, Direct Slave Burst Read with Prefetch of Four Lwords (8-Bit Local Bus)

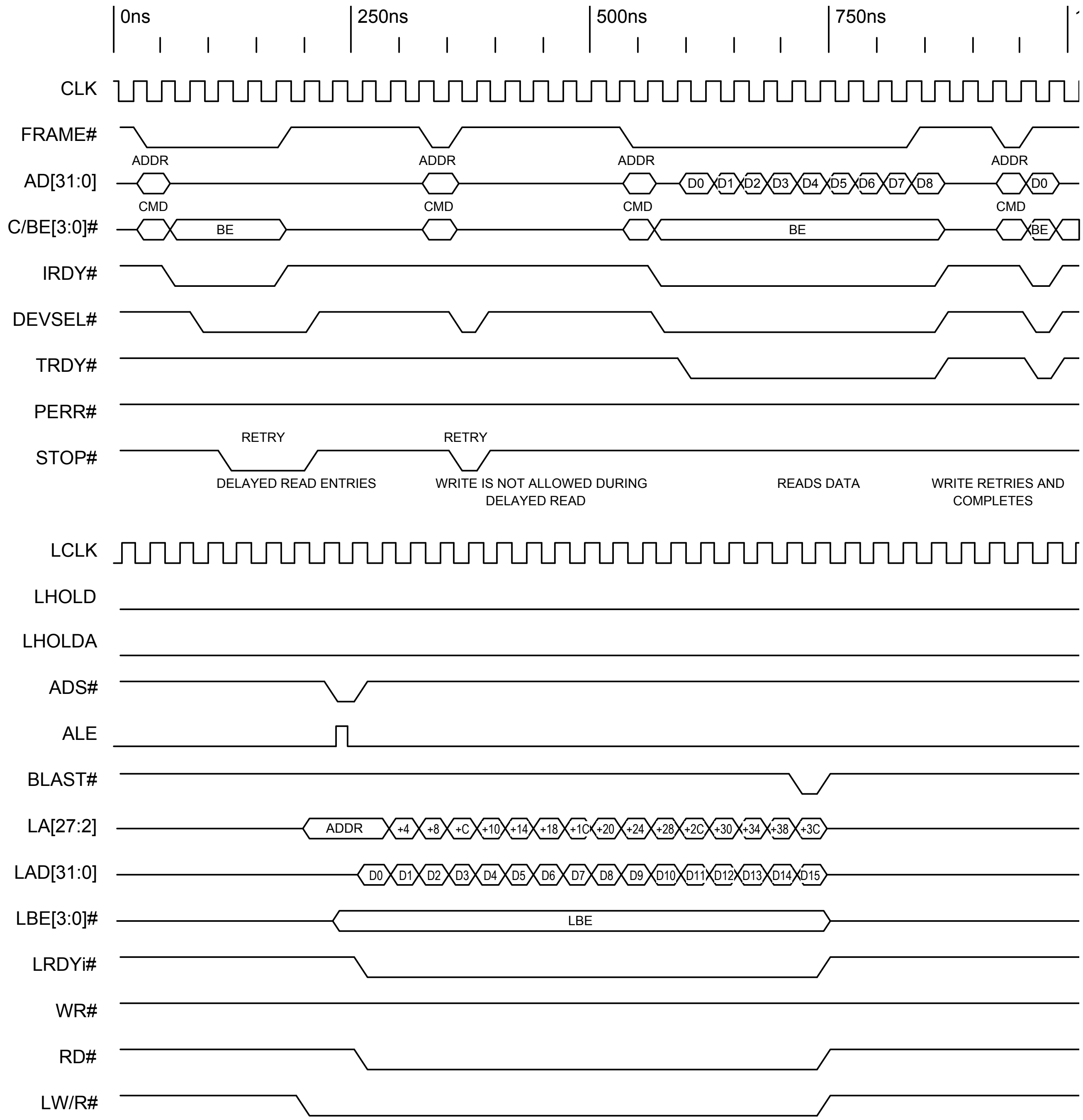


Note: Direct Slave read for Space 0 (same for Spaces 1, 2, and 3 and Expansion ROM)
Prefetch eight Lwords, 32-bit Local Bus

Timing Diagram 4-25. C Mode, Direct Slave Read with Read Ahead Mode Enabled (CNTRL[16]=1)



Timing Diagram 4-26. C Mode, Direct Slave Burst Write with PCI Write Release Bus Mode Enabled (CNTRL[18]=1)

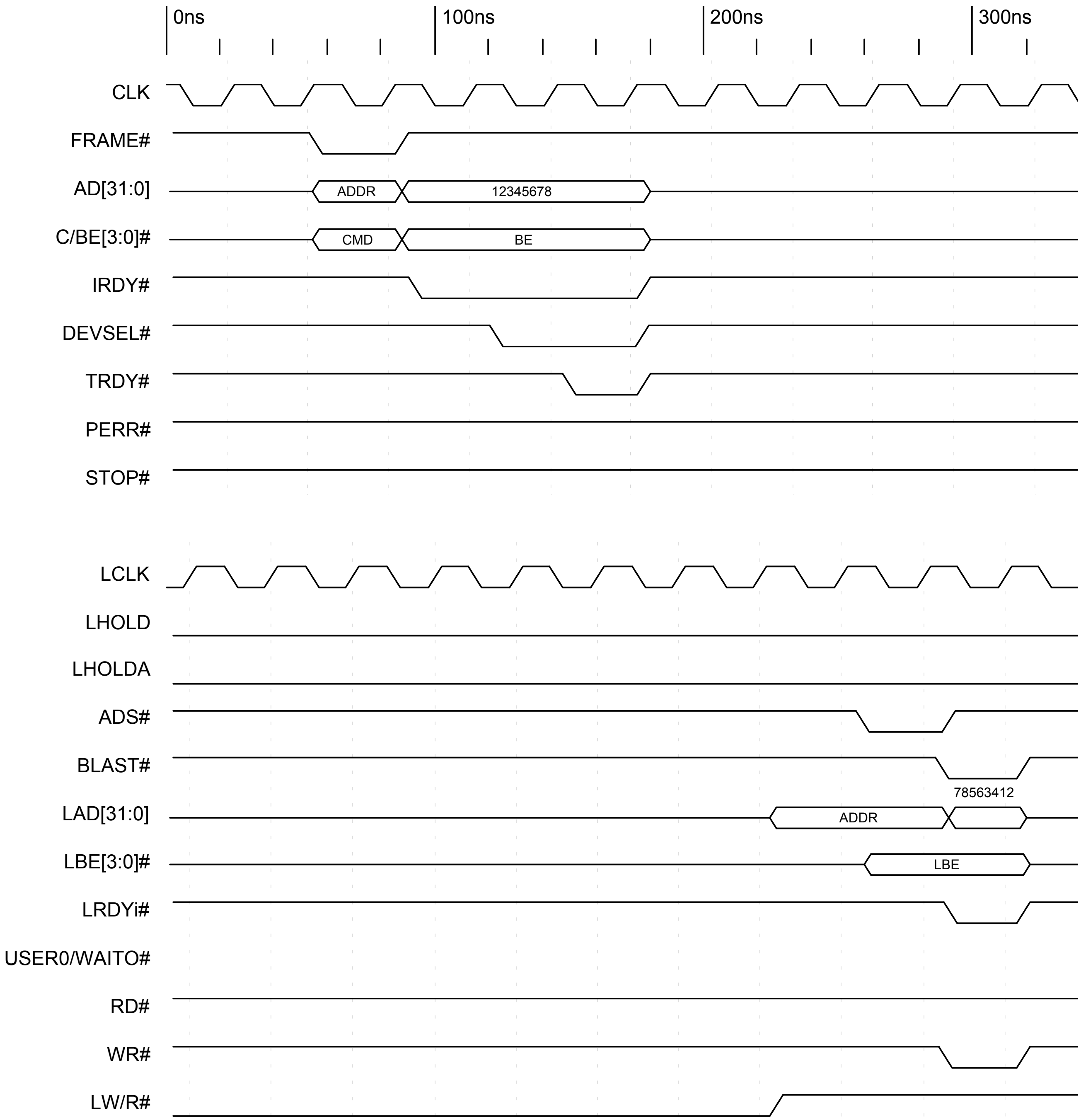


Note: Disconnect immediately for a read
Does not effect pending reads when Write cycle occurs
Does not flush the Read FIFO if PCI Read cycle completes
Force Retry on write if read is pending
De-assert TRDY# until space is available in the Direct Slave Write FIFO

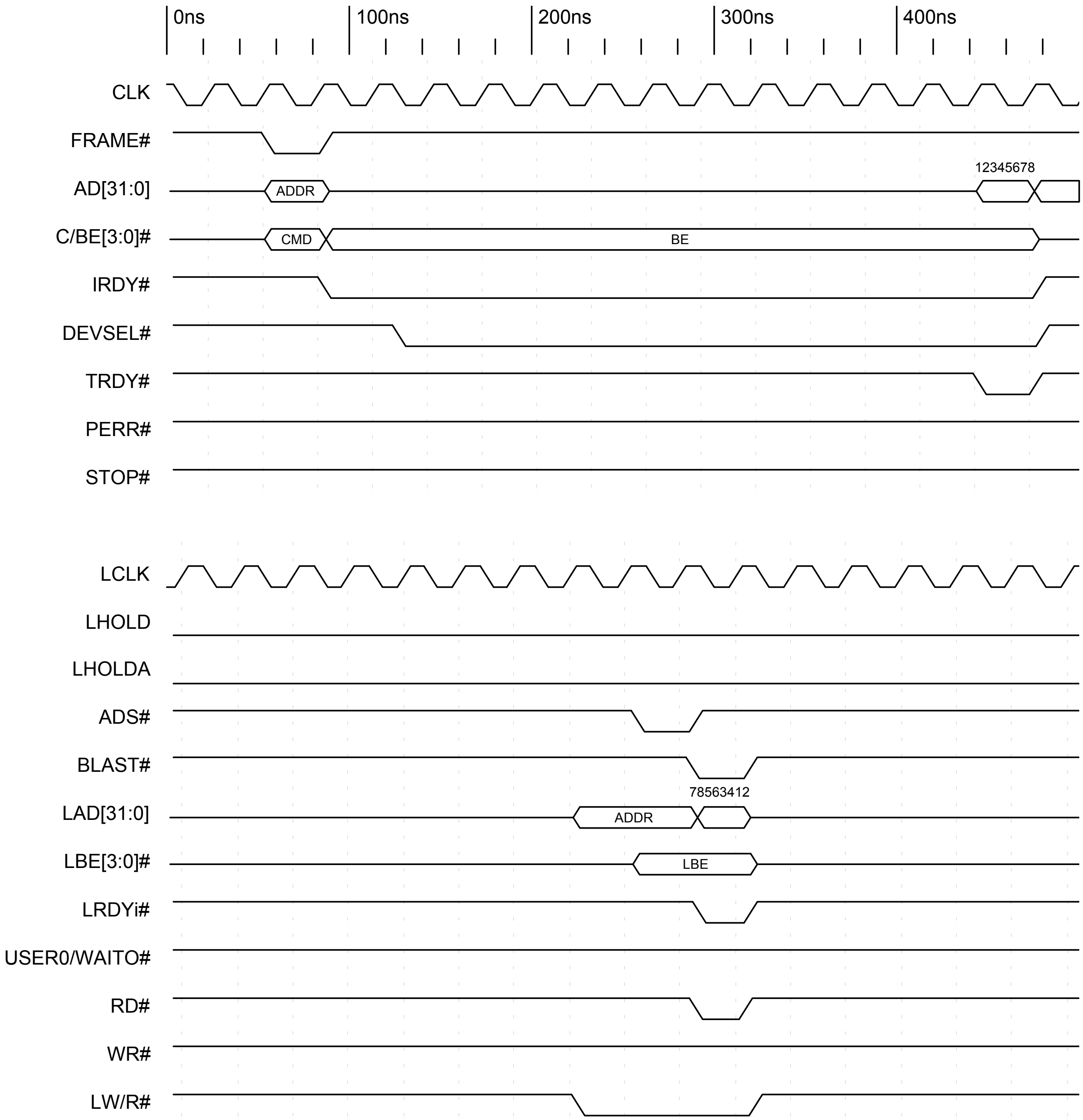
Timing Diagram 4-27. C Mode, Direct Slave Burst Read with PCI Write Release Bus Mode Disabled (PCI Write Hold Bus Mode Enabled), PCI Read No Write Mode and PCI Read No Flush Mode (Read Ahead Mode) Enabled, PCI Read with Write Flush Mode Disabled, and PCI Delayed Read Mode Enabled (CNTRL[18:14]=01101)

4—PCI Target (Direct Slave)

4.4.3 Big Endian Mode and J Mode Local Bus

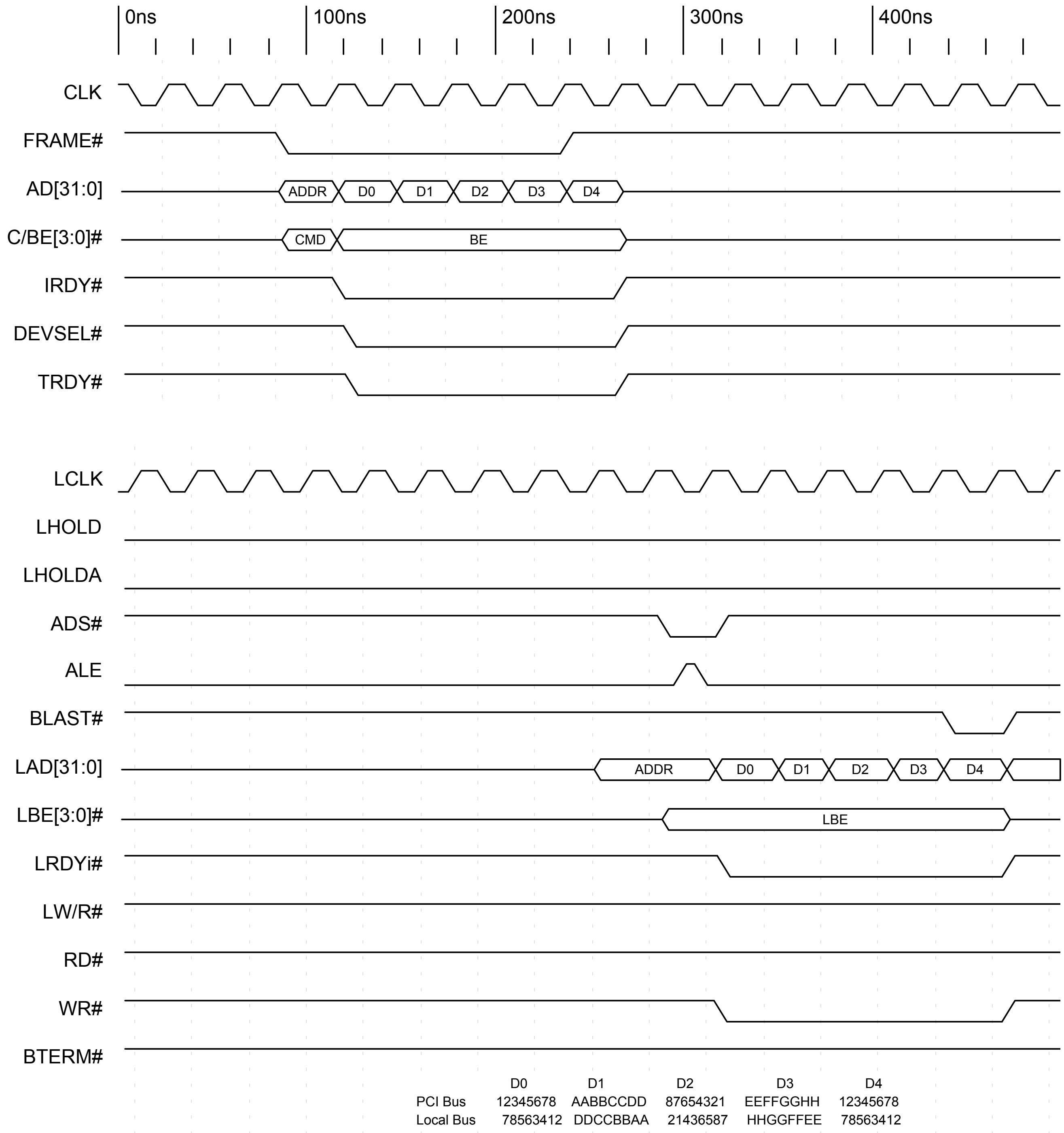


Timing Diagram 4-28. J Mode, Direct Slave Single Write, Local Bus Big Endian (32-Bit)



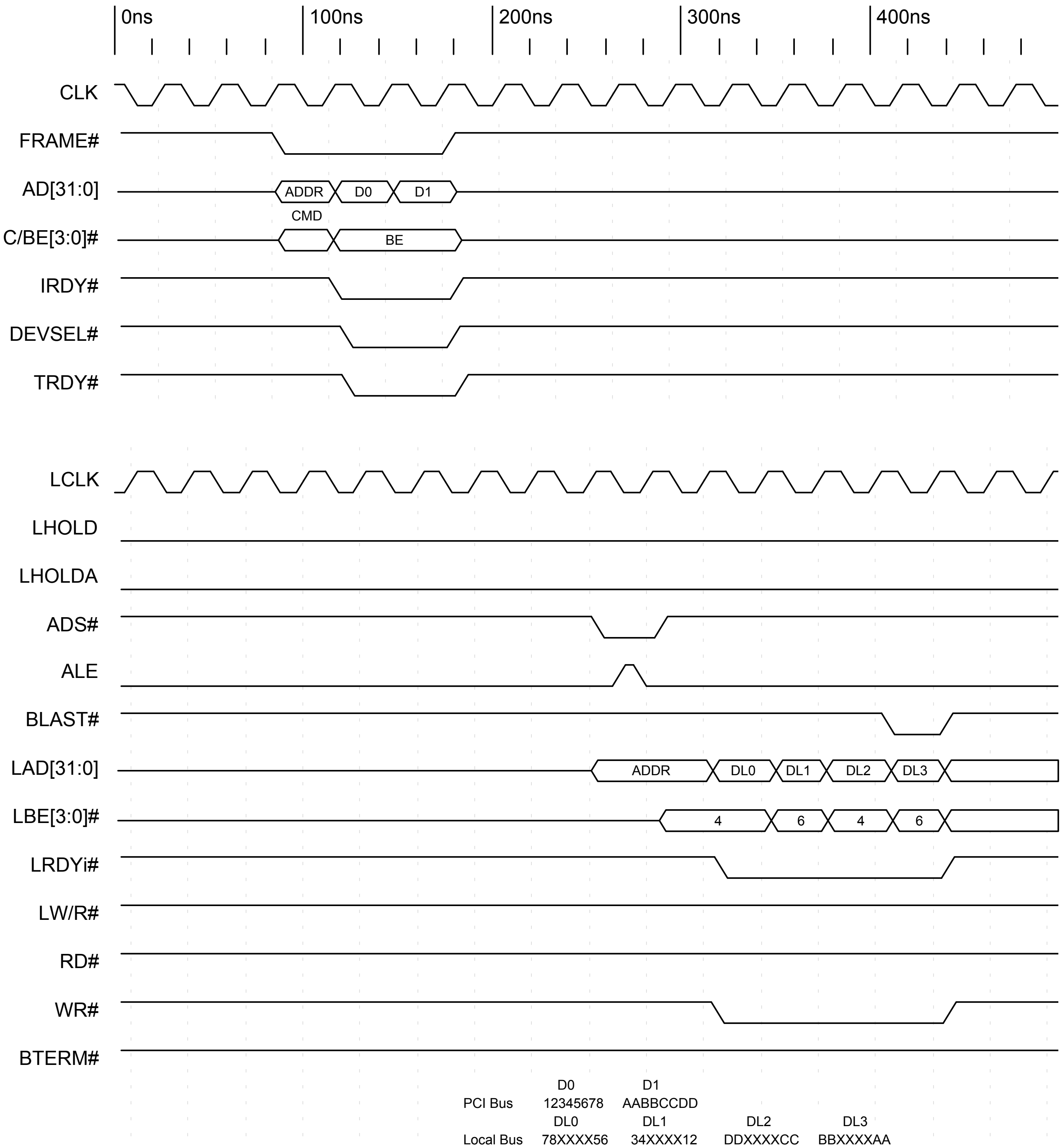
Note: Space 0 is mapped to I/O
Address-to-data = zero wait states
Data-to-data = zero wait states
Read strobe delay = zero wait states

Timing Diagram 4-29. J Mode, Direct Slave Single Read, Local Bus Big Endian (32-Bit)



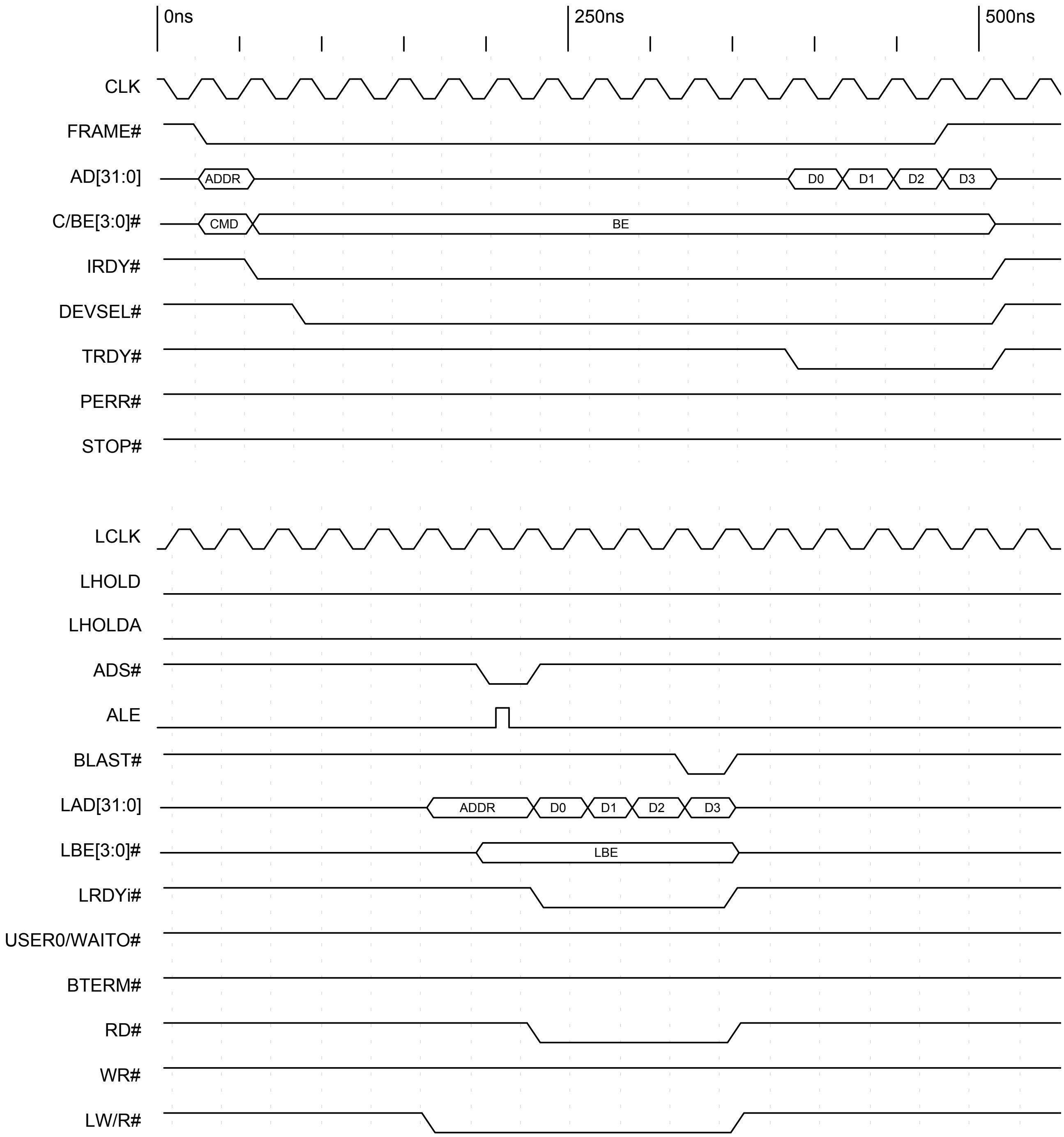
Note: Local Bus: Big Endian, 32 bit
Burst enabled (burst write of five Lwords), BTERM# enabled
Address-to-data = zero wait states (NWAD)
Write strobe delay = zero wait states
Write cycle hold = zero wait states

Timing Diagram 4-30. J Mode, Direct Slave Burst Write, Local Bus Big Endian (32-Bit)



Note: Local Bus: Big Endian, 16 bit
Burst enabled (burst write of four Lwords), BTERM# enabled
Address-to-data = zero wait states
Write strobe delay = zero wait states
Write cycle hold = zero wait states

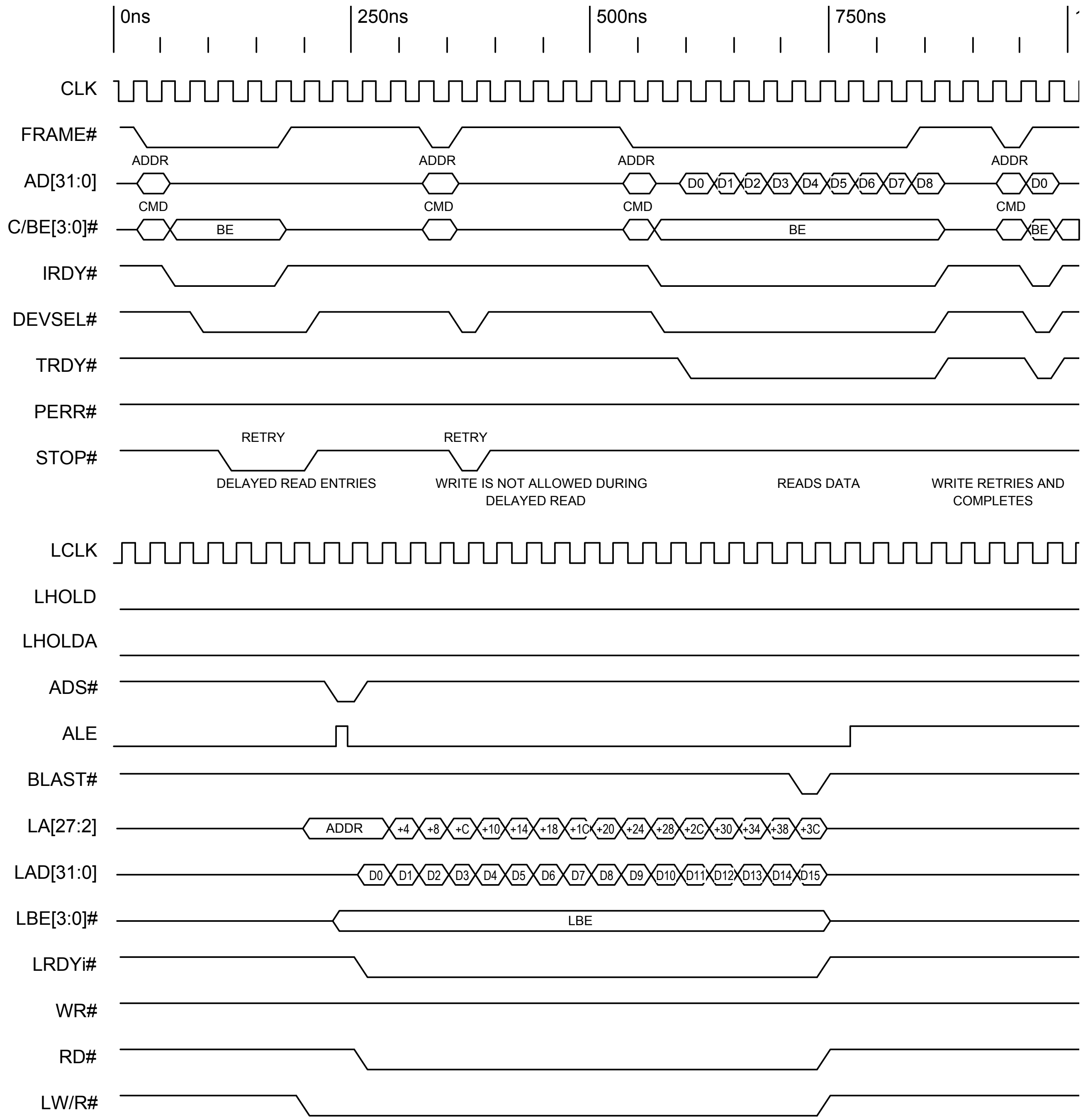
Timing Diagram 4-31. J Mode, Direct Slave Burst Write, Local Bus Big Endian (16-Bit)



	D0	D1	D2	D3
PCI Bus	12345678	AABBCCDD	87654321	EEFFGGHH
Local Bus	78563412	DDCCBBAA	21436587	HHGGFFEE

Note: Prefetch four Lwords, Local burst
Address-to-data = zero wait states (NRAD)
Data-to-data = zero wait states (NRDD)
Read strobe delay = zero wait states

Timing Diagram 4-32. J Mode, Direct Slave Burst Read, Local Bus Big Endian (32-Bit)



Note: Burst enabled (Burst read of four words)
Address-to-data = one NRAD wait state
Data-to-data = zero wait states
Read strobe delay = three wait states

Timing Diagram 4-33. J Mode, Direct Slave Burst Read, Local Bus Big Endian (16-Bit)

5 LOCAL CHIP SELECT

5.1 OVERVIEW

The PCI 9050-1 provides four chip select outputs to selectively enable devices on its Local Bus. Each active-low chip select is programmable and independent of any local address space. Without this feature, external address decoding logic is required to implement chip selects.

5.2 CHIP SELECT BASE ADDRESS REGISTERS

There are four Chip Select Base Address registers. These registers control the four chip select pins on the PCI 9050-1. [*For example*, Chip Select 0 Base Address register (CS0BASE) controls CS0#, Chip Select 1 Base Address register (CS1BASE) controls CS1#, and so forth.]

The Chip Select Base Address registers serve three purposes:

1. To enable or disable chip select functions within the PCI 9050-1. If enabled, the chip select signal is active if the Local Bus Address falls within the address specified by the range and base address. If disabled, the chip select signal is not active.
2. To set the range of the Local Bus Addresses for which the chip select signal(s) is active.
3. To set the Local Base Address, at which the range starts.

The three rules used to program the Chip Select Base Address registers are as follows:

1. Range must be a power of 2 (only the most significant bit is 1).
2. Base address must be a multiple of the range or 0.
3. Address range must be encompassed by one or more Local Address Spaces. Otherwise, the chip select decoder does not see addresses which have not been claimed by the PCI 9050-1 on behalf of a Local Address Space, and a chip select is not asserted.

Each 28-bit Chip Select Base Address register is programmed, as listed in the following table.

Table 5-1. Chip Select Base Address Register Signal Programming

MSB=27						LSB=0
XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXY

The *Y* bit (bit 0) enables or disables the chip select signal. *X* bits are used to determine the range and base address of where the CS# pin is asserted. To program the base and range, the *X* bits are set as follows:

- Device length or range is specified by the first bit set above the *Y* bit. Determined by setting a bit in the register, calculated by shifting the range value (a power of 2) one bit to the right (range divided by 2).
- Base Address is determined by the bit(s) set above the range bit. The address is not shifted from its original value. The base address uses all bits in the register above (to the left of) the range bit, and none of the bits in the register at or below (to the right of) the range bit.

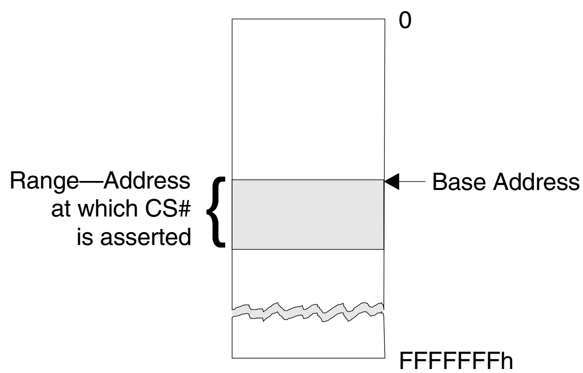


Figure 5-1. Chip Select Base Address and Range

5—Local Chip Select

5.3 PROCEDURE FOR USING CHIP SELECT BASE ADDRESS REGISTERS

The following describes the procedure for using the Chip Select Base Address registers.

1. Determine the range in hex. The range must be a power of 2 (only the highest order bit is set).
2. Set a bit in the Chip Select Base Address register to specify the range. Calculate this value by shifting the range value one bit to the right (range divided by 2). Only one bit may be set to encode the range.
3. Determine the base address. The base address must be a multiple of the range [the base address cannot contain ones (1) at or below (to the right of) the encoded range bit]. Set the base address directly into the bits above the range bit. The base address is not shifted from its original value.
4. Set the Enable bit (bit 0) in the Chip Select Base Address register to 1.

5.3.1 Chip Select Base Address Register Use Example

A 16K SRAM device is attached to the Local Bus and a chip select is provided. The base address is specified to be 24000h. The following figure illustrates this example.

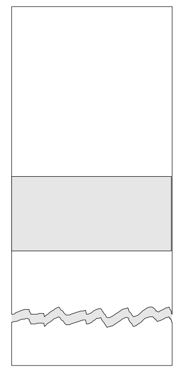


Figure 5-2. Memory Map Example

1. Determine the range in hex and divide the value by 2 (*for example*, 16K is equivalent to 4000h, leaving the range encoding at 2000h).
2. Determine the base address (*for example*, 24000h). Verify that the base address does not overwrite the range bit or any lower bits.
3. Set the base address into the bits above the range encoding. The base address is not shifted from its original value.
4. Set the Enable bit (bit 0).

The following is a complete example of setting the Chip Select Base Address register with a range of 4000h, a base address of 24000h, and enabled:

MSB=27						LSB=0
0000	0000	0010	0110	0000	0000	0001

6 PCI/LOCAL INTERRUPTS AND USER I/O

6.1 OVERVIEW

There are two local interrupt pins and a register bit that can trigger PCI interrupt INTA#. Each pin has a global Enable or Disable bit. In addition, each pin is programmable to a different polarity and is level-sensitive. Each interrupt has a status bit indicating which interrupt source is active. The Software Interrupt bit (INTCSR[7]) can be set to trigger the INTA# PCI interrupt.

6.2 INTERRUPTS

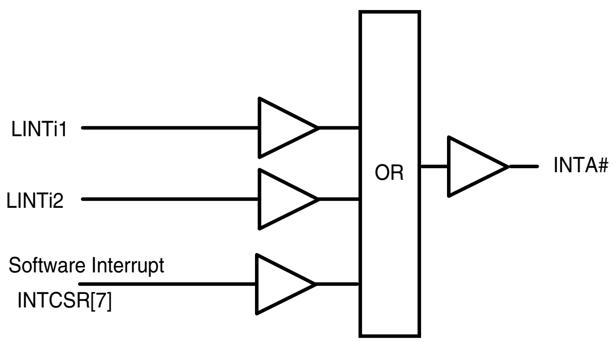


Figure 6-1. Interrupt and Error Sources

6.2.1 PCI Interrupts (INTA#)

A PCI 9050-1 PCI interrupt (INTA#) can be asserted by Local Interrupt Input 2 or 1 (LINTi[2:1]), which are described in the next section.

INTA#, or individual sources of an interrupt, can be enabled or disabled with the PCI 9050-1 Interrupt Control/Status register (INTCSR). This register also provides the interrupt status of each interrupt source.

A software interrupt can be enabled or disabled with INTCSR[7].

The PCI 9050-1 PCI Bus interrupt is a level output. Disabling an interrupt enable bit or clearing the cause(s) of the interrupt can clear an interrupt.

6.2.2 Local Interrupt Input (LINTi[2:1])

The PCI 9050-1 provides two Local interrupts, LINTi[2:1]. The Local interrupts can be used to generate a PCI interrupt. LINTi[2:1] support different polarity, programmable through the Interrupt Control/ Status register (INTCSR[4, 1], respectively), and are level sensitive.

6.2.3 All Modes PCI SERR# (PCINMI)

The PCI 9050-1 asserts a SERR# pulse if Parity Error Response is enabled (PCICR[6]=1) and it detects an address or data parity error.

The SERR# output can be enabled or disabled with the SERR# Enable bit (PCICR[8]).

6.3 USER I/O

The PCI 9050-1 supports four user I/O pins, USER[3:0]. All are multiplexed with other functional pins—USER0/WAITO#, USER1/LLOCKo#, USER2/ CS2#, and USER3/CS3#. Pin configuration is defined by bits in the CNTRL register. The default functionality for each of these pins is USER*x*. Default I/O configuration for all USER[3:0] pins is input.

It is recommended that unused USER I/O pins be configured as outputs, rather than the default setting as inputs; otherwise, input pins should be pulled to a known state.

7 REGISTERS

7.1 REGISTER ADDRESS MAPPING

Table 7-1. PCI Configuration Registers

PCI Configuration Register Address	To ensure software compatibility with other versions of the PCI 9050-1 family and to ensure compatibility with future enhancements, write 0 to all unused bits. 31 24	23 16	15 8	7 0	PCI Writable	Serial EEPROM Writable
00h	Device ID		Vendor ID		N	Y
04h	Status		Command		Y	N
08h	Class Code			Revision ID	N	Y[31:8]
0Ch	Built-In Self Test	Header Type	PCI Bus Latency Timer	Cache Line Size	Y[7:0]	N
10h	PCI Base Address 0 for Memory Accesses to Local Configuration Registers				Y	N
14h	PCI Base Address 1 for I/O Accesses to Local Configuration Registers				Y	N
18h	PCI Base Address 2 for Memory Accesses to Local Address Space 0				Y	N
1Ch	PCI Base Address 3 for Memory Accesses to Local Address Space 1				Y	N
20h	PCI Base Address 4 for Memory Accesses to Local Address Space 2				Y	N
24h	PCI Base Address 5 for Memory Accesses to Local Address Space 3				Y	N
28h	Cardbus CIS Pointer ***(Not Supported)***				N	N
2Ch	Subsystem ID		Subsystem Vendor ID		N	Y
30h	PCI Expansion ROM Base Address				Y	N
34h	***Reserved***				N	N
38h	***Reserved***				N	N
3Ch	Maximum Latency ***(Not Supported)***	Minimum Grant ***(Not Supported)***	Interrupt Pin	Interrupt Line	Y[7:0]	Y[15:8]

Table 7-2. Local Configuration Registers

PCI (Offset from Local Base Address)	To ensure software compatibility with other versions of the PCI 9050 family and to ensure compatibility with future enhancements, write "0" to all unused bits. 31 … 0	PCI Writable	Serial EEPROM Writable
00h	Local Address Space 0 Range	Y	Y
04h	Local Address Space 1 Range	Y	Y
08h	Local Address Space 2 Range	Y	Y
0Ch	Local Address Space 3 Range	Y	Y
10h	Expansion ROM Range	Y	Y
14h	Local Address Space 0 Local Base Address (Remap)	Y	Y
18h	Local Address Space 1 Local Base Address (Remap)	Y	Y
1Ch	Local Address Space 2 Local Base Address (Remap)	Y	Y
20h	Local Address Space 3 Local Base Address (Remap)	Y	Y
24h	Expansion ROM Local Base Address (Remap)	Y	Y
28h	Local Address Space 0 Bus Region Descriptors	Y	Y
2Ch	Local Address Space 1 Bus Region Descriptors	Y	Y
30h	Local Address Space 2 Bus Region Descriptors	Y	Y
34h	Local Address Space 3 Bus Region Descriptors	Y	Y
38h	Expansion ROM Bus Region Descriptors	Y	Y
3Ch	Chip Select 0 Base Address	Y	Y
40h	Chip Select 1 Base Address	Y	Y
44h	Chip Select 2 Base Address	Y	Y
48h	Chip Select 3 Base Address	Y	Y
4Ch	Interrupt Control/Status	Y	Y
50h	User I/O, Direct Slave Response, Serial EEPROM, and Initialization Control	Y	Y

7.2 PCI CONFIGURATION REGISTERS

All registers may be written to or read from using Byte, Word, or Lword accesses.

Register 7-1. (PCIIDR; 00h) PCI Configuration ID

Bit	Description	Read	Write	Value after Reset
15:0	**Vendor ID.** Identifies manufacturer of device. Defaults to the PCI SIG-issued Vendor ID of PLX, if blank or no serial EEPROM is present.	Yes	Serial EEPROM	10B5h
31:16	**Device ID.** Identifies particular device. Defaults to PLX part number for PCI interface chip if blank or no serial EEPROM is present.	Yes	Serial EEPROM	9050h

Register 7-2. (PCICR; 04h) PCI Command

Bit	Description	Read	Write	Value after Reset
0	**I/O Space.** Value of 1 allows the device to respond to I/O space accesses. Value of 0 disables the device from responding to I/O space accesses.	Yes	Yes	0
1	**Memory Space.** Value of 1 allows the device to respond to Memory Space accesses. A value of 0 disables the device from responding to Memory Space accesses.	Yes	Yes	0
2	**Master Enable.** ***Not Supported.***	Yes	No	0
3	**Special Cycle.** ***Not Supported.***	Yes	No	0
4	**Memory Write/Invalidate.** ***Not Supported.***	Yes	No	0
5	**VGA Palette Snoop.** ***Not Supported.***	Yes	No	0
6	**Parity Error Response.** Value of 0 indicates a parity error is ignored and operation continues. Value of 1 indicates parity error response is enabled [PERR# and SERR#, if SERR# is enabled (PCICR[8]=1)]. Parity error is always signaled in PCISR[15].	Yes	Yes	0
7	**Wait Cycle Control.** Controls whether the device does address/data stepping. Value of 0 indicates the device never does stepping. Value of 1 indicates the device always does stepping. ***Note:*** *Hardwired to 0.*	Yes	No	0
8	**SERR# Enable.** Value of 1 enables the SERR# driver. Value of 0 disables the SERR# driver.	Yes	Yes	0
9	**Fast Back-to-Back Enable.** Indicates what type of fast back-to-back transfers a Master can perform on a bus. Value of 1 indicates fast back-to-back transfers can occur to any agent on the bus. Value of 0 indicates fast back-to-back transfers can occur only to the same agent as the previous cycle.	Yes	No	0
15:10	***Reserved*.**	Yes	No	0h

Register 7-3. (PCISR; 06h) PCI Status

Bit	Description	Read	Write	Value after Reset
6:0	***Reserved.***	Yes	No	0h
7	**Fast Back-to-Back Capable.** Value of 1 indicates the adapter can accept fast back-to-back transactions. Value of 0 indicates the adapter cannot accept fast back-to-back transactions.	Yes	No	1
8	**Master Data Parity Error Detected.** ***Not Supported.***	Yes	No	0
10:9	**DEVSEL Timing**. Indicates timing for DEVSEL# assertion. Value of 01 is medium.	Yes	No	01
11	**Signaled Target Abort.** Value of 1 indicates the PCI 9050-1 signaled a Target Abort. Value of 1 clears the bit (0).	Yes	Yes/Clr	0
12	**Received Target Abort.** Value of 1 indicates the PCI 9050-1 received a Target Abort signal. ***Not Supported.***	Yes	No	0
13	**Received Master Abort.** Value of 1 indicates the PCI 9050-1 received a Master Abort signal. ***Not Supported.***	Yes	No	0
14	**Signaled System Error.** Value of 1 indicates the PCI 9050-1 reported a system error on the SERR# signal. Value of 1 clears the Error Status bit (0).	Yes	Yes/Clr	0
15	**Detected Parity Error.** Value of 1 indicates the PCI 9050-1 detected a PCI Bus parity error, even if parity error handling is disabled (the Parity Error Response bit in the Command Register is clear). To cause this bit to be set, one of two conditions must exist: 1) the PCI 9050-1 detected a parity error during a PCI Address phase; or, 2) the PCI 9050-1 detected a data parity error when it was the target of a write. Value of 1 clears the bit (0).	Yes	Yes/Clr	0

Register 7-4. (PCIREV; 08h) PCI Revision ID

Bit	Description	Read	Write	Value after Reset
7:0	**Revision ID.** PCI 9050-1 Silicon revision.	Yes	Serial EEPROM	Current Rev Number

Register 7-5. (PCICCR; 09-0Bh) PCI Class Code

Bit	Description	Read	Write	Value after Reset
7:0	**Specific Register Level Programming Interface.** None defined.	Yes	Serial EEPROM	00h
15:8	**Subclass Encoding (80h).** (Other Bridge Device)**.**	Yes	Serial EEPROM	80h
23:16	**Base Class Encoding.** (Bridge Device).	Yes	Serial EEPROM	06h

Register 7-6. (PCICLSR; 0Ch) PCI Cache Line Size

Bit	Description	Read	Write	Value after Reset
7:0	**System Cache Line Size.** Specified in units of 32-bit Lwords. Can be written and read; however, the value has no effect on chip operation.	Yes	Yes	0h

Register 7-7. (PCILTR; 0Dh) PCI Bus Latency Timer

Bit	Description	Read	Write	Value after Reset
7:0	**PCI Bus Latency Timer.** ***Not Supported*.**	Yes	No	0h

Register 7-8. (PCIHTR; 0Eh) PCI Header Type

Bit	Description	Read	Write	Value after Reset
6:0	**Configuration Layout Type.** Specifies layout of registers 10h through 3Fh in configuration space. Only one encoding, 0, is defined. All other encodings are ***reserved***.	Yes	No	0h
7	**Header Type.** Value of 1 indicates multiple functions. Value of 0 indicates single function.	Yes	No	0

Register 7-9. (PCIBISTR; 0Fh) PCI Built-In Self Test (BIST)

Bit	Description	Read	Write	Value after Reset
7:0	**Built-In Test.** Value of 0 indicates device passed its test. ***Not Supported*.**	Yes	No	0

Register 7-10. (PCIBAR0; 10h) PCI Base Address 0 for Memory Accesses to Local Configuration Registers

Bit	Description	Read	Write	Value after Reset
0	**Memory Space Indicator.** Value of 0 indicates the register maps into Memory space. Value of 1 indicates the register maps into I/O space. ***Note:*** *Hardwired to 0.*	Yes	No	0
2:1	**Register Location.** Values: 00 = Locate anywhere in 32-bit Memory Address space 01 = *PCI r2.1*, Locate below 1-MB Memory Address space *PCI r2.2*, ***Reserved*** 10 = Locate anywhere in 64-bit Memory Address space 11 = ***Reserved*** ***Note:*** *Hardwired to 0.*	Yes	No	00
3	**Prefetchable.** Value of 1 indicates there are no side effects on reads. ***Note:*** *Hardwired to 0.*	Yes	No	0
6:4	**Memory Base Address.** Memory base address for access to Local configuration registers (uses 128 bytes). ***Note:*** *Hardwired to 0.*	Yes	No	000
31:7	**Memory Base Address.** Memory base address for access to Local configuration registers.	Yes	Yes	0h

Note: *PCIBAR0 can be enabled or disabled by using CNTRL[13:12].*

Register 7-11. (PCIBAR1; 14h) PCI Base Address 1 for I/O Accesses to Local Configuration Registers

Bit	Description	Read	Write	Value after Reset
0	**Memory Space Indicator.** Value of 0 indicates the register maps into Memory space. Value of 1 indicates the register maps into I/O space. ***Note:*** *Hardwired to 1.*	Yes	No	1
1	***Reserved.***	Yes	No	0
6:2	**I/O Base Address.** Base Address for I/O access to Local configuration registers (uses 128 bytes). ***Note:*** *Hardwired to 0.*	Yes	No	0h
31:7	**I/O Base Address.** Base Address for I/O access to Local configuration registers.	Yes	Yes	0h

Note: *PCIBAR1 can be enabled or disabled by using CNTRL[13:12].*

Register 7-12. (PCIBAR2; 18h) PCI Base Address 2 for Memory Accesses to Local Address Space 0

Bit	Description	Read	Write	Value after Reset
0	**Memory Space Indicator.** Value of 0 indicates the register maps into Memory space. Value of 1 indicates the register maps into I/O space. (Specified in the LAS0RR register.)	Yes	No	0
2:1	**Register Location (If Memory Space).** Values: 00 = Locate anywhere in 32-bit Memory Address space 01 = *PCI r2.1*, Locate below 1-MB Memory Address space *PCI r2.2*, ***Reserved*** 10 = Locate anywhere in 64-bit Memory Address space 11 = ***Reserved*** (Specified in the LAS0RR register.) If I/O Space, bit 1 is always 0 and bit 2 is included in the base address.	Yes	Mem: No I/O: Bit 1 No, Bit 2 Yes	00
3	**Prefetchable (If Memory Space).** Value of 1 indicates there are no side effects on reads. Reflects value of LAS0RR[3] and provides only status to the system. Does not affect PCI 9050-1 operation. The associated Bus Region Descriptor register controls prefetching functions of this address space. (Specified in the LAS0BRD register.) If I/O Space, bit 3 is included in the base address.	Yes	Mem: No I/O: Yes	0
31:4	**Base Address.** Base address for access to the Local Address space.	Yes	Yes	0h

Note: *PCIBAR2 can be enabled or disabled by setting or clearing LAS0BA[0].*

Register 7-13. (PCIBAR3; 1Ch) PCI Base Address 3 for Memory Accesses to Local Address Space 1

Bit	Description	Read	Write	Value after Reset
0	**Memory Space Indicator.** Value of 0 indicates the register maps into Memory space. Value of 1 indicates the register maps into I/O space. (Specified in the LAS1RR register.)	Yes	No	0
2:1	**Register Location.** Values: 00 = Locate anywhere in 32-bit Memory Address space 01 = *PCI r2.1*, Locate below 1-MB Memory Address space *PCI r2.2*, ***Reserved*** 10 = Locate anywhere in 64-bit Memory Address space 11 = ***Reserved*** (Specified in the LAS1RR register.) If I/O Space, bit 1 is always 0 and bit 2 is included in the base address.	Yes	Mem: No I/O: Bit 1 No, Bit 2 Yes	00
3	**Prefetchable (If Memory Space).** Value of 1 indicates there are no side effects on reads. Reflects value of LAS1RR[3] and provides only status to the system. Does not affect PCI 9050-1 operation. The associated Bus Region Descriptor register controls prefetching functions of this address space. (Specified in the LAS1BRD register.) If I/O Space, bit 3 is included in base address.	Yes	Mem: No I/O: Yes	0
31:4	**Base Address.** Base address for access to Local Address space.	Yes	Yes	0h

Note: *PCIBAR3 can be enabled or disabled by setting or clearing LAS1BA[0].*

Register 7-14. (PCIBAR4; 20h) PCI Base Address 4 for Memory Accesses to Local Address Space 2

Bit	Description	Read	Write	Value after Reset
0	**Memory Space Indicator.** Value of 0 indicates the register maps into Memory space. Value of 1 indicates the register maps into I/O space. (Specified in the LAS2RR register.)	Yes	No	0
2:1	**Register Location.** Values: 00 = Locate anywhere in 32-bit Memory Address space 01 = *PCI r2.1*, Locate below 1-MB Memory Address space *PCI r2.2*, ***Reserved*** 10 = Locate anywhere in 64-bit Memory Address space 11 = ***Reserved*** (Specified in the LAS2RR register.) If I/O Space, bit 1 is always 0 and bit 2 is included in the base address.	Yes	Mem: No I/O: Bit 1 No, Bit 2 Yes	00
3	**Prefetchable (If Memory Space).** Value of 1 indicates there are no side effects on reads. Reflects value of LAS2RR[3] and provides only status to the system. Does not affect the PCI 9050-1 operation. The associated Bus Region Descriptor register controls prefetching functions of this address space. (Specified in the LAS2BRD register.) If I/O Space, bit 3 is included in base address.	Yes	Mem: No I/O: Yes	0
31:4	**Base Address.** Base address for access to Local Address space.	Yes	Yes	0h

Note: *PCIBAR4 can be enabled or disabled by setting or clearing LAS2BA[0].*

Register 7-15. (PCIBAR5; 24h) PCI Base Address 5 for Memory Accesses to Local Address Space 3

Bit	Description	Read	Write	Value after Reset
0	**Memory Space Indicator.** Value of 0 indicates the register maps into Memory space. Value of 1 indicates the register maps into I/O space. (Specified in the LAS3RR register.)	Yes	No	0
2:1	**Register Location.** Values: 00 = Locate anywhere in 32-bit Memory Address space 01 = *PCI r2.1*, Locate below 1-MB Memory Address space *PCI r2.2*, ***Reserved*** 10 = Locate anywhere in 64-bit Memory Address space 11 = ***Reserved*** (Specified in the LAS3RR register.) If I/O Space, bit 1 is always 0 and bit 2 is included in the base address.	Yes	Mem: No I/O: Bit 1 No, Bit 2 Yes	00
3	**Prefetchable (If Memory Space).** Value of 1 indicates there are no side effects on reads. Reflects value of LAS3RR[3] and provides only status to the system. Does not affect the PCI 9050-1 operation. The associated Bus Region Descriptor register controls prefetching functions of this address space. (Specified in the LAS3BRD register.) If I/O Space, bit 3 is included in base address.	Yes	Mem: No I/O: Yes	0
31:4	**Base Address.** Base address for access to Local Address space.	Yes	Yes	0h

Note: *PCIBAR5 can be enabled or disabled by setting or clearing LAS3BA[0].*

Register 7-16. (PCICIS; 28h) PCI Cardbus CIS Pointer

Bit	Description	Read	Write	Value after Reset
31:0	**PCMCIA Cardbus Information Structure Pointer.** ***Not Supported***.	Yes	No	0h

Register 7-17. (PCISVID; 2Ch) PCI Subsystem Vendor ID

Bit	Description	Read	Write	Value after Reset
15:0	**Subsystem Vendor ID.** Unique Add-in Board Vendor ID.	Yes	Serial EEPROM	0h

Register 7-18. (PCISID; 2Eh) PCI Subsystem ID

Bit	Description	Read	Write	Value after Reset
15:0	**Subsystem ID.** Unique Add-in Board Device ID.	Yes	Serial EEPROM	0h

Register 7-19. (PCIERBAR; 30h) PCI Expansion ROM Base Address

Bit	Description	Read	Write	Value after Reset
0	**Address Decode Enable.** Value of 1 indicates a device accepts accesses to the Expansion ROM address. Value of 0 indicates a device does not accept accesses to Expansion ROM space.	Yes	Yes	0
10:1	***Reserved***.	Yes	No	0h
31:11	**Expansion ROM Base Address (upper 21 bits).**	Yes	Yes	0h

Register 7-20. (PCIILR; 3Ch) PCI Interrupt Line

Bit	Description	Read	Write	Value after Reset
7:0	**Interrupt Line Routing Value.** Indicates to which system interrupt controller(s) input the interrupt line is connected.	Yes	Yes	0h

Register 7-21. (PCIIPR; 3Dh) PCI Interrupt Pin

Bit	Description	Read	Write	Value after Reset
7:0	**Interrupt Pin Register.** Indicates which interrupt pin the device uses. The following values are decoded: 0 = No Interrupt Pin 1 = INTA# 2 = INTB# 3 = INTC# 4 = INTD#	Yes	Serial EEPROM	1h

Register 7-22. (PCIMGR; 3Eh) PCI Minimum Grant

Bit	Description	Read	Write	Value after Reset
7:0	**Min_Gnt.** Specifies the necessary length of a Burst period device, assuming a clock rate of 33 MHz. Value is a multiple of 1/4 µs increments. ***Not Supported.***	Yes	No	0h

Register 7-23. (PCIMLR; 3Fh) PCI Maximum Latency

Bit	Description	Read	Write	Value after Reset
7:0	**Max_Lat.** Specifies how often the device must gain access to the PCI Bus. Value is a multiple of 1/4 µs increments. ***Not Supported.***	Yes	No	0h

7.3 LOCAL CONFIGURATION REGISTERS

Register 7-24. (LAS0RR; 00h) Local Address Space 0 Range

Bit	Description	Read	Write	Value after Reset
0	**Memory Space Indicator.** Value of 0 indicates Local Address Space 0 maps into PCI Memory space. Value of 1 indicates Address Space 0 maps into PCI I/O space.	Yes	Yes	0
2:1	When mapped into Memory space, encoding is as follows: 00 = Locate anywhere in 32-bit PCI Address space 01 = *PCI r2.1*, Locate below 1-MB Memory Address space *PCI r2.2*, ***Reserved*** 10 = Locate anywhere in 64-bit PCI Address space 11 = ***Reserved*** When mapped into I/O space, bit 1 must be set to 0. Bit 2 is included with bits [27:3] to indicate the decoding range.	Yes	Yes	00
3	When mapped into Memory space, writing a 1 indicates reads are prefetchable (does not affect the PCI 9050-1 operation, but is used for system status). When mapped into I/O space, it is included with bits [27:2] to indicate the decoding range.	Yes	Yes	0
27:4	Specifies which PCI Address bits to use for decoding a PCI access to Local Bus Space 0. Each bit corresponds to a PCI Address bit. Bit 27 corresponds to address bit 27. Write 1 to all bits that are to be included in decode and 0 to all others (used in conjunction with PCIBAR2). Default is 1 MB. ***Note:*** *Range (**not** Range register) must be power of 2. "Range register value" is two's complement of range.*	Yes	Yes	FF0000h
31:28	***Reserved.*** (PCI address bits [31:28] are always included in decoding.)	Yes	No	0h

Register 7-25. (LAS1RR; 04h) Local Address Space 1 Range

Bit	Description	Read	Write	Value after Reset
0	**Memory Space Indicator.** Value of 0 indicates Local Address Space 1 maps into PCI Memory space. Value of 1 indicates address Space 1 maps into PCI I/O space.	Yes	Yes	0
2:1	When mapped into Memory space, encoding is as follows: 00 = Locate anywhere in 32-bit PCI Address space 01 = *PCI r2.1*, Locate below 1-MB Memory Address space *PCI r2.2*, ***Reserved*** 10 = Locate anywhere in 64-bit PCI Address space 11 = ***Reserved*** When mapped into I/O space, bit 1 must be set to 0. Bit 2 is included with bits [27:3] to indicate the decoding range.	Yes	Yes	00
3	When mapped into Memory space, writing a 1 indicates reads are prefetchable (does not affect the PCI 9050-1 operation, but is used for system status). When mapped into I/O space, it is included with bits [27:2] to indicate the decoding range.	Yes	Yes	0
27:4	Specifies which PCI Address bits to use for decoding a PCI access to Local Bus Space 1. Each bit corresponds to a PCI Address bit. Bit 27 corresponds to address bit 27. Write 1 to all bits that are to be included in decode and 0 to all others (used in conjunction with PCIBAR3). ***Note:*** *Range (**not** Range register) must be power of 2. "Range register value" is two's complement of range.*	Yes	Yes	0h
31:28	***Reserved.*** (PCI address bits [31:28] are always included in decoding.)	Yes	No	0h

Register 7-26. (LAS2RR; 08h) Local Address Space 2 Range

Bit	Description	Read	Write	Value after Reset
0	**Memory Space Indicator.** Value of 0 indicates Local Address Space 2 maps into PCI Memory space. Value of 1 indicates address Space 2 maps into PCI I/O space.	Yes	Yes	0
2:1	When mapped into Memory space, encoding is as follows: 00 = Locate anywhere in 32-bit PCI Address space 01 = *PCI r2.1*, Locate below 1-MB Memory Address space *PCI r2.2*, ***Reserved*** 10 = Locate anywhere in 64-bit PCI Address space 11 = ***Reserved*** When mapped into I/O space, bit 1 must be set to 0. Bit 2 is included with bits [27:3] to indicate the decoding range.	Yes	Yes	00
3	When mapped into Memory space, writing a 1 indicates reads are prefetchable (does not affect the PCI 9050-1 operation, but is used for system status). When mapped into I/O space, it is included with bits [27:2] to indicate the decoding range.	Yes	Yes	0
27:4	Specifies which PCI Address bits to use for decoding a PCI access to Local Bus Space 2. Each bit corresponds to a PCI Address bit. Bit 27 corresponds to address bit 27. Write 1 to all bits that are to be included in decode and 0 to all others (used in conjunction with PCIBAR4). ***Note:*** *Range (**not** Range register) must be power of 2. "Range register value" is two's complement of range.*	Yes	Yes	0h
31:28	***Reserved.*** (PCI address bits [31:28] are always included in decoding.)	Yes	No	0h

Register 7-27. (LAS3RR; 0Ch) Local Address Space 3 Range

Bit	Description	Read	Write	Value after Reset
0	**Memory Space Indicator.** Value of 0 indicates Local Address Space 3 maps into PCI Memory space. Value of 1 indicates address Space 3 maps into PCI I/O space.	Yes	Yes	0
2:1	When mapped into Memory space, encoding is as follows: 00 = Locate anywhere in 32-bit PCI Address space 01 = *PCI r2.1*, Locate below 1-MB Memory Address space *PCI r2.2*, ***Reserved*** 10 = Locate anywhere in 64-bit PCI Address space 11 = ***Reserved*** When mapped into I/O space, bit 1 must be set to 0. Bit 2 is included with bits [27:3] to indicate the decoding range.	Yes	Yes	00
3	When mapped into Memory space, writing a 1 indicates reads are prefetchable (does not affect the PCI 9050-1 operation, but is used for system status). When mapped into I/O space, it is included with bits [27:2] to indicate the decoding range.	Yes	Yes	0
27:4	Specifies which PCI Address bits to use for decoding a PCI access to Local Bus Space 3. Each bit corresponds to a PCI Address bit. Bit 27 corresponds to address bit 27. Write 1 to all bits that are to be included in decode and 0 to all others (used in conjunction with PCIBAR5). ***Note:*** *Range (**not** Range register) must be power of 2. "Range register value" is two's complement of range.*	Yes	Yes	0h
31:28	***Reserved.*** (PCI address bits [31:28] are always included in decoding.)	Yes	No	0h

Register 7-28. (EROMRR; 10h) Expansion ROM Range

Bit	Description	Read	Write	Value after Reset
10:0	***Reserved***.	Yes	No	0h
27:11	Specifies PCI address bits used to decode PCI-to-Local Bus Expansion ROM. Each of the bits corresponds to an Address bit. Value of 1 indicates the bits should be included in decode. Write a value of 0 to all others (used in conjunction with PCIERBAR). Default is 64 KB. ***Notes:*** *Range (**not** Range register) must be power of 2. “Range register value” is two’s complement of range.* *EROMRR should normally be programmed by way of the serial EEPROM to a value of 0h, unless Expansion ROM is present on the Local Bus. If the value is not 0h (default value is 64K), system BIOS may attempt to allocate Expansion ROM address space and then access it at the local base address specified in EROMBA (default value is 1 MB) to determine whether the Expansion ROM image is valid. If the image is not valid, as defined in Section 6.3.1.1 (PCI Expansion ROM Header Format) of PCI r2.2, the system BIOS unmaps the Expansion ROM address space it initially allocated, by writing 0h to PCIERBAR.*	Yes	Yes	11111111111100000
31:28	***Reserved***. (PCI address bits [31:28] are always included in decoding.)	Yes	No	0h

Register 7-29. (LAS0BA; 14h) Local Address Space 0 Local Base Address (Remap)

Bit	Description	Read	Write	Value after Reset
0	**Space 0 Enable.** Value of 1 enables decoding of PCI addresses for Direct Slave access to Local Bus Space 0. Value of 0 disables decoding. ***Note:*** *PCIBAR2 can be enabled or disabled by setting or clearing this bit.*	Yes	Yes	0
1	***Reserved.***	Yes	Yes	0
3:2	If Local Bus Space 0 is mapped into Memory space, bits are not used. When mapped into I/O space, included with bits [27:4] for remapping.	Yes	Yes	00
27:4	**Remap PCI Address to Local Address Space 0 into Local Address Space.** Bits in this register remap (replace) PCI Address bits used in decode as Local Address bits. ***Note:*** *Remap Address value must be a multiple of the Range (**not** the Range register).*	Yes	Yes	0h
31:28	***Reserved.*** (Local address bits [31:28] do not exist in the PCI 9050-1.)	Yes	No	0h

Register 7-30. (LAS1BA; 18h) Local Address Space 1 Local Base Address (Remap)

Bit	Description	Read	Write	Value after Reset
0	**Space 1 Enable.** Value of 1 enables decoding of PCI addresses for Direct Slave access to Local Bus Space 1. Value of 0 disables decoding. ***Note:*** *PCIBAR3 can be enabled or disabled by setting or clearing this bit.*	Yes	Yes	0
1	***Reserved.***	Yes	Yes	0
3:2	If Local Bus Space 1 is mapped into Memory space, bits are not used. When mapped into I/O space, included with bits [27:4] for remapping.	Yes	Yes	00
27:4	**Remap PCI Address to Local Address Space 1 into Local Address Space.** Bits in this register remap (replace) PCI Address bits used in decode as Local Address bits. ***Note:*** *Remap Address value must be a multiple of the Range (**not** the Range register).*	Yes	Yes	0h
31:28	***Reserved.*** (Local address bits [31:28] do not exist in the PCI 9050-1.)	Yes	No	0h

Register 7-31. (LAS2BA; 1Ch) Local Address Space 2 Local Base Address (Remap)

Bit	Description	Read	Write	Value after Reset
0	**Space 2 Enable.** Value of 1 enables decoding of PCI addresses for Direct Slave access to Local Bus Space 2. Value of 0 disables decoding. ***Note:*** *PCIBAR4 can be enabled or disabled by setting or clearing this bit.*	Yes	Yes	0
1	***Reserved.***	Yes	No	0
3:2	If Local Bus Space 2 is mapped into Memory space, bits are not used. When mapped into I/O space, included with bits [27:4] for remapping.	Yes	Yes	00
27:4	**Remap PCI Address to Local Address Space 2 into Local Address Space.** Bits in this register remap (replace) PCI Address bits used in decode as Local Address bits. ***Note:*** *Remap Address value must be a multiple of the Range (**not** the Range register).*	Yes	Yes	0h
31:28	***Reserved.*** (Local address bits [31:28] do not exist in the PCI 9050-1.)	Yes	No	0h

Register 7-32. (LAS3BA; 20h) Local Address Space 3 Local Base Address (Remap)

Bit	Description	Read	Write	Value after Reset
0	**Space 3 Enable.** Value of 1 enables decoding of PCI addresses for Direct Slave access to Local Bus Space 3. Value of 0 disables decoding. ***Note:*** *PCIBAR5 can be enabled or disabled by setting or clearing this bit.*	Yes	Yes	0
1	***Reserved.***	Yes	No	0
3:2	If Local Bus Space 3 is mapped into Memory space, bits are not used. When mapped into I/O space, included with bits [27:4] for remapping.	Yes	Yes	00
27:4	**Remap PCI Address to Local Address Space 3 into Local Address Space.** Bits in this register remap (replace) PCI Address bits used in decode as Local Address bits. ***Note:*** *Remap Address value must be a multiple of the Range (**not** the Range register).*	Yes	Yes	0h
31:28	***Reserved.*** (Local address bits [31:28] do not exist in the PCI 9050-1.)	Yes	No	0h

Register 7-33. (EROMBA; 24h) Expansion ROM Local Base Address (Remap)

Bit	Description	Read	Write	Value after Reset
10:0	***Reserved.***	Yes	No	0h
27:11	Remap PCI Expansion ROM Space into Local Address Space. Bits in this register remap (replace) the PCI Address bits used in decode as Local Address bits. Default base is 1 MB. ***Note:*** *Remap Address value must be a multiple of the Range (**not** the Range register).*	Yes	Yes	00000001000000000
31:28	***Reserved.*** (Local address bits [31:28] do not exist in the PCI 9050-1.)	Yes	No	0h

Register 7-34. (LAS0BRD; 28h) Local Address Space 0 Bus Region Descriptors

Bit	Description	Read	Write	Value after Reset
0	**Burst Enable.** Value of 1 indicates bursting is enabled. Value of 0 indicates bursting is disabled. Bursting occurs if the prefetch count is not equal to 00.	Yes	Yes	0
1	**LRDYi# Input Enable.** Value of 1 indicates enabled. Value of 0 indicates disabled.	Yes	Yes	0
2	**BTERM# Input Enable.** Value of 1 indicates BTERM# Input is enabled. Value of 0 indicates BTERM# input is disabled. Burst length limited to four Lwords.	Yes	Yes	0
4:3	**Prefetch Count.** Number of Lwords to prefetch during Memory Read cycle. Used only if bit 5 is high (prefetch count enabled). Values: 00 = Do not prefetch. Only read bytes specified by C/BE lines. 01 = Prefetch 4 Lwords if bit 5 is set. 10 = Prefetch 8 Lwords if bit 5 is set. 11 = Prefetch 16 Lwords if bit 5 is set.	Yes	Yes	00
5	**Prefetch Count Enable.** Value of 1 prefetches up to the number of Lwords specified in the prefetch count. Value of 0 ignores the count and prefetching continues until terminated by the PCI Bus.	Yes	Yes	0
10:6	**NRAD Wait States.** Number of Read Address-to-Data wait states (0-31).	Yes	Yes	0h
12:11	**NRDD Wait States.** Number of Read Data-to-Data wait states (0-3).	Yes	Yes	00
14:13	**NXDA Wait States.** Number of Read/Write Data-to-Address wait states (0-3). LAD Bus Write data is not valid during NXDA wait states.	Yes	Yes	00
19:15	**NWAD Wait States.** Number of Write Address-to-Data wait states (0-31). LAD Bus data is valid during NWAD wait states.	Yes	Yes	0h
21:20	**NWDD Wait States.** Number of Write Data-to-Data wait states (0-3).	Yes	Yes	00
23:22	**Bus Width.** Values: 00 = 8-bit 01 = 16-bit 10 = 32-bit 11 = ***Reserved***	Yes	Yes	10
24	**Byte Ordering.** Value of 1 indicates Big Endian. Value of 0 indicates Little Endian.	Yes	Yes	0
25	**Big Endian Byte Lane Mode.** Value of 1 indicates that in Big Endian mode byte lanes, [31:16] be used for a 16-bit Local Bus, and byte lane [31:24] for an 8-bit Local Bus. Value of 0 indicates that in Big Endian mode byte lanes, [15:0] be used for a 16-bit Local Bus, and byte lane [7:0] for an 8-bit Local Bus.	Yes	Yes	0
27:26	**Read Strobe Delay.** Number of clocks from beginning of cycle until RD# strobe is asserted (0-3). This value must be ≤ NRAD for RD# to be asserted.	Yes	Yes	00
29:28	**Write Strobe Delay.** Number of clocks from beginning of cycle until WR# strobe is asserted (0-3). This value must be ≤ NWAD for WR# to be asserted.	Yes	Yes	00
31:30	**Write Cycle Hold.** Number of clocks from WR# de-assertion until the end of the cycle (0-3). Used to extend data hold time.	Yes	Yes	00

Register 7-35. (LAS1BRD; 2Ch) Local Address Space 1 Bus Region Descriptors

Bit	Description	Read	Write	Value after Reset
0	**Burst Enable.** Value of 1 indicates bursting is enabled. Value of 0 indicates bursting is disabled. Bursting occurs if the prefetch count is not equal to 00.	Yes	Yes	0
1	**LRDYi# Input Enable.** Value of 1 indicates enabled. Value of 0 indicates disabled.	Yes	Yes	0
2	**BTERM# Input Enable.** Value of 1 indicates BTERM# input is enabled. Value of 0 indicates BTERM# input is disabled. Burst length limited to four Lwords.	Yes	Yes	0
4:3	**Prefetch Count.** Number of Lwords to prefetch during Memory Read cycle. Used only if bit 5 is high (prefetch count enabled). Values: 00 = Do not prefetch. Only read bytes specified by C/BE lines. 01 = Prefetch 4 Lwords if bit 5 is set. 10 = Prefetch 8 Lwords if bit 5 is set. 11 = Prefetch 16 Lwords if bit 5 is set.	Yes	Yes	00
5	**Prefetch Count Enable.** Value of 1 prefetches up to the number of Lwords specified in the prefetch count. Value of 0 ignores the count and prefetching continues until terminated by the PCI Bus.	Yes	Yes	0
10:6	**NRAD Wait States.** Number of Read Address-to-Data wait states (0-31).	Yes	Yes	0h
12:11	**NRDD Wait States.** Number of Read Data-to-Data wait states (0-3).	Yes	Yes	00
14:13	**NXDA Wait States.** Number of Read/Write Data-to-Address wait states (0-3). LAD Bus Write data is not valid during NXDA wait states.	Yes	Yes	00
19:15	**NWAD Wait States.** Number of Write Address-to-Data wait states (0-31). LAD Bus data is valid during NWAD wait states.	Yes	Yes	0h
21:20	**NWDD Wait States.** Number of Write Data-to-Data wait states (0-3).	Yes	Yes	00
23:22	**Bus Width.** Values: 00 = 8-bit 01 = 16-bit 10 = 32-bit 11 = ***Reserved***	Yes	Yes	10
24	**Byte Ordering.** Value of 1 indicates Big Endian. Value of 0 indicates Little Endian.	Yes	Yes	0
25	**Big Endian Byte Lane Mode.** Value of 1 indicates that in Big Endian mode byte lanes, [31:16] be used for a 16-bit Local Bus, and byte lane [31:24] for an 8-bit Local Bus. Value of 0 indicates that in Big Endian mode byte lanes, [15:0] be used for a 16-bit Local Bus, and byte lane [7:0] for an 8-bit Local Bus.	Yes	Yes	0
27:26	**Read Strobe Delay.** Number of clocks from beginning of cycle until RD# strobe is asserted (0-3). This value must be ≤ NRAD for RD# to be asserted.	Yes	Yes	00
29:28	**Write Strobe Delay.** Number of clocks from beginning of cycle until WR# strobe is asserted (0-3). This value must be ≤ NWAD for WR# to be asserted.	Yes	Yes	00
31:30	**Write Cycle Hold.** Number of clocks from WR# de-assertion until the end of the cycle (0-3). Used to extend data hold time.	Yes	Yes	00

Register 7-36. (LAS2BRD; 30h) Local Address Space 2 Bus Region Descriptors

Bit	Description	Read	Write	Value after Reset
0	**Burst Enable.** Value of 1 indicates bursting is enabled. Value of 0 indicates bursting is disabled. Bursting occurs if the prefetch count is not equal to 00.	Yes	Yes	0
1	**LRDYi# Input Enable.** Value of 1 indicates enabled. Value of 0 indicates disabled.	Yes	Yes	0
2	**BTERM# Input Enable.** Value of 1 indicates BTERM# input is enabled. Value of 0 indicates BTERM# input is disabled. Burst length limited to four Lwords.	Yes	Yes	0
4:3	**Prefetch Count.** Number of Lwords to prefetch during Memory Read cycle. Used only if bit 5 is high (prefetch count enabled). Values: 00 = Do not prefetch. Only read bytes specified by C/BE lines. 01 = Prefetch 4 Lwords if bit 5 is set. 10 = Prefetch 8 Lwords if bit 5 is set. 11 = Prefetch 16 Lwords if bit 5 is set.	Yes	Yes	0
5	**Prefetch Count Enable.** Value of 1 prefetches up to the number of Lwords specified in the prefetch count. Value of 0 ignores the count and prefetching continues until terminated by the PCI Bus.	Yes	Yes	0
10:6	**NRAD Wait States.** Number of Read Address-to-Data wait states (0-31).	Yes	Yes	0h
12:11	**NRDD Wait States.** Number of Read Data-to-Data wait states (0-3).	Yes	Yes	00
14:13	**NXDA Wait States.** Number of Read/Write Data-to-Address wait states (0-3). LAD Bus Write data is not valid during NXDA wait states.	Yes	Yes	00
19:15	**NWAD Wait States.** Number of Write Address-to-Data wait states (0-31). LAD Bus data is valid during NWAD wait states.	Yes	Yes	0h
21:20	**NWDD Wait States.** Number of Write Data-to-Data wait states (0-3).	Yes	Yes	00
23:22	**Bus Width.** Values: 00 = 8-bit 01 = 16-bit 10 = 32-bit 11 = ***Reserved***	Yes	Yes	10
24	**Byte Ordering.** Value of 1 indicates Big Endian. Value of 0 indicates Little Endian.	Yes	Yes	0
25	**Big Endian Byte Lane Mode.** Value of 1 indicates that in Big Endian mode byte lanes, [31:16] be used for a 16-bit Local Bus, and byte lane [31:24] for an 8-bit Local Bus. Value of 0 indicates that in Big Endian mode byte lanes, [15:0] be used for a 16-bit Local Bus, and byte lane [7:0] for an 8-bit Local Bus.	Yes	Yes	0
27:26	**Read Strobe Delay.** Number of clocks from beginning of cycle until RD# strobe is asserted (0-3). This value must be ≤ NRAD for RD# to be asserted.	Yes	Yes	00
29:28	**Write Strobe Delay.** Number of clocks from beginning of cycle until WR# strobe is asserted (0-3). This value must be ≤ NWAD for WR# to be asserted.	Yes	Yes	00
31:30	**Write Cycle Hold.** Number of clocks from WR# de-assertion until the end of the cycle (0-3). Used to extend data hold time.	Yes	Yes	00

Register 7-37. (LAS3BRD; 34h) Local Address Space 3 Bus Region Descriptors

Bit	Description	Read	Write	Value after Reset
0	**Burst Enable.** Value of 1 indicates bursting is enabled. Value of 0 indicates bursting is disabled. Bursting occurs if the prefetch count is not equal to 00.	Yes	Yes	0
1	**LRDYi# Input Enable.** Value of 1 indicates enabled. Value of 0 indicates disabled.	Yes	Yes	0
2	**BTERM# Input Enable.** Value of 1 indicates BTERM# input is enabled. Value of 0 indicates BTERM# input is disabled. Burst length limited to four Lwords.	Yes	Yes	0
4:3	**Prefetch Count.** Number of Lwords to prefetch during Memory Read cycle. Used only if bit 5 is high (prefetch count enabled). Values: 00 = Do not prefetch. Only read bytes specified by C/BE lines. 01 = Prefetch 4 Lwords if bit 5 is set. 10 = Prefetch 8 Lwords if bit 5 is set. 11 = Prefetch 16 Lwords if bit 5 is set.	Yes	Yes	00
5	**Prefetch Count Enable.** Value of 1 prefetches up to the number of Lwords specified in the prefetch count. Value of 0 ignores the count and prefetching continues until terminated by the PCI Bus.	Yes	Yes	0
10:6	**NRAD Wait States.** Number of Read Address-to-Data wait states (0-31).	Yes	Yes	0h
12:11	**NRDD Wait States.** Number of Read Data-to-Data wait states (0-3).	Yes	Yes	00
14:13	**NXDA Wait States.** Number of Read/Write Data-to-Address wait states (0-3). LAD Bus Write data is not valid during NXDA wait states.	Yes	Yes	00
19:15	**NWAD Wait States.** Number of Write Address-to-Data wait states (0-31). LAD Bus data is valid during NWAD wait states.	Yes	Yes	0h
21:20	**NWDD Wait States.** Number of Write Data-to-Data wait states (0-3).	Yes	Yes	00
23:22	**Bus Width.** Values: 00 = 8-bit 01 = 16-bit 10 = 32-bit 11 = ***Reserved***	Yes	Yes	10
24	**Byte Ordering.** Value of 1 indicates Big Endian. Value of 0 indicates Little Endian.	Yes	Yes	0
25	**Big Endian Byte Lane Mode.** Value of 1 indicates that in Big Endian mode byte lanes, [31:16] be used for a 16-bit Local Bus, and byte lane [31:24] for an 8-bit Local Bus. Value of 0 indicates that in Big Endian mode byte lanes, [15:0] be used for a 16-bit Local Bus, and byte lane [7:0] for an 8-bit Local Bus.	Yes	Yes	0
27:26	**Read Strobe Delay.** Number of clocks from beginning of cycle until RD# strobe is asserted (0-3). This value must be ≤ NRAD for RD# to be asserted.	Yes	Yes	00
29:28	**Write Strobe Delay.** Number of clocks from beginning of cycle until WR# strobe Is asserted (0-3). This value must be ≤ NWAD for WR# to be asserted.	Yes	Yes	00
31:30	**Write Cycle Hold.** Number of clocks from WR# de-assertion until the end of the cycle (0-3). Used to extend data hold time.	Yes	Yes	00

Register 7-38. (EROMBRD; 38h) Expansion ROM Bus Region Descriptors

Bit	Description	Read	Write	Value after Reset
0	**Burst Enable.** Value of 1 indicates bursting is enabled. Value of 0 indicates bursting is disabled. Bursting occurs if the prefetch count (bits [4:3]) are not equal to 00.	Yes	Yes	0
1	**LRDYi# Input Enable.** Value of 1 indicates enabled. Value of 0 indicates disabled.	Yes	Yes	0
2	**BTERM# Input Enable.** Value of 1 indicates BTERM# input is enabled. Value of 0 indicates BTERM# input is disabled. Burst length limited to four Lwords.	Yes	Yes	0
4:3	**Prefetch Count.** Number of Lwords to prefetch during Memory Read cycle. Used only if bit 5 is high (prefetch count enabled). Values: 00 = Do not prefetch. Only read bytes specified by C/BE lines. 01 = Prefetch 4 Lwords if bit 5 is set. 10 = Prefetch 8 Lwords if bit 5 is set. 11 = Prefetch 16 Lwords if bit 5 is set.	Yes	Yes	00
5	**Prefetch Count Enable.** Value of 1 prefetches up to the number of Lwords specified in the prefetch count. Value of 0 ignores the count and prefetching continues until terminated by the PCI Bus.	Yes	Yes	0
10:6	**NRAD Wait States.** Number of Read Address-to-Data wait states (0-31).	Yes	Yes	0h
12:11	**NRDD Wait States.** Number of Read Data-to-Data wait states (0-3).	Yes	Yes	00
14:13	**NXDA Wait States.** Number of Read/Write Data-to-Address wait states (0-3). LAD Bus Write data is not valid during NXDA wait states.	Yes	Yes	00
19:15	**NWAD Wait States.** Number of Write Address-to-Data wait states (0-31). LAD Bus data is valid during NWAD wait states.	Yes	Yes	0h
21:20	**NWDD Wait States.** Number of Write Data-to-Data wait states (0-3).	Yes	Yes	00
23:22	**Bus Width.** Values: 00 = 8-bit 01 = 16-bit 10 = 32-bit 11 = ***Reserved***	Yes	Yes	10
24	**Byte Ordering.** Value of 1 indicates Big Endian. Value of 0 indicates Little Endian.	Yes	Yes	0
25	**Big Endian Byte Lane Mode.** Value of 1 indicates that in Big Endian mode byte lanes, [31:16] be used for a 16-bit Local Bus, and byte lane [31:24] for an 8-bit Local Bus. Value of 0 indicates that in Big Endian mode byte lanes, [15:0] be used for a 16-bit Local Bus, and byte lane [7:0] for an 8-bit Local Bus.	Yes	Yes	0
27:26	**Read Strobe Delay.** Number of clocks from beginning of cycle until RD# strobe is asserted (0-3). This value must be ≤ NRAD for RD# to be asserted.	Yes	Yes	00
29:28	**Write Strobe Delay.** Number of clocks from beginning of cycle until WR# strobe is asserted (0-3). This value must be ≤ NWAD for WR# to be asserted.	Yes	Yes	00
31:30	**Write Cycle Hold.** Number of clocks from WR# de-assertion until the end of the cycle (0-3). Used to extend data hold time.	Yes	Yes	00

7.3.1 Chip Select Registers

Register 7-39. (CS0BASE; 3Ch) Chip Select 0 Base Address

Bit	Description	Read	Write	Value after Reset
0	**Chip Select 0 Enable.** Value of 1 indicates enabled. Value of 0 indicates disabled.	Yes	Yes	0
27:1	**Local Base Address of Chip Select 0.** Write zeros (0) in the least significant bits to define the range for Chip Select 0. Starting from bit 1 and scanning toward bit 27, the first "1" found defines size. The remaining most significant bits, excluding the first "1" found, define base address.	Yes	Yes	0h
31:28	***Reserved.***	Yes	No	0h

Register 7-40. (CS1BASE; 40h) Chip Select 1 Base Address

Bit	Description	Read	Write	Value after Reset
0	**Chip Select 1 Enable.** Value of 1 indicates enabled. Value of 0 indicates disabled.	Yes	Yes	0
27:1	**Local Base Address of Chip Select 1.** Write zeros (0) in the least significant bits to define the range for Chip Select 1. Starting from bit 1 and scanning toward bit 27, the first "1" found defines size. The remaining most significant bits, excluding the first "1" found, define base address.	Yes	Yes	0h
31:28	***Reserved.***	Yes	No	0h

Register 7-41. (CS2BASE; 44h) Chip Select 2 Base Address

Bit	Description	Read	Write	Value after Reset
0	**Chip Select 2 Enable.** Value of 1 indicates enabled. Value of 0 indicates disabled.	Yes	Yes	0
27:1	**Local Base Address of Chip Select 2.** Write zeros (0) in the least significant bits to define the range for Chip Select 2. Starting from bit 1 and scanning toward bit 27, the first "1" found defines size. The remaining most significant bits, excluding the first "1" found, define the base address.	Yes	Yes	0h
31:28	***Reserved.***	Yes	No	0h

Register 7-42. (CS3BASE; 48h) Chip Select 3 Base Address

Bit	Description	Read	Write	Value after Reset
0	**Chip Select 3 Enable.** Value of 1 indicates enabled. Value of 0 indicates disabled.	Yes	Yes	0
27:1	**Local Base Address of Chip Select 3.** Write zeros (0) in the least significant bits to define the range for Chip Select 3. Starting from bit 1 and scanning toward bit 27, the first "1" found defines size. The remaining most significant bits, excluding the first "1" found, define base address.	Yes	Yes	0h
31:28	***Reserved.***	Yes	No	0h

7.3.2 Control Registers

Register 7-43. (INTCSR; 4Ch) Interrupt Control/Status

Bit	Description	Read	Write	Value after Reset
0	**Local Interrupt 1 Enable.** Value of 1 indicates enabled. Value of 0 indicates disabled.	Yes	Yes	0
1	**Local Interrupt 1 Polarity.** Value of 1 indicates active high. Value of 0 indicates Active low.	Yes	Yes	0
2	**Local Interrupt 1 Status.** Value of 1 indicates interrupt active. Value of 0 indicates Interrupt not active.	Yes	No	0
3	**Local Interrupt 2 Enable.** Value of 1 indicates enabled. Value of 0 indicates disabled.	Yes	Yes	0
4	**Local Interrupt 2 Polarity.** Value of 1 indicates active high. Value of 0 indicates Active low.	Yes	Yes	0
5	**Local Interrupt 2 Status.** Value of 1 indicates interrupt active. Value of 0 indicates Interrupt not active.	Yes	No	0
6	**PCI Interrupt Enable.** Value of 1 enables PCI interrupt.	Yes	Yes	0
7	**Software Interrupt.** Value of 1 generates interrupt.	Yes	Yes	0
31:8	***Reserved*.**	Yes	No	0h

Register 7-44. (CNTRL; 50h) User I/O, Direct Slave Response, Serial EEPROM, and Initialization Control

Bit	Description	Read	Write	Value after Reset
0	**User I/O 0 or WAITO# Pin Select.** Selects the USER0/WAITO# pin function. Value of 1 indicates pin is WAITO#. Value of 0 indicates pin is USER0.	Yes	Yes	0
1	**User I/O 0 Direction.** Value of 0 indicates Input. Value of 1 indicates Output. The pin is always an output if the WAITO# function is selected.	Yes	Yes	0
2	**User I/O 0 Data.** If programmed as an output, writing a value of 1 causes the corresponding pin to go high. If programmed as an input, reading provides the state of the corresponding pin.	Yes	Yes	0
3	**User I/O 1 or LLOCKo# Pin Select.** Selects the USER1/LLOCKo# pin function. Value of 1 indicates pin is LLOCKo#. Value of 0 indicates pin is USER1.	Yes	Yes	0
4	**User I/O 1 Direction.** Value of 0 indicates Input. Value of 1 indicates Output. The pin is always an output if the LLOCKo# function is selected.	Yes	Yes	0
5	**User I/O 1 Data.** If programmed as an output, writing a value of 1 causes corresponding pin to go high. If programmed as an input, reading provides the state of the corresponding pin.	Yes	Yes	0
6	**User I/O 2 or CS2# Pin Select.** Selects the USER2/CS2# pin function. Value of 1 indicates pin is CS2#. Value of 0 indicates pin is USER2.	Yes	Yes	0
7	**User I/O 2 Direction.** Value of 0 indicates Input. Value of 1 indicates Output. The pin is always an output if the CS2# function is selected.	Yes	Yes	0
8	**User I/O 2 Data.** If programmed as an output, writing a value of 1 causes corresponding pin to go high. If programmed as an input, reading provides the state of the corresponding pin.	Yes	Yes	0
9	**User I/O 3 or CS3# Pin Select.** Selects the USER3/CS3# pin function. Value of 1 indicates pin is CS3#. Value of 0 indicates pin is USER3.	Yes	Yes	0
10	**User I/O 3 Direction.** Value of 0 indicates Input. Value of 1 indicates Output. The pin is always an output if the CS3# function is selected.	Yes	Yes	0
11	**User I/O 3 Data.** If programmed as an output, writing a value of 1 causes corresponding pin to go high. If programmed as an input, reading provides the state of the corresponding pin.	Yes	Yes	0
13:12	**PCI Configuration Base Address Register (PCIBAR) Enables.** Values: 00, 11 = PCIBAR0 (Memory) and PCIBAR1 (I/O) enabled. 01 = PCIBAR0 (Memory) only 10 = PCIBAR1 (I/O) only ***Note:*** *PCIBAR0 and PCIBAR1 should be enabled for the PC platform.*	Yes	Yes	00
14	**PCI Delayed Read Mode.** Value of 1 immediately disconnects for a read. Prefetch the data into the Direct Slave Read FIFO. Returns data when PCI Read cycle is reapplied (*PCI r2.1*-compatible). Value of 0 de-asserted TRDY# until Read data is available.	Yes	Yes	0
15	**PCI Read with Write Flush Mode.** Value of 1 flushes a pending Read cycle if a Write cycle is detected. Value of 0 does not effect pending reads when a Write cycle occurs (*PCI r2.1*-compatible).	Yes	Yes	0

Register 7-44. (CNTRL; 50h) User I/O, Direct Slave Response, Serial EEPROM, and Initialization Control

Bit	Description	Read	Write	Value after Reset
16	**PCI Read No Flush Mode.** Value of 1 does not flush the Read FIFO if the PCI Read cycle completes (Read Ahead mode). Value of 0 flushes the Read FIFO if a PCI Read cycle completes.	Yes	Yes	0
17	**PCI Read No Write Mode.** Value of 1 forces Retry on writes if a read is pending. Value of 0 allows a write to occur while a read is pending.	Yes	Yes	0
18	**PCI Write Release Bus Mode Enable.** Value of 1 disconnects if the Write FIFO becomes full. Value of 0 de-asserts TRDY# until space is available in the Direct Slave Write FIFO (PCI Write Hold Bus mode).	Yes	Yes	0
22:19	**Direct Slave Retry Delay Clocks.** The number of PCI clocks (multiplied by 8) after the beginning of a Direct Slave cycle until a Retry is issued. Valid for Read cycles only if bit 14 is low. Valid for Write cycles only if bit 17 is low. ***Note:*** *This field should be set to a value of 3h or greater (refer to PCI 9050-1 Design Notes).*	Yes	Yes	0h
23	**Direct Slave Lock Enable.** Value of 1 enables PCI Direct Slave locked sequences. Value of 0 disables Direct Slave locked sequences.	Yes	Yes	0
24	**Serial EEPROM Clock for Local or PCI Bus Reads or Writes to Serial EEPROM.** Toggling this bit generates a serial EEPROM clock. (Refer to the manufacturer's data sheet for the particular serial EEPROM being used.)	Yes	Yes	0
25	**Serial EEPROM Chip Select.** For Local or PCI Bus reads or writes to serial EEPROM, setting this bit to 1 provides the serial EEPROM Chip Select.	Yes	Yes	0
26	**Write Bit to Serial EEPROM.** For writes, this output bit is the input to the serial EEPROM. Clocked into the serial EEPROM by the serial EEPROM clock.	Yes	Yes	0
27	**Read Serial EEPROM Data Bit.** For reads, this input bit is the serial EEPROM output. Clocked out of the serial EEPROM by the serial EEPROM clock.	Yes	No	—
28	**Serial EEPROM Valid.** Value of 1 indicates a valid serial EEPROM is present.	Yes	No	0
29	**Reload Configuration Registers.** When this bit is set to 0, writing a value of 1 causes the PCI 9050-1 to reload the Local Configuration registers from serial EEPROM.	Yes	Yes	0
30	PCI Adapter Software Reset. Value of 1 resets the PCI 9050-1, issues a reset to the Local Bus, and floats all other Local Bus output and I/O pins. The PCI 9050-1 remains in this reset condition until the PCI Host clears this bit. The contents of the PCI and Local Configuration registers are not reset.	Yes	Yes	0
31	**Mask Revision.**	Yes	No	0

8 PIN DESCRIPTIONS

8.1 PIN SUMMARY

Table 8-2 through Table 8-5 describe the pins common to all Bus modes:

- Power and Ground
- Serial EEPROM Interface
- PCI System Bus Interface
- Local Bus Support

Table 8-6 and Table 8-7 describe the Local Bus Data Transfer pins.

Unspecified pins are no connects (NC).

For a visual view of the pinout, refer to Section 10.

The following table lists abbreviations used in this section to represent pin types.

Table 8-1. Pin Type Abbreviations

Abbreviation	Pin Type
I/O	Input and output
I	Input only
O	Output only
TS	Three-state
OD	Open drain
TP	Totem pole
STS	Sustained three-state—driven high for one CLK before float
PU50K	Internal pull-up to V_{CC} with 50K resistor.
PU100K	Internal pull-up to V_{CC} with 100K resistor.
PD50K	Internal pull-down to V_{CC} with 50K resistor.

***Note:** Internal resistor values are nominal and may vary widely from published values.*

8.2 PULL-UP/PULL-DOWN RESISTOR REQUIREMENTS

Suggested values for external pull-up/pull-down resistors are from 1K to 10K Ohms.

No specific recommendations for pull-up/pull-down resistors are made for BCLKO, LCLK, and LHOLD pins.

8.2.1 Input Pins (Pin Type I)

This section discusses the pull-up/pull-down resistor requirements for the input pins—BTERM#, EEDO, LHOLD, LINTi[1:2], LRDYi#, MODE, and TEST.

The following Local Bus inputs internally connect to ground through a 50K-Ohm pull-down resistor—LHOLD and TEST.

- The internal pull-down resistor on the TEST input pin selects normal logic operation. Tie to ground for normal operation.
- The internal pull-down resistor on the LHOLD input pin gives the PCI 9050-1 ownership of the Local Bus (unless LHOLD is driven high to override the pull-down resistor).

The following Local Bus inputs internally connect to V_{CC} through a 100K-Ohm pull-up resistor—BTERM#, EEDO, LINTi[1:2], LRDYi#, and MODE.

- If the MODE input pin is not tied high or low, default functionality with the internal pull-up resistor is J mode.
- If either LINTi[1:2] is configured as active high rather than the default active low, then a pull-down resistor should be connected to hold the pin in an inactive state.
- If used, external pull-up resistors on the BTERM#, EEDO, and LRDYi#, input pins are recommended. Otherwise, they may be tied high or low.

8.2.2 Output Pins (Pin Type O)

This section discusses the pull-up/pull-down resistor requirements for the output pins—ADS#, ALE, CS[1:0]#, BLAST#, EECS, LA[27:2], LBE[3:0]#, LRESET#, LW/R#, RD#, and WR#.

The PCI 9050-1 floats Local Bus output signals (except CS[1:0]#, LHOLDA, and RD#) when its Local Bus is idle.

- **Three-state outputs**—ADS#, ALE, CS[1:0]#, BLAST#, LA[27:2], LBE[3:0]#, LW/R#, RD#, and WR#
  - To keep Local Bus output signals in an inactive state during float, external pull-up resistors are recommended on the following output pins if used—ADS#, BLAST#, LA[27:2], LBE[3:0]#, LW/R#, and WR#.
  - If ALE output is used, an external pull-down resistor is recommended to keep ALE output in the inactive state during float.
- **Totem-pole outputs**—EECS and LRESET#
  - If LRESET# output is used, an external pull-up resistor is recommended to keep LRESET# output in the inactive state during float.
  - An external pull-down resistor is recommended to keep EECS output in the inactive state during float.

8.2.3 I/O Pins (Pin Type I/O)

This section discusses the pull-up/pull-down resistor requirements for the I/O pins—LAD[31:0], USER0/WAIT#, USER1/LLOCK#, USER2/CS2#, and USER3/CS3#

The PCI 9050-1 floats Local Bus I/O signals (except CS[3:2]#) when its Local Bus is idle.

External pull-down resistors are recommended on the LAD[31:0] I/O pins, to keep connected signals in a known state or to keep unconnected inputs from oscillating and using additional power.

External pull-up resistors are recommended on the following I/O pins to keep the output signals in the inactive state during float:

- USER0/WAITO# if configured as WAIT0# output
- USER1/LLOCK# if configured as LLOCK# output

Note: *Multiplexed pins are configured as inputs at reset. If output functionality is programmed in serial EEPROM, pin configuration occurs when the serial EEPROM contents are loaded following PCI reset.*

If any of USER[3:0] multiplexed pins are configured as USER inputs (default functionality), they should be pulled to a known state.

8.2.4 NC Pins

Do not connect No Connect pins.

8.3 PINOUT

Table 8-2. Power, Ground, and Unused Pins

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
NC	Spare	2	N/A	45, 67	***Not Used.***
TEST	Test	1	I PD50K	99	Test pin. Pull high for test or reduced power state. Tie low for normal operation. When TEST is pulled high, all outputs except RD# (pin 126) are placed in high-impedance state. RD# provides a NANDTREE output when TEST is pulled high.
V_{DD}	Power	10	I	1, 10, 27, 41, 50, 66, 81, 103, 121, 146	Power supply pins (5V). Liberal .01 to .1 μF decoupling capacitors should be placed near the PCI 9050-1.
V_{SS}	Ground	10	I	9, 26, 40, 51, 65, 80, 104, 120, 147, 160	Ground pins.
Total		23			

Table 8-3. Serial EEPROM Interface Pins

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
EECS	Serial EEPROM Chip Select	1	O TP 8 mA	142	Serial EEPROM Chip Select.
EEDI	Serial EEPROM Data In	1	O TP 8 mA	145	Write data to serial EEPROM.
EEDO	Serial EEPROM Data Out	1	I PU100K	143	Read data from serial EEPROM.
EESK	Serial Data Clock	1	O TP 8 mA	144	Serial EEPROM clock pin.
Total		4			

Table 8-4. PCI System Bus Interface Pins

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
AD[31:0]	Address and Data	32	I/O TS PCI	150-157, 2-8, 11, 23-25, 28-32, 34-39, 42-43	Multiplexed on the same PCI pins. A bus transaction consists of an Address phase, followed by one or more Data phases. The PCI 9050-1 supports both Read and Write bursts.
C/BE[3:0]#	Bus Command and Byte Enables	4	I	158, 12, 22, 33	Multiplexed on the same PCI pins. During the Address phase of a transaction, defines the bus command. During the Data phase, used as byte enables. For additional information, refer to *PCI r2.1*.
CLK	Clock	1	I	149	Provides timing for all transactions on PCI and is an input to every PCI device. PCI operates up to 33 MHz.
DEVSEL#	Device Select	1	O STS PCI	16	When actively driven, indicates the driving device decoded its address as the current access target.
FRAME#	Cycle Frame	1	I PU100K	13	Driven by the current Master to indicate the beginning and duration of an access. Asserted to indicate a bus transaction is beginning. While asserted, Data transfers continue. When de-asserted, the transaction is in the final Data phase.
IDSEL	Initialization Device Select	1	I PU50K	159	Chip select used during Configuration Read or Write transactions.
INTA#	Interrupt A	1	O OC PCI	44	Requests an interrupt.
IRDY#	Initiator Ready	1	I PU100K	14	Indicates the ability of the initiating agent (Bus Master) to complete the current Data phase of the transaction.
LOCK#	Lock	1	I PU100K	18	Indicates an atomic operation that may require multiple transactions to complete.
PAR	Parity	1	I/O TS PCI	21	Indicates even parity across AD[31:0] and C/BE[3:0]#. Parity generation is required by all PCI agents. PAR is stable and valid one clock after the Address phase. For Data phases, PAR is stable and valid one clock after IRDY# is asserted on a Write transaction or TRDY# is asserted on a Read transaction. Once PAR is valid, it remains valid until one clock after completion of the current Data phase.
PERR#	Parity Error	1	O STS PCI	19	Indicates only the reporting of data parity errors during all PCI transactions, except during a Special cycle.

Table 8-4. PCI System Bus Interface Pins (Continued)

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
RST#	Reset	1	I PU100K	148	Brings PCI-specific registers, sequencers, and signals to a consistent state.
SERR#	System Error	1	O OC PCI	20	For reporting address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic.
STOP#	Stop	1	O STS PCI	17	Indicates the current target is requesting the Master to stop the current transaction.
TRDY#	Target Ready	1	O STS PCI	15	Indicates the ability of the target agent (selected device) to complete the current Data phase of the transaction.
Total		49			

Table 8-5. Local Bus Support Pins

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
BCLKO	BCLK Out	1	O TP 12 mA	63	Provides a buffered version of the PCI clock for optional use by the Local Bus. Not in phase with the PCI clock.
CS[1:0]#	Chip Selects 1 and 0	2	O TS 8 mA	131, 130	General purpose chip selects. The base and range of each may be programmed in the configuration registers.
LCLK	Local Bus Clock	1	I	135	Local clock (required) up to 40 MHz; may be asynchronous to the PCI clock.
LHOLD	Hold Request	1	I PU50K	134	Asserted by a Local Bus Master to request Local Bus use. Can be left unterminated to provide permanent Local Bus ownership to the PCI 9050-1.
LHOLDA	Hold Acknowledge	1	O TP 8 mA	133	Asserted by the PCI 9050-1 to grant Local Bus control to a Local Bus Master. When the PCI 9050-1 needs the Local Bus, it signals a preempt by de-asserting LHOLDA.
LINTi1	Local Interrupt 1 In	1	I PU100K	137	When asserted, causes a PCI interrupt. Polarity is determined by INTCSR[1].
LINTi2	Local Interrupt 2 In	1	I PU100K	136	When asserted, causes a PCI interrupt. Polarity is determined by INTCSR[4].
LRESET#	Local Reset Out	1	O TP 8 mA	132	Local Bus reset output, asserted when the PCI 9050-1 is reset, and used to reset devices on the Local Bus.
MODE	Bus Mode	1	I PU100K	68	Selects the PCI 9050-1 Bus Operation mode. 0 = C mode (Non-Multiplexed) 1 = J mode (Multiplexed)
USER0/ WAITO#	User I/O 0 or WAIT Out	1	I/O TS 8 mA	138	Can be programmed to be a configurable User I/O pin, USER0, or the Local Bus WAIT Output pin, WAITO#. WAITO# is asserted when wait states are caused by the internal wait state generator. Serves as an output to provide ready-out status. Default functionality is USER0. Pin configuration occurs when the serial EEPROM contents are loaded following PCI reset, or upon subsequent writing to the CNTRL[1:0] register bits.

Table 8-5. Local Bus Support Pins (Continued)

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
USER1/ LLOCKo#	User I/O 1 or LLOCK Out	1	I/O TS 8 mA	139	Can be programmed to be a configurable User I/O pin, USER1, or the Local Bus LLOCK Output pin, LLOCKo#. LLOCKo# indicates an atomic operation that may require multiple transactions to complete and can be used by the Local Bus to lock resources. Default functionality is USER1. Pin configuration occurs when the serial EEPROM contents are loaded following PCI reset, or upon subsequent writing to the CNTRL[4:3] register bits. The PCI 9050-1 asserts LLOCKo# during the first clock of an atomic operation (address cycle) and de-asserts it a minimum of one clock following the last bus access for the atomic operation. LLOCKo# is de-asserted after the PCI 9050-1 detects PCI FRAME#, with PCI LOCK# de-asserted at the same time.
USER2/CS2#	User I/O 2 or Chip Select 2 Out	1	I/O TS 8 mA	140	Can be programmed to be a configurable User I/O pin, USER2, or as the Chip Select 2 Output pin, CS2#. Default functionality is USER2. Pin configuration occurs when the serial EEPROM contents are loaded following PCI reset, or upon subsequent writing to the CNTRL[7:6] register bits.
USER3/CS3#	User I/O 3 or Chip Select 3 Out	1	I/O TS 8 mA	141	Can be programmed to be a configurable User I/O pin, USER3, or as the Chip Select 3 Output pin, CS3#. Default functionality is USER3. Pin configuration occurs when the serial EEPROM contents are loaded following PCI reset, or upon subsequent writing to the CNTRL[10:9] register bits.
Total		14			

Table 8-6. Mode-Independent Local Bus Data Transfer Pins

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
ADS#	Address Strobe	1	O TS 24 mA	123	Indicates valid address and the start of a new Bus access. Asserted for the first clock of a Bus access.
ALE	Address Latch Enable	1	O TS 8 mA	64	Asserted during the Address phase and de-asserted before the Data phase.
BLAST#	Burst Last	1	O TS 8 mA	124	Signal driven by the current Local Bus Master to indicate the last transfer in a Bus access. BLAST# is not asserted until internal wait states expire.
LRDYi#	Local Ready In	1	I PU100K	128	Local ready input indicates Read data is on the Local Bus, or that Write data is accepted. Used in conjunction with the programmable wait state generator. LRDYi# is not sampled until internal wait states expire. LRDYi# is ignored when BTERM# is enabled and asserted.
LW/R#	Write/Read	1	O TS 8 mA	127	Asserted low for reads and high for writes.
RD#	Read Strobe	1	O TS 24 mA	126	General purpose read strobe. The timing is controlled by the current Bus Region Descriptor register. Normally asserted during NRAD wait states, unless Read Strobe Delay clocks are programmed in bits [27:26]. Remains asserted throughout Burst and NRDD wait states.
WR#	Write Strobe	1	O TS 24 mA	125	General purpose write strobe. The timing is controlled by the current Bus Region Descriptor register. Normally asserted during NWAD wait states, unless Write Strobe Delay clocks are programmed in bits [29:28]. Remains asserted throughout Burst and NWDD wait states. The LAD data bus hold time can be extended beyond WR# de-assertion if Write Cycle Hold clocks are programmed in bits [31:30].
Total		7			

Table 8-7. Mode-Dependent Local Bus Data Transfer Pins

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
BTERM#	Burst Terminate	1	I PU100K	129	If disabled through the PCI 9050-1 Configuration registers, the PCI 9050-1 bursts up to four transactions, Lword transfer depends upon the bus width and type. If enabled, the PCI 9050-1 continues to burst until BTERM# input is asserted. BTERM# is a ready input that breaks up a Burst cycle and causes another Address cycle to occur. BTERM# is not sampled until internal wait states expire. LRDYi# is ignored when BTERM# is enabled and asserted.

Table 8-7. Mode-Dependent Local Bus Data Transfer Pins (Continued)

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
LA[27:2]	Address Bus	26	O TS 8 mA	122, 119-105, 102-100, 98-92	Carries the upper 26 bits of the 28-bit physical address bus. Increment during bursts indicate successive Data cycles.
LAD[31:0]	Data Bus	32	I/O TS 8 mA	52-62, 69-79, 82-91	During the Data phase, the Bus carries 32-, 16-, or 8-bit data quantities, depending on bus width configuration: • 8-bit = LAD[7:0] • 16-bit = LAD[15:0] • 32-bit = LAD[31:0] **J Mode Only**—During the Address phase, the Bus carries the 28-bit physical address (LAD[27:0]).
LBE[3:0]#	Byte Enables	4	O TS 24 mA	46-49	Byte enables are encoded based on configured bus width. **32-Bit Bus** The four byte enables indicate which of the four bytes are active during a data cycle: • LBE3# Byte Enable 3 = LAD[31:24] • LBE2# Byte Enable 2 = LAD[23:16] • LBE1# Byte Enable 1 = LAD[15:8] • LBE0# Byte Enable 0 = LAD[7:0] **16-Bit Bus** LBE[3, 1:0]# are encoded to provide BHE#, LA1, and BLE#, respectively. • LBE3# Byte High Enable (BHE#) = LAD[15:8] • LBE2# ***Not Used*** • LBE1# Address bit 1 (LA1) • LBE0# Byte Low Enable (BLE#) = LAD[7:0] **8-Bit Bus** LBE[1:0]# are encoded to provide LA1 and LA0, respectively: • LBE3# ***Not Used*** • LBE2# ***Not Used*** • LBE1# Address bit 1 (LA1) • LBE0# Address bit 0 (LA0)
Total		63			

9 ELECTRICAL SPECIFICATIONS

9.1 GENERAL ELECTRICAL SPECIFICATIONS

Table 9-1. Absolute Maximum Ratings

Specification	Maximum Rating
Storage Temperature	-65 to +150 °C
Ambient Temperature with Power Applied	-55 to +125 °C
Supply Voltage to Ground	-0.5 to +7.0V
Input Voltage (V_{IN})	V_{SS} -0.5V V_{DD} +0.5V
Output Voltage (V_{OUT})	V_{SS} -0.5V V_{DD} +0.5V

Table 9-2. Operating Ranges

Ambient Temperature	Junction Temperature	Supply Voltage (V_{DD})	Input Voltage (V_{IN})	
			Min	Max
-40 to +85 °C	115 °C	5V ±5%	V_{SS}	V_{DD}

Table 9-3. Capacitance (Sample Tested Only)

Parameter	Test Conditions	Pin Type	Typical Value	Units
C_{IN}	V_{IN} = 2.0V f = 1 MHz	Input	5	pF
C_{OUT}	V_{OUT} = 2.0V f = 1 MHz	Output	10	pF

Table 9-4. Electrical Characteristics over Operating Range

Parameter	Description	Test Conditions		Min	Max	Units
V_{OH}	Output High Voltage	V_{DD} = Min V_{IN} = V_{IH} or V_{IL}	I_{OH} = -4.0 mA	2.4	—	V
V_{OL}	Output Low Voltage		I_{OL} = per Tables	—	0.4	V
V_{IH}	Input High Level	—	—	2.0	—	V
V_{IL}	Input Low Level	—	—	—	0.8	V
I_{LI}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{DD}$, V_{DD} = Max		-10	+10	µA
I_{OZ}	Three-State Output Leakage Current	$V_{SS} \le V_{IN} \le V_{DD}$, V_{DD} = Max		-10	+10	µA
I_{CC}	Power Supply Current	V_{DD} = 5.25V, PCLK = LCLK = 33 MHz		—	130	mA

9.2 LOCAL INPUTS

Local Bus Input Setup and Hold Times (Figure 9-1):

- Hold time = 2 ns min
- Setup time = 8 ns max

Definitions:

- **T_{HOLD}**—Time that an input signal is stable after the rising edge of LCLK.
- **T_{SETUP}**—Setup time. The time that an input signal is stable before the rising edge of LCLK.

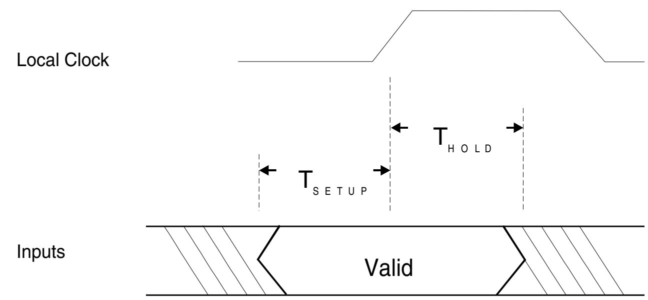


Figure 9-1. PCI 9050-1 Local Input Setup and Hold Waveform

Table 9-5. AC Electrical Characteristics (Local Inputs) over Operating Range

Frequency	Min	Max
Local Clock Input	0	40 MHz
PCI Clock Input	0	33 MHz

9.3 LOCAL OUTPUTS

Definition:

- **T_{VALID}**—Output valid (clock-to-out). The time after the rising edge of LCLK until the output is stable.

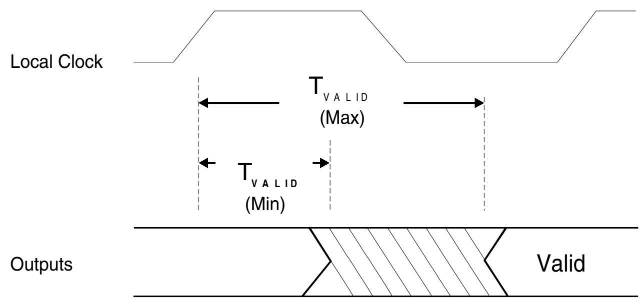


Figure 9-2. PCI 9050-1 Local Output Delay

Table 9-6. AC Electrical Characteristics (Local Outputs) over Operating Range

Signals (Synchronous Outputs) C_L = 50 pF, V_{CC} = 5.0 ±5%	T_{VALID} (Min) ns (Hold)	T_{VALID} ns Typical Min/Max	T_{VALID} (Max) ns (Worst Case)
ADS#	3	8	10
BCLKO	2	7	8
BLAST#	5	9	16
CS[1:0]#	4	11	17
LA[27:2]	5	10	14
LAD[31:0]	5	11	16
LBE[3:0]#	4	10	15
LHOLDA	3	—	9
LRESET#	5*	14	17*
LW/R#	4	7	12
RD#	7	16	27
USER0/WAITO#	4*	5 PCLK/8	12*
USER1/LLOCKo#	4*	5 PCLK/8	12*
USER2/CS2#	5*	5 PCLK/11	17*
USER3/CS3#	5*	5 PCLK/11	17*
WR#	4	8	13

Note: *The values followed with an asterisk (*) are referenced from the PCI Bus.*

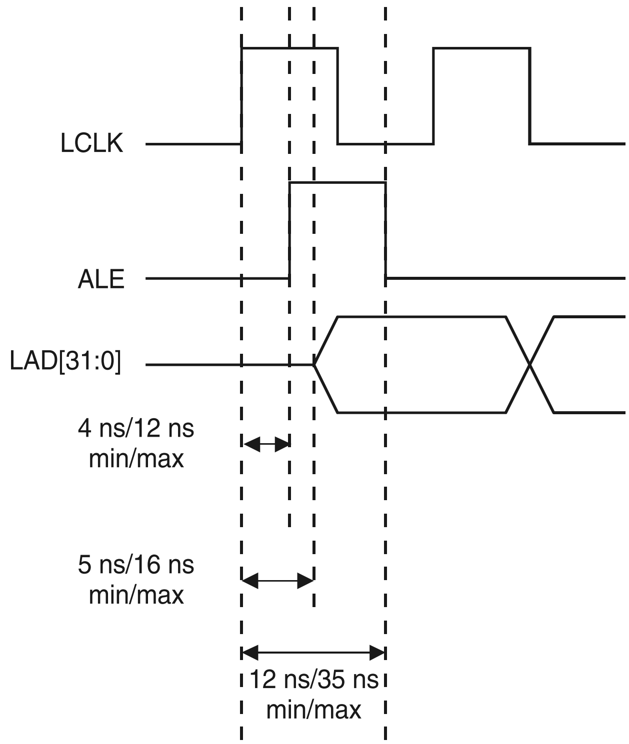


Figure 9-3. PCI 9050-1 ALE Output Delay (Min/Max) to the Local Clock

Note: *The ALE pulse width is independent of clock frequency.*

Table 9-7. ALE Operation

Signal	T_{VALID} (ns) from Local Clock Min/Max	Pulse Width (ns) Min/Max
ALE	4 / 12	8 / 23
LAD[31:0]	5 / 16	N/A

10 PHYSICAL SPECIFICATIONS

10.1 MECHANICAL LAYOUT

For 160-pin PQFP

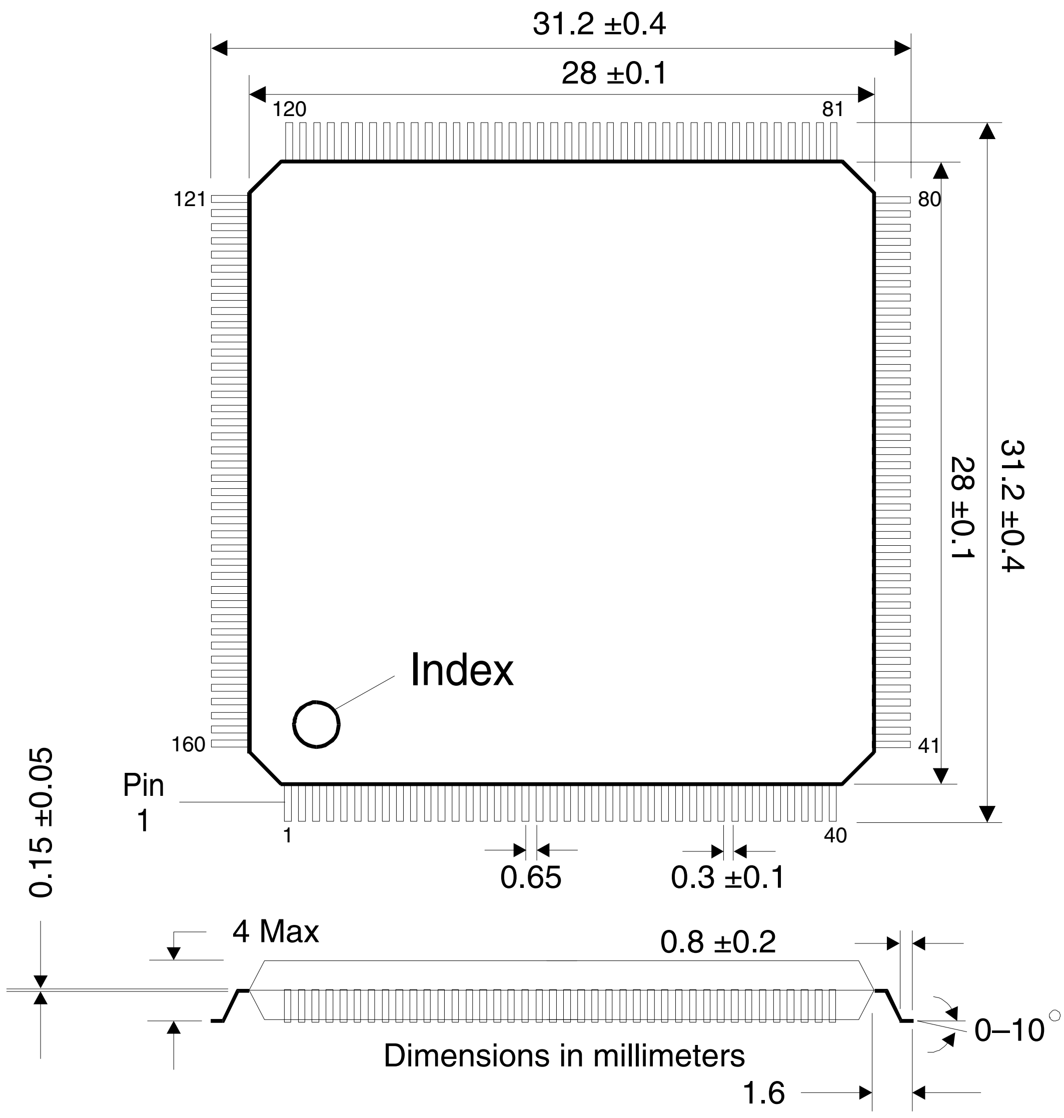


Figure 10-1. Mechanical Dimensions and Package Outline

10.2 TYPICAL ADAPTER BLOCK DIAGRAM

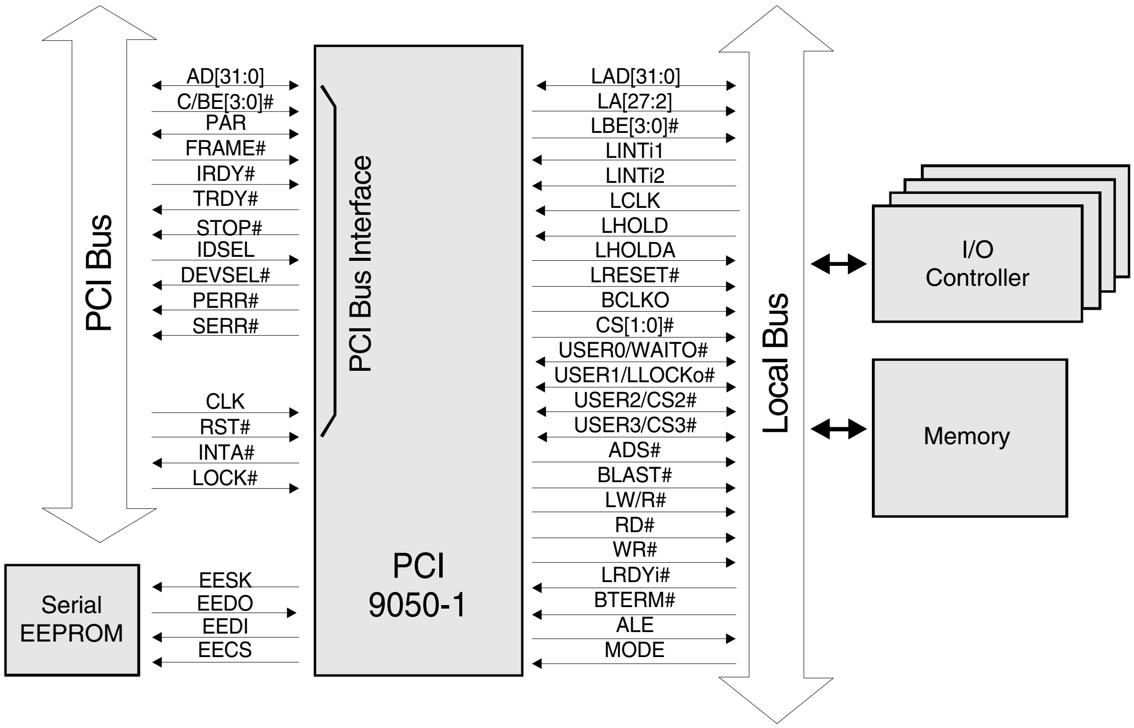


Figure 10-2. PCI 9050-1 Block Diagram

10.3 PIN ASSIGNMENTS

Refer to Section 8 for pin descriptions.

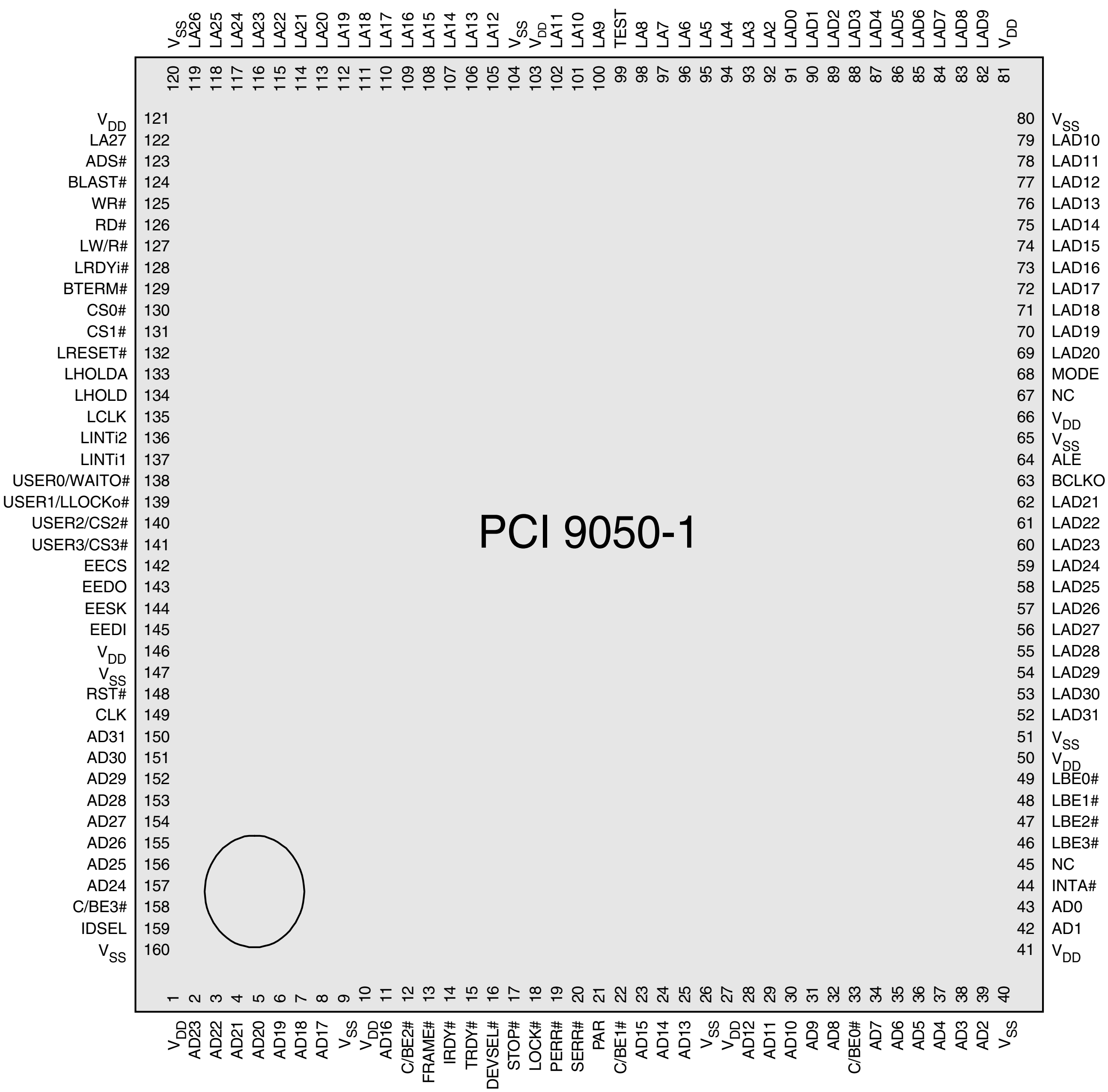


Figure 10-3. Pin Assignments

A GENERAL INFORMATION

The PLX PCI 9050 family provides low cost connectivity for PCI slave designs. It is specifically targeted at easing the transition of existing ISA designs to the more feature-rich and performance-oriented PCI Bus. The PCI 9050-1 provides Direct Slave PCI functions by interfacing the adapter's I/O circuitry (control, address, and data lines) to a host computer's microprocessor/memory architecture by way of the 32-bit PCI Bus, which typically runs at 33 MHz.

A.1 ORDERING INSTRUCTIONS

Continuing its drive to provide single-chip PCI interfaces for every market, PLX offers to designers its PCI 9050-1 Bus Target Interface Chip for low cost adapters.

Package	Ordering Part Number
160-pin PQFP	PCI 9050-1

A.2 UNITED STATES AND INTERNATIONAL REPRESENTATIVES, AND DISTRIBUTORS

A list of PLX Technology, Inc., representatives and distributors can be found at http://www.plxtech.com.

A.3 TECHNICAL SUPPORT

PLX Technology, Inc., technical support information is listed at http://www.plxtech.com; or call 408 774-9060 or 800 759-3735.

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