8Mb
ZBT® SRAM

MT55L512L18F, MT55L512V18F,
MT55L256L32F, MT55L256V32F,
MT55L256L36F, MT55L256V36F

3.3V V$_{DD}$, 3.3V or 2.5V I/O

FEATURES
- High frequency and 100 percent bus utilization
- Fast cycle times: 10ns, 11ns and 12ns
- Single +3.3V ±5% power supply (V$_{DD}$)
- Separate +3.3V or +2.5V isolated output buffer supply (V$_{DDQ}$)
- Advanced control logic for minimum control signal interface
- Individual BYTE WRITE controls may be tied LOW
- Single R/W# (read/write) control pin
- CKE# pin to enable clock and suspend operations
- Three chip enables for simple depth expansion
- Clock-controlled and registered addresses, data I/Os and control signals
- Internally self-timed, fully coherent WRITE
- Internally self-timed, registered outputs to eliminate the need to control OE#
- SNOOZE MODE for reduced-power standby
- Common data inputs and data outputs
- Linear or Interleaved Burst Modes
- Burst feature (optional)
- Pin/function compatibility with 2Mb, 4Mb, and 18Mb ZBT SRAM
- 100-pin TQFP
- 165-pin FBGA
- 119-pin BGA package
- Automatic power-down

OPTIONS   MARKING*
- Timing (Access/Cycle/MHz)
    7.5ns/10ns/100 MHz   -10
    8.5ns/11ns/90 MHz   -11
    9ns/12ns/83 MHz   -12
- Configurations
  3.3V I/O
    512K x 18   MT55L512L18F
    256K x 32   MT55L256L32F
    256K x 36   MT55L256L36F
  2.5V I/O
    512K x 18   MT55L512V18F
    256K x 32   MT55L256V32F
    256K x 36   MT55L256V36F
- Package
  100-pin TQFP   T
  165-pin FBGA   F
  119-pin, 14mm x 22mm BGA   B
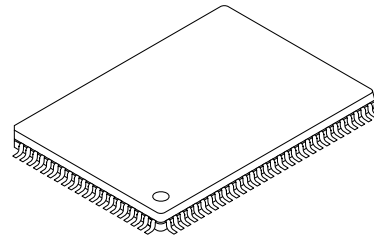- Operating Temperature Range
  Commercial (0°C to +70°C)   None
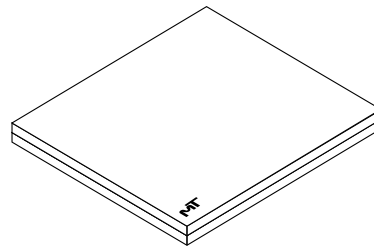 Industrial (-40°C to +85°C)**   IT
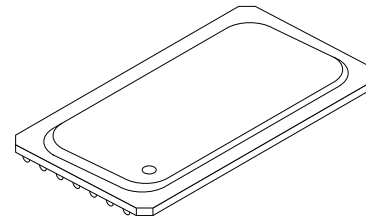
100-Pin TQFP[1]

165-Pin FBGA
(Preliminary Package Data)

119-Pin BGA[2]

**NOTE:** 1. JEDEC-standard MS-026 BHA (LQFP).
2. JEDEC-standard MS-028 BHA (PBGA).

Part Number Example:
MT55L256L32FT-11

* A Part Marking Guide for the FBGA devices can be found on Micron's Web site—http://www.micron.com/support/index.html.

** Industrial temperature range offered in specific speed grades and confgurations. Contact factory for more information.

MICRON™

FUNCTIONAL BLOCK DIAGRAM
512K x 18
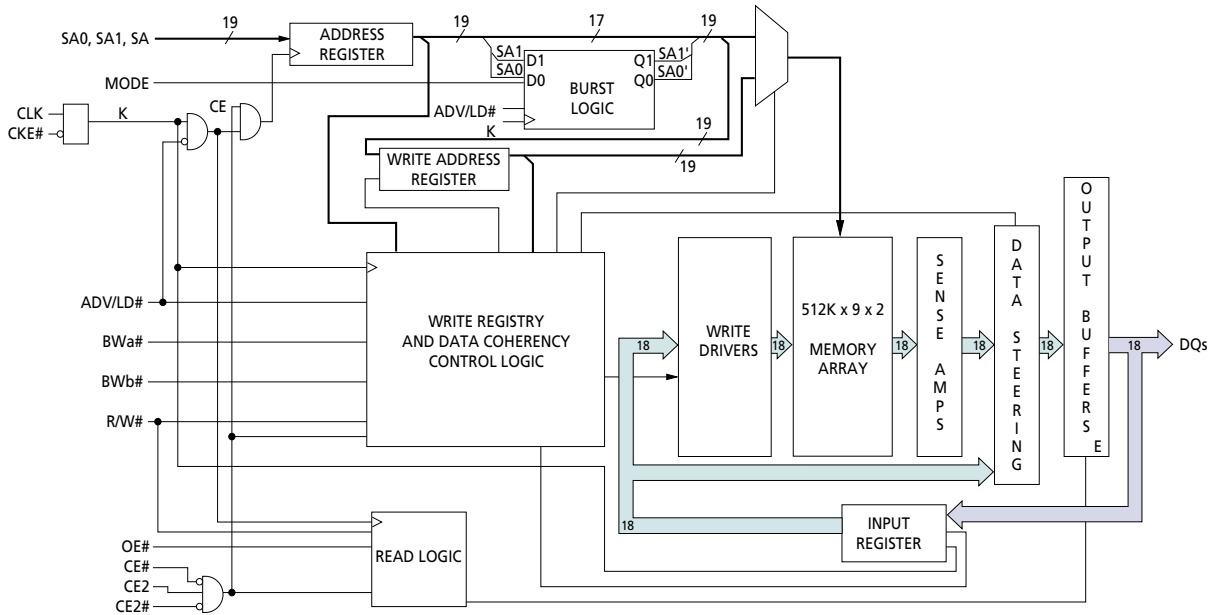
FUNCTIONAL BLOCK DIAGRAM
256K x 32/36
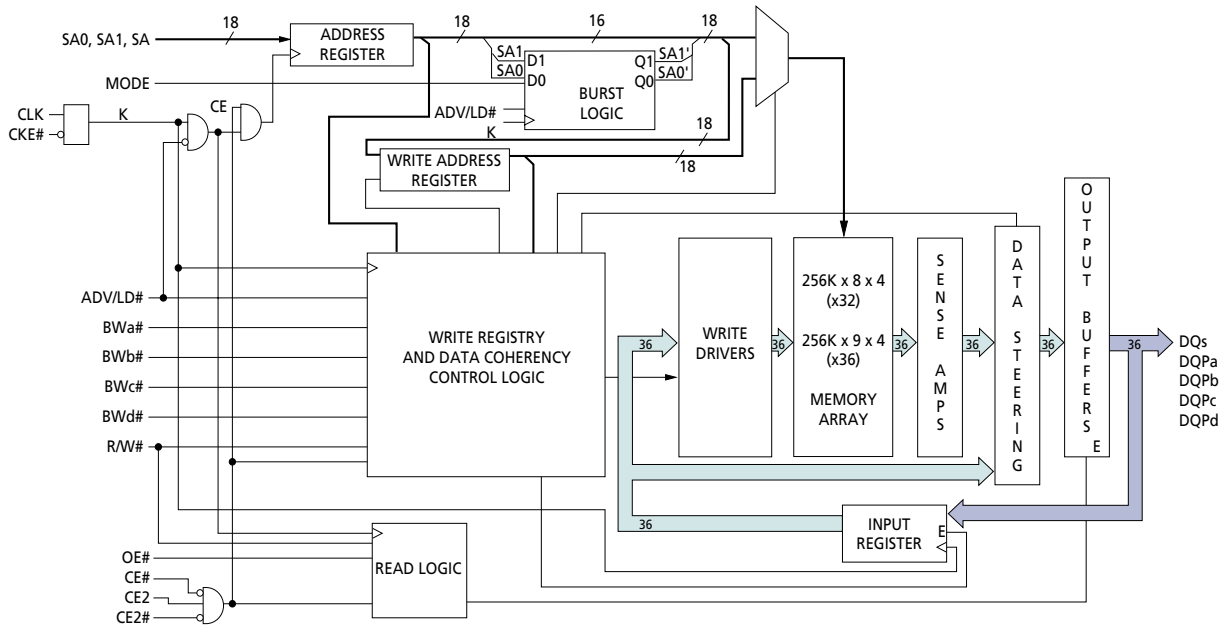
NOTE: Functional block diagrams illustrate simplified device operation. See truth table, pin descriptions, and timing diagrams for detailed information.

GENERAL DESCRIPTION

The Micron® Zero Bus Turnaround™ (ZBT®) SRAM family employs high-speed, low-power CMOS designs using an advanced CMOS process.

Micron's 8Mb ZBT SRAMs integrate a 512K x 18, 256K x 32, or 256K x 36 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. These SRAMs are optimized for 100 percent bus utilization, eliminating any turnaround cycles for READ to WRITE, or WRITE to READ, transitions. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, chip enable (CE#), two additional chip enables for easy depth expansion (CE2, CE2#), cycle start input (ADV/LD#), synchronous clock enable (CKE#), byte write enables (BWa#, BWb#, BWc#, and BWd#), and read/write (R/W#).

Asynchronous inputs include the output enable (OE#, which may be tied LOW for control signal mini-mization), clock (CLK), and snooze enable (ZZ, which may be tied LOW if unused). There is also a burst mode pin (MODE) that selects between interleaved and linear burst modes. MODE may be tied HIGH, LOW, or left unconnected if burst is unused. The flow-through data-out (Q) is enabled by OE#. WRITE cycles can be from one to four bytes wide as controlled by the write control inputs.

All READ, WRITE, and DESELECT cycles are initi-ated by the ADV/LD# input. Subsequent burst ad-dresses can be internally generated as controlled by the burst advance pin (ADV/LD#). Use of burst mode is optional. It is allowable to give an address for each individual READ and WRITE cycle. BURST cycles wrap around after the fourth access from a base address.

To allow for continuous, 100 percent use of the data bus, the flow-through ZBT SRAM uses a LATE WRITE cycle. For example, if a WRITE cycle begins in clock cycle one, the address is present on rising edge one. BYTE WRITEs need to be asserted on the same cycle as the address. The write data associated with the address is required one cycle later, or on the rising edge of clock cycle two.

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. During a BYTE WRITE cycle, BWa# controls DQa pins; BWb# controls DQb pins; BWc# controls DQc pins; and BWd# controls DQd pins. Cycle types can only be defined when an address is loaded, i.e., when ADV/LD# is LOW. Parity/ECC bits are available only on the x18 and x36 versions.

Micron's 8Mb ZBT SRAMs operate from a +3.3V V_DD power supply, and all inputs and outputs are LVTTL-compatible. Users can choose either a 3.3V or 2.5V I/O version. The device is ideally suited for systems requir-ing high bandwidth and zero bus turnaround delays.

Please refer to the Micron Web site (www.micron.com/datasheets) for the latest data sheet.

TQFP PIN ASSIGNMENT TABLE

PIN #	x18	x32	x36
1	NC	NF	DQPc
2	NC	DQc	DQc
3	NC	DQc	DQc
4	VDDQ		
5	Vss		
6	NC	DQc	DQc
7	NC	DQc	DQc
8	DQb	DQc	DQc
9	DQb	DQc	DQc
10	Vss		
11	VDDQ		
12	DQb	DQc	DQc
13	DQb	DQc	DQc
14	Vss^1		
15	VDD		
16	VDD^2		
17	Vss		
18	DQb	DQd	DQd
19	DQb	DQd	DQd
20	VDDQ		
21	Vss		
22	DQb	DQd	DQd
23	DQb	DQd	DQd
24	DQb	DQd	DQd
25	NC	DQd	DQd

PIN #	x18	x32	x36
26	Vss		
27	VDDQ		
28	NC	DQd	DQd
29	NC	DQd	DQd
30	NC	NF	DQPd
31	MODE (LBO#)		
32	SA		
33	SA		
34	SA		
35	SA		
36	SA1		
37	SA0		
38	DNU		
39	DNU		
40	Vss		
41	VDD		
42	DNU		
43	DNU		
44	SA		
45	SA		
46	SA		
47	SA		
48	SA		
49	SA		
50	SA		

PIN #	x18	x32	x36
51	NC	NF	DQPa
52	NC	DQa	DQa
53	NC	DQa	DQa
54	VDDQ		
55	Vss		
56	NC	DQa	DQa
57	NC	DQa	DQa
58		DQa	DQa
59		DQa	DQa
60	Vss		
61	VDDQ		
62		DQa	DQa
63		DQa	DQa
64	ZZ		
65	VDD		
66	Vss		
67	Vss		
68	DQa	DQb	DQb
69	DQa	DQb	DQb
70	VDDQ		
71	Vss		
72	DQa	DQb	DQb
73	DQa	DQb	DQb
74	DQa	DQb	DQb
75	NC	DQb	DQb

PIN #	x18	x32	x36
76	Vss		
77	VDDQ		
78	NC	DQb	DQb
79	NC	DQb	DQb
80	SA	NF	DQPb
81	SA		
82	SA		
83	SA		
84	NF^3		
85	ADV/LD#		
86	OE# (G#)		
87	CKE#		
88	R/W#		
89	CLK		
90	Vss		
91	VDD		
92	CE2#		
93	BWa#		
94	BWb#		
95	NC	BWc#	BWc#
96	NC	BWd#	BWd#
97	CE2		
98	CE#		
99	SA		
100	SA		

NOTE:
1. Pins 14 and 66 do not have to be connected directly to Vss if the input voltage is $\leq V_{IL}$.
2. Pins 16 does not have to be connected directly to VDD if the input voltage is $\geq V_{IH}$.
3. Pin 84 is reserved for address expansion to 18Mb device.

PIN ASSIGNMENT (TOP VIEW)
100-PIN TQFP

x18

Top pins (80–51): SA, NC, NC, VDDQ, Vss, NC, DQa, DQa, DQa, Vss, VDDQ, DQa, Vss, Vss1, VDD, ZZ, DQa, DQa, VDDQ, Vss, DQa, DQa, NC, NC, Vss, VDDQ, NC, NC, NC

Left pins 81–100:
Pin	Signal
81	SA
82	SA
83	SA
84	NF[3]
85	ADV/LD#
86	OE# (G#)
87	CKE#
88	R/W#
89	CLK
90	Vss
91	VDD
92	CE2#
93	BWa#
94	BWb#
95	NC
96	NC
97	CE2
98	CE#
99	SA
100	SA

Right pins 50–31:
Pin	Signal
50	SA
49	SA
48	SA
47	SA
46	SA
45	SA
44	SA
43	DNU
42	DNU
41	VDD
40	Vss
39	DNU
38	DNU
37	SA0
36	SA1
35	SA
34	SA
33	SA
32	SA
31	MODE (LBO#)

Bottom pins (1–30): NC, NC, NC, VDDQ, Vss, NC, DQb, DQb, Vss, VDDQ, DQb, DQb, Vss1, VDD, DQb2, DQb, VDDQ, Vss, DQb, DQb, NC, Vss, VDDQ, NC, NC, NC

x32/x36

Top pins (80–51): NF/DQPb[4], DQb, DQb, VDDQ, Vss, DQb, DQb, DQb, Vss, VDDQ, DQb, Vss, Vss1, VDD, ZZ, DQa, DQa, VDDQ, Vss, DQa, DQa, DQa, Vss, VDDQ, DQa, DQa, NF/DQPa[4]

Left pins 81–100:
Pin	Signal
81	SA
82	SA
83	SA
84	NF[3]
85	ADV/LD#
86	OE# (G#)
87	CKE#
88	R/W#
89	CLK
90	Vss
91	VDD
92	CE2#
93	BWa#
94	BWb#
95	BWc#
96	BWd#
97	CE2
98	CE#
99	SA
100	SA

Right pins 50–31:
Pin	Signal
50	SA
49	SA
48	SA
47	SA
46	SA
45	SA
44	SA
43	DNU
42	DNU
41	VDD
40	Vss
39	DNU
38	DNU
37	SA0
36	SA1
35	SA
34	SA
33	SA
32	SA
31	MODE (LBO#)

Bottom pins (1–30): NF/DQPc[4], DQc, DQc, VDDQ, Vss, DQc, DQc, DQc, Vss, VDDQ, DQc, Vss1, VDD, VDD2, Vss, DQd, VDDQ, DQd, DQd, DQd, Vss, VDDQ, DQd, NF/DQPd[4]

NOTE:
1. Pins 14 and 66 do not have to be connected directly to Vss if the input voltage is $\leq$ VIL.
2. Pins 16 does not have to be connected directly to VDD if the input voltage is $\geq$ VIH.
3. Pin 84 is reserved for address expansion to 18Mb device.
4. NF for x32 version, DQPx for x36 version.

TQFP PIN DESCRIPTIONS

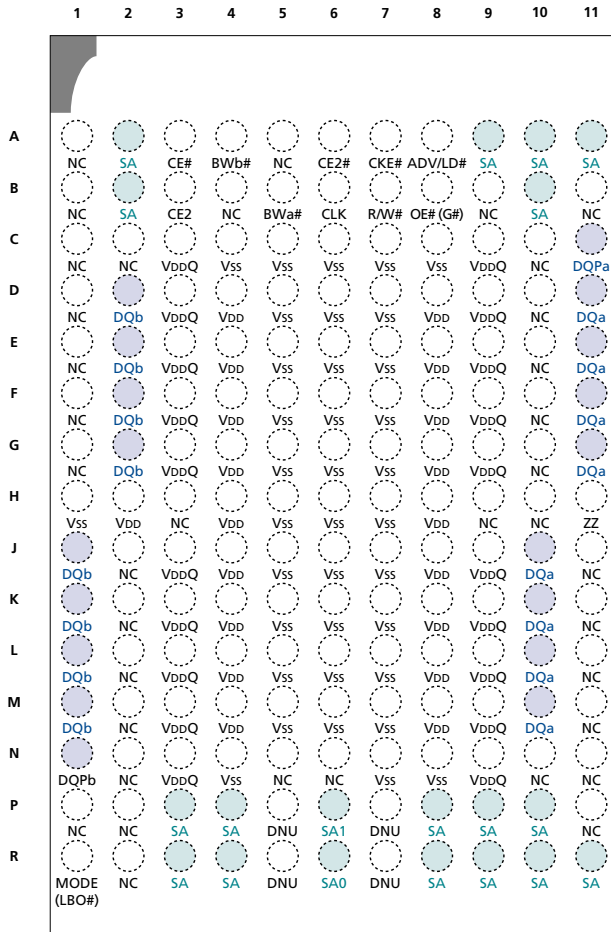| x18	x32/x36	SYMBOL	TYPE	DESCRIPTION
37 36 32-35, 44-50, 80-83, 99, 100	37 36 32-35, 44-50, 81-83, 99, 100	SA0 SA1 SA	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK. Pin 84 is reserved as an address bit for the higher-density 18Mb ZBT SRAM. SA0 and SA1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.
93 94 – –	93 94 95 96	BWa# BWb# BWc# BWd#	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written when a WRITE cycle is active and must meet the setup and hold times around the rising edge of CLK. BYTE WRITEs need to be asserted on the same cycle as the address. BWa# controls DQa pins; BWb# controls DQb pins; BWc# controls DQc pins; BWd# controls DQd pins.
89	89	CLK	Input	Clock: This signal registers the address, data, chip enables, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
98	98	CE#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and is sampled only when a new external address is loaded (ADV/LD# is LOW).
92	92	CE2#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and is sampled only when a new external address is loaded (ADV/LD# is LOW). This input can be used for memory depth expansion.
97	97	CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device and is sampled only when a new external address is loaded (ADV/LD# is LOW). This input can be used for memory depth expansion.
86	86	OE# (G#)	Input	Output Enable: This active LOW, asynchronous input enables the data I/O output drivers. G# is the JEDEC-standard term for OE#.
85	85	ADV/LD#	Input	Synchronous Address Advance/Load: When HIGH, this input is used to advance the internal burst counter, controlling burst access after the external address is loaded. When ADV/LD# is HIGH, R/W# is ignored. A LOW on ADV/LD# clocks a new address at the CLK rising edge.
87	87	CKE#	Input	Synchronous Clock Enable: This active LOW input permits CLK to propagate throughout the device. When CKE is HIGH, the device ignores the CLK input and effectively internally extends the previous CLK cycle. This input must meet setup and hold times around the rising edge of CLK.
64	64	ZZ	Input	Snooze Enable: This active HIGH, asynchronous input causes the device to enter a low-power standby mode in which all data in the memory array is retained. When ZZ is active, all other inputs are ignored.

TQFP PIN DESCRIPTIONS (CONTINUED)

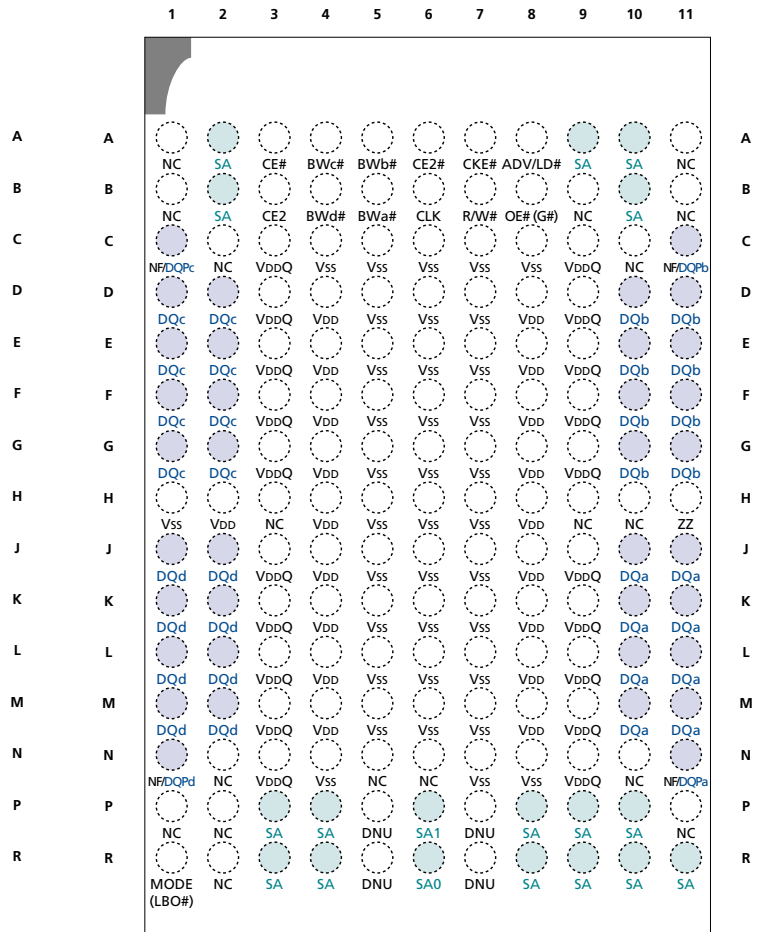| x18	x32/x36	SYMBOL	TYPE	DESCRIPTION
88	88	R/W#	Input	Read/Write: This input determines the cycle type when ADV/LD# is LOW and is the only means for determining READs and WRITEs. READ cycles may not be converted into WRITEs (and vice versa) other than by loading a new address. A LOW on this pin permits BYTE WRITE operations and must meet the setup and hold times around the rising edge of CLK. Full bus-width WRITEs occur if all byte write enables are LOW.
31	31	MODE (LBO#)	Input	Mode: This input selects the burst sequence. A LOW on this pin selects linear burst. NC or HIGH on this pin selects interleaved burst. Do not alter input state while device is operating. LBO# is the JEDEC-standard term for MODE.
(a) 58, 59, 62, 63, 68, 69, 72-74 (b) 8, 9, 12, 13, 18, 19, 22-24	(a) 52, 53, 56-59, 62, 63 (b) 68, 69, 72-75, 78, 79 (c) 2, 3, 6-9, 12, 13 (d) 18, 19, 22-25, 28, 29	DQa DQb DQc DQd	Input/ Output	SRAM Data I/Os: Byte "a" is associated with DQa pins; Byte "b" is associated with DQb pins; Byte "c" is associated with DQc pins; Byte "d" is associated with DQd pins. Input data must meet setup and hold times around the rising edge CLK.
n/a	51 80 1 30	NF/DQPa NF/DQPb NF/DQPc NF/DQPd	NF/ I/O	No Function/Data Bits: On the x32 version, these pins are No Function (NC) and can be left floating or connected to GND to minimize thermal impedance. On the x36 version, these bits are DQs.
15, 16, 41, 65, 91	15, 16, 41, 65, 91	V_{DD}	Supply	Power Supply: See DC Electrical Characteristics and Operating Conditions for range.
4, 11, 20, 27, 54, 61, 70, 77	4, 11, 20, 27, 54, 61, 70, 77	V_{DDQ}	Supply	Isolated Output Buffer Supply: See DC Electrical Characteristics and Operating Conditions for range.
5, 10, 14, 17, 21, 26, 40, 55, 60, 66, 67, 71, 76, 90	5, 10, 14, 17, 21, 26, 40, 55, 60, 66, 67, 71, 76, 90	V_{SS}	Supply	Ground: GND.
1-3, 6, 7, 25, 28-30, 51-53, 56, 57, 75, 78, 79, 95, 96	n/a	NC	–	No Connect: These pins can be left floating or connected to GND to minimize thermal impedance.
38, 39, 42, 43	38, 39, 42, 43	DNU	–	Do Not Use: These signals may either be unconnected or wired to GND to minimize thermal impedance.
84	84	NF	–	No Function: This pin is internally connected to the die and will have the capacitance of an input pin. It is allowable to leave this pin unconnected or driven by signals. Pin 84 is reserved as an address pin for the 18Mb ZBT SRAM.

PIN LAYOUT (TOP VIEW)
165-PIN FBGA

x18

	1	2	3	4	5	6	7	8	9	10	11
A	NC	SA	CE#	BWb#	NC	CE2#	CKE#	ADV/LD#	SA	SA	SA
B	NC	SA	CE2	NC	BWa#	CLK	R/W#	OE# (G#)	NC	SA	NC
C	NC	NC	VDDQ	Vss	Vss	Vss	Vss	Vss	VDDQ	NC	DQPa
D	NC	DQb	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	NC	DQa
E	NC	DQb	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	NC	DQa
F	NC	DQb	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	NC	DQa
G	NC	DQb	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	NC	DQa
H	Vss	VDD	NC	VDD	Vss	Vss	Vss	VDD	NC	NC	ZZ
J	DQb	NC	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQa	NC
K	DQb	NC	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQa	NC
L	DQb	NC	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQa	NC
M	DQb	NC	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQa	NC
N	DQPb	NC	VDDQ	Vss	NC	NC	Vss	Vss	VDDQ	NC	NC
P	NC	NC	SA	SA	DNU	SA1	DNU	SA	SA	SA	NC
R	MODE (LBO#)	NC	SA	SA	DNU	SA0	DNU	SA	SA	SA	SA

TOP VIEW

x32/x36

	1	2	3	4	5	6	7	8	9	10	11
A	NC	SA	CE#	BWc#	BWb#	CE2#	CKE#	ADV/LD#	SA	SA	NC
B	NC	SA	CE2	BWd#	BWa#	CLK	R/W#	OE# (G#)	NC	SA	NC
C	NF/DQPc	NC	VDDQ	Vss	Vss	Vss	Vss	Vss	VDDQ	NC	NF/DQPb
D	DQc	DQc	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQb	DQb
E	DQc	DQc	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQb	DQb
F	DQc	DQc	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQb	DQb
G	DQc	DQc	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQb	DQb
H	Vss	VDD	NC	VDD	Vss	Vss	Vss	VDD	NC	NC	ZZ
J	DQd	DQd	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQa	DQa
K	DQd	DQd	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQa	DQa
L	DQd	DQd	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQa	DQa
M	DQd	DQd	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQa	DQa
N	NF/DQPd	NC	VDDQ	Vss	NC	NC	Vss	Vss	VDDQ	NC	NF/DQPa
P	NC	NC	SA	SA	DNU	SA1	DNU	SA	SA	SA	NC
R	MODE (LBO#)	NC	SA	SA	DNU	SA0	DNU	SA	SA	SA	SA

TOP VIEW

*No Function (NF) is used on the x32 version. Parity (DQPx) is used on the x36 version.
NOTE: Pin 9B is reserved for address expansion to 18Mb.

FBGA PIN DESCRIPTIONS

x18	x32/x36	SYMBOL	TYPE	DESCRIPTION
6R 6P 2A, 9A, 2B, 3P, 3R, 4P, 4R, 8P, 8R, 9P, 9R, 10A, 10B, 10P, 10R, 11A, 11R	6R 6P 2A, 9A, 2B, 3P, 3R, 4P, 4R, 8P, 8R, 9P, 9R, 10A, 10B, 10P, 10R, 11R	SA0 SA1 S A	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
5B 4A – –	5B 5A 4A 4B	BWa# BWb# BWc# BWd#	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A byte write enable is LOW for a WRITE cycle and HIGH for a READ cycle. For the x18 version, BWa# controls DQa's and DQPa; BWb# controls DQb's and DQPb. For the x32 and x36 versions, BWa# controls DQa's and DQPa; BWb# controls DQb's and DQPb; BWc# controls DQc's and DQPc; BWd# controls DQd's and DQPd. Parity is only available on the x18 and x36 versions.
7A	7A	CKE#	Input	Synchronous Clock Enable: This active LOW input permits CLK to propogate throughout the device. When CKE# is HIGH, the device ignores the CLK input and effectively internally extends the previous CLK cycle. This input must meet the setup and hold times around the rising edge of CLK.
7B	7B	R/W#	Input	Read/Write: This input determines the cycle type when ADV/LD# is LOW and is the only means for determining READs and WRITEs. READ cycles may not be converted into WRITEs (and vice versa) other than by loading a new address. A LOW on this pin permits BYTE WRITE operations to meet the setup and hold times around the rising edge of CLK. Full bus-width WRITEs occur if all byte write enables are LOW.
6B	6B	CLK	Input	Clock: This signal registers the address, data, chip enable, byte write enables, and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
3A	3A	CE#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device. CE# is sampled only when a new external address is loaded. (ADV/LD# is LOW)
6A	6A	CE2#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and is sampled only when a new external address is loaded.
11H	11H	ZZ	Input	Snooze Enable: This active HIGH, asynchronous input causes the device to enter a low-power standby mode in which all data in the memory array is retained. When ZZ is active, all other inputs are ignored.
3B	3B	CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device and is sampled only when a new external address is loaded.
8B	8B	OE#(G#)	Input	Output Enable: This active LOW, asynchronous input enables the data I/O output drivers.

(continued on next page)

FBGA PIN DESCRIPTIONS (continued)

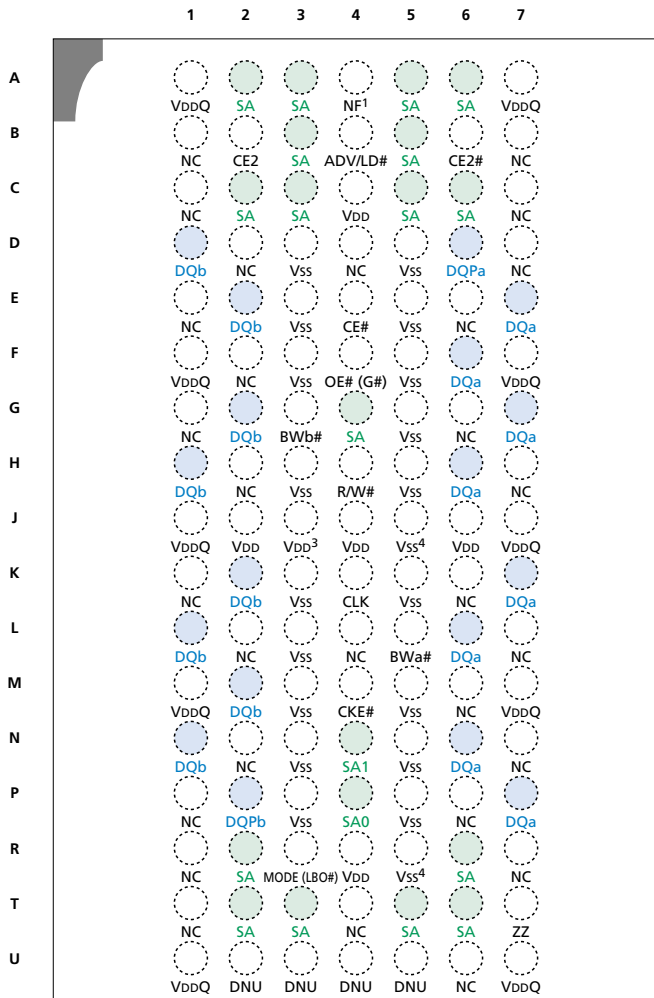| x18	x32/x36	SYMBOL	TYPE	DESCRIPTION
8A	8A	ADV/LD#	Input	Synchronous Address Advance/Load: When HIGH, this input is used to advance the internal burst counter, controlling burst access after the external address is loaded. When ADV/LD# is HIGH, R/W# is ingored. A LOW on ADV/LD# clocks a new address at the CLK rising edge.
1R	1R	MODE (LB0#)	Input	Mode: This input selects the burst sequence. A LOW on this input selects "linear burst." NC or HIGH on this input selects "interleaved burst." Do not alter input state while device is operating.
(a) 10J, 10K, 10L, 10M, 11D, 11E, 11F, 11G (b) 1J, 1K, 1L, 1M, 2D, 2E, 2F, 2G	(a) 10J, 10K, 10L, 10M, 11J, 11K, 11L, 11M (b) 10D, 10E, 10F, 10G, 11D, 11E, 11F, 11G (c) 1D, 1E, 1F, 1G, 2D, 2E, 2F, 2G (d) 1J, 1K, 1L, 1M, 2J, 2K, 2L, 2M	DQa DQb DQc DQd	Input/Output	SRAM Data I/Os: For the x18 version, Byte "a" is associated DQas; Byte "b" is associated with DQbs. For the x32 and x36 versions, Byte "a" is associated with DQas; Byte "b" is associated with DQbs; Byte "c" is associated with DQcs; Byte "d" is associated with DQds. Input data must meet setup and hold times around the rising edge of CLK.
11C 1N – –	11N 11C 1C 1N	NF/DQPa NF/DQPb NF/DQPc NF/DQPd	NF/I/O	No Function/Parity Data I/Os: On the x32 version, these are No Function (NF). On the x18 version, Byte "a" parity is DQPa; Byte "b" parity is DQPb. On the x36 version, Byte "a" parity is DQPa; Byte "b" parity is DQPb; Byte "c" parity is DQPc; Byte "d" parity is DQPd.
2H, 4D, 4E, 4F, 4G, 4H, 4J, 4K, 4L, 4M, 8D, 8E, 8F, 8G, 8H, 8J, 8K, 8L, 8M	2H, 4D, 4E, 4F, 4G, 4H, 4J, 4K, 4L, 4M, 8D, 8E, 8F, 8G, 8H, 8J, 8K, 8L, 8M	V_{DD}	Supply	Power Supply: See DC Electrical Characteristics and Operating Conditions for range.
3C, 3D, 3E, 3F, 3G, 3J, 3K, 3L, 3M, 3N, 9C, 9D, 9E, 9F, 9G, 9J, 9K, 9L, 9M, 9N	3C, 3D, 3E, 3F, 3G, 3J, 3K, 3L, 3M, 3N, 9C, 9D, 9E, 9F, 9G, 9J, 9K, 9L, 9M, 9N	V_{DDQ}	Supply	Isolated Output Buffer Supply: See DC Electrical Characteristics and Operating Conditions for range.

(continued on next page)

FBGA PIN DESCRIPTIONS (continued)

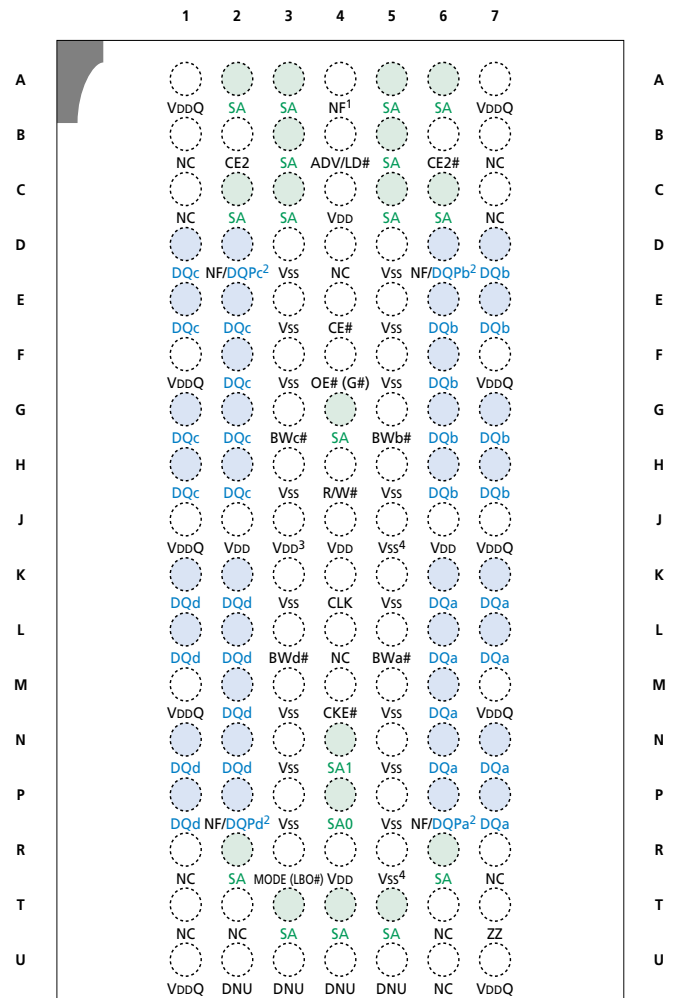| x18	x32/x36	SYMBOL	TYPE	DESCRIPTION
1H, 4C, 4N, 5C, 5D, 5E, 5F, 5G, 5H, 5J, 5K, 5L, 5M, 6C, 6D, 6E, 6F, 6G, 6H, 6J, 6K, 6L, 6M, 7C, 7D, 7E, 7F, 7G, 7H, 7J, 7K, 7L, 7M, 7N, 8C, 8N	1H, 4C, 4N, 5C, 5D, 5E, 5F, 5G, 5H, 5J, 5K, 5L, 5M, 6C, 6D, 6E, 6F, 6G, 6H, 6J, 6K, 6L, 6M, 7C, 7D, 7E, 7F, 7G, 7H, 7J, 7K, 7L, 7M, 7N, 8C, 8N	V_{SS}	Supply	Ground: GND.
5P, 5R, 7P, 7R	5P, 5R, 7P, 7R	DNU	–	Do Not Use: These signals may either be unconnected or wired to GND to improve package heat dissipation.
1A, 1B, 1C, 1D, 1E, 1F, 1G, 1P, 2C, 2J, 2K, 2L, 2M, 2N, 2P, 2R, 3H, 4B, 9B, 5A, 5N, 6N, 9H, 10C, 10D, 10E, 10F, 10G, 10H, 10N, 11B, 11J, 11K, 11L, 11M, 11N, 11P	1A, 1B, 1P, 2C, 2N, 2P, 2R, 3H, 5N, 6N, 9B, 9H, 10C, 10H, 10N, 11A, 11B, 11P	NC	–	No Connect: These signals are not internally connected and may be connected to ground to improve package heat dissipation. Pin 9B is reserved for 16MB address expansion.
		NF	—	No Function: These pins are internally connected to the die and have the capacitance of an input pin. It is allowable to leave these pins unconnected or driven by signals.

PIN LAYOUT (TOP VIEW)
119-PIN BGA

x18

	1	2	3	4	5	6	7
A	VDDQ	SA	SA	NF[1]	SA	SA	VDDQ
B	NC	CE2	SA	ADV/LD#	SA	CE2#	NC
C	NC	SA	SA	VDD	SA	SA	NC
D	DQb	NC	Vss	NC	Vss	DQPa	NC
E	NC	DQb	Vss	CE#	Vss	NC	DQa
F	VDDQ	NC	Vss	OE# (G#)	Vss	DQa	VDDQ
G	NC	DQb	BWb#	SA	Vss	NC	DQa
H	DQb	NC	Vss	R/W#	Vss	DQa	NC
J	VDDQ	VDD	VDD[3]	VDD	Vss[4]	VDD	VDDQ
K	NC	DQb	Vss	CLK	Vss	NC	DQa
L	DQb	NC	Vss	NC	BWa#	DQa	NC
M	VDDQ	DQb	Vss	CKE#	Vss	NC	VDDQ
N	DQb	NC	Vss	SA1	Vss	DQa	NC
P	NC	DQPb	Vss	SA0	Vss	NC	DQa
R	NC	SA	MODE (LBO#)	VDD	Vss[4]	SA	NC
T	NC	SA	SA	NC	SA	SA	ZZ
U	VDDQ	DNU	DNU	DNU	DNU	NC	VDDQ

TOP VIEW

x32/x36

	1	2	3	4	5	6	7
A	VDDQ	SA	SA	NF[1]	SA	SA	VDDQ
B	NC	CE2	SA	ADV/LD#	SA	CE2#	NC
C	NC	SA	SA	VDD	SA	SA	NC
D	DQc	NF/DQPc[2]	Vss	NC	Vss	NF/DQPb[2]	DQb
E	DQc	DQc	Vss	CE#	Vss	DQb	DQb
F	VDDQ	DQc	Vss	OE# (G#)	Vss	DQb	VDDQ
G	DQc	DQc	BWc#	SA	BWb#	DQb	DQb
H	DQc	DQc	Vss	R/W#	Vss	DQb	DQb
J	VDDQ	VDD	VDD[3]	VDD	Vss[4]	VDD	VDDQ
K	DQd	DQd	Vss	CLK	Vss	DQa	DQa
L	DQd	DQd	BWd#	NC	BWa#	DQa	DQa
M	VDDQ	DQd	Vss	CKE#	Vss	DQa	VDDQ
N	DQd	DQd	Vss	SA1	Vss	DQa	DQa
P	DQd	NF/DQPd[2]	Vss	SA0	Vss	NF/DQPa[2]	DQa
R	NC	SA	MODE (LBO#)	VDD	Vss[4]	SA	NC
T	NC	NC	SA	SA	SA	NC	ZZ
U	VDDQ	DNU	DNU	DNU	DNU	NC	VDDQ

TOP VIEW

NOTE:
1. Pin 4A is reserved for address expansion to 18Mb.
2. No Function (NF) is used on the x32 version. Parity (DQPx) is used on the x36 version.
3. Pin 3J does not have to be connected directly to V_{DD} if the input voltage is $\geq V_{IH}$.
4. Pins 5J and 5R do not have to be connected directly to V_{SS} if the input voltage is $\leq V_{IH}$.

BGA PIN DESCRIPTIONS

x18	x32/x36	SYMBOL	TYPE	DESCRIPTION
4P 4N 2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 2R, 6R, 2T, 3T, 5T, 6T	4P 4N 2A, 2C, 2R, 3A, 3B, 3C, 3T, 4T, 5A, 5B, 5C, 5T, 6A, 6C, 6R	SA0 SA1 S A	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
5L 3G – –	5L 5G 3G 3L	BWa# BWb# BWc# BWd#	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A byte write enable is LOW for a WRITE cycle and HIGH for a READ cycle. For the x18 version, BWa# controls DQa's and DQPa; BWb# controls DQb's and DQPb. For the x32 and x36 versions, BWa# controls DQa's and DQPa; BWb# controls DQb's and DQPb; BWc# controls DQc's and DQPc; BWd# controls DQd's and DQPd. Parity is only available on the x18 and x36 versions.
4M	4M	CKE#	Input	Synchronous Clock Enable: This active LOW input permits CLK to propagate throughout the device. When CKE# is HIGH, the device ignores the CK input and effectively internally extends the previous CLK cycle. This input must meet the setup and hold times around the rising edge of CLK.
4H	4H	R/W#	Input	Read/Write: This input determines the cycle type when ADV/LD# is lOW and is the only means for determining READs and WRITEs. READ cycles may not be converted into WRITEs (and vice versa) other than by loading a new address. A LOW on this pin permits BYTE WRITE operations must meet the setup and hold times around the rising edge of CLK. Full bus-width WRITEs occur if all byte write enables are LOW.
4K	4K	CLK	Input	Clock: This signal registers the address, data, chip enable, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
4E	4E	CE#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device. CE# is sampled only when a new external address is loaded.
6B	6B	CE2#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and is sampled only when a new external address is loaded.
7T	7T	ZZ	Input	Snooze Enable: This active HIGH, asynchronous input causes the device to enter a low-power standby mode in which all data in the memory array is retained. When ZZ is active, all other inputs are ignored.
2B	2B	CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device and is sampled only when a new external address is loaded.

BGA PIN DESCRIPTIONS (continued)

x18	x32/x36	SYMBOL	TYPE	DESCRIPTION
4F	4F	OE#	Input	Output Enable: This active LOW, asynchronous input enables the data I/O output drivers.
4B	4B	ADV#/LD#	Input	Synchronous Address Advance/Load: When HIGH, this input is used to advance the internal burst counter, controlling burst access after the external addressis loaded. When ADV#/LD# is HIGH, R/W# is ignored. A LOW on ADV/LD# clocks a new address at the CLK rising edge.
3R	3R	MODE	Input	Mode: This input selects the burst sequence. A LOW on this input selects "linear burst." NC or HIGH on this input selects "interleaved burst." Do not alter input state while device is operating.
4A	4A	NF	Input	No Function: These pins are internally connected to the die and will have the capacitance of input pins. It is allowable to leave these pins unconnected or driven by signals. These pins are reserved for address expansion; 4A becomes an SA at 18Mb density.
(a) 6F, 6H, 6L, 6N, 7E, 7G, 7K, 7P (b) 1D, 1H, 1L, 1N, 2E, 2G, 2K, 2M	(a) 6K, 6L, 6M, 6N, 7K, 7L, 7N, 7P (b) 6E, 6F, 6G, 6H, 7D, 7E, 7G, 7H (c) 1D, 1E, 1G, 1H, 2E, 2F, 2G, 2H (d) 1K, 1L, 1N, 1P, 2K, 2L, 2M, 2N	DQa DQb DQc DQd	Input/ Output	SRAM Data I/Os: For the x18 version, Byte "a" is DQa's; Byte "b" is DQb's. For the x32 and x36 versions, Byte "a" is DQa's; Byte "b" is DQb's; Byte "c" is DQc's; Byte "d" is DQd's. Input data must meet setup and hold times around the rising edge of CLK.
6D 2P – –	6P 6D 2D 2P	NF/DQPa NF/DQPb NF/DQPc NF/DQPd	NF/ I/O	No Function/Parity Data I/Os: On the x32 version, these are No Function (NF). On the x18 version, Byte "a" parity is DQPa; Byte "b" parity is DQPb. On the x36 version, Byte "a" parity is DQPa; Byte "b" parity is DQPb; Byte "c" parity is DQPc; Byte "d" parity is DQPd.
2J, 4C, 4J, 4R, 5R, 6J	2J, 4C, 4J, 4R, 5R, 6J	V_DD	Supply	Power Supply: See DC Electrical Characteristics and Operating Conditions for range.
1A, 1F, 1J, 1M, 1U, 7A, 7F, 7J, 7M, 7U	1A, 1F, 1J, 1M, 1U, 7A, 7F, 7J, 7M, 7U	V_DDQ	Supply	Isolated Output Buffer Supply: See DC Electrical Characteristics and Operating Conditions for range.

BGA PIN DESCRIPTIONS (continued)

x18	x32/x36	SYMBOL	TYPE	DESCRIPTION
3D, 3E, 3F, 3H, 3K, 3L, 3M, 3N, 3P, 5D, 5E, 5F, 5G, 5H, 5K, 5M, 5N, 5P	3D, 3E, 3F, 3H, 3K, 3M, 3N, 3P, 5D, 5E, 5F, 5H, 5K, 5M, 5N, 5P	V_{SS}	Supply	Ground: GND.
2U, 3U, 4U, 5U	2U, 3U, 4U, 5U	DNU	–	Do Not Use: These signals may either be unconnected or wired to GND to improve package heat dissipation.
1B, 1C, 1E, 1G, 1K, 1P, 1R, 1T, 2D, 2F, 2H, 2L, 2N, 3J, 4D, 4L, 4T, 5J, 6E, 6G, 6K, 6M, 6P, 6U, 7B, 7C, 7D, 7H, 7L, 7N, 7R	1B, 1C, 1R, 1T, 2T, 3J, 4D, 4L, 5J, 6T, 6U, 7B, 7C, 7R	NC	–	No Connect: These signals are not internally connected and may be connected to ground to improve package heat dissipation.
		NF	I/O	No Function: These pins are internally connected to the die and have the capacitance of an input pin. It is allowable to leave these pins unconnected or driven by signals.

INTERLEAVED BURST ADDRESS TABLE (MODE = NC OR HIGH)

FIRST ADDRESS (EXTERNAL)	SECOND ADDRESS (INTERNAL)	THIRD ADDRESS (INTERNAL)	FOURTH ADDRESS (INTERNAL)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X00	X...X11	X...X10
X...X10	X...X11	X...X00	X...X01
X...X11	X...X10	X...X01	X...X00

LINEAR BURST ADDRESS TABLE (MODE = LOW)

FIRST ADDRESS (EXTERNAL)	SECOND ADDRESS (INTERNAL)	THIRD ADDRESS (INTERNAL)	FOURTH ADDRESS (INTERNAL)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X10	X...X11	X...X00
X...X10	X...X11	X...X00	X...X01
X...X11	X...X00	X...X01	X...X10

PARTIAL TRUTH TABLE FOR READ/WRITE COMMANDS (x18)

FUNCTION	R/W#	BWa#	BWb#
READ	H	X	X
WRITE Byte "a"	L	L	H
WRITE Byte "b"	L	H	L
WRITE All Bytes	L	L	L
WRITE ABORT/NOP	L	H	H

NOTE: Using R/W# and byte write(s), any one or more bytes may be written.

PARTIAL TRUTH TABLE FOR READ/WRITE COMMANDS (x32/x36)

FUNCTION	R/W#	BWa#	BWb#	BWc#	BWd#
READ	H	X	X	X	X
WRITE Byte "a"	L	L	H	H	H
WRITE Byte "b"	L	H	L	H	H
WRITE Byte "c"	L	H	H	L	H
WRITE Byte "d"	L	H	H	H	L
WRITE All Bytes	L	L	L	L	L
WRITE ABORT/NOP	L	H	H	H	H

NOTE: Using R/W# and byte write(s), any one or more bytes may be written.

STATE DIAGRAM FOR ZBT SRAM
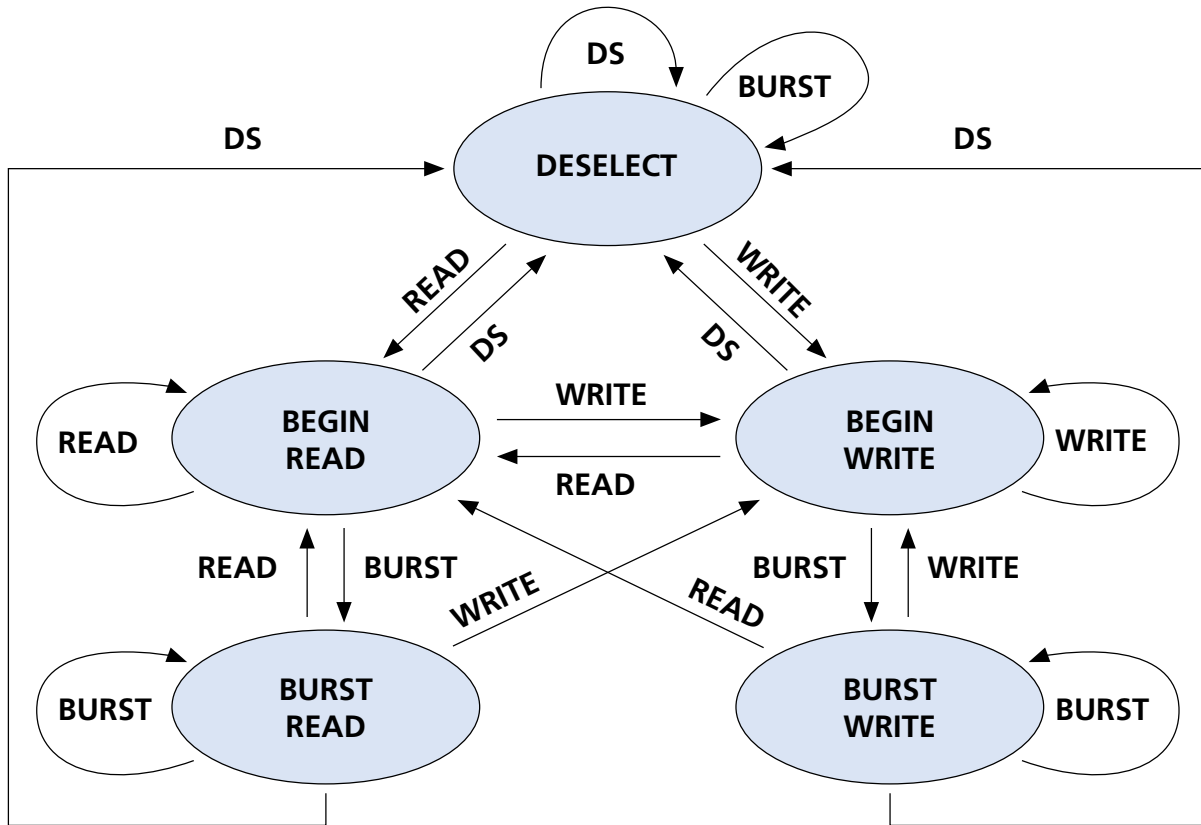
KEY:

COMMAND	OPERATION
DS	DESELECT
READ	New READ
WRITE	New WRITE
BURST	BURST READ, BURST WRITE or CONTINUE DESELECT

NOTE: 1. A STALL or IGNORE CLOCK EDGE cycle is not shown in the above diagram. This is because CKE# HIGH only blocks the clock (CLK) input and does not change the state of the device.
2. States change on the rising edge of the clock (CLK).

TRUTH TABLE

(Notes 5-10)

OPERATION	ADDRESS USED	CE#	CE2#	CE2	ZZ	ADV/LD#	R/W#	BWx	OE#	CKE#	CLK	DQ	NOTES
DESELECT Cycle	None	H	X	X	L	L	X	X	X	L	L-H	High-Z	
DESELECT Cycle	None	X	H	X	L	L	X	X	X	L	L-H	High-Z	
DESELECT Cycle	None	X	X	L	L	L	X	X	X	L	L-H	High-Z	
CONTINUE DESELECT Cycle	None	X	X	X	L	H	X	X	X	L	L-H	High-Z	1
READ Cycle (Begin Burst)	External	L	L	H	L	L	H	X	L	L	L-H	Q	
READ Cycle (Continue Burst)	Next	X	X	X	L	H	X	X	L	L	L-H	Q	1, 11
NOP/DUMMY READ (Begin Burst)	External	L	L	H	L	L	H	X	H	L	L-H	High-Z	2
DUMMY READ (Continue Burst)	Next	X	X	X	L	H	X	X	H	L	L-H	High-Z	1, 2, 11
WRITE Cycle (Begin Burst)	External	L	L	H	L	L	L	L	X	L	L-H	D	3
WRITE Cycle (Continue Burst)	Next	X	X	X	L	H	X	L	X	L	L-H	D	1, 3, 11
NOP/WRITE ABORT (Begin Burst)	None	L	L	H	L	L	L	H	X	L	L-H	High-Z	2, 3
WRITE ABORT (Continue Burst)	Next	X	X	X	L	H	X	H	X	L	L-H	High-Z	1, 2, 3, 11
IGNORE CLOCK EDGE (Stall)	Current	X	X	X	L	X	X	X	X	H	L-H	–	4
SNOOZE MODE	None	X	X	X	H	X	X	X	X	X	X	High-Z	

NOTE:
1. CONTINUE BURST cycles, whether READ or WRITE, use the same control inputs. The type of cycle performed (READ or WRITE) is chosen in the initial BEGIN BURST cycle. A CONTINUE DESELECT cycle can only be entered if a DESELECT cycle is executed first.
2. DUMMY READ and WRITE ABORT cycles can be considered NOPs because the device performs no external operation. A WRITE ABORT means a WRITE command is given, but no operation is performed.
3. OE# may be wired LOW to minimize the number of control signals to the SRAM. The device will automatically turn off the output drivers during a WRITE cycle. OE# may be used when the bus turn-on and turn-off times do not meet an application's requirements.
4. If an IGNORE CLOCK EDGE command occurs during a READ operation, the DQ bus will remain active (Low-Z). If it occurs during a WRITE cycle, the bus will remain in High-Z. No WRITE operations will be performed during the IGNORE CLOCK EDGE cycle.
5. X means "Don't Care." H means logic HIGH. L means logic LOW. BWx = H means all byte write signals (BWa#, BWb#, BWc# and BWd#) are HIGH. BWx = L means one or more byte write signals are LOW.
6. BWa# enables WRITEs to Byte "a" (DQa pins); BWb# enables WRITEs to Byte "b" (DQb pins); BWc# enables WRITEs to Byte "c" (DQc pins); BWd# enables WRITEs to Byte "d" (DQd pins).
7. All inputs except OE# and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
8. Wait states are inserted by setting CKE# HIGH.
9. This device contains circuitry that will ensure that the outputs will be in High-Z during power-up.
10. The device incorporates a 2-bit burst counter. Address wraps to the initial address every fourth BURST cycle.
11. The address counter is incremented for all CONTINUE BURST cycles.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{DD} Supply
   Relative to V_{SS} .... -0.5V to +4.6V
Voltage on $V_{DD}Q$ Supply
   Relative to V_{SS} .... -0.5V to V_{DD}
V_{IN} .... -0.5V to $V_{DD}Q$ + 0.5V
Storage Temperature (TQFP) .... -55°C to +150°C
Storage Temperature (FBGA) .... -55°C to +125°C
Junction Temperature** .... +150°C
Short Circuit Output Current 100mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Junction temperature depends upon package type, cycle time, loading, ambient temperature, and airflow. See Micron Technical Note TN-05-14 for more information.

3.3V I/O DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(0°C ≤ T_A ≤ +70°C; V_{DD}, $V_{DD}Q$ = +3.3V ±0.165V unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	V_{DD} + 0.3	V	1, 2
Input High (Logic 1) Voltage	DQ pins	V_{IH}	2.0	V_{DD} + 0.3	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{DD}	IL_I	-1.0	1.0	µA	3
Output Leakage Current	Output(s) disabled, 0V ≤ V_{IN} ≤ V_{DD}	IL_O	-1.0	1.0	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1, 4
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1, 4
Supply Voltage		V_{DD}	3.135	3.465	V	1
Isolated Output Buffer Supply		$V_{DD}Q$	3.135	V_{DD}	V	1, 5

NOTE:
1. All voltages referenced to V_{SS} (GND).
2. Overshoot: V_{IH} ≤ +4.6V for t ≤ ^{t}KHKH/2 for I ≤ 20mA
   Undershoot: V_{IL} ≥ -0.7V for t ≤ ^{t}KHKH/2 for I ≤ 20mA
   Power-up: V_{IH} ≤ +3.465V and V_{DD} ≤ +3.135V for t ≤ 200ms
3. MODE pin has an internal pull-up, and input leakage = ±10µA.
4. The load used for V_{OH}, V_{OL} testing is shown in Figure 2. AC load current is higher than the shown DC values. AC I/O curves are available upon request.
5. $V_{DD}Q$ should never exceed V_{DD}. V_{DD} and $V_{DD}Q$ can be externally wired together to the same power supply.

2.5V I/O DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(0°C ≤ T_A ≤ +70°C; V_{DD} = +3.3V ±0.165V; $V_{DD}Q$ = +2.5V +0.4V/-0.125V unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	Data bus (DQx)	$V_{IH}Q$	1.7	$V_{DD}Q$ + 0.3	V	1, 2
	Inputs	V_{IH}	1.7	V_{DD} + 0.3	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.7	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{DD}	IL_I	-1.0	1.0	µA	3
Output Leakage Current	Output(s) disabled, 0V ≤ V_{IN} ≤ $V_{DD}Q$ (DQx)	IL_O	-1.0	1.0	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	1.7	–	V	1
	I_{OH} = -1.0mA	V_{OH}	2.0	–	V	1
Output Low Voltage	I_{OL} = 2.0mA	V_{OL}	–	0.7	V	1
	I_{OL} = 1.0mA	V_{OL}	–	0.4	V	1
Supply Voltage		V_{DD}	3.135	3.465	V	1
Isolated Output Buffer Supply		$V_{DD}Q$	2.375	2.9	V	1

TQFP CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Control Input Capacitance	T_A = +25°C; f = 1 MHz V_{DD} = 3.3V	C_I	3	4	pF	1
Input/Output Capacitance (DQ)		C_O	4	5	pF	1
Address Capacitance		C_A	3	3.5	pF	1
Clock Capacitance		C_{CK}	3	3.5	pF	1

BGA CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Address/Control Input Capacitance	T_A = 25°C; f = 1 MHz V_{DD} = 3.3V	C_I	4	7	pF	1
Input/Output Capacitance (DQ)		C_O	4.5	5.5	pF	1
Address Capacitance		C_A	4	7	pF	1
Clock Capacitance		C_{CK}	4.5	5.5	pF	1

FBGA CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Address/Control Input Capacitance		C_I	2.5	3.5	pF	4
Output Capacitance (Q)	T_A = 25°C; f = 1 MHz	C_O	4	5	pF	4
Clock Capacitance		C_{CK}	2.5	3.5	pF	4

NOTE: 1. All voltages referenced to V_{SS} (GND).
2. Overshoot: V_{IH} ≤ +4.6V for t ≤ ^tKHKH/2 for I ≤ 20mA
   Undershoot: V_{IL} ≥ -0.7V for t ≤ ^tKHKH/2 for I ≤ 20mA
   Power-up: V_{IH} ≤ +3.465V and V_{DD} ≤ +3.135V for t ≤ 200ms
3. MODE pin has an internal pull-up, and input leakage = ±10µA.
4. This parameter is sampled.

I_{DD} OPERATING CONDITIONS AND MAXIMUM LIMITS

(Note 1) (0°C ≤ T_A ≤ +70°C; V_{DD} = +3.3V ±0.165V unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX -10	MAX -11	MAX -12	UNITS	NOTES
Power Supply Current: Operating	Device selected; All inputs ≤ V_{IL} or ≥ V_{IH}; Cycle time ≥ ^tKC (MIN); V_{DD} = MAX; Outputs open	I_{DD}	165	300	275	250	mA	2, 3, 4
Power Supply Current: Idle	Device selected; V_{DD} = MAX; CKE# ≥ V_{IH}; All inputs ≤ V_{SS} + 0.2 or ≥ V_{DD} - 0.2; Cycle time ≥ ^tKC (MIN)	I_{DD1}	10	28	22	20	mA	2, 3, 4
CMOS Standby	Device deselected; V_{DD} = MAX; All inputs ≤ V_{SS} + 0.2 or ≥ V_{DD} - 0.2; All inputs static; CLK frequency = 0	I_{SB2}	0.5	10	10	10	mA	3, 4
TTL Standby	Device deselected; V_{DD} = MAX; All inputs ≤ V_{IL} or ≥ V_{IH}; All inputs static; CLK frequency = 0	I_{SB3}	6	25	25	25	mA	3, 4
Clock Running	Device deselected; V_{DD} = MAX; ADV/LD# ≥ V_{IH}; All inputs ≤ V_{SS} + 0.2 or ≥ V_{DD} - 0.2; Cycle time ≥ ^tKC (MIN)	I_{SB4}	37	65	65	60	mA	3, 4
Snooze Mode	ZZ ≥ V_{IH}	I_{SB2Z}	0.5	10	10	10	mA	4

TQFP THERMAL RESISTANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	UNITS	NOTES
Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	θ_{JA}	40	°C/W	5
Thermal Resistance (Junction to Top of Case)		θ_{JC}	8	°C/W	5

BGA THERMAL RESISTANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	UNITS	NOTES
Junction to Ambient (Airflow of 1m/s)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	θ_{JA}	40	°C/W	5
Junction to Case (Top)		θ_{JC}	9	°C/W	5

NOTE:
1. $V_{DD}Q$ = +3.3V ±0.165V for 3.3V I/O configuration; $V_{DD}Q$ = +2.5V +0.4V/-0.125V for 2.5V I/O configuration.
2. I_{DD} is specified with no output current and increases with faster cycle times. $I_{DD}Q$ increases with faster cycle times and greater output loading.
3. "Device deselected" means device is in a deselected cycle as defined in the truth table. "Device selected" means device is active (not in deselected mode).
4. Typical values are measured at +3.3V, +25°C and 12ns cycle time.
5. This parameter is sampled.

FBGA THERMAL RESISTANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	UNITS	NOTES
Junction to Ambient (Airflow of 1m/s)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	θ_{JA}	40	°C/W	1, 11
Junction to Case (Top)		θ_{JC}	9	°C/W	1, 11
Junction to Pins (Bottom)		θ_{JB}	17	°C/W	1, 11

AC ELECTRICAL CHARACTERISTICS

(Notes 2, 3, 4) (0°C ≤ T_A ≤ +70°C; V_{DD} = +3.3V ±0.165V unless otherwise noted)

DESCRIPTION	SYMBOL	-10 MIN	-10 MAX	-11 MIN	-11 MAX	-12 MIN	-12 MAX	UNITS	NOTES
Clock									
Clock cycle time	^tKHKH	10		11		12		ns	
Clock frequency	^fKF		100		90		83	MHz	
Clock HIGH time	^tKHKL	2.5		3.0		3.0		ns	5
Clock LOW time	^tKLKH	2.5		3.0		3.0		ns	5
Output Times									
Clock to output valid	^tKHQV		7.5		8.5		9.0	ns	
Clock to output invalid	^tKHQX	3.0		3.0		3.0		ns	6
Clock to output in Low-Z	$^tKHQX1$	3.0		3.0		3.0		ns	6, 7, 8, 9
Clock to output in High-Z	^tKHQZ		5.0		5.0		5.0	ns	6, 7, 8, 9
OE# to output valid	^tGLQV		5.0		5.0		5.0	ns	2
OE# to output in Low-Z	^tGLQX	0		0		0		ns	6, 7, 8, 9
OE# to output in High-Z	^tGHQZ		5.0		5.0		5.0	ns	6, 7, 8, 9
Setup Times									
Address	^tAVKH	2.0		2.2		2.5		ns	10
Clock enable (CKE#)	^tEVKH	2.0		2.2		2.5		ns	10
Control signals	^tCVKH	2.0		2.2		2.5		ns	10
Data-in	^tDVKH	2.0		2.2		2.5		ns	10
Hold Times									
Address	^tKHAX	0.5		0.5		0.5		ns	10
Clock enable (CKE#)	^tKHEX	0.5		0.5		0.5		ns	10
Control signals	^tKHCX	0.5		0.5		0.5		ns	10
Data-in	^tKHDX	0.5		0.5		0.5		ns	10

NOTE:
1. This parameter is sampled.
2. OE# can be considered a "Don't Care" during WRITEs; however, controlling OE# can help fine-tune a system for turnaround timing.
3. Test conditions as specified with output loading as shown in Figure 1 for 3.3V I/O ($V_{DD}Q$ = +3.3V ±0.165V) and Figure 3 for 2.5V I/O ($V_{DD}Q$ = +2.5V +0.4V/-0.125V).
4. A WRITE cycle is defined by R/W# LOW having been registered into the device at ADV/LD# LOW. A READ cycle is defined by R/W# HIGH with ADV/LD# LOW. Both cases must meet setup and hold times.
5. Measured as HIGH above V_{IH} and LOW below V_{IL}.
6. Refer to Technical Note TN-55-01, "Designing with ZBT SRAMs," for a more thorough discussion on these parameters.
7. This parameter is sampled.
8. This parameter is measured with output loading as shown in Figure 2 for 3.3V I/O and Figure 4 for 2.5V I/O.
9. Transition is measured ±200mV from steady state voltage.
10. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when they are being registered into the device. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when the chip is enabled. Chip enable must be valid at each rising edge of CLK when ADV/LD# is LOW to remain enabled.
11. Preliminary package data.

3.3V I/O AC TEST CONDITIONS

Input pulse levels .... Vss to 3.3V
Input rise and fall times 1ns
Input timing reference levels 1.5V
Output reference levels 1.5V
Output load .... See Figures 1 and 2

2.5V I/O AC TEST CONDITIONS

Input pulse levels .... Vss to 2.5V
Input rise and fall times 1ns
Input timing reference levels 1.25V
Output reference levels 1.25V
Output load .... See Figures 3 and 4

3.3V I/O Output Load Equivalents
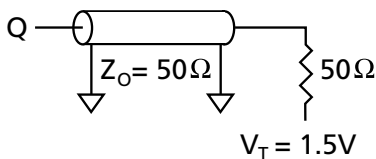
Figure 1

2.5V I/O Output Load Equivalents
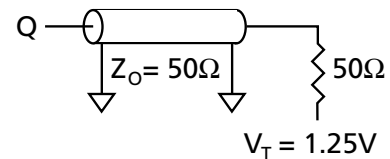
Figure 3
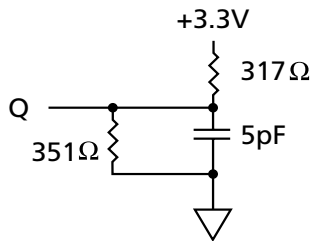
Figure 2
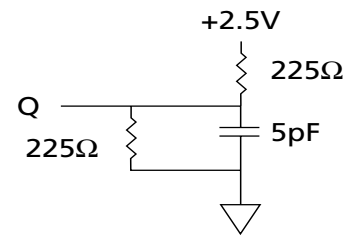
Figure 4

LOAD DERATING CURVES

The Micron 512K x 18, 256K x 32, and 256K x 36 ZBT SRAM timing is dependent upon the capacitive loading on the outputs.

Consult the factory for copies of I/O current versus voltage curves.

SNOOZE MODE

SNOOZE MODE is a low-current, "power-down" mode in which the device is deselected and current is reduced to I_{SB2Z}. The duration of SNOOZE MODE is dictated by the length of time the ZZ pin is in a HIGH state. After the device enters SNOOZE MODE, all inputs except ZZ become disabled and all outputs go to High-Z.

The ZZ pin is an asynchronous, active HIGH input that causes the device to enter SNOOZE MODE. When the ZZ pin becomes a logic HIGH, I_{SB2Z} is guaranteed after the time ^tZZI is met. Any READ or WRITE operation pending when the device enters SNOOZE MODE is not guaranteed to complete successfully. Therefore, SNOOZE MODE must not be initiated until valid pending operations are completed. Similarly, when exiting SNOOZE MODE during ^tRZZ, only a DESELECT or READ cycle should be given.

SNOOZE MODE ELECTRICAL CHARACTERISTICS

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Current during SNOOZE MODE	ZZ ≥ V_{IH}	I_{SB2Z}		10	mA	
ZZ active to input ignored		^tZZ	0	^tKHKH	ns	1
ZZ inactive to input sampled		^tRZZ	0	^tKHKH	ns	1
ZZ active to snooze current		^tZZI		^tKHKH	ns	1
ZZ inactive to exit snooze current		^tRZZI	0		ns	1

NOTE: 1. This parameter is sampled.

SNOOZE MODE WAVEFORM

READ/WRITE TIMING

DON'T CARE   UNDEFINED
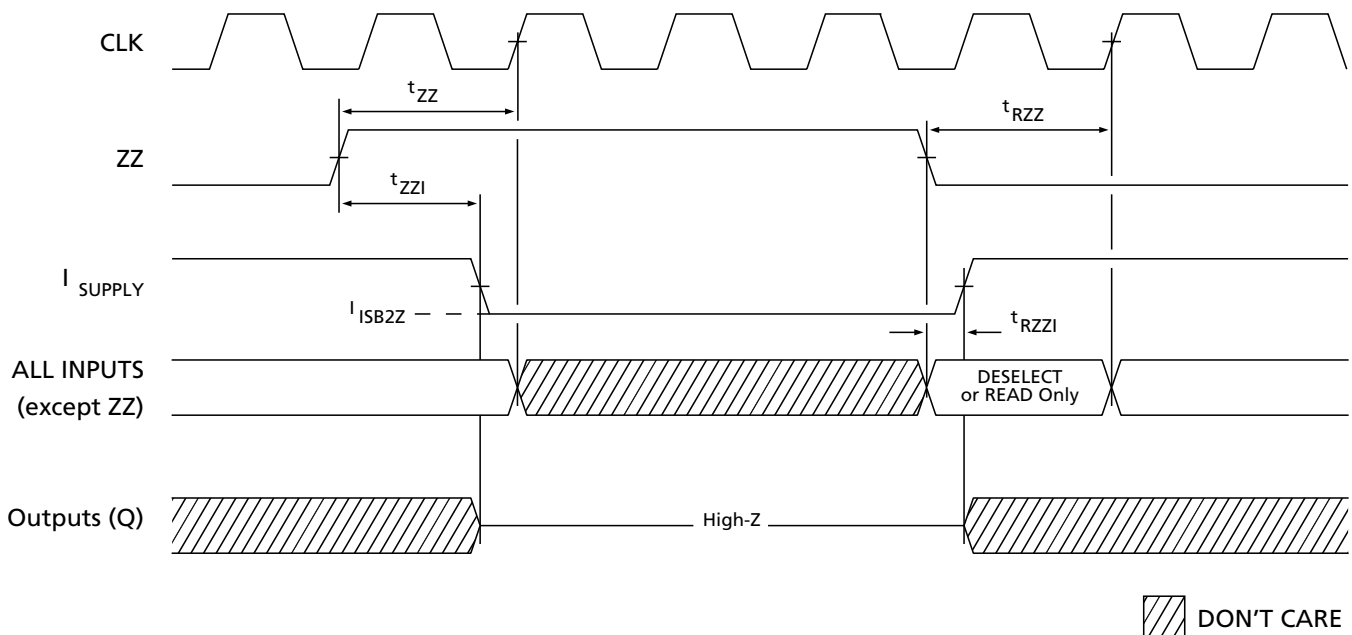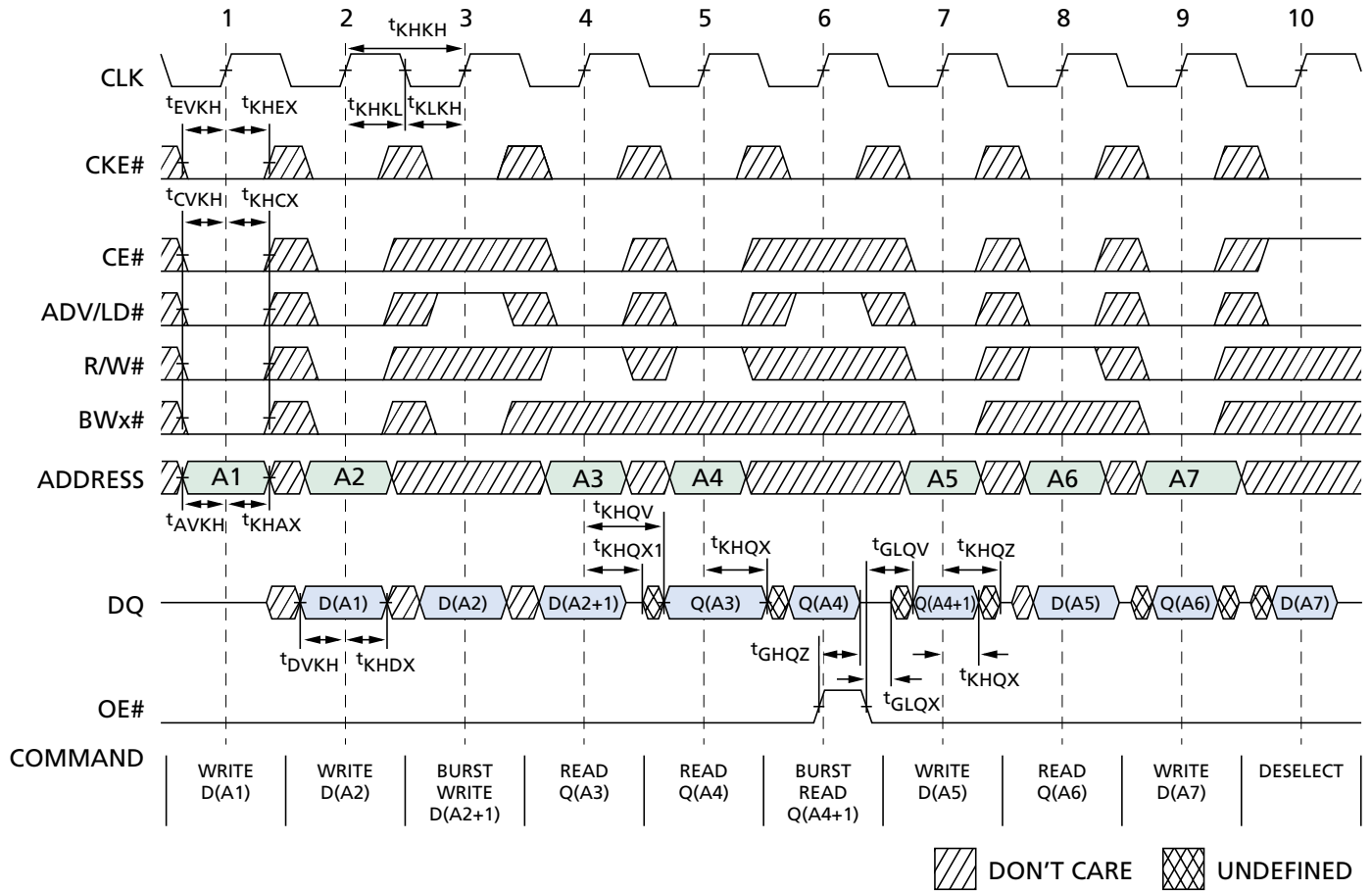
READ/WRITE TIMING PARAMETERS

SYM	-10 MIN	-10 MAX	-11 MIN	-11 MAX	-12 MIN	-12 MAX	UNITS
t_{KHKH}	10		11		12		ns
f_{KF}		100		90		83	MHz
t_{KHKL}	2.5		3.0		3.0		ns
t_{KLKH}	2.5		3.0		3.0		ns
t_{KHQV}		7.5		8.5		9.0	ns
t_{KHQX}	3.0		3.0		3.0		ns
t_{KHQX1}	3.0		3.0		3.0		ns
t_{KHQZ}		5.0		5.0		5.0	ns
t_{GLQV}		5.0		5.0		5.0	ns
t_{GLQX}	0		0		0		ns

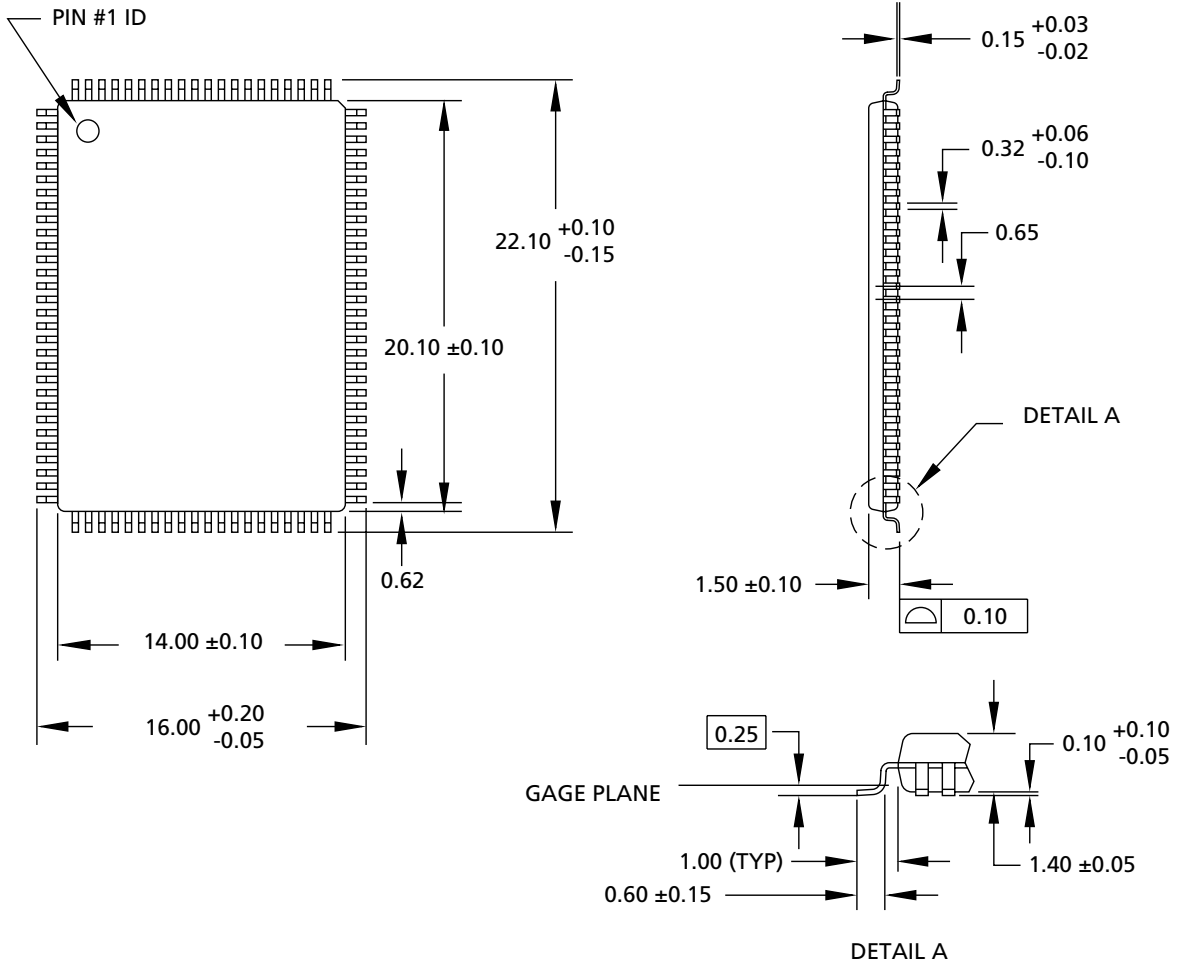| SYM	-10 MIN	-10 MAX	-11 MIN	-11 MAX	-12 MIN	-12 MAX	UNITS
t_{GHQZ}		5.0		5.0		5.0	ns
t_{AVKH}	2.0		2.2		2.5		ns
t_{EVKH}	2.0		2.2		2.5		ns
t_{CVKH}	2.0		2.2		2.5		ns
t_{DVKH}	2.0		2.2		2.5		ns
t_{KHAX}	0.5		0.5		0.5		ns
t_{KHEX}	0.5		0.5		0.5		ns
t_{KHCX}	0.5		0.5		0.5		ns
t_{KHDX}	0.5		0.5		0.5		ns

NOTE:
1. For this waveform, ZZ is tied LOW.
2. Burst sequence order is determined by MODE (0 = linear, 1 = interleaved). BURST operations are optional.
3. CE# represents three signals. When CE# = 0, it represents CE# = 0, CE2# = 0, CE2 = 1.
4. Data coherency is provided for all possible operations. If a READ is initiated, the most current data is used. The most recent data may be from the input data register.

NOP, STALL, AND DESELECT CYCLES
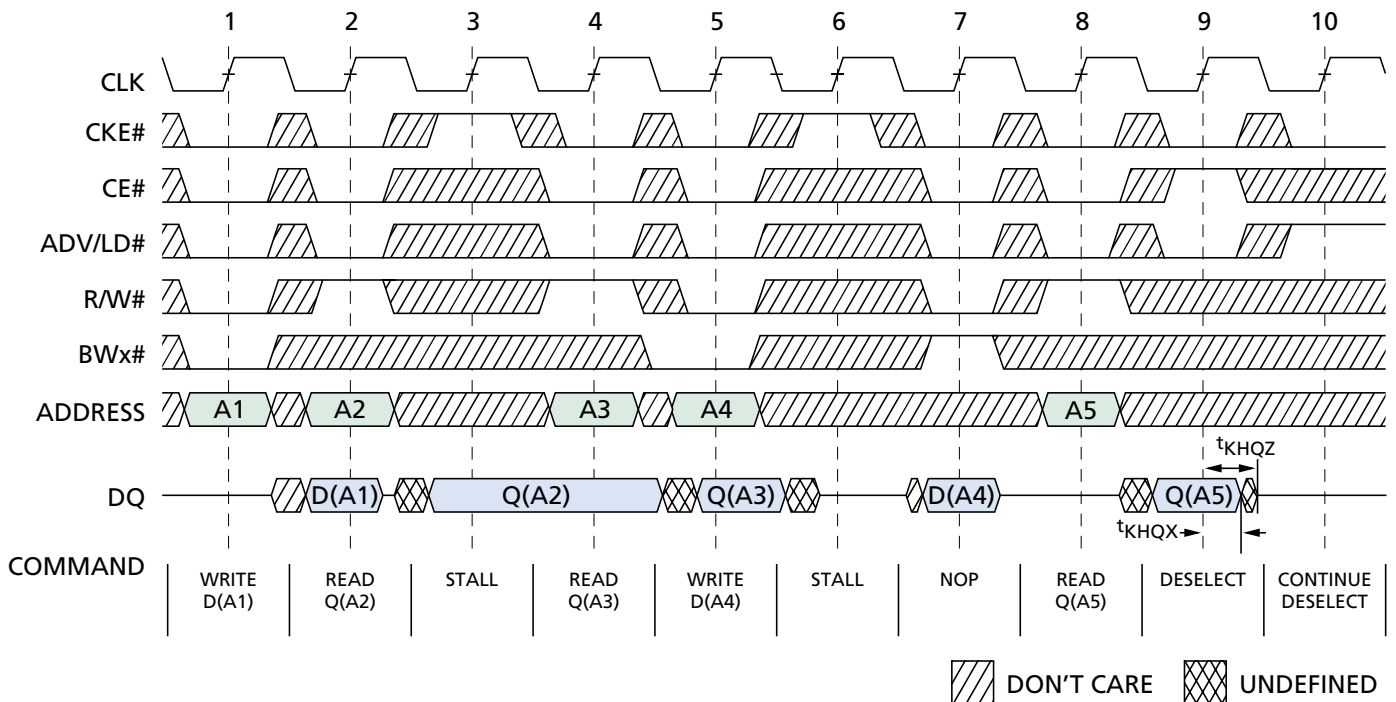
NOP, STALL, AND DESELECT TIMING PARAMETERS

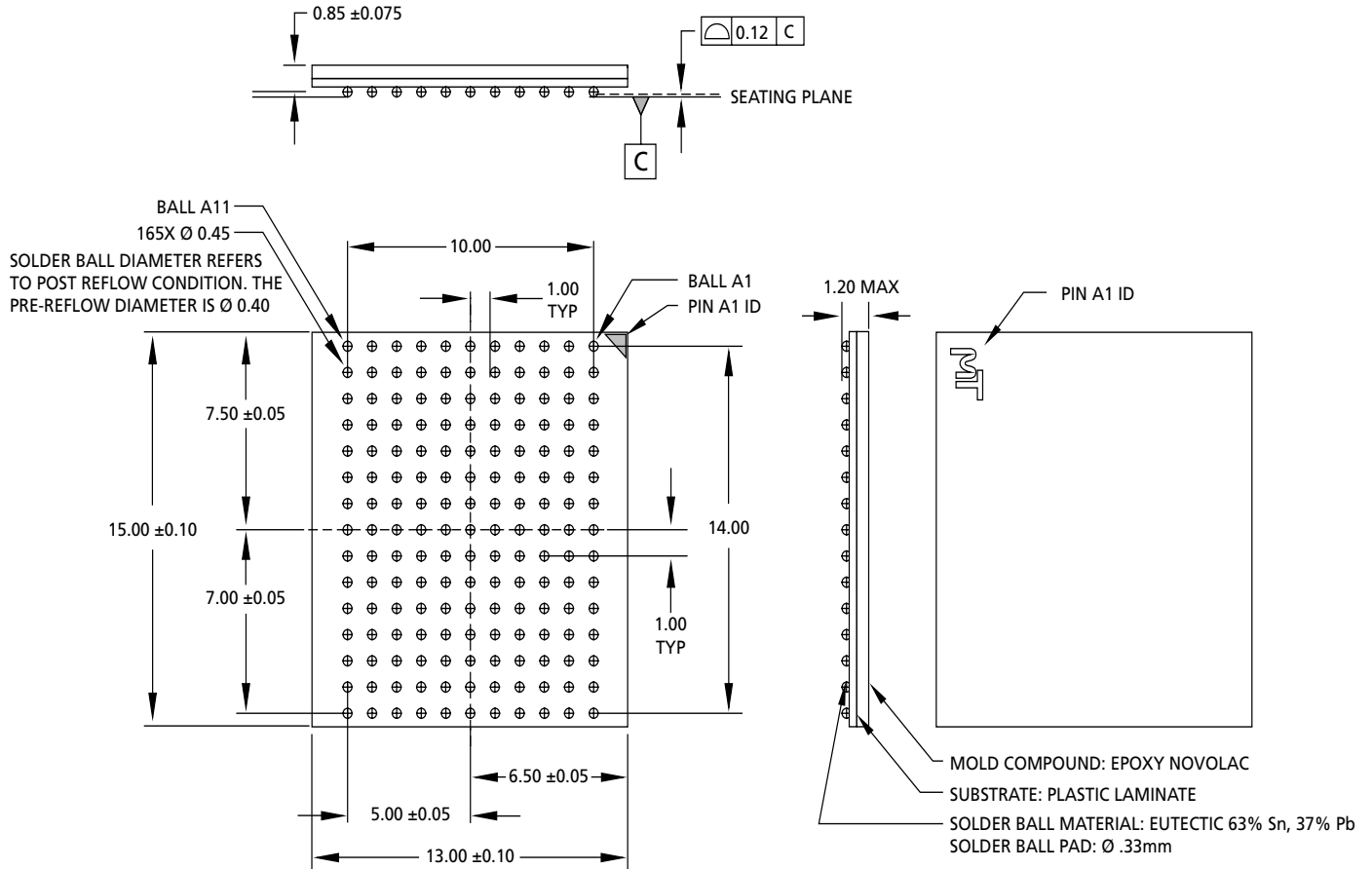| SYM	-10		-11		-12		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
t_{KHQX}	3.0		3.0		3.0		ns
t_{KHQZ}		5.0		5.0		5.0	ns

NOTE:
1. The IGNORE CLOCK EDGE or STALL cycle (clock 3) illustrates CKE# being used to create a "pause." A WRITE is not performed during this cycle.
2. For this waveform, ZZ and OE# are tied LOW.
3. CE# represents three signals. When CE# = 0, it represents CE# = 0, CE2# = 0, CE2 = 1.
4. Data coherency is provided for all possible operations. If a READ is initiated, the most current data is used. The most recent data may be from the input data register.

100-PIN PLASTIC TQFP (JEDEC LQFP)

PIN #1 ID

22.10 $^{+0.10}_{-0.15}$

20.10 ±0.10

0.62

14.00 ±0.10

16.00 $^{+0.20}_{-0.05}$

0.15 $^{+0.03}_{-0.02}$

0.32 $^{+0.06}_{-0.10}$

0.65

DETAIL A

1.50 ±0.10

0.10

0.25

GAGE PLANE

0.10 $^{+0.10}_{-0.05}$
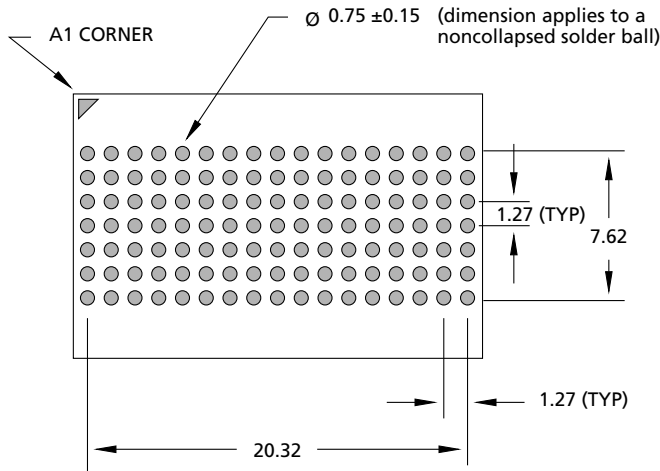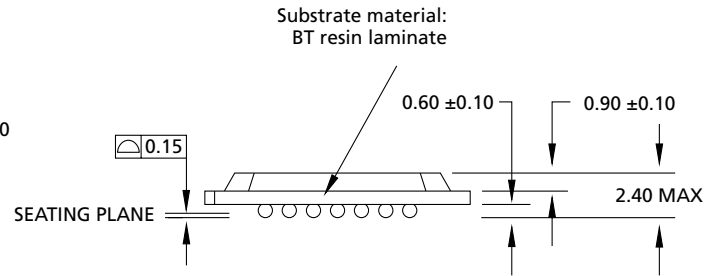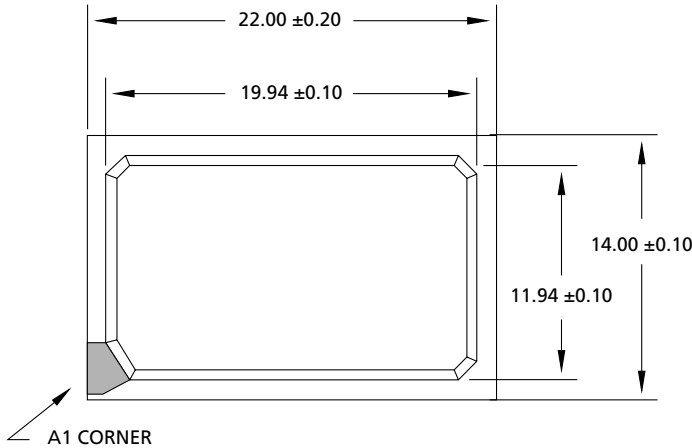
1.00 (TYP)

0.60 ±0.15

1.40 ±0.05

DETAIL A

NOTE: 1. All dimensions in millimeters.

2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.25mm per side.

165-PIN FBGA

NOTE: 1. All dimensions in millimeters $\frac{MAX}{MIN}$ or typical where noted.

119-PIN BGA

22.00 ±0.20

19.94 ±0.10

14.00 ±0.10

11.94 ±0.10

A1 CORNER

Substrate material:
BT resin laminate

0.60 ±0.10

0.90 ±0.10

0.15

2.40 MAX

SEATING PLANE

A1 CORNER

∅ 0.75 ±0.15 (dimension applies to a noncollapsed solder ball)

1.27 (TYP)

7.62

1.27 (TYP)

20.32

NOTE: 1. All dimensions in millimeters $\frac{MAX}{MIN}$ or typical where noted.

2. Solder ball pad is 0.6mm.

REVISION HISTORY

Removed note "Not Recommended for New Designs," Rev. 6/01 .... June 7/01

Added industrial temperature references and notes, Rev. 3/01 .... March 19/01
Changed 16Mb references to 18Mb
Changed NC/DQPx to NF/DQPx

Added 119-pin PBGA package, Rev. 1/01, FINAL .... January 10/01

Removed FBGA Part Marking Guide, Rev. 8/00, FINAL .... August 1/00

Added FBGA Part Marking Guide, Rev 7/00 .... 7/21/00
Added Revision History
Removed 119-Pin PBGA packages and references

Added 165-pin FBGA Package 6/13/00