

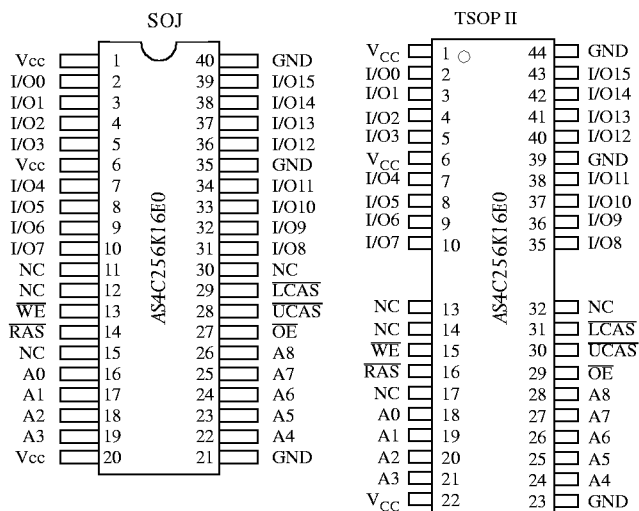
High speed 256K×16 CMOS DRAM (EDO)

Preliminary information

Features

- Organization: 262,144 words × 16 bits
- High speed
  - 30/35/50/60 ns  $\overline{\text{RAS}}$  access time
  - 16/18/25/30 ns column address access time
  - 10/12 ns  $\overline{\text{CAS}}$  access time
- Low power consumption
  - Active: 770 mW max (4C256K16E0-50)
  - Standby: 5.5 mW max, CMOS I/O
- EDO page mode
- 512 refresh cycles, 8 ms refresh interval
  - $\overline{\text{RAS}}$ -only or  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh
- Read-modify-write
- TTL-compatible, three-state I/O
- JEDEC standard packages
  - 400 mil, 40-pin SOJ
  - 400 mil, 40/44-pin TSOP II
- 5V power supply
- Latch-up current > 200 mA

Pin arrangement



Pin designation

Pin(s)	Description
A0 to A8	Address inputs
$\overline{\text{RAS}}$	Row address strobe
I/O0 to I/O15	Input/output
$\overline{\text{OE}}$	Output enable
$\overline{\text{UCAS}}$	Column address strobe, upper byte
$\overline{\text{LCAS}}$	Column address strobe, lower byte
$\overline{\text{WE}}$	Read/write control
$V_{\text{CC}}$	Power (5V ± 0.5V)
GND	Ground

Selection guide

	Symbol	4C256K16E0-30	4C256K16E0-35	4C256K16E0-50	4C256K16E0-60	Unit
Maximum $\overline{\text{RAS}}$ access time	$t_{\text{RAC}}$	30	35	50	60	ns
Maximum column address access time	$t_{\text{CAA}}$	16	18	25	30	ns
Maximum $\overline{\text{CAS}}$ access time	$t_{\text{CAC}}$	10	10	10	12	ns
Maximum output enable ( $\overline{\text{OE}}$ ) access time	$t_{\text{OEA}}$	10	10	10	10	ns
Minimum read or write cycle time	$t_{\text{RC}}$	65	70	85	100	ns
Minimum EDO page mode cycle time	$t_{\text{PC}}$	12	14	25	30	ns
Maximum operating current	$I_{\text{CC1}}$	200	190	140	130	mA
Maximum CMOS standby current	$I_{\text{CC5}}$	1.0	1.0	1.0	1.0	mA



### Functional description

The AS4C256K16E0 is a high performance 4 megabit CMOS Dynamic Random Access Memory (DRAM) organized as 262,144 words by 16 bits. The AS4C256K16E0 is fabricated with advanced CMOS technology and designed with innovative design techniques resulting in high speed, extremely low power and wide operating margins at component and system levels.

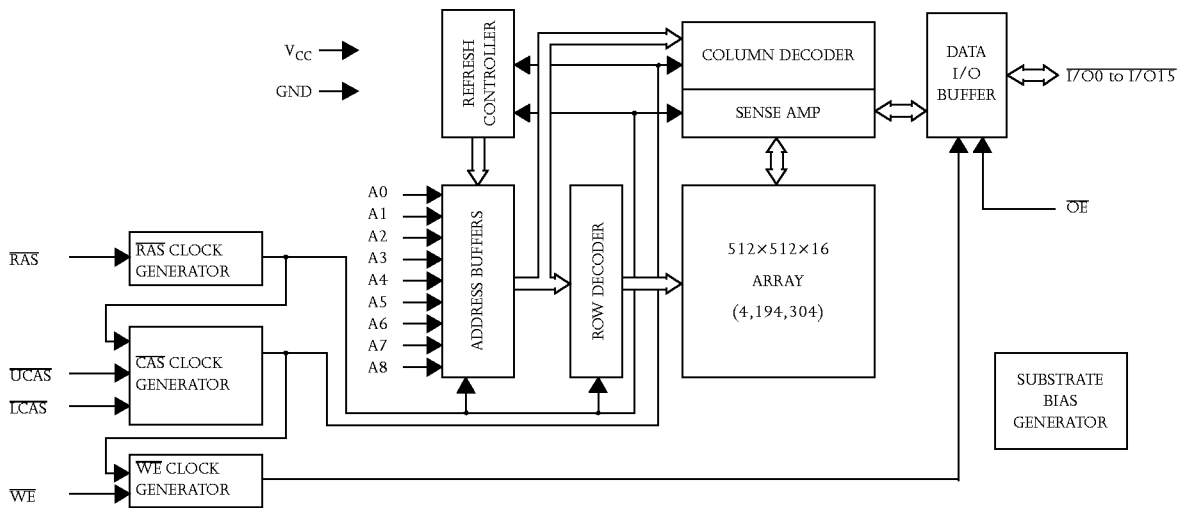
The AS4C256K16E0 features a high speed page mode operation in which high speed read, write and read-write are performed on any of the 512 × 16 bits defined by the column address. The asynchronous column address uses an extremely short row address capture time to ease the system level timing constraints associated with multiplexed addressing. Output is tri-stated by a column address strobe (CAS) which acts as an output enable independent of RAS. Very fast CAS to output access time eases system design.

Refresh on the 512 address combinations of A0 to A8 during an 8 ms period is accomplished by performing any of the following:

- RAS-only refresh cycles
- Hidden refresh cycles
- CAS-before-RAS refresh cycles
- Normal read or write cycles

The AS4C256K16E0 is available in standard 40-pin plastic SOJ and 40/44-pin TSOP II packages compatible with widely available automated testing and insertion equipment. System level features include single power supply of 5V ± 0.5V tolerance and direct interface with TTL logic families.

### Logic block diagram



### Recommended operating conditions

(Ta = 0°C to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
	GND	0.0	0.0	0.0	V
Input voltage	V <sub>IH</sub>	2.4	—	V <sub>CC</sub> + 1	V
	V <sub>IL</sub>	-1.0	—	0.8	V



### Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Input voltage	$V_{in}$	-1.0	+7.0	V
Output voltage	$V_{out}$	-1.0	+7.0	V
Power supply voltage	$V_{CC}$	-1.0	+7.0	V
Operating temperature	$T_{OPR}$	0	+70	°C
Storage temperature (plastic)	$T_{STG}$	-55	+150	°C
Soldering temperature × time	$T_{SOLDER}$	–	260 × 10	°C × sec
Power dissipation	$P_D$	–	1	W
Short circuit output current	$I_{out}$	–	50	mA
Latch-up current		200	–	mA

NOTE: Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### DC electrical characteristics

Parameter	Symbol	Test conditions	-30		-35		-50		-60		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
Input leakage current	$I_{IL}$	$0V \leq V_{in} \leq +5.5V$ pins not under test = 0V	-10.0	10.0	-10.0	10.0	-10.0	10.0	-10.0	10.0	$\mu A$	
Output leakage current	$I_{OL}$	$D_{OUT}$ disabled, $0V \leq V_{out} \leq +5.5V$	-10.0	10.0	-10.0	10.0	-10.0	10.0	-10.0	10.0	$\mu A$	
Operating power supply current	$I_{CC1}$	RAS, UCAS, ICAS, address cycling; $t_{RC} = \text{min}$	–	200	–	190	–	140	–	130	mA	1,2
TTL standby power supply current	$I_{CC2}$	$\overline{RAS} = \overline{UCAS} = \overline{ICAS} = V_{IH}$	–	2.0	–	2.0	–	2.0	–	2.0	mA	
Average power supply current, $\overline{RAS}$ refresh mode	$I_{CC3}$	$\overline{RAS}$ cycling, $\overline{UCAS} = \overline{ICAS} = V_{IH}$ , $t_{RC} = \text{min}$	–	200	–	190	–	140	–	130	mA	1
EDO page mode average power supply current	$I_{CC4}$	$\overline{RAS} = \overline{UCAS} = \overline{ICAS} = V_{IL}$ , address cycling; $t_{SC} = \text{min}$	–	190	–	180	–	70	–	65	mA	1,2
CMOS standby power supply current	$I_{CC5}$	$\overline{RAS} = \overline{UCAS} = \overline{ICAS} = V_{CC} - 0.2V$	–	1.0	–	1.0	–	1.0	–	1.0	mA	
CAS-before-RAS refresh power supply current	$I_{CC6}$	RAS, UCAS, ICAS, cycling; $t_{RC} = \text{min}$	–	200	–	190	–	140	–	130	mA	1
Output Voltage	$V_{OH}$	$I_{OUT} = -5.0 \text{ mA}$	2.4	–	2.4	–	2.4	–	2.4	–	V	
	$V_{OL}$	$I_{OUT} = 4.2 \text{ mA}$	–	0.4	–	0.4	–	0.4	–	0.4	V	



## AC parameters common to all waveforms

Std Symbol	Parameter	-30		-35		-50		-60		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
$t_{RC}$	Random read or write cycle time	65	–	70	–	85	–	100	–	ns	
$t_{RP}$	$\overline{RAS}$ precharge time	25	–	25	–	25	–	30	–	ns	
$t_{RAS}$	$\overline{RAS}$ pulse width	30	75K	35	75K	50	75K	60	75K	ns	
$t_{CAS}$	$\overline{CAS}$ pulse width	5	–	6	–	10	–	12	–	ns	
$t_{RCD}$	$\overline{RAS}$ to $\overline{CAS}$ delay time	15	20	16	24	15	35	15	45	ns	6
$t_{RAD}$	$\overline{RAS}$ to column address delay time	10	14	11	17	15	25	15	30	ns	7
$t_{RSH(R)}$	$\overline{CAS}$ to $\overline{RAS}$ hold time (read cycle)	10	–	10	–	10	–	12	–	ns	
$t_{CSH}$	$\overline{RAS}$ to $\overline{CAS}$ hold time	30	–	35	–	50	–	60	–	ns	
$t_{CRP}$	$\overline{CAS}$ to $\overline{RAS}$ precharge time	5	–	5	–	5	–	5	–	ns	
$t_{ASR}$	Row address setup time	0	–	0	–	0	–	0	–	ns	
$t_{RAH}$	Row address hold time	5	–	6	–	9	–	9	–	ns	
$t_T$	Transition time (rise and fall)	1.5	50	1.5	50	3	50	3	50	ns	4,5
$t_{REF}$	Refresh period	–	8	–	8	–	8	–	8	ms	3
$t_{CLZ}$	$\overline{CAS}$ to output in low Z	0	–	0	–	3	–	3	–	ns	8

## Read cycle

Std Symbol	Parameter	-30		-35		-50		-60		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
$t_{RAC}$	Access time from $\overline{RAS}$	–	30	–	35	–	50	–	60	ns	6
$t_{CAC}$	Access time from $\overline{CAS}$	–	10	–	10	–	10	–	12	ns	6,13
$t_{AA}$	Access time from address	–	16	–	18	–	25	–	30	ns	7,13
$t_{AR(R)}$	Column add hold from $\overline{RAS}$	26	–	28	–	30	–	40	–	ns	
$t_{RCS}$	Read command setup time	0	–	0	–	0	–	0	–	ns	
$t_{RCH}$	Read command hold time to $\overline{CAS}$	0	–	0	–	0	–	0	–	ns	9
$t_{RRH}$	Read command hold time to $\overline{RAS}$	0	–	0	–	0	–	0	–	ns	9
$t_{RAL}$	Column address to $\overline{RAS}$ Lead time	16	–	18	–	25	–	30	–	ns	
$t_{CPN}$	$\overline{CAS}$ precharge time	3	–	4	–	5	–	5	–	ns	
$t_{OFF}$	Output buffer turn-off time	0	8	0	8	0	8	0	10	ns	8,10



## Write cycle

Std Symbol	Parameter	-30		-35		-50		-60		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
$t_{ASC}$	Column address setup time	0	–	0	–	0	–	0	–	ns	
$t_{CAH}$	Column address hold time	5	–	5	–	9	–	10	–	ns	
$t_{AWR}$	Column address hold time to $\overline{RAS}$	26	–	28	–	30	–	40	–	ns	
$t_{WCS}$	Write command setup time	0	–	0	–	0	–	0	–	ns	11
$t_{WCH}$	Write command hold time	0	–	0	–	0	–	0	–	ns	11
$t_{WCR}$	Write command hold time to $\overline{RAS}$	26	–	28	–	30	–	40	–	ns	
$t_{WCP}$	Write command pulse width	5	–	5	–	9	–	10	–	ns	
$t_{RWL}$	Write command to $\overline{RAS}$ lead time	10	–	11	–	12	–	12	–	ns	
$t_{CWL}$	Write command to $\overline{CAS}$ lead time	10	–	11	–	12	–	12	–	ns	
$t_{DS}$	Data-in setup time	0	–	0	–	0	–	0	–	ns	12
$t_{DH}$	Data-in hold time	5	–	5	–	9	–	10	–	ns	12
$t_{DHR}$	Data-in hold time to $\overline{RAS}$	26	–	28	–	30	–	45	–	ns	

## Read-modify-write cycle

Std Symbol	Parameter	-30		-35		-50		-60		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
$t_{RWC}$	$\overline{\text{Read-write cycle time}}$	100	–	105	–	120	–	130	–	ns	
$t_{RWD}$	$\overline{RAS}$ to $\overline{WE}$ delay time	50	–	54	–	60	–	70	–	ns	11
$t_{CWD}$	$\overline{CAS}$ to $\overline{WE}$ delay time	26	–	28	–	30	–	35	–	ns	11
$t_{AWD}$	Column address to $\overline{WE}$ delay time	32	–	35	–	40	–	50	–	ns	11
$t_{RSH(W)}$	$\overline{CAS}$ to $\overline{RAS}$ hold time (write)	10	–	10	–	12	–	15	–	ns	
$t_{CAS(W)}$	$\overline{CAS}$ pulse width (write)	15	–	15	–	15	–	15	–	ns	



## EDO page mode cycle

Std Symbol	Parameter	-30		-35		-50		-60		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
t <sub>PC</sub>	Read or write cycle time (fast page)	12	–	14	–	25	–	30	–	ns	14
t <sub>CAP</sub>	Access time from $\overline{\text{CAS}}$ precharge	–	19	–	21	–	23	–	28	ns	13
t <sub>CP</sub>	$\overline{\text{CAS}}$ precharge time (fast page)	3	–	4	–	5	–	5	–	ns	
t <sub>PCM</sub>	EDO page mode RMW cycle	56	–	58	–	60	–	60	–	ns	
t <sub>CRW</sub>	Page mode $\overline{\text{CAS}}$ pulse width (RMW)	44	–	46	–	50	–	50	–	ns	
t <sub>RASP</sub>	$\overline{\text{RAS}}$ pulse width	30	75K	35	75K	50	75K	60	75K	ns	

## Refresh cycle

Std Symbol	Parameter	-30		-35		-50		-60		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
t <sub>CSR</sub>	$\overline{\text{CAS}}$ setup time ( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ )	10	–	10	–	10	–	10	–	ns	3
t <sub>CHR</sub>	$\overline{\text{CAS}}$ hold time ( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ )	7	–	8	–	10	–	15	–	ns	3
t <sub>RPC</sub>	$\overline{\text{RAS}}$ precharge to $\overline{\text{CAS}}$ hold time	0	–	0	–	0	–	0	–	ns	
t <sub>CPT</sub>	$\overline{\text{CAS}}$ precharge time ( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ counter test)	8	–	8	–	8	–	8	–	ns	

## Output enable

Std Symbol	Parameter	-30		-35		-50		-60		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
t <sub>ROH</sub>	$\overline{\text{RAS}}$ hold time referenced to $\overline{\text{OE}}$	5	–	5	–	5	–	5	–	ns	
t <sub>OE A</sub>	$\overline{\text{OE}}$ access time	–	10	–	10	–	10	–	10	ns	
t <sub>OED</sub>	$\overline{\text{OE}}$ to data delay	5	–	5	–	8	–	10	–	ns	
t <sub>OEZ</sub>	Output buffer turnoff delay from $\overline{\text{OE}}$	–	8	–	8	–	8	–	10	ns	8
t <sub>OE H</sub>	$\overline{\text{OE}}$ command hold time	8	–	8	–	8	–	10	–	ns	

## Self refresh cycle

Std Symbol	Parameter	-30		-35		-50		-60		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
t <sub>ASSH</sub>	$\overline{\text{RAS}}$ pulse width (CBR self refresh)	100K	–	100K	–	100K	–	100K	–	ns	
t <sub>RPS</sub>	$\overline{\text{RAS}}$ precharge time (CBR self refresh)	85	–	85	–	85	–	100	–	ns	
t <sub>OED</sub>	$\overline{\text{CAS}}$ hold time (CBR self refresh)	30	–	30	–	30	–	30	–	ns	



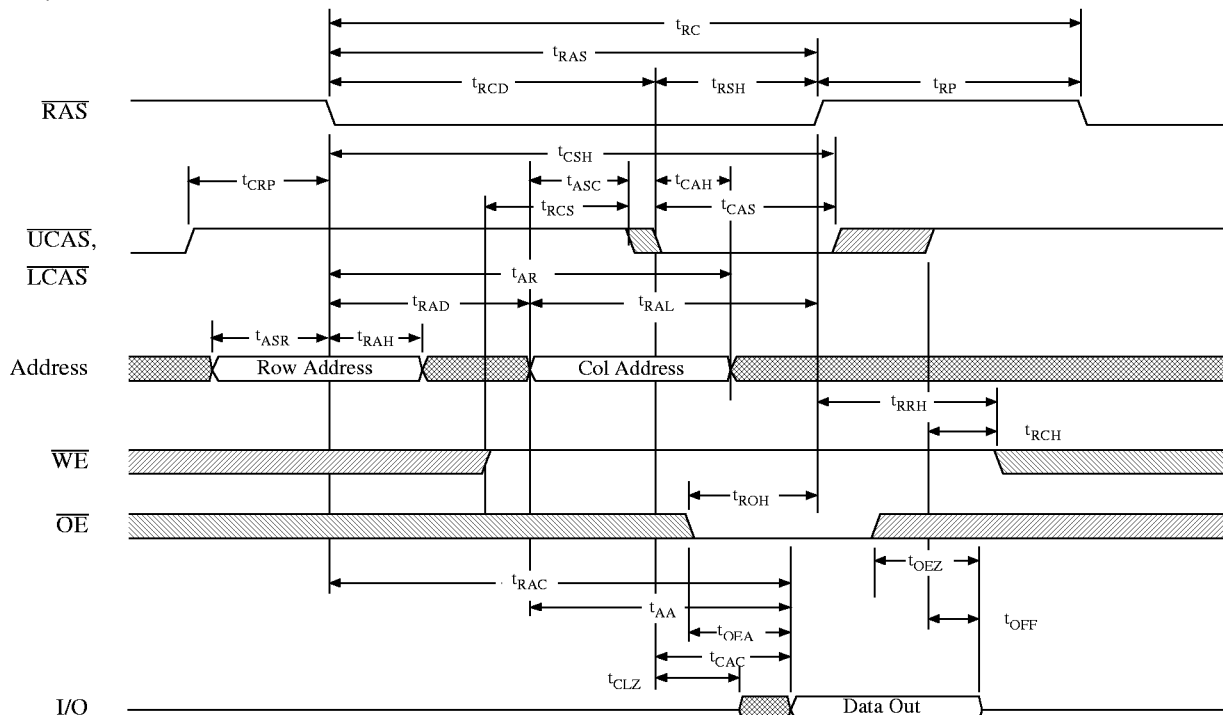
Notes

- 1  $I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$ , and  $I_{CC6}$  depend on cycle rate.
- 2  $I_{CC1}$  and  $I_{CC4}$  depend on output loading. Specified values are obtained with the output open.
- 3 An initial pause of 200  $\mu$ s is required after power-up followed by any 8  $\overline{RAS}$  cycles before proper device operation is achieved. In the case of an internal refresh counter, a minimum of 8  $\overline{CAS}$ -before- $\overline{RAS}$  initialization cycles instead of 8  $\overline{RAS}$  cycles are required. 8 initialization cycles are required after extended periods of bias without clocks (greater than 8 ms).
- 4 AC Characteristics assume  $t_T = 5$  ns. All AC parameters are measured with a load equivalent to two TTL loads and 100 pF,  $V_{IL}(\text{min}) \geq \text{GND}$  and  $V_{IH}(\text{max}) \leq V_{CC}$ .
- 5  $V_{IH}(\text{min})$  and  $V_{IL}(\text{max})$  are reference levels for measuring timing of input signals. Transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
- 6 Operation within the  $t_{RCD}(\text{max})$  limit insures that  $t_{RAC}(\text{max})$  can be met.  $t_{RCD}(\text{max})$  is specified as a reference point only. If  $t_{RCD}$  is greater than the specified  $t_{RCD}(\text{max})$  limit, then access time is controlled exclusively by  $t_{CAC}$ .
- 7 Operation within the  $t_{RAD}(\text{max})$  limit insures that  $t_{RAC}(\text{max})$  can be met.  $t_{RAD}(\text{max})$  is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD}(\text{max})$  limit, then access time is controlled exclusively by  $t_{AA}$ .
- 8 Assumes three state test load (5 pF and a 380  $\Omega$  Thevenin equivalent).
- 9 Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
- 10  $t_{OFF}(\text{max})$  defines the time at which the output achieves the open circuit condition; it is not referenced to output voltage levels.
- 11  $t_{WCS}$ ,  $t_{WCH}$ ,  $t_{RWD}$ ,  $t_{CWD}$  and  $t_{AWD}$  are not restrictive operating parameters. They are included in the datasheet as electrical characteristics only. If  $t_{WS} \geq t_{WS}(\text{min})$  and  $t_{WH} \geq t_{WH}(\text{min})$ , the cycle is an early write cycle and data out pins will remain open circuit, high impedance, throughout the cycle. If  $t_{RWD} \geq t_{RWD}(\text{min})$ ,  $t_{CWD} \geq t_{CWD}(\text{min})$  and  $t_{AWD} \geq t_{AWD}(\text{min})$ , the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is satisfied, the condition of the data out at access time is indeterminate.
- 12 These parameters are referenced to  $\overline{CAS}$  leading edge in early write cycles and to  $\overline{WE}$  leading edge in read-write cycles.
- 13 Access time is determined by the longest of  $t_{CAA}$  or  $t_{CAC}$  or  $t_{CAP}$
- 14  $t_{ASC} \geq t_{CP}$  to achieve  $t_{PC}(\text{min})$  and  $t_{CAP}(\text{max})$  values.
- 15 These parameters are sampled and not 100% tested.

Key to switching waveform

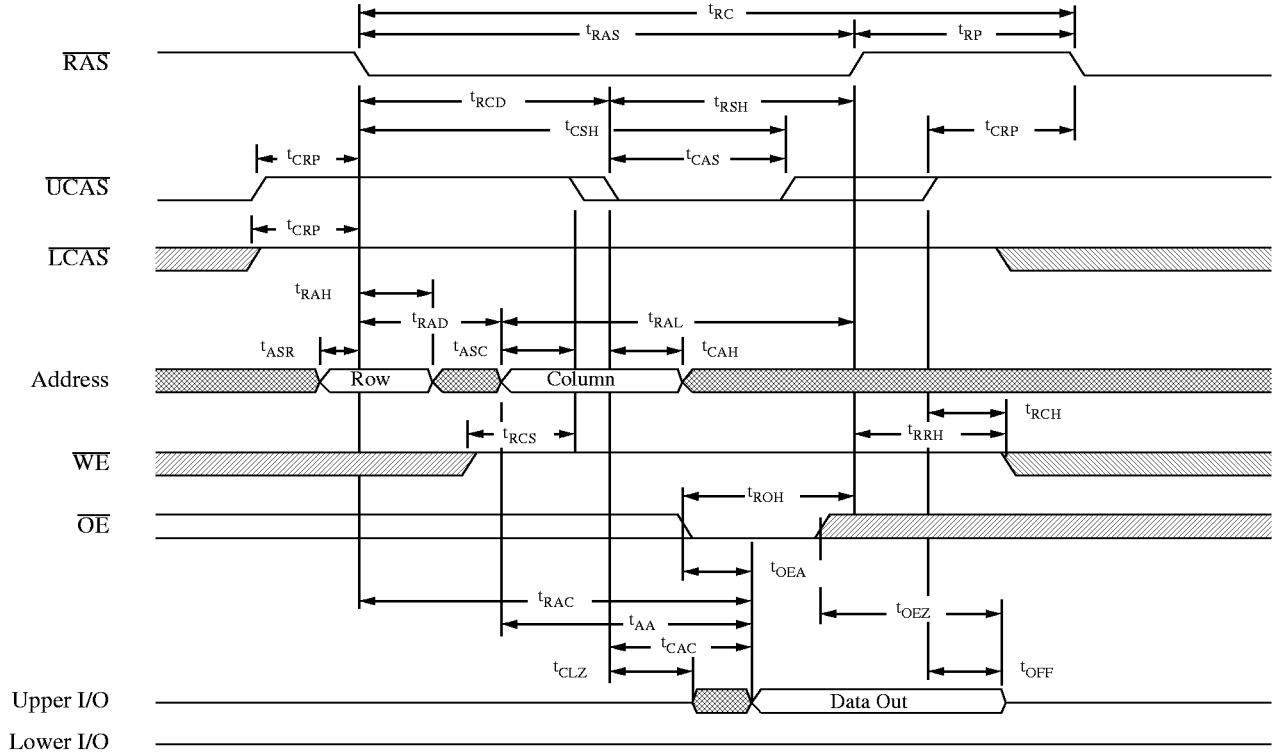


Read cycle waveform

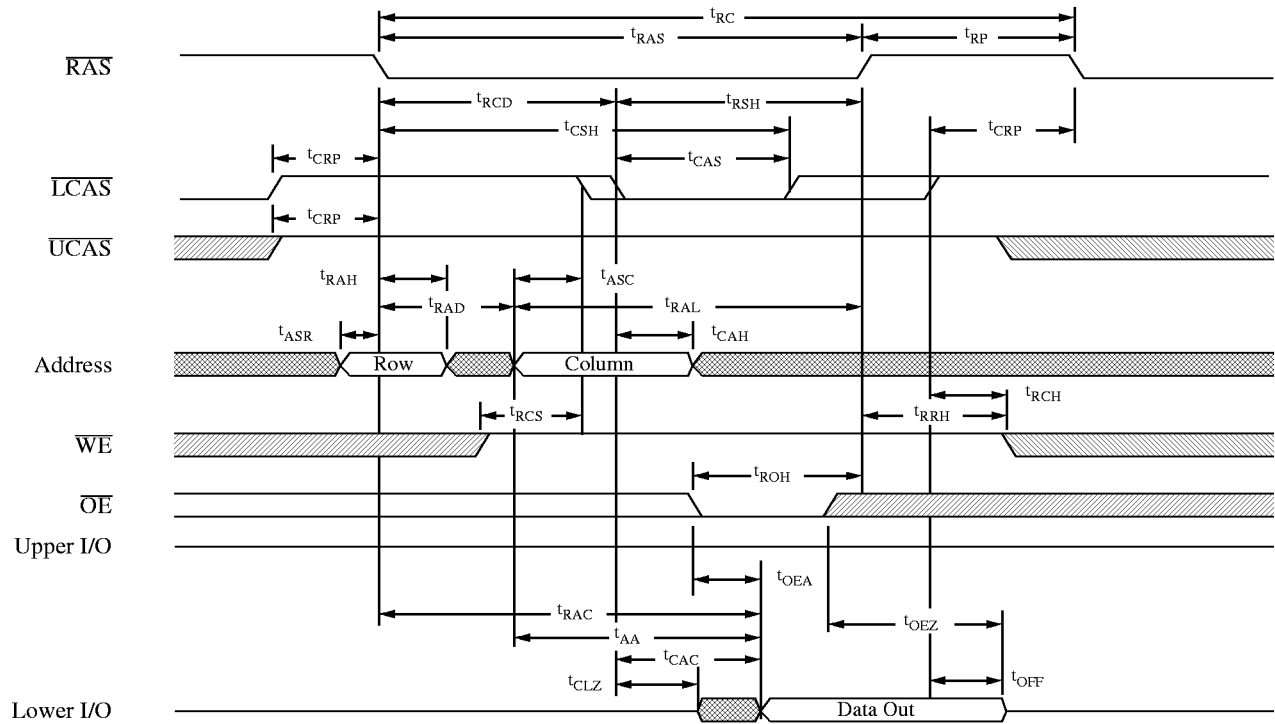




Upper byte read cycle waveform



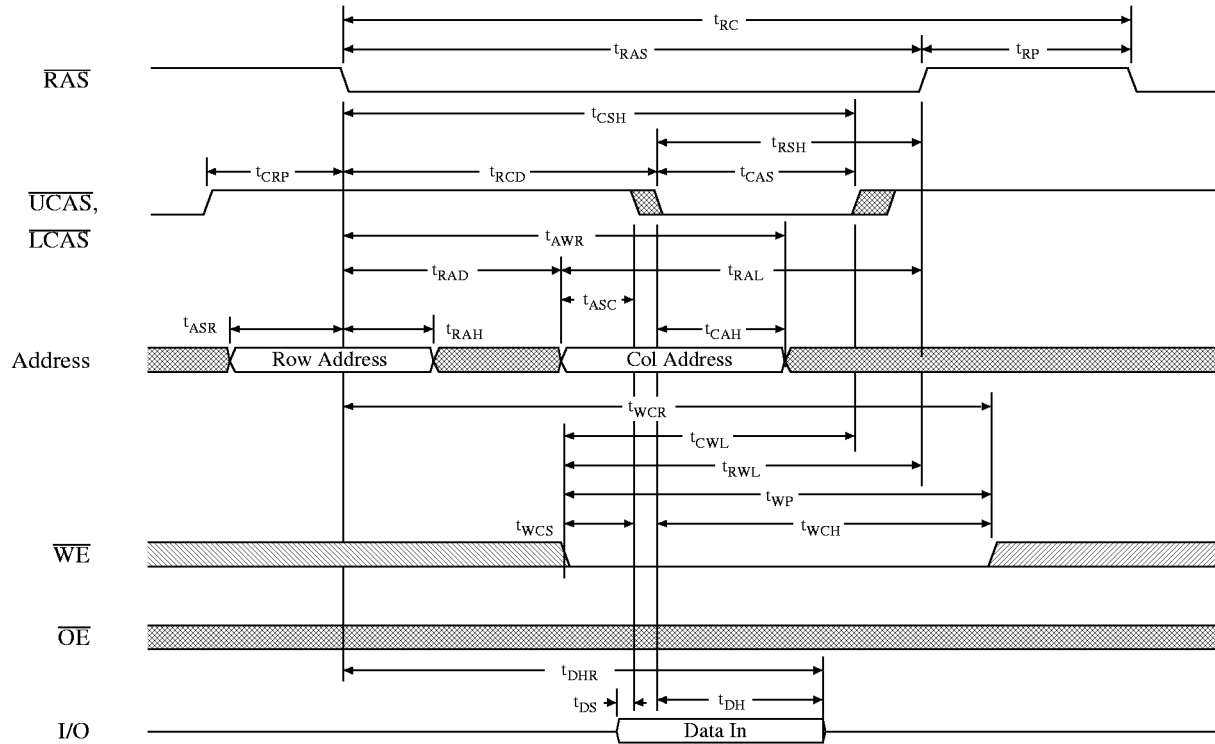
Lower byte read cycle waveform



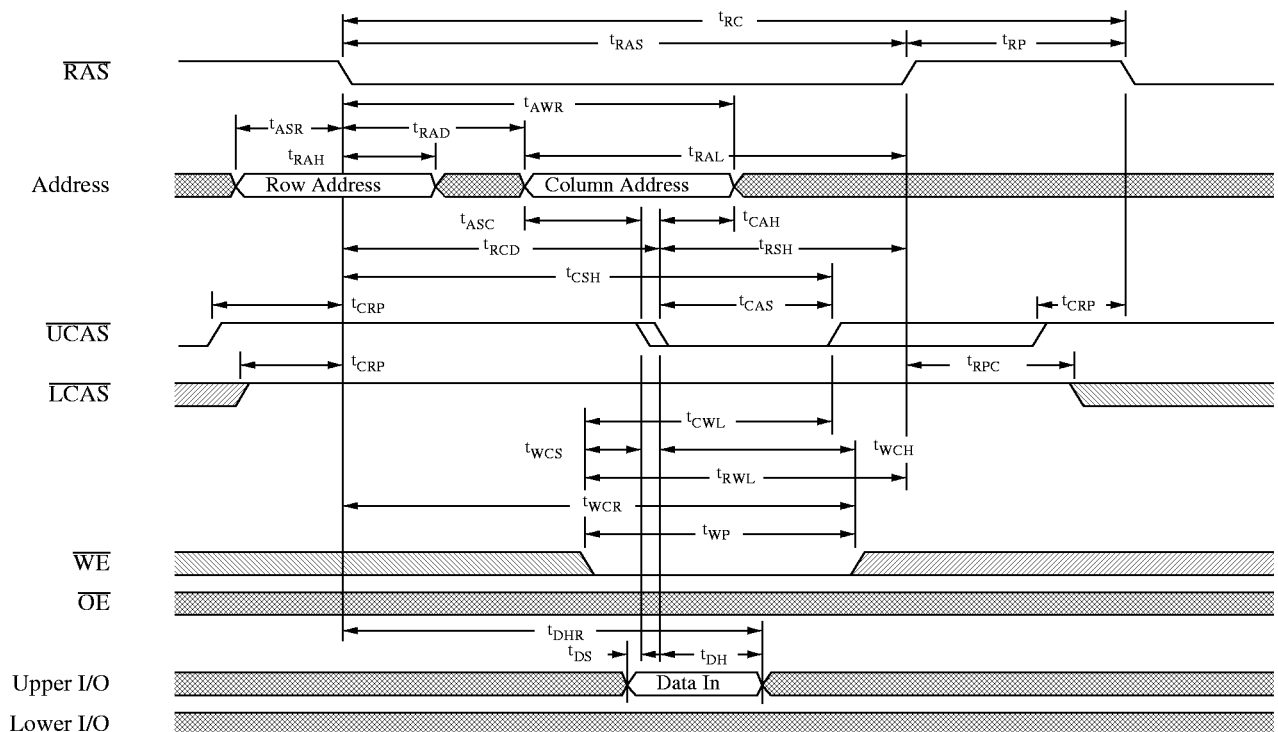




Early write cycle waveform

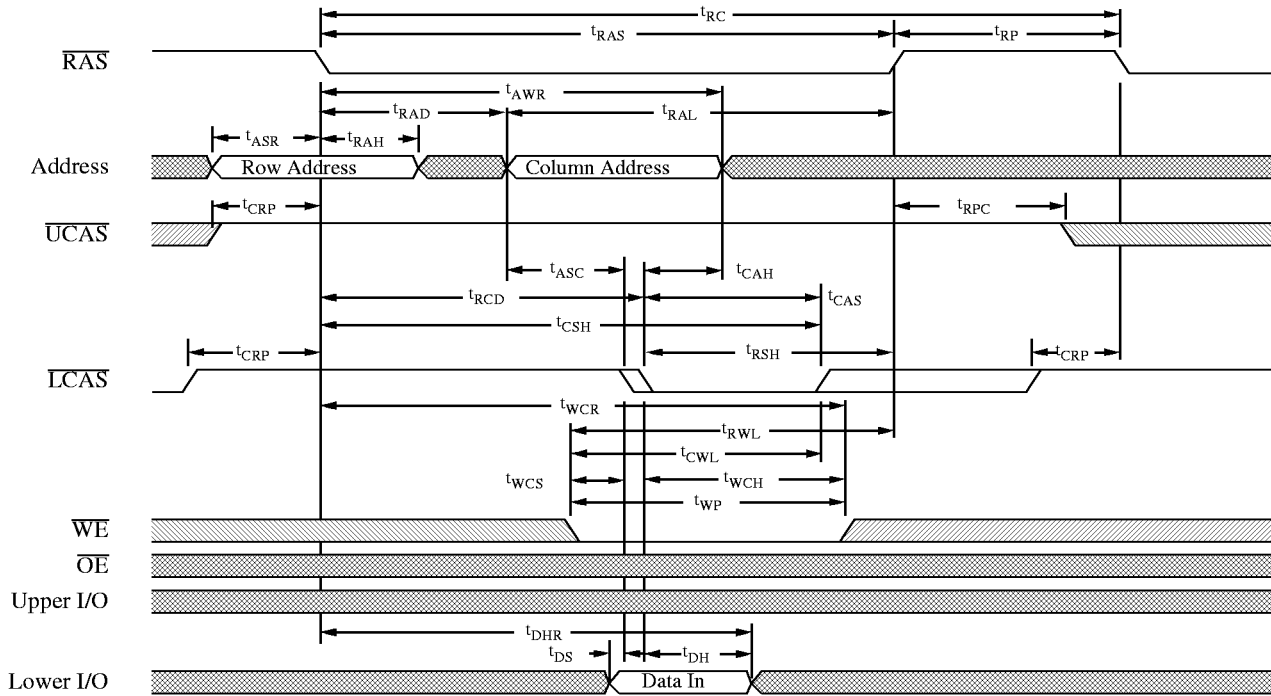


Upper byte early write cycle waveform



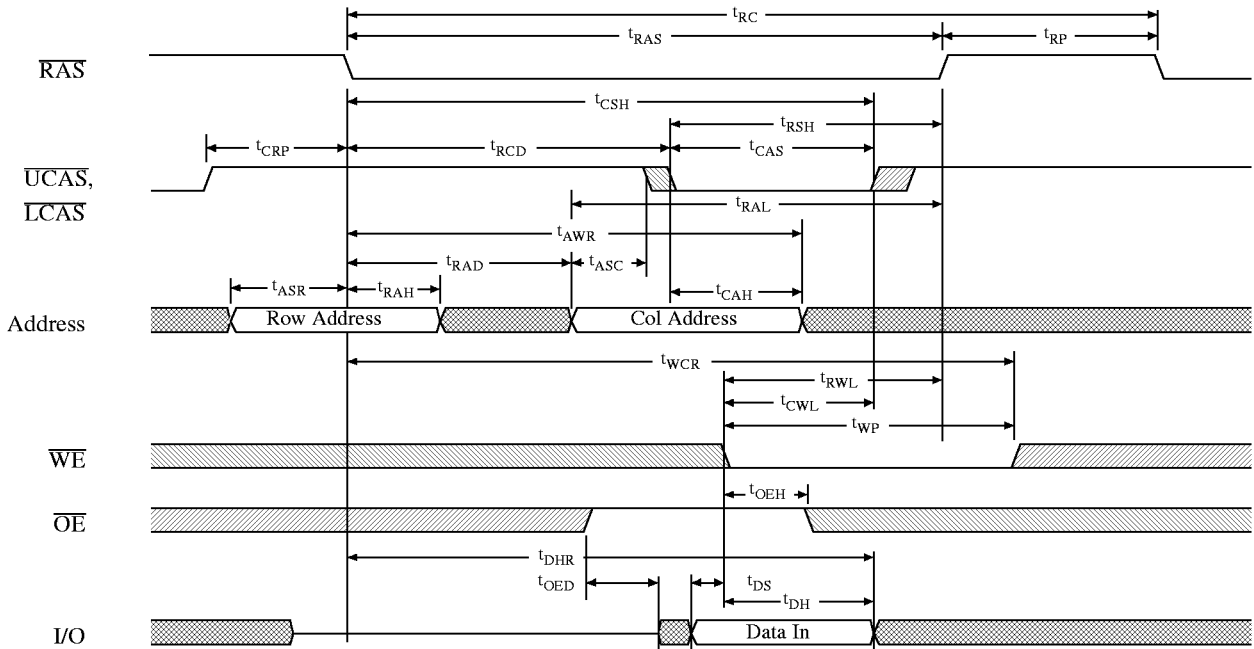


Lower byte early write cycle waveform



Write cycle waveform

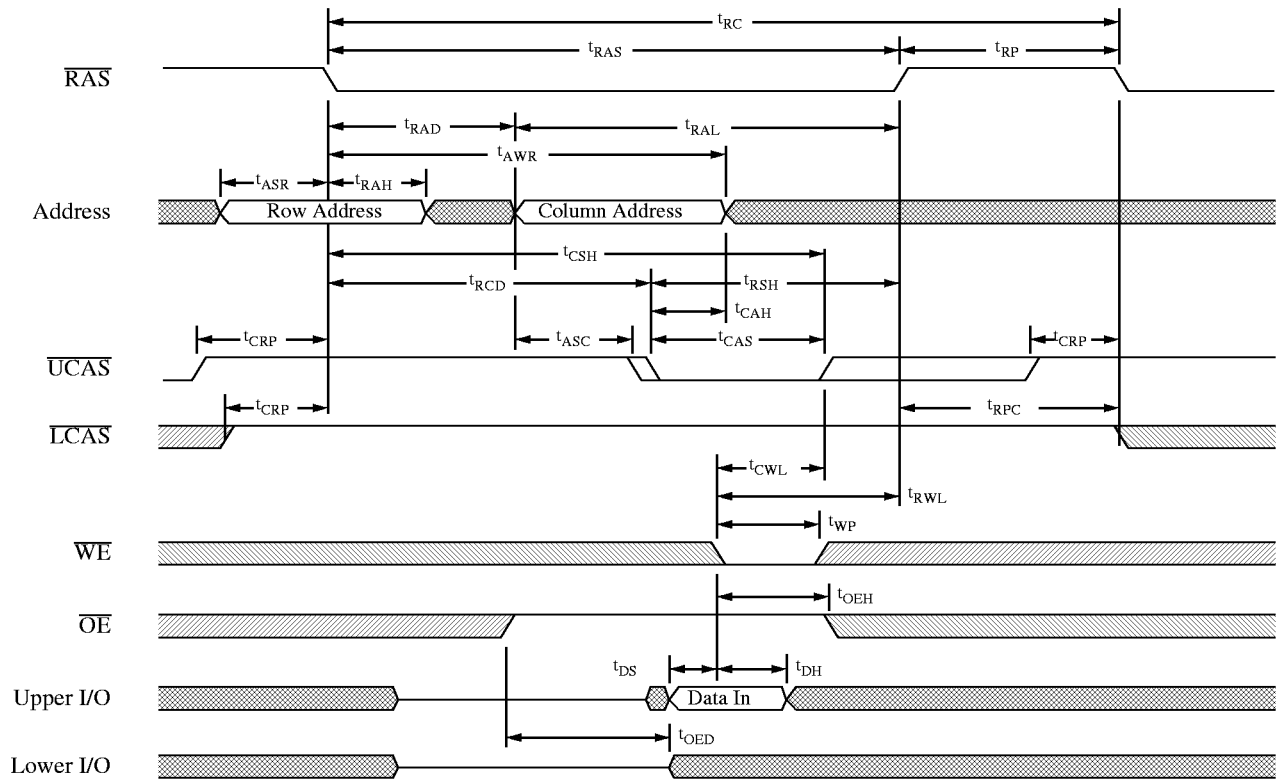
(OE controlled)





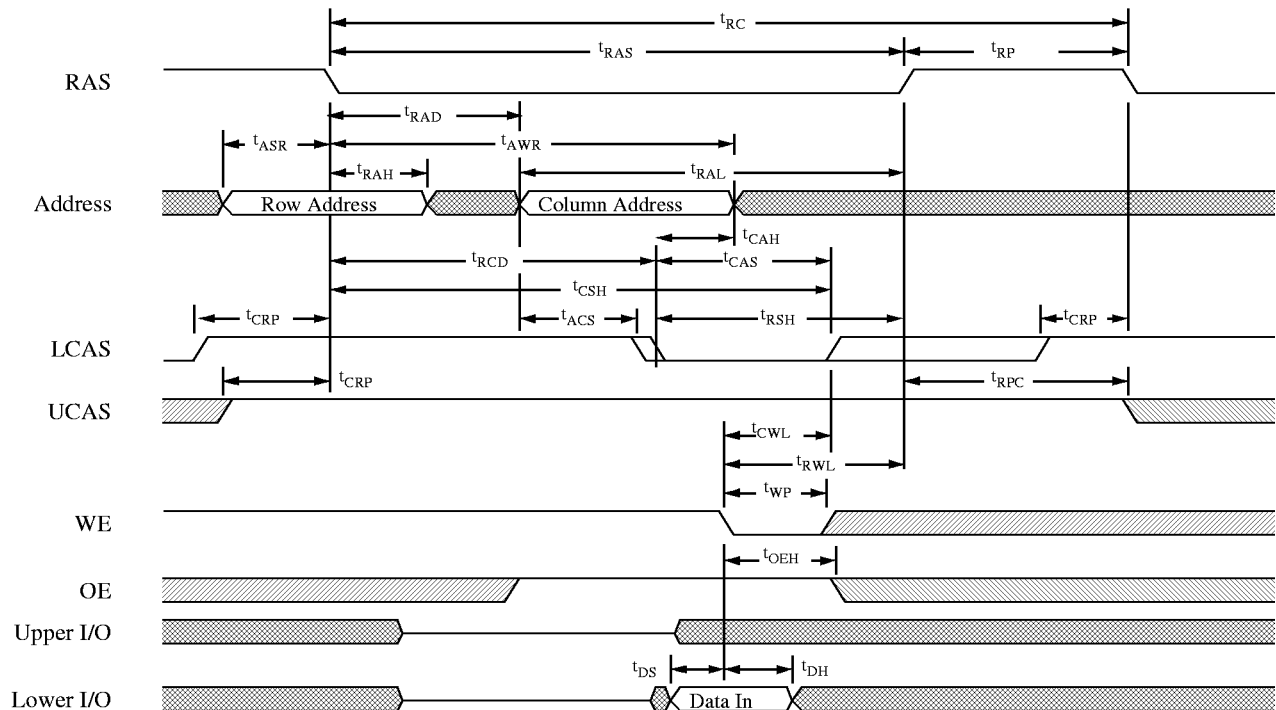
Upper byte write cycle waveform

(OE controlled)



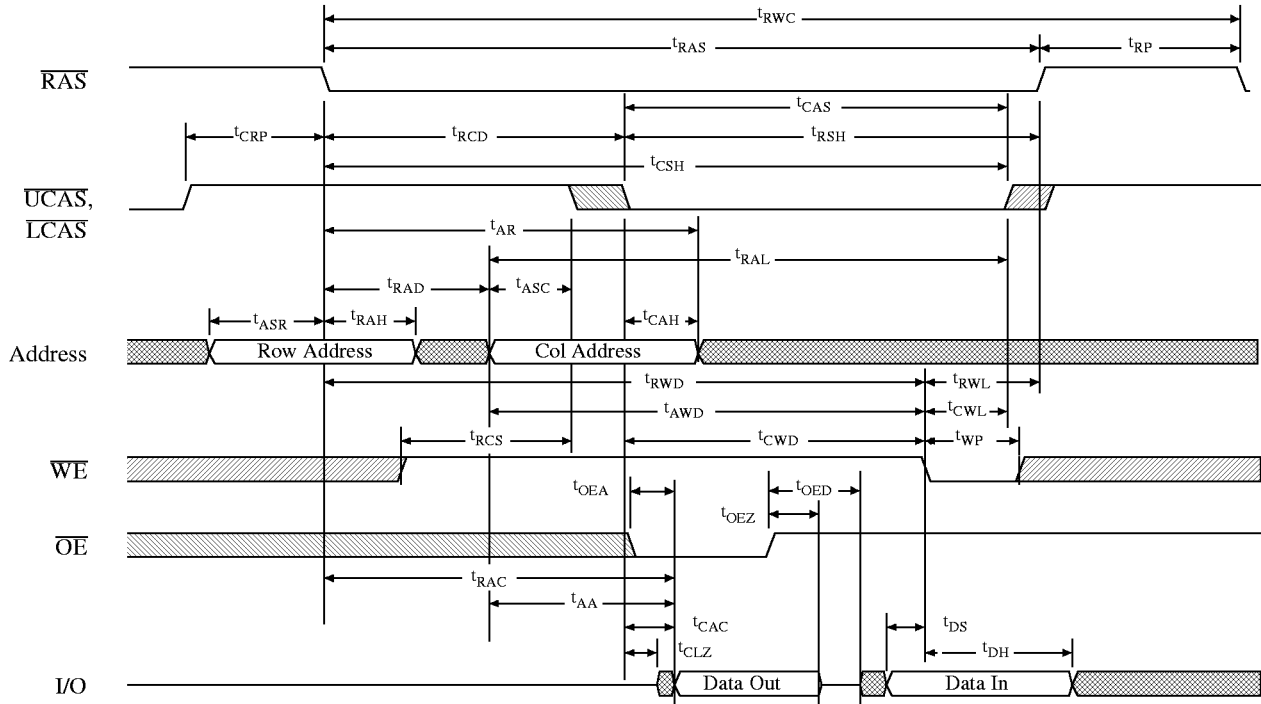
Lower byte write cycle waveform

(OE controlled)



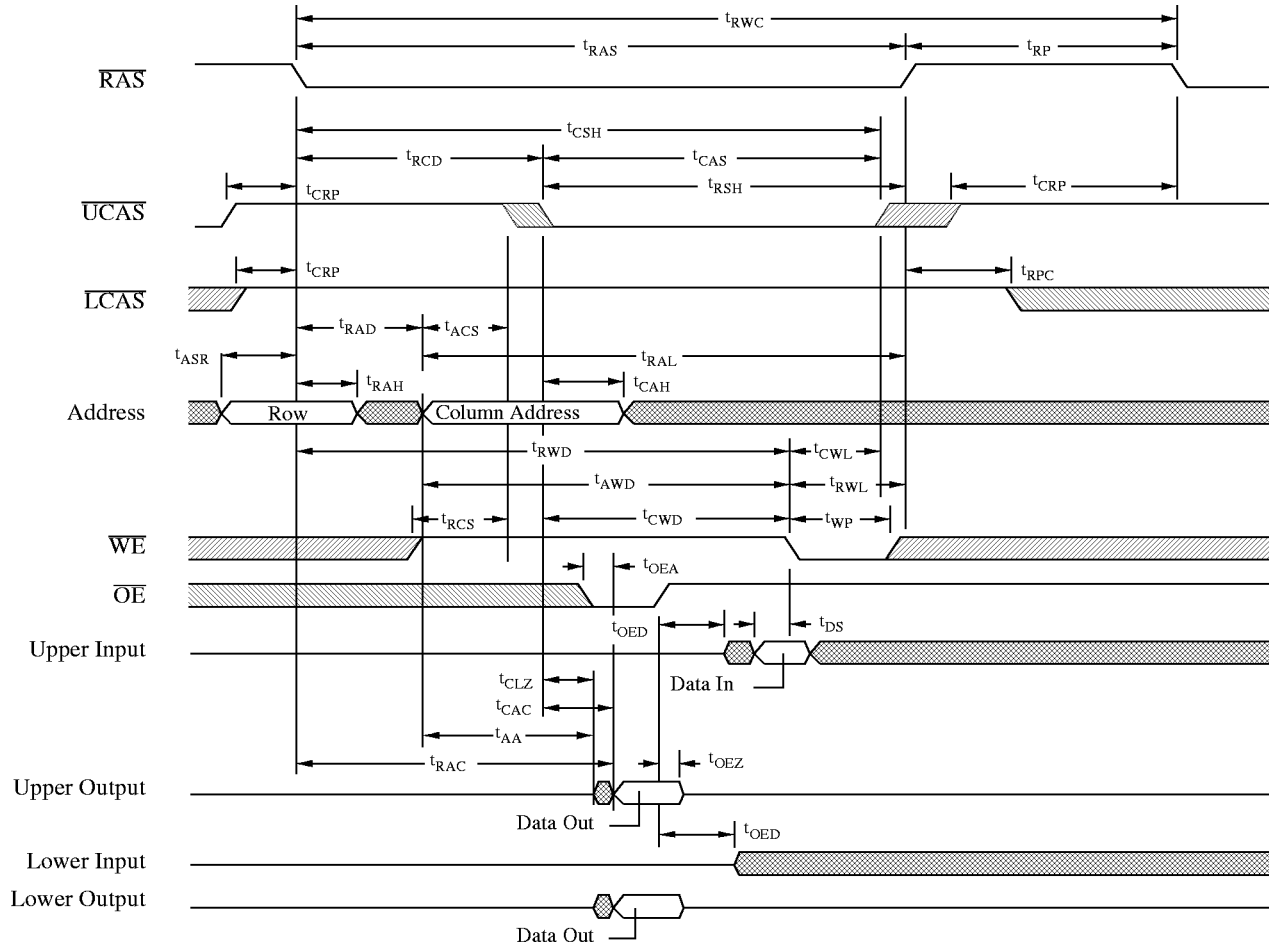


Read-modify-write cycle waveform



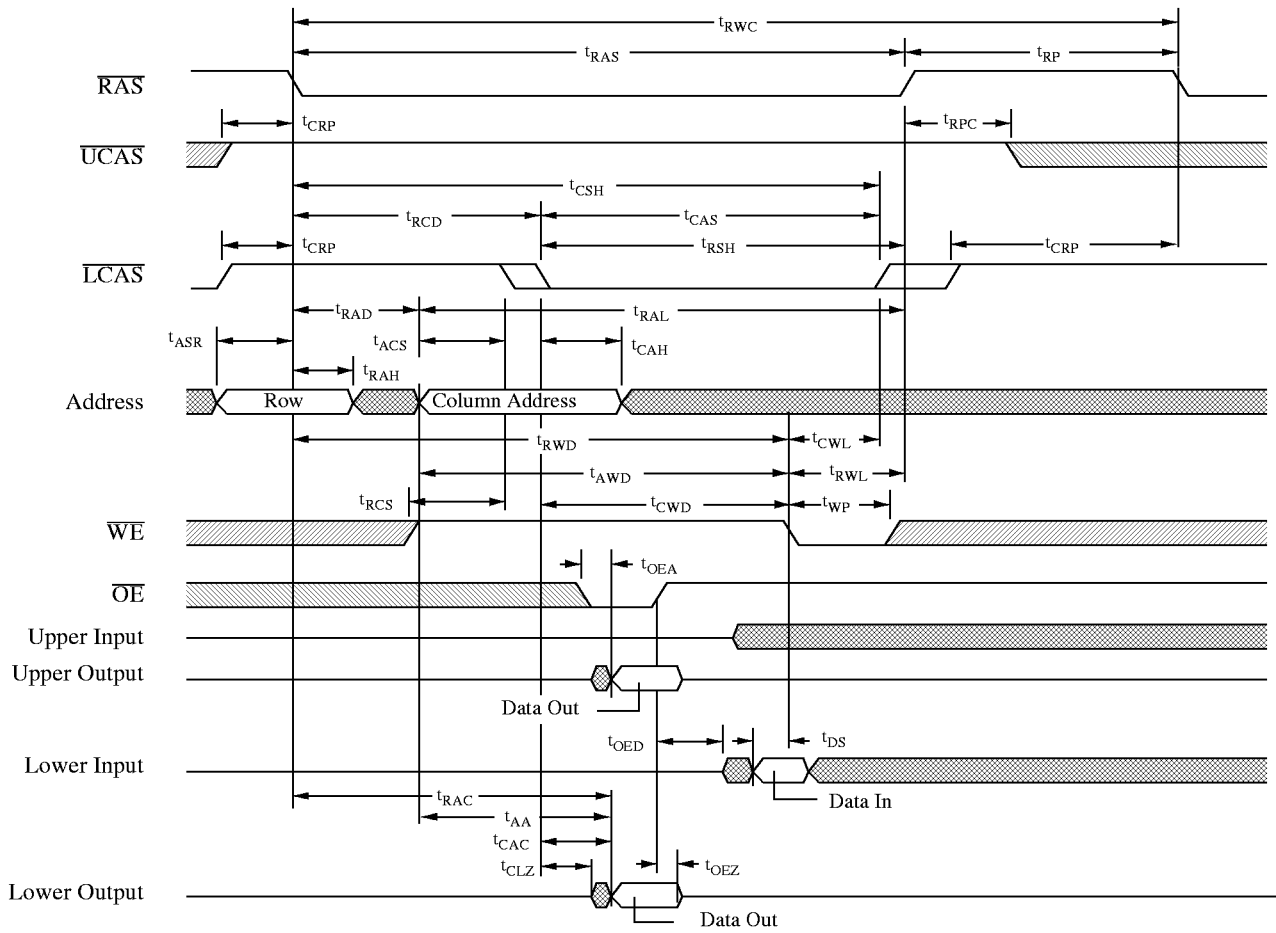


Upper byte read-modify-write cycle waveform



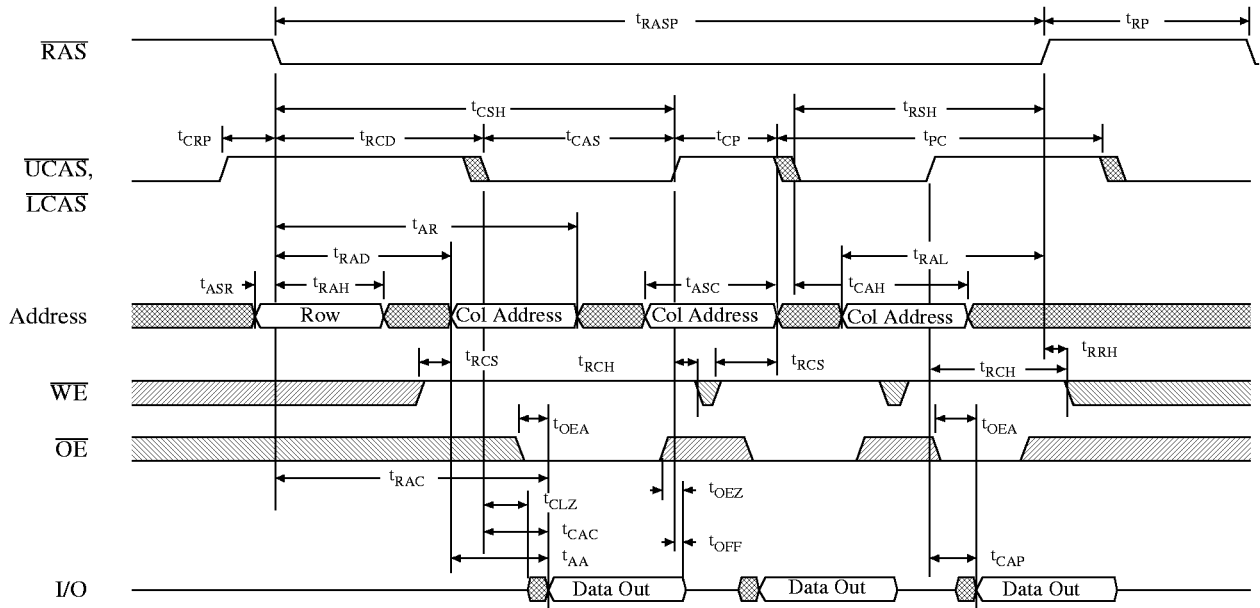


Lower byte read-modify-write cycle waveform

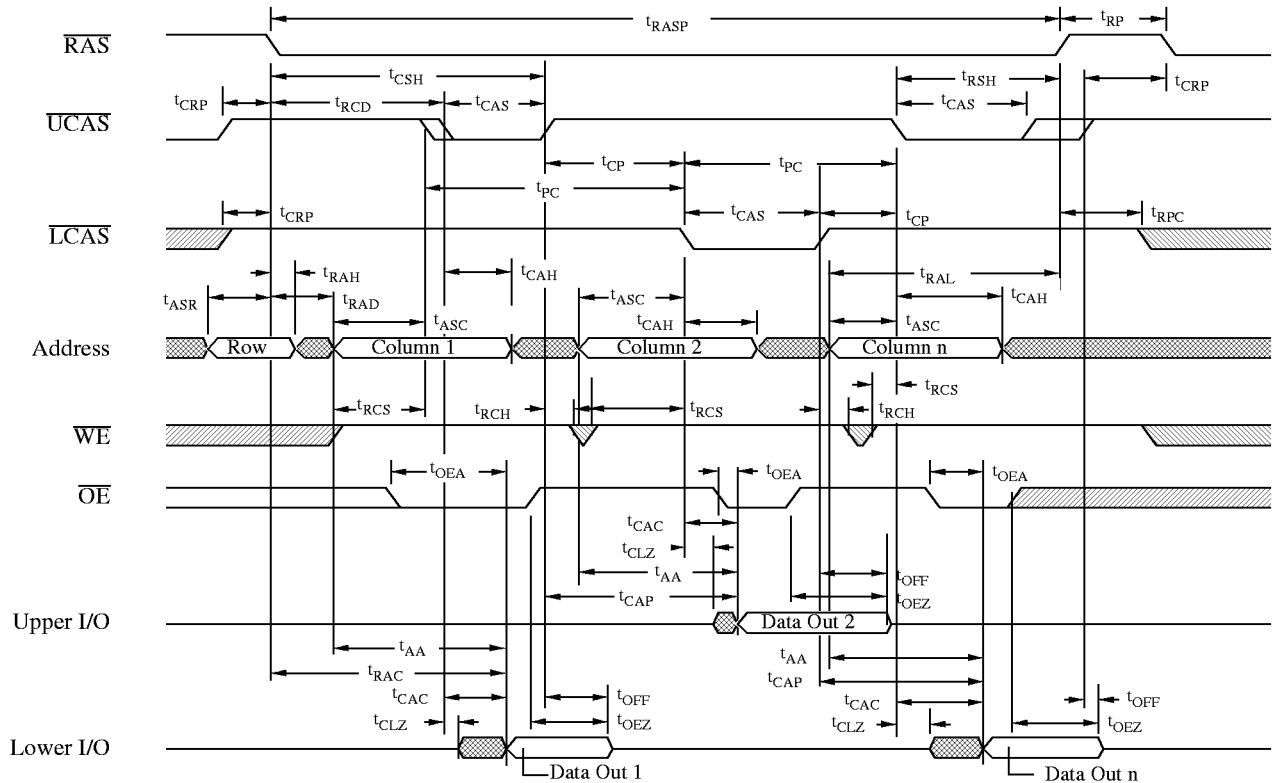




EDO page mode read cycle waveform

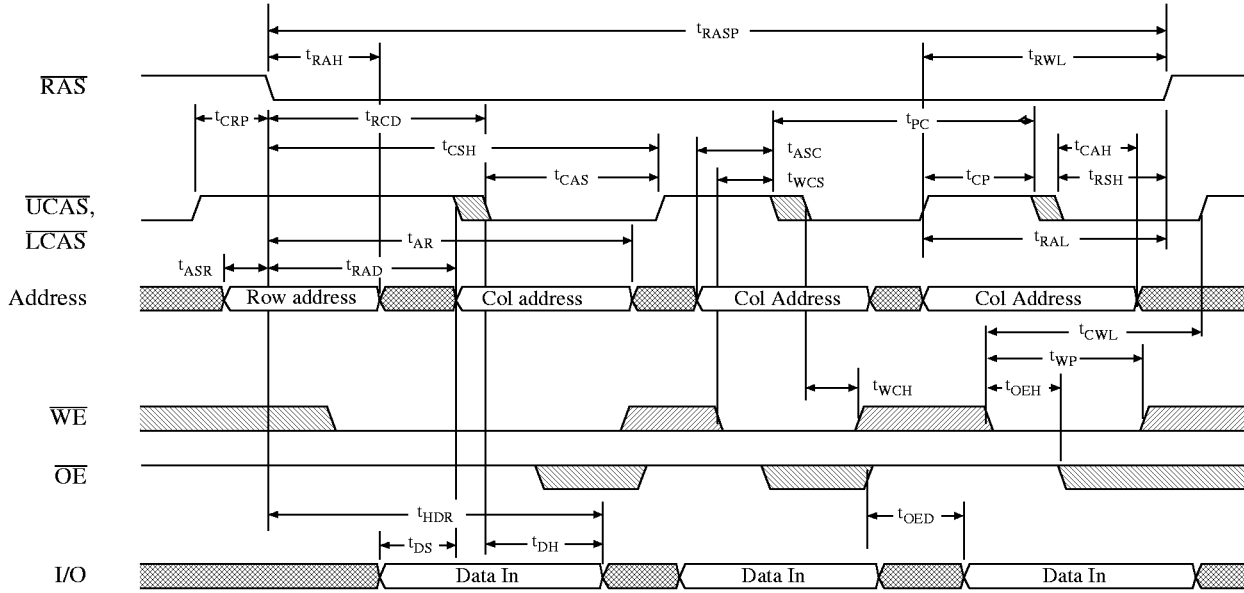


EDO page mode byte read cycle waveform

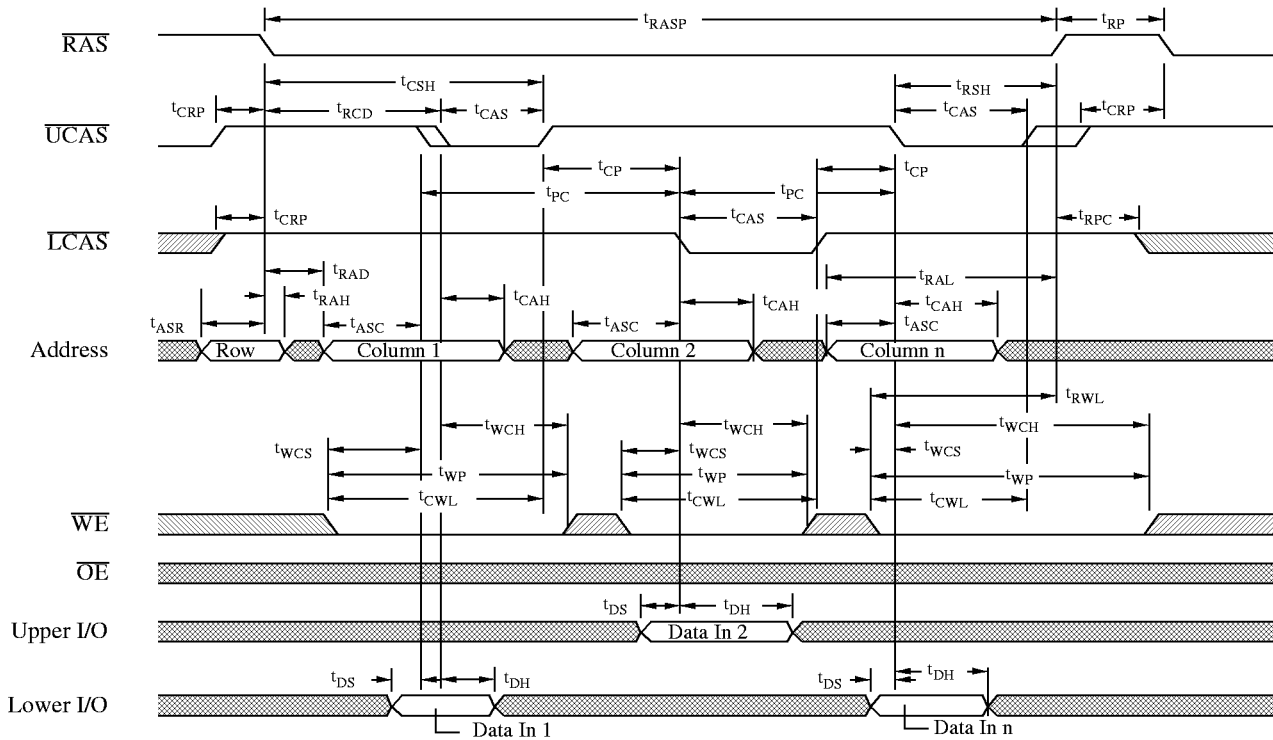




EDO page mode early write cycle waveform



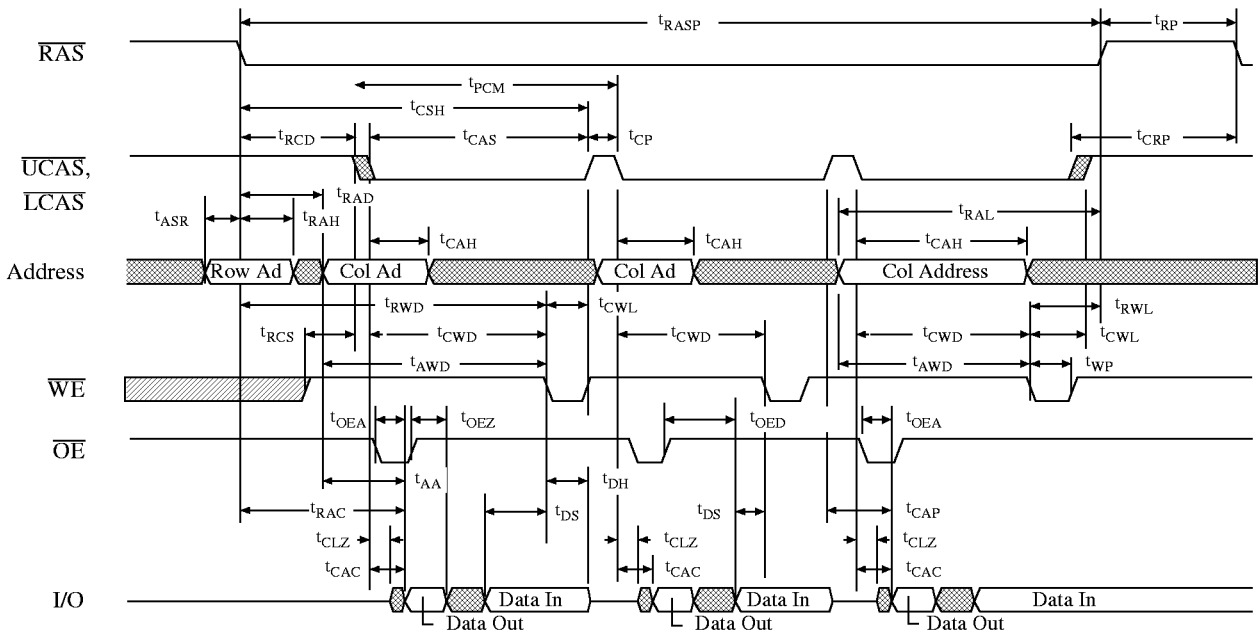
EDO page mode byte early write cycle waveform





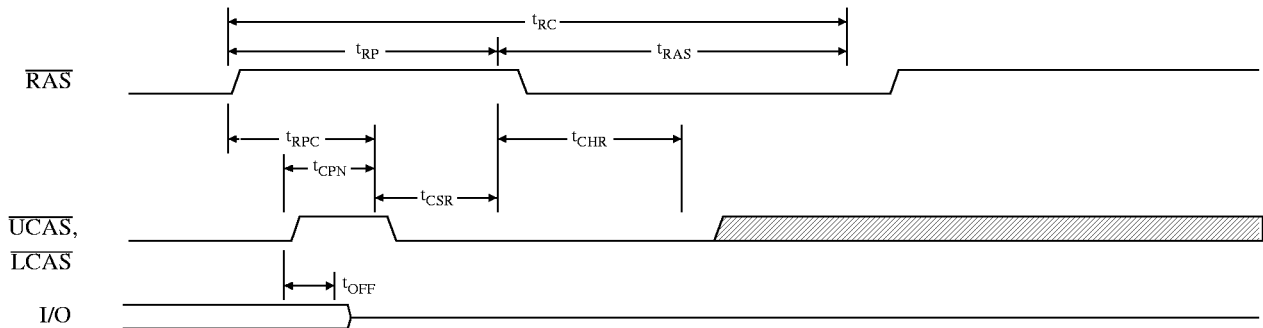


EDO page mode read-modify-write cycle waveform



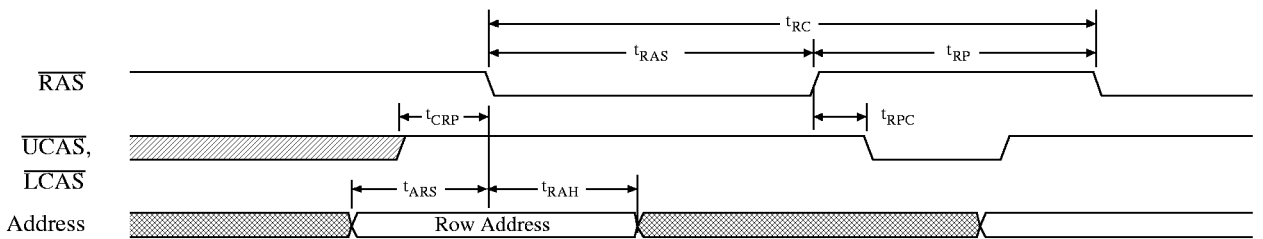
CAS-before-RAS refresh cycle waveform

(WE = A9 = V<sub>IH</sub> or V<sub>IL</sub>)



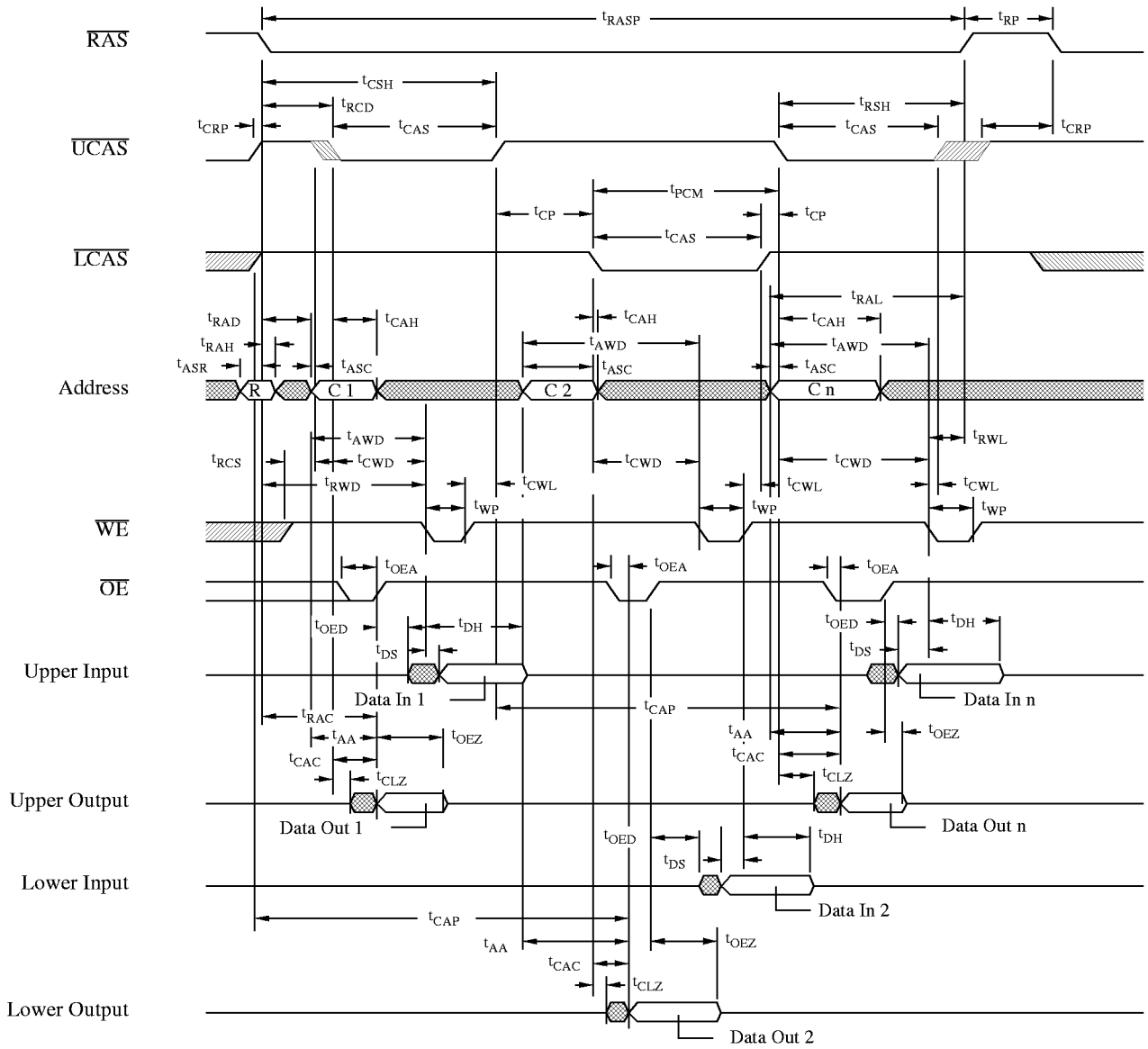
RAS only refresh cycle waveform

(WE = OE = V<sub>IH</sub> or V<sub>IL</sub>)



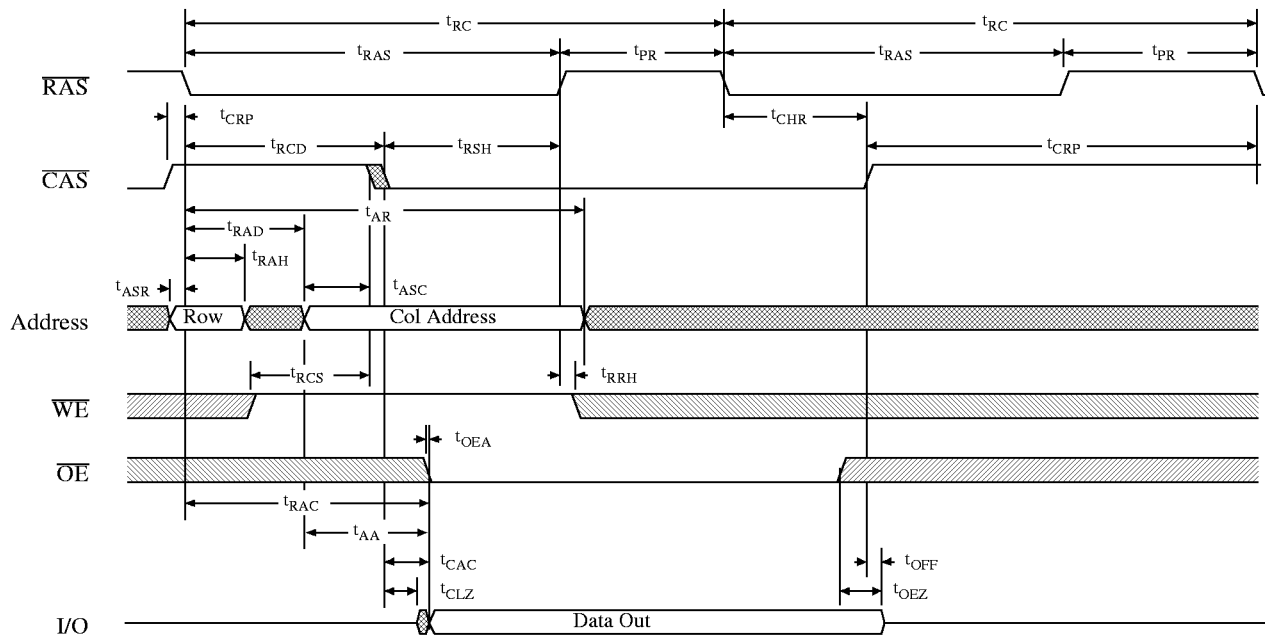


EDO page mode byte read-modify-write cycle

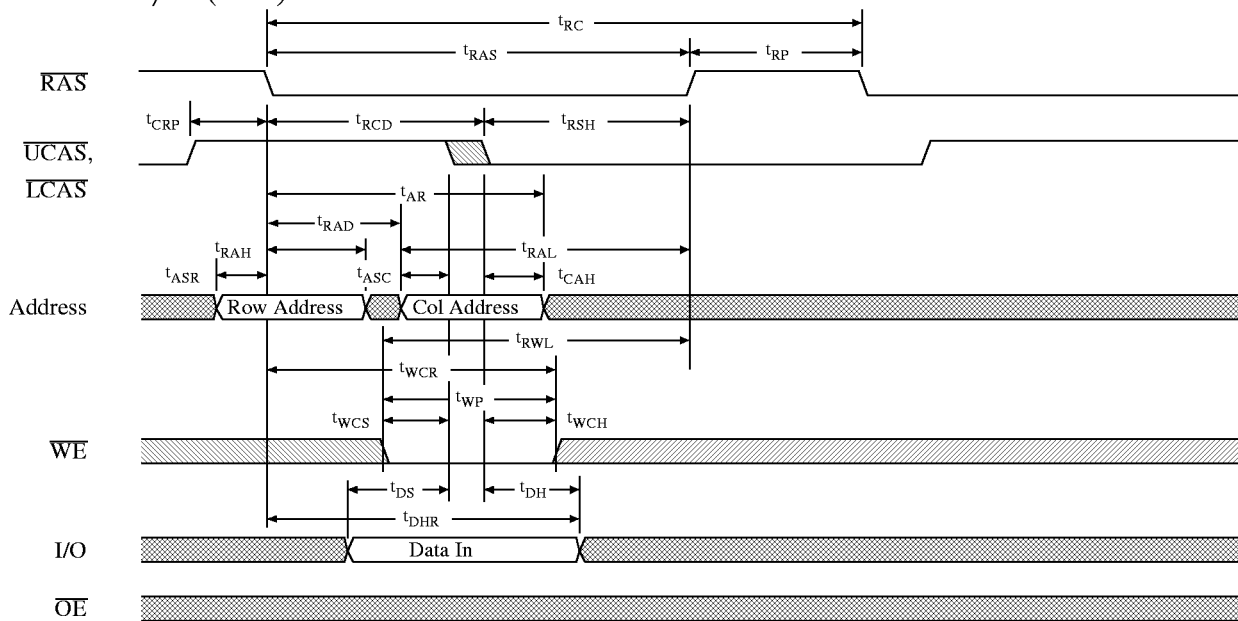




Hidden refresh cycle (read) waveform

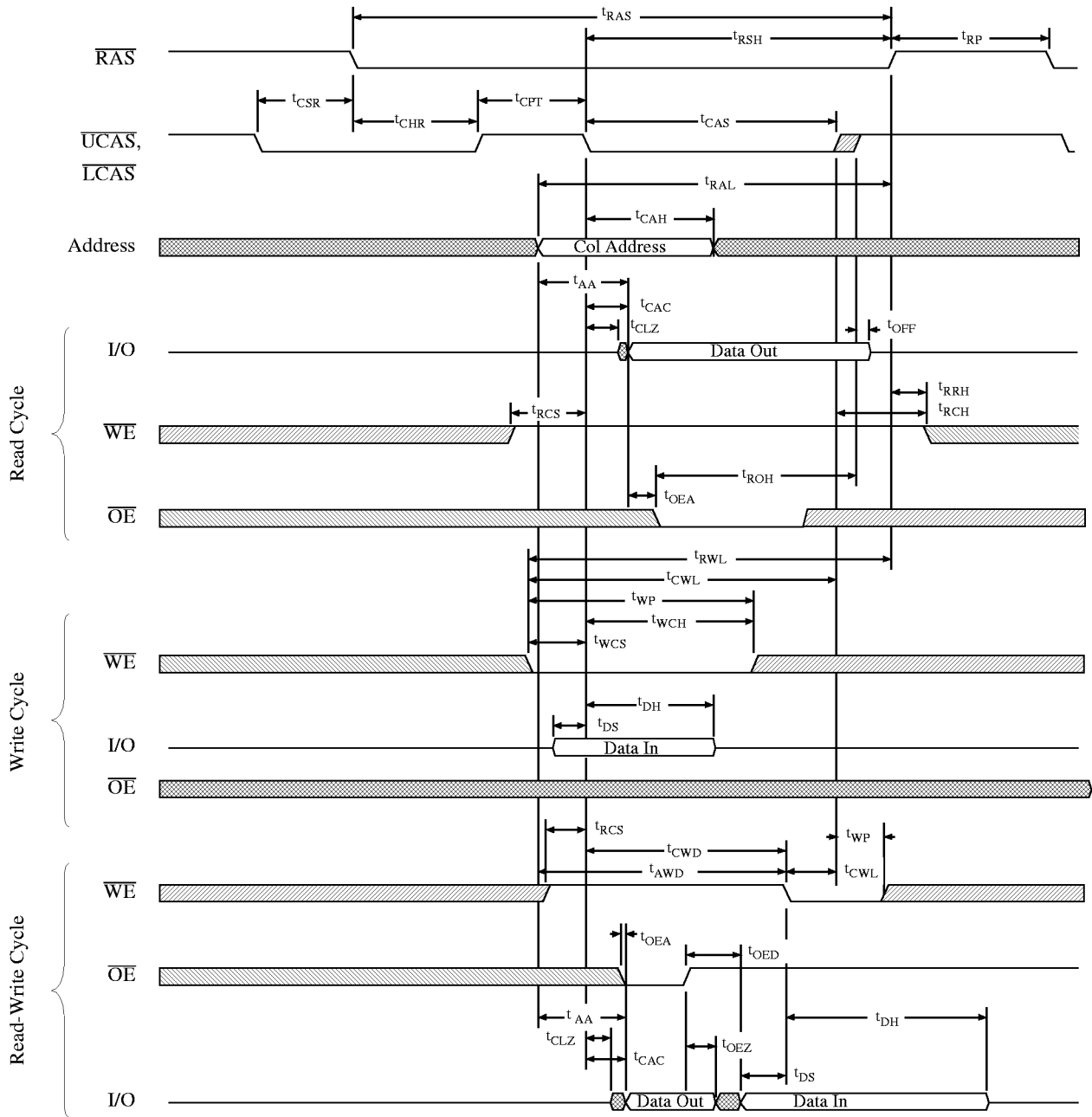


Hidden refresh cycle (write) waveform



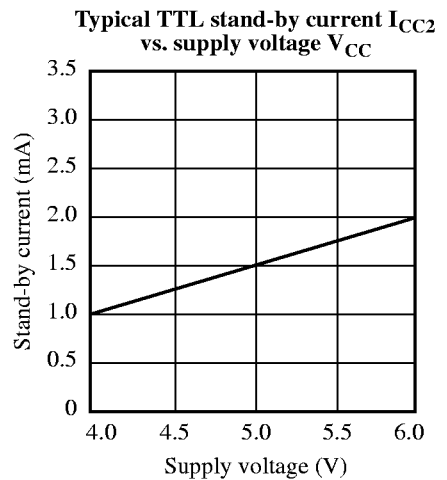
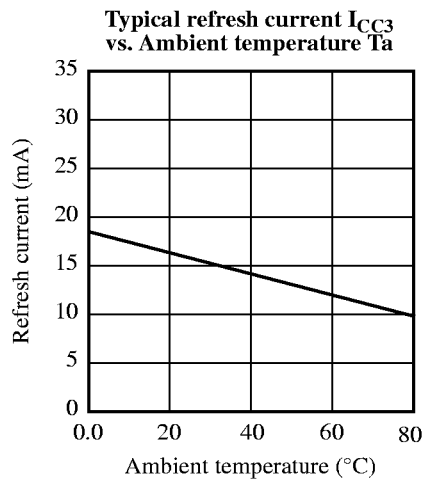
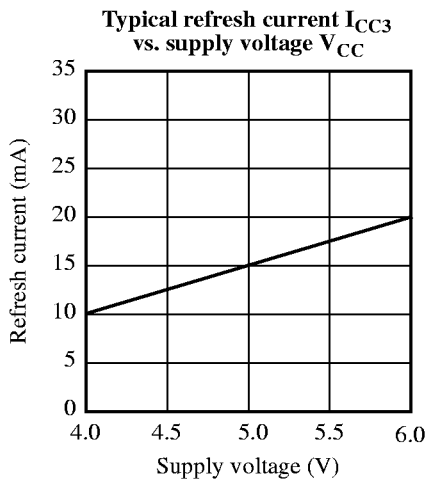
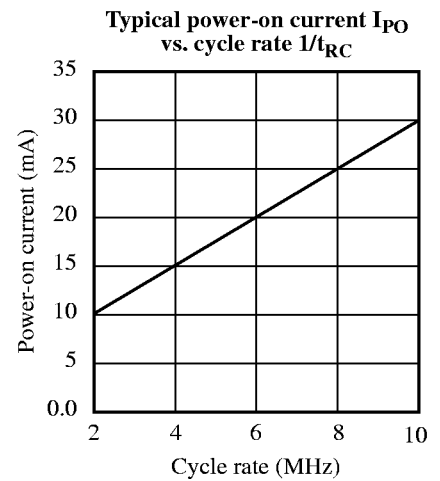
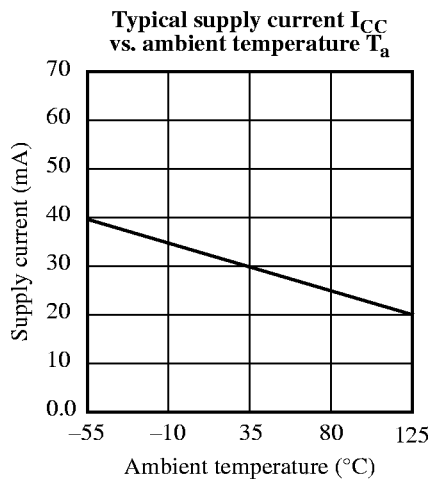
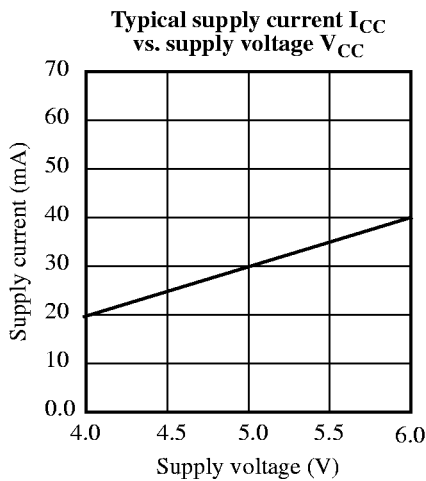
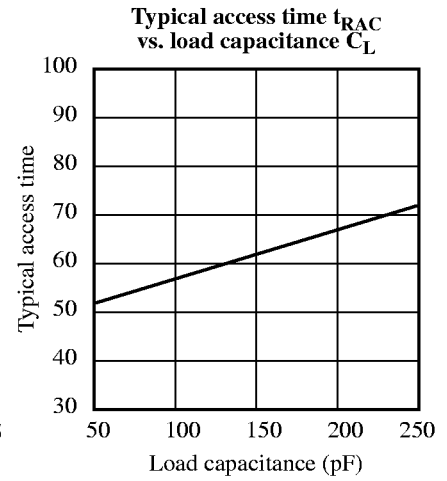
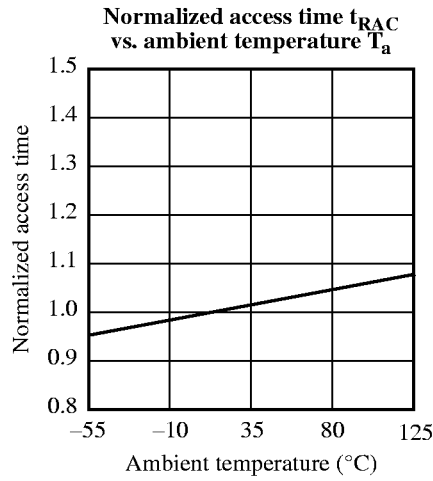
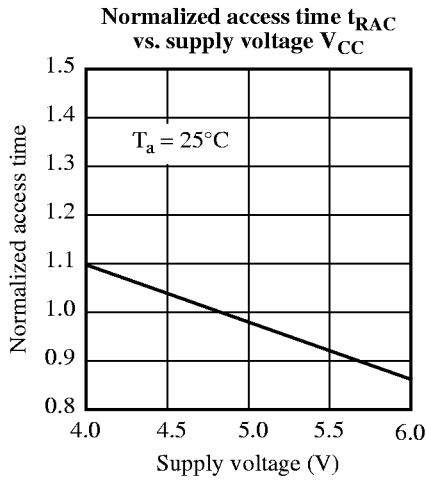


CAS-before-RAS refresh counter test cycle waveform



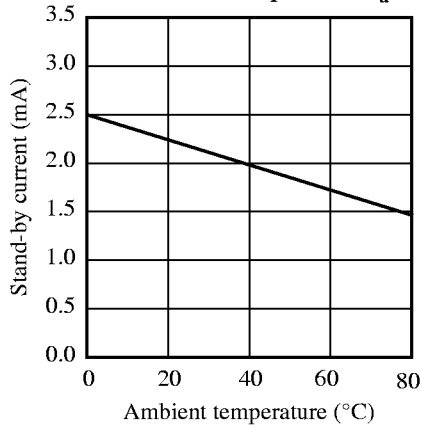


Typical DC and AC characteristics

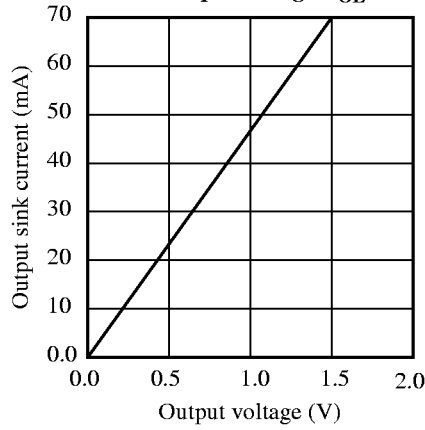




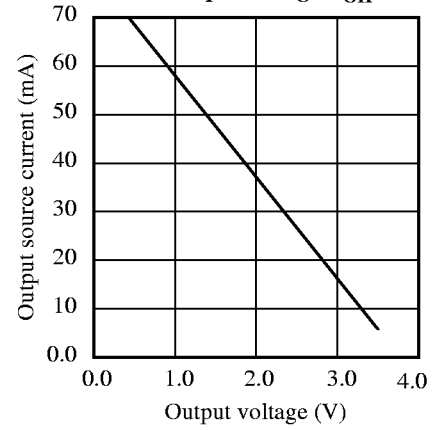
Typical TTL stand-by current  $I_{CC2}$  vs. ambient temperature  $T_a$



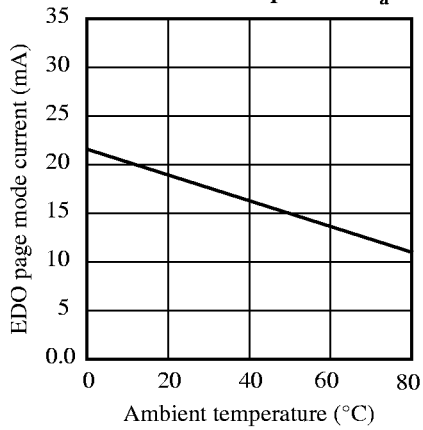
Typical output sink current  $I_{OL}$  vs. output voltage  $V_{OL}$



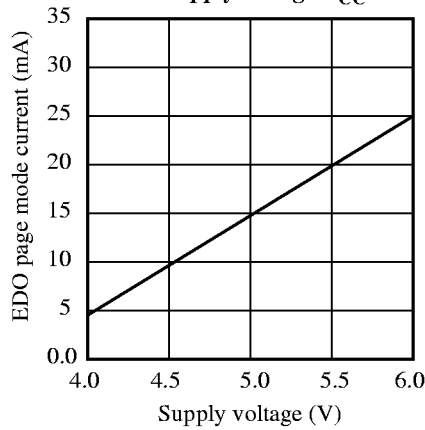
Typical output source current  $I_{OH}$  vs. output voltage  $V_{OH}$



Typical EDO page mode current  $I_{CC4}$  vs. ambient temperature  $T_a$

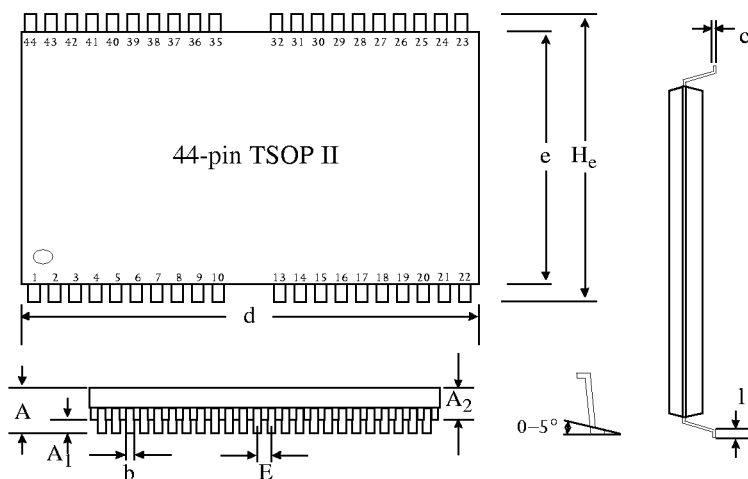


Typical EDO page mode current  $I_{CC4}$  vs. supply voltage  $V_{CC}$

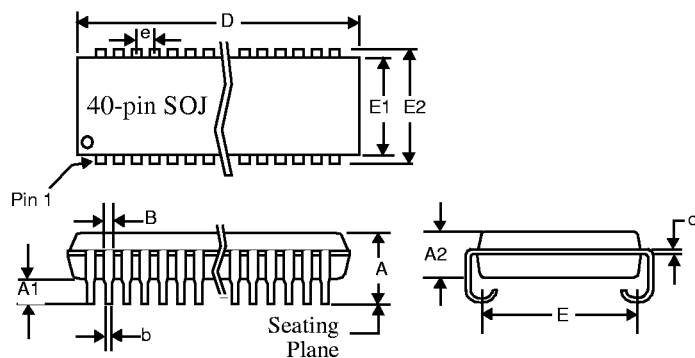




Package dimensions



44-pin TSOP II		
	Min (mm)	Max (mm)
A		1.2
A <sub>1</sub>	0.05	
A <sub>2</sub>	0.95	1.05
b	0.25	0.45
c	0.015 (typical)	
d	20.85	21.05
e	10.06	10.26
H <sub>e</sub>	11.56	11.96
E	0.80 (typical)	
l	0.40	0.60



40-pin SOJ 400 mil		
	Min	Max
A	0.128	0.148
A <sub>1</sub>	0.025	-
A <sub>2</sub>	1.105	1.115
B	0.026	0.032
b	0.015	0.020
c	0.007	0.013
D	1.120	1.130
E	0.370 (typical)	
E <sub>1</sub>	0.395	0.405
E <sub>2</sub>	0.435	0.445

Capacitance

$f = 1 \text{ MHz}$ ,  $T_a = \text{room temperature}$ ,  $V_{CC} = 5V \pm 0.5V$

Parameter	Symbol	Signals	Test Conditions	Max	Unit
Input capacitance	$C_{IN1}$	A0 to A8	$V_{in} = 0V$	5	pF
	$C_{IN2}$	RAS, UCAS, ICAS, WE, OE	$V_{in} = 0V$	7	pF
I/O capacitance	$C_{I/O}$	I/O0 to I/O15	$V_{in} = V_{out} = 0V$	7	pF

Ordering codes

Package \ Access Time	30ns	35ns	50 ns	60 ns
Plastic SOJ, 400 mil, 40-pin	AS4C256K16E0-30JC	AS4C256K16E0-35JC	AS4C256K16E0-50JC	AS4C256K16E0-60JC
TSOP II, 400 mil, 40/44-pin			AS4C256K16E0-50TC	

Part numbering system

AS4C	256K16E0	-XX	X	C
DRAM prefix	Device number	RAS access time	Package: J = SOJ T = TSOP II	Commercial temperature range, 0°C to 70 °C