Final

Am7901B/C
Subscriber Line Audio-Processing Circuit (SLAC) WORLD-CHIP

Advanced
Micro
Devices

DISTINCTIVE CHARACTERISTICS

- Combination CODEC and Filter
- No trimming or adjustments required
- Uses digital signal processing
- Six user-programmable digital filters
- Dynamic Time Slot assignment
- Only two external components (non-precision)
- Dual PCM ports

- 4.096-MHz, 64-channel expanded mode operation
- Built-in test modes
- Microprocessor-compatible Serial Interface
- Control Interface to SLIC
- Low standby power
- Selectable A-law, μ-law (Am7901B) or linear, A-law (Am7901C)

GENERAL DESCRIPTION

The Subscriber Line Audio-Processing Circuit (SLAC™) performs the codec and filtering functions necessary in digital voice switching machines. In this application, the SLAC processes voiceband analog signals into Pulse-Code Modulated (PCM) outputs and processes PCM inputs into analog outputs. The SLAC's performance is compatible with applicable AT&T® and CCITT specifications. The device consists of three main sections: transmit processor, receive processor, and control logic.

The transmit section contains an anti-aliasing filter, an interpolative A/D converter, and a digital signal processor. The analog signals received are converted and digitally processed to generate either 8-bit μ-law or A-law codes (Am7901B) or 16-bit linear or 8-bit A-law (Am7901C). Either one of two output ports may be selected for PCM data transmission.
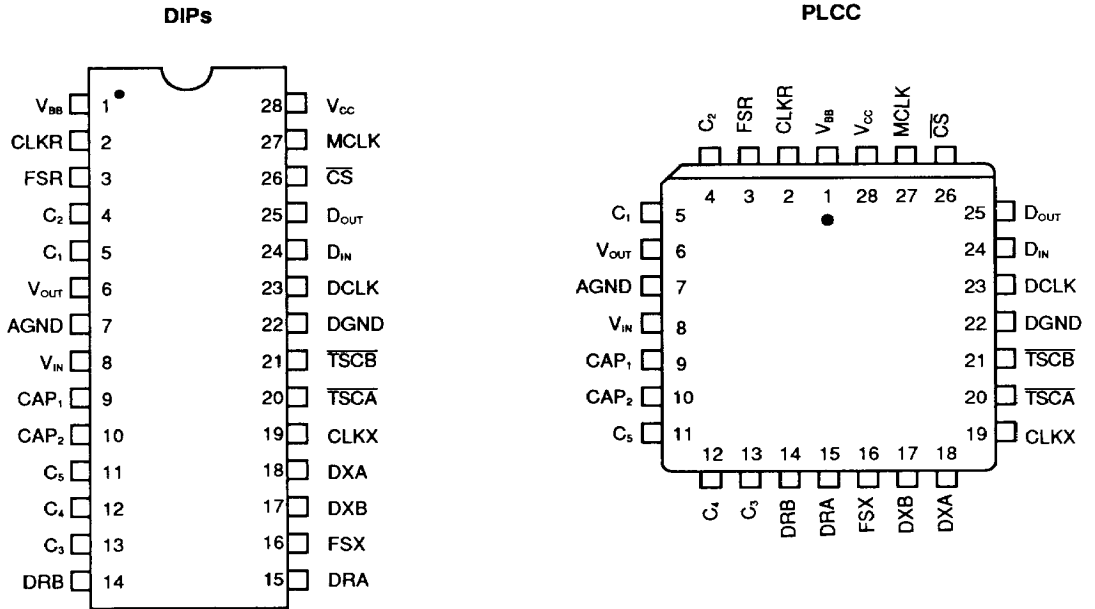
BLOCK DIAGRAM
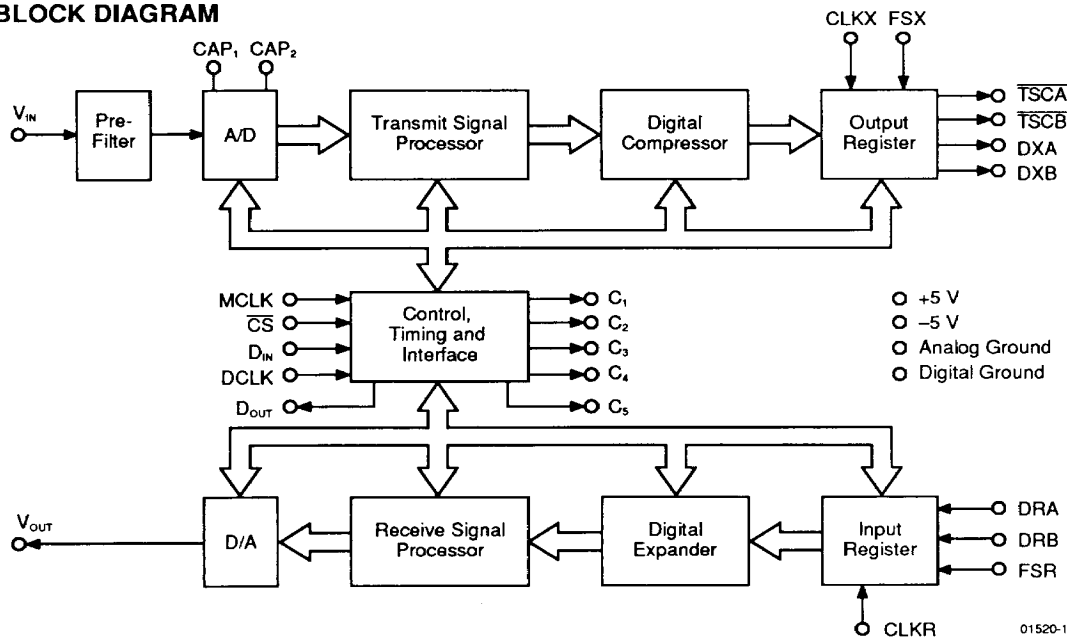
01520-1

GENERAL DESCRIPTION (continued)

The receive section contains a digital signal processor and a D/A converter. Either 8 bit μ-law or A-law codes (Am7901B) or 16-bit linear or 8-bit A-law codes (Am7901C) are received, processed and converted to analog signals. Either one of two input ports may be selected for reception of PCM data.

The control I/O provides a microprocessor-compatible serial interface and allows the user bi-directional access to many programmable features and the capability to completely control the operation of the device via a comprehensive set of commands.
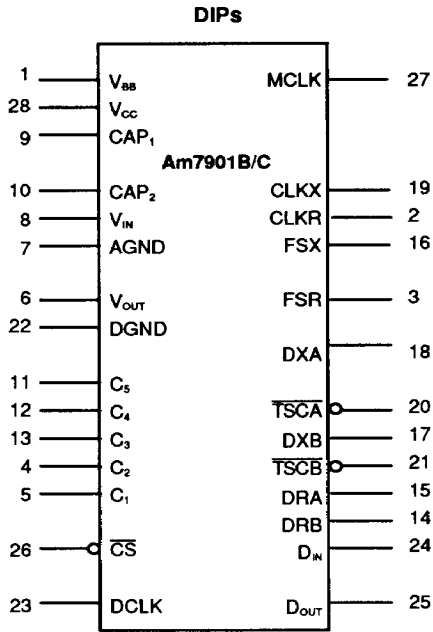
CONNECTION DIAGRAM
Top View

DIPs

PLCC

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL

DIPs

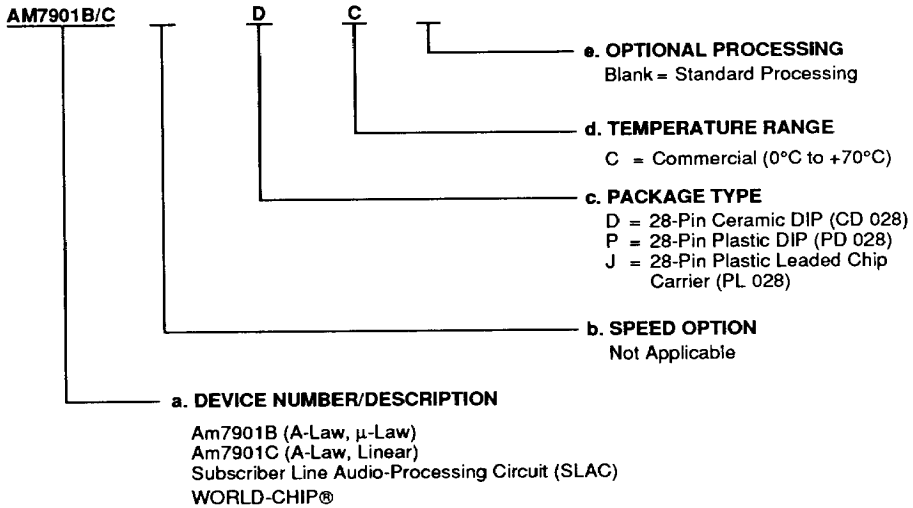|		
1 — V_{BB}	MCLK — 27	
28 — V_{CC}		
9 — CAP_1		
	Am7901B/C	
10 — CAP_2	CLKX — 19	
8 — V_{IN}	CLKR — 2	
7 — AGND	FSX — 16	
6 — V_{OUT}	FSR — 3	
22 — DGND		
	DXA — 18	
11 — C_5		
12 — C_4	$\overline{TSCA}$ — 20	
13 — C_3	DXB — 17	
4 — C_2	$\overline{TSCB}$ — 21	
5 — C_1	DRA — 15	
	DRB — 14	
26 — $\overline{CS}$	D_{IN} — 24	
23 — DCLK	D_{OUT} — 25	

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ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing

AM7901B/C   **D**   **C**

e. OPTIONAL PROCESSING
Blank = Standard Processing

d. TEMPERATURE RANGE
C = Commercial (0°C to +70°C)

c. PACKAGE TYPE
D = 28-Pin Ceramic DIP (CD 028)
P = 28-Pin Plastic DIP (PD 028)
J = 28-Pin Plastic Leaded Chip
       Carrier (PL 028)

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am7901B (A-Law, μ-Law)
Am7901C (A-Law, Linear)
Subscriber Line Audio-Processing Circuit (SLAC)
WORLD-CHIP®

Valid Combinations	
AM7901B	DC, PC, JC
AM7901C	DC, PC, JC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTIONS

AGND
Analog ground.

$C_5–C_1$
Latched Outputs

The serial interface may be used to write data to a register whose outputs are brought out to $C_5–C_1$. These 5 lines are TTL-compatible and may be used to control the operation of a SLIC or any other device associated with the subscriber line. C_5 is used as an output in the Auto-zero Speedup Mode.

CAP_2, CAP_1
An external series resistor and capacitor are connected to these pins. These components are part of the integrator in the A/D converter. The recommended values of these non-precision components are 1K ohm ±5% and 2000 pF ±20%.

CLKX, CLKR
PCM Clocks

The PCM Clocks determine the rate at which PCM data is serially shifted into or out of the PCM ports. The maximum clock frequency is 4.096 MHz and the minimum clock frequency is 128 kHz. CLKX determines the rate at which PCM data is transmitted. CLKR determines the rate at which PCM data is received.

$\overline{CS}$
Chip Select

The Chip Select input enables the device to either input or output control data. A level of –5 V on this input places the device in the Auto-zero Speedup Mode.

DCLK
Data Clock

The Data Clock shifts control data either into or out of the SLAC. The maximum clock rate is 2.048 MHz. A level of –5 V on this pin forces the device into the Reset state.

D_{IN}
Data Input

Control data is serially written via the Data Input port. The input rate is determined by the Data Clock.

D_{OUT}
Data Output

Control data is serially read via the Data Output port. The output rate is determined by the Data Clock. D_{OUT} is high-impedance when control data output is completed and $\overline{CS}$ is High.

DGND
Digital ground.

DRA, DRB
PCM Inputs

The receive-PCM data is serially received from either the DRA or the DRB port. The port selection is under user program control. For μ-law and A-law, 8 bits are received and for linear code, 16 bits are received. The data is received in 8- or 16-bit bursts every 125 μs at the CLKR rate.

DXA, DXB
PCM Outputs

The transmit-PCM data is serially fed out to either the DXA or the DXB port. The port selection is under user program control. For μ-law and A-law, 8 bits are transmitted and for linear code, 16 bits are transmitted. The output is available every 125 μs and the data is shifted out in 8 or 16-bit bursts at the CLKX rate. DXA and DXB are high-impedance between bursts and also in the standby mode.

FSX, FSR
Frame Sync

The Frame Sync pulse is an 8-kHz signal which identifies the beginning of a frame. The SLAC references individual time slots with respect to the Frame Sync pulse. FSX is the transmit-PCM Frame Sync and FSR is the receive-PCM Frame Sync. The FSX pulse must not be longer than 8 clock periods when companded code is used, and 16 clock periods when linear code is used.

MCLK
Master Clock

The Master Clock must be a 2.048 ±100 ppm clock input. MCLK is used by the digital signal processors. Loss of MCLK must be treated like a loss of power.

$\overline{TSCA}$, $\overline{TSCB}$
Time Slot Control

The Time Slot Control outputs are open-drain outputs and are normally High. $\overline{TSCA}$ is Low when PCM data is present on the DXA output and $\overline{TSCB}$ is Low when PCM data is present on the DXB output.

V_{BB}
–5-V power supply.

V_{CC}
+5-V power supply.

V_{IN}
Analog Input

The analog input is applied to the transmit path of the SLAC. The signal is sampled, digitally processed and encoded for the PCM output.

V_{OUT}
Analog Output

The received-PCM data is digitally processed and converted to an analog signal at the V_{OUT} pin.

FUNCTIONAL DESCRIPTION

Device Operation

General

The Am7901B/C performs the codec and filtering functions associated with the four-wire section of the subscriber line circuitry in a digital switch. When used with the Am795XX Subscriber Line Interface Circuit (SLIC), the pair provide a complete solution to the BORSCHT functions (see Figure 1).

The SLAC contains A/D and D/A converters. A microprocessor-compatible interface is provided to program the device into a variety of modes. These operating modes include companded or linear-code operation, dynamic time-slot assignment, and PCM-port selection.

The SLAC samples the analog signal at the V_{IN} pin and digitally processes it to produce either a linear or companded PCM code at the DXA or DXB output (see Figure 2). Conversely, it receives either a linear or companded PCM code at the DRA or DRB input and digitally processes it to produce an analog output at the V_{OUT} pin. The processing is accomplished at the frame rate (8 kHz), and the digital output/input is available for transmission/reception every 125 µs.

Transmit Signal Processor

In the transmit path (see Figure 3), the analog signal is converted, filtered, compressed, and made available for output.

The prefilter is an integrated anti-aliasing filter which prevents signals near the sample rate from folding back into the voiceband during decimation. The A/D is designed to have a wide dynamic range and excellent signal-to-noise performance. It uses a modified sigma delta loop with a D/A converter to track the input signal at a 512-kHz sampling rate.

The Signal Processor contains an ALU, RAM, ROM and control logic to implement the filter sections. The B, X, and GX blocks shown in Figure 3 are user-programmable filter sections and their coefficients are stored in the Coefficient RAM. These filters may be transparent when not required in a system. The digital compressor may be bypassed when linear-code operation is desired.

The decimator reduces the high input sample rate. The X filter is a 4-tap Finite Impulse Response (FIR) section and is part of the frequency response correction network. The GX filter allows the user to program up to 12-dB gain in the transmit path with an accuracy of ±0.051 dB up to 10.4 dB and ±0.15 dB up to 12 dB. The B filter has 8 taps and operates on samples input from the Receive Signal Processor in order to provide trans-hybrid balancing in the loop. The low-pass filter limits the output bandwidth to meet the transmission requirements. The high-pass filter rejects 15-Hz and 50/60-Hz frequencies and may be disabled for testing.

Transmit PCM Interface

The Transmit PCM Interface receives either a 16-bit linear code (for linear operation) or an 8-bit compressed code (for µ-law and A-law operation) from the digital compressor. This code is loaded into the output register. The Transmit PCM Interface logic (see Figure 4) controls the transmission of data onto the PCM highway through the output port-selection circuitry and the Time Slot Control block.

The Frame Sync (FSX) pulse identifies the beginning of a Transmit frame and all channels (time slots) are referenced to it. The logic contains user-programmable Transmit Time Slot and Transmit Clock Slot registers. The Time Slot register is normally 5-bits wide and allows up to thirty-two 8-bit channels or sixteen 16-bit channels (using CLKX = 2.048 MHz) in each frame. But in the expanded mode, 6 bits may be programmed to give thirty-two 16-bit channels or sixty-four 8-bit channels (using CLKX = 4.096 MHz) in each frame. The expanded mode bit becomes the sixth bit of the Time Slot register. If this bit is Low, one of channels 0 to 31 is selected and if it is High, one of channels 32 to 64 is selected. This feature allows any combination of channel assignments and clock frequencies (over a range of 128 kHz to 4.096 MHz) in a system. For µ-law and A-law operation, 8 bits/channel are output and for linear code operation, 16 bits/channel are output. The data is transmitted Most Significant Bit (MSB) first. The Clock Slot register is 3 bits wide and may be programmed to offset the Time Slot assignment by 0 to 7 CLKX periods to eliminate any clock skew in the system (see Figure 5).

In the Am7901B/C, the PCM data may be user-programmed to be output onto one of two ports, DXA or DXB. Correspondingly, either $\overline{TSCA}$ or $\overline{TSCB}$ is also Low.

Receive PCM Interface

The Receive PCM Interface logic (see Figure 6) controls the reception of data from the PCM highway and transfers it for expansion (µ-law or A-law) to the Receive Signal Processor. The operation of this interface is identical to the Transmit section.

The Frame Sync (FSR) pulse identifies the beginning of a Receive frame and all channels (time slots) are referenced to it. The logic contains user-programmable Receive Time Slot and Receive Clock Slot registers. The Time Slot register is normally 5-bits wide and allows up to thirty-two 8-bit channels (using CLKR = 2.048 MHz) in each frame. But in the expanded mode, 6 bits may be programmed to give thirty-two 16-bit channels or sixty-four 8-bit channels (using CLKR = 4.096 MHz) in each frame. The expanded mode bit becomes the sixth bit of the Time Slot register. If this bit is Low, one of channels 0 to 31 is selected and if it is High, one of channels 32 to 63 is selected. This feature allows any combination

of clock frequencies (over a range of 128 kHz to 4.096 MHz) and channel assignments in a system. For μ-law and A-law operation, 8 bits/channel are input and for linear code, 16 bits/channel are input. The MSB of the code must be received first. The Clock Slot register is 3-bits wide and may be programmed to offset the Time Slot assignment by 0 to 7 CLKR periods to eliminate any clock skews in the system (see Figure 7).

In the Am7901B/C, the PCM data may be user-programmed to be input from one of two ports, DRA or DRB.
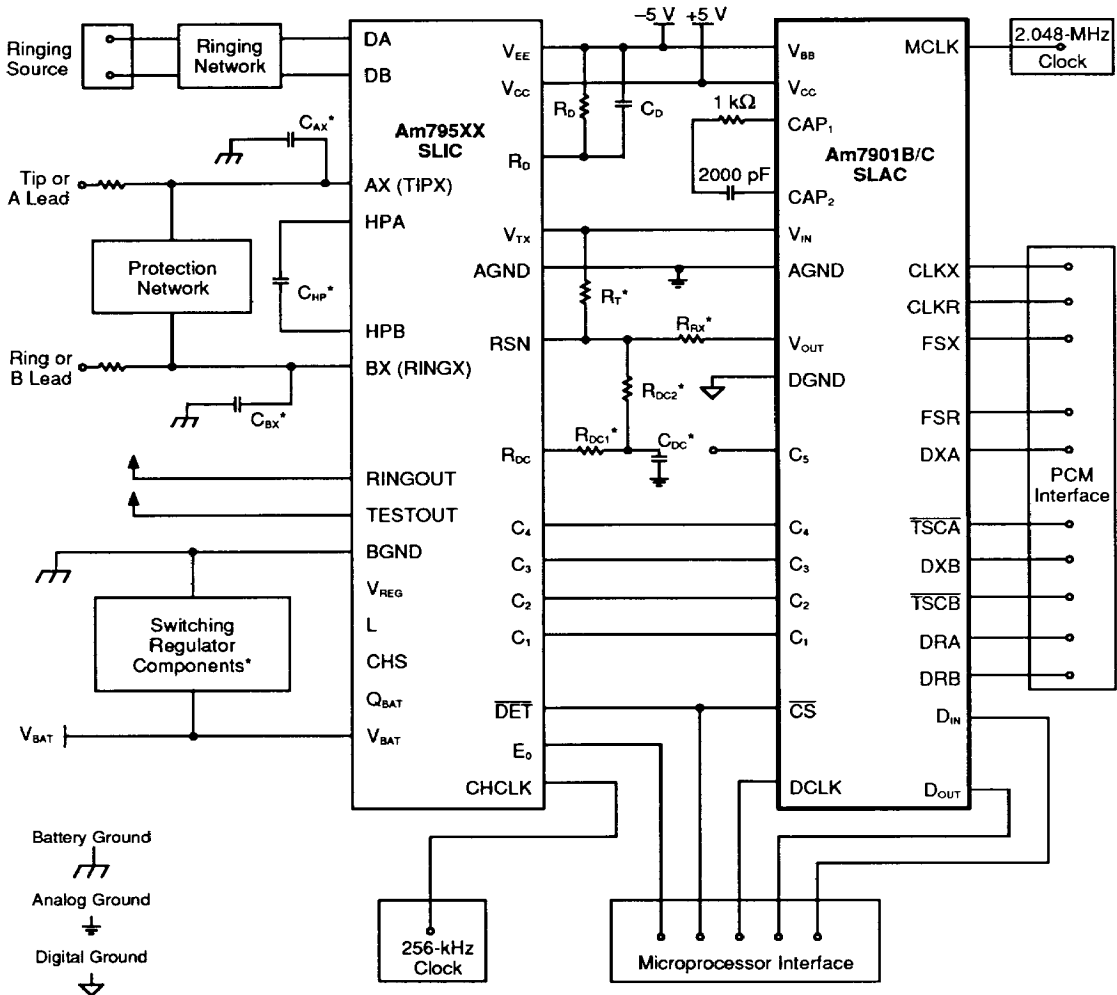
*Component values are user-programmable. Refer to SLIC product specification.

Figure 1. Single-Channel Subscriber Line System
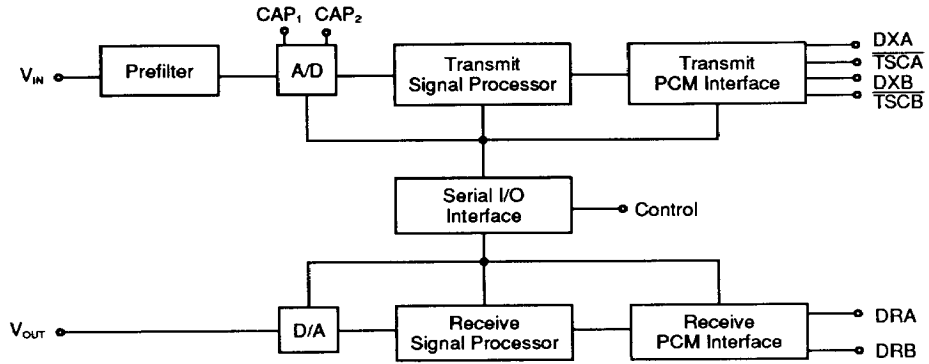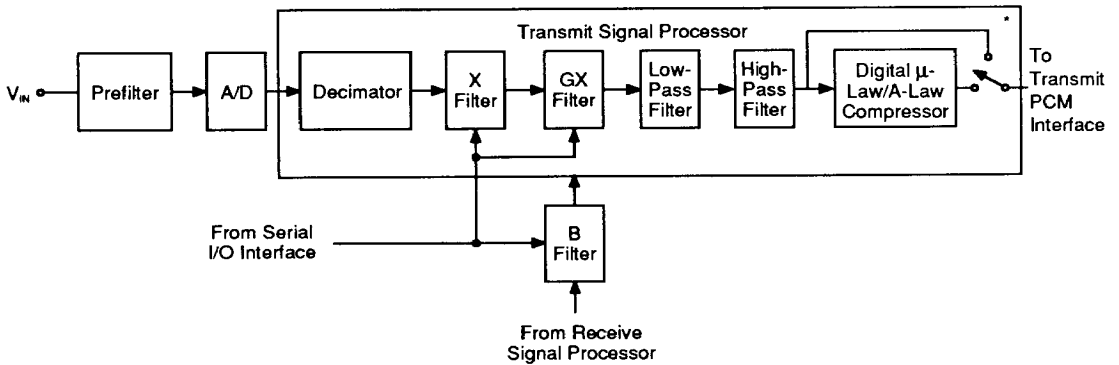
01520-3

Figure 2. SLAC Block Diagram   01520-4

* Am7901C linear mode only.

Figure 3. Transmit Signal Processor   01520-5
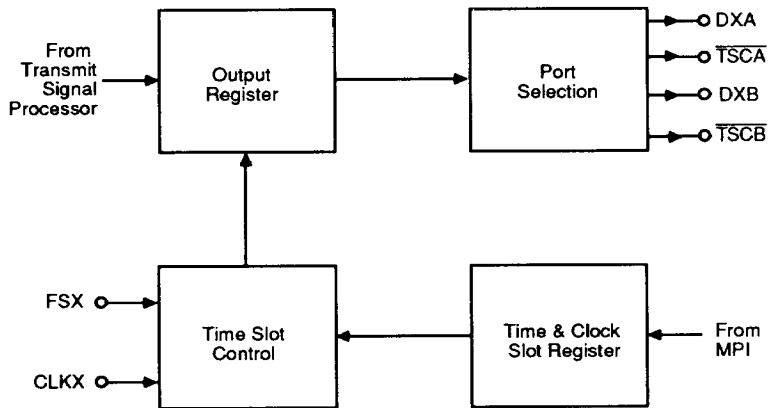

Figure 4. Transmit PCM Interface   01520-6

Receive Signal Processor

In the receive path (see Figure 8), the digital signal is expanded, filtered, converted to analog, and output onto the V_{OUT} pin.

The Signal Processor contains an ALU, RAM, ROM and control logic to implement the filter sections. The Z, R and GR are user-programmable filter sections and their coefficients are stored in the coefficient RAM. These filters may be made transparent when not required in a system.

The low-pass filter band-limits the signal. The GR filter allows the user to program a loss of up to 12 dB with an accuracy of ±0.051 dB. The R filter is a 4-tap FIR section and is part of the frequency response correction network. The Z filter provides feedback from the Transmit Signal Processor to the Receive Signal Processor and is used to modify the effective input impedance to the system. The interpolator provides the higher sample rate to the D/A converter.
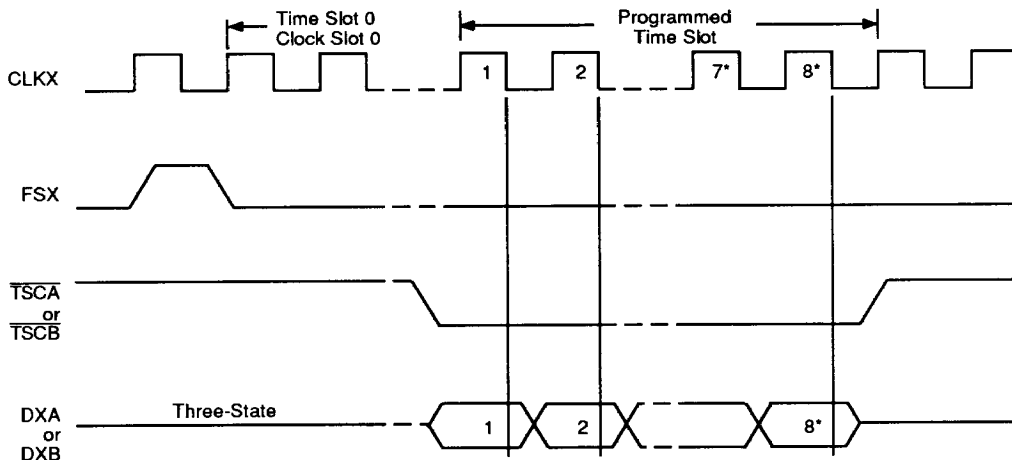
*For linear code, the 7th and 8th clock cycles correspond to the 15th and 16th clock cycles.

Figure 5. Transmit PCM Timing Diagram   01520–7
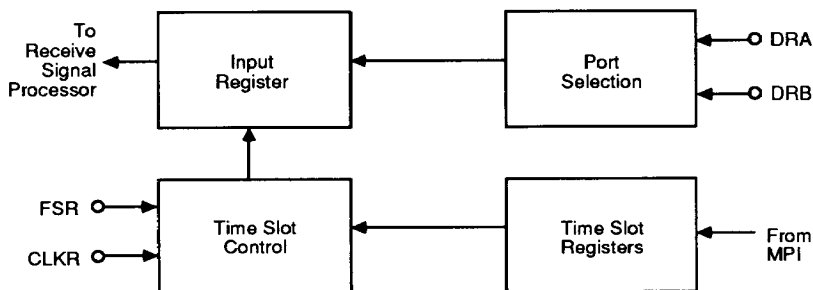
Figure 6. Receive PCM Interface   01520–9
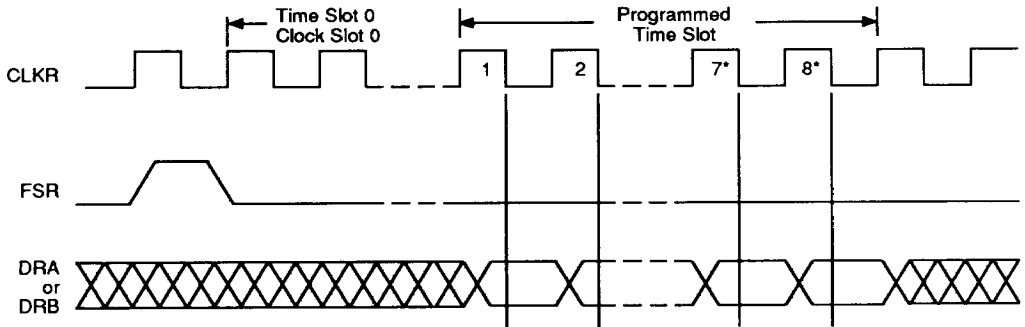
*For linear code, the 7th and 8th clock cycles correspond to the 15th and 16th clock cycles.

01520-10

Figure 7. Receive PCM Timing Diagram
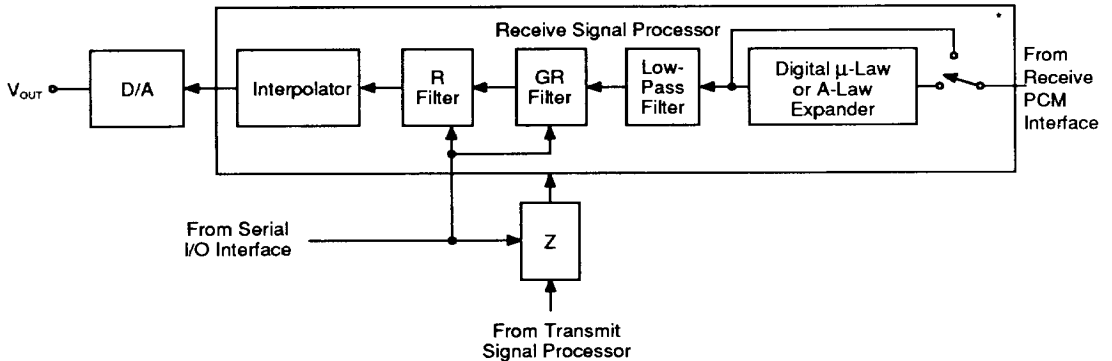
* For Am7901B, the expander cannot be bypassed.

Figure 8. Receive Signal Processor

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Serial I/O Interface

A microprocessor may be used to program the SLAC and control its operation using the Serial I/O Interface (see Figure 9). Additionally, data programmed previously may be read out for verification. The control word format is shown in Table 1. Commands are provided to:

- Set active/inactive modes
- Set up test functions
- Set up operating functions
- Program filter coefficients
- Assign time slots and port selection

- Write to the SLIC latch
- Enable/Disable each user-programmable filter

The interface consists of 4 pins, $\overline{CS}$, DCLK, D$_{IN}$ and D$_{OUT}$. The device is accessed by $\overline{CS}$ and data is serially loaded-in on D$_{IN}$ or read-out on D$_{OUT}$ under control of DCLK. Either commands or data words may be written to the SLAC, but only data words can be read out. All words are 8-bits wide and are written or read MSB first (see Figure 10).

For both reception or transmission of words, exactly 8 Data Clock cycles must be received after $\overline{CS}$ goes Low. $\overline{CS}$ must stay High (off period) for a minimum time pe-

riod before it can go Low again. During this off-period, the logic decodes and executes the command. All reading of data must be preceded by an input command requesting the data. Once control data transmission has begun, no new input commands will be accepted until control data transmission is completed.

A Serial I/O cycle is defined by transitions of $\overline{CS}$ and DCLK. Upon proper application of power supplies and MCLK, the device expects the first word to be a command. A number of commands require additional data words to be input or output. The SLAC will not accept new commands until all this data has been transferred.

There are two possible operations of DCLK and $\overline{CS}$ for the SLAC to function correctly. If the $\overline{CS}$ is held in the High state between accesses, the DCLK may free run

with no change to the internal control data. Using this method, the same DCLK may be run to a number of SLACs and individual $\overline{CS}$ lines will select the appropriate device to access. If the DCLK is held in the Low state between accesses, the $\overline{CS}$ line may make multiple transitions between accesses for a particular SLAC. This allows running one $\overline{CS}$ line to all SLACs and selecting a particular device through enabling or disabling its DCLK.

It should be noted that the DCLK can stay in the Low state indefinitely with no loss of internal control information. However, it should not be held in the High state for more than 20 μs to ensure proper operation as indicated by the Switching Characteristics Table.
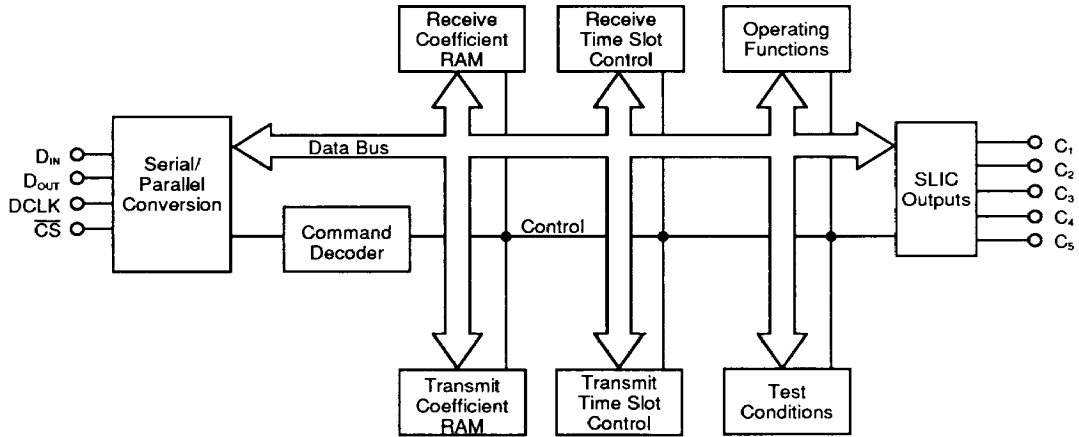
01520–11

Figure 9. Serial I/O Interface

01520–12

Figure 10. Serial I/O Interface Timing Diagram

Table 1: Control Word Summary

The Serial I/O Interface consists of Data Input, Data Output, Data Clock and $\overline{CS}$ Input. Data is read in (read out) on the Serial Data Input (output). The Serial Input consists of 8-bit (byte) command words which may be followed with additional bytes of input data or may be followed by the SLAC outputting bytes of data. All words are input with MSB (D_7) first and LSB (D_0) last. All out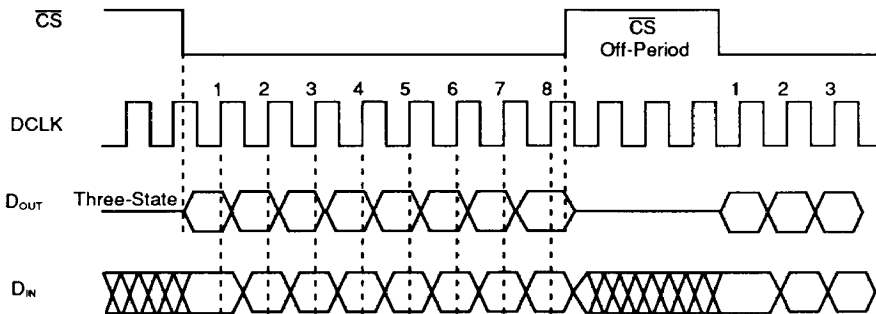puts are output with the MSB (D_7) first and the LSB (D_0) last. Words are written or read one at a time, with $\overline{CS}$ going High for at least the minimum off-period (see under Switching Characteristics) before the next read or write operation. The first 3 bits of the command word indicate the type of command and the last 5 bits contain either data or further information about the command. The classes of command are:

D_7	D_6	D_5	
0	0	0	Inactivate/No Operation
0	0	1	Transmit Time Slot Selection
0	1	0	Receive Time Slot Selection
0	1	1	Clock Slot and Gain Selection Read Slot, Gain and PCM Mode
1	0	0	Set Basic and Operating Functions and PCM Modes
1	0	1	Read/Write Coefficients, Set Test Modes, Select μ-law/A-law/linear
1	1	0	Data for SLIC Interface
1	1	1	Activate/No Operation

MSB	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	LSB	
	0	0	0	0	0	0	0	0	Inactivate	
	0	0	1	T	T	T	T	T	Transmit Time Slot Selection	Choose 1 of 32 Time Slots
	0	1	0	T	T	T	T	T	Receive Time Slot Selection	Choose 1 of 32 Time Slots
	0	1	1	0	0	C	C	C	Transmit Clock Slot Selection	Choose 1 of 8 Clock Slots
	0	1	1	0	1	C	C	C	Receive Clock Slot Selection	Choose 1 of 8 Clock Slots
	0	1	1	1	0	0	1	0	Transmit Gain Selection (GX)	Followed by 2 Bytes of Data
	0	1	1	1	1	0	1	0	Receive Gain Selection (GR)	Followed by 2 Bytes of Data
	0	1	1	1	0	1	0	1	Read Transmit Time and Clock Slot	Followed by 1 Byte of Data
	0	1	1	1	0	0	0	1	Read Transmit Gain (GX)	Followed by 2 Bytes of Data
	0	1	1	1	1	1	0	1	Read Receive Time and Clock Slot	Followed by 1 Byte of Data
	0	1	1	1	1	0	0	1	Read Receive Gain (GR)	Followed by 2 Bytes of Data
	0	1	1	1	0	1	1	1	Read PCM Mode	Followed by 1 Byte of Data
	1	0	0	0	B	X	R	Z	Enable Filters	
	1	0	0	1	D_R	D_x	R_{EX}	T_{EX}	PCM-Mode Selection	
	1	0	1	0	0	0	0	0	Write B Coefficients	Followed by 12 Bytes of Data
	1	0	1	0	0	1	0	0	Write X Coefficients	Followed by 8 Bytes of Data
	1	0	1	0	1	0	0	0	Write R Coefficients	Followed by 8 Bytes of Data
	1	0	1	0	1	1	0	0	Write Z Coefficients	Followed by 8 Bytes of Data
	1	0	1	0	0	0	1	1	Read B Coefficients	Followed by 12 Bytes of Data
	1	0	1	0	0	1	1	1	Read X Coefficients	Followed by 8 Bytes of Data
	1	0	1	0	1	0	1	1	Read R Coefficients	Followed by 8 Bytes of Data
	1	0	1	0	1	1	1	1	Read Z Coefficients	Followed by 8 Bytes of Data
	1	0	1	1	0	0	0	0	Reset to normal conditions	
	1	0	1	1	0	0	0	1	Add –6 dB to receive gain	
	1	0	1	1	0	0	1	0	Cutoff receive path	
	1	0	1	1	0	1	1	1	Test mode–analog loop-back	
	1	0	1	1	0	1	0	0	Test mode–digital loop-back	
	1	0	1	1	0	0	1	1	Disable High-Pass Filter (set to 1) and freeze auto zero circuit	
	1	0	1	1	1	0	0	B	Choose PCM Code	
	1	1	0	C	C	C	C	C	Outputs to SLIC	
	1	1	1	1	1	1	1	1	Activate	

Am7901B/C Detailed Serial Command Definitions

Inactivate (Standby Mode)

MSB							LSB
0	0	0	0	0	0	0	0

In the inactive mode, none of the programmed information is changed and the analog output is set to zero volts through a moderate series impedance. The Serial I/O remains active, the SLIC control outputs remain valid, and the PCM outputs are high impedance.

Activate (Operational mode)

MSB							LSB
1	1	1	1	1	1	1	1

Valid PCM data is not transmitted until after the second FSX pulse is received following the execution of the Activate command.

Transmit Time Slot Selection

MSB							LSB
0	0	1	T_4	T_3	T_2	T_1	T_0

Bits T_4 through T_0 select one of 32 time slots.

Transmit Clock Slot Selection

MSB							LSB
0	1	1	0	0	C_2	C_1	C_0

Bits C_2 through C_0 select one of eight clock slot offsets within the time slot.

Read Transmit Time and Clock Slots

Command

MSB							LSB
0	1	1	1	0	1	0	1

Output Data

T_4	T_3	T_2	T_1	T_0	C_2	C_1	C_0	Byte 1

The transmit time and clock slots are read out time slot first, followed by clock slot.

Receive Time Slot Selection

MSB							LSB
0	1	0	T_4	T_3	T_2	T_1	T_0

Bits T_4 through T_0 select one of 32 time slots.

Receive Clock Slot Selection

MSB							LSB
0	1	1	0	1	C_2	C_1	C_0

Bits C_2 through C_0 select one of eight clock slot offsets within the time slot.

Read Receive Time and Clock Slots

Command

MSB							LSB
0	1	1	1	1	1	0	1

Output Data

T_4	T_3	T_2	T_1	T_0	C_2	C_1	C_0	Byte 1

The receive time and clock slots are read out time slot first, followed by clock slot.

Write GX Filter Coefficients

Command

MSB							LSB
0	1	1	1	0	0	1	0

Input Data

C_{40} m_{40}		C_{30} m_{30}	Byte 1
C_{20} m_{20}		C_{10} m_{10}	Byte 2

Read GX Filter Coefficients

Command

MSB							LSB
0	1	1	1	0	0	0	1

Output Data

C_{40} m_{40}		C_{30} m_{30}	Byte 1
C_{20} m_{20}		C_{10} m_{10}	Byte 2

Write GR Filter Coefficients

Command

MSB   LSB

0	1	1	1	1	0	1	0

Input Data

C_{40} m_{40}	C_{30} m_{30}	Byte 1
C_{20} m_{20}	C_{10} m_{10}	Byte 2

Read GR Filter Coefficients

Command

MSB   LSB

0	1	1	1	1	0	0	1

Output Data

C_{40} m_{40}	C_{30} m_{30}	Byte 1
C_{20} m_{20}	C_{10} m_{10}	Byte 2

Write PCM Mode Selection

MSB   LSB

1	0	0	1	D_R	D_X	R_{EX}	T_{EX}

Receive Port: $D_R = 0$: PCM data is input on DRA.
                       $D_R = 1$: PCM data is input on DRB.

Transmit Port: $D_X = 0$: PCM data is output on DXA.
                       $D_X = 1$: PCM data is output on DXB.

Receive $R_{EX} = 0$: Reset Receive Expanded Mode.
Expanded Mode: $R_{EX} = 1$: Set Receive Expanded Mode.

Transmit $T_{EX} = 0$: Reset Transmit Expanded Mode.
Expanded Mode: $T_{EX} = 1$: Set Transmit Expanded Mode.

Read PCM Mode Selection

Command

MSB   LSB

0	1	1	1	0	1	1	1

Output Data

1	1	1	1	D_R	D_X	R_{EX}	T_{EX}

Enable Filters

MSB   LSB

1	0	0	0	EB	EX	ER	EZ

B Filter: EB = 0: B filter disabled.
               EB = 1: B filter enabled.
X Filter: EX = 0: X filter disabled.
               EX = 1: X filter enabled.
R Filter: ER = 0: R filter disabled.
               ER = 1: R filter enabled.
Z Filter: EZ = 0: Z filter disabled.
               EZ = 1: Z filter enabled.

Write Test Mode Selection

MSB   LSB

1	0	1	1	0	T_3	T_2	T_1

T3	T2	T1	Function
0	0	0	Reset to normal conditions as follows. Receive gain is set to the value stored in the GR register. Analog and digital loopback modes are reset. The high-pass filter is enabled and the auto-zero circuit is operational. The receive path is not cutoff.
0	0	1	Add –6 dB to receive gain.
0	1	0	Cutoff receive path.
0	1	1	Disable high-pass filter (set to 1) and freeze auto-zero circuit.
1	0	0	Activate digital loopback.
1	1	1	Activate analog loopback.

Select PCM Coding

MSB   LSB

1	0	1	1	1	0	0	B

Bit B selects the type of PCM code to be used.

For the Am7901B: B = 0: A-law.
                        B = 1: μ-law.

For the Am7901C: B = 0: Linear.
                        B = 1: A-law.

Write SLIC Output Registers

MSB   LSB

1	1	0	C_5	C_4	C_3	C_2	C_1

Write B Filter Coefficients

Command

MSB   LSB

1	0	1	0	0	0	0	0

Input Data

C_{30}	m_{30}	C_{20}	m_{20}	Byte 1
C_{10}	m_{10}	C_{31}	m_{31}	Byte 2
C_{21}	m_{21}	C_{11}	m_{11}	Byte 3
C_{32}	m_{32}	C_{22}	m_{22}	Byte 4
C_{12}	m_{12}	C_{33}	m_{33}	Byte 5
C_{23}	m_{23}	C_{13}	m_{13}	Byte 6
C_{34}	m_{34}	C_{24}	m_{24}	Byte 7
C_{14}	m_{14}	C_{35}	m_{35}	Byte 8
C_{25}	m_{25}	C_{15}	m_{15}	Byte 9
C_{36}	m_{36}	C_{26}	m_{26}	Byte 10
C_{16}	m_{16}	C_{37}	m_{37}	Byte 11
C_{27}	m_{27}	C_{17}	m_{17}	Byte 12

Read B Filter Coefficients

Command

MSB   LSB

1	0	1	0	0	0	1	1

Output Data

C_{30}	m_{30}	C_{20}	m_{20}	Byte 1
C_{27}	m_{27}	C_{17}	m_{17}	Byte 12

Write X Filter Coefficients

Command

MSB   LSB

1	0	1	0	0	1	0	0

Input Data

C_{40}	m_{40}	C_{30}	m_{30}	Byte 1
C_{20}	m_{20}	C_{10}	m_{10}	Byte 2
C_{41}	m_{41}	C_{31}	m_{31}	Byte 3
C_{21}	m_{21}	C_{11}	m_{11}	Byte 4
C_{42}	m_{42}	C_{32}	m_{32}	Byte 5
C_{22}	m_{22}	C_{12}	m_{12}	Byte 6
C_{43}	m_{43}	C_{33}	m_{33}	Byte 7
C_{23}	m_{23}	C_{13}	m_{13}	Byte 8

Read X Filter Coefficients

Command

MSB   LSB

1	0	1	0	0	1	1	1

Output Data

C_{40}	m_{40}	C_{30}	m_{30}	Byte 1
C_{23}	m_{23}	C_{13}	m_{13}	Byte 8

Write R Filter Coefficients

Command

MSB   LSB

1	0	1	0	1	0	0	0

Input Data

C_{43}	m_{43}	C_{33}	m_{33}	Byte 1
C_{23}	m_{23}	C_{13}	m_{13}	Byte 2
C_{42}	m_{42}	C_{32}	m_{32}	Byte 3
C_{22}	m_{22}	C_{12}	m_{12}	Byte 4
C_{41}	m_{41}	C_{31}	m_{31}	Byte 5
C_{21}	m_{21}	C_{11}	m_{11}	Byte 6
C_{40}	m_{40}	C_{30}	m_{30}	Byte 7
C_{20}	m_{20}	C_{10}	m_{10}	Byte 8

Read R Filter Coefficients

Command

MSB							LSB
1	0	1	0	1	0	1	1

Output Data

C_{43} m_{43}	C_{33} m_{33}	Byte 1
C_{20} m_{20}	C_{10} m_{10}	Byte 8

Read Z Filter Coefficients

Command

MSB							LSB
1	0	1	0	1	1	1	1

Output Data

C_{43} m_{43}	C_{33} m_{33}	Byte 1
C_{20} m_{20}	C_{10} m_{10}	Byte 8

Write Z Filter Coefficients

Command

MSB							LSB
1	0	1	0	1	1	0	0

Input Data

C_{43} m_{43}	C_{33} m_{33}	Byte 1
C_{23} m_{23}	C_{13} m_{13}	Byte 2
C_{42} m_{42}	C_{32} m_{32}	Byte 3
C_{22} m_{22}	C_{12} m_{12}	Byte 4
C_{41} m_{41}	C_{31} m_{31}	Byte 5
C_{21} m_{21}	C_{11} m_{11}	Byte 6
C_{40} m_{40}	C_{30} m_{30}	Byte 7
C_{20} m_{20}	C_{10} m_{10}	Byte 8

Digital Filters

The SLAC uses digital signal processing to implement the various filters (see Figure 11).

The advantages of digital filters are:

- High reliability
- No drift with time or temperature
- Unit-to-unit repeatability
- Superior transmission performance

Six of the digital filters in the signal processing sections are user-programmable. These allow the user to independently modify the gain in both the transmit and receive paths, provide trans-hybrid balancing in the system, and adjust the two-wire line termination impedance. This programming capability feature allows the user to optimize the performance of the SLAC for his system.

General Description of CSD Coefficients

The filter functions are performed by a series of multiplications and accumulations. A multiplication is accomplished by repeatedly shifting the multiplicand and summing the result with the previous value at that summation node. The method used in the SLAC is known as Canonic Signed Digit (CSD) multiplication and splits each coefficient into a series of CSD coefficients.

Each programmable filter section has the following general transfer function:

$$HF(z) = h_0 + h_1 z^{-1} + h_2 z^{-2} + \ldots + h_n z^{-n} \tag{1}$$

where the number of taps in the filter = $n + 1$.

The values of the user-defined coefficients (h_i) are assigned via the MPI. Each of the coefficients (h_i) is defined in the following general equation:

$$h_i = B_1 2^{-M_1} + B_2 2^{-M_2} + \ldots + B_N 2^{-M_N}, \tag{2}$$

where:

the number of shifts = $M_i \leq M_{i+1}$

sign = $B_i = \pm 1$

N = Number of CSD coefficients.

The value of h_i in (2) represents a decimal number which is broken down into a sum of successive values of:

± 1.0 multiplied by 2^{-0}, or 2^{-1}, or $2^{-2} \ldots 2^{-7} \ldots$

or

± 1.0 multiplied by 1, or 1/2, or 1/4 $\ldots$ 1/128 $\ldots$

The limit on the negative powers of 2 is determined by the length of the registers in the ALU.

The coefficient h_i in Equation 2 can be considered to be a value made up of N binary 1s in a binary register where the leftmost part represents whole numbers, the rightmost part represents decimal fractions, and a decimal point separates them. The first binary 1 is shifted M_1 bits to the right of the decimal point, the second binary 1 is
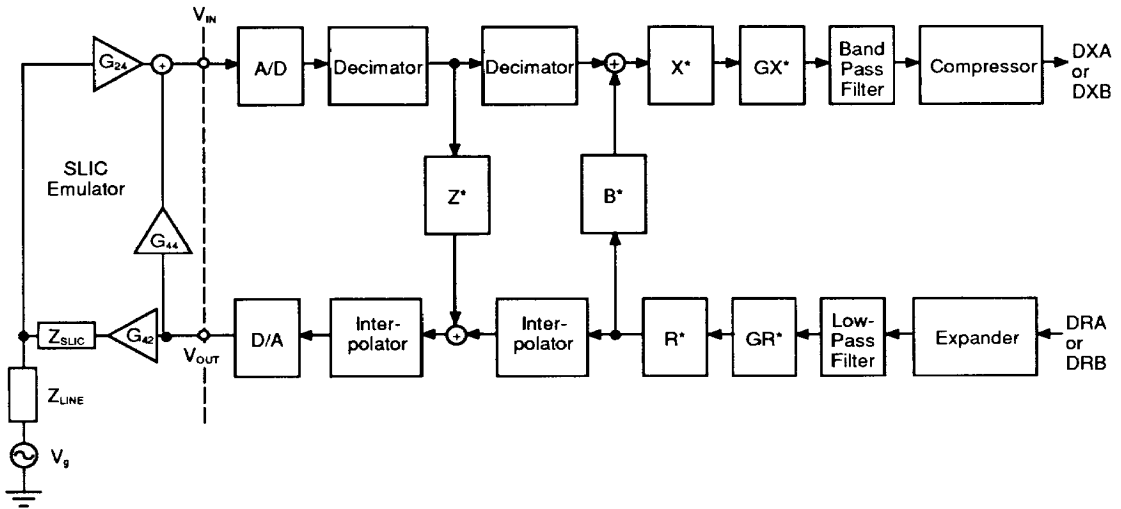
*User-Programmable Filters

Figure 11. SLAC Signal Processing Flow   01520–13

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shifted M_2 bits to the right of the decimal point, the third binary 1 is shifted M_3 bits to the right of the decimal point, and so on.

Note that when M_1 is 0, the resulting value is a binary 1 in front of the decimal point, that is, no shift. If M_2 is also 0, the result is another binary 1 in front of the decimal point, giving a total value of binary 10 in front of the decimal point (i.e., a decimal value of 2.0). The value of N, therefore, determines the range of values the coefficient h_i can take; for example, if N = 3 the maximum and minimum values are ±3, and if N = 4 the values are between ±4.

Detailed Description of SLAC Coefficients

The CSD coding scheme in the SLAC uses a value called m_i, where m_1 represents the distance shifted right of the decimal point for the first binary 1, m_2 represents the distance shifted to the right of the *previous* binary 1, and m_3 represents the number of shifts to the right of the second binary 1. Note that the range of values determined by N is unchanged. Equation 2 is now modified (in the case of N = 4) to:

$$h_i = B_1 2^{-M_1} + B_2 2^{-M_2} + B_3 2^{-M_3} + B_4 2^{-M_4} \qquad (3)$$

$$h_i = C_1 2^{-m_1} + C_1 C_2 2^{-(m_1 + m_2)} + C_1 C_2 C_3 2^{-(m_1 + m_2 + m_3)}$$
$$+ C_1 C_2 C_3 C_4 2^{-(m_1 + m_2 + m_3 + m_4)} \qquad (4)$$

$$h_i = C_1 2^{-m_1} \cdot [1 + C_2 2^{-m_2} \cdot \{1 + C_3 2^{-m_3} \cdot (1 + C_4 2^{-m_4})\}] \qquad (5)$$

where:

$M_1 = m_1$	and	$B_1 = C_1$
$M_2 = m_1 + m_2$		$B_2 = C_1 \cdot C_2$
$M_3 = m_1 + m_2 + m_3$		$B_3 = C_1 \cdot C_2 \cdot C_3$
$M_4 = m_1 + m_2 + m_3 + m_4$		$B_4 = C_1 \cdot C_2 \cdot C_3 \cdot C_4$

In the SLAC, a coefficient h_i consists of N CSD coefficients, each being made up of 4 bits and formatted as $C_{xy}m_{xy}$, where C_{xy} is one bit (MSB) and m_{xy} is three bits. Each CSD coefficient is broken down as follows:

C_{xy} is the sign bit (0 = positive, 1 = negative).

m_{xy} is the 3-bit shift code. It is encoded as a binary number as follows:

000:	illegal
001:	6 shifts
010:	5 shifts
011:	4 shifts
100:	3 shifts
101:	2 shifts
110:	1 shift
111:	0 shifts

y   is the coefficient number (the i in h_i).

x   is the position of this CSD coefficient within the h_i coefficient. It represents the relative position of the binary 1 represented by this CSD coefficient within the h_i coefficient. The most significant binary 1 is represented by x = 1. The next most significant binary 1 is represented by x = 2, and so on.

Thus, $C_{13}m_{13}$ represents the sign and the relative shift position for the first (most significant) binary 1 in the 4th (h_3) coefficient.

The number of CSD coefficients, N, is limited to 4 in the GR, GX, R, X, and Z filters, and 3 for the B filter. Note also that the GX filter coefficient equation is slightly different from that of the other filters:

$$h_{iGX} = 1 + h_i \qquad (6)$$

Please refer to the section detailing the commands for complete details on the programming of the coefficients.

Two-Wire Impedance Matching

A feedback path is provided from the transmit to the receive section via the Z filter. This filter may be programmed to modify the effective termination impedance (Z_{SLIC}) of a SLIC or a transformer hybrid to a desired value. The desired impedance may be complex. This feature allows the user to terminate each SLIC in a Subscriber Line System with a fixed resistor and digitally modify their impedance using the Z filter.

The X and R filters are the Transmit and Receive attenuation distortion correction filters. These filter sections are programmed to compensate the attenuation distortion caused by the Z filter.

Trans-Hybrid Balance

In a traditional line card system, a balance network is used with the SLIC to achieve trans-hybrid balancing. If the balance network perfectly matches the subscriber's line, infinite trans-hybrid balancing is achieved. But in general, the matching in traditional systems is poor and trans-hybrid balancing is not very good. Some systems have up to 2 or 3 compromise networks per line that must be selected semi-automatically or manually to provide the balance.

In the SLAC, a feedback path is provided from the receive to the transmit section via the B filter. This filter may be programmed to cancel the received signal from the transmit signal path and achieve a significantly improved level of trans-hybrid balance.

Gain Adjustment

Signal levels in the transmit and receive paths may be modified by programming the GX and GR filters. The GX filter allows the user to add up to 12 dB of gain with an accuracy of 0.051 dB up to 10.4 dB and ±0.15 dB up to 12 dB in the transmit path. The GR filter allows the user to add up to 12 dB of loss with an accuracy of ±0.051 dB in the receive path.

Test Features

The SLAC simplifies system testing by providing both digital and analog loop-back paths. Under program control, either the DRA or DRB input is looped to the DXA or

DXB output (digital loop-back) through a path from the output of the interpolator in the receive path to the input of the decimator in the transmit path, or the V_{IN} input is looped to the V_{OUT} output (analog loop-back) through the Z filter. To allow testing of the subscriber loop cabling for leakage, the transmit high pass filter may be disabled and auto-zero operation interrupted. The receive analog output may be programmed to cut off. This receive cut-off command may be used to stop oscillations in the four-wire side of the telephone network.

The SLAC contains an auto-zero circuit in the A/D converter which takes several seconds to settle following a change in the offset voltage at V_{IN}. To facilitate component testing of the SLAC, there is a test mode available to accelerate settling of the auto-zero circuit. This test mode is activated by holding the CS input at -5 V for at least 64 ms with the offset voltage applied to V_{IN} (and no signal). The auto-zero will settle in this time. In a component test environment, this procedure should be followed after programming the filters. The C_S output is also used in this mode. The output level on C_S may be modified.

Note: The digital loopback (DLB) path processes an internal data word 2-bits shorter than in normal mode. Therefore, DLB signal processing performance is not equivalent to normal mode signal processing and does not meet the specified Transmission specifications. DLB is recommended for use with 0-dB programmed gain/attenuation and PCM signal levels above -25 dBm0.

Stand-By Mode

The SLAC is forced into the stand-by mode either by a hardware reset applied to the DCLK input or by reception of the Inactivate command. In this mode, power is switched off from all circuitry that can be turned off. No transmission or reception of PCM data takes place. However, the circuits which contain programmed information retain their data. The Serial I/O Interface remains active to receive new commands.

Power-On Clear

Before any other commands are written to the SLAC, 13 Inactivate commands should be sent to the serial port of the SLAC in case the SLAC powers up in the middle of a read sequence. Alternatively, a hardware reset operation can be carried out by applying -5 V to the DCLK pin. A loss of MCLK should be treated like a loss of power.

Stand-Alone Mode

In the stand-alone mode, the serial interface is not used. The DCLK and D_{IN} pins may be used to control the device. Applying -5 V to the DCLK pin resets the device and the D_{IN} pin can subsequently be used to power-up or power-down the SLAC.

DCLK	D_{IN}	
0	X	Normal Mode
1	X	Normal Mode
-5 V	0	Reset and Power-Down
-5 V	1	Reset and Power-Up

Reset State

The Reset State of the device is:

a. Both Transmit and Receive Time and Clock Slots are set to 0.

b. A-law is selected.

c. B, X, R, Z filters are disabled.

d. Both Transmit (GX) and Receive (RX) gains are set to unity.

e. SLIC outputs are set High.

f. Normal conditions are selected.

g. DXA/DRA ports are selected.

μ-Law: Positive Input Values

1	2	3	4	5	6		7	8
Segment Number	Number of Intervals X Interval Size	Value at Segment End Points	Decision Value Number n	Decision Value x_n (1)	Character Signal (5) Bit Number 1 2 3 4 5 6 7 8		Value at Decoder Output y_n (3)	Decoder Output Value Number
		8159	(128)	(8159)	- - - - - - - - - - -			
					1 0 0 0 0 0 0 0		8031	127
8	16×256		127	7903			⋮	⋮
			⋮	⋮	(2)			
			113	4319				
		4063			1 0 0 0 1 1 1 1		4191	112
			112	4063				
7	16×128		⋮	⋮	(2)		⋮	⋮
			97	2143				
		2015			1 0 0 1 1 1 1 1		2079	96
			96	2015				
6	16×64		⋮	⋮	(2)		⋮	⋮
			81	1055				
		991			1 0 1 0 1 1 1 1		1023	80
			80	991				
5	16×32		⋮	⋮	(2)		⋮	⋮
			65	511				
		479			1 0 1 1 1 1 1 1		495	64
			64	479				
4	16×16		⋮	⋮	(2)		⋮	⋮
			49	239				
		223			1 1 0 0 1 1 1 1		231	48
			48	223				
3	16×8		⋮	⋮	(2)		⋮	⋮
			33	103				
		95			1 1 0 1 1 1 1 1		99	32
			32	95				
2	16×4		⋮	⋮	(2)		⋮	⋮
			17	35				
		31			1 1 1 0 1 1 1 1		33	16
			16	31				
1			⋮	⋮	(2)		⋮	⋮
	15×2		2	3				
					1 1 1 1 1 1 1 0		2	1
	1×1		1	1	1 1 1 1 1 1 1 1			
			0	0			0	0

Notes:
1. 8159 normalized value units correspond to $T_{MAX} = 3.17$ dBm0.
2. The character signal corresponding to positive input values between two successive decision values numbered n and n + 1 (see column 4) is (255 − n) expressed as a binary number.
3. The value at the decoder is $y_0 = x_0 = 0$ for $n = 0$, and $y_n = \frac{x_n + x_n + 1}{2}$ for $n = 1, 2, \ldots, 127$.
4. x_{128} is a virtual decision value.
5. Bit 1 is a 0 for negative input values.

A-Law, Positive Input Values

1	2	3	4	5	6		7	8
Segment Number	Number of Intervals X Interval Size	Value at Segment End Points	Decision Value Number n	Decision Value x_n (1)	Character Signal Before Inversion of the Even Bits		Value at Decoder Output y_n (3)	Decoder Output Value Number
					Bit Number 1 2 3 4 5 6 7 8			
		4096	(128)	(4096)	– – – – – – – – – –			
					1 1 1 1 1 1 1 1		4032	128
7	16×128		127	3968				
			⋮	⋮		(2)	⋮	⋮
			113	2176				
		2048			1 1 1 1 0 0 0 0		2112	113
			112	2048				
6	16×64		⋮	⋮		(2)	⋮	⋮
			97	1086				
		1024			1 1 1 0 0 0 0 0		1056	97
			96	1024				
5	16×32		⋮	⋮		(2)	⋮	⋮
			81	544				
		512			1 1 0 1 0 0 0 0		528	81
			80	512				
4	16×16		⋮	⋮		(2)	⋮	⋮
			65	272				
		256			1 1 0 0 0 0 0 0		264	65
			64	256				
3	16×8		⋮	⋮		(2)	⋮	⋮
			49	136				
		128			1 0 1 1 0 0 0 0		132	49
			48	128				
2	16×4		⋮	⋮		(2)	⋮	⋮
			33	68				
		64			1 0 1 0 0 0 0 0		66	33
			32	64				
1 ↓	32×2		⋮	⋮		(2)	⋮	⋮
			1	2				
					1 0 0 0 0 0 0 0		1	1
			0	0				

Notes:
1. 4096 normalized value units correspond to $T_{MAX} = 3.14$ dBm0.

2. The character signals are obtained by inverting the even bits of the signals of column 6. Before this inversion, the character signal corresponding to positive input values between two successive decision values numbered n and $n+1$ (see column 4) is $(128+n)$ expressed as a binary number.

3. The value at the decoder output is $y_n = \dfrac{x_{n-1} + x_n}{2}$ for $n = 1, \ldots, 127, 128$.

4. x_{128} is a virtual decision value.

5. Bit 1 is a 0 for negative input values.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... −60 to 125°C
Ambient Temperature under Bias .... 0 to 70°C
V_{CC} with respect to DGND .... −0.4 to +6.0 V
V_{BB} with respect to DGND .... +0.4 to −6.0 V
V_{IN} with respect to AGND .... V_{BB} to V_{CC}

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES
Commercial (C) Devices

Ambient Temperature (T_A) .... 0 to 70°C
V_{CC} .... +5.0 V ±5%
V_{BB} .... −5.0 V ±5%
DGND .... 0 V
AGND .... DGND ±100 mV

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range (Note 1) unless otherwise specified

Parameters	Description	Test Conditions	Min	Typ	Max	Units
Z_{IN}	Analog Input Impedance	−3.2 V < V_{IN} < 3.2 V	20			kΩ
Z_{OUT}	Analog Output Impedance	−3.2 V < V_{OUT} < 3.2 V			20	Ω
V_{IOS}	Offset Voltage Allowed on V_{IN}				±40	mV
V_{OOS}	Analog Output Offset Voltage				±30	mV
V_{IR}	Analog Input Voltage Range				±3.2 V	V
V_{OR}	Analog Output Voltage Range	R_L ≥ 10 kΩ, C_L ≤ 50 pF			±3.2 V	V
I_{OUT}	Analog Output Current		350			μA
V_{IL}	Input Low Voltage (All Digital Inputs Except DCLK in Stand Alone Mode and $\overline{CS}$ in Auto Zero Speedup Mode)		−0.5		0.8	V
V_{IH}	Input High Voltage (All Digital Inputs)		2.0		V_{CC}	V
V_{OL}	Output Low Voltage (All Digital Outputs)	I_{OL} = 2 mA			0.45	V
V_{OH}	Output High Voltage (All Outputs Except TSC)	I_{OH} = 400 μA	2.4			V
I_{OL}	Output Leakage Current				±10	μA
I_{IL}	Input Leakage Current				±1	μA
I_{IL} (V_{IN})	Input Leakage Current on V_{IN} Pin				±0.2	μA
I_{CC} (S)	V_{CC} Supply Current (Standby)				15	mA
I_{BB} (S)	V_{BB} Supply Current (Standby)	V_{CC} = 5.25 V			10	mA
I_{CC} (A)	V_{CC} Supply Current (Active)	V_{BB} = −4.75 V			60	mA
I_{BB} (A)	V_{BB} Supply Current (Active)				20	mA
PSRR	V_{CC} Power Supply Rejection Ratio	200 mV p-p @ 1.02 kHz on the appropriate supply, V_{CC} = +5 V, V_{BB} = −5 V	35			dB
PSRR	V_{BB} Power Supply Rejection Ratio		30			dB
C_I	Input Capacitance (Digital)			5		pF
C_O	Output Capacitance (Digital)			8		pF

Note: 1. Typical values are for T_A = 25°C and nominal supply voltages. Min and max specifications are over the temperature and supply voltage ranges shown in the above table entitled "Operating Ranges."

TRANSMISSION CHARACTERISTICS

(All specifications are guaranteed with 0 dB ≤ GX ≤ +12 dB, −12 dB ≤ GR ≤ 0 dB and A-law or μ-law companded PCM, unless otherwise specified.)

When GR = 0 dB, a 1020 Hz sine wave signal with level of 0 dBm0 at the digital input will correspond to an rms

voltage of 1.6 V for A-law and 1.588 V for μ-law at the analog output. When GX = 0 dB, a 1020-Hz sine wave signal with rms voltage of 1.569 V for A-law and 1.557 V for μ-law at the analog input will correspond to a level of 0 dBm0 at the digital output.

Description	Test Conditions	Min	Typ	Max	Units
Attenuation Distortion	1020 Hz at −10 dBm0		(see Fig. 12)		dB
Gain (either path) a. deviation from ideal value b. deviation from initial value	1020 Hz at −10 dBm0	−0.2 −0.2		+0.2 +0.2	dB dB
Group Delay Distortion (either path)	−10 dBm0 signal		(see Fig. 14)		
Harmonic Distortion	(Note 1)			−40	dB
Intermodulation Distortion	a. (Note 2) b. (Note 3)			−35 −49	dB dBm0
Crosstalk a. Go-to-Return Path b. Return-to-Go path	300–3400 Hz, 0 dBm0 300–3400 Hz, 0 dBm0		−90 −90	−70 −70	dB dB
Gain Tracking (either path)			(see Fig. 15, 17)		dB
Signal to Total Distortion (either path)			(see Fig. 16, 18, 19)		dB

μ-Law Companded PCM

Idle Channel Noise (weighted, transmit)				19	dBrnc0
Idle Channel Noise (weighted, receive)				15	dBrnc0

A-Law Companded PCM

Idle Channel Noise (weighted, transmit)				−68	dBm0p
Idle Channel Noise (weighted, receive)				−78	dBm0p

Notes: 1. Applied signal is a 0-dBm0 sine wave within 300 to 3400 Hz. The signal measured is any frequency in the range 300 to 3400 Hz.

2. Two different frequencies, f_1 and f_2, in the range 300–3400 Hz and of equal levels in the range −4 to −21 dBm0 are applied. $2f_1$–f_2 products are measured relative to the level of either f_1 or f_2.

3. Any intermodulation product due to a signal in the range 300–3400 Hz with input level −9 dBm0 and a 50-Hz signal with input level −23 dBm0.

Transmit Path Only
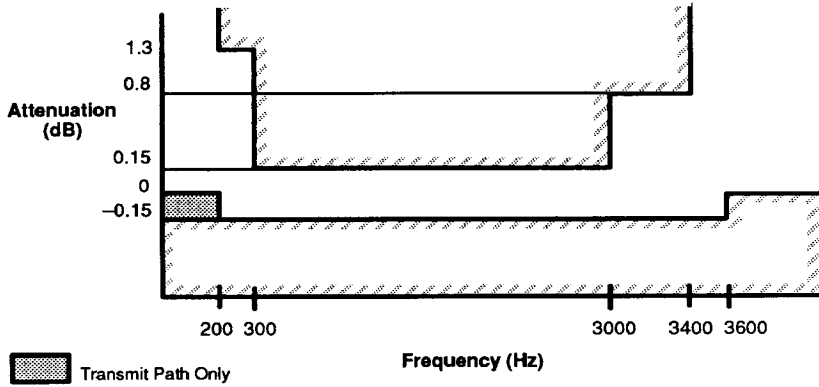
Note: Measured per CCITT Rec. G.714 Paragraph 7.

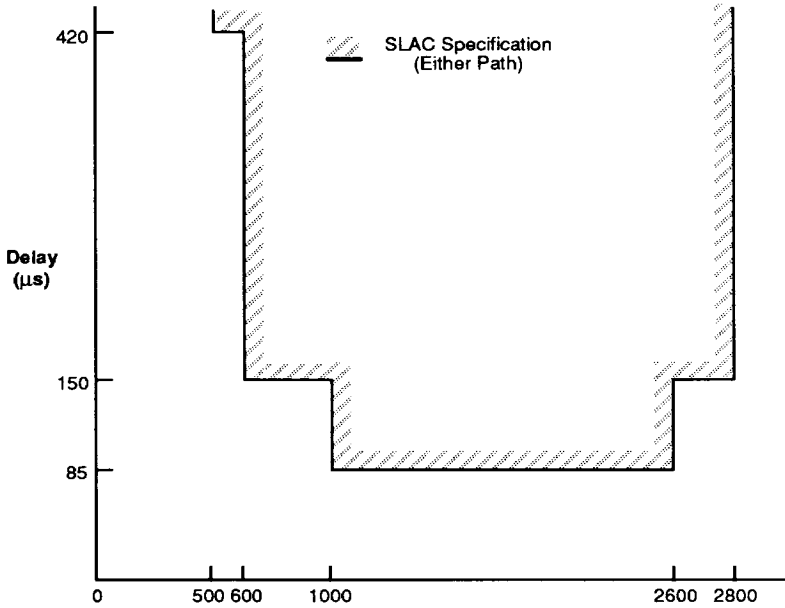**Figure 12. Attenuation Distortion Transmit or Receive Path**   01520–14
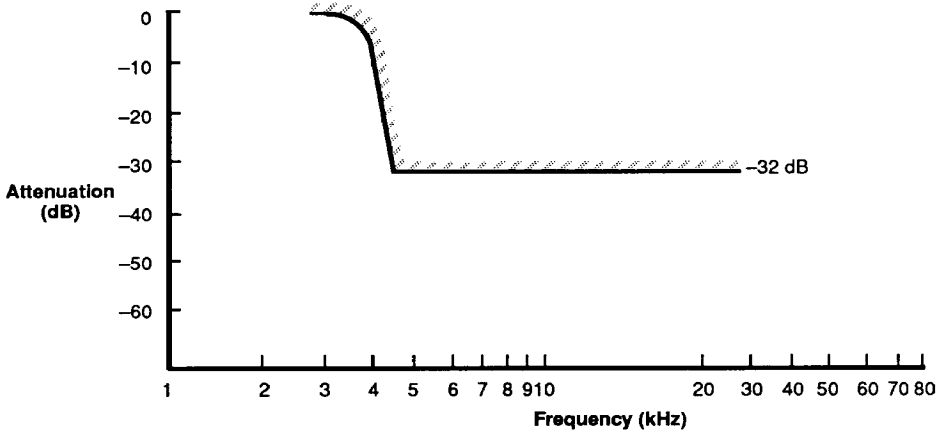
Notes: 1. The frequency is 1020 Hz.
2. Input signal level is 0 dBm0.

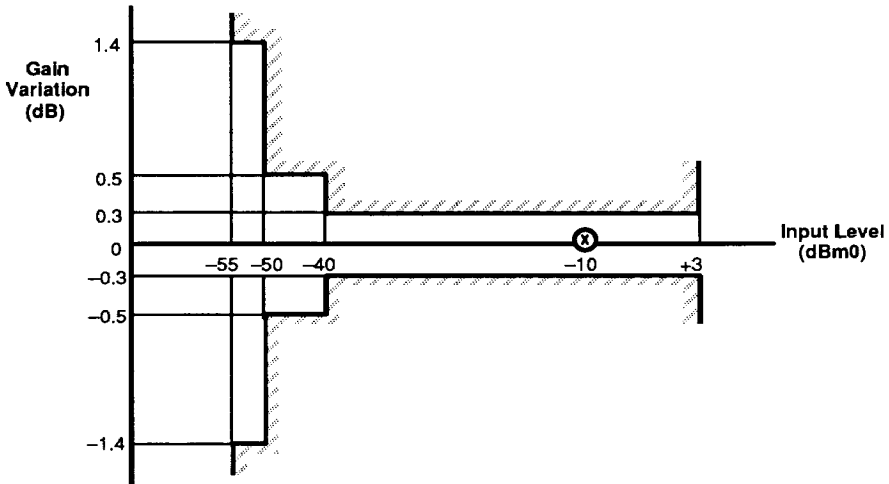**Figure 13. Out of Band Signals (End-to-End)**   01520–15

Note: Minimum value of group delay is taken as reference.

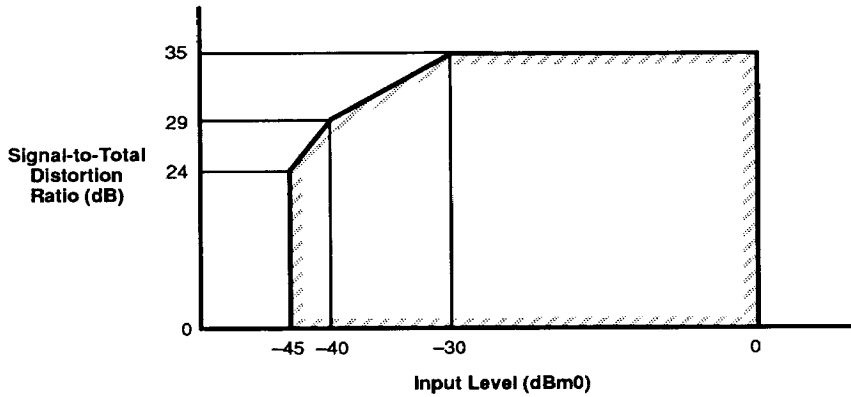**Figure 14. Group Delay Distortion (Either Path)**

01520-16

Note: Measured per CCITT Rec. G.714 Paragraph 15.

01520-17

Figure 15. Gain Tracking with Tone (Method 2) Transmit or Receive Path

Am7901B/C   **25**

Note: Measured per CCITT Rec. G.714 Paragraph 14.

01520–18

Figure 16. Signal-to-Total Distortion With Tone (Method 2) Transmit or Receive Path

a. Noise Test Signal
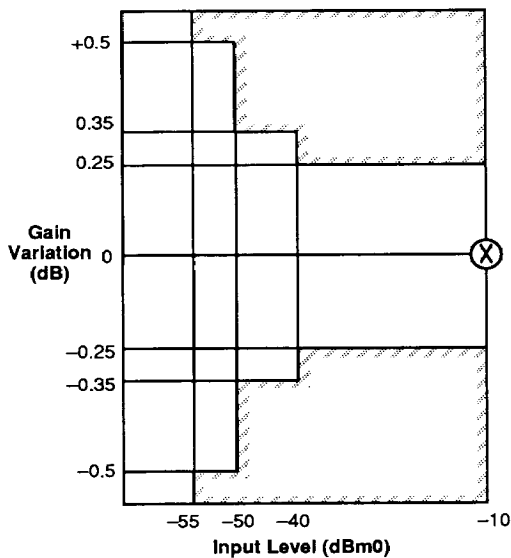
b. Sinusoidal Test Signal
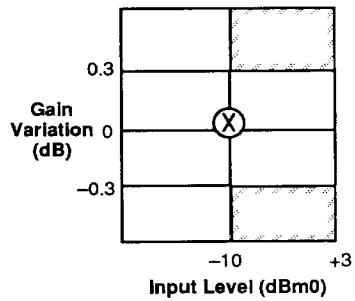
Note: Measured per CCITT Rec. G.714 Paragraph 15.

01520-19

Figure 17. Gain Tracking with Noise (Method 1) Transmit or Receive Path

Am7901B/C
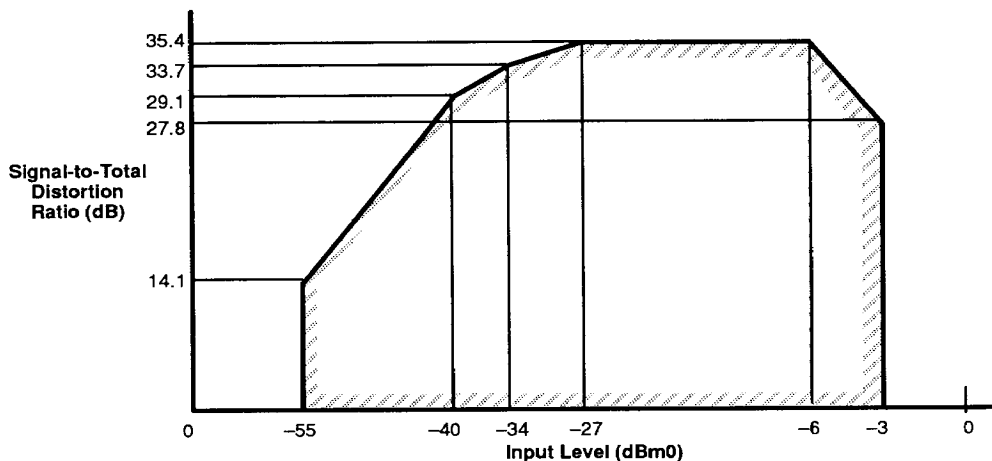
Note: Measured per CCITT Rec. G.714 Paragraph 14.   01520–20

Figure 18. Signal-to-Total Distortion With Noise (Receive Path—Method 1)
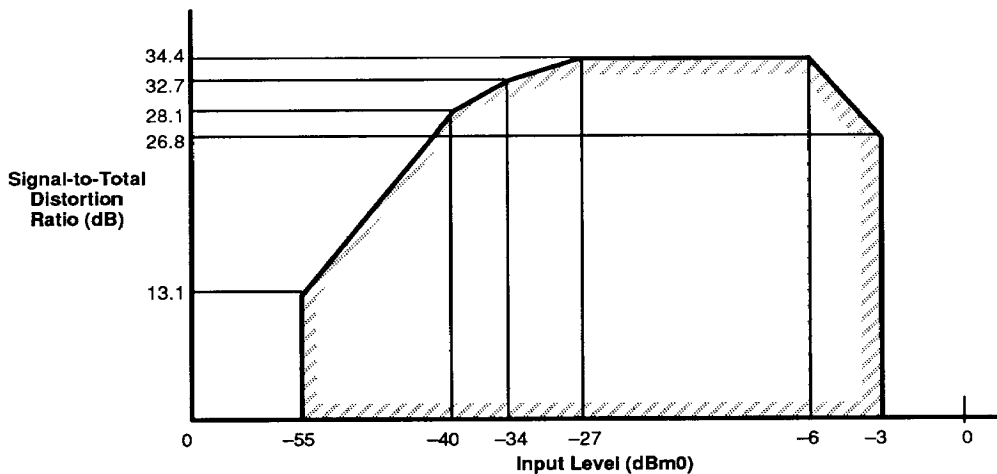
Note: Measured per CCITT Rec. G.714 Paragraph 1.   01520–21

Figure 19. Signal-to-Total Distortion With Noise (Transmit Path—Method 1)

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

$T_A = 0$ to $70°C$, $V_{CC} = +5\ V\ \pm5\%$, $V_{BB} = -5\ V\ \pm5\%$ (see Notes 1, 6 & 7)

No.	Parameter	Description	Min	Typ	Max	Units
Serial Interface Input Mode						
1	t_{DCH}	Data Clock High Pulse Width (Note 2)	0.220		20	µs
2	t_{DCL}	Data Clock Low Pulse Width (Note 2)	0.220			µs
3	t_{DCR}	Rise Time of Clock	5		50	ns
4	t_{DCF}	Fall Time of Clock	5		50	ns
5	t_{ICSS}	Chip Select Setup Time	175			ns
6	t_{ICSH}	Chip Select Hold Time	50			ns
7	t_{ICSL}	Chip Select Pulse Width (Notes 3 & 8)		$8\ t_{DCY}$		ns
8	t_{ICSO}	Chip Select Off Time after byte written to or before byte read from B, Z, X, R, GX or GR in Active mode: Otherwise:	$32\ t_{MCY}$ $7\ t_{MCY}$			
9	t_{IDS}	Input Data Setup Time	50			ns
10	t_{IDH}	Input Data Hold Time	30			ns
11	t_{OLH}	Output Latch Propagation Delay	0.75		2.1	µs
Serial Interface Output Mode						
12	t_{OCSS}	Chip Select Setup Time	150			ns
13	t_{OCSH}	Chip Select Hold Time	50			ns
14	t_{OCSL}	Chip Select Pulse Width (Notes 3 & 8)		$8\ t_{DCY}$		ns
15	t_{OCSO}	Chip Select Off Time after byte written to or before byte read from B, Z, X, R, GX or GR in Active mode: Otherwise:	$32\ t_{MCY}$ $7\ t_{MCY}$			
16	t_{ODD}	Output Data Turn on Delay			100	ns
17	t_{ODH}	Output Data Hold Time	30			ns
18	t_{ODOF}	Output Turn off Delay			100	ns
19	t_{ODC}	Output Data Valid	30		150	ns
PCM Interface						
20	t_{PCY}	PCM Clock Period (Note 4)	0.244		7.8	µs
21	t_{PCH}	PCM Clock High Pulse Width (Note 4)	110			ns
22	t_{PCL}	PCM Clock Low Pulse Width (Note 4)	110			ns
23	t_{PCF}	Fall Time of Clock	5		15	ns
24	t_{PCR}	Rise Time of Clock	5		15	ns
25	t_{FSS}	Frame Sync Setup Time	50		$(t_{PCY} - 30)$	ns
26	t_{FSH}	Frame Sync Hold Time (Companded Mode)	30		$(8\ t_{PCY} - 50)$	ns
		Frame Sync Hold Time (Linear Mode)	30		$(16\ t_{PCY} - 50)$	ns
27	t_{TSD}	Delay to TSC Valid (Note 5)	$(N\ t_{PCY} + 30)$		$(N\ t_{PCY} + 150)$	ns
28	t_{TSO}	Delay to TSC Off (High Impedance)	30			ns
29	t_{DXD}	PCM Data Output Delay	95		185	ns
30	t_{DXH}	PCM Data Output Hold Time	30		100	ns
31	t_{DXZ}	PCM Data Output Delay to High Z	45		90	ns
32	t_{DRS}	PCM Data Input Setup Time	50			ns
33	t_{DRH}	PCM Data Input Hold Time	30			ns

SWITCHING CHARACTERISTICS (continued)

Master Clock

34	t_{MCY}	Master Clock Period	488.23	488.28	488.33	ns
35	t_{MCH}	Master Clock High Pulse Width	220			ns
36	t_{MCL}	Master Clock Low Pulse Width	238			ns
37	t_{MCR}	Rise Time of Clock	5		15	ns
38	t_{MCF}	Fall Time of Clock	5		15	ns

Notes: 1. Min and Max values are valid on all digital outputs except C_5–C_1 with a 150-pF load. C_5–C_1 outputs are valid with a 30-pF load.

2. The Data Clock may be stopped in the Low state indefinitely without loss of information. Data will not be clocked in or out while the clock is in the Low state.

3. Chip Select Pulse Width is nominally 8 Data Clock Cycles with a minimum value of 7 Data Clock Cycles + t_{ICSH} + t_{ICSS} and a maximum value of 9 Data Clock Cycles – t_{ICSH} – t_{ICSS}.

4. The maximum allowed PCM clock frequency is 4.096 MHz. The actual PCM clock rate is dependent on the number of channels allocated within a frame. The minimum clock frequency is 128 kHz.

5. $\overline{TSC}$ is delayed from FS by a typical value of N t_{PCY}, where N is the value stored in the Time/Clock Slot register.

6. The Frame Sync pulses (FSX, FSR) repeat at an 8-kHz rate.

7. FSR, FSX, CLKR, CLKX, and MCLK all must be synchronized and exactly 256 cycles of MCLK must be guaranteed between Frame Syncs. All five clocks must not be interrupted to assure proper operation.
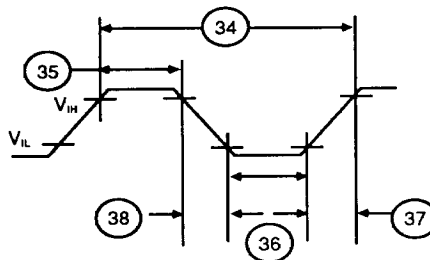
8. t_{DCY} is 1 Data Clock Cycle.
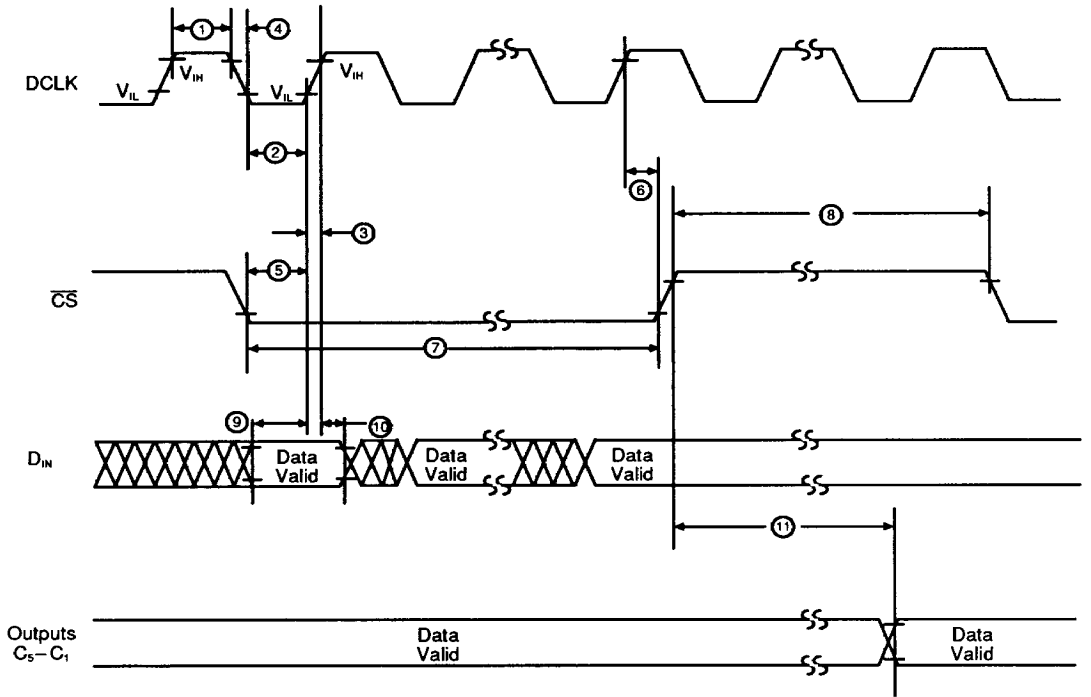
SWITCHING WAVEFORMS
Timing Diagrams

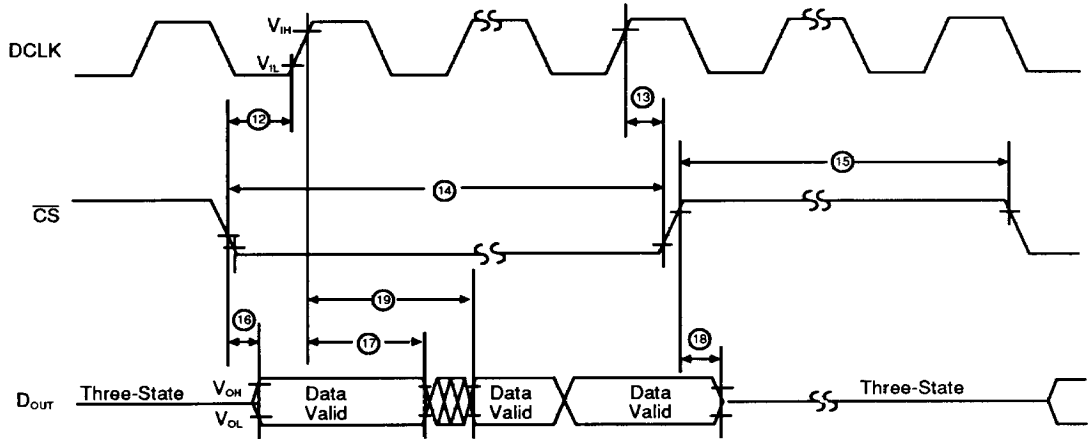**Input and Output Waveforms
For AC Tests**
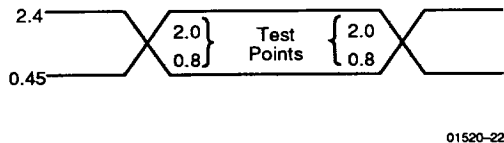
Master Clock Timing

01520–22

01520–23

Serial Interface (Input Mode)

01520-24

Serial Interface (Output Mode)

01520-25

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PCM Highway Timing

01520-26

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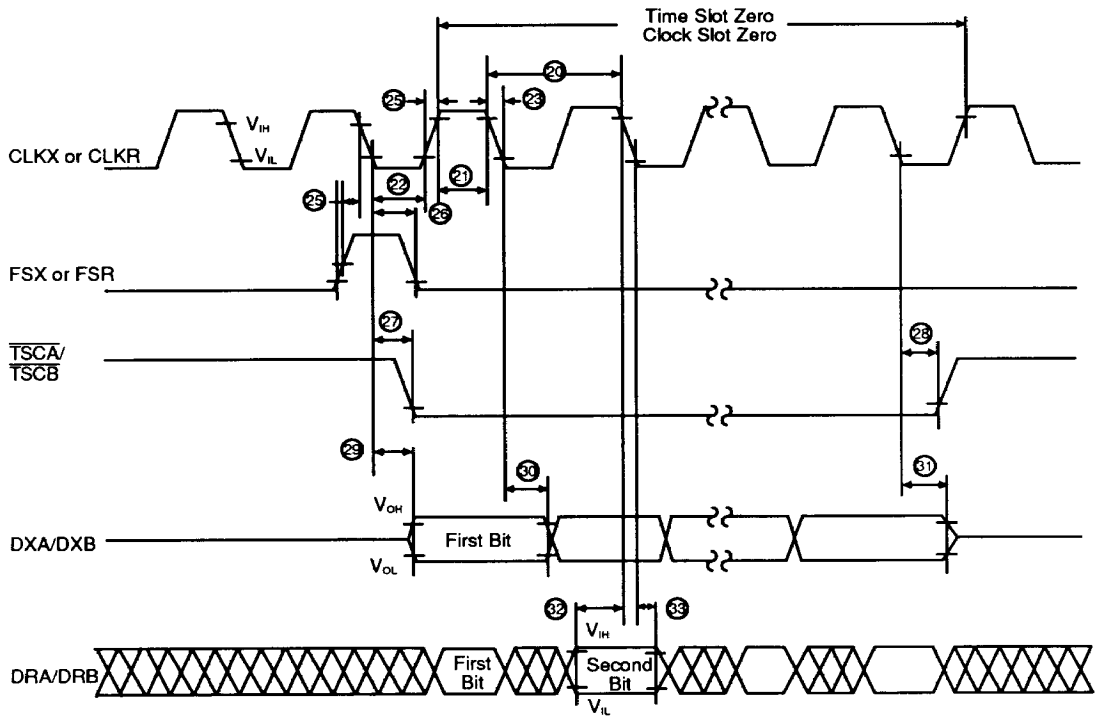
AMD 8-Channel Subscriber Line Card

01520-27

Am7901B/C
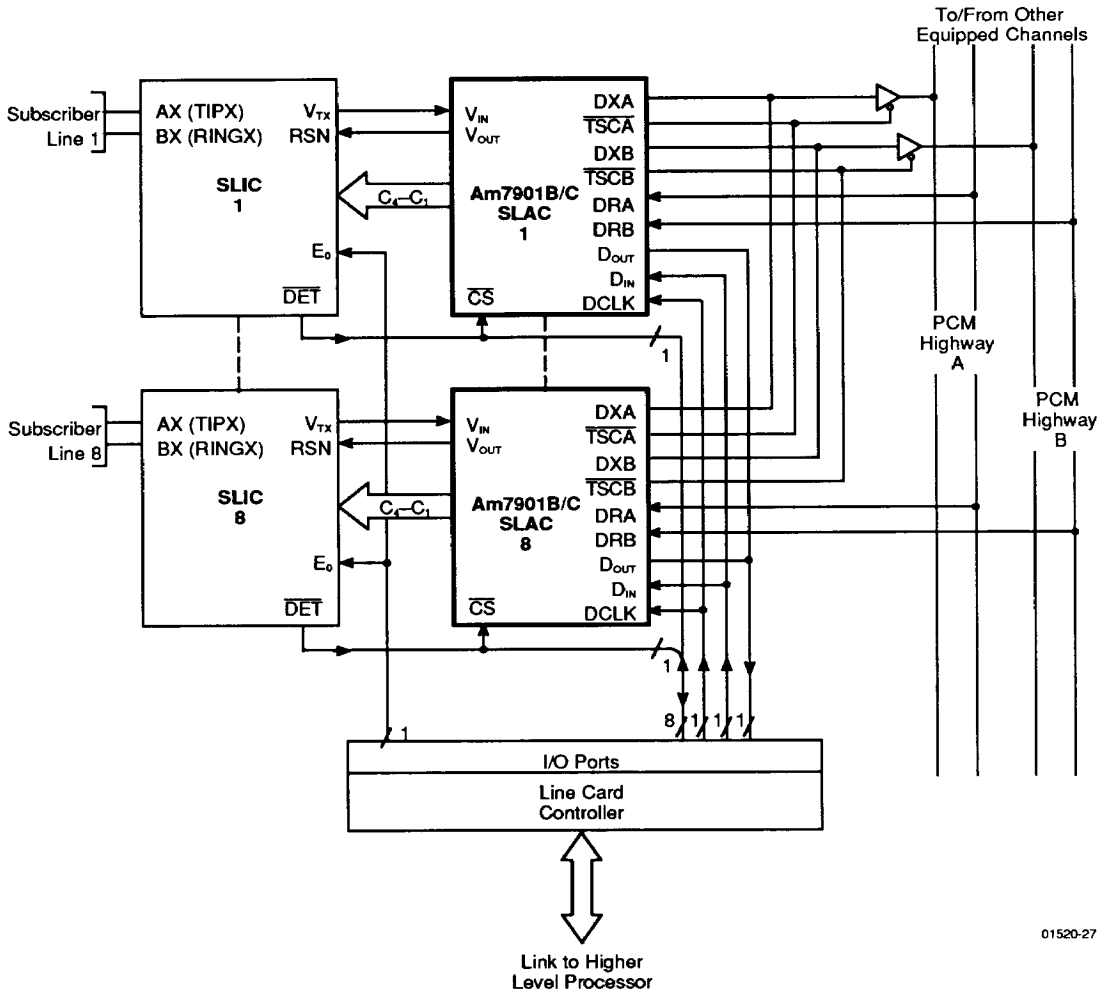
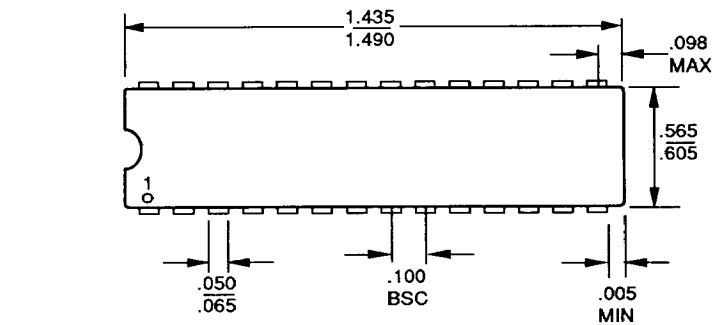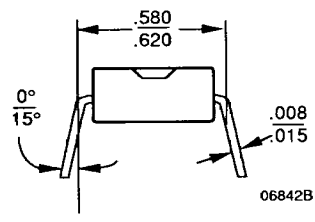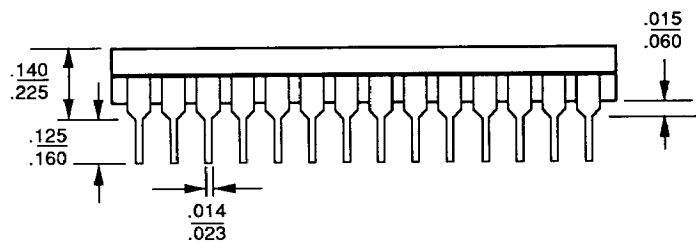## PHYSICAL DIMENSIONS

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CD 028

06837C

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06842B

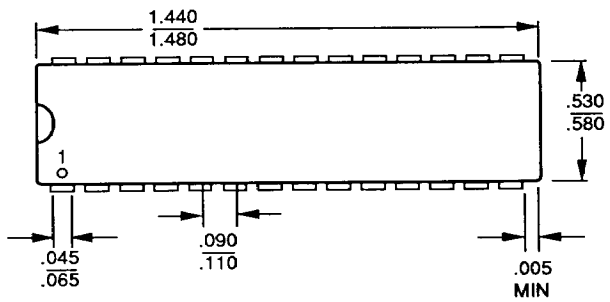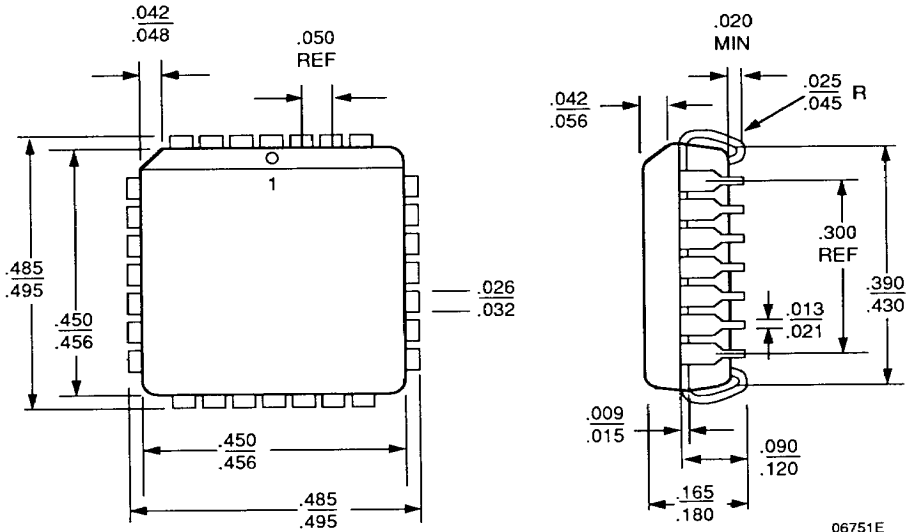This Material Copyrighted By Its Respective Manufacturer
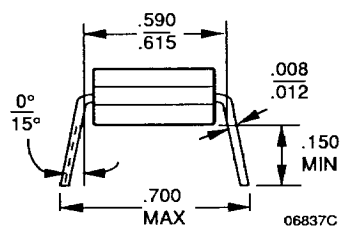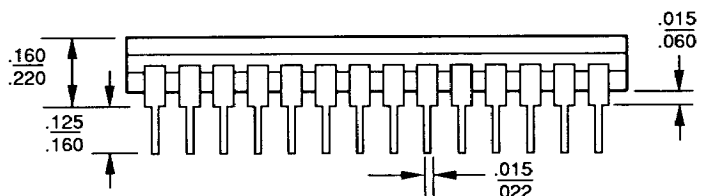
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