Final

Am6148

Microprocessor-Compatible 8-Bit A/D Converter

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

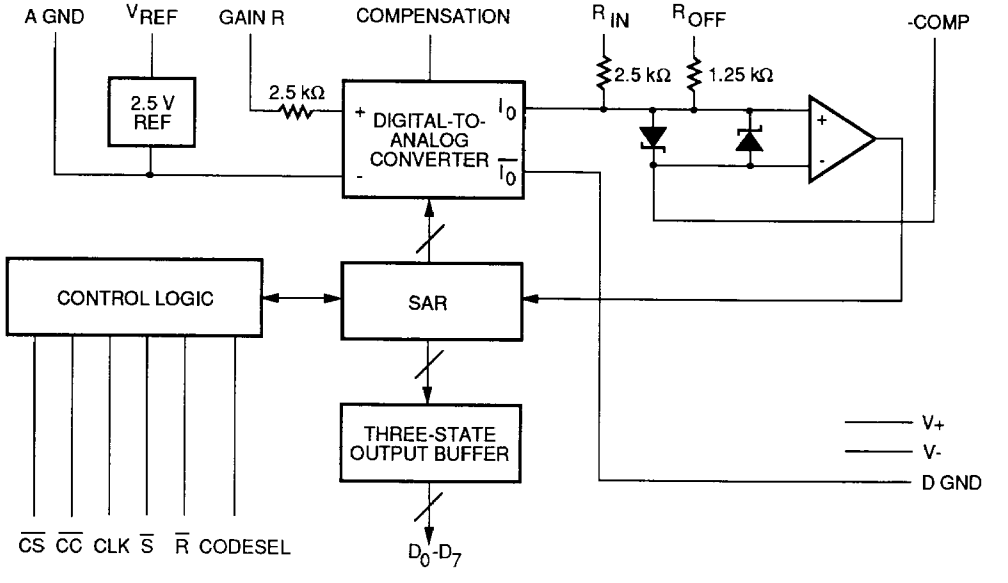
- 1 µs conversion time
- Trimmed internal voltage reference
- 0.1% nonlinearity
- Ratiometric operation
- Low operating voltages
- Internal matched gain, reference and offset resistors
- Microprocessor compatible
- Three-state outputs
- Pin-programmable unipolar or bipolar two's complement conversion
- Conversion complete output available as interrupt or as multiplexed output on data bus
- Available in slim, 24-pin, 0.3-in. package

GENERAL DESCRIPTION

The Am6148 is a microprocessor-compatible, 8-bit, high-speed, analog-to-digital converter. It includes a precision reference, DAC, comparator, SAR, scale resistors, 3-state output buffers and control logic. The Am6148 is offered in a space-saving, .300-inch-wide, 24-pin package. The Am6148 is capable of completing an 8-bit conversion in under one microsecond and can handle input voltage ranges of 0 to +10 V, 0 to +5 V, and ±5 V without external components. With appropriate external resistors, the user can program the device to operate on other input-signal ranges (2 or 3 precision resistors are required). Full 8-bit monotonic performance with no missing codes is guaranteed over temperature. It has three-state outputs for bus compatibility and a status output.

The Am6148 is useful in microprocessor-based systems or can be used in a stand-alone mode. The conversion time is short enough to allow most microprocessors to accept data immediately after requesting a conversion. Applications include analog I/O subsystems, process control and servo-control.

BLOCK DIAGRAM



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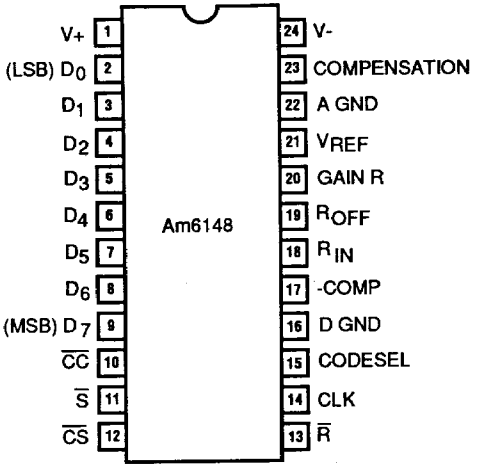
CONNECTION DIAGRAM

D-24-SLIM



Slim, 0.3" Package

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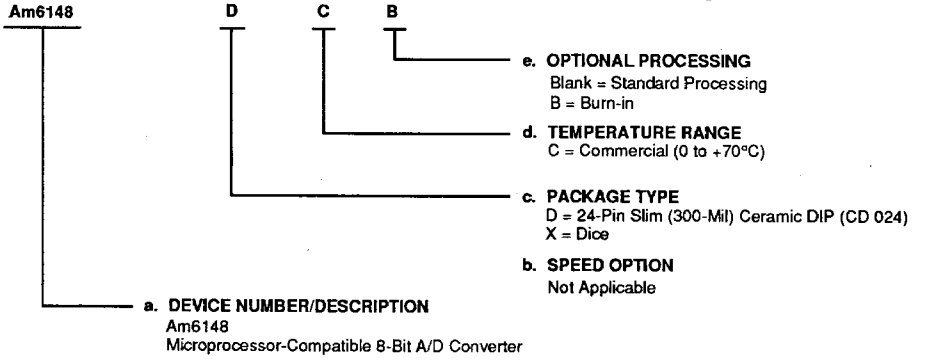
ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
Am6148	DC, DCB, XM, XC

Valid Combinations

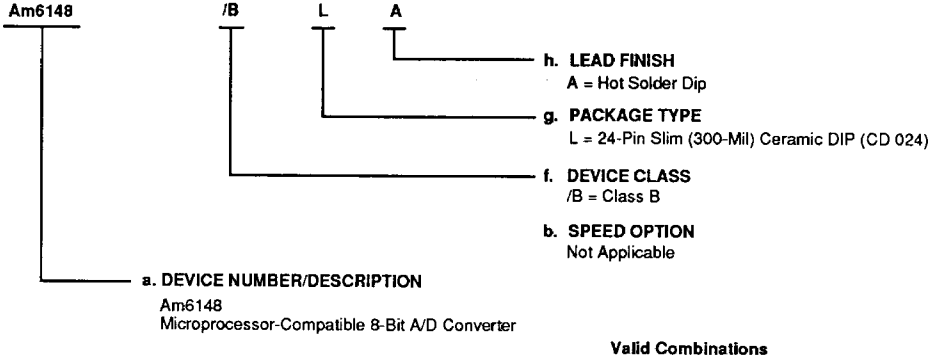
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-M-38510 and MIL-STD-883C requirements. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
f. Device Class
g. Package Type
h. Lead Finish



Valid Combinations	
Am6148	/BLA

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 4, 5, 6.

PIN DESCRIPTION

$\overline{CC}$
Conversion Complete

This active-LOW output indicates the end of a conversion.

CLK
Clock

A TTL level clock is used at this input to produce the internal timing of the Am6148 during a conversion.

CODESEL
Code Select

A logic 1 on this input enables the Am6148 to output data in binary offset format; a logic 0 results in two's complement format.

–COMP
Comparator Inverting Input

Allows the user to add an offset voltage to null the system or as a zero reference. It may also be used as a high-impedance input, normally it is connected to analog ground.

COMPENSATION
Reference Amplifier Compensation

An external capacitor is connected between this pin and V– to provide frequency compensation for the DAC reference amplifier.

$\overline{CS}$
Chip Select

Enables the Am6148 for read and start conversion operations.

$D_0 - D_7$
Data Outputs

Eight three-state outputs, used to transfer data from the Am6148 to the processor.

GAIN R
Reference Input Gain Resistor

A 2.5 kΩ resistor in series with the positive input of the DAC reference amplifier. When 2.5 V is applied to this pin, a 1.0-mA reference current flows to the DAC. This produces a DAC full-scale current of 4 mA.

$\overline{S}$
Start Conversion

An active LOW input that resets the successive approximation register. When $\overline{S}$ is taken back HIGH, the Am6148 begins a conversion.

$\overline{R}$
Read

An active-LOW input that enables the three-state outputs and allows data to be transferred from the Am6148 to the processor.

R_{IN}
Analog Input Resistor

A 2.5-kΩ resistor in series with the summing node at the noninverting input to the comparator. It converts the analog input voltage to a current for comparison with the current at the DAC Io output. When the DAC has a reference current of 1.0 mA, this input can be used alone for a 0 to +10 V input range, or in conjunction with the R_{OFF} input for a –5 to +5 V range.

R_{OFF}
Input Offset Resistor

A 1.25-kΩ resistor in series with the summing node at the noninverting input of the comparator. When this input is connected to the 2.5-V reference, a half-scale offset current enters the summing node. This allows a bipolar input range of –5 to +5-V at the R_{IN} input. The R_{OFF} pin may also be used as an analog voltage input for a 0 to +5 V range. When R_{OFF} is not used, this pin should be connected to AGND.

V_{REF}
Reference Voltage Output

The output of the internal, precision 2.5 V reference.

THEORY OF OPERATION

A conversion cycle in the Am6148 begins by taking the Start Conversion, $\overline{S}$, input LOW simultaneously with $\overline{CS}$ LOW and the CLK input LOW; this resets the Successive Approximation Register (SAR). When $\overline{S}$ is returned HIGH, all bits of the SAR are ones with the exception of the MSB, which is set to a zero. The output of the SAR is fed to a DAC that converts it to a current. The current from the DAC output is then compared with the current generated by the analog input voltage. Based on this comparison, the SAR either keeps the MSB as a zero or resets it to a one before beginning the next approximation. This process of successive removal and testing continues until all bits have been tested. At that time the Conversion Complete, $\overline{CC}$, output goes LOW, and the Am6148 is ready to output the data byte or begin a new conversion.

Read operations in the Am6148 are initiated by taking $\overline{CS}$ and $\overline{R}$ both LOW to enable the three-state data outputs. When the three-state outputs are enabled there are two formats for reading data out of the Am6148: two's complement format is selected by holding CODESEL LOW during the read, and binary offset is selected by holding CODESEL HIGH. Table 1 shows the complete decoding of the Am6148 control lines.

The full-scale output current of the DAC is determined by the reference current supplied to the GAIN R and/or REF_{IN} inputs of the Am6148. The DAC full-scale output current is four times the reference current. The GAIN R input is a 2.5-kΩ series resistor that will convert the 2.5 V internal reference voltage into a 1-mA reference current.

Once the DAC reference current is set up, the Am6148 can be operated with either a unipolar or bipolar input signal. Two inputs are provided for unipolar operation, the R_{IN} input has a 2-kΩ resistor connected between it and the comparator summing node. The R_{OFF} input is identical to R_{IN}, except the value of the resistor is 1.25 kΩ. The R_{IN} input is used alone for a unipolar input of 0 to +10 V and the R_{OFF} input is used alone for 0 to +5-V signals. The bipolar operation of the Am6148 requires a half-scale offset current to be supplied to the comparator summing node. This can be accomplished by connecting the R_{OFF} input to the V_{REF} output, which produces a 2-mA offset current to the comparator summing node. A –5 to +5 V input signal can be applied at R_{IN}.

DEFINITION OF TERMS

Resolution: The number of possible analog input levels an A/D will resolve. Expressed as the number of output bits, or 1 part in 2^n where n is the number of bits.

Monotonicity (Missing Codes): Monotonicity is a property of the D/A within a successive approximation (S/A) A/D. Each increment in the digital code to the D/A is accompanied by an analog output that is greater than, or equal to, that of the proceeding code. Monotonicity of the D/A is a necessary requirement for a S/A A/D to have no missing codes.

Differential Nonlinearity: The deviation between the actual code width of an A/D from the ideal code width. The code width is defined as the range of analog input value which produces a given digital output code. An ideal value of a code width is equivalent to $FSR/2^n$, where n is the number of bits.

Linearity: The deviation of each individual code from an ideal straight-line transfer curve between zero and full scale, with the straight line measured from the middle of each particular code.

Inherent Quantization Error: Quantization Error is a direct consequence of the resolution of the A/D. All analog voltages within a given range are represented by a single digital output code. There is, therefore, an *inherent* ±1/2 LSB conversion error even for a perfect A/D.

Gain Error: Defined as the difference between the analog input levels required to produce the first and the last digital output-code transitions. Gain error is a measure of the deviation between the actual gain from the ideal gain of FS-2 LSB.

Unipolar Offset Error: Difference between the ideal (+1/2 LSB) and the actual analog input level required to produce the first digital code transition (00....00 to 00....01) over the complete temperature range.

TABLE 1. AM6148 CONTROL SIGNAL DECODING

Signals						
CLK	$\overline{CS}$	$\overline{S}$	$\overline{R}$	CODESEL	$\overline{CC}$	Function
X	1	X	X	X	X	Outputs Three-stated
0	0	0	X	X	X	Reset SAR
X	0	1	0	X	1	Outputs Three-stated
X	0	1	0	0	0	Read Data (Two's Complement Code)
X	0	1	0	1	0	Read Data (Binary Offset Code)

X = Don't Care

Bipolar Offset Error: Difference between the ideal (1/2 FSR – 1/2 LSB) and the actual analog input level required to produce the major carry-output digital-code transition (from 01....11 to 10....00).

Power Supply Sensitivity: A measure of the change in gain of the A/D resulting from a change in supply voltage. Usually expressed in total %FS for a percentage change in supply voltage.

Conversion Time: The measure of how long it takes for the A/D to arrive at the correct digital-output code. It is the time between the clock edge that starts a conversion after receiving a start command and the edge of the status line ($\overline{CC}$) which signifies that the conversion is completed.

MAXIMUM RATINGS

Storage Temperature	–65 to +150°C
Lead Temperature (Soldering 60 sec)	300°C
Minimum Operating Voltage	9.7 V
V+ to DGND	–0.3 to +7.0 V
V– to DGND	+0.3 to –7.0 V
Max Differential V+ to V–	±12 V
Digital Inputs to DGND	–0.5 to +6.0 V
AGND to DGND	± 1 V
V_{REF} Max Output Current	15 mA
Max Input Current at REF_{IN}	2 mA
Voltage at GAIN R, REF_{IN}	V– to V+
Voltage at R_{IN}, R_{OFF}	±12 V
DAC Compliance Voltage	–2 to +12 V

Stresses above those listed under MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commerical	0 to +70°C
Military	–55 to +125°C
Die Size	0.116 x 0.156 in.

Operating ranges define those limits between which the functionality of the device is guaranteed.

ELECTRICAL CHARACTERISTICS

(These specifications apply for commercial: V+ = +5 V, V– = –5.2 V ±5%; military: V+ = ±5 V, ±4.5 V & ±5.5 V, V_{REF} connected to GAIN R, 0°C ≤ T ≤ 70°C and f_{CLOCK} = 500 kHz.)
Included in Group A Subgroups 1,2,3,4,5,6 as noted.

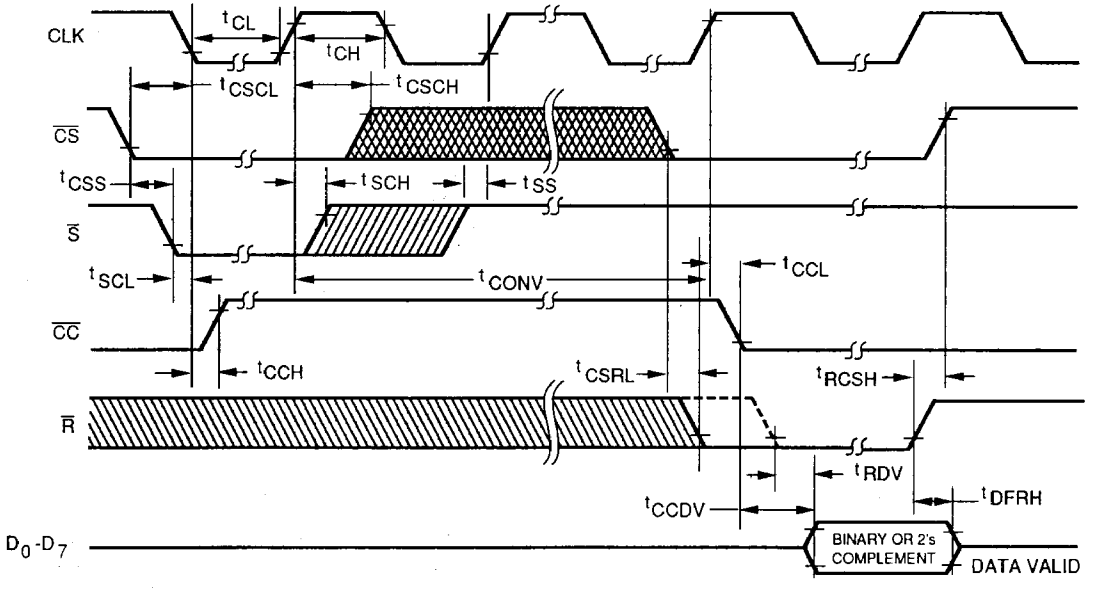
Parameter	Description	Test Conditions		Min.	Max.	Unit
Transfer Characteristics						
	Resolution			8	8	bit
	Monotonicity			8	8	bit
	Differential Nonlinearity				±1/2	LSB
	Linearity				±1/2	LSB
	Inherent Quantization Error				±1/2	LSB
	Unipolar Gain Error	V_{IN} = 0 to +5 V			±4	LSB
		V_{IN} = 0 to +10 V	COM'L		±2	LSB
			MIL		±4	LSB
	Unipolar Offset Error				±1	LSB
	Bipolar Gain Error	V_{IN} = –5 V to +5 V	COM'L		±2	LSB
			MIL		±4	LSB
	Bipolar Offset Error				±2	LSB
	Pos Power Supply Sensitivity	V+ = +4.5 to +5.5 V			0.2	%FS
	Neg Power Supply Sensitivity	V– = –5.5 to –4.5 V			0.2	%FS
Internal Reference						
V_{REF}	Reference Voltage	I_{REF} = 1 mA	COMM	2.485	2.515	V
			MIL	2.470	2.530	V
$\Delta V_{REF}/V_{REF}$	Load Regulation	I_{REF} = 1 to 5 mA			0.2	$\%V_{REF}$
$\Delta V_{REF}/V_{REF}$	Line Regulation	V+ = +4.5 to +5.5 V			0.2	$\%V_{REF}$
Digital Inputs						
	Logic Level Input Voltage					
V_{IH}	Logic 1			2.0		V
V_{IL}	Logic 0				0.8	V
	Logic Level Input Current					
I_{IH}	Logic 1	V_{IN} = 2.7 V			40	µA
I_{IL}	Logic 0	V_{IN} = 0.4 V			10	µA
	Logic Level Output Voltages					
V_{OH}	Logic 1	I_{OH} = –400 µA		2.4		V
V_{OL}	Logic 0	I_{OL} = 8 mA			0.5	V
I_{OZ}	Off–State Output Current	V_O = 2.4 V		–20	+20	mA
		V_O = 0.4 V		–20	+20	mA
Power Requirements						
I+	Positive Supply Current				60	mA
I–	Negative Supply Voltage				–85	mA
	Power Dissipation				800	mW

AC CHARACTERISTICS over operating range unless otherwise specified.

Parameter	Description	Test Conditions	Min.	Max.	Unit
t_{CONV}	Conversion Time			2	µs
t_{CSS}	$\overline{CS}$ LOW to $\overline{S}$ LOW	Note 1	0		ns
t_{CSCL}	$\overline{CS}$ LOW to CLK LOW	Note 1	0		ns
t_{SCL}	$\overline{S}$ LOW to CLK LOW	Note 1	0		ns
t_{CCH}	$\overline{CC}$ HIGH from CLK LOW	Note 1		55	ns
t_{SCH}	$\overline{S}$ HIGH from CLK HIGH	Note 1	0		ns
t_{SS}	$\overline{S}$ HIGH Before CLK HIGH	Note 1	10		ns
t_{CSCH}	$\overline{CS}$ HIGH from CLK HIGH	Note 1	0		ns
t_{CCL}	$\overline{CC}$ LOW from CLK HIGH	Note 1	15	40	ns
t_{CSRL}	$\overline{CS}$ LOW to $\overline{R}$ LOW	Note 1	0		ns
t_{CCDV}	$\overline{CC}$ LOW to Data Valid	Note 1	3	40	ns
t_{RDV}	$\overline{R}$ LOW to Data Valid	Note 1	15	40	ns
t_{DFRH}	Date Float from $\overline{R}$ HIGH	Note 1	20	75	ns
t_{RCSH}	$\overline{R}$ HIGH to $\overline{CS}$ HIGH	Note 1	0		ns
t_{CL}	CLK LOW	Note 1	50		ns
t_{CH}	CLK HIGH	Note 1	50		ns

Note 1. Guaranteed by characterization. Not tested.

System Timing



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APPLICATIONS INFORMATION

The Am6148 contains all the active components required to perform a complete A/D conversion. The device is specified over the complete temperature range and includes the effects of the on-chip voltage reference.

Figures 2 and 3 show the Am6148 used in unipolar and bipolar configurations. Gain and offset errors may be trimmed for optimum performance using external components (discussed later). The maximum offset error, unipolar and bipolar, are specified as ±1 LSB and ±2 LSB, respectively, over the complete temperature range and in many applications would not require any trimming.

Both Figures 2 and 3 show the Am6148 configured as an I/O port. A conversion is started by performing a write operation to the port address. The $\overline{IOW}$ line strobes the $\overline{S}$ input to start the conversion. Operating with a 10-MHz clock, the Am6148 completes a conversion within 1 µs; therefore with many CPUs, a read operation could occur immediately after starting the conversion and receive valid data. The Am6148 requires a minimum of nine clock cycles to complete a conversion, which most microprocessors can meet fairly easily. However, if the Am6148 is used with a slower clock, a circuit similar to Figure 4 may be used to hold the processor in wait states during the read operation until the $\overline{CC}$ output goes LOW.

The data from the A/D converter can be read out using a normal I/O read operation to the port address. The output code may be offset binary or two's complement depending upon the logic state of CODESEL (logic 1 = offset binary, logic 0 = two's complement).

The Am6148 may also be interfaced with a DMA controller for burst-mode operation. Figure 5 shows the Am6148 interfaced with the Am9517A DMA Controller. The DMA mode of operation begins with a software request for block transfer by the Am9517A. The Am6148 begins a conversion each time it receives a request and holds the DMA controller in wait states until each conversion is complete. This cycle is repeated until a complete block of data has been transferred to memory.

Unipolar Configuration (Figure 2)

The Am6148 is intended to have a nominal 1/2 LSB offset so that the exact analog input for a given code will be in the middle of the code. If no trims are used, the Am6148 is guaranteed to have ±1 LSB max zero-offset error and ±2 LSB max gain error (0 to +10-V full scale). If the offset trim is not required, R_{OFF}, (pin 19) should be connected to analog ground. The two resistors (R_1 and R_2) and potentiometer (R_3) are not needed. If the gain error (full scale) trim is not required, resistor R_5 should be removed and the analog input connected to R_{IN} directly. The 100 Ω full-scale adjust potentiometer (R_4) is not needed and the V_{REF} output is connected directly to GAIN R. When a 0 to +5-V input range is required, the analog input is connected to R_{OFF} instead of R_{IN}. R_{IN} should be connected to analog ground in this application.

Unipolar Calibration

The initial offset error can be trimmed by R_3 by connecting R_{OFF} to R_1 and R_2. The first A/D transition (0000 0000 to 0000 0001) should occur for an input level of +1/2 LSB (19.5 mV). The gain error (full scale) trim is done by applying a signal 1-1/2 LSBs below the nominal full scale (9.94 for a 10-V input range). R_4 is trimmed to give the last transitions (1111 1110 to 1111 1111).

Bipolar Configuration (Figure 3)

If the offset and gain errors are acceptable, one or both of the trimmers plus the 50-Ω resistor R_3 can be removed. The analog input is applied directly to R_{IN} and V_{REF} is connected to GAIN R and R_{OFF} directly.

Bipolar Calibration

Bipolar calibration is similar to unipolar calibration. First, a signal +1/2 LSB above negative full scale (–4.9805 V) for the ±5-V input range is applied to R_3 and potentiometer R_1 is trimmed to give the first transition (0000 0000 to 0000 0001). Then a signal 1-1/2 LSB below positive full scale (+4.9941 V) is applied and potentiometer R_2 trimmed to give the last transition (1111 1110 to 1111 1111).

Offset and gain calibration can be more accurately trimmed by summing a small triangular wave voltage to the analog input signal, and the digital outputs monitored to determine the center point of the code transition.

Driving the Am6148

The Am6148 is a successive approximation type analog-to-digital converter. During the conversion cycle, the A/D input current is modulated by the DC test current at the A/D clock frequency. Thus, it is important to recognize that the signal source driving the Am6148 must be capable of holding a constant output voltage under dynamically changing load currents. Many operational amplifiers have closed-loop output impedance equal to the open-loop output impedance (usually a few hundred ohms) divided by the loop gain at the frequency of interest. At high frequencies, where the loop gain is low, the amplifier output impedance rises to its open-loop value. The output of the amplifier may return to its nominal voltage before the converter makes a comparison, so that little or no error is introduced. However, many precision amplifiers have limited bandwidth, which recover very slowly from output transients. The use of wideband amplifiers is recommended plus a unity-gain buffer included inside the amplifier feedback loop.

Supplying Decoupling and Layout Considerations

The Am6148 is built using a very high-frequency bipolar process; therefore, it is very important that the power supplies be filtered, well regulated and free from high-

frequency noise. Switching power supplies are not recommended because of the switching spikes present. Decoupling of the supplies with 10-µF tantalum capacitors in parallel with 0.1-µF disc ceramic-type capacitors is recommended. If the supplies are still noisy then further filtering can be achieved by inserting low-value series resistors (metal film) between the supplies and the decoupling capacitors.

Circuit layout should attempt to keep analog circuitry of the Am6148 and associated components as far away from logic interconnections as possible. The analog ground (AGND) is the ground point for the internal reference, D/A converter and comparator and should be a high-quality ground. In most cases, the AGND and DGND can be connected together at the package, but in some situations, the DGND can be connected to the most convenient ground, and the AGND to the analog power return.

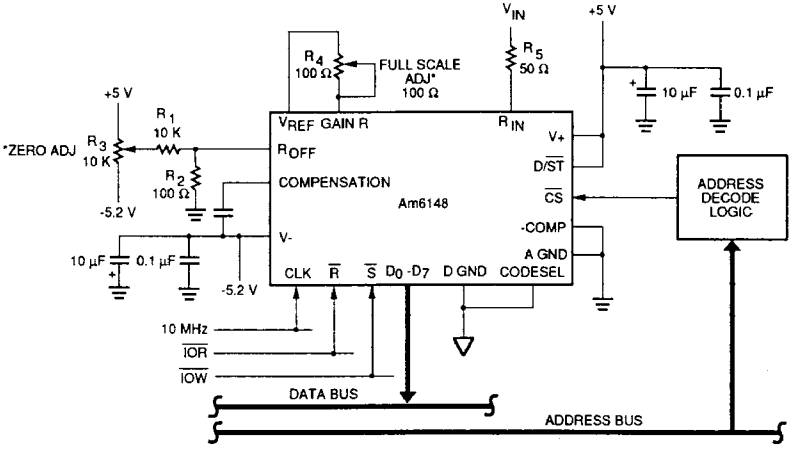

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Figure 2. Am6148 Unipolar Configuration

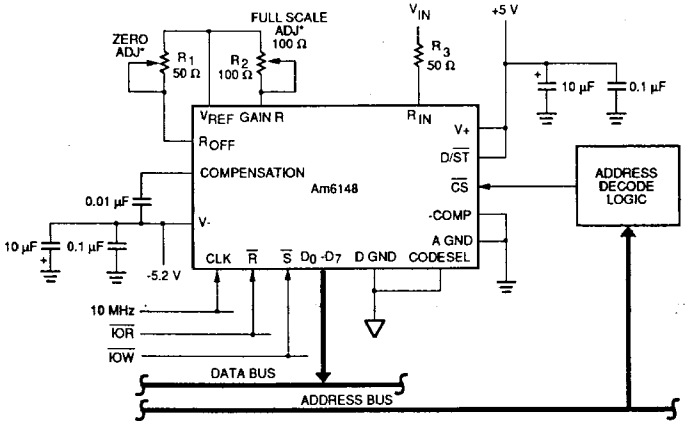

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Figure 3. Am6148 Bipolar Configuration

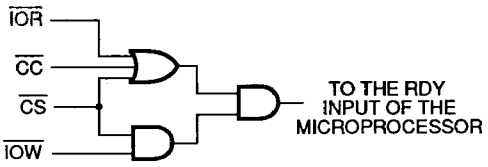

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Figure 4. Am6148 $\overline{CC}$ to Microprocessor RDY Interface

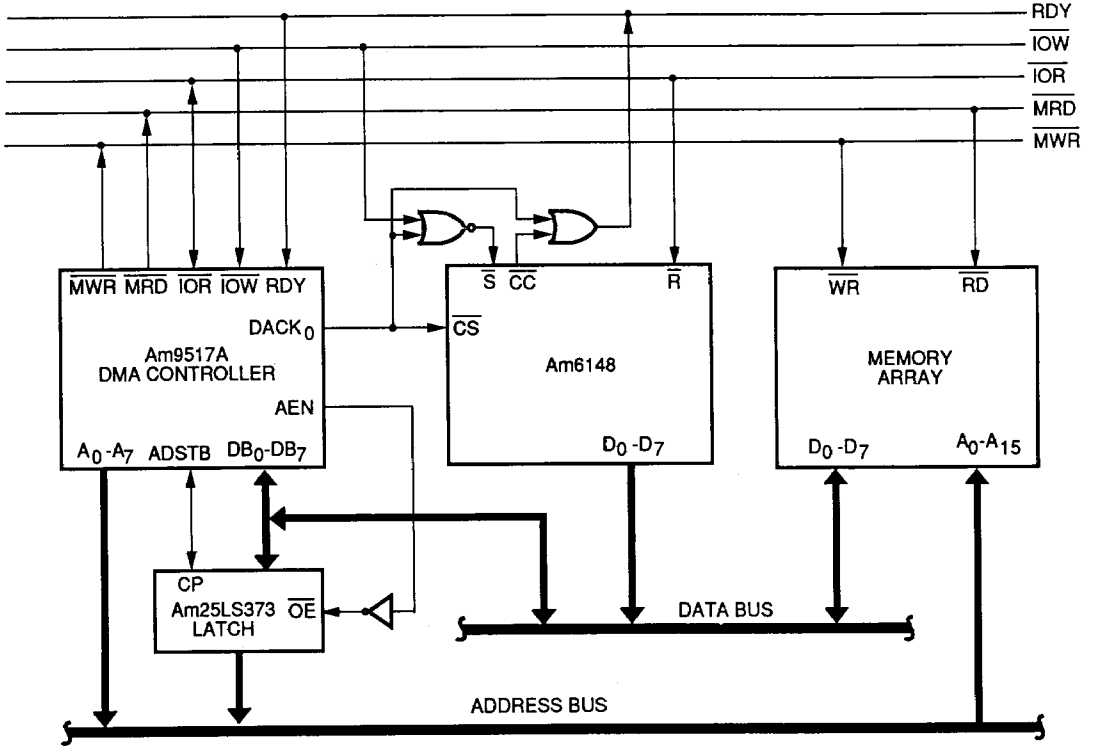

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Figure 5. Am6148 DMA Configuration

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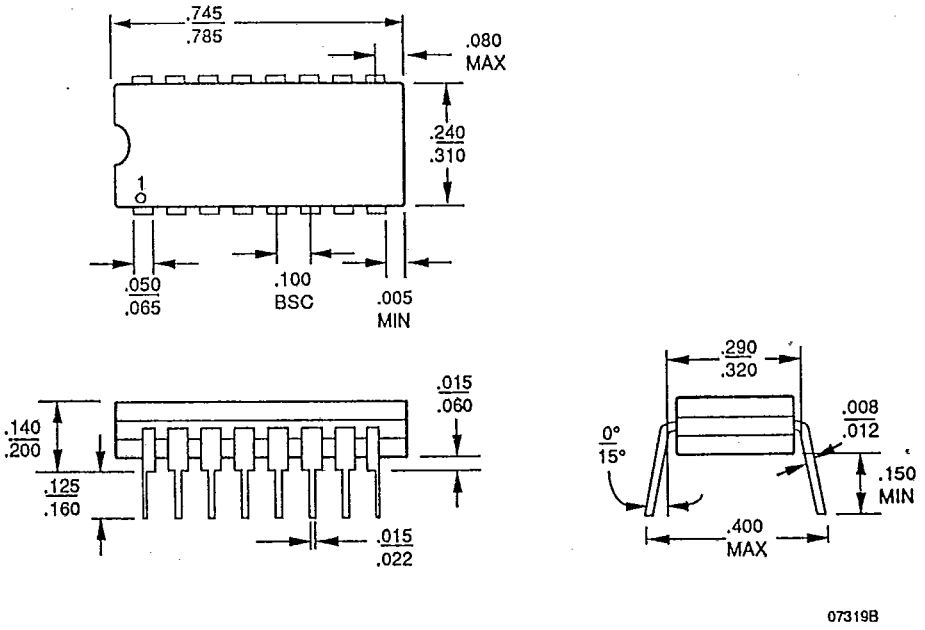
PHYSICAL DIMENSIONS
CD 016



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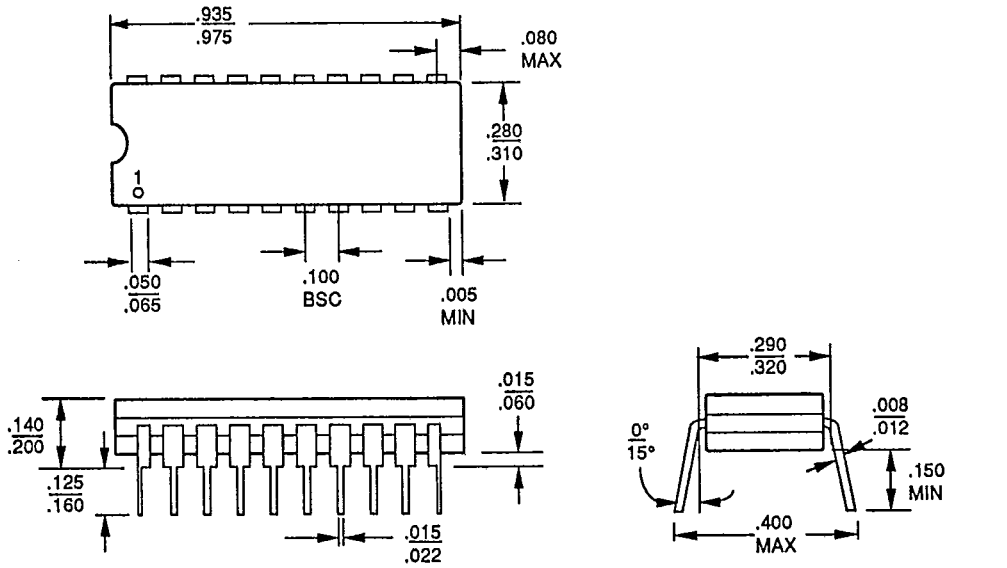
CD 020



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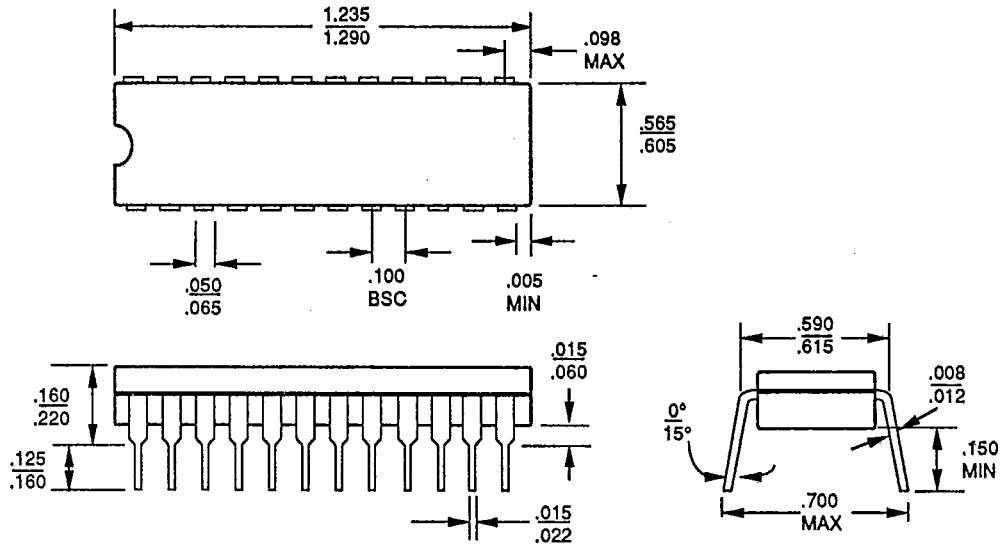
PHYSICAL DIMENSIONS (continued)
CD 024



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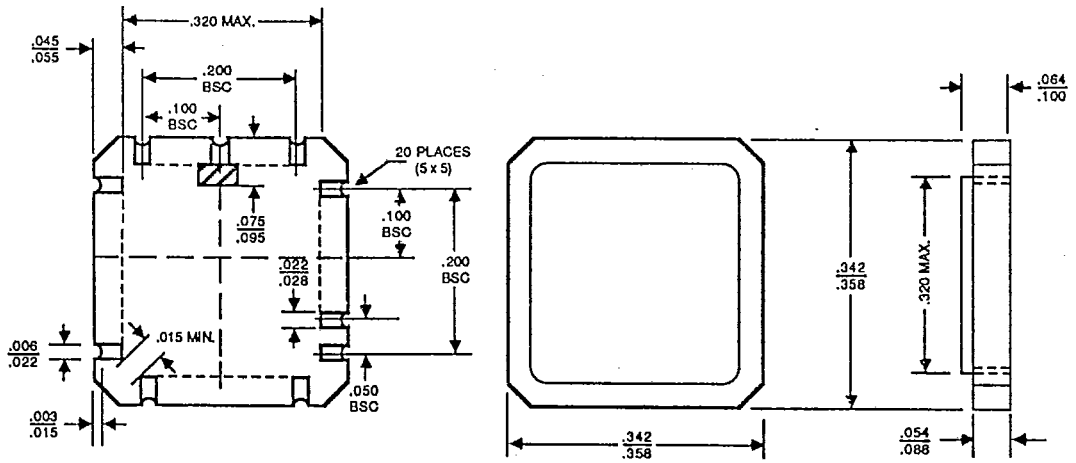
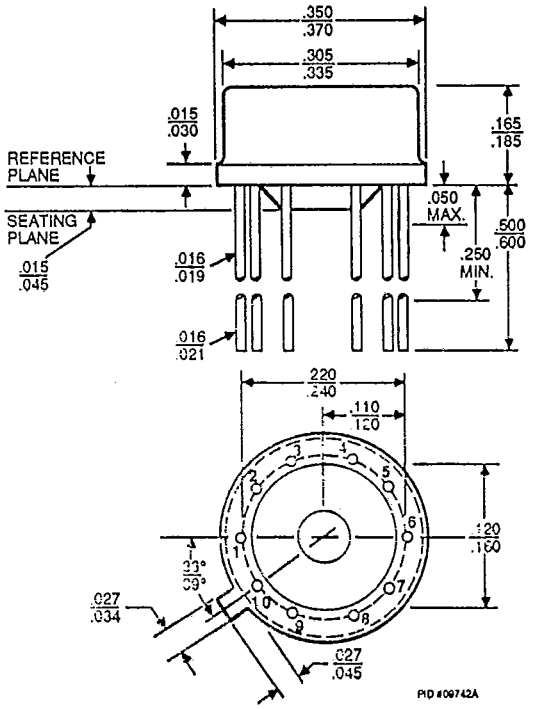
CL 020



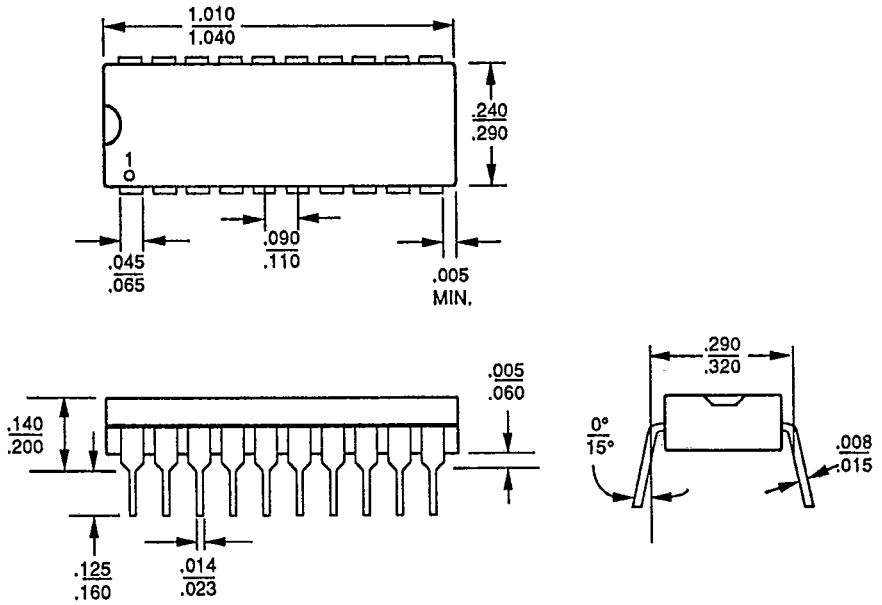
PID #07318C

PHYSICAL DIMENSIONS (continued)

MC 010



PD 020



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