PM5395

CRSU™ 4x2488

Quad Clock Recovery and Synthesis Unit for 2488 Mbit/s

Data Sheet

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Revision History

Issue No.	Issue Date	Details of Change
5	December 2002	Updated power numbers. Added reference to Bellcore spec GR253 -CORE 1995 and 2000 release. Note added to QSFI-4 Common Electrical Interface Overview, detailing the QSFI-4 is not IEEE LVDS compliant when CSU channel 0 is reset. Added Jitter Tolerance plot. Typical Intrinsic Jitter number added. LCRUTO pins are now documented. CRU reset period added.
4	November 2002	Master register 000DH ICO Swing Bits no longer reserved and updated for looptime settings.
3	May 2002	Document ported to new template. System side OIF SFI-4 interface is now referenced as QSFI-4.
2	Nov 2001	Added more FEC details. Removed note that indicated automatic AIS insertion (mechanism provided for AIS insertion but not automatic). Added Patent information
1	March 2000	Document created

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1 Definitions

The following table defines the abbreviations for the CRSU™ 4x2488.

Table 1 Abbreviations Used in this Document

AIS	Alarm Indication Signal
AIS-L	Alarm Indication Signal for Line overhead
APS	Automatic Protection Switching
ASSP	Application Specific Standard Product
ATM	Asynchronous Transfer Mode
BER	Bit Error Rate
BIP	Bit Interleaved Parity
CMOS	Complementary Metal Oxide Semiconductor
CRC	Cyclic Redundancy Check
CRU	Clock Recovery Unit
CSU	Clock Synthesis Unit
DCC	Data Communication Channel
DRU	Data Recovery Unit
ECL	Emitter Controlled Logic
ERDI	Enhanced Remote Defect Indication
ESD	Electrostatic Discharge
FCS	Frame Check Sequence
FEBE	Far-End Block Error
FIFO	First-In First-Out
GFC	Generic Flow Control
HCS	Header Check Sequence
HDLC	High-level Data Link Layer
ICO	Current Controlled Oscillator
JAT	Jitter Attenuator
LCD	Loss of Cell Delineation
LOF	Loss of Frame
LOP	Loss of Pointer
LOS	Loss of Signal
LVDS	Low Voltage Differential Signaling
NC	No Connect, indicates an Unused pin
NDF	New Data Flag
NNI	Network-Network Interface
ODL	Optical Data Link
OOF	Out of Frame
PECL	Pseudo-ECL

PISO	Parallel to Serial Converter
PLL	Phase-Locked Loop
POS	Packet Over SONET
PPP	Point-to-Point Protocol
PRBS	Pseudo-Random Bit Sequence
QSFI-4	Quad Serdes/Framer Electrical Interface
RDI-L	Line Remote Defect Indication
RRMP	Receive Regenerator and Multiplexor Processor
RDI	Remote Defect Indication
RIFD	Receive In-band FEC Decoder
RSOP	Receive Section Overhead Processor
RXLI	Receive Line Interface
SBER	SONET/SDH Bit Error Rate Monitor
SD	Signal Degrade
SDH	Synchronous Digital Hierarchy
SF	Signal Fail
SONET	Synchronous Optical Network
SPE	Synchronous Payload Envelopes
SRLI	SONET/SDH Receive Line Interface
STLI	SONET/SDH Transmit Line Interface
STSI	Space and Timeslot Interchange
TIFE	Transmit In-band FEC Encoder
TOH	Transport Overhead
TRSP	Transmit Regenerator and Section Processor
TXLI	Transmit Line Interface
UI	Unit Interval
UNI	User-Network Interface
VCI	Virtual Connection Indicator
VCXO	Voltage Controlled Crystal Oscillator
VPI	Virtual Path Indicator
WAN	Wide Area Network
XOR	Exclusive OR logic operator

2 Features

2.1 General

- Single chip Clock Recovery and Synthesis Unit supporting four SONET/SDH links operating at 2488.32 Mbit/s.
- Processes four independent bit-serial 2488.32 Mbit/s STS-48 (STM-16) data streams with on-chip clock and data recovery and clock synthesis.
- Complies with Bellcore GR-253-CORE jitter tolerance, jitter transfer and intrinsic jitter criteria.
- Implements In-band Forward Error Correction (FEC) source and sink function according to ANSI Committee T1, Letter Ballot LB812.
- Implements In-band Forward Error Correction (FEC) line regeneration equipment (LRE) function according to ANSI Committee T1, Letter Ballot LB812.
- Provides performance monitoring of SONET Section, and Line layer entities or SDH Regenerator Section, and Multiplexer Section entities.
- Interfaces with downstream SONET/SDH framer devices over a set of four 4-bit, 622 MHz ports that conforms to the timing and AC characteristics defined in the Optical Internetworking Forum, contribution OIF-SFI4-01.0.
- Supports line loop-back from the line side receive stream to the transmit stream and system side loop-back from the QSFI-4 transmit interface to the QSFI-4 receive stream interface.
- Supports loop-timing of the transmit stream from the associated receive stream.
- Supports Internal Channel-to-Channel loop Function. Channel 0 can be internally connected to Channel 1, and Channel 2 can be connected to Channel 3.
- Provides a standard 5 signal IEEE 1149.1 JTAG test port for boundary scan board test purposes.
- Provides a generic 16-bit microprocessor bus interface for configuration, control, and status monitoring.
- Low power 1.8V CMOS core logic with 3.3V CMOS/TTL compatible digital inputs and digital outputs. PECL inputs and CML outputs are 3.3V compatible.
- Industrial temperature range (-40°C to +85°C Ambient, 125°C Maximum Junction Temperature).
- 580 pin 35mmx35mm UBGA package.

2.2 SONET Section and Line / SDH Regenerator and Multiplexer Section

- Frames to the SONET/SDH receive stream and inserts the framing bytes (A1, A2) into the transmit stream; unscrambles the received stream and scrambles the transmit stream.

- Calculates and compares the bit interleaved parity (BIP) error detection codes (B1, B2) for the receive stream. Calculates and inserts B1 in the transmit stream. Accumulates near end errors (B1, B2) and far end errors (M1).
- Extracts and filters the automatic protection switch (APS) channel (K1, K2) bytes into internal registers.
- Extracts and filters the synchronization status message (S1) byte into an internal register for the receive stream.
- Detects loss of signal (LOS), out of frame (OOF), loss of frame (LOF), line remote defect indication (RDI-L), line alarm indication signal (AIS-L), and protection switching byte failure alarms on the receive stream.
- Provides a mechanism to insert automatic line AIS insertion following detection of various received alarms LOS and LOF on to the QSFI-4 system side receive interface.
- Configurable to force Line AIS in the transmit stream.

2.3 SONET / SDH In-band Forward Error Correction

- Implements In-band Forward Error Correction sink function with a maximum delay of 15µs. Frames to the FEC status indication signal (FSI), and optionally outputs corrected data onto the receive system side interface.
- Counts corrected FEC errors in a set of software readable registers.
- Implements In-band Forward Error Correction source function with a maximum delay of 15µs. Optionally inserts FEC checksum bytes and FSI into the transmit stream. Line BIP (B2) bytes are compensated for the inserted FEC byte values.
- Support FEC Line Regeneration Equipment function with a maximum delay of 15.36µs by looping the receive stream to the transmit stream after FEC error correction.

3 Applications

- DWDM Terminal Multiplexers.
- ATM and Multi-service Switches, routers, and switch/routers
- SONET/SDH Add/Drop Multiplexers with data processing capabilities
- SONET/SDH ATM/POS Test Equipment

4 References

1. Applicable Recommendations and Standards. The designer is required to read these references during the Design Planning task. See the Device Design Procedure, PMC-1940424.

2. Telcordia - GR-253-CORE “SONET Transport Systems: Common Generic Criteria”, Issue 3, September 2000.

3. Telcordia - GR-253-CORE “SONET Transport Systems: Common Generic Criteria”, Issue 2, December 1995.

4. Telcordia - GR-436-CORE “Digital Network Synchronization Plan”, Issue 1 Revision 1, June 1996.

5. ANSI - T1.105-1995, “Synchronous Optical Network (SONET) – Basic Description including Multiplex Structure, Rates, and Formats”, 1995.

6. ANSI – T1 Letter Ballot LB812, “In-band FEC for SONET”, October 1999.

7. ETS 300 417-1-1, "Generic Functional Requirements for Synchronous Digital Hierarchy (SDH) Equipment", January 1996.

8. ITU-T Recommendation G.703 - "Physical/Electrical Characteristics of Hierarchical Digital Interfaces", 1991.

9. ITU-T Recommendation G.704 - "General Aspects of Digital Transmission Systems; Terminal Equipment - Synchronous Frame Structures Used At 1544, 6312, 2048, 8488 and 44 736 kbit/s Hierarchical Levels", July 1995.

10. ITU, Recommendation G.707 - "Network Node Interface For The Synchronous Digital Hierarchy", 1996.

11. ITU Recommendation G781, “Structure of Recommendations on Equipment for the Synchronous Design Hierarchy (SDH)”, January 1994.

12. ITU, Recommendation G.783 - "Characteristics of Synchronous Digital Hierarchy (SDH) Equipment Functional Blocks", 1996.

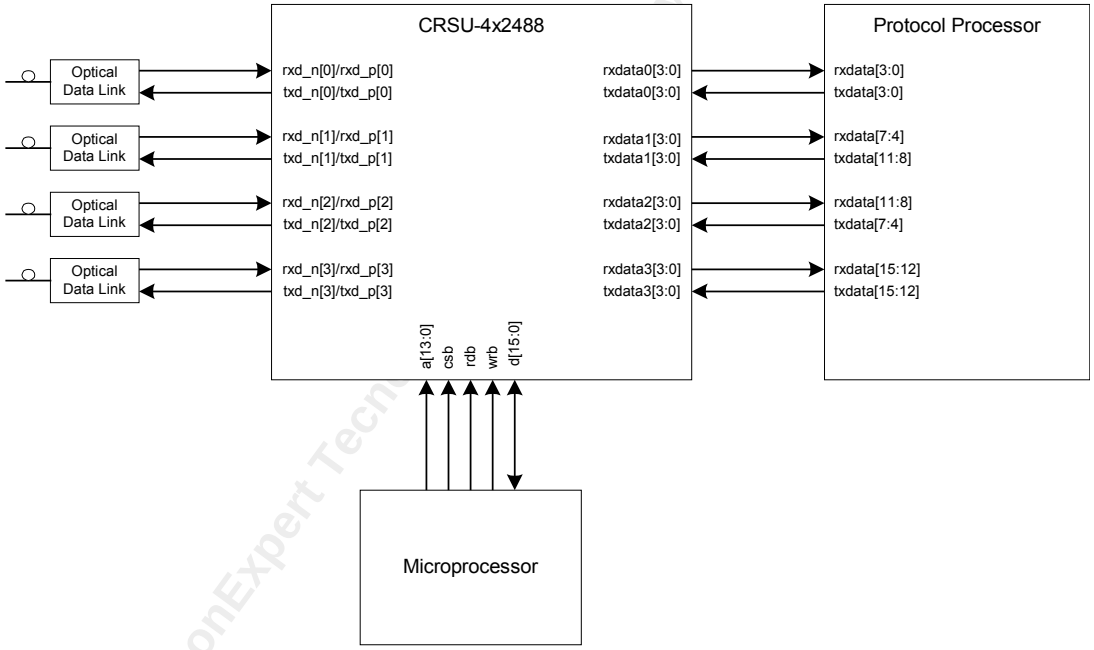
13. OIF-SFI4-01.0, “SFI-4: Common electrical interface between framers and serializer/deserializer parts for STS-192/STM-64 interfaces”. September 26, 2000.

14. IEEE std 1596.3-1996, “IEEE Standard for Low-Voltage Differential Signals (LVDS) for scaleable Coherent Interface (SCI)”, March 21, 1996

5 Application Examples

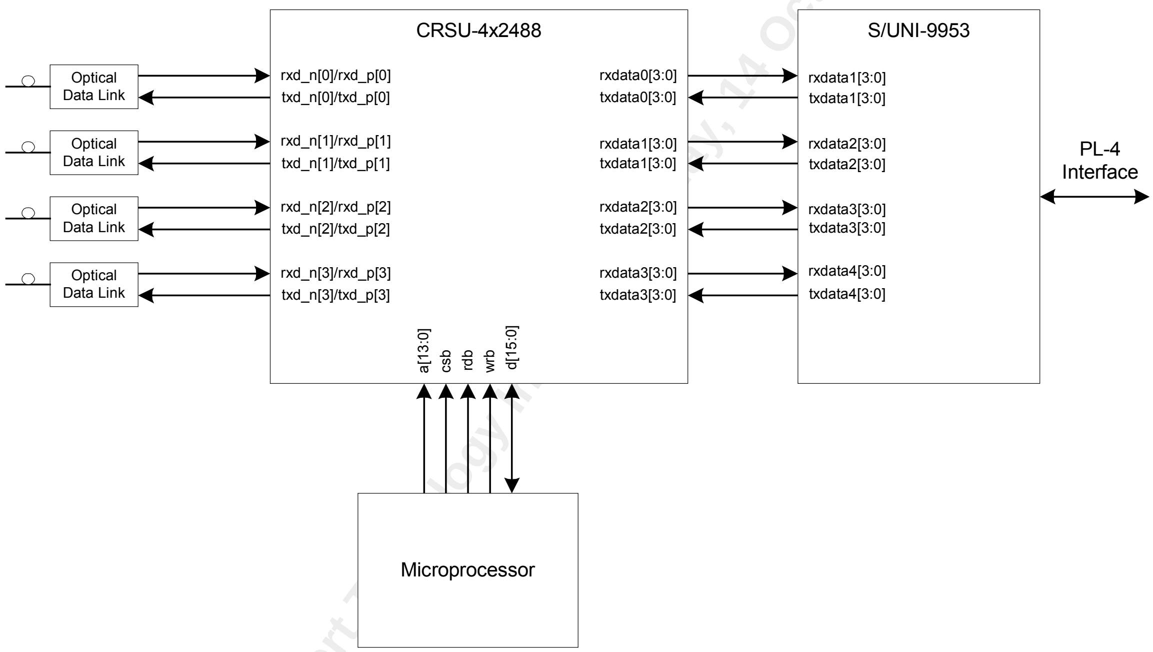
The PM5395 CRSU 4x2488 is applicable to many types of equipment that implement a 2.488 Gbit/s serial interfaces. When the device is configured for pass through mode the CRSU 4x2488 bridges between an optical module and a Protocol Processor. No higher level processing of the data is done after the data is extracted from the serial stream. In this mode, the CRSU 4x2488 may serve as the SERDES for data streams of arbitrary formats provided for optical line-side data rates of 2.488Gbit/s. The CRSU 4x2488 provides clock and data recovery functions in the receive direction and clock synthesis functions in the transmit direction. The four interfaces to the optical module are serial 2.488 Gbit/s serial streams and the interface to the Protocol Processor is a quad 4-bit version of the Optical Internetworking Forum SFI-4 Specification. Figure 1 shows a simplified connection diagram to illustrate the example of the CRSU 4x2488 connected to a Protocol Processor.

Figure 1 2.488 Gbit/s Stream Pure SERDES Application



The PM5395 CRSU 4x2488 is applicable to equipment implementing SONET OC-48 or SDH STM-16 interfaces. Figure 2 shows the CRSU 4x2488 connected to the S/UNI-9953 OC-192 Physical Layer Device. The CRSU 4x2488 also directly connects to the SPECTRA-9953 SONET/SDH Payload Extractor Aligner for channelized OC-192 applications. In addition to bridging between the optical module and the SONET/SDH framer devices, the CRSU 4x2488 optionally performs SONET section and line layer or SDH regenerator and multiplex section performance monitoring. It provides clock and data recovery functions in the receive direction and clock synthesis functions in the transmit direction. The interfaces to the optical module are serial 2.488 Gbit/s streams and the interface to SONET/SDH framers is a quad 4-bit version of the Optical Internetworking Forum SFI-4 Specification.

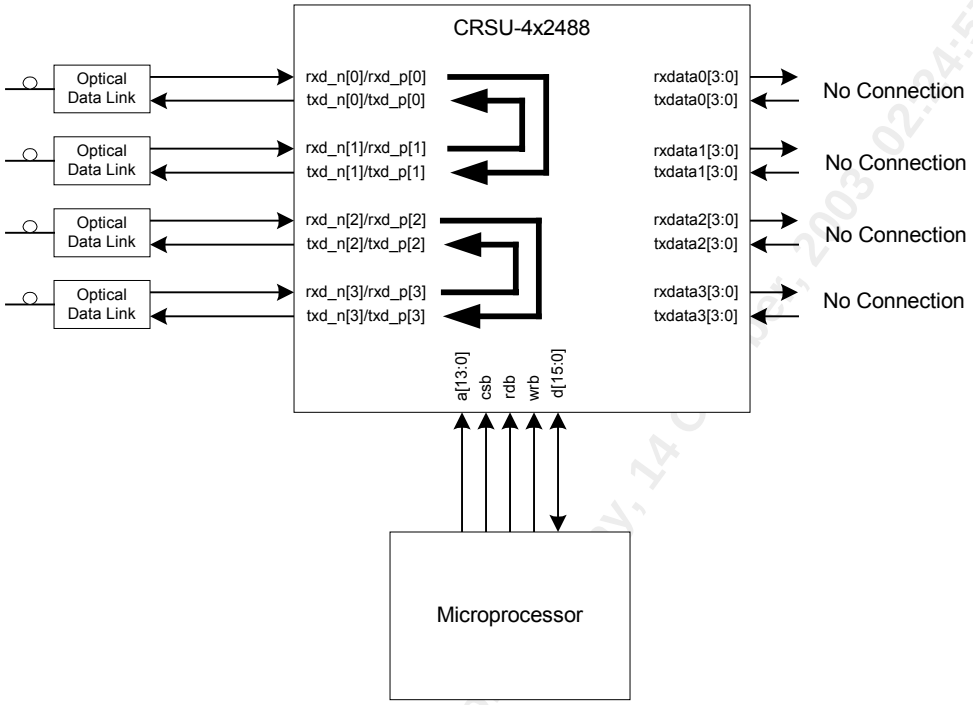
Figure 2 STS-48 (STM-16) SERDES Application



In a typical In-band Forward Error Correction (FEC) termination application, the CRSU 4x2488 performs clock and data recovery in the receive direction and clock synthesis in the transmit direction of the line interface. In addition, in the receive direction, errors in the received data stream are corrected using the FEC checksum bytes embedded in the SONET transport overhead or SDH section overhead bytes. In the transmit direction, FEC checksum bytes are inserted into the overhead bytes.

In a typical In-band Forward Error Correction (FEC) Line Regeneration Equipment (LRE) application as shown in Figure 3, the CRSU 4x2488 performs clock and data recovery in the receive direction and is loop timed in the transmit direction of the line interface. Errors in the received data stream are corrected using the FEC checksum bytes embedded in the SONET transport overhead or SDH section overhead bytes and it transmitted out the transmit line interface

Figure 3 STS-48 (STM-16) FEC Line Regeneration Equipment (LRE) Application



6 Block Diagram

Figure 4 Normal Operation

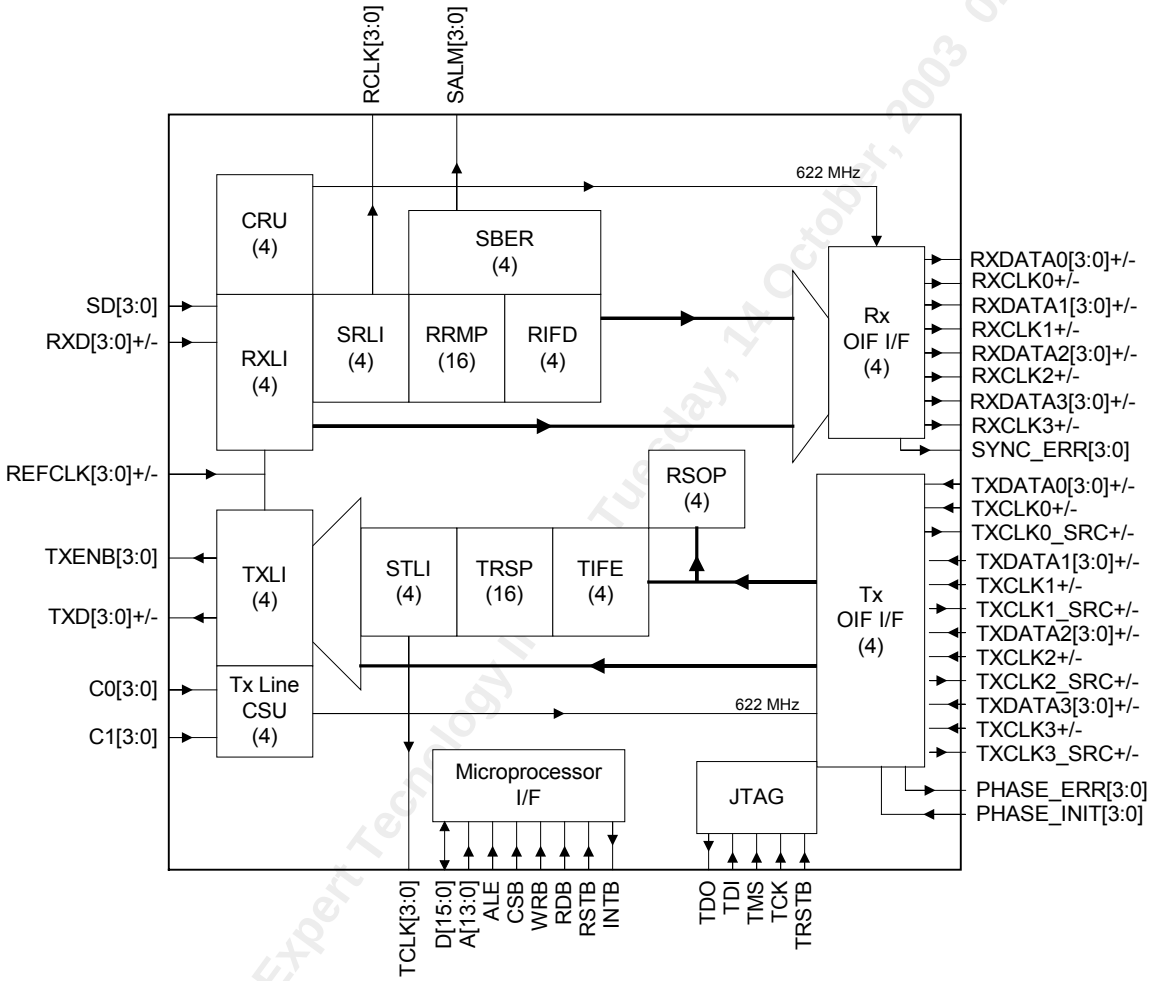
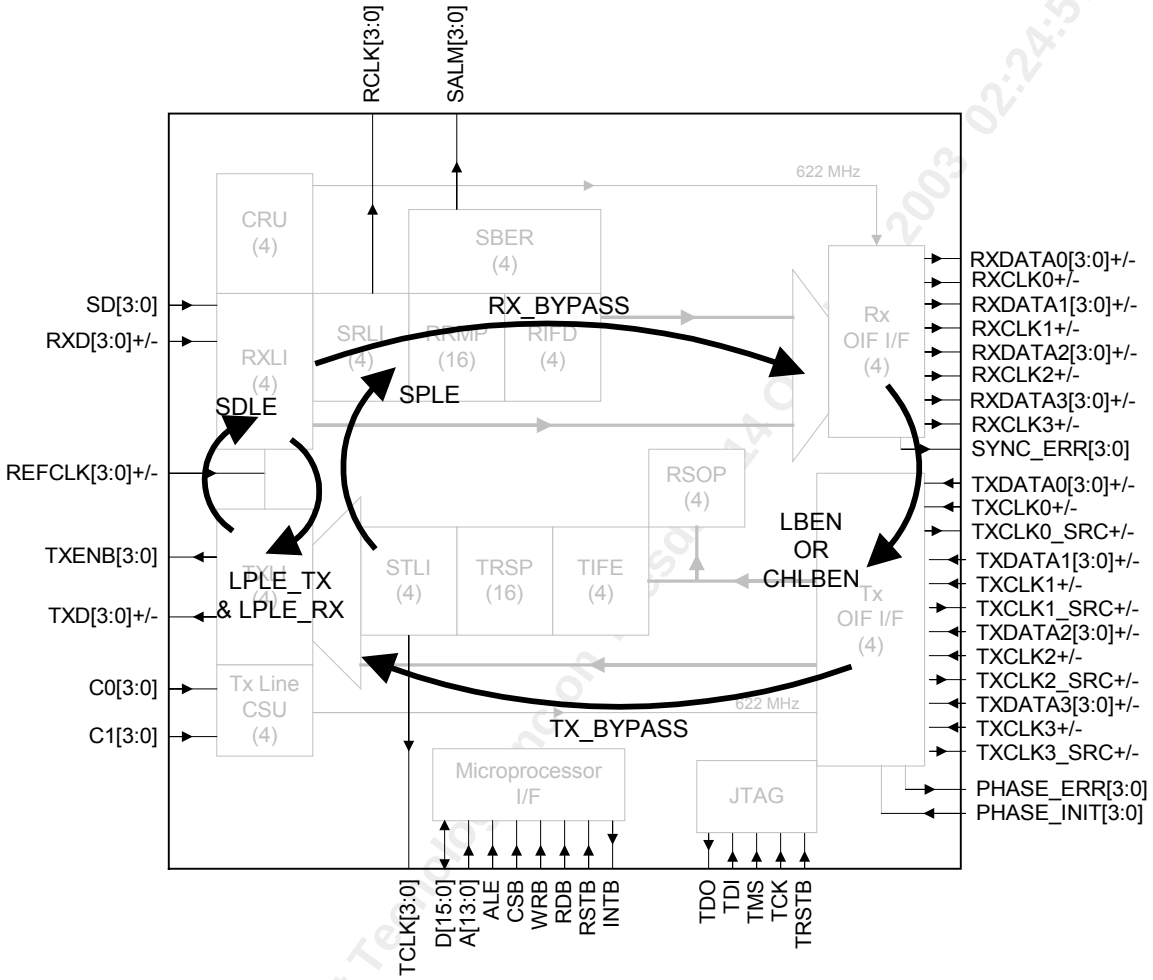


Figure 5 Loop-back and Bypass Operation Modes



7 Description

The PM5395 CRSU 4x2488 Quad Clock Recovery and Synthesis Unit Interface is a monolithic integrated circuit that bridges between the optical module and the SONET/SDH framer devices. It provides clock and data recovery functions in the receive direction and clock synthesis functions in the transmit direction. The interfaces to the optical module are serial 2.488 Gbit/s streams and the interface to SONET/SDH framers is a quad 4-bit version of the Optical Internetworking Forum SFI-4 Specification.

The CRSU 4x2488 receives SONET/SDH streams using a bit serial interface, recovers the clock and data and processes section and line overhead. The CRSU 4x2488 performs framing (A1, A2), de-scrambling, detects alarm conditions, and monitors section and line bit interleaved parity (B1, B2), accumulating error counts at each level for performance monitoring purposes. Line remote error indications (M1) are also accumulated. Optionally, the CRSU 4x2488 frames to the in-band forward error correction status indication byte and processes the checksum bytes. Detected errors are accumulated and corrected. Processing delay is limited to less than 15µs.

The CRSU–4x2488 transmits SONET/SDH streams using a bit serial interface. The CRSU 4x2488 synthesizes the transmit clock from a 155.52MHz frequency reference and performs framing pattern insertion (A1, A2), scrambling, alarm signal insertion, and creates section bit interleaved parity codes (B1) as required to allow performance monitoring at the far end. Optionally, the CRSU 4x2488 supports In-band FEC functions. FEC status indication bytes, and checksum bytes are inserted into the transport overhead bytes and the line BIP bytes are compensated to reflect the inserted checksum bytes. Processing delay is limited to less than 15µs. The CRSU 4x2488 also supports the insertion of a large variety of errors into the transmit stream, such as framing pattern errors, and bit interleaved parity errors which are useful for system diagnostics and tester applications.

For all modes no line rate clocks are required directly by the CRSU–4x2488 as it synthesizes the transmit clock and recovers the receive clock using a 155.52 MHz reference clock. The CRSU 4x2488 outputs a set of four differential PECL line data (TXD[3:0]+/-).

The CRSU–4x2488 is configured, controlled and monitored via a generic 16-bit microprocessor bus interface. The CRSU–4x2488 also provides a standard 5 signal IEEE 1149.1 JTAG test port for boundary scan board test purposes.

The CRSU–4x2488 is implemented in low power, +1.8 Volt, CMOS technology. It has TTL compatible digital inputs and TTL/CMOS compatible digital outputs. High speed inputs and outputs support 3.3V compatible pseudo-ECL (PECL) and CML, respectively. The CRSU–4x2488 is packaged in a 580 pin UBGA package.

The CRSU 4x2488 provides three main modes of operation, SERDES mode, PMON mode and Regenerator modes as shown in Table 2. In-band FEC is an optional feature that can be used in both the PMON and Regenerator modes.

Table 2 CRSU 4x2488 Modes of Operation

Operational Mode	Mode Description
SERDES Mode	Quad 2.488 Gbit/s serializer/deserializer
PMON Mode	Quad OC-48 (2.488 Gbit/s) serializer/deserializer with SONET/SDH overhead performance monitoring and optional Forward Error Correction
Regenerator Mode	Quad 2.488 Gbit/s serializer/deserializer with internal regenerator connection between channel 0 to channel 1 and channel 2 to channel 3 Performance monitoring (PMON Mode) and Forward Error Correction are optional for this mode.

SERDES Mode

In SERDES Mode, the CRSU 4x2488 provides clock recovery and synthesis for four independent bit-serial streams. In this mode, the CRSU 4x2488 can be used as a bridge between a SONET/SDH framer and other devices such as emerging G.709 framers. The CRSU 4x2488 connects to the framer or higher layer device via a quad 4-bit version of the OIF SFI-4 specification.

PMON Mode

The CRSU 4x2488 provides a PMON Mode to support DWDM and other applications that require optimized devices to perform SONET/SDH compliant data recovery as well as overhead performance monitoring. The CRSU–4x2488 receives SONET/SDH streams using a bit serial interface, recovers the clock and data and processes section and line overhead. The CRSU 4x2488 performs framing (A1, A2), de-scrambling, detects alarm conditions, and monitors section and line bit interleaved parity (B1, B2), accumulating error counts at each level for performance monitoring purposes. Line remote error indications (M1) are also accumulated. Optionally, the CRSU–4x2488 frames to the in-band forward error correction status indication byte and processes the checksum bytes. Detected errors are accumulated and corrected. Processing delay is limited to less than 15 µs.

The CRSU–4x2488 transmits SONET/SDH streams using a bit serial interface. The CRSU–4x2488 synthesizes the transmit clock from a 155.52 MHz frequency reference and performs framing pattern insertion (A1, A2), scrambling, alarm signal insertion, and creates section bit interleaved parity codes (B1) as required to allow performance monitoring at the far end. Optionally, the CRSU–4x2488 supports In-band FEC functions. FEC status indication bytes, and checksum bytes are inserted into the transport overhead bytes and the line BIP bytes are compensated to reflect the inserted checksum bytes. Processing delay is limited to less than 15µs. The CRSU–4x2488 also supports the insertion of a large variety of errors into the transmit stream, such as framing pattern errors, and bit interleaved parity errors which are useful for system diagnostics and tester applications.

Regenerator Mode

The CRSU 4x2488 provides a Regenerator Mode to support dense regenerator applications. In this mode, the CRSU 4x2488 provides an internal connection between channel 0 to channel 1 and from channel 2 to channel 3. The CRSU 4x2488 performs clock and data recovery in the receive direction and is loop timed in the transmit direction of the line interface. While in regenerator mode, the performance monitoring capability (PMON Mode) and Forward Error Correction functions may be utilized. These functions can be flexibly configured to allow conversion from OC-48 SONET/SDH streams on one side while supporting in-band forward error correction on the other side, processing delay is limited to less than 15.36µs.

Both PMON and Regenerator modes of the CRSU 4x2488 support in-band FEC according to ANSI-T1 letter ballot LB812. In-band FEC checksum bytes are inserted into the SONET Transport or SDH section overhead bytes in the transmit direction. In the receive direction, errors in the received data stream are corrected using the FEC checksum bytes embedded in the SONET transport overhead or the SDH section overhead bytes.

8 Pin Diagram

Table 3 CRSU 4x2488 Top Left Corner Pin-Out

	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19
A	vss	vss	vss	vss	vss	avdl_qs fim	vss	rxdata0 [1]+	rxdata0 [2]+	txclk_s rc0+	rxdata1 [1]+	rxdata1 [2]+	txclk_s rc1+	rxdata2 [1]+	rxdata2 [2]+	txclk_s rc2+
B	vss	vss	vss	vss	res	avdl_qs fim	vss	rxdata0 [1]-	rxdata0 [2]-	txclk_s cr0-	rxdata1 [1]-	rxdata1 [2]-	txclk_s rc1-	rxdata2 [1]-	rxdata2 [2]-	txclk_s rc2-
C	vss	vss	vss	vss	resk	VSS	rxdata0 [0]-	rxclk0-	rxdata0 [3]-	rxdata1 [0]-	rxclk1-	rxdata1 [3]-	rxdata2 [0]-	rxclk2-	rxdata2 [3]-	rxdata3 [0]-
D	vss	vss	vss	vss	avdh_qs fim	VSS	rxdata0 [0]+	rxclk0+	rxdata0 [3]+	rxdata1 [0]+	rxclk1+	rxdata1 [3]+	rxdata2 [0]+	rxclk2+	rxdata2 [3]+	rxdata3 [0]+
E	vss	vss	vss	vss	avdh_qs fim	avdl_qs fim	avdl_qs fim	avdh_qs fim	avdl_qs fim	avdh_qs fim	avdl_qs fim	avdh_qs fim	avdl_qs fim	avdh_qs fim	avdl_qs fim	avdh_qs fim
F	vddo	vddo	vddo	vddo	vddo											
G	d[15]	d[14]	d[13]	vddo	vddi											
H	d[12]	d[11]	d[9]	vddo	d[10]											
J	d[8]	d[7]	d[5]	d[6]	vddi											
K	d[4]	d[3]	d[1]	d[2]	vddo											
L	d[0]	csb	wrb	rdb	vddi											
M	ale	a[0]	vddo	a[2]	a[1]											
N	a[3]	a[4]	a[6]	a[5]	vddi											
P	a[7]	a[8]	a[11]	a[10]	a[9]											
R	vddo	a[12]	rstb	a[13]	vddi											
T	intb	NC	vddi	lcruto[0]	VSS											
U	vddo	vddo	vddo	vddo	vddo											

Table 4 CRSU 4x2488 Bottom Left Corner Pin-Out

V	c0[0]	c1[0]	avdh_cru_0	avdh_cru_0	avdh_cru_0											
W	vss	VSS	VSS	qavd	avdl_0											
Y	rxd[0]+	vss	avdh_cru_0	avdh_cru_0	avdh_cru_0											
AA	rxd[0]-	vss	vss	vss	avdl_0											
AB	vss	vss	avdh_tx_0	avdh_tx_0	avdh_tx_0											
AC	txd[0]-	vss	vss	vss	avdl_0											
AD	txd[0]+	vss	vss	vss	avdl_0											
AE	vss	vss	refclk[0]+	avdh_csu_0	avdh_csu_0											
AF	vss	vss	refclk[0]-	avdh_csu_0	avdh_csu_0											
AG	avdl_0	avdl_0	avdl_0	avdl_0	avdl_0											
AH	vss	vss	vss	vddi	vddi											
AJ	vss	vss	vss	vss	vss											
AK	vss	vss	vss	vss	vss	avdh_cru_1	avdl_1	avdh_cru_1	avdl_1	avdh_tx_1	avdl_1	avdl_1	avdh_csu_1	avdh_csu_1	vddo	vddi
AL	vss	vss	vss	vss	vss	avdh_cru_1	qavd	avdh_cru_1	vss	avdh_tx_1	vss	vss	avdh_csu_1	avdh_csu_1	avdl_1	lcruto[1]
AM	vss	vss	vss	vss	vss	avdh_cru_1	VSS	avdh_cru_1	vss	avdh_tx_1	vss	vss	refclk[1]+	refclk[1]-	avdl_1	lcruto[2]
AN	vss	vss	vss	vss	vss	c1[1]	VSS	vss	vss	vss	vss	vss	vss	vss	avdl_1	VSS
AP	vss	vss	vss	vss	vss	c0[1]	vss	rxd[1]+	rxd[1]-	vss	txd[1]-	txd[1]+	vss	vss	avdl_1	NC
	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19

Table 5 CRSU 4x2488 Top Right Corner Pin-Out

18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
rxdata3[1]+	rxdata3[2]+	vss	vddi	txdata0[1]+	txdata0[2]+	txdata1[0]+	txclk1+	txdata1[3]+	txdata2[1]+	txdata2[2]+	txdata3[0]+	txclk3+	vss	vss	vss	vss	vss	A
rxdata3[1]-	rxdata3[2]-	vddi	vddi	txdata0[1]-	txdata0[2]-	txdata1[0]-	txclk1-	txdata1[3]-	txdata2[1]-	txdata2[2]-	txdata3[0]-	txclk3-	vss	vss	vss	vss	vss	B
rxclk3-	rxdata3[3]-	txclk_src3+	txdata0[0]-	txclk0-	txdata0[3]-	txdata1[1]-	txdata1[2]-	txdata2[0]-	txclk2-	txdata2[3]-	txdata3[1]-	txdata3[2]-	txdata3[3]+	vss	vss	vss	vss	C
rxclk3+	rxdata3[3]+	txclk_src3-	txdata0[0]+	txclk0+	txdata0[3]+	txdata1[1]+	txdata1[2]+	txdata2[0]+	txclk2+	txdata2[3]+	txdata3[1]+	txdata3[2]+	txdata3[3]-	vss	vss	vss	vss	D
avdl_qsfim	avdh_qsfim	avdl_qsfim	avdl_qsfim	avdh_qsfim	avdl_qsfim	avdh_qsfim	avdl_qsfim	avdh_qsfim	avdl_qsfim	avdh_qsfim	avdl_qsfim	avdh_qsfim	avdl_qsfim	vss	vss	vss	vss	E
													vddo	vddo	vddo	vddo	vddo	F
													vddo	NC	sync_err[3]	sync_err[2]	sync_err[1]	G
													vddo	sync_err[0]	phase_init[3]	vddo	phase_init[2]	H
													phase_init[1]	phase_init[0]	vddo	phase_err[3]	phase_err[2]	J
													vddi	phase_err[1]	phase_err[0]	rclk[3]	vss	K
													rclk[2]	vddi	rclk[1]	rclk[0]	vss	L
													tclk[3]	tclk[2]	tclk[1]	vddi	tclk[0]	M
													salm[3]	salm[2]	vddi	salm[1]	vss	N
													vddo	salm[0]	tck	tms	vss	P
													tdi	tdo	vddi	trstb	vss	R
													NC	VSS	vddi	lcruto[3]	vss	T
													vddo	vddo	vddo	vddo	vddo	U

Table 6 CRSU 4x2488 Bottom Right Corner Pin-Out

													avdl_3	avdl_3	avdl_3	avdl_3	avdl_3	V
													avdh_csu_3	avdh_csu_3	refclk[3]-	vss	vss	W
													avdh_csu_3	avdh_csu_3	refclk[3]+	vss	vss	Y
													avdl_3	vss	vss	vss	txd[3]+	AA
													avdl_3	vss	vss	vss	txd[3]-	AB
													avdh_tx_3	avdh_tx_3	avdh_tx_3	vss	vss	AC
													avdl_3	vss	vss	vss	rxd[3]-	AD
													avdh_cru_3	avdh_cru_3	avdh_cru_3	vss	rxd[3]+	AE
													avdl_3	qavd	VSS	VSS	vss	AF
													avdh_cru_3	avdh_cru_3	avdh_cru_3	c1[3]	c0[3]	AG
													vss	vss	vss	vss	vss	AH
													vddi	vddi	vss	vss	vss	AJ
vddi	sd[1]	vddi	avdh_cru_2	avdl_2	avdh_cru_2	avdl_2	avdh_tx_2	avdl_2	avdl_2	avdh_csu_2	avdh_csu_2	avdl_2	vss	vss	vss	vss	vss	AK
vddi	sd[2]	txenb[2]	avdh_cru_2	qavd	avdh_cru_2	vss	avdh_tx_2	vss	vss	avdh_csu_2	avdh_csu_2	avdl_2	vss	vss	vss	vss	vss	AL
VSS	sd[3]	txenb[3]	avdh_cru_2	VSS	avdh_cru_2	vss	avdh_tx_2	vss	vss	refclk[2]+	refclk[2]-	avdl_2	vss	vss	vss	vss	vss	AM
NC	vddo	txenb[1]	c1[2]	VSS	vss	vss	vss	vss	vss	vss	vss	avdl_2	vss	vss	vss	vss	vss	AN
vddo	sd[0]	txenb[0]	c0[2]	vss	rxd[2]+	rxd[2]-	vss	txd[2]-	txd[2]+	vss	vss	avdl_2	vss	vss	vss	vss	vss	AP
18	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	

9 Pin Description

9.1 Serial Line Side Interface Signals (33)

Pin Name	Type	Pin No.	Function
REFCLK[3]+ REFCLK[3]- REFCLK[2]+ REFCLK[2]- REFCLK[1]+ REFCLK[1]- REFCLK[0]+ REFCLK[0]-	Differential PECL Input	Y3 W3 AM8 AM7 AM22 AM21 AE32 AF32	The differential **reference clock** inputs (REFCLK[3:0]+/-) provide a jitter-free 155.52 MHz nominal reference clock for both the clock recovery and the clock synthesis circuits for each of the four independent line interfaces. In practice, jitter on REFCLK_P / REFCLK_N inputs must be less than 1 psec RMS in 12KHz to 20MHz band in order for CRSU4x2488 to comply with Bellcore GR-253 intrinsic jitter specs on transmit data outputs. Note: Any jitter on REFCLK_P / REFCLK_N up to about 20 MHz will also appear at the transmit data output. Please refer to the Operation section for a discussion of PECL interfacing issues.
RXD[3]+ RXD[3]- RXD[2]+ RXD[2]- RXD[1]+ RXD[1]- RXD[0]+ RXD[0]-	Differential PECL Input	AE1 AD1 AP13 AP12 AP27 AP26 Y34 AA34	The **receive differential data** PECL inputs (RXD[3:0]+/-) contain the four NRZ bit serial receive streams. Each of four receive clocks is recovered from the corresponding RXD[3:0]+/- bit stream. The receive inputs are internally terminated with differential 100-Ω termination. Please refer to the Operation section for a discussion of PECL interfacing issues.
TXD[3]+ TXD[3]- TXD[2]+ TXD[2]- TXD[1]+ TXD[1]- TXD[0]+ TXD[0]-	Differential CML Output	AA1 AB1 AP9 AP10 AP23 AP24 AD34 AC34	The **transmit differential data** CML outputs (TXD[3:0]+/-) contain the set of four 2488.32 Mbit/s nominal transmit streams. Each of the four TXD+/- outputs is driven using the synthesized clock from the corresponding CSU. Signal swing is 2/3rd of standard PECL and is compatible with the requirements of most Optical Modules.
SD[3] SD[2] SD[1] SD[0]	TTL Input	AM17 AL17 AK17 AP17	The receive **signal detect** TTL inputs (SD[3:0]) indicates the presence of valid receive signal power from the Optical Physical Medium Dependent Device associated with the corresponding receive differential data PECL inputs (RXD[3:0]+/-). Logic high indicates the presence of valid data. A logic low indicates a loss of signal.
TXENB[3] TXENB[2] TXENB[1] TXENB[0]	TTL Output	AM16 AL16 AN16 AP16	The **transmit enable** TTL outputs (TXENB[3:0]) controls downstream optical modules. The TXENB[3:0] signals reflect the value written to the TX_ENB[3:0] register bits. When TXENB[*X*] is set low, the associated optical module is enabled. When TXENB[*X*] is set high, the associated optical module is disabled. TXENB[3:0] are asynchronous outputs.
NC		G4	No Connect. This pin should be left unconnected.

9.2 Clocks and Alarms (12)

Pin Name	Type	Pin No.	Function
RCLK[3] RCLK[2] RCLK[1] RCLK[0]	Output	K2 L5 L3 L2	The **receive clock** (RCLK[3:0]) signals provide timing reference for the four independent receive interfaces. Each RCLK[X] is equal to the RXD[X] recovered clock divided by 32 (nominal 77.76 MHz 50% duty cycle clock). **NOTE: RCLK[*X*] is by default disabled, it can be enabled by programming the RCLKEN bit to logic '1' in the corresponding Receive SRLI Clock Configuration register 1110H, 1310H, 1510H , 1710H and KILL_RX_CLK[x] register 000EH to logic '0'.** **This clock is derived from a digital source and may be subject to jitter. Out of spec data frequency will cause unstable clock, see section 13.2.2**
TCLK[3] TCLK[2] TCLK[1] TCLK[0]	Output	M5 M4 M3 M1	The **transmit clock** (TCLK[3:0]) signals provide timing reference for the four independent transmit line interfaces. TCLK[*X*] is equal to the TXD[X] data clock frequency divided by 32 (nominal 77.76MHz 50% duty cycle clock). **NOTE: TCLK[*X*] is by default disabled, it can be enabled by programming the TCLKEN bit to logic '1' in the corresponding STLI PGM Clock Configuration register 1090H, 1290H, 1490H, 1690H and KILL_TX_CLK[x] register 000EH to logic '0'.** **This clock is derived from a digital source and may be subject to jitter.**
SALM[3] SALM[2] SALM[1] SALM[0]	Output	N5 N4 N2 P4	The **section alarm** (SALM[3:0]) signals report alarms in the four independent receive interfaces. SALM[*X*] is configurable to be set high when an out of frame (OOF), loss of signal (LOS), loss of frame (LOF), line alarm indication signal (AIS-L), line remote defect indication (RDI-L), signal fail (SF) or signal degrade (SD) alarm is detected. Each alarm indication can be independently enabled using register bits in the corresponding SALM Enables Master Register 0011H and 0012H. SALM is set low when none of the enabled alarms is active.

9.3 System Side Interface Signals (100)

Pin Name	Type	Pin No.	Function
RXDATA0[3]+ RXDATA0[3]- RXDATA0[2]+ RXDATA0[2]- RXDATA0[1]+ RXDATA0[1]- RXDATA0[0]+ RXDATA0[0]-	Analog LVDS Output	D26 C26 A26 B26 A27 B27 D28 C28	The **channel 0 receive data** (RXDATA0[3:0]+/-) signals carry the data received on the serial line interface channel 0 (RXD[0]+/-). When SONET/SDH framing is used RXDATA0[3]+/- is the most significant bit (corresponding to bit 1 and bit 5 of each SONET/SDH octet, the first and fifth bit transmitted). RXDATA0[0]+/- is the least significant bit (corresponding to bit 4 and bit 8 of each octet, the fourth and last bit transmitted). When SONET/SDH framing is not used by setting the RX_BYPASS_CH[0] register bit to logic '1', RXDATA0[3]+/- is the first and fifth bit transmitted, while RXDATA0[0]+/- is the last bit transmitted. The choice to nibble boundaries in relation to the serial data stream RXD[0]+/- is arbitrary. RXDATA0[3:0]+/- is updated on the rising edge of RXCLK0+/-.
RXCLK0+ RXCLK0-	Analog LVDS Output	D27 C27	The **channel 0 receive clock** (RXCLK0+/-) signal provide timing reference for the channel 0 receive data stream. RXCLK0+/- is a nominal 622.08 MHz, 50% duty cycle clock that is a divide by 4 of the line rate clock recovered from RXD[0]+/-. The RXDATA0[3:0]+/- signals are updated on the rising edge of RXCLK0+/-. **NOTE: out of spec data frequency will cause unstable clock, see section 13.2.2**
RXDATA1[3]+ RXDATA1[3]- RXDATA1[2]+ RXDATA1[2]- RXDATA1[1]+ RXDATA1[1]- RXDATA1[0]+ RXDATA1[0]-	Analog LVDS Output	D23 C23 A23 B23 A24 B24 D25 C25	The **channel 1 receive data** (RXDATA1[3:0]+/-) signals carry the data received on the serial line interface channel 1 (RXD[1]+/-). When SONET/SDH framing is used RXDATA1[3]+/- is the most significant bit (corresponding to bit 1 and bit 5 of each SONET/SDH octet, the first and fifth bit transmitted). RXDATA1[0]+/- is the least significant bit (corresponding to bit 4 and bit 8 of each octet, the fourth and last bit transmitted). When SONET/SDH framing is not used by setting the RX_BYPASS_CH[1] register bit to logic '1', RXDATA1[3]+/- is the first and fifth bit transmitted, while RXDATA1[0]+/- is the last bit transmitted. The choice to nibble boundaries in relation to the serial data stream RXD[1]+/- is arbitrary. RXDATA1[3:0]+/- is updated on the rising edge of RXCLK1+/-.

Pin Name	Type	Pin No.	Function
RXCLK1+ RXCLK1-	Analog LVDS Output	D24 C24	The **channel 1 receive clock** (RXCLK1+/-) signal provide timing reference for the channel 1 receive data stream. RXCLK1 is a nominal 622.08 MHz, 50% duty cycle clock that a divide by 4 of the line rate clock recovered from RXD[1]+/-. The RXDATA1[3:0]+/- signals are updated on the rising edge of RXCLK1+/-. **NOTE: out of spec data frequency will cause unstable clock, see section 13.2.2**
RXDATA2[3]+ RXDATA2[3]- RXDATA2[2]+ RXDATA2[2]- RXDATA2[1]+ RXDATA2[1]- RXDATA2[0]+ RXDATA2[0]-	Analog LVDS Output	D20 C20 A20 B20 A21 B21 D22 C22	The **channel 2 receive data** (RXDATA2[3:0]+/-) signals carry the data received on the serial line interface channel 2 (RXD[2]+/-). When SONET/SDH framing is used RXDATA2[3]+/- is the most significant bit (corresponding to bit 1 and bit 5 of each SONET/SDH octet, the first and fifth bit transmitted). RXDATA2[0]+/- is the least significant bit (corresponding to bit 4 and bit 8 of each octet, the fourth and last bit transmitted). When SONET/SDH framing is not used by setting the RX_BYPASS_CH[2] register bit to logic '1', RXDATA2[3]+/- is the first and fifth bit transmitted, while RXDATA2[0]+/- is the last bit transmitted. The choice to nibble boundaries in relation to the serial data stream RXD[2]+/- is arbitrary. RXDATA2[3:0]+/- is updated on the rising edge of RXCLK2+/-.
RXCLK2+ RXCLK2-	Analog LVDS Output	D21 C21	The **channel 2 receive clock** (RXCLK2+/-) signal provide timing reference for the channel 2 receive data stream. RXCLK1 is a nominal 622.08 MHz, 50% duty cycle clock that a divide by 4 of the line rate clock recovered from RXD[2]+/-. The RXDATA2[3:0]+/- signals are updated on the rising edge of RXCLK2+/-. **NOTE: out of spec data frequency will cause unstable clock, see section 13.2.2**
RXDATA3[3]+ RXDATA3[3]- RXDATA3[2]+ RXDATA3[2]- RXDATA3[1]+ RXDATA3[1]- RXDATA3[0]+ RXDATA3[0]-	Analog LVDS Output	D17 C17 A17 B17 A18 B18 D19 C19	The **channel 3 receive data** (RXDATA3[3:0]+/-) signals carry the data received on the serial line interface channel 3 (RXD[3]+/-). When SONET/SDH framing is used RXDATA3[3]+/- is the most significant bit (corresponding to bit 1 and bit 5 of each SONET/SDH octet, the first and fifth bit transmitted). RXDATA3[0]+/- is the least significant bit (corresponding to bit 4 and bit 8 of each octet, the fourth and last bit transmitted). When SONET/SDH framing is not used by setting the RX_BYPASS_CH[3] register bit to logic '1', RXDATA3[3]+/- is the first and fifth bit transmitted, while RXDATA3[0]+/- is the last bit transmitted. The choice to nibble boundaries in relation to the serial data stream RXD[3]+/- is arbitrary. RXDATA3[3:0]+/- is updated on the rising edge of RXCLK3+/-.

Pin Name	Type	Pin No.	Function
RXCLK3+ RXCLK3-	Analog LVDS Output	D18 C18	The **channel 3 receive clock** (RXCLK3+/-) signal provide timing reference for the channel 3 receive data stream. RXCLK3+/- is a nominal 622.08 MHz, 50% duty cycle clock that is a divide by 4 of the line rate clock recovered from RXD[3]+/-. The RXDATA3[3:0]+/- signals are updated on the rising edge of RXCLK3+/-. **NOTE: out of spec data frequency will cause unstable clock, see section 13.2.2**
TXCLK_SRC0+ TXCLK_SRC0-	Analog LVDS Output	A25 B25	The **channel 0 transmit source clock** (TXCLK_SRC[0]+/-) signal provide timing reference for the channel 0 transmit data stream. TXCLK_SRC[0]+/- is nominal 622.08 MHz, 50% duty cycle clock that is a divide by 4 of the line rate clock used to time TXD[0]+/-. It is expected that an upstream device would use TXCLK_SRC[0]+/- as timing reference for TXCLK0+/- and TXDATA0[3:0]+/-.
TXCLK0+ TXCLK0-	Analog LVDS Input	D14 C14	The **channel 0 transmit clock** (TXCLK0+/-) signal provide timing reference for the channel 0 transmit data stream. TXCLK0+/- is a nominal 622.08 MHz, 50% duty cycle clock that is a divide by 4 of the line rate clock used to time TXD[0]+/-. It is expected that TXCLK0+/- is a buffered version of TXCLK_SRC[0]+/-. The TXDATA0[3:0]+/- signals are sampled on the rising edge of TXCLK0+/-.
TXDATA0[3]+ TXDATA0[3]- TXDATA0[2]+ TXDATA0[2]- TXDATA0[1]+ TXDATA0[1]- TXDATA0[0]+ TXDATA0[0]-	Analog LVDS Input	D13 C13 A13 B13 A14 B14 D15 C15	The **channel 0 transmit data** (TXDATA0[3:0]+/-) signals carry the data to be transmitted on the serial line interface channel 0 (TXD[0]+/-). When SONET/SDH framing is used TXDATA0[3]+/- is the most significant bit (corresponding to bit 1 and bit 5 of each SONET/SDH octet, the first and fifth bit received, for example). TXDATA0[0]+/- is the least significant bit (corresponding to bit 4 and bit 8 of each octet, the fourth and last bit received, for example). The actual nibble boundaries in relation to the serial data stream TXD[0]+/- is arbitrary. When SONET/SDH framing is not used by setting the enabling the setting the TX_BYPASS_CH[0] register bit to logic '1', TXDATA0[3]+/- is the first and fifth bit received, while TXDATA0[0]+/- is the last bit received. The choice to nibble boundaries in relation to the serial data stream TXD[0]+/- is arbitrary. TXDATA0[3:0]+/- is sampled on the rising edge of TXCLK0+/-.

Pin Name	Type	Pin No.	Function
TXCLK_SRC1+ TXCLK_SRC1-	Analog LVDS Output	A22 B22	The **channel 1 transmit source clock** (TXCLK_SRC[1]+/-) signal provide timing reference for the channel 1 transmit data stream. TXCLK_SRC[1]+/- is nominal 622.08 MHz, 50% duty cycle clock that is a divide by 4 of the line rate clock used to time TXD[1]+/-. It is expected that an upstream device would use TXCLK_SRC[1]+/- as timing reference for TXCLK1+/- and TXDATA1[3:0]+/-.
TXCLK1+ TXCLK1-	Analog LVDS Input	A11 B11	The **channel 1 transmit clock** (TXCLK1+/-) signal provide timing reference for the channel 1 transmit data stream. TXCLK1+/- is a nominal 622.08 MHz, 50% duty cycle clock that is a divide by 4 of the line rate clock used to time TXD[1]+/-. It is expected that TXCLK1+/- is a buffered version of TXCLK_SRC[1]+/-. The TXDATA1[3:0]+/- signals are sampled on the rising edge of TXCLK1+/-.
TXDATA1[3]+ TXDATA1[3]- TXDATA1[2]+ TXDATA1[2]- TXDATA1[1]+ TXDATA1[1]- TXDATA1[0]+ TXDATA1[0]-	Analog LVDS Input	A10 B10 D11 C11 D12 C12 A12 B12	The **channel 1 transmit data** (TXDATA1[3:0]+/-) signals carry the data to be transmitted on the serial line interface channel 1 (TXD[1]+/-). When SONET/SDH framing is used TXDATA1[3]+/- is the most significant bit (corresponding to bit 1 and bit 5 of each SONET/SDH octet, the first and fifth bit received, for example). TXDATA1[0]+/- is the least significant bit (corresponding to bit 4 and bit 8 of each octet, the fourth and last bit received, for example). The actual nibble boundaries in relation to the serial data stream TXD[1]+/- is arbitrary. When SONET/SDH framing is not used by setting the enabling the setting the TX_BYPASS_CH[1] register bit to logic '1', TXDATA1[3]+/- is the first and fifth bit received, while TXDATA1[0]+/- is the last bit received. The choice to nibble boundaries in relation to the serial data stream TXD[1]+/- is arbitrary. TXDATA1[3:0]+/- is sampled on the rising edge of TXCLK1+/-.
TXCLK_SRC2+ TXCLK_SRC2-	Analog LVDS Output	A19 B19	The **channel 2 transmit source clock** (TXCLK_SRC[2]+/-) signal provide timing reference for the channel 2 transmit data stream. TXCLK_SRC[2]+/- is nominal 622.08 MHz, 50% duty cycle clock that is a divide by 4 of the line rate clock used to time TXD[2]+/-. It is expected that an upstream device would use TXCLK_SRC[2]+/- as timing reference for TXCLK2+/- and TXDATA2[3:0]+/-.

Pin Name	Type	Pin No.	Function
TXCLK2+ TXCLK2-	Analog LVDS Input	D9 C9	The **channel 2 transmit clock** (TXCLK2+/-) signal provide timing reference for the channel 2 transmit data stream. TXCLK2+/- is a nominal 622.08 MHz, 50% duty cycle clock that is a divide by 4 of the line rate clock used to time TXD[2]+/-. It is expected that TXCLK2+/- is a buffered version of TXCLK_SRC[2]+/-. The TXDATA2[3:0]+/- signals are sampled on the rising edge of TXCLK2+/-.
TXDATA2[3]+ TXDATA2[3]- TXDATA2[2]+ TXDATA2[2]- TXDATA2[1]+ TXDATA2[1]- TXDATA2[0]+ TXDATA2[0]-	Analog LVDS Input	D8 C8 A8 B8 A9 B9 D10 C10	The **channel 2 transmit data** (TXDATA2[3:0]+/-) signals carry the data to be transmitted on the serial line interface channel 2 (TXD[2]+/-). When SONET/SDH framing is used TXDATA2[3]+/- is the most significant bit (corresponding to bit 1 and bit 5 of each SONET/SDH octet, the first and fifth bit received, for example). TXDATA2[0]+/- is the least significant bit (corresponding to bit 4 and bit 8 of each octet, the fourth and last bit received, for example). The actual nibble boundaries in relation to the serial data stream TXD[2]+/- is arbitrary. When SONET/SDH framing is not used by setting the enabling the setting the TX_BYPASS_CH[2] register bit to logic '1', TXDATA2[3]+/- is the first and fifth bit received, while TXDATA2[0]+/- is the last bit received. The choice to nibble boundaries in relation to the serial data stream TXD[2]+/- is arbitrary. TXDATA2[3:0]+/- is sampled on the rising edge of TXCLK2+/-.
TXCLK_SRC3+ TXCLK_SRC3-	Analog LVDS Output	C16 D16	The **channel 3 transmit source clock** (TXCLK_SRC[3]+/-) signal provide timing reference for the channel 3 transmit data stream. TXCLK_SRC[3]+/- is nominal 622.08 MHz, 50% duty cycle clock that is a divide by 4 of the line rate clock used to time TXD[3]+/-. It is expected that an upstream device would use TXCLK_SRC[3]+/- as timing reference for TXCLK3+/- and TXDATA3[3:0]+/-.
TXCLK3+ TXCLK3-	Analog LVDS Input	A6 B6	The **channel 3 transmit clock** (TXCLK3+/-) signal provide timing reference for the channel 3 transmit data stream. TXCLK3+/- is a nominal 622.08 MHz, 50% duty cycle clock that is a divide by 4 of the line rate clock used to time TXD[3]+/-. It is expected that TXCLK3+/- is a buffered version of TXCLK_SRC[3]+/-. The TXDATA3[3:0]+/- signals are sampled on the rising edge of TXCLK3+/-.

Pin Name	Type	Pin No.	Function
TXDATA3[3]+ TXDATA3[3]- TXDATA3[2]+ TXDATA3[2]- TXDATA3[1]+ TXDATA3[1]- TXDATA3[0]+ TXDATA3[0]-	Analog LVDS Input	C5 D5 D6 C6 D7 C7 A7 B7	The **channel 3 transmit data** (TXDATA3[3:0]+/-) signals carry the data to be transmitted on the serial line interface channel 3 (TXD[3]+/-). When SONET/SDH framing is used TXDATA3[3]+/- is the most significant bit (corresponding to bit 1 and bit 5 of each SONET/SDH octet, the first and fifth bit received, for example). TXDATA3[0]+/- is the least significant bit (corresponding to bit 4 and bit 8 of each octet, the fourth and last bit received, for example). The actual nibble boundaries in relation to the serial data stream TXD[3]+/- is arbitrary. When SONET/SDH framing is not used by setting the enabling the setting the TX_BYPASS_CH[3] register bit to logic '1', TXDATA3[3]+/- is the first and fifth bit received, while TXDATA3[0]+/- is the last bit received. The choice to nibble boundaries in relation to the serial data stream TXD[3]+/- is arbitrary. TXDATA3[3:0]+/- is sampled on the rising edge of TXCLK3+/-.
SYNC_ERR[3] SYNC_ERR[2] SYNC_ERR[1] SYNC_ERR[0]	Output	G3 G2 G1 H4	The **synchronization error** signal indicates the associated RXCLK[3:0]+/- clock signal is not derived from the associated RXD[3:0]+/- input signal. This signal follows the state of the SD[3:0] input signals from the optical modules as well as the CRU Data Out of Lock signal. The SYNC_ERR[3:0] can be disabled by setting the SYNC_ERR_EN_CH[n] bit in the TXENB Control register 0013H to logic '0'. The SYNC_ERR[3:0] inversion bit in the Configuration and Clock Monitor register 000BH can invert the polarity of all the SYNC_ERR[3:0] output pins. After a reset the SYNC_ERR[3:0] pins are enabled and set to logic '1'.
PHASE_INIT[3] PHASE_INIT[2] PHASE_INIT[1] PHASE_INIT[0]	Input	H3 H1 J5 J4	The **phase initialization** signals indicate if the phase relationship between the TXDATA and TXCLK is stable and can be locked in, allowing for the greatest tolerance to phase shift during operation. When PHASE_INIT[3:0] is set to logic one the associated channel FIFO is re-centered, holding fifo read and write pointers to the same location. The operation of PHASE_INIT[3:0] is controlled by the PHASE_EN bit in the QSFIM_2488 Control Register 1001H, 1201H, 1401H and 1601H.
PHASE_ERR[3] PHASE_ERR[2] PHASE_ERR[1] PHASE_ERR[0]	Output	J2 J1 K4 K3	A **phase error** signals indicate if the phase relationship between the TXDATA and TXCLK has exceed the limits of the FIFO and has cause the FIFO to overflow or underflow. When the PHASE_ERR[3:0] is set to logic one the associated channel has had a FIFO error. Once PHASE_ERR[3:0] is assert it will remain asserted until cleared by either the associated PHASE_INIT[3:0] signal or by reading the QSFIM_2488 Status register 1000H, 1200H, 1400H and 1600H.

9.4 Microprocessor Interface Signals (36)

Pin Name	Type	Pin No.	Function
CSB	Input	L33	The active low **chip select** (CSB) signal is low during CRSU 4x2488 register accesses. If CSB is not required (i.e. register accesses controlled using the RDB and WRB signals only), CSB must be connected to an inverted version of the RSTB input.
RDB	Input	L31	The active low **read enable** (RDB) signal is low during a CRSU 4x2488 read access. The CRSU 4x2488 drives the D[15:0] bus with the contents of the addressed register while RDB and CSB are low.
WRB	Input	L32	The active low **write strobe** (WRB) signal is low during a CRSU 4x2488 register write access. The D[15:0] bus contents are clocked into the addressed register on the rising WRB edge while CSB is low.
D[15] D[14] D[13] D[12] D[11] D[10] D[9] D[8] D[7] D[6] D[5] D[4] D[3] D[2] D[1] D[0]	I/O	G34 G33 G32 H34 H33 H30 H32 J34 J33 J31 J32 K34 K33 K31 K32 L34	The bi-directional **data bus**, D[15:0], is used during CRSU 4x2488 read and write accesses.
A[13]	Input	R31	The **address** bit 13 is used as the **test register select** signal which selects between normal and test mode register accesses. When A[13] is high, the value on the A[12:0] selects a test register access. When A[13] is low, normal mode register accesses are enabled. For normal operation A[13] may be tied low.
A[12] A[11] A[10] A[9] A[8] A[7] A[6] A[5] A[4] A[3] A[2] A[1] A[0]	Input	R33 P32 P31 P30 P33 P34 N32 N31 N33 N34 M31 M30 M33	The **address** bus (A[12:0]) selects specific registers during CRSU 4x2488 register accesses.
RSTB	Schmidt TTL Input	R32	The active low **reset** (RSTB) signal provides an asynchronous CRSU 4x2488 reset. RSTB is a Schmidt triggered input with an integral pull-up resistor.

Pin Name	Type	Pin No.	Function
ALE	Input	M34	The **address latch enable** (ALE) is an active-high signal and latches the address bus A[15:0] when low. When ALE is high, the internal address latches are transparent. It allows the CRSU 4x2488 to interface to a multiplexed address/data bus. The ALE input has an integral pull up resistor.
INTB	OD Output	T34	The active low **interrupt** (INTB) is set low when a CRSU 4x2488 enabled interrupt source is active. CRSU 4x2488 may be enabled to report many alarms or events via interrupts. INTB is tri-stated when the interrupt is acknowledged via the appropriate register access. INTB is an open drain output.

9.5 JTAG Test Access Port (TAP) Signals (5)

Pin Name	Type	Pin No.	Function
TCK	Input	P3	The **test clock** (TCK) signal provides timing for test operations that can be carried out using the IEEE P1149.1 test access port.
TMS	Input	P2	The **test mode select** (TMS) signal controls the test operations that can be carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an integral pull up resistor.
TDI	Input	R5	When the CRSU 4x2488 is configured for JTAG operation, the **test data input** (TDI) signal carries test data into the CRSU 4x2488 via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an integral pull up resistor.
TDO	Tri-state Output	R4	The **test data output** (TDO) signal carries test data out of the CRSU 4x2488 via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tri-state output which is inactive except when scanning of data is in progress.
TRSTB	Schmidt TTL Input	R2	The active low **test reset** (TRSTB) signal provides an asynchronous CRSU 4x2488 test access port reset via the IEEE P1149.1 test access port. TRSTB is a Schmidt triggered input with an integral pull up resistor. In the event that TRSTB is not used, it must be connected to RSTB.

9.6 Analog Miscellaneous Signals (32)

Pin Name	Type	Pin No.	Function
VSS	Analog Signal	D29 C29 AF2 AF3 AN14 AM14 AN28 AM28 W33 W32	These pins must be tied to ground during normal operation.

Pin Name	Type	Pin No.	Function
C0[3] C1[3] C0[2] C1[2] C0[1] C1[1] C0[0] C1[0]	Analog Signal	AG1 AG2 AP15 AN15 AP29 AN29 V34 V33	The **analog clock synthesis capacitor port** (C0[3:0] and C1[3:0]) pins are provided for the four independent transmit serial streams that must meet SONET/SDH jitter transfer specifications. A 100 nF non-polarized capacitor is attached across C0[*X*] and C1[*X*].
NC	Output	T5 AN18 AP19 T33	No Connect. These pins should be left unconnected.
VSS	Input	T4 AM18 AN19 T30	Must be connected to ground during normal mode operation.
LCRUTO[3] LCRUTO[2] LCRUTO[1] LCRUTO[0]	Output	T2 AM19 AL19 T31	155Mhz **recovered clock** (LCRUTO [3:0]) signals provide timing reference for the four independent receive interfaces. Each LCRUTO [[X] is equal to the RXD[X] recovered clock divided by 16 (nominal 155.56 MHz 50% duty cycle clock). Derived directly from the clock recovery unit(CRU). Provides a clock reference, subject to less jitter than RCLK[3:0] **(divide-by-32, 77.76 MHz)**. **NOTE: LCRUTO[*X*] is by default disabled, it can be enabled by programming the LCRUTO_EN_CHx bit to logic '1' in register 0013H.**
RES RESK	Analog Signal	B30 C30	An off-chip 3.16k ohm ±1% resistor is connected between the positive resistor reference pin RES and a Kelvin ground contact RESK for the QSFI-4 LVDS reference circuitry. An on-chip negative feedback path will force an internal 0.80V reference voltage onto RES, therefore forcing 252 uA of current to flow through the resistor.

9.7 Analog Power (120)

Pin Name	Pin Type	PIN No.	Function
QAVD (4)	Analog Power	AF4 AL14 AL28 W31	The **quiet power** (QAVD) pins for the analog core. QAVD should be connected to well-decoupled analog +3.3V supply. Please see the Operation section for detailed information.
AVDH_CRU_0 (6)	Analog Power	Y32 Y31 Y30 V32 V31 V30	The 3.3 volt **analog power** (AVDH) pins for the channel 0 PECL data receiver, Clock Recovery Unit (CRU) and Recovered Jitter Attenuator. The AVDH_CRU_0 pins should be connected through passive filtering networks to a well-decoupled +3.3V analog power supply. Please see the Operation section for detailed information.

Pin Name	Pin Type	PIN No.	Function
AVDH_CRU_1 (6)	Analog Power	AM27 AL27 AK27 AM29 AL29 AK29	The 3.3 volt **analog power** (AVDH) pins for the channel 1 PECL data receiver, Clock Recovery Unit (CRU) and Recovered Jitter Attenuator. The AVDH_CRU_1 pins should be connected through passive filtering networks to a well-decoupled +3.3V analog power supply. Please see the Operation section for detailed information.
AVDH_CRU_2 (6)	Analog Power	AM13 AL13 AK13 AM15 AL15 AK15	The 3.3 volt **analog power** (AVDH) pins for the channel 2 PECL data receiver, Clock Recovery Unit (CRU) and Recovered Jitter Attenuator. The AVDH_CRU_2 pins should be connected through passive filtering networks to a well-decoupled +3.3V analog power supply. Please see the Operation section for detailed information.
AVDH_CRU_3 (6)	Analog Power	AE5 AE4 AE3 AG4 AG3 AG5	The 3.3 volt **analog power** (AVDH) pins for the channel 3 PECL data receiver, Clock Recovery Unit (CRU) and Recovered Jitter Attenuator. The AVDH_CRU_3 pins should be connected through passive filtering networks to a well-decoupled +3.3V analog power supply. Please see the Operation section for detailed information.
AVDH_TX_0 (3)	Analog Power	AB32 AB31 AB30	The 3.3 volt **analog power** (AVDH) pins for the channel 0 PECL data Transmitter. The AVDH_TX_0 pins should be connected through passive filtering networks to a well-decoupled +3.3V analog power supply. Please see the Operation section for detailed information.
AVDH_TX_1 (3)	Analog Power	AM25 AL25 AK25	The 3.3 volt **analog power** (AVDH) pins for the channel 1 PECL data Transmitter. The AVDH_TX_1 pins should be connected through passive filtering networks to a well-decoupled +3.3V analog power supply. Please see the Operation section for detailed information.
AVDH_TX_2 (3)	Analog Power	AM11 AL11 AK11	The 3.3 volt **analog power** (AVDH) pins for the channel 2 PECL data Transmitter. The AVDH_TX_2 pins should be connected through passive filtering networks to a well-decoupled +3.3V analog power supply. Please see the Operation section for detailed information.
AVDH_TX_3 (3)	Analog Power	AC5 AC4 AC3	The 3.3 volt **analog power** (AVDH) pins for the channel 3 PECL data Transmitter. The AVDH_TX_3 pins should be connected through passive filtering networks to a well-decoupled +3.3V analog power supply. Please see the Operation section for detailed information.
AVDH_CSU_0 (4)	Analog Power	AF31 AF30 AE31 AE30	The 3.3 volt **analog power** (AVDH) pins for the channel 0 PECL Clock Synthesizer Unit (CSU) and PECL Reference Clock Receiver. The AVDH_CSU_0 pins should be connected through passive filtering networks to a well-decoupled +3.3V analog power supply. Please see the Operation section for detailed information.

Pin Name	Pin Type	PIN No.	Function
AVDH_CSU_1 (4)	Analog Power	AL21 AK21 AL22 AK22	The 3.3 volt **analog power** (AVDH) pins for the channel 1 PECL Clock Synthesizer Unit (CSU) and PECL Reference Clock Receiver. The AVDH_CSU_1 pins should be connected through passive filtering networks to a well-decoupled +3.3V analog power supply. Please see the Operation section for detailed information.
AVDH_CSU_2 (4)	Analog Power	AL7 AK7 AL8 AK8	The 3.3 volt **analog power** (AVDH) pins for the channel 2 PECL Clock Synthesizer Unit (CSU) and PECL Reference Clock Receiver. The AVDH_CSU_2 pins should be connected through passive filtering networks to a well-decoupled +3.3V analog power supply. Please see the Operation section for detailed information.
AVDH_CSU_3 (4)	Analog Power	W5 W4 Y5 Y4	The 3.3 volt **analog power** (AVDH) pins for the channel 3 PECL Clock Synthesizer Unit (CSU) and PECL Reference Clock Receiver. The AVDH_CSU_3 pins should be connected through passive filtering networks to a well-decoupled +3.3V analog power supply. Please see the Operation section for detailed information.
AVDH_QSFIM (13)	Analog Power	D30 E30 E27 E25 E23 E21 E19 E17 E14 E12 E10 E8 E6	The 3.3 volt **analog power** (AVDH) pins for all channels of the QSFI-4 interface. The AVDH_QSFIM pins should be connected through passive filtering networks to a well-decoupled +3.3V analog power supply. Please see the Operation section for detailed information.
AVDL_0 (9)	Analog Power	W30 AA30 AC30 AD30 AG34 AG33 AG32 AG31 AG30	The 1.8 volt **analog power** (AVDL) pins for channel 0. The AVDL_0 pins should be connected through passive filtering networks to a well-decoupled +1.8V analog power supply. Please see the Operation section for detailed information.
AVDL_1 (8)	Analog Power	AK28 AK26 AK24 AK23 AL20 AM20 AN20 AP20	The 1.8 volt **analog power** (AVDL) pins for channel 1. The AVDL_1 pins should be connected through passive filtering networks to a well-decoupled +1.8V analog power supply. Please see the Operation section for detailed information.

Pin Name	Pin Type	PIN No.	Function
AVDL_2 (9)	Analog Power	AK14 AK12 AK10 AK9 AK6 AL6 AM6 AN6 AP6	The 1.8 volt **analog power** (AVDL) pins for channel 2. The AVDL_2 pins should be connected through passive filtering networks to a well-decoupled +1.8V analog power supply. Please see the Operation section for detailed information.
AVDL_3 (9)	Analog Power	AF5 AD5 AB5 AA5 V5 V4 V3 V2 V1	The 1.8 volt **analog power** (AVDL) pins for channel 3. The AVDL_3 pins should be connected through passive filtering networks to a well-decoupled +1.8V analog power supply. Please see the Operation section for detailed information.
AVDL_QSFIM (16)	Analog Power	A29 B29 E29 E28 E26 E24 E22 E20 E18 E16 E15 E13 E11 E9 E7 E5	The 1.8 volt **analog power** (AVDL) pins for all channels of the QSFI-4 interface. The AVDL_QSFIM pins should be connected through passive filtering networks to a well-decoupled +1.8V analog power supply. Please see the Operation section for detailed information.

9.8 Digital Power (56)

Pin Name	Pin Type	PIN No.	Function
VDDO (33)	Digital Switching Power	G31 H2 H31 K30 M32 R34 AP18 AN17 J3 H5 G5 F1 F2 F3 F4 F5 P5 U1 U2 U3 U4 U5 AK20 U30 U31 U32 U33 U34 F30 F31 F32 F33 F34	The **digital switching power** (VDDO) pins should be connected to a well-decoupled +3.3V digital power supply.

Pin Name	Pin Type	PIN No.	Function
VDDI (23)	Digital Core Power	G30 J30 L30 N30 R30 T32 AK19 AK18 AL18 AK16 T3 R3 N3 M2 L4 K5 B15 A15 B16 AJ4 AJ5 AH30 AH31	The **digital core power** (VDDI) pins should be connected to a well-decoupled +1.8V digital power supply.

9.9 Ground (186)

Pin Name	Pin Type	PIN No.	Function
VSS (186)	Digital Ground	A1 B1 C1 D1 E1 A2 B2 C2 D2 E2 K1 L1 N1 P1 R1 T1 W1 W2 Y1 Y2 AA2 AA3 AA4 AB2 AB3 AB4 AC1 AC2 AD2 AD3 AD4 AE2 AF1 AH1 AH2 AH3 AH4 AH5 AJ1 AJ2 AJ3	The **ground** (VSS) pins should be connected to a low inductance ground plane connected to both the digital and analog power supplies. Please see the Operation section for detailed information.

Pin Name	Pin Type	PIN No.	Function
VSS (continued)		AK1 AK2 AK3 AK4 AK5 AL1 AL2 AL3 AL4 AL5 AM1 AM2 AM3 AM4 AM5 AN1 AN2 AN3 AN4 AN5 AP1 AP2 AP3 AP4 AP5 AN7 AP7 AN8 AP8 AL9 AM9 AN9 AL10 AM10 AN10 AN11 AP11 AL12 AM12 AN12 AN13 AP14 AN21 AP21	

Pin Name	Pin Type	PIN No.	Function
VSS (continued)		AN22 AP22 AL23 AM23 AN23 AL24 AM24 AN24 AN25 AP25 AL26 AM26 AN26 AP30 AP31 AP32 AP33 AP34 AN30 AN31 AN32 AN33 AN34 AM30 AM31 AM32 AM33 AM34 AL30 AL31 AL32 AL33 AL34 AK30 AK31 AK32 AK33 AK34 AJ30 AJ31 AJ32 AJ33	

Pin Name	Pin Type	PIN No.	Function
VSS (continued)		AJ34 AH32 AH33 AH34 AF33 AF34 AE33 AE34 AD31 AD32 AD33 AC31 AC32 AC33 AB33 AB34 AA31 AA32 AA33 Y33 W34 E31 E32 E33 E34 D31 D32 D33 D34 C31 C32 C33 C34 B31 B32 B33	

Pin Name	Pin Type	PIN No.	Function
VSS (continued)		B34 A30 A31 A32 A33 A34 A28 B28 A3 A4 A5 B3 B4 B5 C3 C4 D3 D4 E3 E4 A16 AP28 AN27	

9.10 Pad Summary

Interface	Digital Inputs	Digital Outputs	Digital Bidir	LVDS Input	LVDS Output	PECL Input	PECL Output	Analog	Total
Serial Line Side Interface	5	4				16	8		33
OIF SFI-4 Interface	4	8		40	48				100
Clocks and Alarms		12							12
Microprocessor	19	1	16						36
JTAG Test Access Port	4	1							5
Analog misc	4	8						20	32
1.8 V Analog Power									69
3.3 V Analog Power									51
1.8 V Digital Power									23
3.3 V Digital Power									33
Ground									186
Totals	36	34	16	40	48	16	8	20	580

Notes on Pin Description

1. All CRSU 4x2488 inputs and bidirectionals present minimum capacitive loading and operate at CMOS/TTL logic levels except: the REFCLK+/-, RXD[3:0]+/- pins which operate at pseudo-ECL (PECL) logic levels, TXD[3:0]+/- pins which operate at 3.3-V CML levels and RXDATA(3..0)[3:0]+/-, RXCLK(3..0)+/-, TXDATA(3..0)[3:0]+/-, TXCLK(3..0)+/-, TXCLK(3..0)_SRC+/- which operate at LVDS logic levels.

2. The CRSU 4x2488 digital outputs and bidirectionals which have 6mA drive capability are: SALM[3:0], TXENB[3:0], SYNC_ERR[3:0], PHASE_ERR[3:0].

   The CRSU 4x2488 digital outputs and bidirectionals which have 9mA drive capability are: RCLK[3:0], TCLK[3:0], TDO and INTB.

3. The CRSU 4x2488 digital outputs and bidirectionals which have 12mA drive capability are: D[15:0].
4. All CRSU 4x2488 digital inputs are 3.3V tolerant.
5. Inputs ALE, RSTB, TMS, TDI and TRSTB have internal pull-up resistors.
6. It is mandatory that every digital ground pin (VSS) be connected to the printed circuit board ground plane to ensure reliable device operation.
7. It is mandatory that every digital power pin (VDDI, VDDO) be connected to the printed circuit board power plane to ensure reliable device operation.
8. It is mandatory that every Analog power pin (QAVD, AVDH, AVDL) be connected to the printed circuit board power plane to ensure reliable device operation.
9. All analog power pins can be sensitive to noise. They must be isolated from the digital power pins. Care must be taken to correctly decouple these pins. (Please refer to App Note: PMC-2011065).
10. Due to ESD protection structures in the pads it is necessary to exercise caution when powering a device up or down. ESD protection devices behave as diodes between power supply pins and from I/O pins to power supply pins. Under extreme conditions it is possible to damage these ESD protection devices or trigger latch up. Please adhere to the recommended power supply sequencing as described in the Operation section of this document.
11. Before any input activity occurs, ensure that the device power supplies are within their nominal voltage range.
12. Hold the device in the reset condition until the device power supplies are within their nominal voltage range.

10 Functional Description

This section provides detail on the functional description of the CRSU 4x2488. Table 7 outlines the blocks that are used in the main modes of operation and the optional functions and their corresponding blocks.

Table 7 Functional Block use per Mode

Operational Mode	Functional Blocks	Optional Blocks
SERDES Mode	RXLI, CRU, RX QSFI-4 TXLI, TX line CSU, TX QSFI-4	
PMON Mode	RXLI, CRU, SRLI, RRMP, SBER, RX QSFI-4 TXLI, TX line CSU, STLI, TRSP, RSOP, TX QSFI-4	FEC: RIFD, TIFE
Regenerator Mode	RXLI, CRU TXLI, TX line CSU	PMON: SRLI, RRMP, SBER, RX QSFI-4 STLI, TRSP, RSOP, TX QSFI-4 FEC: RIFD, TIFE

10.1 Receive Line Interface (RXLI)

The four Receive Line Interface blocks (RXLI) allow direct interface of the CRSU 4x2488 to four independent optical data link modules (ODLs) or other medium interfaces. Each block performs clock and data recovery on the incoming 2488.32 Mbit/s data stream and converts the data into a 16-bit wide format.

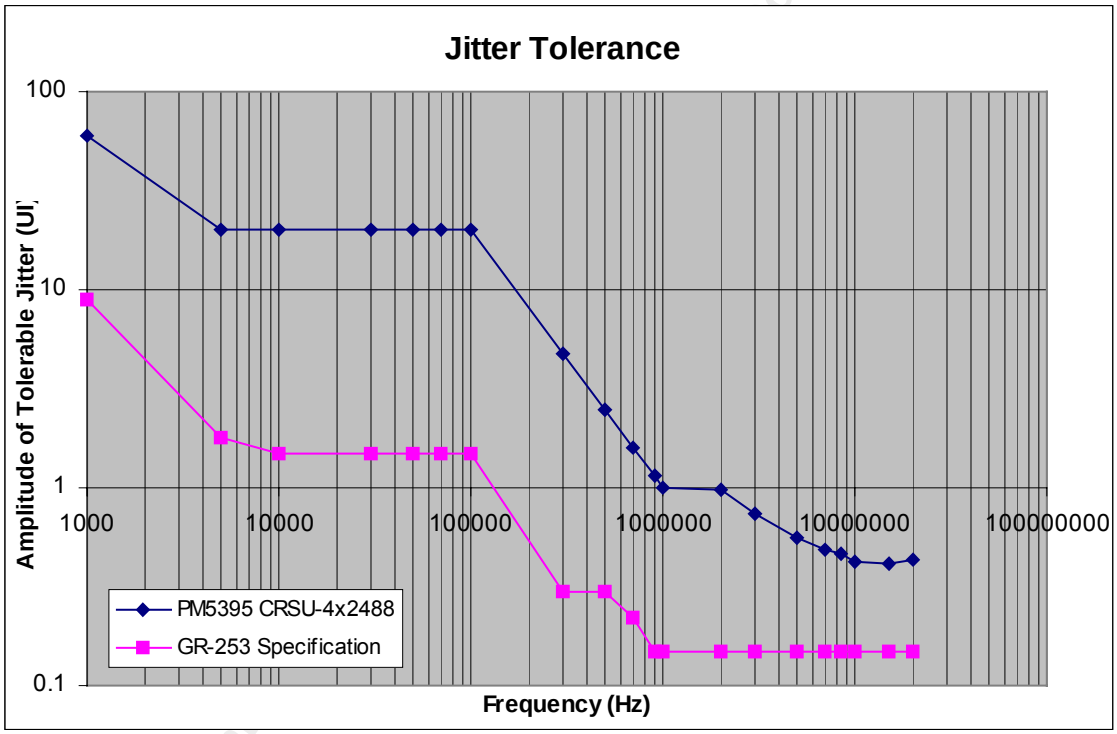
The clock recovery unit (CRU) recovers the clock from the incoming bit serial data stream and is compliant with SONET and SDH jitter tolerance requirements. The clock recovery unit utilizes a 155.52 MHz reference clock to train and monitor its clock recovery PLL. Under loss of signal conditions, the clock recovery unit continues to output a line rate clock that is locked to this reference for keep alive purposes. The clock recovery unit provides status bits that indicate whether it is locked to data or the reference, register 1103 Channel 0. The CRU also supports a serial loop-back, register 1102 bit 7 and signal detect input, when deasserted squelches normal input data.

Initially upon start-up, the PLL locks to the reference clock, REFCLK. When the frequency of the recovered clock is within approximately 400 ppm of the reference clock, the PLL attempts to lock to the data. Once in data lock and the loss of signal detector is enabled (register 1103 bit 10), the PLL reverts to the reference clock if no data transitions occur within a programmable number of bit periods or if the recovered clock drifts beyond 1000 ppm of the reference clock.

When the transmit clock is derived from the recovered clock (loop timing), the accuracy of the transmit clock is directly related to the REFCLK reference accuracy in the case of a loss of signal condition. To meet the Bellcore GR-253-CORE SONET Network Element free-run accuracy specification, the reference must be within +/-4.6 ppm. When not loop timed, the REFCLK accuracy may be relaxed to +/-20 ppm.

The loop filter transfer function is optimized to enable the PLL to track the jitter, yet tolerate the minimum transition density expected in a received SONET data signal. The total loop dynamics of the clock recovery PLL yield a jitter tolerance that exceeds the minimum tolerance specified for SONET equipment by GR-253-CORE. Please refer to the Figure 6 below.

Figure 6 Typical STS-48c (STM-16c) Jitter Tolerance



10.2 SONET/SDH Receive Line Interface (SRLI)

The four SONET/SDH receive line interface blocks perform initial byte and frame alignment on four independent incoming 2488 Mbit/s data streams based on the SONET/SDH A1/A2 framing pattern.

While out of frame, the SRLI monitors the receive data stream for an occurrence of the A1/A2 framing pattern. The SRLI adjusts its byte and frame alignment when three consecutive A1 bytes followed by three consecutive A2 bytes occur in the data stream. The SRLI informs the downstream RRMP framer blocks when the framing pattern has been detected to reinitialize to the new transport frame alignment. While in frame, the SRLI maintains the same byte and frame alignment until the RRMP declares out of frame.

10.3 Receive Regenerator and Multiplexor Processor (RRMP)

The CRSU 4x2488 contains 16 Receive Regenerator and Multiplex section Processor (RRMP) blocks. They are grouped into four sets of 4 RRMPs each. Each group processes the transport overhead of one of the four independent received data streams. Within each set of RRMPs, the first RRMP processes the first 4 STS-3 (STM-1) in the multiplexing structure of an STS-48 (STM-16) stream. The second RRMP processes the next set of 4 STS-3 (STM-1) streams and so on.

The RRMP frames to the data stream by operating with an upstream pattern detector (SRLI) that searches for occurrences of the A1/A2 framing pattern. Once the SRLI has found an A1/A2 framing pattern, the RRMP monitors for the next occurrence of the framing pattern 125µs later. Two framing pattern algorithms are provided to improve performance in the presence of bit errors. The selection of algorithm is done be setting the ALGO2 bit in the RRMP Configuration Register, 1120H, 1320H, 1520H and 1720H. In algorithm 1 (ALGO2 = logic 0), the RRMP declares frame alignment (removes OOF defect) when the 12 A1 and the 12 A2 bytes are seen error-free in the first STS-12 (STM-4) of the STS-48 (STM-16) stream. In algorithm 2 (ALGO2 = logic 1), the RRMP declares frame alignment (removes OOF defect) when only the last A1 byte and the first four bits of the first A2 byte are seen error-free in the first STS-12 (STM-4) of the STS-48 (STM-16) stream. Once in frame, the RRMP monitors the framing pattern and declares OOF when one or more bit errors in the framing pattern are detected for four consecutive frames. Again, depending upon the algorithm either 24 framing bytes or 12 framing bits are examined for bit errors in the framing pattern.

The performance of these framing algorithms in the presence of bit errors and random data is robust. When looking for frame alignment the performance of each algorithm is dominated by the alignment algorithm used in the SRLI which always examines 3 A1 and 3 A2 framing bytes. The probability of falsely framing to random data is less than 0.00001% for either algorithm. Once in frame alignment, the RRMP continuously monitors the framing pattern. When the incoming stream contains a 10^{-3} BER, the first algorithm provides a 99.75% probability that the mean time between OOF occurrences is 1.3 seconds and the second algorithm provides a 99.75% probability that the mean time between OOF occurrences is 7 minutes.

The RRMP also detects loss of frame (LOF) defect and loss of signal (LOS) defect. LOF is declared when an out of frame (OOF) condition exists for a total period of 3ms during which there is no continuous in frame period of 3 ms. LOF output is removed when an in frame condition exists for a continuous period of 3 ms. LOS is declared when a continuous period of 20 µs without transitions on the received data stream is detected. LOS is removed when two consecutive framing patterns are found (based on algorithm 1 or algorithm 2) and during the intervening time (one frame) there are no continuous periods of 20 µs without transitions on the received data stream.

The RRMP calculates the section BIP-8 error detection code (B1) on the scrambled data of the complete frame. The section BIP-8 code is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 code is compared with the BIP-8 code extracted from the B1 byte of STS-1 (STM-0) #1 of the following frame after de-scrambling. Any difference indicates a section BIP-8 error. The RRMP accumulates section BIP-8 errors in a microprocessor readable 16-bit saturating counter (up to 1 second accumulation time). Optionally, block section BIP-8 errors can be accumulated.

The RRMP optionally de-scrambles the received data stream.

The RRMP calculates the line BIP-8 error detection codes (B2) on the de-scrambled line overhead and synchronous payload envelope bytes of the constituent STS-1 (STM-0). The line BIP-8 code is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 codes are compared with the BIP-8 codes extracted from the B2 byte of the constituent STS-1 (STM-0) of the following frame after de-scrambling. Any difference indicates a line BIP-8 error. The RRMP accumulates line BIP-8 errors in a microprocessor readable 24 bit saturating counter (up to 1 second accumulation time). Optionally, block BIP errors can be accumulated.

The RRMP extracts the line remote error indication (REI-L) errors from the M1 byte of STS-1 (STM-0) #3 and accumulates them in a microprocessor readable 24-bit saturating counter (up to 1 second accumulation time). Optionally, block line REI errors can be accumulated.

The RRMP extracts and filters the K1/K2 APS bytes for three frames. The filtered K1/K2 APS bytes are accessible through microprocessor readable registers. The RRMP also monitors the unfiltered K1/K2 APS bytes to detect APS byte failure (APSBF) defect, line alarm indication signal (AIS-L) defect and line remote defect indication (RDI-L) defect. APS byte failure is declared when twelve consecutive frames have been received where no three consecutive frames contain identical K1 bytes. The APS byte failure is removed upon detection of three consecutive frames containing identical K1 bytes. The detection of invalid APS codes must be done in software by polling the K1/K2 APS register. Line AIS is declared when the bit pattern 111 is observed in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. Line AIS is removed when any pattern other than 111 is observed for three or five consecutive frames. Line RDI is declared when the bit pattern 110 is observed in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. Line RDI is removed when any pattern other than 110 is observed for three or five consecutive frames.

The RRMP extracts and filters the synchronization status message (SSM) for eight frames. The filtered SSM is accessible through microprocessor readable registers.

RRMP optionally inserts line alarm indication signal (AIS-L).

A maskable interrupt is activated to indicate any change in the status of out of frame (OOF), loss of frame (LOF), loss of signal (LOS), line remote defect indication (RDI-L), line alarm indication signal (AIS-L), change of synchronization status message (COSSM), change of APS bytes (COAPS), APS byte failure (APSBF), section BIP-8 errors, line BIP-8 errors and line remote error indication (REI-L) events.

The RRMP block provides de-scrambled data and frame alignment indication signals for use by the Receive In-band Forward Error Correction Decoder blocks (RIFD).

10.4 Receive In-band Forward Error Correction Decoder (RIFD)

The RIFD block decodes the In-band Forward Error Correction checksum bytes imbedded in the section and line overhead bytes and performs error correction on the received stream. Each RIFD block processes one of the four STS-48 receive streams and interfaces to a set of four upstream RRMP blocks. Error correction is disabled under LOS, LOF and AIS-L alarm conditions.

10.4.1 FEC Decoder

The FEC Decoder extracts the FEC check bits from in-band FEC compliant data streams and uses them to correct up to 24 random bit errors for each STS-48/STM-16 row. The FEC check bits are located in the transport overhead. The decoder corrects the payload bytes, the line/MS overhead bytes, and the FEC check bits. Section/RS overhead bytes are not corrected because they are not included in the in-band FEC coverage.

The decoder performs error correction using a (4359, 4320) shortened code derived from a (8191, 8152) binary BCH code. It uses the extracted FEC check bits to assemble eight interleaved (4359,4320) code blocks to provide FEC coverage for each STS-48/STM-16 row.

The decoding function adds 14.6 us of delay to the data when running at the nominal STS-48/STM-16 data rate.

The decoder extracts the FEC Status Indication (FSI) byte from the transport overhead to determine whether error correction is enabled or disabled by the transmitter. Section defects such as loss of frame, loss of signal, and AIS-L/MS-AIS cause the decoder to disable error correction at the beginning of the next frame boundary. Microprocessor control is provided to disable error correction with the decoder delay added or removed. The decoder can be optionally programmed to generate an interrupt when FSI enables or disables the decoder.

10.4.2 Performance Monitors

The RIFD provides two performance monitors: a line BIP monitor and an error correction monitor.

The line BIP monitor calculates the line BIP for a received STS-48/STM-16 frame and compares it to the B2 bytes of the following received frame. Any differences in the comparison indicate a BIP error. The monitor counts either BIP-8 or block BIP-24 errors and accumulates the number of errors in a 22-bit register which allows for 1 second of accumulation time for BIP-8 errors and 32 second of accumulation time for block BIP-24 errors. This register can be read by the microprocessor. BIP calculations can be performed on either the corrected data stream or the uncorrected data stream.

The correction monitor counts of the number of bit errors that have been corrected. The error count is accumulated in a 21-bit register which allows for 1 second of accumulation time if the frames contain the maximum number of errors that are correctable by the RIFD. This register can be read by the microprocessor, and its value can be used to find the raw BER from the last FEC decoding point in the network.

The performance monitors can be optionally programmed to generate interrupts when BIP errors and/or corrected bit errors are detected.

10.5 SONET/SDH Bit Error Rate Monitor (SBER)

The SBER block provides two independent bit error rate monitoring circuits (BERM block). It is used to monitor the Multiplexer Section BIP (B2) with one BERM block dedicated to monitor the Signal Degrade (SD) alarm and the other BERM block dedicated to monitor the Signal Fail (SF) alarm. These alarms can then be used to control system level features such as Automatic Protection Switching (APS).

The BERM block utilizes a sliding window based algorithm. This algorithm provides a much superior detection, clearing and false detection performance than the simple jumping window (i.e. using a counter that can be reset and polled at a regular interval) algorithm.

10.6 Receive QSFI-4 Interface (Rx QSFI-4 I/F)

Each of the four independent Receive QSFI-4 Interface blocks carries the received data from the associated 2.488 Gbit/s input data stream in nibble-wide format. The clock and data are phase locked to the associated receive data stream. When the CRSU 4x2488 is processing SONET/SDH data, the nibbles may be software configured to be aligned to the incoming octets. When processing arbitrary data streams, the nibbles are not aligned to any underlying structure of the received data stream.

10.6.1 Receive QSFI-4 Clock Output

Each 4-bit slice of the ReceiveQSFI-4 interface uses the 2.488 Gbit/s recovered clock from the associated CRU as it's timing source associated receive QSFI-4 interface. The frequency of the RXCLK[*n*] is therefore locked to the line side clock but the phase of the RXCLK[*n*] is not guaranteed to be locked to the line side clock.

10.7 Transmit QSFI-4 Interface (Tx QSFI-4 I/F)

Each of the four independent Transmit QSFI-4 Interface blocks carries the transmit data to the associated 2.488 Gbit/s data stream in nibble-wide format. The clock and data are phase locked to the associated transmit data stream.

10.7.1 Transmit QSFI-4 Clock Synthesis Unit (Tx QSFI-4 CSU)

Each of the four independent Transmit QSFI-4 interface slices provides timing to external devices which are connected to the TXDATA*n*[3:0] buses. It is expected that the external devices buffer the source clock (TXCLK_SRC[*n*]) generated by the CRSU 4x2488 and return it (TXCLK[*n*]) synchronously with the data (TXCLK*n*[3:0]). The TXCLK_SRC[*n*] clock signal is slaved to the associated transmit line interface clock synthesis unit. Thus, each transmit QSFI-4 interface slice is frequency locked to the associated transmit data stream (TXD[*n*]+/-).

10.8 Receive Section Overhead Processor (RSOP)

The RSOP frames to the data stream by operating with the upstream pattern detector, SRLI, that searches for occurrences of the SONET framing pattern in the bit-serial data stream. The RSOP provides two framing algorithms that provide improved performance in the presence of bit errors. The RSOP provides the appropriate clock and frame alignment indication signals for use by downstream circuitry.

10.9 Transmit In-band Forward Error Correction Encoder (TIFE)

The Transmit In-band Forward Error Correction block inserts In-band Forward Error Correction checksum bytes into in the section and line overhead bytes of the SONET/SDH frame. Each TIFE block processes one of the four STS-48 transmit streams and interfaces to a set of four downstream TRSP blocks.

10.9.1 B2 Compensation

The TIFE inserts FEC parity bits into section and line overhead bytes. Consequently, the B2 bytes carried in the transmit QSFI-4 interface is no longer valid and must be compensated. The B2 compensation block maintains two registers. The first is a scratch pad register and is cleared at the start of every frame. It accumulates the changes (XOR) between the line overhead bytes delivered by the transmit QSFI-4 interface and the modification by the TIFE due to FEC parity bits insertion. The second register is a history register. It maintains a record of all the modifications to line overhead bytes at FEC parity bit positions. At the end of every frame, the contents of the scratch pad and the history register are XOR'ed together and the result stored back in the history register. The B2 bytes delivered to the downstream transmit regenerator section processor block (TRSP) is the XOR of the B2 bytes carried in the transmit QSFI-4 interface and the contents of the history register. The compensated B2 bytes are used to calculate the FEC parity bits. The TRSP should not recalculate the B2 bytes frame after the TIFE has placed the bytes in the frame. This requires that the B2DISABLE bit in register in registers 1052, 1062, 1072 and 1082 for channel 0 and the equivalent registers in the other channels.

The TIFE will always recalculate and insert the B2 byte into the frame whether it is in state 1 or state 2 as defined by STATE[1:0] bits in Register 1040H. As a result the B1 must always be recalculated in the TRSP if the TIFE block is placed in either state.

10.9.2 FEC Encoder

The FEC encoder block inserts FEC parity bits to the section and line overhead bytes in the transmit stream. The FEC encoder block also sets the FEC status indication (FSI) bits. The FEC encoder block contains 8 parallel encoder circuits, each of which operate on one of the eight bit-interleaved code blocks. Each encoder circuit consists of a 39-bit long division circuit that finds the remainder, R(x) given by R(x) = I(x) mod G(x). The information bits are represented by I(x) = $a_{4358}x^{4358}$ + … + $a_{39}x^{39}$ where an (n=4358 to 39). The most significant term of the polynomial ($a_{4358}x^{4358}$) is associated with the first bit transmitted and the least significant term ($a_{39}x^{39}$) is associated with the last bit transmitted. The generator polynomial is given by G (x) = $x^{39} + x^{37} + x^{36} + x^{35} + x^{33} + x^{31} + x^{30} + x^{29} + x^{28} + x^{26} + x^{24} + x^{23} + x^{21} + x^{20} + x^{17} + x^{15} + x^{13} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^6 + x^5 + x^3 + x^2 + 1$. The FEC parity bits are this remainder, R(x) and are inserted into the transport overhead bytes.

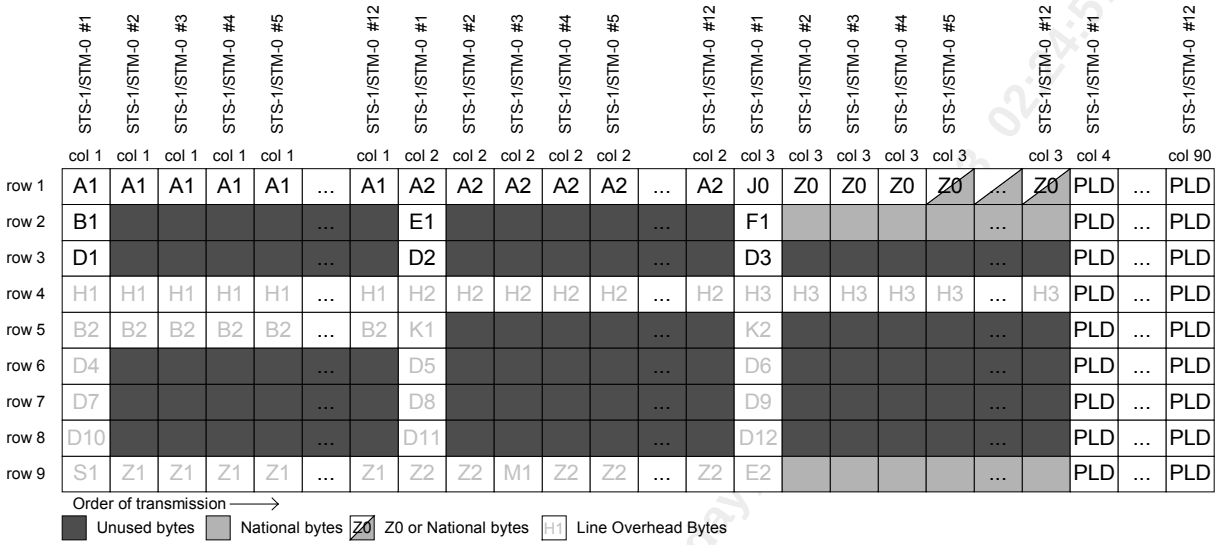
10.10 Transmit Regenerator and Section Processor (TRSP)

The CRSU 4x2488 contains 16 Transmit Regenerator and Section Processor (TRSP) blocks. They are grouped into four sets of 4 TRSP blocks each. Each group processes the section overhead of one of the four independent transmit data streams. Within each set of TRSPs, the first TRSP processes the first 4 STS-3 (STM-1) in the multiplexing structure of an STS-48 (STM-16) stream. The second TRSP processes the next set of 4 STS-3 (STM-1) streams and so on.

The TRSP calculates the section BIP-8 error detection code on the transmit data stream. The section BIP-8 byte is calculated on the scrambled bytes of the complete frame. The section BIP-8 byte is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 error detection code is inserted in the B1 byte of STS-1 (STM-0) #1 of the following frame before scrambling. The TRSP scrambles the transmit data stream with the frame synchronous scrambler

The TRSP can insert most of the section overhead bytes from internal registers. Since there are multiple sources for the same overhead byte, the SOH bytes are prioritized according to Figure 8 before being inserted into the data stream

Figure 7 STS-48 (STM-16) in SOH, Master TRSP



Note, only the overhead from the first STS-12 (STM-4) of the STS-48 (STM-16) can be use as a source. Overhead from the other three STS-12's (STM-4's) are internally generated or are assigned default values as described below.

Figure 8 SOH Insertion Priority

BYTE	HIGHEST priority			LOWEST priority
A1		76h (A1ERR =1)	F6h (A1A2EN= 1)	A1 pass through
A2			28h (A1A2EN= 1)	A2 pass through
J0	STS-1/STM-0 # (J0Z0INCEN=1)	J0[7:0] (TRACE EN=1)	J0V (J0REGEN =1)	J0 pass through
Z0	STS-1/STM-0 # (J0Z0INCEN=1)		Z0V (Z0REGEN =1)	Z0 pass through
B1	B1 pass through (B1DISABLE=1)			Calculated B1 XOR B1MASK
E1			E1V (E1REGEN =1)	E1 pass through
F1			F1V (F1REGEN =1)	F1 pass through

BYTE	HIGHEST priority			LOWEST priority
D1-D3			D1D3V (D1D3REGEN=1)	D1-D3 pass through
National				National pass through
Unused			UnusedV (UnusedEN=1)	Unused pass through
PLD				PLD pass through

The Z0DEF register bit defines the Z0/NATIONAL growth bytes for row #1. When Z0DEF is set to logic one, the Z0/NATIONAL bytes are defined according to ITU. When Z0DEF is set to logic zero, the Z0/NATIONAL bytes are defined according to Telcordia.

Figure 9 Z0/National Growth Bytes Definition for Row #1

TRSP	Type	Z0DEF = 0	Z0DEF = 1
STS-48 (STM-16)	Z0	From STS-1/STM-0 #1 to #48	From STS-1/STM-0 #1 to #16
	National	None	From STS-1/STM-0 #17 to #48

The TRSP calculates the line BIP-8 error detection codes on the transmit data stream. One line BIP-8 error detection code is calculated for each of the constituent STS-1 (STM-0). The line BIP-8 byte is calculated on the unscrambled bytes of the STS-1 (STM-0) except for the 9 SOH bytes. The line BIP-8 byte is based on a bit interleaved parity calculation using even parity. For each STS-1 (STM-0), the calculated BIP-8 error detection code is inserted in the B2 byte of the following frame before scrambling. Optionally the TRSP can be set to scramble the transmit data stream or not. The scrambling is controlled by the DS_CD[3:0] bits in the Diagnostics Register 0010H.

If the Transmit FEC Encoder is enabled the line BIP-8 (B2) calculation should be disabled in the TRSP. The correct B2 byte is calculated and inserted into the frame after the FEC bytes are added to the frame by the TIFE encoder. The TRSP line BIP-8 calculation should only be used if the transmit encoder is disabled. In order to disable the TRSP line BIP-8 insertion the B2DISABLE bit in the TRSP Error Insertion Register 1052H, 1062H, 1072H and 1082H must be set to logic '1'.

The TRSP calculates the section BIP-8 error detection code on the transmit data stream. The section BIP-8 byte is calculated on the scrambled bytes of the complete frame. The section BIP-8 byte is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 error detection code is inserted in the B1 byte of STS-1 (STM-0) #1 of the following frame before scrambling.

10.11 SONET/SDH Transmit Line Interface (STLI)

Each of the four independent SONET/SDH transmit line interface block properly formats the associated outgoing 2488 Mbit/s data stream. This block interfaces the TRSP blocks to the Transmit Line Interface block.

10.12 Transmit Line Interface (TXLI)

Each of the four independent Transmit Line Interface (TXLI) blocks allows the CRSU 4x2488 to interface directly to Optical Data Link (ODL) modules or other medium interfaces. This block performs clock synthesis and performs parallel to serial conversion on the outgoing 2488.32 Mbit/s data streams.

The transmit clock is synthesized from a 155.52. MHz reference. The transfer function yields a typical low pass corner of **20** MHz above which reference jitter is attenuated at **6** dB per octave. The design of the loop filter and PLL is optimized for minimum intrinsic jitter. With a low jitter 155.52MHz reference, the intrinsic jitter is typically less than 0.075 UI pp and 0.005UI RMSwhen measured using a 12K-20MHz filter. See section 19.5 OC-48 Interface Timing Characteristics for the reference clock specifications.

The REFCLK reference should be within ±20 ppm to meet the SONET free-run accuracy requirements specified in GR-253-CORE.

The Parallel to Serial Converter (PISO) converts the transmit byte serial data stream to a bit serial stream. The transmit bit serial stream appears on the associated TXD+/- CML output.

10.12.1 Transmit Line Interface Clock Synthesis Unit (Tx Line I/F CSU)

The CSU is a fully integrated clock synthesis unit. It generates low jitter multi-phase differential clocks at 2488.32 MHz for the usage by the transmitter. The REFCLK is used as a low jitter reference clock to the CSU.

10.13 JTAG Test Access Port Interface

The JTAG Test Access Port block provides JTAG support for boundary scan. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE and STCTEST instructions are supported. The CRSU 4x2488 identification code is 153950CD hexadecimal.

10.14 Microprocessor Interface

The Microprocessor Interface Block provides the logic required to interface the generic microprocessor bus with the normal mode and test mode registers within the CRSU 4x2488. The normal mode registers are used during normal operation to configure and monitor the CRSU 4x2488. The test mode registers are used to enhance the testability of the CRSU 4x2488. The register set is accessed as shown below. The corresponding memory map address is identified by the address column of the table. Addresses that are not shown are not used and must be treated as Reserved.

Table 8 Register Memory Map

Address	Register Description
0000	Identity, and Global Performance Monitor Update Trigger
0001	Master Reset
0002	Master Interrupt Status RX CH0
0003	Master Interrupt Status RX CH1
0004	Master Interrupt Status RX CH2
0005	Master Interrupt Status RX CH3
0006	Master Interrupt Status TX CH0
0007	Master Interrupt Status TX CH1
0008	Master Interrupt Status TX CH2
0009	Master Interrupt Status TX CH3
000A	Channel Interrupt Status
000B	Configuration and Clock Monitor
000C	Bypass and Fiber Order
000D	Bypass modes
000E	Clock Control
000F	Bypass and Channel Loopback
0010	Diagnostics
0011	Channel 3 and 2 SALM Enables
0012	Channel 1 and 0 SALM Enables
0013	TXENB Control
0014	Device Number
0015-0FFF	Unused
	CHANNEL 0 TX REGISTERS
	QSFIM_2488
1000	QSFIM_2488 Status
1001	QSFIM_2488 Control
1002	QSFIM_2488 Reserved
1003-101F	Unused
1020	Reserved
1021	Reserved
1022-102F	Unused
	RSOP
1030	RSOP Control
1031	RSOP Interrupt Status
1032	RSOP Reserved

Address	Register Description
1033	RSOP Reserved
1034-103F	Unused
	TIFE
1040	TIFE Configuration
1041	TIFE Control
1042	TIFE Error Insertion Byte 0
1043	TIFE Error Insertion Byte 1
1044	TIFE Error Insertion Byte 2
1045	TIFE Error Insertion Byte 3
1046-104F	Unused
	TRSP
1050	TRSP Configuration
1051	TRSP Register Insertion
1052	TRSP Error Insertion
1053	TRSP Transmit J0 and Z0
1054	TRSP Transmit E1 and F1
1055	TRSP Transmit D1D3
1056	TRSP Reserved
1057	TRSP Reserved
1058	TRSP Reserved
1059	TRSP Reserved
105A	TRSP B1 Mask
105B-105F	Unused
1060	TRSP Aux1 Configuration
1061	TRSP Aux1 Reserved
1062	TRSP Aux1 Error Insertion
1063	TRSP Aux1 Z0 Transmit
1064-106A	TRSP Aux1 Reserved
106B-106F	Unused
1070	TRSP Aux2 Configuration
1071	TRSP Aux2 Reserved
1072	TRSP Aux2 Error Insertion
1073	TRSP Aux2 Z0 Transmit
1074-107A	TRSP Aux2 Reserved
107B-107F	Unused
1080	TRSP Aux3 Configuration
1081	TRSP Aux3 Reserved

Address	Register Description
1082	TRSP Aux3 Error Insertion
1083	TRSP Aux2 Z0 Transmit
1084-108A	TRSP Aux3 Reserved
108B-108F	Unused
	STLI
1090	STLI Clock Configuration
1091	STLI Reserved
1092-109F	Unused
	TXLI
10A0	TXLI Control/Status
10A1	TXLI CSU Control
10A2	TXLI Pattern Register
10A3- 10FF	Unused
	CHANNEL 0 RX REGISTERS
	RXLI
1100	RXLI Interrupt Status
1101	RXLI Interrupt Control
1102	RXLI CRU Control
1103	RXLI CRU Clock Training Configuration and Status
1104	RXLI PRBS Control
1105	RXLI Pattern
1106-110F	Unused
	SRLI
1110	SRLI Clock Configuration
1111	SRLI Reserved
1112-111F	Unused
	RRMP
1120	RRMP Configuration
1121	RRMP Status
1122	RRMP Interrupt Enable
1123	RRMP Interrupt Status
1124	RRMP Received APS
1125	RRMP Received SSM

Address	Register Description
1126	RRMP AIS enable
1127	RRMP Section BIP Error Counter
1128	RRMP Line BIP Error Counter (LSB)
1129	RRMP Line BIP Error Counter (MSB)
112A	RRMP Line REI Error Counter (LSB)
112B	RRMP Line REI Error Counter (MSB)
112C-112F	Unused
1130-1135	RRMP Reserved 2(slave)
1140-1145	RRMP Reserved 3(slave)
1150-1155	RRMP Reserved 4(slave)
1136	RRMP AIS enable 2 (Slave)
1146	RRMP AIS enable 3 (Slave)
1156	RRMP AIS enable 4 (Slave)
1137-113B	RRMP Reserved 2(slave)
1147-114B	RRMP Reserved 3(slave)
1157-115B	RRMP Reserved 4(slave)
113C-113F	Unused
114C-114F	Unused
115C-115F	Unused
	RIFD
1160	RIFD Configuration
1161	RIFD Status
1162	RIFD interrupt enable
1163	RIFD interrupt status
1164	RIFD correctable error count LSB
1165	RIFD correctable error count MSB
1166	RIFD Line BIP error count LSB
1167	RIFD Line BIP error count MSB
1168-117F	Unused
	SBER
1180	SBER Configuration
1181	SBER Status
1182	SBER Interrupt Enable
1183	SBER Interrupt Status
1184	SBER SF BERM Accumulation Period (LSB)
1185	SBER SF BERM Accumulation Period (MSB)
1186	SBER SF BERM Saturation Threshold (LSB)

Address	Register Description
1187	SBER SF BERM Saturation Threshold (MSB)
1188	SBER SF BERM Declaring Threshold (LSB)
1189	SBER SF BERM Declaring Threshold (MSB)
118A	SBER SF BERM Clearing Threshold (LSB)
118B	SBER SF BERM Clearing Threshold (MSB)
118C	SBER SD BERM Accumulation Period (LSB)
118D	SBER SD BERM Accumulation Period (MSB)
118E	SBER SD BERM Saturation Threshold (LSB)
118F	SBER SD BERM Saturation Threshold (MSB)
1190	SBER SD BERM Declaring Threshold (LSB)
1191	SBER SD BERM Declaring Threshold (MSB)
1192	SBER SD BERM Clearing Threshold (LSB)
1193	SBER SD BERM Clearing Threshold (MSB)
1194-11FF	Unused
	CHANNEL 1 TX REGISTERS
	QSFIM_2488
1200	QSFIM_2488 Status
1201	QSFIM_2488 Control
1202	QSFIM_2488 Reserved
1203-121F	Unused
1220	Reserved
1221	Reserved
1222-122F	Unused
	RSOP
1230	RSOP Control
1231	RSOP Interrupt Status
1232	RSOP Reserved
1233	RSOP Reserved
1234-123F	Unused
	TIFE
1240	TIFE Configuration
1241	TIFE Control
1242	TIFE Error Insertion Byte 0
1243	TIFE Error Insertion Byte 1

Address	Register Description
1244	TIFE Error Insertion Byte 2
1245	TIFE Error Insertion Byte 3
1246-124F	Unused
	TRSP
1250	TRSP Configuration
1251	TRSP Register Insertion
1252	TRSP Error Insertion
1253	TRSP Transmit J0 and Z0
1254	TRSP Transmit E1 and F1
1255	TRSP Transmit D1D3
1256	TRSP Reserved
1257	TRSP Reserved
1258	TRSP Reserved
1259	TRSP Reserved
125A	TRSP B1 Mask
125B-125F	Unused
1260	TRSP Aux1 Configuration
1261	TRSP Aux1 Register Insertion
1262	TRSP Aux1 Error Insertion
1263	TRSP Aux1 Z0 Transmit
1264-126A	TRSP Aux1 Reserved
126B-126F	Unused
1270	TRSP Aux2 Configuration
1271	TRSP Aux2 Register Insertion
1272	TRSP Aux2 Error Insertion
1273	TRSP Aux2 Z0 Transmit
1274-127A	TRSP Aux2 Reserved
127B-127F	Unused
1280	TRSP Aux3 Configuration
1281	TRSP Aux3 Register Insertion
1282	TRSP Aux3 Error Insertion
1283	TRSP Aux2 Z0 Transmit
1284-128A	TRSP Aux3 Reserved
128B-128F	Unused
	STLI
1290	STLI Clock Configuration
1291	STLI Reserved

Address	Register Description
1292-129F	Unused
	TXLI
12A0	TXLI Control/Status
12A1	TXLI CSU Control
12A2	TXLI Pattern Register
12A3-12FF	Unused
	CHANNEL 1 RX REGISTERS
	RXLI
1300	RXLI Interrupt Status
1301	RXLI Interrupt Control
1302	RXLI CRU Control
1303	RXLI CRU Clock Training Configuration and Status
1304	RXLI PRBS Control
1305	RXLI Pattern
1306-130F	Unused
	SRLI
1310	SRLI Clock Configuration
1311	SRLI Reserved
1312-111F	Unused
	RRMP
1320	RRMP Configuration
1321	RRMP Status
1322	RRMP Interrupt Enable
1323	RRMP Interrupt Status
1324	RRMP Received APS
1325	RRMP Received SSM
1326	RRMP AIS enable
1327	RRMP Section BIP Error Counter
1328	RRMP Line BIP Error Counter (LSB)
1329	RRMP Line BIP Error Counter (MSB)
132A	RRMP Line REI Error Counter (LSB)
132B	RRMP Line REI Error Counter (MSB)
132C-132F	Unused
1330-1335	RRMP Reserved 2(slave)

Address	Register Description
1340-1345	RRMP Reserved 3(slave)
1350-1355	RRMP Reserved 4(slave)
1336	RRMP AIS enable 2 (Slave)
1346	RRMP AIS enable 3 (Slave)
1356	RRMP AIS enable 4 (Slave)
1337-133B	RRMP Reserved 2(slave)
1347-134B	RRMP Reserved 3(slave)
1357-135B	RRMP Reserved 4(slave)
133C-133F	Unused
134C-134F	Unused
135C-135F	Unused
	RIFD
1360	RIFD Configuration
1361	RIFD Status
1362	RIFD interrupt enable
1363	RIFD interrupt status
1364	RIFD correctable error count LSB
1365	RIFD correctable error count MSB
1366	RIFD Line BIP error count LSB
1367	RIFD Line BIP error count MSB
1368-137F	Unused
	SBER
1380	SBER Configuration
1381	SBER Status
1382	SBER Interrupt Enable
1383	SBER Interrupt Status
1384	SBER SF BERM Accumulation Period (LSB)
1385	SBER SF BERM Accumulation Period (MSB)
1386	SBER SF BERM Saturation Threshold (LSB)
1387	SBER SF BERM Saturation Threshold (MSB)
1388	SBER SF BERM Declaring Threshold (LSB)
1389	SBER SF BERM Declaring Threshold (MSB)
138A	SBER SF BERM Clearing Threshold (LSB)
138B	SBER SF BERM Clearing Threshold (MSB)
138C	SBER SD BERM Accumulation Period (LSB)
138D	SBER SD BERM Accumulation Period (MSB)
138E	SBER SD BERM Saturation Threshold (LSB)

Address	Register Description
138F	SBER SD BERM Saturation Threshold (MSB)
1390	SBER SD BERM Declaring Threshold (LSB)
1391	SBER SD BERM Declaring Threshold (MSB)
1392	SBER SD BERM Clearing Threshold (LSB)
1393	SBER SD BERM Clearing Threshold (MSB)
1394-13FF	Unused
	CHANNEL 2 TX REGISTERS
	QSFIM_2488
1400	QSFIM_2488 Status
1401	QSFIM_2488 Control
1402	QSFIM_2488 Reserved
1403-141F	Unused
1420	Reserved
1421	Reserved
1422-142F	Unused
	RSOP
1430	RSOP Control
1431	RSOP Interrupt Status
1432	RSOP Reserved
1433	RSOP Reserved
1434-143F	Unused
	TIFE
1440	TIFE Configuration
1441	TIFE Control
1442	TIFE Error Insertion Byte 0
1443	TIFE Error Insertion Byte 1
1444	TIFE Error Insertion Byte 2
1445	TIFE Error Insertion Byte 3
1446-144F	Unused
	TRSP
1450	TRSP Configuration
1451	TRSP Register Insertion

Address	Register Description
1452	TRSP Error Insertion
1453	TRSP Transmit J0 and Z0
1454	TRSP Transmit E1 and F1
1455	TRSP Transmit D1D3
1456	TRSP Reserved
1457	TRSP Reserved
1458	TRSP Reserved
1459	TRSP Reserved
145A	TRSP B1 Mask
145B-145F	Unused
1460	TRSP Aux1 Configuration
1461	TRSP Aux1 Register Insertion
1462	TRSP Aux1 Error Insertion
1463	TRSP Aux1 Z0 Transmit
1464-146A	TRSP Aux1 Reserved
146B-146F	Unused
1470	TRSP Aux2 Configuration
1471	TRSP Aux2 Register Insertion
1472	TRSP Aux2 Error Insertion
1473	TRSP Aux2 Z0 Transmit
1474-147A	TRSP Aux2 Reserved
147B-147F	Unused
1480	TRSP Aux3 Configuration
1481	TRSP Aux3 Register Insertion
1482	TRSP Aux3 Error Insertion
1483	TRSP Aux2 Z0 Transmit
1484-148A	TRSP Aux3 Reserved
148B-148F	Unused
	STLI
1490	STLI Clock Configuration
1491	STLI Reserved
1492-149F	Unused
	TXLI
14A0	TXLI Control/Status
14A1	TXLI CSU Control
14A2	TXLI Pattern Register
14A3- 14FF	Unused

Address	Register Description
	CHANNEL 2 RX REGISTERS
	RXLI
1500	RXLI Interrupt Status
1501	RXLI Interrupt Control
1502	RXLI CRU Control
1503	RXLI CRU Clock Training Configuration and Status
1504	RXLI PRBS Control
1505	RXLI Pattern
1506-150F	Unused
	SRLI
1510	SRLI Clock Configuration
1511	SRLI Reserved
1512-151F	Unused
	RRMP
1520	RRMP Configuration
1521	RRMP Status
1522	RRMP Interrupt Enable
1523	RRMP Interrupt Status
1524	RRMP Received APS
1525	RRMP Received SSM
1526	RRMP AIS enable
1527	RRMP Section BIP Error Counter
1528	RRMP Line BIP Error Counter (LSB)
1529	RRMP Line BIP Error Counter (MSB)
152A	RRMP Line REI Error Counter (LSB)
152B	RRMP Line REI Error Counter (MSB)
152C-152F	Unused
1530-1535	RRMP Reserved 2(slave)
1540-1545	RRMP Reserved 3(slave)
1550-1555	RRMP Reserved 4(slave)
1536	RRMP AIS enable 2 (Slave)
1546	RRMP AIS enable 3 (Slave)
1556	RRMP AIS enable 4 (Slave)
1537-153B	RRMP Reserved 2(slave)
1547-154B	RRMP Reserved 3(slave)

Address	Register Description
1557-155B	RRMP Reserved 4(slave)
153C-153F	Unused
154C-154F	Unused
155C-155F	Unused
	RIFD
1560	RIFD Configuration
1561	RIFD Status
1562	RIFD interrupt enable
1563	RIFD interrupt status
1564	RIFD correctable error count LSB
1565	RIFD correctable error count MSB
1566	RIFD Line BIP error count LSB
1567	RIFD Line BIP error count MSB
1568-157F	Unused
	SBER
1580	SBER Configuration
1581	SBER Status
1582	SBER Interrupt Enable
1583	SBER Interrupt Status
1584	SBER SF BERM Accumulation Period (LSB)
1585	SBER SF BERM Accumulation Period (MSB)
1586	SBER SF BERM Saturation Threshold (LSB)
1587	SBER SF BERM Saturation Threshold (MSB)
1588	SBER SF BERM Declaring Threshold (LSB)
1589	SBER SF BERM Declaring Threshold (MSB)
158A	SBER SF BERM Clearing Threshold (LSB)
158B	SBER SF BERM Clearing Threshold (MSB)
158C	SBER SD BERM Accumulation Period (LSB)
158D	SBER SD BERM Accumulation Period (MSB)
158E	SBER SD BERM Saturation Threshold (LSB)
158F	SBER SD BERM Saturation Threshold (MSB)
1590	SBER SD BERM Declaring Threshold (LSB)
1591	SBER SD BERM Declaring Threshold (MSB)
1592	SBER SD BERM Clearing Threshold (LSB)
1593	SBER SD BERM Clearing Threshold (MSB)
1594-15FF	Unused

Address	Register Description
	CHANNEL 3 TX REGISTERS
	QSFIM_2488
1600	QSFIM_2488 Status
1601	QSFIM_2488 Control
1602	QSFIM_2488 Reserved
1603-161F	Unused
1620	Reserved
1621	Reserved
1622-162F	Unused
	RSOP
1630	RSOP Control
1631	RSOP Interrupt Status
1632	RSOP Reserved
1633	RSOP Reserved
1634-163F	Unused
	TIFE
1640	TIFE Configuration
1641	TIFE Control
1642	TIFE Error Insertion Byte 0
1643	TIFE Error Insertion Byte 1
1644	TIFE Error Insertion Byte 2
1645	TIFE Error Insertion Byte 3
1646-164F	Unused
	TRSP
1650	TRSP Configuration
1651	TRSP Register Insertion
1652	TRSP Error Insertion
1653	TRSP Transmit J0 and Z0
1654	TRSP Transmit E1 and F1
1655	TRSP Transmit D1D3
1656	TRSP Reserved
1657	TRSP Reserved
1658	TRSP Reserved

Address	Register Description
1659	TRSP Reserved
165A	TRSP B1 Mask
165B-165F	Unused
1660	TRSP Aux1 Configuration
1661	TRSP Aux1 Register Insertion
1662	TRSP Aux1 Error Insertion
1663	TRSP Aux1 Z0 Transmit
1664-166A	TRSP Aux1 Reserved
166B-166F	Unused
1670	TRSP Aux2 Configuration
1671	TRSP Aux2 Register Insertion
1672	TRSP Aux2 Error Insertion
1673	TRSP Aux2 Z0 Transmit
1674-167A	TRSP Aux2 Reserved
167B-167F	Unused
1680	TRSP Aux3 Configuration
1681	TRSP Aux3 Register Insertion
1682	TRSP Aux3 Error Insertion
1683	TRSP Aux2 Z0 Transmit
1684-168A	TRSP Aux3 Reserved
168B-168F	Unused
	STLI
1690	STLI Clock Configuration
1691	STLI Reserved
1692-169F	Unused
	TXLI
16A0	TXLI Control/Status
16A1	TXLI CSU Control
16A2	TXLI Pattern Register
16A3- 16FF	Unused
	CHANNEL 3 RX REGISTERS
	RXLI
1700	RXLI Interrupt Status
1701	RXLI Interrupt Control
1702	RXLI CRU Control

Address	Register Description
1703	RXLI CRU Clock Training Configuration and Status
1704	RXLI PRBS Control
1705	RXLI Pattern
1706-170F	Unused
	SRLI
1710	SRLI Clock Configuration
1711	SRLI Reserved
1712-171F	Unused
	RRMP
1720	RRMP Configuration
1721	RRMP Status
1722	RRMP Interrupt Enable
1723	RRMP Interrupt Status
1724	RRMP Received APS
1725	RRMP Received SSM
1726	RRMP AIS enable
1727	RRMP Section BIP Error Counter
1728	RRMP Line BIP Error Counter (LSB)
1729	RRMP Line BIP Error Counter (MSB)
172A	RRMP Line REI Error Counter (LSB)
172B	RRMP Line REI Error Counter (MSB)
172C-172F	Unused
1730-1735	RRMP Reserved 2(slave)
1740-1745	RRMP Reserved 3(slave)
1750-1755	RRMP Reserved 4(slave)
1736	RRMP AIS enable 2 (Slave)
1746	RRMP AIS enable 3 (Slave)
1756	RRMP AIS enable 4 (Slave)
1737-173B	RRMP Reserved 2(slave)
1747-174B	RRMP Reserved 3(slave)
1757-175B	RRMP Reserved 4(slave)
173C-173F	Unused
174C-174F	Unused
175C-175F	Unused
	RIFD
1760	RIFD Configuration

Address	Register Description
1761	RIFD Status
1762	RIFD interrupt enable
1763	RIFD interrupt status
1764	RIFD correctable error count LSB
1765	RIFD correctable error count MSB
1766	RIFD Line BIP error count LSB
1767	RIFD Line BIP error count MSB
1768-177F	Unused
	SBER
1780	SBER Configuration
1781	SBER Status
1782	SBER Interrupt Enable
1783	SBER Interrupt Status
1784	SBER SF BERM Accumulation Period (LSB)
1785	SBER SF BERM Accumulation Period (MSB)
1786	SBER SF BERM Saturation Threshold (LSB)
1787	SBER SF BERM Saturation Threshold (MSB)
1788	SBER SF BERM Declaring Threshold (LSB)
1789	SBER SF BERM Declaring Threshold (MSB)
178A	SBER SF BERM Clearing Threshold (LSB)
178B	SBER SF BERM Clearing Threshold (MSB)
178C	SBER SD BERM Accumulation Period (LSB)
178D	SBER SD BERM Accumulation Period (MSB)
178E	SBER SD BERM Saturation Threshold (LSB)
178F	SBER SD BERM Saturation Threshold (MSB)
1790	SBER SD BERM Declaring Threshold (LSB)
1791	SBER SD BERM Declaring Threshold (MSB)
1792	SBER SD BERM Clearing Threshold (LSB)
1793	SBER SD BERM Clearing Threshold (MSB)
1794-1FFF	Unused

Notes on Register Memory Map

1. For all register accesses, CSB must be low.
2. Addresses that are not shown must be treated as Reserved.
3. A[13] is used as the test resister select (TRS) and should be set to logic 0 for all normal mode register accesses.

11 Normal Mode Register Description

Normal mode registers are used to configure and monitor the operation of the CRSU 4x2488. Normal mode registers (as opposed to test mode registers) are selected when A[13] is low.

Notes on Normal Mode Register Bits

1. Writing values into Unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of this product, Unused register bits must be written with logic 0. Reading back Unused bits can produce either a logic 1 or a logic 0; hence, Unused register bits should be masked off by software when read.
2. All configuration bits that can be written into can also be read back. This allows the processor controlling the CRSU 4x2488 to determine the programming state of the device.
3. Writeable normal mode register bits are cleared to logic 0 upon reset unless otherwise noted.
4. Writing into read-only normal mode register bit locations does not affect CRSU 4x2488 operation unless otherwise noted.
5. Certain register bits are reserved. These bits are associated with mega-cell functions that are Unused in this application. To ensure that the CRSU 4x2488 operates as intended, reserved register bits must only be written with the logic level as specified. Writing to reserved registers should be avoided. The recommend procedure to modify any register bit is to first read the register value, modify only the selected bit or bits and write the modified value back to the register. This method ensures that any reserved bits remain unchanged.
6. Register 0014H provides a fixed pattern which software can use to identify the device in the system.

Register 0000H: Identity and Global Performance Monitor Update Trigger

Bit	Type	Function	Default
Bit 15	R	TIP	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	R	TYPE[4]	0
Bit 7	R	TYPE[3]	0
Bit 6	R	TYPE[2]	0
Bit 5	R	TYPE[1]	1
Bit 4	R	TYPE[0]	0
Bit 3	R	REVCODE[3]	0
Bit 2	R	REVCODE[2]	0
Bit 1	R	REVCODE[1]	0
Bit 0	R	REVCODE[0]	1

This register allows the revision number of the CRSU 4X2488 to be read by software permitting graceful migration to newer, feature-enhanced versions of the CRSU 4X2488.

In addition, writing to the CRSU-4X2488 Identity and Global Performance Monitor Update register (0000H) performs a global performance monitor update by simultaneously loading all the performance meter registers in the, RRMP, RIFD blocks.

REVCODE [3:0]

The REVCODE bits can be read to provide a binary CRSU-4X2488 revision number.

REVCODE [3:0]	Revision
0000	A
0001	B

TYPE[4:0]

The TYPE bits can be read to distinguish the CRSU-4X2488 from the other members of the family of devices. The TYPE[4:0] register for the PM5395 CRSU -4X2488 is 00010.

TIP

The TIP bit is set to logic one when the performance meter registers are being loaded. Writing to this register with the DRESET_CH[n] bit in register 0001H equal to logic 0 initiates an accumulation interval transfer and loads all the performance meter registers in the CRSU-4X2488. TIP remains high while the transfer is in progress, and is set to logic zero when the transfer is complete. TIP can be polled by a microprocessor to determine when the accumulation interval transfer is complete.

Register 0001H: Master Reset

Bit	Type	Function	Default
Bit 15	R/W	MREG_RESET	0
Bit 14	R/W	RX_ARSTB_CH3	1
Bit 13	R/W	RX_ARSTB_CH2	1
Bit 12	R/W	RX_ARSTB_CH1	1
Bit 11	R/W	RX_ARSTB_CH0	1
Bit 10	R/W	TX_ARSTB_CH3	1
Bit 9	R/W	TX_ARSTB_CH2	1
Bit 8	R/W	TX_ARSTB_CH1	1
Bit 7	R/W	TX_ARSTB_CH0	1
Bit 6	R/W	QSFI-4_ARSTB	1
Bit 5	R	Unused	X
Bit 4	R	Unused	X
Bit 3	R/W	DRESET_CH3	0
Bit 2	R/W	DRESET_CH2	0
Bit 1	R/W	DRESET_CH1	0
Bit 0	R/W	DRESET_CH0	0

DRESET_CH[3:0]

The DRESET_CH[3:0] bit allows the digital circuitry in the CRSU-4X2488 to be reset under software control. If the corresponding DRESET_CH[3:0] bit is a logic one, all the digital circuitry in channel n, except the Master Registers, is held in reset. This bit is not self-clearing. Therefore, a logic zero must be written to bring the channel out of reset A hardware reset or asserting MREG_RESET clears the DRESET_CH[3:0] bit, thus negating the digital software reset.

QSFI-4_ARSTB

The QSFI-4 Analog Reset bit. When QSFI-4_ARSTB is set to logic zero the QSFI-4 Interface analog circuitry in both the transmit and receive directions and across all four channels is placed into reset. This bit is not self clearing, therefore a logic one must be written to bring the analog circuitry out of reset. A hardware reset sets QSFI-4_ARSTB to logic one clearing any software reset

TX_ARSTB_CH[3:0]

The Transmit Analog Reset bit. When TX_ARSTB_CH[3:0] is set to logic zero all 2.488 GHz Line Side analog circuitry in the transmit side of channel n is placed into reset. This bit is not self-clearing. Therefore, a logic one must be written to bring the analog circuitry out of reset A hardware reset sets the TX_ARSTB_CH[3:0] bit to logic one clearing any software reset. After the power is first applied or after a hardware or software reset the CRSU 4x2488 requires a period of 10 msec before the 2.488 GHz Line Side analog circuitry is within operating specifications.

RX_ARSTB_CH[3:0]

The Receive Analog Reset bit. When RX_ARSTB_CH[3:0] is set to logic zero all 2.488 GHz Line Side analog circuitry in the receive side of channel n is placed into reset. This bit is not self-clearing. Therefore, a logic one must be written to bring the analog circuitry out of reset A hardware reset sets the RX_ARSTB_CH[3:0] bit to logic one clearing any software reset. After the power is first applied or after a hardware or software reset the CRSU 4x2488 requires a period of 10 msec before the 2.488 GHz Line Side analog circuitry is within operating specifications.

MREG_RESET

The Master Register Reset. The MREG_RESET bit resets all master registers to their default values. In order to completely reset all digital circuitry in the device the MREG_RESET must be applied and removed then the DRESET_CH[3:0] must be asserted and removed. If the MREG_RESET bit is a logic one, all the master registers, except register 0001H bit 15, are held in reset. This bit is not self-clearing. Therefore, a logic zero must be written in order to resume normal operation. A hardware reset clears the MREG_RESET bit.

Register 0002H: Master Interrupt Status RX CH0

Bit	Type	Function	Default
Bit 15	R/W	INT_RX_CH0_EN	0
Bit 14	R	Unused	X
Bit 13	R	Unused	X
Bit 12	R	Unused	X
Bit 11	R	Unused	X
Bit 10	R	Unused	X
Bit 9	R	Unused	X
Bit 8	R	Unused	X
Bit 7	R	RRMP_INT_0	0
Bit 6	R	Unused	X
Bit 5	R	RIFD_INT_0	0
Bit 4	R	Unused	X
Bit 3	R	SBER_INT_0	0
Bit 2	R	Unused	X
Bit 1	R	RXLI_INT_0	0
Bit 0	R	Unused	X

This register allows the source of an active interrupt to be identified down to the block level. Further register accesses are required of the block in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

RXLI_INT_0

The RXLI Interrupt Status for channel 0 indicates an interrupt from the 2.488 GHz Line Side Receiver has occurred. The interrupt status bit is set to logic 1 to indicate a pending interrupt. The interrupt status bit is independent of the INT_RX_CH0_EN interrupt enable bit. This bit can only be cleared by removing the underlying interrupt condition in the RXLI block.

SBER_INT_0

The SBER Interrupt Status for channel 0 indicates an interrupt from the Section Bit Error (SBER) block has occurred. The interrupt status bit is set to logic 1 to indicate a pending interrupt. The interrupt status bit is independent of the INT_RX_CH0_EN interrupt enable bit. This bit can only be cleared by removing the underlying interrupt condition in the SBER block.

RIFD_INT_0

The RIFD Interrupt Status for channel 0 indicates an interrupt from the Receive In-band FEC Decoder (RIFD) has occurred. The interrupt status bit is set to logic 1 to indicate a pending interrupt. The interrupt status bit is independent of the INT_RX_CH0_EN interrupt enable bit. This bit can only be cleared by removing the underlying interrupt condition in the RIFD block.

RRMP_INT_0

The RRMP Interrupt Status for channel 0 indicates an interrupt from the Receive Regenerator and Multiplexer section Processor (RRMP) block has occurred. The interrupt status bit is set to logic 1 to indicate a pending interrupt. The interrupt status bit is independent of the INT_RX_CH0_EN interrupt enable bit. This bit can only be cleared by removing the underlying interrupt condition in the RRMP block.

INT_RX_CH0_EN

The interrupt enable for Receive Channel 0 controls the assertion of the interrupt (INTB) output pin. When a logic 1 is written to INT_RX_CH0_EN, the RXLI_INT_0, SBER_INT_0, RIFD_INT_0 or RRMP_INT_0 pending interrupt will assert the interrupt (INTB) output. When a logic 0 is written to INT_RX_CH0_EN, the RXLI_INT_0, SBER_INT_0, RIFD_INT_0 or RRMP_INT_0 pending interrupt will not assert the interrupt (INTB) output.

Register 0003H: Master Interrupt Status RX CH1

Bit	Type	Function	Default
Bit 15	R/W	INT_RX_CH1_EN	0
Bit 14	R	Unused	X
Bit 13	R	Unused	X
Bit 12	R	Unused	X
Bit 11	R	Unused	X
Bit 10	R	Unused	X
Bit 9	R	Unused	X
Bit 8	R	Unused	X
Bit 7	R	RRMP_INT_1	0
Bit 6	R	Unused	X
Bit 5	R	RIFD_INT_1	0
Bit 4	R	Unused	X
Bit 3	R	SBER_INT_1	0
Bit 2	R	Unused	X
Bit 1	R	RXLI_INT_1	0
Bit 0	R	Unused	X

This register allows the source of an active interrupt to be identified down to the block level. Further register accesses are required of the block in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

RXLI_INT_1

The RXLI Interrupt Status for channel 1 indicates an interrupt from the 2.488 GHz Line Side Receiver has occurred. The interrupt status bit is set to logic 1 to indicate a pending interrupt. The interrupt status bit is independent of the INT_RX_CH1_EN interrupt enable bit. This bit can only be cleared by removing the underlying interrupt condition in the RXLI block.

SBER_INT_1

The SBER Interrupt Status for channel 1 indicates an interrupt from the Section Bit Error (SBER) block has occurred. The interrupt status bit is set to logic 1 to indicate a pending interrupt. The interrupt status bit is independent of the INT_RX_CH1_EN interrupt enable bit. This bit can only be cleared by removing the underlying interrupt condition in the SBER block.

RIFD_INT_1:

The RIFD Interrupt Status for channel 1 indicates an interrupt from the Receive In-band FEC Decoder (RIFD) has occurred. The interrupt status bit is set to logic 1 to indicate a pending interrupt. The interrupt status bit is independent of the INT_RX_CH1_EN interrupt enable bit. This bit can only be cleared by removing the underlying interrupt condition in the RIFD block.

RRMP_INT_1

The RRMP Interrupt Status for channel 1 indicates an interrupt from the Receive Regenerator and Multiplexer section Processor (RRMP) block has occurred. The interrupt status bit is set to logic 1 to indicate a pending interrupt. The interrupt status bit is independent of the INT_RX_CH1_EN interrupt enable bit. This bit can only be cleared by removing the underlying interrupt condition in the RRMP block.

INT_RX_CH1_EN

The interrupt enable for Receive Channel 1 controls the assertion of the interrupt (INTB) output pin. When a logic 1 is written to INT_RX_CH1_EN, the RXLI_INT_1, SBER_INT_1, RIFD_INT_1 or RRMP_INT_1 pending interrupt will assert the interrupt (INTB) output. When a logic 0 is written to INT_RX_CH1_EN, the RXLI_INT_1, SBER_INT_1, RIFD_INT_1 or RRMP_INT_1 pending interrupt will not assert the interrupt (INTB) output.

Register 0004H: Master Interrupt Status RX CH2

Bit	Type	Function	Default
Bit 15	R/W	INT_RX_CH2_EN	0
Bit 14	R	Unused	X
Bit 13	R	Unused	X
Bit 12	R	Unused	X
Bit 11	R	Unused	X
Bit 10	R	Unused	X
Bit 9	R	Unused	X
Bit 8	R	Unused	X
Bit 7	R	RRMP_INT_2	0
Bit 6	R	Unused	X
Bit 5	R	RIFD_INT_2	0
Bit 4	R	Unused	X
Bit 3	R	SBER_INT_2	0
Bit 2	R	Unused	X
Bit 1	R	RXLI_INT_2	0
Bit 0	R	Unused	X

This register allows the source of an active interrupt to be identified down to the block level. Further register accesses are required of the block in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

RXLI_INT_2

The RXLI Interrupt Status for channel 2 indicates an interrupt from the 2.488 GHz Line Side Receiver has occurred. The interrupt status bit is set to logic 1 to indicate a pending interrupt. The interrupt status bit is independent of the INT_RX_CH2_EN interrupt enable bit. This bit can only be cleared by removing the underlying interrupt condition in the RXLI block.

SBER_INT_2

The SBER Interrupt Status for channel 2 indicates an interrupt from the Section Bit Error (SBER) block has occurred. The interrupt status bit is set to logic 1 to indicate a pending interrupt. The interrupt status bit is independent of the INT_RX_CH2_EN interrupt enable bit. This bit can only be cleared by removing the underlying interrupt condition in the SBER block.

RIFD_INT_2

The RIFD Interrupt Status for channel 2 indicates an interrupt from the Receive In-band FEC Decoder (RIFD) has occurred. The interrupt status bit is set to logic 1 to indicate a pending interrupt. The interrupt status bit is independent of the INT_RX_CH2_EN interrupt enable bit. This bit can only be cleared by removing the underlying interrupt condition in the RIFD block.

RRMP_INT_2

The RRMP Interrupt Status for channel 2 indicates an interrupt from the Receive Regenerator and Multiplexer section Processor (RRMP) block has occurred. The interrupt status bit is set to logic 1 to indicate a pending interrupt. The interrupt status bit is independent of the INT_RX_CH2_EN interrupt enable bit. This bit can only be cleared by removing the underlying interrupt condition in the RRMP block.

INT_RX_CH2_EN

The interrupt enable for Receive Channel 2 controls the assertion of the interrupt (INTB) output pin. When a logic 1 is written to INT_RX_CH2_EN, the RXLI_INT_2, SBER_INT_2, RIFD_INT_2 or RRMP_INT_2 pending interrupt will assert the interrupt (INTB) output. When a logic 0 is written to INT_RX_CH2_EN, the RXLI_INT_2, SBER_INT_2, RIFD_INT_2 orRRMP_INT_2 pending interrupt will not assert the interrupt (INTB) output.

Register 0005H: Master Interrupt Status RX CH3

Bit	Type	Function	Default
Bit 15	R/W	INT_RX_CH3_EN	0
Bit 14	R	Unused	X
Bit 13	R	Unused	0
Bit 12	R	Unused	X
Bit 11	R	Unused	0
Bit 10	R	Unused	X
Bit 9	R	Unused	0
Bit 8	R	Unused	X
Bit 7	R	RRMP_INT_3	0
Bit 6	R	Unused	X
Bit 5	R	RIFD_INT_3	0
Bit 4	R	Unused	X
Bit 3	R	SBER_INT_3	0
Bit 2	R	Unused	X
Bit 1	R	RXLI_INT_3	0
Bit 0	R	Unused	X

This register allows the source of an active interrupt to be identified down to the block level. Further register accesses are required of the block in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

RXLI_INT_3

The RXLI Interrupt Status for channel 3 indicates an interrupt from the 2.488 GHz Line Side Receiver has occurred. The interrupt status bit is set to logic 1 to indicate a pending interrupt. The interrupt status bit is independent of the INT_RX_CH3_EN interrupt enable bit. This bit can only be cleared by removing the underlying interrupt condition in the RXLI block.

SBER_INT_3

The SBER Interrupt Status for channel 3 indicates an interrupt from the Section Bit Error (SBER) block has occurred. The interrupt status bit is set to logic 1 to indicate a pending interrupt. The interrupt status bit is independent of the INT_RX_CH3_EN interrupt enable bit. This bit can only be cleared by removing the underlying interrupt condition in the SBER block.

RIFD_INT_3

The RIFD Interrupt Status for channel 3 indicates an interrupt from the Receive In-band FEC Decoder (RIFD) has occurred. The interrupt status bit is set to logic 1 to indicate a pending interrupt. The interrupt status bit is independent of the INT_RX_CH3_EN interrupt enable bit. This bit can only be cleared by removing the underlying interrupt condition in the RIFD block.

RRMP_INT_3

The RRMP Interrupt Status for channel 3 indicates an interrupt from the Receive Regenerator and Multiplexer section Processor (RRMP) block has occurred. The interrupt status bit is set to logic 1 to indicate a pending interrupt. The interrupt status bit is independent of the INT_RX_CH3_EN interrupt enable bit. This bit can only be cleared by removing the underlying interrupt condition in the RRMP block.

INT_RX_CH3_EN

The interrupt enable for Receive Channel 3 controls the assertion of the interrupt (INTB) output pin. When a logic 1 is written to INT_RX_CH3_EN, the RXLI_INT_3, SBER_INT_3, RIFD_INT_3 or RRMP_INT_3 pending interrupt will assert the interrupt (INTB) output. When a logic 0 is written to INT_RX_CH3_EN, the RXLI_INT_3, SBER_INT_3, RIFD_INT_3 or RRMP_INT_3 pending interrupt will not assert the interrupt (INTB) output.

Register 0006H: Master Interrupt Status TX CH0

Bit	Type	Function	Default
Bit 15	R/W	INT_TX_CH0_EN	0
Bit 14	R	Unused	X
Bit 13	R	TXLI_INT_0	0
Bit 12	R	Unused	X
Bit 11	R	RSOP_INT_0	0
Bit 10	R	Unused	X
Bit 9	R	Unused	X
Bit 8	R	Unused	X
Bit 7	R	Unused	X
Bit 6	R	Unused	X
Bit 5	R	Unused	X
Bit 4	R	Unused	X
Bit 3	R	Unused	X
Bit 2	R	Unused	X
Bit 1	R	Unused	X
Bit 0	R	Unused	X

This register allows the source of an active interrupt to be identified down to the block level. Further register accesses are required of the block in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

RSOP_INT_0

The RSOP Interrupt Status for channel 0 indicates an interrupt from the Receive Section Overhead Processor (RSOP) block has occurred. The interrupt status bit is set to logic 1 to indicate a pending interrupt. The interrupt status bit is independent of the INT_TX_CH0_EN interrupt enable bit. This bit can only be cleared by removing the underlying interrupt condition in the RSOP block.

TXLI_INT_0

The TXLI Interrupt Status for channel 0 indicates an interrupt from the 2.488 GHz Line Side Transmitter has occurred. The interrupt status bit is set to logic 1 to indicate a pending interrupt. The interrupt status bit is independent of the INT_TX_CH0_EN interrupt enable bit. This bit can only be cleared by removing the underlying interrupt condition in the TXLI block.

INT_TX_CH0_EN

The interrupt enable for the Transmitter section of Channel 0 controls the assertion of the interrupt (INTB) output pin. When a logic 1 is written to INT_TX_CH0_EN, the TXLI_INT_0 or RSOP_INT_0 pending interrupt will assert the interrupt (INTB) output. When a logic 0 is written to INT_TX_CH0_EN, the TXLI_INT_0 or RSOP_INT_0 pending interrupt will not assert the interrupt (INTB) output.

Register 0007H: Master Interrupt Status TX CH1

Bit	Type	Function	Default
Bit 15	R/W	INT_TX_CH1_EN	0
Bit 14	R	Unused	X
Bit 13	R	TXLI_INT_1	0
Bit 12	R	Unused	X
Bit 11	R	RSOP_INT_1	0
Bit 10	R	Unused	X
Bit 9	R	Unused	X
Bit 8	R	Unused	X
Bit 7	R	Unused	X
Bit 6	R	Unused	X
Bit 5	R	Unused	X
Bit 4	R	Unused	X
Bit 3	R	Unused	X
Bit 2	R	Unused	X
Bit 1	R	Unused	X
Bit 0	R	Unused	X

This register allows the source of an active interrupt to be identified down to the block level. Further register accesses are required of the block in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

RSOP_INT_1

The RSOP Interrupt Status for channel 1 indicates an interrupt from the Receive Section Overhead Processor (RSOP) block has occurred. The interrupt status bit is set to logic 1 to indicate a pending interrupt. The interrupt status bit is independent of the INT_TX_CH1_EN interrupt enable bit. This bit can only be cleared by removing the underlying interrupt condition in the RSOP block.

TXLI_INT_1

The TXLI Interrupt Status for channel 1 indicates an interrupt from the 2.488 GHz Line Side Transmitter has occurred. The interrupt status bit is set to logic 1 to indicate a pending interrupt. The interrupt status bit is independent of the INT_TX_CH1_EN interrupt enable bit. This bit can only be cleared by removing the underlying interrupt condition in the TXLI block.

INT_TX_CH1_EN

The interrupt enable for the Transmitter section of Channel 1 controls the assertion of the interrupt (INTB) output pin. When a logic 1 is written to INT_TX_CH1_EN, the TXLI_INT_1 or RSOP_INT_1 pending interrupt will assert the interrupt (INTB) output. When a logic 0 is written to INT_TX_CH1_EN, the TXLI_INT_1 or RSOP_INT_1 pending interrupt will not assert the interrupt (INTB) output.

Register 0008H: Master Interrupt Status TX CH2

Bit	Type	Function	Default
Bit 15	R/W	INT_TX_CH2_EN	0
Bit 14	R	Unused	X
Bit 13	R	TXLI_INT_2	0
Bit 12	R	Unused	X
Bit 11	R	RSOP_INT_2	0
Bit 10	R	Unused	X
Bit 9	R	Unused	X
Bit 8	R	Unused	X
Bit 7	R	Unused	X
Bit 6	R	Unused	X
Bit 5	R	Unused	X
Bit 4	R	Unused	X
Bit 3	R	Unused	X
Bit 2	R	Unused	X
Bit 1	R	Unused	X
Bit 0	R	Unused	X

This register allows the source of an active interrupt to be identified down to the block level. Further register accesses are required of the block in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

RSOP_INT_2

The RSOP Interrupt Status for channel 2 indicates an interrupt from the Receive Section Overhead Processor (RSOP) block has occurred. The interrupt status bit is set to logic 1 to indicate a pending interrupt. The interrupt status bit is independent of the INT_TX_CH2_EN interrupt enable bit. This bit can only be cleared by removing the underlying interrupt condition in the RSOP block.

TXLI_INT_2

The TXLI Interrupt Status for channel 2 indicates an interrupt from the 2.488 GHz Line Side Transmitter has occurred. The interrupt status bit is set to logic 1 to indicate a pending interrupt. The interrupt status bit is independent of the INT TX_CH2_EN interrupt enable bit. This bit can only be cleared by removing the underlying interrupt condition in the TXLI block.

INT_TX_CH2_EN

The interrupt enable for the Transmitter section of Channel 2 controls the assertion of the interrupt (INTB) output pin. When a logic 1 is written to INT_TX_CH2_EN, the TXLI_INT_2 or RSOP_INT_2 pending interrupt will assert the interrupt (INTB) output. When a logic 0 is written to INT_TX_CH2_EN, the TXLI_INT_2 or RSOP_INT_2 pending interrupt will not assert the interrupt (INTB) output.

Register 0009H: Master Interrupt Status TX CH3

Bit	Type	Function	Default
Bit 15	R/W	INT_TX_CH3_EN	0
Bit 14	R	Unused	X
Bit 13	R	TXLI_INT_CH3	0
Bit 12	R	Unused	X
Bit 11	R	RSOP_INT_CH3	0
Bit 10	R	Unused	X
Bit 9	R	Unused	X
Bit 8	R	Unused	X
Bit 7	R	Unused	X
Bit 6	R	Unused	X
Bit 5	R	Unused	X
Bit 4	R	Unused	X
Bit 3	R	Unused	X
Bit 2	R	Unused	X
Bit 1	R	Unused	X
Bit 0	R	Unused	X

This register allows the source of an active interrupt to be identified down to the block level. Further register accesses are required of the block in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

RSOP_INT_3

The RSOP Interrupt Status for channel 3 indicates an interrupt from the Receive Section Overhead Processor (RSOP) block has occurred. The interrupt status bit is set to logic 1 to indicate a pending interrupt. The interrupt status bit is independent of the INT_TX_CH3_EN interrupt enable bit. This bit can only be cleared by removing the underlying interrupt condition in the RSOP block.

TXLI_INT_3

The TXLI Interrupt Status for channel 3 indicates an interrupt from the 2.488 GHz Line Side Transmitter has occurred. The interrupt status bit is set to logic 1 to indicate a pending interrupt. The interrupt status bit is independent of the INT_TX_CH3_EN interrupt enable bit. This bit can only be cleared by removing the underlying interrupt condition in the TXLI block.

INT_TX_CH3_EN

The interrupt enable for the Transmitter section of Channel 3 controls the assertion of the interrupt (INTB) output pin. When a logic 1 is written to INT_TX_CH3_EN, the TXLI_INT_3 or RSOP_INT_3 pending interrupt will assert the interrupt (INTB) output. When a logic 0 is written to INT_TX_CH3_EN, the TXLI_INT_3 or RSOP_INT_3 pending interrupt will not assert the interrupt (INTB) output.

Register 000AH: Channel Interrupt Status

Bit	Type	Function	Default
Bit 15	R	TX_INT_CH3	0
Bit 14	R	TX_INT_CH2	0
Bit 13	R	TX_INT_CH1	0
Bit 12	R	TX_INT_CH0	0
Bit 11	R	RX_INT_CH3	0
Bit 10	R	RX_INT_CH2	0
Bit 9	R	RX_INT_CH1	0
Bit 8	R	RX_INT_CH0	0
Bit 7	R	QSFIM_INT_CH3	0
Bit 6	R	QSFIM_INT_CH2	0
Bit 5	R	QSFIM_INT_CH1	0
Bit 4	R	QSFIM_INT_CH0	0
Bit 3	R	Unused	X
Bit 2	R	Unused	X
Bit 1	R	Unused	X
Bit 0	R	Unused	X

This register allows the source of an active interrupt to be identified down to a single channel of the CRSU 4x2488. Further register accesses are required of the channel in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

QSFIM_INT_CH[3:0]

The QSFIM Interrupt Status for channel 3..0 indicates an interrupt from the QSFIM_2488 interface block has occurred. The interrupt status bit is set to logic 1 to indicate a pending interrupt. The interrupt status bit is independent of the interrupt enable bit. This bit can only be cleared by removing the underlying interrupt condition in the QSFIM_2488 block.

RX_INT_CH[3:0]

The Receive Interrupt Status for channel 3..0 indicates an interrupt in the Master Interrupt Status RX CH3..0 Register is active. The interrupt status bit is set to logic 1 to indicate when any bit in register is set. Software can determine which of the channels is the source of the INTB interrupt by interrogating this register. This bit can only be cleared by removing the underlying interrupt condition in the Master Interrupt Status RX CH3..0 Register. Note: In order to clear the Master Interrupt Status RX CH3..0 Register the associated block level interrupt registers must be cleared.

TX_INT_CH[3:0]

The Transmit Interrupt Status for channel 3..0 indicates an interrupt in the Master Interrupt Status TX CH3..0 Register is active. The interrupt status bit is set to logic 1 to indicate a any bit in register is set. Software can determine which of the channels is the source of the INTB interrupt by interrogating this register. This bit can only be cleared by removing the underlying interrupt condition in the Master Interrupt Status TX CH3..0 Register. Note: In order to clear the Master Interrupt Status TX CH3..0 Register the associated block level interrupt registers must be cleared.

Register 000BH: Configuration

Bit	Type	Function	Default
Bit 15	R	Unused	0
Bit 14	R/W	SYNC_ERR_INV	0
Bit 13	R/W	PHASE_ERR_INV	0
Bit 12	R/W	WCIMODE	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R	Reserved	0
Bit 6	R	Reserved	0
Bit 5	R	Reserved	0
Bit 4	R	Reserved	0
Bit 3	R	Reserved	0
Bit 2	R	Reserved	0
Bit 1	R	Reserved	0
Bit 0	R	Reserved	0

WCIMODE

The write on clear interrupt mode (WCIMODE) bit selects the clear interrupt mode. When a logic 1 is written to WCIMODE, the clear interrupt mode is clear on write. In this mode of operation a logic 1 must be written to clear the active interrupt bit. When a logic 0 is written to WCIMODE, the clear interrupt mode is clear on read. In this mode of operation the act of reading the active interrupt clears the bit. The WCIMODE bit effects the operation of all Interrupt Register Bits in the CRSU 4x2488.

PHASE_ERR_INV

The PHASE_ERR pin inversion bit will invert the polarity of all the PHASE_ERR[3:0] output pins. After a reset the PHASE_ERR[3:0] pins are an active high signal. Setting this bit to a logic 1 will change the PHASE_ERR[3:0] pins to operate as an active low signal.

SYNC_ERR_INV

The SYNC_ERR pin inversion bit will invert the polarity of all the SYNC_ERR[3:0] output pins. After a reset the SYNC_ERR[3:0] pins are an active high signal. Setting this bit to a logic 1 will change the SYNC_ERR[3:0] pins to operate as an active low signal. The SYNC_ERR[3:0] pins can be enabled or disabled by the SYNC_ERR_EN_CH[3:0] bits 3 to 0 Register 0013H.

Register 000CH: Bypass and fiber order

Bit	Type	Function	Default
Bit 15	R/W	Reserved	1
Bit 14	R/W	Reserved	1
Bit 13	R/W	Reserved	1
Bit 12	R/W	Reserved	1
Bit 11	R/W	TIFE_BYPASS_CH3	0
Bit 10	R/W	TIFE_BYPASS _CH2	0
Bit 9	R/W	TIFE_BYPASS _CH1	0
Bit 8	R/W	TIFE_BYPASS _CH0	0
Bit 7	R/W	RX_BYPASS_CH3	1
Bit 6	R/W	RX_BYPASS_CH2	1
Bit 5	R/W	RX_BYPASS_CH1	1
Bit 4	R/W	RX_BYPASS_CH0	1
Bit 3	R/W	TX_BYPASS_CH3	1
Bit 2	R/W	TX_BYPASS_CH2	1
Bit 1	R/W	TX_BYPASS_CH1	1
Bit 0	R/W	TX_BYPASS_CH0	1

TX_BYPASS_CH[3:0]

Transmit Bypass mode selection bit. When TX_BYPASS[3:0] is set to logic one all SONET processing blocks on the transmit side of the channel are bypassed. When enabled data is passed directly from the QSFIM_2488 interface to 2.488 GHz Line Side transmitter without processing. When TX_BYPASS[3:0] is set to logic zero the data is processed by the SRLI, RSOP, TIFE, TRSP and STLI blocks.

RX_BYPASS_CH[3:0]

Receive Bypass mode selection bit. When RX_BYPASS[3:0] is set to logic one all SONET processing blocks on the receive side of the channel are bypassed. When enabled data is passed directly from the 2.488 GHz Line Side Receiver to QSFIM_2488 interface without processing. When RX_BYPASS[3:0] is set to logic zero the data is processed by the SRLI, RRMP and RIFD blocks.

Note: The error monitoring performed by the RRMP and SBER remains functional even if the RX_BYPASS_CH[3:0] is enable. In this mode data from the Receive line interface can be monitored for errors but will not alter the data stream passing through the device. Optionally the RRMP and SBER can be disabled using the clock control bits in register 000EH.

TIFE_BYPASS_CH[3:0]

This register bit controls the state of the TIFE. When TIFE_BYPASS_CH[3:0] is set to logic one the TIFE is placed in a zero-delay mode wherein the data and frame pulse outputs are equal to the data and frame pulse inputs delayed by two clock cycles. While in this mode, no bytes in the frame are modified by TIFE. Transitions into and out of this state can cause errors in the current frame. **Note: When TIFE_BYPASS_CH[3:0] is set to logic one it overrides the value set in register 1140H. Setting this bit to logic is equivalent to setting the TIFE into state 3.**

Register 000DH: Diagnostic Loopback and ICO control

Bit	Type	Function	Default
Bit 15	R/W	Reserved	1
Bit 14	R/W	Reserved	1
Bit 13	R/W	Reserved	1
Bit 12	R/W	Reserved	1
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	SPLE_CH3	0
Bit 6	R/W	SPLE_CH2	0
Bit 5	R/W	SPLE_CH1	0
Bit 4	R/W	SPLE_CH0	0
Bit 3	R/W	Unused	X
Bit 2	R/W	ICO_CTRL_1	1
Bit 1	R/W	ICO_CTRL_0	0
Bit 0	R/W	Reserved	0

ICO_CTRL_0

ICO_CTRL_1

These register bits control the ICO swing control logic within the CSU and CRU in order to minimize the loop-time intrinsic jitter and normal mode intrinsic jitter on all channels.
NOTE: these bits are required to be programmed when LOOPTIME operation is required. See operations section 13.7 for looptime configuration setup.

ico_crtl_1	ico_crtl_0	
1	1	Nominal ICO Swing
1	0	10% ICO swing increase **(DEFAULT)**
0	1	20% ICO swing increase **(LOOP-TIME MODE)**
0	0	30% ICO swing increase

SPLE_CH[3:0]

The System Side Parallel Loopback, SPLE bit enables the CRSU 4x2488 loopback where the transmitter STLI block is directly connected to its receiver SRLI block. This bit loops the data received on theQSFI-4 TXDATA interface back theQSFI-4 RXDATA signals after it has past through all the SONET processing blocks. When SPLE is logic one, loopback is enabled. Under this operating condition, the CRSU 4x2488 continues to operate normally in the 2.488 GHz Line Side transmit direction but data input into the 2.488 GHz Line Side Receiver is ignored. When SPLE is logic zero, the CRSU 4x2488 operates normally. **NOTE: This loopback mode only works when the Transmit and Receive side By-Pass modes (Register 000C bits 0 to 7) are disabled. The SPLE will not work in pure SERDES mode.**

DESCRAMBLE_DELAY_CH[3:0]

The descramble delay bit will ensure that frame descrambling is not asserted until three frames have passed with correct frame alignment bytes. This will ensure that any downstream framers will not try and frame to any framing pattern alias that may be contained in the payload. When DESCRAMBLE_DELAY_CH[3:0] is logic 1, the descramble delay will be enabled i.e the descrambler will not be enabled for three frames after frame alignment.

Register 000EH: Clock Control

Bit	Type	Function	Default
Bit 15	R/W	KILL_RRMP_CLK_CH3	1
Bit 14	R/W	KILL_RRMP_CLK_CH2	1
Bit 13	R/W	KILL_RRMP_CLK_CH1	1
Bit 12	R/W	KILL_RRMP_CLK_CH0	1
Bit 11	R/W	KILL_RIFD_CLK_CH3	1
Bit 10	R/W	KILL_RIFD_CLK_CH2	1
Bit 9	R/W	KILL_RIFD_CLK_CH1	1
Bit 8	R/W	KILL_RIFD_CLK_CH0	1
Bit 7	R/W	KILL_TX_CLK_CH3	1
Bit 6	R/W	KILL_TX_CLK_CH2	1
Bit 5	R/W	KILL_TX_CLK_CH1	1
Bit 4	R/W	KILL_TX_CLK_CH0	1
Bit 3	R/W	KILL_RX_CLK_CH3	1
Bit 2	R/W	KILL_RX_CLK_CH2	1
Bit 1	R/W	KILL_RX_CLK_CH1	1
Bit 0	R/W	KILL_RX_CLK_CH0	1

KILL_RX_CLK_CH[3:0]

The Kill Receive clock register bit stops the receive side clock of the selected channel. When KILL_RX_CLK_CH[3:0] is enabled the clock to the SRLI, RRMP, SBER and RIFD is held at a constant value. Stopping the clock prevents the blocks from operating and thus greatly reduces the power consumed by the blocks. Enabling KILL_RX_CLK_CH[3:0] does not effect the operation of the transmit side of the channel.

Note: If KILL_RX_CLK_CH[3:0] is enabled the RX_BYPASS_CH[3:0] bits in Register 000CH must be enabled in order for data to flow from the Receive Line side RXD+/- inputs to the QSFI-4 Interface RXDATA outputs.

KILL_TX_CLK_CH[3:0]

The Kill Transmit clock register bit stops the transmit side clock of the selected channel. When KILL_TX_CLK_CH[3:0] is enabled the clock to the SRLI, RSOP, TIFE, TRSP and STLI is held at a constant value. Stopping the clock prevents the blocks from operating and thus greatly reduces the power consumed by the blocks. Enabling KILL_TX_CLK_CH[3:0] does not effect the operation of the receive side of the channel.

Note: If KILL_TX_CLK_CH[3:0] is enabled the TX_BYPASS_CH[3:0] bits in Register 000CH must be enabled in order for data to flow from the QSFI-4 Interface TXDATA inputs to the Transmit Line Side TXD+/- outputs.

KILL_RIFD_CLK_CH[3:0]

The Kill the RIFD clock register bit stops the RIFD block clock of the selected channel. When KILL_RIFD_CLK_CH[3:0] is enabled the clock to the RIFD is held at a constant value. Stopping the clock prevents the block from operating and thus greatly reduces the power consumed. Enabling KILL_RIFD_CLK_CH[3:0] does not effect the operation of the transmit side of the channel.

Note: If KILL_RIFD_CLK_CH[3:0] is enabled the RX_BYPASS_CH[3:0] bits in Register 000CH must be enabled in order for data to flow from the Receive Line side RXD+/- inputs to the QSFI-4 Interface RXDATA outputs. When enabled the SRLI, RRMP and SBER are still operational and can be used for error monitoring purposes.

KILL_RRMP_CLK_CH[3:0]

The Kill the RRMP clock register bit stops the RRMP block clock of the selected channel. When KILL_RRMP_CLK_CH[3:0] is enabled the clock to the RRMP is held at a constant value. Stopping the clock prevents the block from operating and thus greatly reduces the power consumed. Enabling KILL_RRMP_CLK_CH[3:0] does not effect the operation of the transmit side of the channel.

Note: If KILL_RRMP_CLK_CH[3:0] is enabled the RX_BYPASS_CH[3:0] bits in Register 000CH must be enabled in order for data to flow from the Receive Line side RXD+/- inputs to the QSFIM Interface RXDATA outputs. When enabled the RRMP and SBER are not operational and can not be used for error monitoring purposes. Enabling the KILL_RRMP_CLK_CH[3:0] and KILL_RIFD_CLK_CH[3:0] is equivalent to enabling the KILL_RX_CLK_CH[3:0].

Register 000FH: Bypass and Loop-across

Bit	Type	Function	Default
Bit 15	R/W	LBEN_CH3	0
Bit 14	R/W	LBEN_CH2	0
Bit 13	R/W	LBEN_CH1	0
Bit 12	R/W	LBEN_CH0	0
Bit 11	R/W	CHLBEN_CH3	0
Bit 10	R/W	CHLBEN_CH2	0
Bit 9	R/W	CHLBEN_CH1	0
Bit 8	R/W	CHLBEN_CH0	0
Bit 7	R/W	ERRCNT_CH3	1
Bit 6	R/W	ERRCNT_CH2	1
Bit 5	R/W	ERRCNT_CH1	1
Bit 4	R/W	ERRCNT_CH0	1
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

ERRCNT_CH[3:0]

The BIP Error Count register bit selects the source of the BIP error count value for the last frame. When ERRCNT_CH[3:0] is set to logic one the SBER error count value is received from the RRMP. When ERRCNT_CH[3:0] is set logic zero the SBER error count value is received from the RIFD. The ERRCNT_CH[3:0] bit must be set to logic zero when the receive FEC is enabled in the RIFD.

If the FEC encoder is enabled this bit should set to logic zero so that the SBER receives the error count after the frame is corrected. If the FEC encoder is not used than this bit should be set to logic one so that the SBER receives the error count from the RRMP. If the SBER count is to be based on the uncorrected frame rather than the corrected frame this be may be set the logic one even if the FEC decoder is enabled.

CHLBEN_CH[3:0]

QSFIM_2488 Interface Channel to Channel Loop-Back Enable (CHLBEN_CH). The CHLBEN_CH[n] bit connects the Receive path of one Channel to the Transmit path of the associated Channel. The following table lists the modes of operation when each CHLBEN_CH[3:0] bit is set to logic one:

CHLBEN Bit Connection

Receive Path of Channel 1 to Transmit Path of Channel 0

Receive Path of Channel 0 to Transmit Path of Channel 1

Receive Path of Channel 3 to Transmit Path of Channel 2

Receive Path of Channel 2 to Transmit Path of Channel 3

When CHLBEN_CH[n] is logic 1 the Data from the Receive Line side RXD[n]+/- input of one channel is routed to the Transmit Line side TXD[n]+/- output pin of the associated channel through the QSFIM_2488 interconnect block. The CHLBEN_CH[3:0] connects data from either the RRMP-RIFD path or the Receive Bypass mode to either the TIFE-TRSP path or the Transmit Bypass mode. The CHLBEN_CH[3:0] is not effected by any of the kill clock control bits in Register 000EH. When CHLBEN_CH[3:0] is enabled the data from the QSFI-4 TXDATA inputs are ignored. **Note: The associated LBEN_CH[3:0] bit must also be set to logic 1 for the cross-channel loopback to operate correctly. See section 13.12 Line side, Channel to Channel Loopback Operation for complete configuration**
LBEN_CH[3:0]

QSFIM_2488 Interface Loop-Back Enable for channel n (LBEN_CH). The LBEN_CH[n] pin selects the Receive to Transmit loop-back mode of operation. When LBEN_CH[n] is logic 1 the Data from the Receive Line side RXD[n]+/- input is routed to the Transmit Line side TXD[n]+/- output pin through the QSFIM interconnect block. The LBEN[3:0] connects data from either the RRMP-RIFD path or the Receive Bypass mode to either the TIFE-TRSP path or the Transmit Bypass mode. The LBEN_CH[3:0] is not effected by any of the kill clock control bits in Register 000EH. When LBEN_CH[3:0] is enabled the data from the QSFI-4 TXDATA inputs are ignored. **Note: LOOPTIME CH[3:0] must be configured when LEBN_CH[3:0] is enabled**. **see 13.11 Line Side, same Channel Loopback Operation**

Register 0010H: Diagnostics#1

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	DS_CH3	0
Bit 6	R/W	DS_CH2	0
Bit 5	R/W	DS_CH1	0
Bit 4	R/W	DS_CH0	0
Bit 3	R/W	DD_CH3	0
Bit 2	R/W	DD_CH2	0
Bit 1	R/W	DD_CH1	0
Bit 0	R/W	DD_CH0	0

DD_CH[3:0]

The Disable Descrambling (DD) bit is used to disable SONET descrambling performed by the RRMP block. When set to logic 1, SONET descrambling is disabled. When set to logic 0, SONET descrambling is enabled. For normal operation, this bit should be set to logic zero.

DS_CH[3:0]

The Disable Scrambling (DS) bit is used to disable SONET scrambling performed by the TRSP block. When set to logic 1, SONET scrambling is disabled. When set to logic 0, SONET scrambling is enabled. For normal operation, this bit should be set to logic zero.

Register 0011H: Channel 3 and 2 SALM Enables

Bit	Type	Function	Default
Bit 15	R/W	OOF_EN_CH3	0
Bit 14	R/W	LOS_RRMP_EN_CH3	0
Bit 13	R/W	LOS_RXLI_EN_CH3	1
Bit 12	R/W	LOF_EN_CH3	0
Bit 11	R/W	LAIS_EN_CH3	0
Bit 10	R/W	LRDI_EN_CH3	0
Bit 9	R/W	SF_EN_CH3	0
Bit 8	R/W	SD_EN_CH3	0
Bit 7	R/W	OOF_EN_CH2	0
Bit 6	R/W	LOS_RRMP_EN_CH2	0
Bit 5	R/W	LOS_RXLI_EN_CH2	1
Bit 4	R/W	LOF_EN_CH2	0
Bit 3	R/W	LAIS_EN_CH2	0
Bit 2	R/W	LRDI_EN_CH2	0
Bit 1	R/W	SF_EN_CH2	0
Bit 0	R/W	SD_EN_CH2	0

SD_EN_CH2

The SALM[2] Signal Degrade enable. The SD_EN_CH2 enables the reporting of Signal Degrade alarms on the section alarm SALM[2] output pin. When SD_EN_CH2 is set to logic one signal degrade alarms from the SBER will set the SALM[2] pin to logic 1. The SALM[2] will remain high until the value set in the SBER SD BERM clearing threshold register is reached. When SD_EN_CH2 is set to logic 0 SD alarms have no effect on the state of SALM[2].

SF_EN_CH2

The SALM[2] Signal Fail enable. The SF_EN_CH2 enables the reporting of Signal Fail alarms on the section alarm SALM[2] output pin. When SF_EN_CH2 is set to logic one signal fail alarms from the SBER will set the SALM[2] pin to logic 1. The SALM[2] will remain high until the value set in the SBER SF BERM Clearing Threshold Register is reached. When SF_EN_CH2 is set to logic 0 signal fail alarms have no effect on the state of SALM[2].

LRDI_EN_CH2

The SALM[2] Line Remote Defect Indication enable. The LRDI_EN_CH2 enables the reporting of LRDI alarms on the section alarm SALM[2] output pin. When LRDI_EN_CH2 is set to logic one LRDI alarms from the RRMP will set the SALM[2] pin to logic 1. The SALM[2] will remain high until the LRDI pattern is removed from the K2 byte for three or five consecutive frames. When LRDI_EN_CH2 is set to logic 0 Line Remote Defect alarms have no effect on the state of SALM[2].

LAIS_EN_CH2

The SALM[2] Line Alarm Indication Status enable. The LAIS_EN_CH2 enables the reporting of LAIS alarms on the section alarm SALM[2] output pin. When LAIS_EN_CH2 is set to logic one LAIS alarms from the RRMP will set the SALM[2] pin to logic 1. The SALM[2] will remain high until the LAIS pattern is removed from the K2 byte for three or five consecutive frames. When LAIS_EN_CH2 is set to logic 0 LAIS alarms have no effect on the state of SALM[2].

LOF_EN_CH2

The SALM[2] Loss Of Frame Status enable. The LOF_EN_CH2 enables the reporting of LOF alarms on the section alarm SALM[2] output pin. When LOF_EN_CH2 is set to logic one LOF alarms from the RRMP will set the SALM[2] pin to logic 1. The SALM[2] will remain high until an in frame condition persists for continuous period of 3 mSec. When LOF_EN_CH2 is set to logic 0 LOF alarms have no effect on the state of SALM[2].

LOS_RRMP_EN_CH2

The SALM[2] Loss Of Signal Status enable. The LOS_RRMP EN_CH2 enables the reporting of LOS alarms on the section alarm SALM[2] output pin. When LOS_RRMP_EN_CH2 is set to logic one LOS alarms from the RRMP will set the SALM[2] pin to logic 1. The SALM[2] will remain high until two consecutive error free framing patterns are found and during the intervening time (one frame) there is no violating period of consecutive all zeros pattern. When LOS_RRMP_EN_CH2 is set to logic 0 an LOS alarm will have no effect on the state of SALM[2].

LOS_RXLI_EN_CH2

The SALM[2] Loss Of Signal Status enable. The LOS_RXLI_EN_CH2 enables the reporting of RXLI LOS alarms on the section alarm SALM[2] output pin. When LOS_RXLI _EN_CH2 is set to logic one LOS alarms from the RXLI will set the SALM[2] pin to logic 1. When LOS_RXLI_EN_CH2 is set to logic 0 an RXLI LOS alarm will have no effect on the state of SALM[2]. The LOS_RXLI is equivalent to the LOS_I interrupt bit in the RXLI Interrupt Status register 1500H.

OOF_EN_CH2

The SALM[2] Out Of Frame Status enable. The OOF_EN_CH2 enables the reporting of OOF alarms on the section alarm SALM[2] output pin. When OOF_EN_CH2 is set to logic one OOF alarms from the RRMP will set the SALM[2] pin to logic 1. The SALM[2] will remain high until the next error free framing patterns are found. When OOF_EN_CH2 is set to logic 0 OOF alarms have no effect on the state of SALM[2].

SD_EN_CH3

The SALM[3] Signal Degrade enable. The SD_EN_CH3 enables the reporting of Signal Degrade alarms on the section alarm SALM[3] output pin. When SD_EN_CH3 is set to logic one signal degrade alarms from the SBER will set the SALM[3] pin to logic 1. The SALM[3] will remain high until the value set in the SBER SD BERM clearing threshold register is reached. When SD_EN_CH3 is set to logic 0 SD alarms have no effect on the state of SALM[3].

SF_EN_CH3

The SALM[3] Signal Fail enable. The SF_EN_CH3 enables the reporting of Signal Fail alarms on the section alarm SALM[3] output pin. When SF_EN_CH3 is set to logic one signal fail alarms from the SBER will set the SALM[3] pin to logic 1. The SALM[3] will remain high until the value set in the SBER SF BERM Clearing Threshold Register is reached. When SF_EN_CH3 is set to logic 0 signal fail alarms have no effect on the state of SALM[3].

LRDI_EN_CH3

The SALM[3] Line Remote Defect Indication enable. The LRDI_EN_CH3 enables the reporting of LRDI alarms on the section alarm SALM[3] output pin. When LRDI_EN_CH3 is set to logic one LRDI alarms from the RRMP will set the SALM[3] pin to logic 1. The SALM[3] will remain high until the LRDI pattern is removed from the K2 byte for three or five consecutive frames. When LRDI_EN_CH3 is set to logic 0 Line Remote Defect alarms have no effect on the state of SALM[3].

LAIS_EN_CH3

The SALM[3] Line Alarm Indication Status enable. The LAIS_EN_CH3 enables the reporting of LAIS alarms on the section alarm SALM[3] output pin. When LAIS_EN_CH3 is set to logic one LAIS alarms from the RRMP will set the SALM[3] pin to logic 1. The SALM[3] will remain high until the LAIS pattern is removed from the K2 byte for three or five consecutive frames. When LAIS_EN_CH3 is set to logic 0 LAIS alarms have no effect on the state of SALM[3].

LOF_EN_CH3

The SALM[3] Loss Of Frame Status enable. The LOF_EN_CH3 enables the reporting of LOF alarms on the section alarm SALM[3] output pin. When LOF_EN_CH3 is set to logic one LOF alarms from the RRMP will set the SALM[3] pin to logic 1. The SALM[3] will remain high until an in frame condition persists for continuous period of 3 mSec. When LOF_EN_CH3 is set to logic 0 LOF alarms have no effect on the state of SALM[3].

LOS_RRMP_EN_CH3

The SALM[3] Loss Of Signal Status enable. The LOS_RRMP EN_CH3 enables the reporting of LOS alarms on the section alarm SALM[3] output pin. When LOS_RRMP_EN_CH3 is set to logic one LOS alarms from the RRMP will set the SALM[3] pin to logic 1. The SALM[3] will remain high until two consecutive error free framing patterns are found and during the intervening time (one frame) there is no violating period of consecutive all zeros pattern. When LOS_RRMP_EN_CH3 is set to logic 0 an RRMP LOS alarm will have no effect on the state of SALM[3].

LOS_RXLI_EN_CH3

The SALM[3] Loss Of Signal Status enable. The LOS_RXLI_EN_CH3 enables the reporting of RXLI LOS alarms on the section alarm SALM[3] output pin. When LOS_RXLI _EN_CH3 is set to logic one LOS alarms from the RXLI will set the SALM[3] pin to logic 1. When LOS_RXLI_EN_CH3 is set to logic 0 an RXLI LOS alarm will have no effect on the state of SALM[3]. The LOS_RXLI is equivalent to the LOS_I interrupt bit in the RXLI Interrupt Status register 1700H.

OOF_EN_CH3

The SALM[3] Out Of Frame Status enable. The OOF_EN_CH3 enables the reporting of OOF alarms on the section alarm SALM[3] output pin. When OOF_EN_CH3 is set to logic one OOF alarms from the RRMP will set the SALM[3] pin to logic 1. The SALM[3] will remain high until the next error free framing patterns are found. When OOF_EN_CH3 is set to logic 0 OOF alarms have no effect on the state of SALM[3].

Register 0012H: Channel 1 and 0 SALM ENABLES

Bit	Type	Function	Default
Bit 15	R/W	OOF_EN_CH1	0
Bit 14	R/W	LOS_RRMP_EN_CH1	0
Bit 13	R/W	LOS_RXLI_EN_CH1	1
Bit 12	R/W	LOF_EN_CH1	0
Bit 11	R/W	LAIS_EN_CH1	0
Bit 10	R/W	LRDI_EN_CH1	0
Bit 9	R/W	SF_EN_CH1	0
Bit 8	R/W	SD_EN_CH1	0
Bit 7	R/W	OOF_EN_CH0	0
Bit 6	R/W	LOS_RRMP_EN_CH0	0
Bit 5	R/W	LOS_RXLI_EN_CH0	1
Bit 4	R/W	LOF_EN_CH0	0
Bit 3	R/W	LAIS_EN_CH0	0
Bit 2	R/W	LRDI_EN_CH0	0
Bit 1	R/W	SF_EN_CH0	0
Bit 0	R/W	SD_EN_CH0	0

SD_EN_CH0

The SALM[0] Signal Degrade enable. The SD_EN_CH0 enables the reporting of Signal Degrade alarms on the section alarm SALM[0] output pin. When SD_EN_CH0 is set to logic one signal degrade alarms from the SBER will set the SALM[0] pin to logic 1. The SALM[0] will remain high until the value set in the SBER SD BERM clearing threshold register is reached. When SD_EN_CH0 is set to logic 0 SD alarms have no effect on the state of SALM[0].

SF_EN_CH0

The SALM[0] Signal Fail enable. The SF_EN_CH0 enables the reporting of Signal Fail alarms on the section alarm SALM[0] output pin. When SF_EN_CH0 is set to logic one signal fail alarms from the SBER will set the SALM[0] pin to logic 1. The SALM[0] will remain high until the value set in the SBER SF BERM Clearing Threshold Register is reached. When SF_EN_CH0 is set to logic 0 signal fail alarms have no effect on the state of SALM[0].

LRDI_EN_CH0

The SALM[0] Line Remote Defect Indication enable. The LRDI_EN_CH0 enables the reporting of LRDI alarms on the section alarm SALM[0] output pin. When LRDI_EN_CH0 is set to logic one LRDI alarms from the RRMP will set the SALM[0] pin to logic 1. The SALM[0] will remain high until the LRDI pattern is removed from the K2 byte for three or five consecutive frames. When LRDI_EN_CH0 is set to logic 0 Line Remote Defect alarms have no effect on the state of SALM[0].

LAIS_EN_CH0

The SALM[0] Line Alarm Indication Status enable. The LAIS_EN_CH0 enables the reporting of LAIS alarms on the section alarm SALM[0] output pin. When LAIS_EN_CH0 is set to logic one LAIS alarms from the RRMP will set the SALM[0] pin to logic 1. The SALM[0] will remain high until the LAIS pattern is removed from the K2 byte for three or five consecutive frames. When LAIS_EN_CH0 is set to logic 0 LAIS alarms have no effect on the state of SALM[0].

LOF_EN_CH0

The SALM[0] Loss Of Frame Status enable. The LOF_EN_CH0 enables the reporting of LOF alarms on the section alarm SALM[0] output pin. When LOF_EN_CH0 is set to logic one LOF alarms from the RRMP will set the SALM[0] pin to logic 1. The SALM[0] will remain high until an in frame condition persists for continuous period of 3 mSec. When LOF_EN_CH0 is set to logic 0 LOF alarms have no effect on the state of SALM[0].

LOS_RRMP_EN_CH0

The SALM[0] Loss Of Signal Status enable. The LOS_RRMP EN_CH0 enables the reporting of LOS alarms on the section alarm SALM[0] output pin. When LOS_RRMP_EN_CH0 is set to logic one LOS alarms from the RRMP will set the SALM[0] pin to logic 1. The SALM[0] will remain high until two consecutive error free framing patterns are found and during the intervening time (one frame) there is no violating period of consecutive all zeros pattern. When LOS_RRMP_EN_CH0 is set to logic 0 an RRMP LOS alarm will have no effect on the state of SALM[0].

LOS_RXLI_EN_CH0

The SALM[0] Loss Of Signal Status enable. The LOS_RXLI_EN_CH0 enables the reporting of RXLI LOS alarms on the section alarm SALM[0] output pin. When LOS_RXLI _EN_CH0 is set to logic one LOS alarms from the RXLI will set the SALM[0] pin to logic 1. When LOS_RXLI_EN_CH0 is set to logic 0 RXLI LOS alarm will have no effect on the state of SALM[0]. The LOS_RXLI is equivalent to the LOS_I interrupt bit in the RXLI Interrupt Status register 1100H.

OOF_EN_CH0

The SALM[0] Out Of Frame Status enable. The OOF_EN_CH0 enables the reporting of OOF alarms on the section alarm SALM[0] output pin. When OOF_EN_CH0 is set to logic one OOF alarms from the RRMP will set the SALM[0] pin to logic 1. The SALM[0] will remain high until the next error free framing patterns are found. When OOF_EN_CH0 is set to logic 0 OOF alarms have no effect on the state of SALM[0].

SD_EN_CH1

The SALM[1] Signal Degrade enable. The SD_EN_CH1 enables the reporting of Signal Degrade alarms on the section alarm SALM[1] output pin. When SD_EN_CH1 is set to logic one signal degrade alarms from the SBER will set the SALM[1] pin to logic 1. The SALM[1] will remain high until the value set in the SBER SD BERM clearing threshold register is reached. When SD_EN_CH1 is set to logic 0 SD alarms have no effect on the state of SALM[1].

SF_EN_CH1

The SALM[1] Signal Fail enable. The SF_EN_CH1 enables the reporting of Signal Fail alarms on the section alarm SALM[1] output pin. When SF_EN_CH1 is set to logic one signal fail alarms from the SBER will set the SALM[1] pin to logic 1. The SALM[1] will remain high until the value set in the SBER SF BERM Clearing Threshold Register is reached. When SF_EN_CH1 is set to logic 0 signal fail alarms have no effect on the state of SALM[1].

LRDI_EN_CH1

The SALM[1] Line Remote Defect Indication enable. The LRDI_EN_CH1 enables the reporting of LRDI alarms on the section alarm SALM[1] output pin. When LRDI_EN_CH1 is set to logic one LRDI alarms from the RRMP will set the SALM[1] pin to logic 1. The SALM[1] will remain high until the LRDI pattern is removed from the K2 byte for three or five consecutive frames. When LRDI_EN_CH1 is set to logic 0 Line Remote Defect alarms have no effect on the state of SALM[1].

LAIS_EN_CH1

The SALM[1] Line Alarm Indication Status enable. The LAIS_EN_CH1 enables the reporting of LAIS alarms on the section alarm SALM[1] output pin. When LAIS_EN_CH1 is set to logic one LAIS alarms from the RRMP will set the SALM[1] pin to logic 1. The SALM[1] will remain high until the LAIS pattern is removed from the K2 byte for three or five consecutive frames. When LAIS_EN_CH1 is set to logic 0 LAIS alarms have no effect on the state of SALM[1].

LOF_EN_CH1

The SALM[1] Loss Of Frame Status enable. The LOF_EN_CH1 enables the reporting of LOF alarms on the section alarm SALM[1] output pin. When LOF_EN_CH1 is set to logic one LOF alarms from the RRMP will set the SALM[1] pin to logic 1. The SALM[1] will remain high until an in frame condition persists for continuous period of 3 mSec. When LOF_EN_CH1 is set to logic 0 LOF alarms have no effect on the state of SALM[1].

LOS_RRMP_EN_CH1

The SALM[1] Loss Of Signal Status enable. The LOS_RRMP EN_CH1 enables the reporting of LOS alarms on the section alarm SALM[1] output pin. When LOS_RRMP_EN_CH1 is set to logic one LOS alarms from the RRMP will set the SALM[1] pin to logic 1. The SALM[1] will remain high until two consecutive error free framing patterns are found and during the intervening time (one frame) there is no violating period of consecutive all zeros pattern. When LOS_RRMP_EN_CH1 is set to logic 0 an RRMP LOS alarm will have no effect on the state of SALM[1].

LOS_RXLI_EN_CH1

The SALM[1] Loss Of Signal Status enable. The LOS_RXLI_EN_CH1 enables the reporting of RXLI LOS alarms on the section alarm SALM[1] output pin. When LOS_RXLI _EN_CH1 is set to logic one LOS alarms from the RXLI will set the SALM[1] pin to logic 1. When LOS_RXLI_EN_CH1 is set to logic 0 an RXLI LOS alarm will have no effect on the state of SALM[1]. The LOS_RXLI is equivalent to the LOS_I interrupt bit in the RXLI Interrupt Status register 1300H.

OOF_EN_CH1

The SALM[1] Out Of Frame Status enable. The OOF_EN_CH1 enables the reporting of OOF alarms on the section alarm SALM[1] output pin. When OOF_EN_CH1 is set to logic one OOF alarms from the RRMP will set the SALM[1] pin to logic 1. The SALM[1] will remain high until the next error free framing patterns are found. When OOF_EN_CH1 is set to logic 0 OOF alarms have no effect on the state of SALM[1].

Register 0013H: TXENB Control

Bit	Type	Function	Default
Bit 15	R/W	LCRUTO_EN_CH3	0
Bit 14	R/W	LCRUTO_EN_CH2	0
Bit 13	R/W	LCRUTO_EN_CH1	0
Bit 12	R/W	LCRUTO_EN_CH0	0
Bit 11	R/W	ANALOG_QSFI-4_ENB	0
Bit 10	R/W	TXENB_CH3	0
Bit 9	R/W	TXENB_CH2	0
Bit 8	R/W	TXENB_CH1	0
Bit 7	R/W	TXENB_CH0	0
Bit 6	R	Unused	X
Bit 5	R	Unused	X
Bit 4	R	Unused	X
Bit 3	R/W	SYNC_ERR_EN_CH3	1
Bit 2	R/W	SYNC_ERR_EN_CH2	1
Bit 1	R/W	SYNC_ERR_EN_CH1	1
Bit 0	R/W	SYNC_ERR_EN_CH0	1

SYNC_ERR_EN_CH[3:0]

QSFIM SYNC_ERR enable. The SYNC_ERR_EN_CH[3:0] controls the operation of the SYNC_ERR[3:0] output pin. When SYNC_ERR_EN_CH[3:0] is set to logic one the SYNC_ERR[3:0] output pins are enabled and indicate when active that the CRU is locked to data stream from the optical module. When SYNC_ERR_EN_CH[3:0] is set to logic zero the SYNC_ERR[3:0] output pin is forced to logic zero. The polarity of the SYNC_ERR[3:0] pins is controlled by the SYNC_ERR_INV bit 14 Register 000BH.

TXENB_CH[3:0]

Transmit Module Enable. The TXENB_CH[3:0] bit controls the state of the TXENB[3:0] output pin. When TXENB_CH[3:0] is set to logic 0 the TXENB[3:0] is set to logic 0. When TXENB_CH[3:0] is set to logic 1 the TXENB[3:0] is set to logic 1.

ANALOG_QSFI-4_ENB

QSFI-4 Interface Analog Circuitry Enable. The ANALOG_QSFI-4_ENB controls the status of the QSFI-4 analog circuitry. When ANALOG_QSFI-4_ENB is set to logic 0, the interface circuit is enable and operates normally. When ANALOG_QSFI-4_ENB is set to logic 1 the interface circuit is disabled and is not functional. Disabling the Analog Circuitry reduces power consumption of the device when the QSFI-4 interface is not required.

LCRUTO_EN_CH[3:0]

2.488 GHz Line Side Interface Clock enable. When the LCRUTO_EN_CH[n] is set to logic '1' the LCRUTO[n] clock output pins for channel n are enabled; a 155Mhz recovered clock will be sourced from LCRUTO pins. When set to logic '0' the LCRUTO[n] clock output pins are forced to logic zero to conserve power.

Register 0014H: Device Number

Bit	Type	Function	Default
Bit 15	R	CHIPID[15]	0
Bit 14	R	CHIPID[14]	1
Bit 13	R	CHIPID[13]	0
Bit 12	R	CHIPID[12]	1
Bit 11	R	CHIPID[11]	0
Bit 10	R	CHIPID[10]	0
Bit 9	R	CHIPID[9]	1
Bit 8	R	CHIPID[8]	1
Bit 7	R	CHIPID[7]	1
Bit 6	R	CHIPID[6]	0
Bit 5	R	CHIPID[5]	0
Bit 4	R	CHIPID[4]	1
Bit 3	R	CHIPID[3]	0
Bit 2	R	CHIPID[2]	1
Bit 1	R	CHIPID[1]	0
Bit 0	R	CHIPID[0]	1

CHIPID[15:0]

The Chip Identification Code provides a software test of the device identity. The CHIPID[15:0] is set to 5395H to identify the device as the PM5395 CRSU 4x2488.

11.1 Channel Register Map

The **CRSU 4x2488** contains four channels in total. The order and number of registers for each channel is the same. The starting location for each channel is offset by 200H. For example if the programmer wanted to access the RSOP Control register in channel two, they would add 2 x 200H = 400H to the value of the channel zero register address. In this case 1030H + 400H = 1430H. Table 9 lists the starting addresses for the Receive and Transmit slices for each channel.

Table 9 CRSU 4x2488 Channel Register Map

Channel	Direction	Starting Address
0	Tx	1000H
0	Rx	1100H
1	Tx	1200H
1	Rx	1300H
2	Tx	1400H
2	Rx	1500H
3	Tx	1600H
3	Rx	1700H

The following section provides the register description for all registers in Channel 0 of the **CRSU 4x2488**. Using the above formula, the address of any other register can be obtained. The register description for channel 0 applies to all other channels.

Channel 0 Register Map:

Register 1000H: QSFIM_2488 Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	RX_ESTORE_ERR_I	X
Bit 1	R	Reserved	X
Bit 0	R	TX_ESTORE_ERR_I	X

TX_ESTORE_ERR_I

The Transmit Elastic Store Error bit provides a status indication of an underflow or overflow condition in the QSFI-4 Transmitter data elastic store. When TX_ESTORE_ERR_I is set to '1' the data in the transmit elastic store has been corrupted and invalid data has been read from the FIFO. If QSFIM_2488 WCIMODE pin is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0 than a read of this register automatically clears the bit.

RX_ESTORE_ERR_I

The Receive Elastic Store Error bit provides a status indication of an underflow or overflow condition in the QSFI-4 Receive data elastic store. When RX_ESTORE_ERR_I is set to '1' the data in the receive elastic store has been corrupted and invalid data has been read from the FIFO. If QSFIM_2488 WCIMODE pin is set to logic 1, only over-writing with a '1' clears this bit. If WCIMODE is set to logic 0 than a read of this register automatically clears the bit.

Register 1001H: QSFIM_2488 Control

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	1
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	—	Unused	X
Bit 10	R/W	RX_ESTORE_RST	0
Bit 9	R/W	RX_ ESTORE_ERR_EN	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	PHASE_EN	1
Bit 5	R/W	TX_ESTORE_RST	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	TX_ESTORE_ERR_EN	0

TX_ESTORE_ERR_EN

The Transmit Elastic Store Error Enable bit connects the TX_ESTORE_ERR_I status bit to the QSFIM_INT_CH0 bit 4 Register 000AH. When TX_ESTORE_ERR_EN is set to logic one, the QSFIM_INT_CH0 bit is set to logic one upon assertion of the TX_ESTORE_ERR_I register bit. When TX_ESTORE_ERR_EN is set low, a change in the TX_ESTORE_ERR_I status does not generate a change in the QSFIM_INT_CH0 bit.

TX_ESTORE_RST

The Elastic Store Reset bit is used to reset the transmit elastic store. When this bit is set to logic 1, the transmit elastic store read and write pointers are reset. When set to low, there is no effect to the elastic store. This bit is not self-clearing and therefore a logic 0 must be written to clear the reset.

PHASE_EN

The Phase Enable bit is used to enable the PHASE_INIT[0] and PHASE_ERR[0] functions. When PHASE_EN is set to logic one the PHASE_INIT[0] input pin will force the Transmit Elastic store to the reset state and PHASE_ERR[0] will follow the state of the TX_ESTORE_ERR bit. When PHASE_EN is set to logic 0 PHASE_INIT[0] will have no effect on the Transmit Elastic Store and PHASE_ERR will be forced to logic one.

RX_ESTORE_ERR_EN

The Receive Elastic Store Error Enable bit connects the RX_ESTORE_ERR_I status bit to the QSFIM_INT_CH1 bit 4 Register 000AH. When RX_ESTORE_ERR_EN is set to logic one, the QSFIM_INT_CH1 bit is set to logic one upon assertion of the RX_ESTORE_ERR_I register bit. When RX_ESTORE_ERR_EN is set low, a change in the RX_ESTORE_ERR_I status does not generate a change in the QSFIM_INT_CH1 bit.

RX_ESTORE_RST

The Receive Elastic Store Reset bit is used to reset the receive elastic store. When this bit is set to high, the receive elastic store read and write pointers are reset. When set to low, there is no effect to the elastic store. This bit is not self-clearing and therefore a logic 0 must be written to clear the reset.

Register 1002H: QSFIM_2488 Reserved

Bit	Type	Function	Default
Bit 15	R/W	Reserved	1
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	1
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

Register 1030H: RSOP Control

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	W	FOOF	X
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	OOF_E	0

OOF_E

The Out of Frame Enable (OOF_E) bit connects the OOF_I status bit to the RSOP_INT_0 bit in the Master Interrupt Status TX CH0 Register 0006H. When OOF_E is set to logic one, the RSOP_INT_0 bit is set to logic one upon assertion of the OOF_I register bit. When OOF_E is set logic 0, a change in the OOF_I status does not generate a change in the RSOP_INT_0 bit.

FOOF

When a logic 1 is written to the Force Out-of-Frame (FOOF) bit location, the RSOP is forced out-of-frame at the next frame boundary, regardless of the framing byte values. The out-of-frame event initiates reframing in an upstream framing pattern detector. The FOOF bit is a write only bit; a Control register read may yield a logic 1 or a logic 0 in this bit position. A logic '0' must be written in the FOOF bit location to remove the force out of frame condition.

Register 1031H: RSOP Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	OOF_I	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	OOF_V	X

OOF_V

The Out of Frame Status bit (OOF_V) reflects the current state of the framer. A logic 1 indicates the Framer can not located the A1, A2 framing pattern in the incoming Transmit data. When this bit is set to logic 0 the framer is locked the A1, A2 framing pattern.

OOF_I

The Out of Frame Interrupt (OOF_I) bit indicates that an event has occurred on the OOF_V status bit. This bit is set high when a change of state transition has occurred on OOF_V status bit. If the corresponding interrupt enable bit is set in the RSOP Control Register then the state of the RSOP_INT_0 bit in the Master Interrupt Status TX CH0 Register 0006H will change to logic 1. The OOF_I bit is cleared to logic 0 when the Interrupt Status register is read. **Note: This interrupt can not be configured for clear-on-write operation. This interrupt is always cleared when the bit is read regardless of the state of the WCIMODE bit in register 000BH.**

Register 1040H: TIFE Configuration

Bit	Type	Function	Default
Bit 15	R	Unused	X
Bit 14	R	Unused	X
Bit 13	R	Unused	X
Bit 12	R	Unused	X
Bit 11	R	Unused	X
Bit 10	R	Unused	X
Bit 9	R	Unused	X
Bit 8	R	Unused	X
Bit 7	R	Unused	X
Bit 6	R	Unused	X
Bit 5	R	Unused	X
Bit 4	R	Unused	X
Bit 3	R	Unused	X
Bit 2	R/W	Reserved	1
Bit 1	R/W	STATE[1]	1
Bit 0	R/W	STATE[0]	0

STATE [1:0]

The Transmit FEC Encoder State control bits control the operational state of the Transmit FEC encoder. A Write to this register will change the operating state on the next frame boundary. Reads of this register will return the pervious value written. The description of each of the operational states are shown below.

STATE [1:0]	TIFE State	State Description
00	N/A	Reserved
01	1	FEC encoding enabled. B2 bytes are corrected for FEC and FSI insertion in past frames.
10	2	FEC encoding disable. The pipeline delay across the Transmit FEC encoder is identical to state 1. B2 bytes are corrected for FEC and FSI insertion in past frames. FSI byte is overwritten but the FEC bytes are not overwritten. This is the reset state.
11	3	FEC encoding disabled, pipeline delay across TIFE is minimized to two TCLK clock cycles. The FSI byte is by default written 0h00 by TIFE. Optionally this state can implement a transparent mode for TIFE where the output data are simply registered versions of the input data if FSI_MASK_EN (Register 1041H bit 14) is deasserted.

Register 1041H: TIFE Control

Bit	Type	Function	Default
Bit 15	R/W	HS_EN	1
Bit 14	R/W	FSI_MASK_EN	1
Bit 13	R	Unused	X
Bit 12	R	Unused	X
Bit 11	R	Unused	X
Bit 10	R	Unused	X
Bit 9	R	Unused	X
Bit 8	R	Unused	X
Bit 7	R	Unused	X
Bit 6	R	Unused	X
Bit 5	R	Unused	X
Bit 4	R/W	INJECT	0
Bit 3	R/W	INSERT_ROW[3]	0
Bit 2	R/W	INSERT_ROW[2]	0
Bit 1	R/W	INSERT_ROW[1]	0
Bit 0	R/W	INSERT_ROW[0]	0

INSERT_ROW[3:0]

The Insertion Row number bits define the row number where the inverted bytes will be inserted. The INSERT_ROW[3:0] bits are written with the binary coded value of the row where the byte inversion is to be done. The minimum row number is 0H and the maximum row number is 8H. This field must be set before the INJECT bit is enabled.

INJECT

The Inject Error into frame bit. Setting this bit to logic ‘1’ enables the inversion of bytes defined by the PARAM_B_n[1:0], PARAM_A_n[10:0], INSERT_EN_n, and INSERT_ROW[3:0] register bits. This bit clears to logic ‘0’ prior to the inverted bytes being inserted in a row. Software can poll the INJECT bit to determine when to insert unique errors in each row of the frame. See the operations section for a complete description of the FEC Encoder Error insertion capabilities.

FSI_MASK_EN

The FSI mask enable bit. This bit enables over-writing of the FSI byte with 00H while Transmit FEC encoder operates in State 3. If this bit is set to logic ‘0’, the FEC encoder does not modify any bytes while in state 3. Setting this bit to logic '0' forces the FEC encoder to pass frames through unchanged.

HS_EN

The handshake enable bit. This bit enables the seven-frame FSI handshaking defined in T1X1.5/99-218R2 In band FEC for SONET specification (See the list of references in Section 2 of this document). When HS_EN is set to logic '1', the FEC encoder waits seven frames before starting or stopping decoding; but FSI is changed to "01" or "00" for these seven frames. When the HS_EN is set to logic '0', the FEC encoder starts or stops encoding on the very next frame and FSI is set "01" or "00" appropriately.

Register 1042H: TIFE Error Insertion Byte 0

Bit	Type	Function	Default
Bit 15	R/W	INSERT_EN_0	0
Bit 14	R	Unused	X
Bit 13	R	Unused	X
Bit 12	R/W	PARAM_A_0[10]	0
Bit 11	R/W	PARAM_A_0[9]	0
Bit 10	R/W	PARAM_A_0[8]	0
Bit 9	R/W	PARAM_A_0[7]	0
Bit 8	R/W	PARAM_A_0[6]	0
Bit 7	R/W	PARAM_A_0[5]	0
Bit 6	R/W	PARAM_A_0[4]	0
Bit 5	R/W	PARAM_A_0[3]	0
Bit 4	R/W	PARAM_A_0[2]	0
Bit 3	R/W	PARAM_A_0[1]	0
Bit 2	R/W	PARAM_A_0[0]	0
Bit 1	R/W	PARAM_B_0[1]	0
Bit 0	R/W	PARAM_B_0[0]	0

PARAM_B_0[1:0]

The byte 0 error insertion Parameter B. The PARAM_B_0[1:0] field along with the PARAM_A_0[10:0] field defines which byte of the row specified by INSERT_ROW[3:0] field will be modified. The maximum value is 3 and the minimum value is 0. The byte selected by PARAM_B_0[1:0] will only be inverted if INSERT_EN_0 is set to logic '1'. See the Operations section for a complete description of the FEC Encoder Error insertion capabilities.

PARAM_A_0[10:0]

The byte 0 error insertion Parameter A. The PARAM_A_0[10:0] field along with the PARAM_B_0[1:0] field defines which byte of the row specified by INSERT_ROW[3:0] field will be modified. The maximum value is 1079 and the minimum value is 0. Values greater than 1079 can result in unexpected behaviour. The byte selected by PARAM_A_0[10:0] will only be inverted if INSERT_EN_0 is set to logic '1'. See the Operations section for a complete description of the FEC Encoder Error insertion capabilities.

INSERT_EN_0

The byte 0 Insertion enable bit. Setting this bit ‘1’ enables inverting the byte defined by the PARAM_B_0[1:0] and PARAM_A_0[10:0] fields. When this bit is set to logic '0' the PARAM_B_0[1:0] and PARAM_A_0[10:0] fields are ignored and no byte modification occurs for the location specified.

Register 1043H: TIFE Error Insertion Byte 1

Bit	Type	Function	Default
Bit 15	R/W	INSERT_EN_1	0
Bit 14	R	Unused	X
Bit 13	R	Unused	X
Bit 12	R/W	PARAM_A_1[10]	0
Bit 11	R/W	PARAM_A_1[9]	0
Bit 10	R/W	PARAM_A_1[8]	0
Bit 9	R/W	PARAM_A_1[7]	0
Bit 8	R/W	PARAM_A_1[6]	0
Bit 7	R/W	PARAM_A_1[5]	0
Bit 6	R/W	PARAM_A_1[4]	0
Bit 5	R/W	PARAM_A_1[3]	0
Bit 4	R/W	PARAM_A_1[2]	0
Bit 3	R/W	PARAM_A_1[1]	0
Bit 2	R/W	PARAM_A_1[0]	0
Bit 1	R/W	PARAM_B_1[1]	0
Bit 0	R/W	PARAM_B_1[0]	0

PARAM_B_1[1:0]

The byte 1 error insertion Parameter B. The PARAM_B_1[1:0] field along with the PARAM_A_1[10:0] field defines which byte of the row specified by INSERT_ROW[3:0] field will be modified. The maximum value is 3 and the minimum value is 0. The byte selected by PARAM_B_1[1:0] will only be inverted if INSERT_EN_1 is set to logic ‘1’. See the Operations section for a complete description of the FEC Encoder Error insertion capabilities.

PARAM_A_1[10:0]

The byte 1 error insertion Parameter A. The PARAM_A_1[10:0] field along with the PARAM_B_1[1:0] field defines which byte of the row specified by INSERT_ROW[3:0] field will be modified. The maximum value is 1079 and the minimum value is 0. Values greater than 1079 can result in unexpected behaviour. The byte selected by PARAM_A_1[10:0] will only be inverted if INSERT_EN_1 is set to logic ‘1’. See the Operations section for a complete description of the FEC Encoder Error insertion capabilities.

INSERT_EN_1

The byte 1 Insertion enable bit. Setting this bit ‘1’ enables inverting the byte defined by the PARAM_B_1[1:0] and PARAM_A_1[10:0] fields. When this bit is set to logic '0' the PARAM_B_1[1:0] and PARAM_A_1[10:0] fields are ignored and no byte modification occurs for the location specified.

Register 1044H: TIFE Error Insertion Byte 2

Bit	Type	Function	Default
Bit 15	R/W	INSERT_EN_2	0
Bit 14	R	Unused	X
Bit 13	R	Unused	X
Bit 12	R/W	PARAM_A_2[10]	0
Bit 11	R/W	PARAM_A_2[9]	0
Bit 10	R/W	PARAM_A_2[8]	0
Bit 9	R/W	PARAM_A_2[7]	0
Bit 8	R/W	PARAM_A_2[6]	0
Bit 7	R/W	PARAM_A_2[5]	0
Bit 6	R/W	PARAM_A_2[4]	0
Bit 5	R/W	PARAM_A_2[3]	0
Bit 4	R/W	PARAM_A_2[2]	0
Bit 3	R/W	PARAM_A_2[1]	0
Bit 2	R/W	PARAM_A_2[0]	0
Bit 1	R/W	PARAM_B_2[1]	0
Bit 0	R/W	PARAM_B_2[0]	0

PARAM_B_2[1:0]

The byte 2 error insertion Parameter B. The PARAM_B_2[1:0] field along with the PARAM_A_2[10:0] field defines which byte of the row specified by INSERT_ROW[3:0] field will be modified. The maximum value is 3 and the minimum value is 0. The byte selected by PARAM_B_2[1:0] will only be inverted if INSERT_EN_2 is set to logic ‘1’. See the Operations section for a complete description of the FEC Encoder Error insertion capabilities.

PARAM_A_2[10:0]

The byte 2 error insertion Parameter A. The PARAM_A_2[10:0] field along with the PARAM_B_2[1:0] field defines which byte of the row specified by INSERT_ROW[3:0] field will be modified. The maximum value is 1079 and the minimum value is 0. Values greater than 1079 can result in unexpected behaviour. The byte selected by PARAM_A_2[10:0] will only be inverted if INSERT_EN_2 is set to logic ‘1’. See the Operations section for a complete description of the FEC Encoder Error insertion capabilities.

INSERT_EN_2

The byte 2 Insertion enable bit. Setting this bit ‘1’ enables inverting the byte defined by the PARAM_B_2[1:0] and PARAM_A_2[10:0] fields. When this bit is set to logic '0' the PARAM_B_2[1:0] and PARAM_A_2[10:0] fields are ignored and no byte modification occurs for the location specified.

Register 1045H: TIFE Error Insertion Byte 3

Bit	Type	Function	Default
Bit 15	R/W	INSERT_EN_3	0
Bit 14	R	Unused	X
Bit 13	R	Unused	X
Bit 12	R/W	PARAM_A_3[10]	0
Bit 11	R/W	PARAM_A_3[9]	0
Bit 10	R/W	PARAM_A_3[8]	0
Bit 9	R/W	PARAM_A_3[7]	0
Bit 8	R/W	PARAM_A_3[6]	0
Bit 7	R/W	PARAM_A_3[5]	0
Bit 6	R/W	PARAM_A_3[4]	0
Bit 5	R/W	PARAM_A_3[3]	0
Bit 4	R/W	PARAM_A_3[2]	0
Bit 3	R/W	PARAM_A_3[1]	0
Bit 2	R/W	PARAM_A_3[0]	0
Bit 1	R/W	PARAM_B_3[1]	0
Bit 0	R/W	PARAM_B_3[0]	0

PARAM_B_3[1:0]

The byte 3 error insertion Parameter B. The PARAM_B_3[1:0] field along with the PARAM_A_3[10:0] field defines which byte of the row specified by INSERT_ROW[3:0] field will be modified. The maximum value is 3 and the minimum value is 0. The byte selected by PARAM_B_3[1:0] will only be inverted if INSERT_EN_3 is set to logic '1'. See the Operations section for a complete description of the FEC Encoder Error insertion capabilities.

PARAM_A_3[10:0]

The byte 3 error insertion Parameter A. The PARAM_A_3[10:0] field along with the PARAM_B_3[1:0] field defines which byte of the row specified by INSERT_ROW[3:0] field will be modified. The maximum value is 1079 and the minimum value is 0. Values greater than 1079 can result in unexpected behaviour. The byte selected by PARAM_A_3[10:0] will only be inverted if INSERT_EN_3 is set to logic '1'. See the Operations section for a complete description of the FEC Encoder Error insertion capabilities.

INSERT_EN_3

The byte 3 Insertion enable bit. Setting this bit ‘1’ enables inverting the byte defined by the PARAM_B_3[1:0] and PARAM_A_3[10:0] fields. When this bit is set to logic '0' the PARAM_B_3[1:0] and PARAM_A_3[10:0] fields are ignored and no byte modification occurs for the location specified.

Register 1050H: TRSP Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	Reserved	0
Bit 10	R/W	LREIEN *(see attached note)*	1
Bit 9	R/W	APSEN *(see attached note)*	1
Bit 8	R/W	Reserved	1
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	1
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	J0Z0INCEN	0
Bit 1	R/W	Z0DEF	0
Bit 0	R/W	A1A2EN	1

A1A2EN

The A1A2 framing enable (A1A2EN) bit controls the insertion of the framing bytes in the data stream. When A1A2EN is set to logic 1, F6h and 28h are inserted in the A1 and A2 bytes. When A1A2EN is set to logic 0, the framing bytes are not inserted. The A1ERR register bit takes precedence over the A1A2EN bit.

For normal operation, the A1A2EN bits in Registers 1060H, 1070H and 1080H must be set to the same value.

Z0DEF

The Z0 definition (Z0DEF) bit defines the Z0 growth bytes. When Z0DEF is set to logic 1, the Z0 bytes are defined according to ITU. The Z0 bytes are located in STS-1/STM-0 #2 to #16. When Z0DEF is set to logic 0, the Z0 bytes are defined according to BELLCORE. The Z0 bytes are located in STS-1/STM-0 #2 to #48.

For normal operation, the Z0DEF bits in registers 1060H, 1070H and 1080H must be set to the same value. **Note: If Z0DEF = 1, National bytes will be passed from the QSFI-4 to the Line transparently. To ensure downstream framers can lock to data, the upstream framer must ensure national bytes are not set to all zeros or all ones pattern.**

J0Z0INCEN

The J0 and Z0 increment enable (J0Z0INCEN) bit controls the insertion of an incremental pattern in the section trace and Z0 growth bytes. When J0ZOINCEN is set to logic 1, the corresponding STS-1/STM-0 path # is inserted in the J0 and Z0 bytes. When J0Z0INCEN is set to logic 0, no incremental pattern is inserted. The J0Z0INCEN register bit takes precedence over the J0REGEN register bit.

For normal operation, the J0Z0INCEN bits in the registers 1060H, 1070H and 1080H, must be set to the same value.

APSEN

The APS enable (APSEN) bit controls the insertion of automatic protection switching in the data stream. When APSEN is set to logic 1, the APS bytes from the RRMP are inserted in the K1/K2 bytes of STS-1/STM-0 #1. The APSEN bit takes precedence over the K1K2REGEN register bit. When APSEN is set to logic 0, the APS bytes from the RRMP are not inserted. **NOTE: The CRSU 4x2488 does not support this feature, therefore this bit must be set to logic 0 for correct operation. If this bit is not set to logic 0 then the FEC control bytes will not be correct for the pay load due to the insertion of the K1/K2 bytes after the FEC code bytes are calculated. Not setting this to logic 0 will also result in the over writing the K1/K2 bytes of the upstream framer.**

LREIEN

The line REI enable (LREIEN) bit controls the insertion of line remote error indication in the data stream. When LREIEN is set to logic 1, the line REI from the RRMP is inserted in the M1 byte of STS-1/STM-0 #3. When LREIEN is set to logic 0, the line REI from the RRMP is not inserted. **NOTE: The CRSU 4x2488 does not support this feature, therefore this bit must be set to logic 0 for correct operation. If this bit is not set to logic 0 then the FEC control bytes will not be correct for the pay load due to the insertion of the M1 byte after the FEC code bytes are calculated. Not setting this to logic 0 will also result in the over writing the M1 bytes of the upstream framer.**

Register 1051H: TRSP Register Insertion

Bit	Type	Function	Default
Bit 15	R/W	UNUSEDV	0
Bit 14	R/W	UNUSEDEN	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	—	Unused	X
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	D1D3REGEN	0
Bit 3	R/W	F1REGEN	0
Bit 2	R/W	E1REGEN	0
Bit 1	R/W	Z0REGEN (See attached note)	1
Bit 0	R/W	J0REGEN (See attached note)	1

J0REGEN

The J0 register enable (J0REGEN) bit controls the insertion of section trace in the data stream. When J0REGEN is set to logic 1, the section trace from the TRSP Transmit J0 and Z0 register is inserted in the J0 byte of STS-1/STM-0 #1. When J0REGEN is set to logic 0, the section trace from the TRSP Transmit J0 and Z0 register is not inserted. **NOTE: If the J0REGEN is enabled the CRSU 4x2488 will overwrite any data written to the J0 byte by any down stream device. Under normal operation this bit should be disabled.**

Z0REGEN

The Z0 register enable (Z0REGEN) bit controls the insertion of Z0 growth bytes in the data stream. When Z0REGEN is set to logic 1, the Z0 growth byte from the TRSP Transmit J0 and Z0 register is inserted in the Z0 bytes of STS-1,5,9 and 13. When Z0REGEN is set to logic 0, the Z0 growth byte from the TRSP Transmit J0 and Z0 register is not inserted. The Z0DEF bit in the TRSP Configuration register bit defines the Z0 bytes. **NOTE: If the Z0REGEN is enabled the CRSU 4x2488 will overwrite any data written to the Z0 byte by any down stream device. Under normal operation this bit should be disabled**

E1REGEN

The E1 register enable (E1REGEN) bit controls the insertion of section order wire in the data stream. When E1REGEN is set to logic 1, the section order wire from the TRSP Transmit E1 and F1 register is inserted in the E1 byte of STS-1/STM-0 #1 according to the priority of Figure 8. When E1REGEN is set to logic 0, the section order wire from the TRSP Transmit E1 and F1 register is not inserted.

F1REGEN

The F1 register enable (F1REGEN) bit controls the insertion of section user channel in the data stream. When F1REGEN is set to logic 1, the section user channel from the TRSP Transmit E1 and F1 register is inserted in the F1 byte of STS-1/STM-0 #1 according to the priority of Figure 8. When F1REGEN is set to logic 0, the section user channel from the TRSP Transmit E1 and F1 register is not inserted.

D1D3REGEN

The D1 to D3 register enable (D1D3REGEN) bit controls the insertion of section data communication channel in the data stream. When D1D3REGEN is set to logic 1, the section DCC from the TRSP Transmit D1D3 and D4D12 register is inserted in the D1 to D3 bytes of STS-1/STM-0 #1. When D1D3REGEN is set to logic 0, the section DCC from the TRSP Transmit D1D3 and D4D12 register is not inserted.

UNUSEDEN

The Unused enable (UNUSEDEN) bit controls the insertion of Unused bytes in the data stream. When UNUSEDEN is set to logic 1, an all one or an all zero pattern is inserted in the Unused bytes according to the value set in the UNUSEDV register bit. When UNUSEDEN is set to logic 0, no pattern is inserted. **NOTE: If the Transmit FEC encoder is enabled, any change to the Line overhead, payload overhead or to the payload itself, after the FEC codes have been inserted, will invalidate the FEC calculations. Under normal operation this bit should not be changed**

UNUSEDV

The Unused value (UNUSEDV) bit controls the value inserted in the Unused bytes. When UNUSEDV is set to logic 1, an all one pattern is inserted in the Unused bytes if enable via the UNUSEDEN register bit. When UNUSEDV is set to logic 0, an all zero pattern is inserted in the Unused bytes if enable via the UNUSEDEN register bit.

Register 1052H: TRSP Error Insertion

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	R/W	B2DISABLE (see attached note)	0
Bit 7	R/W	B1DISABLE (see attached note)	0
Bit 6	R/W	LOSINS	0
Bit 5	R/W	LAISINS	0
Bit 4	R/W	LRDIINS	0
Bit 3	R/W	A1ERR	0
Bit 2	R/W	Reserved	1
Bit 1	R/W	Reserved	1
Bit 0	R/W	Reserved	1

A1ERR

The A1 error insertion (A1ERR) bit is used to introduce framing errors in the A1 bytes. When A1ERR is set to logic 1, 76h instead of F6h is inserted in all of the A1 bytes of the STS-12/STM-4 #1. When A1ERR is set to logic 0, no framing errors are introduced. The A1ERR will take precedence over the A1A2EN bit in the TRSP Configuration Register.

LRDIINS

The line RDI insertion (LRDIINS) bit is used to force a line remote defect indication in the data stream. When LRDIINS is set to logic 1, the 110 pattern is inserted in bits 6, 7 and 8 of the K2 byte of STS-1/STM-0 #1 to force a line RDI condition. When LRDIINS is set to logic 0, the line RDI condition is removed.

LAISINS

The line AIS insertion (LAISINS) bit is used to force a line alarm indication signal in the data stream. When LAISINS is set to logic 1, all ones are inserted in the line overhead and in the payload (all the bytes of the frame except the section overhead bytes) to force a line AIS condition. When LAISINS is set to logic 0, the line AIS condition is removed. Line AIS is inserted/removed on frame boundary before scrambling. **NOTE: This bit must be set to the same value as the LAISINS bits in registers 1062H, 1072H, and 1082H.**

LOSINS

The LOS insertion (LOSINS) bit is used to force a loss of signal condition in the data stream. When LOSINS is set to logic 1, the data steam is set to all zero (after scrambling) to force a loss of signal condition. When LOSINS is set to logic 0, the loss of signal condition is removed. **Note, this bit must be set to the same value as the other LOSINS bits in registers 1062H, 1072H and 1082H.**

B1DISABLE

The B1 disable insertion (B1DISABLE) bit is used to set the B1 byte in a pass through mode. When B1DISABLE is set to logic one, the B1 byte value from the QSFI-4 interface is passed through transparently without being overwritten. When B1DISABLE is set to logic zero, a valid B1 byte is inserted. **Note, the TIFE will always recalculate and insert the B2 byte into the frame whether it is in state 1 or state 2 as defined by STATE[1:0] bits in Register 1040H. As a result the B1 must always be recalculated in the TRSP if the TIFE block is placed in either state.**

B2DISABLE

The B2 disable insertion (B2DISABLE) bit is used to set the B2 byte in a pass through mode. When B2DISABLE is set to logic one, the B2 byte value from the FEC encoder or the TXDATAn bus is passed through transparently without being overwritten. When B2DISABLE is set to logic zero, a valid B2 byte is inserted on the data output stream. **NOTE: The B2DISABLE bit must be set to logic '1' if the FEC encoder is enabled. If this bit is not set to logic 0 then the B2 inserted by the FEC encoder will be corrupted resulting is false B2 error indications and or FEC decoding failures downstream. The B2DISABLE bits in Registers 1062H, 1072H and 1082H must also be set to logic 1 when this bit is set to logic 1.**

Register 1053H: TRSP Transmit J0 and Z0

Bit	Type	Function	Default
Bit 15	R/W	J0V[7]	0
Bit 14	R/W	J0V[6]	0
Bit 13	R/W	J0V[5]	0
Bit 12	R/W	J0V[4]	0
Bit 11	R/W	J0V[3]	0
Bit 10	R/W	J0V[2]	0
Bit 9	R/W	J0V[1]	0
Bit 8	R/W	J0V[0]	1
Bit 7	R/W	Z0V[7]	1
Bit 6	R/W	Z0V[6]	1
Bit 5	R/W	Z0V[5]	0
Bit 4	R/W	Z0V[4]	0
Bit 3	R/W	Z0V[3]	1
Bit 2	R/W	Z0V[2]	1
Bit 1	R/W	Z0V[1]	0
Bit 0	R/W	Z0V[0]	0

Z0V[7:0]

The Z0 byte value (Z0V[7:0]) bits hold the Z0 growth byte to be inserted in the data stream. The Z0V[7:0] value is inserted in the Z0 bytes if the insertion is enabled via the Z0REGEN bit in the TRSP Register Insertion register. The Z0DEF bit in the TRSP Configuration register defines the Z0 bytes.

J0V[7:0]

The J0 byte value (J0V[7:0]) bits hold the section trace to be inserted in the data stream. The J0V[7:0] value is inserted in the J0 byte of STS-1/STM-0 #1 if the insertion is enabled via the J0REGEN bit in the TRSP Register Insertion register.

Register 1054H: TRSP Transmit E1 and F1

Bit	Type	Function	Default
Bit 15	R/W	E1V[7]	0
Bit 14	R/W	E1V[6]	0
Bit 13	R/W	E1V[5]	0
Bit 12	R/W	E1V[4]	0
Bit 11	R/W	E1V[3]	0
Bit 10	R/W	E1V[2]	0
Bit 9	R/W	E1V[1]	0
Bit 8	R/W	E1V[0]	0
Bit 7	R/W	F1V[7]	0
Bit 6	R/W	F1V[6]	0
Bit 5	R/W	F1V[5]	0
Bit 4	R/W	F1V[4]	0
Bit 3	R/W	F1V[3]	0
Bit 2	R/W	F1V[2]	0
Bit 1	R/W	F1V[1]	0
Bit 0	R/W	F1V[0]	0

F1V[7:0]

The F1 byte value (F1V[7:0]) bits hold the section user channel to be inserted in the data stream. The F1V[7:0] value is inserted in the F1 byte of STS-1/STM-0 #1 if the insertion is enabled via the F1REGEN bit in the TRSP Register Insertion register.

E1V[7:0]

The E1 byte value (E1V[7:0]) bits hold the section order wire to be inserted in the data stream. The E1V[7:0] value is inserted in the E1 byte of STS-1/STM-0 #1 if the insertion is enabled via the E1REGEN bit in the TRSP Register Insertion register.

Register 1055H: TRSP Transmit D1D3

Bit	Type	Function	Default
Bit 15	R/W	D1D3V[7]	0
Bit 14	R/W	D1D3V[6]	0
Bit 13	R/W	D1D3V[5]	0
Bit 12	R/W	D1D3V[4]	0
Bit 11	R/W	D1D3V[3]	0
Bit 10	R/W	D1D3V[2]	0
Bit 9	R/W	D1D3V[1]	0
Bit 8	R/W	D1D3V[0]	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

D1D3V[7:0]

The D1D3 byte value (D1D3V[7:0]) bits hold the section data communication channel to be inserted in the data stream. The D1D3V[7:0] value is inserted in the D1 to D3 bytes of STS-1/STM-0 #1 if the insertion is enabled via the D1D3REGEN bit in the TRSP Register Insertion register.

Register 1056H: TRSP Reserved

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

Register 1057H: TRSP Reserved

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

Register 1058H: TRSP Reserved

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

Register 1059H: TRSP Reserved

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

Register 105AH: TRSP Transmit B1Mask

Bit	Type	Function	Default
Bit 15	R/W	B1MASK[7]	0
Bit 14	R/W	B1MASK[6]	0
Bit 13	R/W	B1MASK[5]	0
Bit 12	R/W	B1MASK[4]	0
Bit 11	R/W	B1MASK[3]	0
Bit 10	R/W	B1MASK[2]	0
Bit 9	R/W	B1MASK[1]	0
Bit 8	R/W	B1MASK[0]	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

B1MASK[7:0]

The B1 mask (B1MASK[7:0]) bits hold the B1 BIP-8 errors to be inserted in the data stream. The B1MASK[7:0] is XOR'ed with the calculated B1 before insertion in the B1 byte.

Register 105B-105FH: unused

Register 1060H: TRSP Aux1 Configuration

Register 1070H: TRSP Aux2 Configuration

Register 1080H: TRSP Aux3 Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	1
Bit 9	R/W	Reserved	1
Bit 8	R/W	Reserved	1
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	1
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	J0Z0INCEN	0
Bit 1	R/W	Z0DEF	0
Bit 0	R/W	A1A2EN	1

A1A2EN

The A1A2EN bit must be set to the same value as the A1A2EN bit in the TRSP Configuration Register.

Z0DEF

The Z0DEF bits must be set to the same value as the Z0DEF bit in the TRSP Configuration Register.

J0Z0INCEN

The J0Z0INCEN must be set to the same value as the J0Z0INCEN bit in the TRSP Configuration Register.

Register 1061H: TRSP Aux1 Register Insertion

Register 1071H: TRSP Aux2 Register Insertion

Register 1081H: TRSP Aux3 Register Insertion

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	—	Unused	X
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Z0REGEN (See attached note)	1
Bit 0	R/W	Reserved	1

Z0REGEN

The Z0 register enable (Z0REGEN) bit controls the insertion of Z0 growth bytes in the data stream. When Z0REGEN is set to logic 1, the Z0 growth byte from the TRSP Transmit J0 and Z0 register is inserted in the Z0 bytes for STS-2,6,10 and 14 (Aux1) or STS-3,7,11,15 (Aux2) or STS-4,8,12,16 (Aux3).. When Z0REGEN is set to logic 0, the Z0 growth byte from the TRSP Transmit J0 and Z0 register is not inserted. The Z0DEF bit in the TRSP Configuration register bit defines the Z0 bytes. **NOTE: If the Z0REGEN is enabled the CRSU 4x2488 will overwrite any data written to the Z0 byte by any down stream device. Under normal operation this bit should be disabled.**

Register 1062H: TRSP Aux1 Error Insertion

Register 1072H: TRSP Aux2 Error Insertion

Register 1082H: TRSP Aux3 Error Insertion

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	R/W	B2DISABLE	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	LOSINS	0
Bit 5	R/W	LAISINS	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	1
Bit 1	R/W	Reserved	1
Bit 0	R/W	Reserved	1

LAISINS

This bit must be set to the same value as the LAISINS bit in the TRSP Error Insertion registers.

LOSINS

This bit must be set to the same value as the LOSINS bit in the TRSP Error Insertion register.

B2DISABLE

The B2 disable insertion (B2DISABLE) bit is used to set the B2 byte in a pass through mode. When B2DISABLE is set to logic one, the B2 byte value from the FEC encoder or the TXDATAn bus is passed through transparently without being overwritten. When B2DISABLE is set to logic zero, a valid B2 byte is inserted on the data out stream. **NOTE: The B2DISABLE bit must be set to logic '1' if the FEC encoder is enabled. If this bit is not set to logic 0 than the B2 inserted by the FEC encoder will be corrupted resulting is false B2 error indications. The B2DISABLE bit in Register 1052H must also be set to logic 1 when this bit is set to logic 1.**

Register 1063H: TRSP Aux1 Transmit Z0

Register 1073H: TRSP Aux2 Transmit Z0

Register 1083H: TRSP Aux3 Transmit Z0

Bit	Type	Function	Default
Bit 15	R/W	RESERVED	0
Bit 14	R/W	RESERVED	0
Bit 13	R/W	RESERVED	0
Bit 12	R/W	RESERVED	0
Bit 11	R/W	RESERVED	0
Bit 10	R/W	RESERVED	0
Bit 9	R/W	RESERVED	0
Bit 8	R/W	RESERVED	1
Bit 7	R/W	Z0V[7]	1
Bit 6	R/W	Z0V[6]	1
Bit 5	R/W	Z0V[5]	0
Bit 4	R/W	Z0V[4]	0
Bit 3	R/W	Z0V[3]	1
Bit 2	R/W	Z0V[2]	1
Bit 1	R/W	Z0V[1]	0
Bit 0	R/W	Z0V[0]	0

Z0V[7:0]

The Z0 byte value (Z0V[7:0]) bits hold the Z0 growth byte to be inserted in the data stream. The Z0V[7:0] value is inserted in the Z0 bytes if the insertion is enabled via the Z0REGEN bit in the TRSP Register Insertion register. The Z0DEF bit in the TRSP Configuration register defines the Z0 bytes.

Register 1064-106AH: TRSP Aux1 Reserved

Register 106BH- 106FH Unused

Register 1074-107AH: TRSP Aux2 Reserved

Register 107BH- 107FH unused

Register 1084-108AH: TRSP Aux3 Reserved

Register 108BH- 108FH unused

Register 1090H: STLI Clock Configuration

Bit	Type	Function	Default
Bit 15	R/W	Reserved	1
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	TCLKEN	0
Bit 0	R/W	TDCLKEN (See Attached Note)	0

TDCLKEN

The transmit clock enable (TDCLKOEN) bit controls the gating of the internal parallel transmit clock. When TDCLKOEN is set to logic 1, the TDCLKO output clock operates normally. When TDCLKOEN is set to logic 0, the TDCLKO output clock is held low. **NOTE: This register bit must be set to logic 1 when sonet or fec functionality is enabled in transmit slices.**

TCLKEN

The transmit clock enable (TCLKEN) bit controls the gating of the TCLK[0] output clock. When TCLKEN is set to logic 1, the TCLK[0] output clock operates normally. When TCLKEN is set to logic 0, the TCLK[0] output clock is held low.

Register 10A0H: TXLI Control/Status

Bit	Type	Function	Default
Bit 15	R	ROOL_I	X
Bit 14	R	Reserved	X
Bit 13	—	Unused	X
Bit 12	R	Reserved	X
Bit 11	R/W	Reserved	1
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	R/W	TX_DISABLE	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	TXCML	0
Bit 5	R/W	PRBS_FPATT	0
Bit 4	R/W	PRBS_ENABLE	0
Bit 3	R/W	LPLE_TX	0
Bit 2	R/W	INV_DATA	0
Bit 1	R	ROOL_V	X
Bit 0	R/W	ROOL_EN	0

ROOL_EN

The Reference Out Of Lock Enable bit connects the ROOL_I status bit to the TXLI_INT_0 bit of the Master Interrupt Status TX CH0 register 0006H, bit 13. When ROOL_EN is set to logic one, the TXLI_INT_0 bit is set to logic 1 upon assertion of the ROOL_I register bit. When ROOL_EN is set low, a change in the ROOL_I status does not generate an interrupt.

ROOL_V

The Reference Out Of Lock status bit indicates the current status of the ROOL detector. The ROOL_V is only latched during a read operation and therefore will change to reflect the current status the ROOL compare logic. See ROOL_I for details of the ROOL function.

INV_DATA

The Serial Data Inversion INV_DATA controls the polarity of the transmitter data. When INV_DATA is set to ‘1’ the polarity of the TXD_P/TXD_N input pins are inverted. When INV_DATA is set to ‘0’ the TXD_P/TXD_N inputs operate normally.

LPLE_TX

The Line Side Parallel Loopback enable loops the recovered data and clock from the RXD[0]+/- input pin to the transmit output, TXD[0]+/- pin. When this bit is set to logic 1 data from the 2.488 Gbs line side Receiver is input into the PISO and data from the QSFI-4 TXDATA interface is ignored. **NOTE: The LOOPTIMEB bit of the TXLI CSU Control register must be set to logic 0 and the LPLE_RX bit of the RXLI CRU Clock Training register 1103H set to logic 1, when LPLE_TX is enabled.**

PRBS_ENABLE

This bit enables the generation of a PRBS23 polynomial data stream or a fixed pattern in place of the normal transmit data. When low, the data output on the TXD[0]+/- pins contains data from the QSFI-4 interface. When PRBS_ENABLE is set to a logic 1 the data output on the TXD[0]+/- pins contains PRBS words or a fixed pattern depending on the value of the PRBS_FPATT bit.

PRBS_FPATT

This bit enables the generation of a PRBS or a fixed pattern in place of the normal transmit data. When low, the TXD[0]+/- output pins contains PRBS words, and when high the fixed pattern written into the PATTERN[15:0] Register is output.

TXCML

The TXCML control bits are used to place the 2.488 Gbs Transmitter outputs, TXD[0]+/-, into one of the following operating modes:

Table 10 TX2488 Mode Control

TXCML Value	Description
1	AC coupling suitable for CML compatible Optical data link devices are used. In this mode a 16mA bias current is generated for the differential CML transmitter that is based on an internal reference resistor matched with the output stage load. The generated current produces a reduced-swing differential CML output amplitude (0.533 Vppd typ.).
0	AC coupling suitable for CML compliant ODL transmitters is used. In this mode a 30.5mA bias current is generated for the differential CML transmitter that is based on an internal reference resistor matched with the output stage load. The generated current produces the standard differential amplitude (default swing of 1.0 Vppd typ.) on 50-Ohm single-ended, or 100 Ohm differential, output terminations (also see section 14.3.1 and 14.3.2).

TX_DISABLE

The Transmitter Disable bit controls the output of the TXD[0]+/- pins of the CRSU 4x2488. If TX_DISABLE is set to logic '1' the output on the TXD[0]+/- pins is forced to the active high state. If TX_DISABLE is set to logic '0' the output on the TXD[0]+/- contains the normal 2.488 Gbs transmit data.

ROOL_I

The reference out of lock status indicates the clock synthesis unit (CSU) phase locked loop is unable to lock to the reference clock on REFCLK[0]+/- or the recovered clock from the RXD[0]+/- or RXD[1]+/- input signal depending on the state of the RECCLK_SEL and LOOPTIMEB bits in register 10A1H. ROOL_I is a logic one if the divided down synthesized clock frequency is greater or less than 1000 ppm of the REFCLK[0]+/- frequency. The ROOL_I signal is a latched value of the frequency compare logic and only indicates that the synthesized clock has failed to lock at some point and does not reflect the current state. At start-up, ROOL_I may be latched to logic 1 for several hundred milliseconds while the PLL obtains lock. To insure that the synthesized clock has locked this bit should be read twice separated by at least 500 uSec. If the WCIMODE bit in register 000BH is set to logic 1, only over-writing with a ‘1’ clears this bit. If the WCIMODE bit is set to a logic 0 than a read of this register automatically clears the bit.

Register 10A1H: TXLI CSU Control

Bit	Type	Function	Default
Bit 15	R/W	RECCLK_SEL	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	CSU_RESET	0
Bit 12	R/W	Reserved	1
Bit 11	R/W	TX2488_ENABLE	1
Bit 10	R/W	Reserved	1
Bit 9	R/W	Reserved	1
Bit 8	R/W	Reserved	0
Bit 7	R/W	LOOPTIMEB	1
Bit 6	R/W	LF_RESISTOR[1]	1
Bit 5	R/W	LF_RESISTOR[0]	1
Bit 4	R/W	Reserved	0
Bit 3	R/W	DIVIDE_RATIO	1
Bit 2	R/W	Reserved	0
Bit 1	R/W	CHARGE_PUMP[1]	0
Bit 0	R/W	CHARGE_PUMP[0]	0

CHARGE_PUMP[1:0]

Configurable output current of the programmable charge pump**. NOTE : these bits are required to be programmed when LOOPTIME operation is required. See operations section 13.7 for looptime configuration setup.**

Bits 1:0	Current Value	
0:0	± 64µA:	**(DEFAULT)**
0:1	± 32µA:	**(LOOP-TIME MODE)**
1:X	± 16µA:	

DIVIDE_RATIO

Sets the divide ratio for the feedback signal to be used in Hogge-II Phase detector. **NOTE : these bits are required to be programmed when LOOPTIME operation is required. See operations section 13.7 for looptime configuration setup.**

0 - divide by 8 **(LOOP-TIME MODE)**

1 - divide by 1 **(DEFAULT)**

Note: In non-loop time operation (LOOPTIMEB set to logic one) this bit must be set to logic one (divide by 1) to insure proper operation. In loop-time (LOOPTIMEB set to logic zero) this bit must be set to logic 0 (divide by 8). If the LPTIMB pin is set low the correct value of this DIVIDE_RATIO bit is automatically selected

LF_RESISTOR[1:0]

Loop filter resistor selects. They allow configuration of loop filter parameters i.e bandwidth, lower bandwidth used for looptime setting. **NOTE : these bits are required to be programmed when LOOPTIME operation is required. See operations section 13.7 for looptime configuration setup.**

Bits [1:0]	Resistor Value	
11	2 x 10KΩ	**(DEFAULT)**
10	2 x 9KΩ	
01	Invalid Mode	
00	2 x 2.5KΩ	**(LOOP-TIME MODE)**

LOOPTIMEB

Used to select the input reference clock for the Transmitter 2.488 Gbs CSU. When set to logic zero the Recovered Line Clock from channel 0 or the Recovered Line Clock from channel 1 is selected as the reference for the transmit CSU clock when the relevant CRU is in a lock to data state (DOOLV status bit = 1'b1). The state of the RECCLK_SEL bit determines which of the Recovered Clocks, same channel or cross channel is used. When this bit is set to logic one the REFCLK[0]+/- input pins are selected as the reference for the transmit CSU clock. A read of this bit will return the looptime input to the CSU. **NOTE: if this bit is asserted to logic '0', looptime enabled, other bits are required to be set. See operations section 13.7 for complete looptime configuration setup.**

TX2488_ENABLE

The 2.488GHz Transmitter Enable provides a global power down of the TX2488 Analog Block Circuit. When set to '0' this bit forces the Transmitter to a low power state and functionality is disabled. When set to '1' the Transmitter operates in the normal mode of operation.

CSU_RESET

The Clock Source Unit Reset provides a complete reset of the CSU2488 Analog Block Circuit. When set to ‘1’ this bit forces the ABC to a known initial state. While the bit is set to ‘1’ the functionality of the block is disabled. When set to ‘0’ the ABC operates in the normal mode of operation. This bit is not self-clearing. Therefore a ‘0’ must be written to the bit to remove the reset condition.**NOTE: When asserted, CSU_RESET must be set to logic 1 for at least 2ms.**

RECCLK_SEL

The Recovered Clock Select bit controls the source of the reference when the LOOPTIMEB register bit is set to logic '0'. When RECCLK_SEL is set to logic '1' the source for the CSU reference clock is the recovered clock from the receive CRU of the adjacent channel. For the channel 0 Transmit CSU the source is channel 1 and for channel 1 the source is the channel 0. The same applies between Channels 2 and 3. There is no connection between channels 0 and 2 or 3 and 1 and 2 or 3. When RECCLK_SEL is set to logic '0' the source for the transmit CSU is from the Receive CRU of the same channel.

Register 10A2H: TXLI Pattern Register

Bit	Type	Function	Default
Bit 15	R/W	FPATT[15]	0
Bit 14	R/W	FPATT[14]	0
Bit 13	R/W	FPATT[13]	0
Bit 12	R/W	FPATT[12]	0
Bit 11	R/W	FPATT[11]	0
Bit 10	R/W	FPATT[10]	0
Bit 9	R/W	FPATT[9]	0
Bit 8	R/W	FPATT[8]	0
Bit 7	R/W	FPATT[7]	0
Bit 6	R/W	FPATT[6]	0
Bit 5	R/W	FPATT[5]	0
Bit 4	R/W	FPATT[4]	0
Bit 3	R/W	FPATT[3]	0
Bit 2	R/W	FPATT[2]	0
Bit 1	R/W	FPATT[1]	0
Bit 0	R/W	FPATT[0]	0

FPATT[15:0]

The FPATT[15:0] provides the fixed pattern that will be monitored for when the PRBS_FPATT bit is set to a logic 1. If PRBS_FPATT is set to logic 0 this register is not used.

Register 1100H: RXLI Interrupt Status

Bit	Type	Function	Default
Bit 15	R	CRU_CLOCK	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R	PRBS_SYNC_I	0
Bit 4	R	PRBS_ERR_I	0
Bit 3	R	FIFO_ERROR_I	0
Bit 2	R	LOS_I	0
Bit 1	R	DOOL_I	0
Bit 0	R	ROOL_I	0

ROOL_I

The reference out-of-lock status indicates the clock recovery unit (CRU) phase locked loop is unable to lock to the reference clock on the REFCLK[0]+/- input pin. ROOL_I is logic one if the synthesized clock frequency is greater or less than 1000 ppm of the REFCLK[0]+/- frequency. The ROOL_I signal is a latched value of the frequency compare logic and only indicates that the synthesized clock has failed to lock at some point and does not reflect the current state. The ROOLV bit in register 1103H indicates the current state of the frequency compare logic. At start-up, ROOL_I may be latched to logic 1 for several hundred milliseconds while the PLL obtains lock. To insure that the synthesized clock has locked this bit should be read twice separated by at least 500 uSec. If the WCIMODE bit in register 000BH is set to logic 1, only over-writing with a '1' clears this bit. If the WCIMODE bit is set to logic 0 than a read of this register automatically clears the bit.

DOOL_I

The recovered data out of lock status indicates the clock recovery unit (CRU) phase locked loop is unable to recover and lock to the input data stream. DOOL_I is a logic one if the divided down recovered 2.488 GHz Line clock frequency is greater or less than 1000 ppm of the REFCLK[0]+/- input pin frequency or if no transitions have occurred on the RXD[0]+/- input for more than value set in the LOS_COUNT[4:0] bits. The DOOL_I signal is a latched value of the frequency compare logic and only indicates that the synthesized clock has failed to lock at some point and does not reflect the current state. The DOOLV bit in register 1103H indicates the current state of the frequency compare logic. If the WCIMODE bit in register 000BH is set to logic 1, only over-writing with a '1' clears this bit. If the WCIMODE bit is set to logic 0 than a read of this register automatically clears the bit.

LOS_I

The loss of signal status indicates the receive signal has exceeded a maximum number of consecutive ones or zeros. LOS_I is a logic zero if the SD[0] input pin is high or less than LOS_COUNT[4:0] consecutive ones or zeros have been received. LOS_I is a logic one if the SD[0] input pin is low and LOS_COUNT[4:0] consecutive ones or zeros have been received. If the WCIMODE bit in register 000BH is set to logic 1, only over-writing with a '1' clears this bit. If WCI_MODE is set to logic 0 than a read of this register automatically clears the bit.

FIFO_ERROR_I

The FIFO Error bit provides a status indication of an underflow or overflow condition in the Line side Receiver elastic data store. The Receiver elastic store buffers the data between the line side Data Recovery Unit and the system side. When FIFO_ERROR_I is set to '1' the data in the elastic store has been corrupted and invalid data has been read from the FIFO. If the WCIMODE bit in register 000BH is set to logic 1, only over-writing with a '1' clears this bit. If the WCIMODE bit is set to logic 0 than a read of this register automatically clears the bit.

PRBS_ERR_I

The PRBS-23 Bit Error bit provides a status indication that a bit error has been detected in the comparison between the incoming data from the RXD[0]+/- pins and the locally generated PRBS-23 polynomial data. The PRBS_ERR_I is set high when the monitor is in the synchronized state and when an error in a PRBS-23 word is detected. If the WCIMODE bit in register 000BH is set to logic 1, only over-writing with a '1' clears this bit. If the WCIMODE bit is set to logic 0 than a read of this register automatically clears the bit.

PRBS_SYNC_I

The PRBS Synchronization bit indicates that a change in the status of PRBS Monitor has occurred. The comparison is made between the incoming data from the RXD[0]+/- and the PRBS pattern generated locally. The PRBS_SYNC_I is set high when the monitor is in the synchronized state and has received two consecutive corrupted words forcing the PRBS monitor to resynchronize. If the WCIMODE bit in register 000BH is set to logic 1, only over-writing with a '1' clears this bit. If the WCIMODE bit is set to logic 0 than a read of this register automatically clears the bit.

CRU_CLOCK

The CRU_CLOCK status bit monitors the state of the CRU clock. Each time this register is read the sampling register is reset. The CRU_CLOCK is set high when the CRU clock transitions from low to high at least once. The CRU_CLOCK is reset low after this register is read and will remain low if no transitions occur on the CRU clock.

Register 1101H: RXLI Interrupt Control

Bit	Type	Function	Default
Bit 15	R/W	SD_DISABLE	0
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R/W	PRBS_SYNC_EN	0
Bit 4	R/W	PRBS_ERR_EN	0
Bit 3	R/W	FIFO_ERROR_EN	0
Bit 2	R/W	LOS_EN	0
Bit 1	R/W	DOOL_EN	0
Bit 0	R/W	ROOL_EN	0

ROOL_EN

The Reference Out Of Lock Enable bit connects the ROOL_I status bit to the RXLI_INT_0 bit of Master Interrupt Status RX CH0 Register, 0002H. When ROOL_EN is set to logic one, the RXLI_INT_0 bit will be set to logic 1 upon assertion of the ROOL_I register bit. When ROOL_EN is set low, a change in the ROOL_I status does not generate an interrupt.

DOOL_EN

The Data Out Of Lock Enable bit connects the DOOL_I status bit to the RXLI_INT_0 bit of the Master Interrupt Status RX CH0 Register, 0002H. When DOOL_EN is set to logic one, the RXLI_INT_0 bit will be set to logic 1 upon assertion of the DOOL_I register bit. When DOOL_EN is set low, a change in the DOOL_I status does not generate an interrupt.

LOS_EN

The Loss of Signal Enable bit connects the LOS_I status bit to the RXLI_INT_0 bit of the Master Interrupt Status RX CH0 Register, 0002H. When LOS_EN is set to logic one, the RXLI_INT_0 bit will be set to logic 1 upon assertion of the LOS_I register bit. When LOS_EN is set low, a change in the LOS_I status does not generate an interrupt.

FIFO_ERROR_EN

The FIFO Error Enable bit connects the FIFO_ERROR_I status bit to the RXLI_INT_0 bit of the Master Interrupt Status RX CH0 Register, 0002H . When FIFO_ERROR_EN is set to logic one, the RXLI_INT_0 bit will be set to logic 1 upon assertion of the FIFO_ERROR_I register bit. When FIFO_ERROR_EN is set low, a change in the FIFO_ERROR_I status does not generate an interrupt.

PRBS_ERR_EN

The PRBS Error Enable bit connects the PRBS_ERR_I status bit to the RXLI_INT_0 bit of the Master Interrupt Status RX CH0 Register, 0002H . When PRBS_ERR_EN is set to logic one, the RXLI_INT_0 bit will be set to logic 1 upon assertion of the PRBS_ERR_I register bit. When PRBS_ERR_EN is set low, a change in the PRBS_ERR_I status does not generate an interrupt.

PRBS_SYNC_EN

The PRBS Synchronized Enable bit connects the PRBS_SYNC_I status bit to the RXLI_INT_0 bit of the Master Interrupt Status RX CH0 Register, 0002H . When PRBS_SYNC_EN is set to logic one, the RXLI_INT_0 bit will be set to logic 1 upon assertion of the PRBS_SYNC_I register bit. When PRBS_SYNC_EN is set low, a change in the PRBS_SYNC_I status does not generate an interrupt.

SD_DISABLE

The Signal Detect Disable bit controls the operation of the SD[0] input pin. When SD_DISABLE is set to a logic one the SD[0] input will be ignored and internal signal will be forced to the active high state and all down stream blocks will operate normally. When SD_DISABLE is set to logic zero the internal signal follows the state of the SD[0] input pin and the state of SD_INV bit.

Register RXLI 1102H: CRU Control

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	CRU_RESET	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	RX2488_ENABLE	1
Bit 11	R/W	Reserved	1
Bit 10	R/W	LOCK_TO_REF	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	SDLE	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	1
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	1
Bit 2	R/W	LOCK_TO_DATA	0
Bit 1	R/W	Reserved	1
Bit 0	R/W	Reserved	1

LOCK_TO_DATA

The Lock to Data bit controls the operation of the CRU state machine. When LOCK_TO_DATA is set to logic '1' the CRU is forced to remain locked to the data, regardless of the quality of the received data. When set to logic '0' the CRU state machine controls the CRU.

NOTE: If both the LOCK_TO_DATA and LOCK_TO_REF are both set to logic 1 the LOCK_TO_DATA bit will take precedence.

When in “lock to data” state and data is removed, the CRU will track to either of it’s limits. In order to re-centre the CRU, lock to data state must be removed to allow the CRU to re-train. For proper operation data should be present when the lock to data bit is set to logic one.

SD (signal detect) will override LOCK_TO_DATA. If SD goes low, the cru will move to a LOCK_TO_REFERENCE state. If SD is high the CRU will remain in the LOCK_TO_DATA state.

SDLE

The Serial Diagnostic Loopback Enable (SDLE) bit, when set to ‘1’, loops the data from the transmit line side PISO to the receive side SIPO. Setting the SDLE to logic '1' is equivalent to connecting the TXD[0]+/- output pins to the RXD[0]+/- input pins. When the SDLE is set to logic '0 the Receive data is taken from the RXD[0]+/- pins.LOCK_TO_REF

The Lock to Reference bit controls the operation of the CRU state machine. When LOCK_TO_REF is set to logic one the CRU state machine will hold the CRU in the Lock-to-Reference state. When the CRU is reset to logic zero the CRU state machine operates normally. NOTE: If both the LOCK_TO_DATA and LOCK_TO_REF are both set to logic 1 the LOCK_TO_DATA bit will take precedence. When LOCK_TO_REF is enabled the DOOL interrupt can give false indications and should be disabled.

RX2488_ENABLE

The 2.488GHz Receiver Enable provides a global power down of the RX2488 Analog Block Circuit. When set to ‘0’, this bit forces the Receiver circuitry to a low power state and functionality is disabled. When set to ‘1’, the receiver operates in the normal mode of operation.

CRU_RESET

The Clock Recovery Unit (CRU) Reset provides a complete reset of the CRU Circuitry. When set to ‘1’ this bit forces the CRU to a known initial state. While the bit is set to ‘1’ the functionality of the block is disabled. When set to ‘0’ the CRU operates in the normal mode of operation. This bit is not self-clearing. Therefore a ‘0’ must writing to the bit to remove the reset condition. **NOTE: to ensure a complete CRU reset, this bit should be toggled for a minimum period of 100μS.**

Register 1103H: RXLI CRU Clock Training Configuration and Status

Bit	Type	Function	Default
Bit 15	R/W	LOS_COUNT[4]	0
Bit 14	R/W	LOS_COUNT[3]	1
Bit 13	R/W	LOS_COUNT[2]	0
Bit 12	R/W	LOS_COUNT[1]	0
Bit 11	R/W	LOS_COUNT[0]	0
Bit 10	R/W	LOSEN	1
Bit 9	R/W	LPLE_RX	0
Bit 8	R/W	INV_SD	0
Bit 7	R/W	INV_DATA	0
Bit 6	R	DOOLV	X
Bit 5	R	ROOLV	X
Bit 4	R	TRAIN	X
Bit 3	R/W	Reserved	1
Bit 2	R/W	Reserved	1
Bit 1	R/W	Reserved	1
Bit 0	R/W	Reserved	1

TRAIN

The CRU reference training status indicates if the CRU is in the process of locking to the reference clock or locking to the receive data. TRAIN is logic zero if the CRU is locking or locked to the reference clock. TRAIN is a logic one if the CRU is locking or locked to the receive data. TRAIN is invalid if the LOCK_TO_REF or LOCK_TO_DATA bits, Register 1102H, are set to logic one.

ROOLV

The recovered reference out of lock status indicates that the clock recovery phase locked loop is unable to lock to the reference clock, REFCLK. ROOLV is logic one if the divided down synthesized clock frequency is not within approximately 488ppm of the REFCLK frequency. At startup, ROOLV may remain at logic 1 for several hundred milliseconds while the PLL obtains lock. **Note: To ensure correct operation of this status bit, LOSEN bit (bit 10 Reg 1103) must be set to logic 1.**

DOOLV

The recovered data out of lock status indicates that the clock recovery phase locked loop is unable to recover and lock to the input data stream. DOOLV is logic one if the divided down recovered clock frequency is not within approximately 1000ppm of the REFCLK frequency or if LOS_I interrupt has been triggered. **Note: To ensure correct operation of this status bit, LOSEN bit (bit 10 Reg 1103) must be set to logic 1.**

INV_DATA

The Serial Data Inversion INV_DATA controls the polarity of the received data. When INV_DATA is set to ‘1’ the polarity of the RXD[0]+/- input pins invert. When INV_DATA is set to ‘0’ the RXD[0]+/- inputs operate normally.

INV_SD

The Signal Detect Inversion INV_SD controls the polarity of the SD[0] input pin. When INV_SD is set to ‘1’ the polarity of the SD[0] input pin is inverted. When INV_SD is set to ‘0’ the polarity of the SD[0] input remains unchanged.

LPLE_RX

The Line Side Parallel loopback configures the receive side for loopback operation. When LPLE_RX is set to logic '1' the input data from the RXD[0]+/- pin is timed to the Transmit clock and can be looped back to the Transmit side (TXD[0]+/-) if the LPLE_TX bit the TXLI Control/Status Register 10A0H is also set to logic '1'. When LPLE_RX is set to logic zero the input data is timed using either the CSU clock or the CRU clock depending on the state of the SOURCE_CLOCK bit, Register 1104H bit 4. **NOTE: When LPLE_RX is set to logic '1' the data sent to the RXDATA system side QSFI-4 interface will be corrupted. When LPLE_RX is enabled the LOOPTIMEB bit of the TXLI CSU Control Register, 10A1H, must be set to logic 0 and the LPLE_TX bit of the TXLI Control/Status register 10A0H must be set to logic 1.**

LOSEN

The loss of signal enable bit controls the signal detection logic. The CRU uses the LOS detector along with the clock difference detector to determine if the CRU is locked to data. When LOSEN is set to logic one the incoming signal is monitored for 1's/0's transitions as determined by LOS_COUNT[4:0] register bits. If LOSEN is reset to logic zero the 1's/0's transition detector is disabled and only the reference clock difference detector is used to determine the status of the 2.488 Gbits/s serial data stream.

LOS_COUNT[4:0]

The Loss of signal 1's/0's transition detector count value. This field sets the value for the number of consecutive all-zeros or all-ones pattern that will force the CRU out of the LOCK TO DATA State. The value in the LOS_COUNT represents a set of sixteen ones or zeros in the pattern, accurate to +/- 15 bits. I.e. to set the consecutive all-ones or all-zeros pattern to 128 the LOS_COUNT should be set to "01000"b. The default value for this field is 128.

Register 1104H: RXLI PRBS Control

Bit	Type	Function	Default
Bit 15	R	PRBS_ERR_CNT[7]	0
Bit 14	R	PRBS_ERR_CNT[6]	0
Bit 13	R	PRBS_ERR_CNT[5]	0
Bit 12	R	PRBS_ERR_CNT[4]	0
Bit 11	R	PRBS_ERR_CNT[3]	0
Bit 10	R	PRBS_ERR_CNT[2]	0
Bit 9	R	PRBS_ERR_CNT[1]	0
Bit 8	R	PRBS_ERR_CNT[0]	0
Bit 7	R/W	CLEAR_ERR_CNT	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R	SYNC_STAT	0
Bit 2	R/W	PRBS_FPATT	0
Bit 1	R/W	PRBS_ENABLE	0
Bit 0	—	Unused	X

PRBS_ENABLE

This bit enables the PRBS or fixed pattern monitor of the RXLI. When low, the monitor is disabled. When high the monitor is enabled and will check the incoming data stream for errors.

PRBS_FPATT

This bit determines whether the RXLI is monitoring a PRBS-23 data stream or a fixed pattern. When low, the data stream contains PRBS-23 words, and when high the fixed pattern written into the PATTERN[15:0] Register is monitored.

SYNC_STAT

The Monitor Synchronization Status bit reflects the state of the PRBS-23 data monitor's state machine. When SYNC_STAT is set low, the PRBS-23 monitor has lost synchronization. When SYNC_STAT is high, the monitor is in synchronization.

CLEAR_ERR_CNT

The Clear Error Count bit clears the PRBS word error count value. When logic 1 is written to this bit the PRBS word error count register is reset to zero. When set to logic 0 the counter operates normally. This bit should be set to logic 1 than immediately set logic 0 to perform the clear counter operation.

PRBS_ERR_CNT[7:0]

The PRBS-23 Error Count is the number of errors in the received PRBS-23 data stream detected during monitoring. Errors are accumulated only when the monitor is in the synchronized state. The PRBS-23 data is compared in 16-bit word increments and the error value represents the number of word errors detected. If there are multiple bit errors within one PRBS word, only one error is counted. The PRBS_ERR_CNT[7:0] register is cleared by writing to the CLEAR_ERR_CNT bit in Register 1104H. The error counter will not wrap around after reaching FFh, it will saturate to this value.

Register 1105H: RXLI Pattern

Bit	Type	Function	Default
Bit 15	R/W	FPATT[15]	0
Bit 14	R/W	FPATT[14]	0
Bit 13	R/W	FPATT[13]	0
Bit 12	R/W	FPATT[12]	0
Bit 11	R/W	FPATT[11]	0
Bit 10	R/W	FPATT[10]	0
Bit 9	R/W	FPATT[9]	0
Bit 8	R/W	FPATT[8]	0
Bit 7	R/W	FPATT[7]	0
Bit 6	R/W	FPATT[6]	0
Bit 5	R/W	FPATT[5]	0
Bit 4	R/W	FPATT[4]	0
Bit 3	R/W	FPATT[3]	0
Bit 2	R/W	FPATT[2]	0
Bit 1	R/W	FPATT[1]	0
Bit 0	R/W	FPATT[0]	0

FPATT[15:0]

The FPATT[15:0] provides the fixed pattern that will be monitored for when the PRBS_FPATT bit is set to a logic 1. If PRBS_FPATT is set to logic 0 this register is not used. **Note: The fixed pattern monitor does not perform a sliding window compare function. Therefore the patterns that can be detected are limited to AAAAH or 5555H, one of two and 3333H, 6666H, 9999H or CCCCH, one of four. The pattern match depends on the alignment from the CRU. As an example, if the pattern AAAAH is set in the transmitter, the software would first set the FPATT[15:0] to AAAAH. If the SYNC_STAT is set to logic one then the CRU is aligned to the data pattern. If the SYNC_STAT is set to logic 0, then the software should set the FPATT[15:0] to 5555H and recheck the SYNC_STAT bit. The procedure also applies to the 3333H, 6666H, 9999H and CCCCH pattern set, except four patterns would be used to check for SYNC_STAT.**

Register 1106H – 110FH: RXLI Reserved

Register 1110H: SRLI Clock Configuration

Bit	Type	Function	Default
Bit 15	R/W	Reserved	1
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	DISFRM	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	RCLKEN	0
Bit 0	—	Unused	X

RCLKEN

The receive clock enable (RCLKEN) bit controls the gating of the RCLK[0] output clock. When RCLKEN is set to logic 1, the RCLK[0] output clock operates normally. When RCLKEN is set to logic 0, the RCLK[0] output clock is held low. **NOTE out of spec data frequency will cause unstable clock, see section 13.2.2**

DISFRM

The disable framing (DISFRM) bit disables the framing algorithm and resets the bit alignment on the RXD[0]+/- input date to none. When DISFRM is set to logic 1, the framing algorithm is disable and the bit alignment is reset to none. When DISFRM is set to logic 0, the framing algorithm is enable and the bit alignment is done when out of frame is declared. **NOTE: under normal operating conditions this bit should not be enabled. Enabling the DISFRM when the device is in the SONET performance monitoring mode, or when the FEC decoder is enabled, will result in the corruption of the framed data. This bit has no effect if the RX_BYPASS_CH0 bit in Register 000CH is enabled.**

Register 1120H: RRMP Configuration

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	R/W	LREIBLK	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	LBIPECNTBLK	0
Bit 9	R/W	LBIPEACCBLK	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	SBIPEACCBLK	0
Bit 6	R/W	Reserved	1
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	1
Bit 3	R/W	LRDI3	0
Bit 2	R/W	LAIS3	0
Bit 1	R/W	ALGO2	0
Bit 0	W	FOOF	X

FOOF

The force out of frame (FOOF) bit forces out of frame condition. When a logic 1 is written to FOOF, the framer block is forced out of frame at the next frame boundary regardless of the framing pattern value. The OOF event initiates re-framing in the SRLI block upstream.

ALGO2

The ALGO2 bit selects the framing pattern used to determine and maintain the frame alignment. When ALGO2 is set to logic 1, the framing pattern consist of the 8 bits of the first A1 framing bytes and the first 4 bits of the last A2 framing bytes (12 bits total). This algorithm examines only 12 framing bits; all other framing bits are ignored. When ALGO2 is set to logic 0, the framing patterns consist of 12 A1 framing bytes and 12 A2 framing bytes.

LAIS3

The line alarm indication signal detection (LAIS3) bit selects the Line AIS detection algorithm. When LAIS3 is set to logic 1, Line AIS is declared when a 111 pattern is detected in bits 6,7,8 of the K2 byte for three consecutive frames. When LAIS3 is set to logic 0, Line AIS is declared when a 111 pattern is detected in bits 6,7,8 of the K2 byte for five consecutive frames.

LRDI3

The line remote defect indication detection (LRDI3) bit selects the Line RDI detection algorithm. When LRDI3 is set to logic 1, Line RDI is declared when a 110 pattern is detected in bits 6,7,8 of the K2 byte for three consecutive frames. When LRDI3 is set to logic 0, Line RDI is declared when a 110 pattern is detected in bits 6,7,8 of the K2 byte for five consecutive frames.

SBIPEACCBLK

The section BIP error accumulation block (SBIPEACCBLK) bit controls the accumulation of section BIP errors. When SBIPEACCBLK is set to logic 1, the section BIP accumulation represents BIP-8 block errors (a maximum of 1 error per frame). When SBIPEACCBLK is set to logic 0, the section BIP accumulation represents BIP-8 errors (a maximum of 8 errors per frame).

LBIPEACCBLK

The line BIP error accumulation block (LBIPEACCBLK) bit controls the accumulation of line BIP errors. When LBIPEACCBLK is set to logic 1, the line BIP accumulation represents BIP-24 block errors (a maximum of 1 error per STS-3/STM-1 per frame). When LBIPEACCBLK is set to logic 0, the line BIP accumulation represents BIP-8 errors (a maximum of 8 errors per STS-1/STM-0 per frame).

LBIPECNTBLK

The line BIP error count block (LBIPECNTBLK) bit controls the indication of line BIP errors in the SBER. When LBIPECNTBLK is set to logic 1, the SBER error rate counts represents BIP-24 block errors (a maximum of 1 error per STS-3/STM-1 per frame). When LBIPECNTBLK is set to logic 0, the SBER error rate counts represents BIP-8 errors (a maximum of 8 errors per STS-1/STM-0 per frame).

LREIBLK

The line REI block (LREIBLK) bit controls the extraction of line REI errors from the M1 byte. When LREIBLK is set to logic 1, the extracted line REI are interpreted as block BIP-24 errors (a maximum of 1 error per STS-3/STM-1 per frame). When LREIBLK is set to logic 0, the extracted line REI are interpreted as BIP-8 errors (a maximum of 8 errors per STS-1/STM-0 per frame).

BUSY

The BUSY (BUSY) bit reports the status of the transfer of section BIP, line BIP and line REI error counters to the holding registers. BUSY is set to logic 1 upon writing to the holding register addresses or by a write to the Identity and Global Performance Monitor Update Trigger Register, 0000H. BUSY is set to logic 0, upon completion of the transfer. This bit should be polled to determine when new data is available in the holding registers.

Register 1121H: RRMP Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R	APSBFV	X
Bit 4	R	LRDIV	X
Bit 3	R	LAISV	X
Bit 2	R	LOSV	X
Bit 1	R	LOFV	X
Bit 0	R	OOFV	X

OOFV

The OOFV bit reflects the current status of the out of frame defect. The OOF defect is declared when four consecutive frames have one or more bit error in their framing pattern. The OOF defect is cleared when two error free framing pattern are found.

LOFV

The LOFV bit reflects the current status of the loss of frame defect. The LOF defect is declared when an out of frame condition exists for a total period of 3 ms during which there is no continuous in frame period of 3 ms. The LOF defect is cleared when an in frame condition exists for a continuous period of 3 ms.

LOSV

The LOSV bit reflects the current status of the loss of signal defect. The LOS defect is declared when 20 µs of consecutive all zeros pattern is detected. The LOS defect is cleared when two consecutive error free framing patterns are found and during the intervening time (one frame) there is no violating period of consecutive all zeros pattern.

LAISV

The LAISV bit reflects the current status of the line alarm indication signal defect. The AIS-L defect is declared when the 111 pattern is detected in bits 6,7 and 8 of the K2 byte for three or five consecutive frames. The AIS-L defect is cleared when any pattern other than 111 is detected in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames.

LRDIV

The LRDIV bit reflects the current status of the line remote defect indication signal defect. The RDI-L defect is declared when the 110 pattern is detected in bits 6, 7, and 8 of the k2 byte for three or five consecutive frames. The RDI-L defect is cleared when any pattern other than 110 is detected in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames.

APSBFV

The APSBF bit reflects the current status of the APS byte failure defect. The APS byte failure defect is declared when no three consecutive identical K1 bytes are received in the last twelve consecutive frames starting with the last frame containing a previously consistent byte. The APS byte failure defect is cleared when three consecutive identical K1 bytes are received.

Register 1122H: RRMP Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	R/W	LREIEE	0
Bit 9	R/W	LBIPEE	0
Bit 8	R/W	SBIPEE	0
Bit 7	R/W	COSSME	0
Bit 6	R/W	COAPSE	0
Bit 5	R/W	APSBFE	0
Bit 4	R/W	LRDIE	0
Bit 3	R/W	LAISE	0
Bit 2	R/W	LOSE	0
Bit 1	R/W	LOFE	0
Bit 0	R/W	OOFE	0

OOFE, LOFE, LOSE, LAISE, LRDIE, APSBFE, COAPSE, COSSME, SBIPEE, LBIPEE, LREIEE

The interrupt enable bits controls the activation of RRMP_INT_0 bit in the Master Interrupt Status RX CH0 0002H register When the interrupt enable bit is set to logic 1, the corresponding pending interrupt will assert the RRMP_INT_0 register bit. When the interrupt enable bit is set to logic 0, the corresponding pending interrupt will not assert the RRMP_INT_0 bit.

Register 1123H: RRMP Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	R	LREIEI	X
Bit 9	R	LBIPEI	X
Bit 8	R	SBIPEI	X
Bit 7	R	COMMSI	X
Bit 6	R	COAPSI	X
Bit 5	R	APSBFI	X
Bit 4	R	LRDII	X
Bit 3	R	LAISI	X
Bit 2	R	LOSI	X
Bit 1	R	LOFI	X
Bit 0	R	OOFI	X

OOFI

The out of frame interrupt status (OOFI) bit is an event indicator. OOFI is set to logic 1 to indicate any change in the status of OOFV. The interrupt status bit is independent of the interrupt enable bit. If the WCIMODE bit in register 000BH is set to logic 1, only over-writing with a '1' clears this bit. If the WCIMODE bit is set to logic 0 than a read of this register automatically clears the bit.

LOFI

The loss of frame interrupt status (LOFI) bit is an event indicator. LOFI is set to logic 1 to indicate any change in the status of LOFV. The interrupt status bit is independent of the interrupt enable bit. LOFI is cleared to logic 0 when this register is read. If the WCIMODE bit in register 000BH is set to logic 1, only over-writing with a '1' clears this bit. If the WCIMODE bit is set to logic 0 than a read of this register automatically clears the bit.

LOSI

The loss of signal interrupt status (LOSI) bit is an event indicator. LOSI is set to logic 1 to indicate any change in the status of LOSV. The interrupt status bit is independent of the interrupt enable bit. If the WCIMODE bit in register 000BH is set to logic 1, only over-writing with a '1' clears this bit. If the WCIMODE bit is set to logic 0 than a read of this register automatically clears the bit.

LAISI

The line alarm indication signal interrupt status (LAISI) bit is an event indicator. LAISI is set to logic 1 to indicate any change in the status of LAISV. The interrupt status bit is independent of the interrupt enable bit. If the WCIMODE bit in register 000BH is set to logic 1, only over-writing with a ‘1’ clears this bit. If the WCIMODE bit is set to logic 0 than a read of this register automatically clears the bit.

LRDII

The line remote defect indication interrupt status (LRDII) bit is an event indicator. LRDII is set to logic 1 to indicate any change in the status of LRDIV. The interrupt status bit is independent of the interrupt enable bit. If the WCIMODE bit in register 000BH is set to logic 1, only over-writing with a ‘1’ clears this bit. If the WCIMODE bit is set to logic 0 than a read of this register automatically clears the bit.

APSBFI

The APS byte failure interrupt status (APSBFI) bit is an event indicator. APSBFI is set to logic 1 to indicate any change in the status of APSBFV. The interrupt status bit is independent of the interrupt enable bit. If the WCIMODE bit in register 000BH is set to logic 1, only over-writing with a ‘1’ clears this bit. If the WCIMODE bit is set to logic 0 than a read of this register automatically clears the bit.

COAPSI

The change of APS bytes interrupt status (COAPSI) bit is an event indicator. COAPSI is set to logic 1 to indicate a new APS bytes. The interrupt status bit is independent of the interrupt enable bit. If the WCIMODE bit in register 000BH is set to logic 1, only over-writing with a ‘1’ clears this bit. If the WCIMODE bit is set to logic 0 than a read of this register automatically clears the bit.

COSSMI

The change of SSM message interrupt status (COSSMI) bit is an event indicator. COSSMI is set to logic 1 to indicate a new SSM message. The interrupt status bit is independent of the interrupt enable bit. If the WCIMODE bit in register 000BH is set to logic 1, only over-writing with a ‘1’ clears this bit. If the WCIMODE bit is set to logic 0 than a read of this register automatically clears the bit.

SBIPEI

The section BIP error interrupt status (SBIPEI) bit is an event indicator. SBIPEI is set to logic 1 to indicate a section BIP error. The interrupt status bit is independent of the interrupt enable bit. If the WCIMODE bit in register 000BH is set to logic 1, only over-writing with a '1' clears this bit. If the WCIMODE bit is set to logic 0 than a read of this register automatically clears the bit.

LBIPEI

The line BIP error interrupt status (LBIPEI) bit is an event indicator. LBIPEI is set to logic 1 to indicate a line BIP error. The interrupt status bit is independent of the interrupt enable bit. If the WCIMODE bit in register 000BH is set to logic 1, only over-writing with a '1' clears this bit. If the WCIMODE bit is set to logic 0 than a read of this register automatically clears the bit.

LREIEI

The line REI error interrupt status (LREIEI) bit is an event indicator. LREIEI is set to logic 1 to indicate a line REI error. The interrupt status bit is independent of the interrupt enable bit. If the WCIMODE bit in register 000BH is set to logic 1, only over-writing with a '1' clears this bit. If the WCIMODE bit is set to logic 0 than a read of this register automatically clears the bit.

Register 1124H: RRMP Receive APS

Bit	Type	Function	Default
Bit 15	R	K1V[7]	X
Bit 14	R	K1V[6]	X
Bit 13	R	K1V[5]	X
Bit 12	R	K1V[4]	X
Bit 11	R	K1V[3]	X
Bit 10	R	K1V[2]	X
Bit 9	R	K1V[1]	X
Bit 8	R	K1V[0]	X
Bit 7	R	K2V[7]	X
Bit 6	R	K2V[6]	X
Bit 5	R	K2V[5]	X
Bit 4	R	K2V[4]	X
Bit 3	R	K2V[3]	X
Bit 2	R	K2V[2]	X
Bit 1	R	K2V[1]	X
Bit 0	R	K2V[0]	X

K1V[7:0]/K2V[7:0]

The APS K1/K2 bytes value (K1V[7:0]/K2V[7:0]) bits represent the extracted K1/K2 APS bytes. K1V/K2V is updated when the same K1 and K2 bytes (forming a single entity) are received for three consecutive frames.

Register 1125H: RRMP Receive SSM

Bit	Type	Function	Default
Bit 15	R/W	BYTESSM	0
Bit 14	R/W	FLTRSSM	0
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	R	SSMV[7]	X
Bit 6	R	SSMV[6]	X
Bit 5	R	SSMV[5]	X
Bit 4	R	SSMV[4]	X
Bit 3	R	SSMV[3]	X
Bit 2	R	SSMV[2]	X
Bit 1	R	SSMV[1]	X
Bit 0	R	SSMV[0]	X

SSMV[7:0]

The synchronization status message value (SSMV[7:0]) bits represent the extracted S1 nibble (or byte). When filtering is enabled via the FLTRSSM register bit, SSMV is updated when the same S1 nibble (or byte) is received for eight consecutive frames. When filtering is disable, SSMV is updated every frame.

FLTRSSM

The filter synchronization status message (FLTRSSM) bit enables the filtering of the SSM nibble (or byte). When FLTRSSM is set to logic 1, the SSM value is updated when the same SSM is received for eight consecutive frames. When FLTRSSM is set to logic 0, the SSM value is updated every frame.

BYTESSM

The byte synchronization status message (BYTESSM) bit extends the SSM from a nibble to a byte. When BYTESSM is set to logic 1, the SSM is a byte and bits 1 to 8 of the S1 byte are considered. When BYTESSM is set to logic 0, the SSM is a nibble and only bits 5 to 8 of the S1 byte are considered.

Register 1126H: RRMP AIS Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	R/W	K2AIS	0
Bit 3	R/W	RLAISINS	0
Bit 2	R/W	RLAISEN	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

RLAISEN

The receive line AIS enable (RLAISEN) bit enables line AIS insertion in the outgoing data stream. When RLAISEN is set to logic 1, line AIS is inserted in the outgoing data stream when an LOF or LOS condition exists or when the incoming K2 byte indicates AIS. When RLAISEN is set to logic 0, no line AIS is inserted regardless of the alarm condition.

This bit should be set to logic 1 for normal operation.

RLAISINS

The receive line AIS insertion (RLAISIN) bit forces line AIS insertion in the receive SONET data stream. When RLAISINS is set to logic 1, all ones are inserted in the line overhead bytes and in the payload bytes (all the bytes of the frame except the section overhead bytes) to force a line AIS condition. When RLAISINS is set to logic 0, the line AIS condition is removed. **Note: In order to have the entire frame covered by the ones insertion the RLAISINS bit in registers 1136H, 1146H and 1156H must be set to the same value.**

K2AIS

The K2 line AIS (K2AIS) bit restricts line AIS to the K2 byte. When K2AIS is set to logic 1, line AIS is only inserted in bits 6, 7 and 8 of the K2 byte. When K2AIS is set to logic 0, line AIS is inserted in the line overhead bytes and in the payload bytes (all the bytes of the frame except the section overhead bytes).

Register 1127H: RRMP Section BIP Error Counter

Bit	Type	Function	Default
Bit 15	R	SBIPE[15]	X
Bit 14	R	SBIPE[14]	X
Bit 13	R	SBIPE[13]	X
Bit 12	R	SBIPE[12]	X
Bit 11	R	SBIPE[11]	X
Bit 10	R	SBIPE[10]	X
Bit 9	R	SBIPE[9]	X
Bit 8	R	SBIPE[8]	X
Bit 7	R	SBIPE[7]	X
Bit 6	R	SBIPE[6]	X
Bit 5	R	SBIPE[5]	X
Bit 4	R	SBIPE[4]	X
Bit 3	R	SBIPE[3]	X
Bit 2	R	SBIPE[2]	X
Bit 1	R	SBIPE[1]	X
Bit 0	R	SBIPE[0]	X

SBIPE[15:0]

The section BIP error (SBIPE[15:0]) bits represent the number of section BIP errors that have been detected since the last accumulation interval. The error counter is transferred to the holding registers by a microprocessor write to any of the RRMP counter registers or the CRSU 4x2488 Identity, and Global Performance Monitor Update register.

Register 1128H: RRMP Line BIP Error Counter (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R	LBIPE[15:0]	XXXX

Register 1129H: RRMP Line BIP Error Counter (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 8		Unused	
Bit 7 to Bit 0	R	LBIPE[23:16]	XX

LBIPE[23:0]

The line BIP error (LBIPE[23:0]) bits represent the number of line BIP errors that have been detected since the last accumulation interval. The error counter is transferred to the holding registers by a microprocessor write to any of the RRMP counter registers or the CRSU 4x2488 Identity, and Global Performance Monitor Update register.

Register 112AH: RRMP Line REI Error Counter (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R	LREIE[15:0]	XXXX

Register 112BH: RRMP Line REI Error Counter (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 8		Unused	
Bit 7 to Bit 0	R	LREIE[23:16]	XX

LREIE[23:0]

The line REI error (LREIE[23:0]) bits represent the number of line REI errors that have been detected since the last accumulation interval. The error counter is transferred to the holding registers by a microprocessor write to any of the RRMP counter registers or the CRSU 4x2488 Identity, and Global Performance Monitor Update register.

Register 1136H: RRMP AIS Enable 2 (Slave)

Register 1146H: RRMP AIS Enable 3 (Slave)

Register 1156H: RRMP AIS Enable 4 (Slave)

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	R/W	Reserved	0
Bit 3	R/W	RLAISINS	0
Bit 2	R/W	RLAISEN	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

RLAISEN

The receive line AIS enable (RLAISEN) bit enables line AIS insertion in the outgoing data stream. When RLAISEN is set to logic 1, line AIS is inserted in the outgoing data stream when a LOF or LOS condition exists or when the incoming K2 byte indicates AIS. When RLAISEN is set to logic 0, no line AIS is inserted regardless of the alarm condition.

This bit should be set to logic 1 for normal operation.

RLAISINS

The receive line AIS insertion (RLAISIN) bit forces line AIS insertion in the receive SONET data stream. When RLAISINS is set to logic 1, all ones are inserted in the line overhead bytes and in the payload bytes (all the bytes of the frame except the section overhead bytes) to force a line AIS condition. When RLAISINS is set to logic 0, the line AIS condition is removed. **Note: In order to have the entire frame covered by the ones insertion the RLAISINS bit in register 1126H must be set to the same value.**

Register 1160H: RIFD Configuration

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R/W	HS_EN	1
Bit 4	R/W	Reserved	0
Bit 3	R/W	BIP_BLK_EN	0
Bit 2	R/W	BIP_PRE_FEC	0
Bit 1	R/W	FEC_ENABLE	0
Bit 0	R/W	FEC_NO_DELAY	0

FEC_NO_DELAY

The FEC no delay (FEC_NO_DELAY) bit controls whether decoder delay should be added to the data when FEC_ENABLE is 0. If FEC_NO_DELAY is set to logic 0, the decoder delay that is normally incurred for FEC decoding is added to the data even though the data is unchanged. If FEC_NO_DELAY is set to logic 1, the decoder delay is not added to the data. NOTE: Under normal operation the FEC_NO_DELAY should be set to logic 0, delay added. By enabling the delay the downstream device will not see and discontinuity in the data due to the FEC_ENABLE bit being changed.

FEC_ENABLE

The FEC enable (FEC_ENABLE) bit controls whether to enable the normal FEC function or to disable it. If FEC_ENABLE is set to logic 1, the FEC function is enabled, and FEC decoding is controlled by the FEC Status Indication (FSI) bits in the SONET/SDH frame. If FEC_ENABLE is set to logic 0, FEC decoding is disabled regardless of the FSI extracted from the frame.

BIP_PRE_FEC

The BIP pre-FEC error report (BIP_PRE_FEC) bit controls whether the BIP should be calculated on the pre-decoded data stream or the post-decoded data stream. If BIP_PRE_FEC is set to logic 1, BIP codes are calculated and compared with B2 on the pre-decoded data. If BIP_PRE_FEC is set to logic 0, BIP codes are calculated and compared with B2 on the post-decoded data. If this bit is changed, the user should also clear the internal BIP error count because the counter contains error count remnants of the previous mode. The internal BIP error count can be cleared by performing a write operation to holding register addresses (1164H, 1165H, 1166H, or 1167H) or by reading the Identity and Global Performance Monitor Update Register 0000H.

BIP_BLK_EN

The BIP block enable (BIP_BLK_EN) bit controls whether the BIP error counter and the BIP count used by the SBER, reports BIP-8 or block BIP-24 errors. If BIP_BLK_EN is set to logic 1, block BIP-24 errors are reported. If it is set to 0, BIP-8 errors are reported. If this bit is changed, the user should also clear the internal BIP error count because the counter contains error count remnants of the previous mode. The internal BIP error count can be cleared by performing a write operation to any of the count holding registers (1164H, 1165H, 1166H, or 1167H) or by reading the Identity and Global Performance Monitor Update Register 0000H.

HS_EN

The handshake enable (HS_EN) bit controls whether the decode function is enabled based on received FSI bits in the SONET/SDH frame or to put the RIFD into test mode by enabling the decode function regardless of the FSI bits received. (The name “handshake enable” is really a misnomer since no handshaking really takes place at all; the transmitter is always the master, and the receiver is always the slave with unidirectional communication only).

When it is set to logic 1, the RIFD enables and disables the decode function normally via FSI. If this bit is set to 0, the RIFD enables the decode function regardless of FSI. Setting this bit to 0 speeds up decode cycle by eliminating the time needed for the 9 consecutive frames to turn the decode function on.

BUSY

The BUSY (BUSY) bit reports the status of the transfer of error counters to the Count holding registers. BUSY is set to logic 1 upon writing to any of the RIFD Count holding registers (1164H, 1165H, 1166H, or 1167H) or by reading the Identity and Global Performance Monitor Update Register 0000H. BUSY is set to logic 0, upon completion of the transfer. This bit should be polled to determine when new data is available in the holding registers.

Register 1161H: RIFD Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	R	FSI_DEC_ON	X

FSI_DEC_ON

The FSI decode on (FSI_DEC_ON) bit reports whether the decode function is enabled or disabled due to the FSI bits extracted from the frame. FSI_DEC_ON is set to logic 1 when the FSI bits extracted from the SONET/SDH frame, after filtering, indicate that the RIFD should decode the data stream. It is set to 0 when the filtered FSI bits indicate that the RIFD should not decode the data stream. This register bit is independent of the global enable/disable control register bit FEC_ENABLE.If register bit HS_EN is set to 0 it has the same effect as receiving nine cumulative FSI bits of 01. Therefore, setting HS_EN to 0 also sets FSI_DEC_ON to 1.

Register 1162H: RIFD Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	R/W	BIPCNT_INT_EN	0
Bit 1	R/W	CORRCNT_INT_EN	0
Bit 0	R/W	FSI_INT_EN	0

FSI_INT_EN

The FSI interrupt enable (FSI_INT_EN) bit controls the activation of the RIFD_INT_0 interrupt bit in the Master Interrupt Status RX CH0 register, 0002H, for decode on/off changes due to FSI. If FSI_INT_EN is 1, the RIFD_INT_0 bit is asserted when the cumulative received FSI bits indicate that the decoder should change its state from decode-on to decode-off or from decode-off to decode-on. The state transition from decode-on to decode-off is made when 3 consecutive FSI bits of 00 is received when the previous state is decode-on; the RIFD_INT_0 is asserted after the receipt of the 3rd FSI of 00. The state transition from decode-off to decode-on is made when 9 consecutive FSI bits of 01 is received when previous state is decode-off; the RIFD_INT_0 is asserted after the receipt of the 9th FSI of 01. If FSI_INT_EN is 0, a pending FSI transition interrupt will not assert RIFD_INT_0.

CORRCNT_INT_EN

The corrected bit error counter interrupt enable (CORRCNT_INT_EN) bit controls the activation of the RIFD_INT_0 interrupt bit in the Master Interrupt Status RX CH0 register, 0002H, when a bit error correction takes place. When CORRCNT_INT_EN is 1, a pending bit correction error interrupt will assert the RIFD_INT_0 bit. The RIFD_INT_0 bit is asserted even when the correction counter saturates. If CORRCNT_INT_EN is 0, a pending correction error interrupt will not assert RIFD_INT_0.

BIPCNT_INT_EN

The BIP counter interrupt enable (BIPCNT_INT_EN) bit controls the activation of the RIFD_INT_0 interrupt bit in the Master Interrupt Status RX CH0 register, 0002H, when a BIP error is detected. When BIPCNT_INT_EN is 1, a pending BIP error interrupt will assert the RIFD_INT_0 bit. The RIFD_INT_0 bit is asserted even when the BIP error counter saturates. If BIPCNT_INT_EN is 0, a pending BIP error interrupt will not assert RIFD_INT_0.

Register 1163H: RIFD Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	R	BIPCNT_STATUS	X
Bit 1	R	CORRCNT_STATUS	X
Bit 0	R	FSI_STATUS	X

FSI_STATUS

The FSI interrupt status (FSI_STATUS) bit is an event indicator. FSI_STATUS is set to logic 1 to indicate a transition in the state of the decode function (decode-on to decode-off, or decode-off to decode-on). The interrupt status bit is independent of the interrupt enable bit. If the WCIMODE bit in register 000BH is set to logic 1, only over-writing with a '1' clears this bit. If the WCIMODE bit is set to logic 0 than a read of this register automatically clears the bit.

CORRCNT_STATUS

The corrected bit error count status (CORRCNT_STATUS) bit is an event indicator. CORRCNT_STATUS is set to logic 1 to indicate that a bit correction has occurred. The interrupt status bit is independent of the interrupt enable bit. If the WCIMODE bit in register 000BH is set to logic 1, only over-writing with a '1' clears this bit. If the WCIMODE bit is set to logic 0 than a read of this register automatically clears the bit.

BIPCNT_STATUS

The BIP count error status (BIPCNT_STATUS) bit is an event indicator. BIPCNT_STATUS is set to logic 1 to indicate that a BIP error has been detected. The interrupt status bit is independent of the interrupt enable bit. If the WCIMODE bit in register 000BH is set to logic 1, only over-writing with a '1' clears this bit. If the WCIMODE bit is set to logic 0 than a read of this register automatically clears the bit.

Register1164H: RIFD correctable error count LSB

Bit	Type	Function	Default
Bit 15	R	CORRCNT [15]	X
Bit 14	R	CORRCNT[14]	X
Bit 13	R	CORRCNT[13]	X
Bit 12	R	CORRCNT[12]	X
Bit 11	R	CORRCNT[11]	X
Bit 10	R	CORRCNT[10]	X
Bit 9	R	CORRCNT[9]	X
Bit 8	R	CORRCNT[8]	X
Bit 7	R	CORRCNT[7]	X
Bit 6	R	CORRCNT[6]	X
Bit 5	R	CORRCNT[5]	X
Bit 4	R	CORRCNT[4]	X
Bit 3	R	CORRCNT[3]	X
Bit 2	R	CORRCNT[2]	X
Bit 1	R	CORRCNT[1]	X
Bit 0	R	CORRCNT[0]	X

CORRCNT[15:0]

The correctable error count register (CORRCNT[20:0]) bits represent the number of correctable bit errors that have been detected since the last accumulation interval. The error count is transferred to the holding register by a write to any of the count holding registers, 1164H to 1167H, or by reading the Identity and Global Performance Monitor Update Register 0000H. The TIP bit in Register 0000H indicates the status of the transfer to this register. This register is not updated if FEC is disabled with the FEC_ENABLE register bit, the FSI protocol, or the ALARM input.

Register 1165H: RIFD correctable error count MSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	R	CORRCNT[20]	X
Bit 3	R	CORRCNT[19]	X
Bit 2	R	CORRCNT[18]	X
Bit 1	R	CORRCNT[17]	X
Bit 0	R	CORRCNT[16]	X

CORRCNT[20:16]

The correctable error count register (CORRCNT[20:0]) bits represent the number of correctable bit errors that have been detected since the last accumulation interval. The error count is transferred to the holding register by a write to any of the count holding registers, 1164H to 1167H, or by reading the Identity and Global Performance Monitor Update Register 0000H.The TIP bit in Register 0000H indicates the status of the transfer to this register. This register is not updated if FEC is disabled with the FEC_ENABLE register bit, the FSI protocol, or the ALARM input.

Register 1166H: RIFD line BIP error count LSB

Bit	Type	Function	Default
Bit 15	R	BIPECNT[15]	X
Bit 14	R	BIPECNT[14]	X
Bit 13	R	BIPECNT[13]	X
Bit 12	R	BIPECNT[12]	X
Bit 11	R	BIPECNT[11]	X
Bit 10	R	BIPECNT[10]	X
Bit 9	R	BIPECNT[9]	X
Bit 8	R	BIPECNT[8]	X
Bit 7	R	BIPECNT[7]	X
Bit 6	R	BIPECNT[6]	X
Bit 5	R	BIPECNT[5]	X
Bit 4	R	BIPECNT[4]	X
Bit 3	R	BIPECNT[3]	X
Bit 2	R	BIPECNT[2]	X
Bit 1	R	BIPECNT[1]	X
Bit 0	R	BIPECNT[0]	X

BIPECNT[15:0]

The line BIP error count register (BIPECNT[21:0]) bits represent the number of line BIP errors that have been detected since the last accumulation interval. The error count is transferred to the holding register by a write to any of the count holding registers, 1164H to 1167H, or by reading the Identity and Global Performance Monitor Update Register 0000H. The TIP bit in Register 0000H indicates the status of the transfer to this register.

Register 1167H: RIFD line BIP error count MSB

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R	BIPECNT[21]	X
Bit 4	R	BIPECNT[20]	X
Bit 3	R	BIPECNT[19]	X
Bit 2	R	BIPECNT[18]	X
Bit 1	R	BIPECNT[17]	X
Bit 0	R	BIPECNT[16]	X

BIPECNT[21:16]

The line BIP error count register (BIPECNT[21:0]) bits represent the number of line BIP errors that have been detected since the last accumulation interval. The error count is transferred to the holding register by a write to any of the count holding registers, 1164H to 1167H, or by reading the Identity and Global Performance Monitor Update Register 0000H. The TIP bit in Register 0000H indicates the status of the transfer to this register.

Register 1180H: SBER Configuration

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R/W	SFBERTEN	0
Bit 4	R/W	SFSMODE	0
Bit 3	R/W	SFCMODE	0
Bit 2	R/W	SDBERTEN	0
Bit 1	R/W	SDSMODE	0
Bit 0	R/W	SDCMODE	0

SDCMODE

The SDCMODE alarm bit selects the Signal Degrade BERM window size to use for clearing alarms. When SDCMODE is a logic 0 the SD BERM will clear an alarm using the same window size used for declaration. When SDCMODE is a logic 1 the SD BERM will clear an alarm using a window size that is 8 times longer than alarm declaration window size. The declaration window size is defined by the SBER SD BERM Accumulation Period register.

SDSMODE

The SDSMODE bit selects the Signal Degrade BERM saturation mode. When SDSMODE is a logic 0 the SD BERM will saturate the BIP count on a per frame basis using the SBER SD Saturation Threshold register value. When SDSMODE is a logic 1 the SD BERM will saturate the BIP count on a per window subtotals accumulation period basis using the SBER SD Saturation Threshold register value.

SDBERTEN

The SDBERTEN bit enables automatic monitoring of line bit error rate threshold events by the Signal Degrade BERM. When SDBERTEN is a logic one, the SD BERM continuously monitors line BIP errors over a period defined in the BERM configuration registers. When SDBERTEN is a logic zero, the SD BERM BIP accumulation logic is disabled, and the BERM logic is reset to restart in the declaration monitoring state.

All SD BERM configuration registers should be set up before the monitoring is enabled.

SFCMODE

The SFCMODE alarm bit selects the Signal Failure BERM window size to use for clearing alarms. When SFCMODE is a logic 0 the SF BERM will clear an alarm using the same window size used for declaration. When SFCMODE is a logic 1 the SF BERM will clear an alarm using a window size that is 8 times longer than alarm declaration window size. The declaration window size is defined by the SBER SF BERM Accumulation Period register.

SFSMODE

The SFSMODE bit selects the Signal Failure BERM saturation mode. When SFSMODE is a logic 0 the SF BERM will saturate the BIP count on a per frame basis using the SBER SF Saturation Threshold register value. When SFSMODE is a logic 1 the SF BERM will saturate the BIP count on a per window subtotals accumulation period basis using the SBER SD Saturation Threshold register value.

SFBERTEN

The SFBERTEN bit enables automatic monitoring of line bit error rate threshold events by the Signal Failure BERM. When SFBERTEN is a logic one, the SF BERM continuously monitors line BIP errors over a period defined in the BERM configuration registers. When SFBERTEN is a logic zero, the SF BERM BIP accumulation logic is disabled, and the BERM logic is reset to restart in the declaration monitoring state.

All SF BERM configuration registers should be set up before the monitoring is enabled.

Register 1181H: SBER Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	R	SFBERV	X
Bit 0	R	SDBERV	X

SDBERV

The SDBERV bit indicates the Signal Failure BERM alarm state. The alarm is declared (SDBERV is a logic one) when the declaring threshold has been exceeded. The alarm is removed (SDBERV is a logic zero) when the clearing threshold has been reached.

SFBERV

The SFBERV bit indicates the Signal Failure BERM alarm state. The alarm is declared (SFBERV is a logic one) when the declaring threshold has been exceeded. The alarm is removed (SFBERV is a logic zero) when the clearing threshold has been reached.

Register 1182H: SBER Interrupt Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	R/W	SFBERE	0
Bit 0	R/W	SDBERE	0

SDBERE

The SDBERE bit is the interrupt enable for the SDBER alarm. When SDBERE set to logic 1, the pending interrupt in the SBER Interrupt Status register, SDBERI, will assert the SBER_INT_0 bit in the Master Interrupt Status RX CH0 0002H register. When SDBERE is set to logic 0, the pending interrupt will not assert the SBER_INT_0 bit.

SFBERE

The SFBERE bit is the interrupt enable for the SFBER alarm. When SFBERE set to logic 1, the pending interrupt in the SBER Interrupt Status Register, SFBERI, will assert the SBER_INT_0 bit in the Master Interrupt Status RX CH0 0002H register. When SFBERE is set to logic 0, the pending interrupt will not assert the SBER_INT_0 bit.

Register 1183H: SBER Interrupt Status

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	R	SFBERI	X
Bit 0	R	SDBERI	X

SDBERI

The SDBERI bit is an event indicator set to logic 1 to indicate any changes in the status of SDBERV. This interrupt status bit is independent of the SDBERE interrupt enable bits. The SDBERI bit is cleared to logic 0 when the SBER Interrupt Status register is read.

SFBERI

The SFBERI bit is an event indicator set to logic 1 to indicate any changes in the status of SFBERV. This interrupt status bit is independent of the SFBERE interrupt enable bits. The SFBERI bit is cleared to logic 0 when the SBER Interrupt Status register is read.

Register 1184H: SBER SF BERM Accumulation Period (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SFSAP[15:0]	0000

Register 1185H: SBER SF BERM Accumulation Period (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SFSAP[31:16]	0000

SFSAP[31:0]

The SFSAP[31:0] bits represent the number of STS-N frames to be used to accumulate a BIP error subtotal. The total evaluation window to declare an alarm is broken into 8 subtotals, so this register value represents 1/8 of the total sliding window size. Refer to the Operations section for the recommended settings.

Register 1186H: SBER SF BERM Saturation Threshold (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SFSATH[15:0]	FFFF

Register 1187H: SBER SF BERM Saturation Threshold (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SFSATH[23:16]	XXFF

SFSATH[23:0]

The SFSTH[23:0] bits represent the allowable number of BIP errors that can be accumulated during a BIP accumulation period before a BER threshold event is asserted. Setting this threshold to 0xFFFFFF disables the saturation functionality. Refer to the Operations section for the recommended settings.

Register 1188H: SBER SF BERM Declaring Threshold (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SFDECTH[15:0]	0000

Register 1189H: SBER SF BERM Declaring Threshold (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SFDECTH[23:16]	XX00

SFDECTH[23:0]

The SFDECTH[23:0] register represent the number of BIP errors that must be accumulated during a full evaluation window in order to declare a BER alarm. Refer to the Operations section for the recommended settings.

Register 118AH: SBER SF BERM Clearing Threshold (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SFCLRTH[15:0]	0000

Register 118BH: SBER SF BERM Clearing Threshold (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SFCLRTH[23:16]	XX00

SFCLRTH[23:0]

The SFCLRTH[23:0] register represent the number of BIP errors that can be accumulated but not exceeded during a full evaluation window in order to clear a BER alarm. Refer to the Operations section for the recommended settings.

Register 118CH: SBER SD BERM Accumulation Period (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SDSAP[15:0]	0000

Register 118DH: SBER SD BERM Accumulation Period (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SDSAP[31:16]	0000

SDSAP[31:0]

The SDSAP[31:0] bits represent the number of STS-N frames to be used to accumulate a BIP error subtotal. The total evaluation window to declare an alarm is broken into 8 subtotals, so this register value represents 1/8 of the total sliding window size. Refer to the Operations section for the recommended settings.

Register 118EH: SBER SD BERM Saturation Threshold (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SDSATH[15:0]	FFFF

Register 118FH: SBER SD BERM Saturation Threshold (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SDSATH[23:16]	XXFF

SDSATH[23:0]

The SDSATH[23:0] bits represent the allowable number of BIP errors that can be accumulated during a BIP accumulation period before a BER threshold event is asserted. Setting this threshold to 0xFFFFFFFF disables the saturation functionality. Refer to the Operations section for the recommended settings.

Register 1190H: SBER SD BERM Declaration Threshold (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SDDECTH[15:0]	0000

Register 1191H: SBER SD BERM Declaration Threshold (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SDDECTH[23:16]	XX00

SDDECTH[23:0]

The SDDECTH[23:0] register represent the number of BIP errors that must be accumulated during a full evaluation window in order to declare a BER alarm. Refer to the Operations section for the recommended settings.

Register 1192H: SBER SD BERM Clearing Threshold (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SDCLRTH[15:0]	0000

Register 1193H: SBER SD BERM Clearing Threshold (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SDCLRTH[23:16]	XX00

SDCLRTH[23:0]

The SDCLRTH[23:0] register represent the number of BIP errors that can be accumulated but not exceeded during a full evaluation window in order to clear a BER alarm. Refer to the Operations section for the recommended settings.

Register 1194-11FFH: Unused

12 Test Features Description

Simultaneously asserting (low) the CSB, RDB and WRB inputs causes all digital output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the CRSU 4x2488. Test mode registers (as opposed to normal mode registers) are selected when TRS (A[13]) is high.

Test mode registers may also be used for board testing. When all of the TSBs within the CRSU 4x2488 are placed in test mode 0, device inputs may be read and device outputs may be forced via the microprocessor interface (refer to the section "Test Mode 0" for details).

In addition, the CRSU 4x2488 also supports a standard IEEE 1149.1 five-signal JTAG boundary scan test port for use in board testing. All digital device inputs may be read and all digital device outputs may be forced via the JTAG test port. For further information on the JTAG test port se section 12.2 JTAG Test Port.

Table 11 Test Mode Register Memory Map

Address	Register
0000H-1FFFH	Normal Mode Registers
2000	Master Test Register
2001	Test Mode Address Force Enable
2002	Test Mode Address Force Value
2003	Reserved
2004-3FFF	Reserved For Test

12.1 Master Test and Test Configuration Registers

Notes on Test Mode Register Bits

1. Writing values into Unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, Unused register bits must be written with logic zero. Reading back Unused bits can produce either a logic one or a logic zero; hence, Unused register bits should be masked off by software when read.
2. Writable test mode register bits are not initialized upon reset unless otherwise noted.

Register 2000H: CRSU 4x2488 Master Test

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	W	PMCATST	0
Bit 4	W	PMCTST	0
Bit 3	W	DBCTRL	0
Bit 2	W	Reserved	0
Bit 1	W	HIZDATA	0
Bit 0	R/W	HIZIO	0

This register is used to enable CRSU 4x2488 test features. All bits, except PMCTST, PMCATST and BYPASS are reset to zero by a reset of the CRSU 4x2488 using the RSTB input. PMCTST, PMCATST, and BYPASS are reset when CSB is logic 1. PMCTST, and PMCATST can also be reset by writing a logic 0 to the corresponding register bit.

Both PMCATST and PMCTST (bit 4 and 5) in this register must be set to high for OC48 line side analog test.

Access to this register is not affected by the Test Mode Address Force functions in registers 2001H and 2002H.

HIZIO, HIZDATA

The HIZIO and HIZDATA bits control the tri-state modes of the CRSU-4X2488 . While the HIZIO bit is a logic one, all output pins of the CRSU-4X2488 except the data bus and output TDO are held tri-state. The microprocessor interface is still active. While the HIZDATA bit is a logic one, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles. The HIZDATA bit is overridden by the DBCTRL bit.

DBCTRL

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin. When the DBCTRL bit is set to logic one and IOTST is set to logic one, the CSB pin controls the output enable for the data bus. While the DBCTRL bit is set, holding the CSB pin high causes the CRSU-4X2488 to drive the data bus and holding the CSB pin low tri-states the data bus. The DBCTRL bit overrides the HIZDATA bit. The DBCTRL bit is used to measure the drive capability of the data bus driver pads.

PMCTST

The PMCTST bit is used to configure the CRSU-4X2488 for manufacturing tests. When PMCTST is set to logic one, the CRSU-4X2488 microprocessor port becomes the test access port used to run the PMC "canned" manufacturing test vectors, and all analog blocks are forced into IDDQ mode. The PMCTST can be cleared by setting CSB to logic one or by writing logic zero to the bit. Both PMCATST and PMCTST (bit 4 and 5) in this register must be set to high for OC48 line side analog test.

PMCATST

The PMCATST bit is used to configure the analog portion of the CRSU-4X2488 for manufacturing tests. The PMCATST can be cleared by setting CSB to logic one or by writing logic zero to the bit. Both PMCATST and PMCTST (bit 4 and 5) in this register must be set to high for OC48 line side analog test.

Register 2001H: CRSU-4X2488 Test Mode Address Force Enable

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	——	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	TM_A_EN[12]	0
Bit 10	R/W	TM_A_EN[11]	0
Bit 9	R/W	TM_A_EN[10]	0
Bit 8	R/W	TM_A_EN[9]	0
Bit 7	R/W	TM_A_EN[8]	0
Bit 6	R/W	TM_A_EN[7]	0
Bit 5	R/W	TM_A_EN[6]	0
Bit 4	R/W	TM_A_EN[5]	0
Bit 3	R/W	TM_A_EN[4]	0
Bit 1	R/W	TM_A_EN[3]	0
Bit 1	R/W	TM_A_EN[2]	0
Bit 0	R/W	TM_A_EN[1]	0

This register is used to force the address pins to a certain value. These bits are valid when either PMCTST or PMCATST is set to logic 1. The TM_A[X] bit is forced when TM_A_EN[X] is logic 1. Otherwise, the A[X] pin is used.

Access to this register is not affected by the Test Mode Address Force functions in registers 2001H and 2002H.

TM_A_EN[12:1]

When TM_A_EN[X] is logic 1 and either PMCTST or PMCATST is logic 1, the TM_A[X] register bit replaces the input pin A[X]. Like PMCTST and PMCATST, TM_A_EN[12:2] bits are cleared only when CSB is logic 1 or when they are written to logic 0.

Register 2002H: CRSU-4X2488Test Mode Address Force Value

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	R/W	TM_A[12]	0
Bit 10	R/W	TM_A[11]	0
Bit 9	R/W	TM_A[10]	0
Bit 8	R/W	TM_A[9]	0
Bit 7	R/W	TM_A[8]	0
Bit 6	R/W	TM_A[7]	0
Bit 5	R/W	TM_A[6]	0
Bit 4	R/W	TM_A[5]	0
Bit 3	R/W	TM_A[4]	0
Bit 1	R/W	TM_A[3]	0
Bit 1	R/W	TM_A[2]	0
Bit 0	R/W	TM_A[1]	0

This register is used to force the address pins to a certain value. These bits are valid when either PMCTST or PMCATST is set to logic 1. The TM_A[X] bit is forced when TM_A_EN[X] is logic 1. Otherwise, the A[X] pin is used.

Access to this register is not affected by the Test Mode Address Force functions in registers 2001H and 2002H.

TM_A[12:1]

When TM_A_EN[X] is logic 1 and either PMCTST or PMCATST is logic 1, the TM_A[X] bit replaces the input pin A[X]. The TM_A[X] bits are not cleared on reset.

Register 2003H: CRSU-4X2488 Reserved Test Register

Bit	Type	Function	Default
Bit 15	—	Unused	X
Bit 14	—	Unused	X
Bit 13	—	Unused	X
Bit 12	—	Unused	X
Bit 11	—	Unused	X
Bit 10	—	Unused	X
Bit 9	—	Unused	X
Bit 8	—	Unused	X
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	R/W	QSFI-4_IDDQ	0

QSFI-4_IDDQ

The QSFI-4_IDDQ bit activates the IDDQ (Quiescent Current) test mode in the QSFI-4 ABC. When set to '1' all Analog Circuits in the QSFI-4M mega ABC are disabled and the IDDQ of the digital circuits can be measured. When this bit is set to '0' all analog circuits operate normally. This bit is only used during production testing.

12.2 JTAG Test Port

The CRSU 4x2488 JTAG Test Access Port (TAP) allows access to the TAP controller and the 4 TAP registers: instruction, bypass, device identification and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device scan path can be bypassed. For more details on the JTAG port, please refer to the Operations section.

Table 12 Instruction Register (Length - 3 bits)

Instructions	Selected Register	Instruction Codes, IR[2:0]
EXTEST	Boundary Scan	000
IDCODE	Identification	001
SAMPLE	Boundary Scan	010
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110
BYPASS	Bypass	111

Table 13 Identification Register

Length	32 bits
Version Number	01H(Revision B)
Part Number	5395H
Manufacturer's Identification Code	0CDH
Device Identification	153950CDH

Table 14 Boundary Scan Register

Name	Register Bit	Cell Type	Device ID
OEB_D[15]	153	OUT_CELL	0x0x153950CD
D[15]	152	IO_CELL	0x0x153950CD
OEB_D[14]	151	OUT_CELL	0x0x153950CD
D[14]	150	IO_CELL	0x0x153950CD
OEB_D[13]	149	OUT_CELL	0x0x153950CD
D[13]	148	IO_CELL	0x0x153950CD
OEB_D[12]	147	OUT_CELL	0x0x153950CD
D[12]	146	IO_CELL	0x0x153950CD
OEB_D[11]	145	OUT_CELL	0x0x153950CD
D[11]	144	IO_CELL	0x0x153950CD
OEB_D[10]	143	OUT_CELL	0x0x153950CD
D[10]	142	IO_CELL	0x0x153950CD

Name	Register Bit	Cell Type	Device ID
OEB_D[9]	141	OUT_CELL	0x0x153950CD
D[9]	140	IO_CELL	0x0x153950CD
OEB_D[8]	139	OUT_CELL	0x0x153950CD
D[8]	138	IO_CELL	0x0x153950CD
OEB_D[7]	137	OUT_CELL	0x0x153950CD
D[7]	136	IO_CELL	0x0x153950CD
OEB_D[6]	135	OUT_CELL	0x0x153950CD
D[6]	134	IO_CELL	0x0x153950CD
OEB_D[5]	133	OUT_CELL	0x0x153950CD
D[5]	132	IO_CELL	0x0x153950CD
OEB_D[4]	131	OUT_CELL	0x0x153950CD
D[4]	130	IO_CELL	0x0x153950CD
OEB_D[3]	129	OUT_CELL	0x0x153950CD
D[3]	128	IO_CELL	0x0x153950CD
OEB_D[2]	127	OUT_CELL	0x0x153950CD
D[2]	126	IO_CELL	0x0x153950CD
OEB_D[1]	125	OUT_CELL	0x0x153950CD
D[1]	124	IO_CELL	0x0x153950CD
OEB_D[0]	123	OUT_CELL	0x0x153950CD
D[0]	122	IO_CELL	0x0x153950CD
CSB	121	IN_CELL	0x0x153950CD
RDB	120	IN_CELL	0x0x153950CD
WRB	119	IN_CELL	0x0x153950CD
ALE	118	IN_CELL	0x0x153950CD
A[0]	117	IN_CELL	0x0x153950CD
A[1]	116	IN_CELL	0x0x153950CD
A[2]	115	IN_CELL	0x0x153950CD
A[3]	114	IN_CELL	0x0x153950CD
A[4]	113	IN_CELL	0x0x153950CD
A[5]	112	IN_CELL	0x0x153950CD
A[6]	111	IN_CELL	0x0x153950CD
A[7]	110	IN_CELL	0x0x153950CD
A[8]	109	IN_CELL	0x0x153950CD
A[9]	108	IN_CELL	0x0x153950CD
A[10]	107	IN_CELL	0x0x153950CD
A[11]	106	IN_CELL	0x0x153950CD
A[12]	105	IN_CELL	0x0x153950CD
A[13]	104	IN_CELL	0x0x153950CD
RSTB	103	IN_CELL	0x0x153950CD

Name	Register Bit	Cell Type	Device ID
OEB_INTB	102	OUT_CELL	0x0x153950CD
INTB	101	OUT_CELL	0x0x153950CD
SD[0]	100	IN_CELL	0x0x153950CD
SD[1]	99	IN_CELL	0x0x153950CD
SD[2]	98	IN_CELL	0x0x153950CD
SD[3]	97	IN_CELL	0x0x153950CD
OEB_TXENB[0]	96	OUT_CELL	0x0x153950CD
TXENB[0]	95	OUT_CELL	0x0x153950CD
OEB_TXENB[1]	94	OUT_CELL	0x0x153950CD
TXENB[1]	93	OUT_CELL	0x0x153950CD
OEB_TXENB[2]	92	OUT_CELL	0x0x153950CD
TXENB[2]	91	OUT_CELL	0x0x153950CD
OEB_TXENB[3]	90	OUT_CELL	0x0x153950CD
TXENB[3]	89	OUT_CELL	0x0x153950CD
OEB_SALM[0]	88	OUT_CELL	0x0x153950CD
SALM[0]	87	OUT_CELL	0x0x153950CD
OEB_SALM[1]	86	OUT_CELL	0x0x153950CD
SALM[1]	85	OUT_CELL	0x0x153950CD
OEB_SALM[2]	84	OUT_CELL	0x0x153950CD
SALM[2]	83	OUT_CELL	0x0x153950CD
OEB_SALM[3]	82	OUT_CELL	0x0x153950CD
SALM[3]	81	OUT_CELL	0x0x153950CD
OEB_TCLK[0]	80	OUT_CELL	0x0x153950CD
TCLK[0]	79	OUT_CELL	0x0x153950CD
OEB_TCLK[1]	78	OUT_CELL	0x0x153950CD
TCLK[1]	77	OUT_CELL	0x0x153950CD
OEB_TCLK[2]	76	OUT_CELL	0x0x153950CD
TCLK[2]	75	OUT_CELL	0x0x153950CD
OEB_TCLK[3]	74	OUT_CELL	0x0x153950CD
TCLK[3]	73	OUT_CELL	0x0x153950CD
OEB_RCLK[0]	72	OUT_CELL	0x0x153950CD
RCLK[0]	71	OUT_CELL	0x0x153950CD
OEB_RCLK[1]	70	OUT_CELL	0x0x153950CD
RCLK[1]	69	OUT_CELL	0x0x153950CD
OEB_RCLK[2]	68	OUT_CELL	0x0x153950CD
RCLK[2]	67	OUT_CELL	0x0x153950CD
OEB_RCLK[3]	66	OUT_CELL	0x0x153950CD
RCLK[3]	65	OUT_CELL	0x0x153950CD
OEB_PHASE_ERR[0]	64	OUT_CELL	0x0x153950CD

Name	Register Bit	Cell Type	Device ID
PHASE_ERR[0]	63	OUT_CELL	0x0x153950CD
OEB_PHASE_ERR[1]	62	OUT_CELL	0x0x153950CD
PHASE_ERR[1]	61	OUT_CELL	0x0x153950CD
OEB_PHASE_ERR[2]	60	OUT_CELL	0x0x153950CD
PHASE_ERR[2]	59	OUT_CELL	0x0x153950CD
OEB_PHASE_ERR[3]	58	OUT_CELL	0x0x153950CD
PHASE_ERR[3]	57	OUT_CELL	0x0x153950CD
PHASE_INIT[0]	56	IN_CELL	0x0x153950CD
PHASE_INIT[1]	55	IN_CELL	0x0x153950CD
PHASE_INIT[2]	54	IN_CELL	0x0x153950CD
PHASE_INIT[3]	53	IN_CELL	0x0x153950CD
OEB_SYNC_ERR[0]	52	OUT_CELL	0x0x153950CD
SYNC_ERR[0]	51	OUT_CELL	0x0x153950CD
OEB_SYNC_ERR[1]	50	OUT_CELL	0x0x153950CD
SYNC_ERR[1]	49	OUT_CELL	0x0x153950CD
OEB_SYNC_ERR[2]	48	OUT_CELL	0x0x153950CD
SYNC_ERR[2]	47	OUT_CELL	0x0x153950CD
OEB_SYNC_ERR[3]	46	OUT_CELL	0x0x153950CD
SYNC_ERR[3]	45	OUT_CELL	0x0x153950CD
LPTIMB	44	IN_CELL	0x0x153950CD
TX_JTAG_TXDATA3[3]	43	IN_CELL	0x0x153950CD
TX_JTAG_TXDATA3[2]	42	IN_CELL	0x0x153950CD
TX_JTAG_TXCLK3	41	IN_CELL	0x0x153950CD
TX_JTAG_TXDATA3[1]	40	IN_CELL	0x0x153950CD
TX_JTAG_TXDATA3[0]	39	IN_CELL	0x0x153950CD
TX_JTAG_TXDATA2[3]	38	IN_CELL	0x0x153950CD
TX_JTAG_TXDATA2[2]	37	IN_CELL	0x0x153950CD
TX_JTAG_TXCLK2	36	IN_CELL	0x0x153950CD
TX_JTAG_TXDATA2[1]	35	IN_CELL	0x0x153950CD
TX_JTAG_TXDATA2[0]	34	IN_CELL	0x0x153950CD
TX_JTAG_TXDATA1[3]	33	IN_CELL	0x0x153950CD
TX_JTAG_TXDATA1[2]	32	IN_CELL	0x0x153950CD
TX_JTAG_TXCLK1	31	IN_CELL	0x0x153950CD
TX_JTAG_TXDATA1[1]	30	IN_CELL	0x0x153950CD
TX_JTAG_TXDATA1[0]	29	IN_CELL	0x0x153950CD
TX_JTAG_TXDATA0[3]	28	IN_CELL	0x0x153950CD
TX_JTAG_TXDATA0[2]	27	IN_CELL	0x0x153950CD
TX_JTAG_TXCLK0	26	IN_CELL	0x0x153950CD
TX_JTAG_TXDATA0[1]	25	IN_CELL	0x0x153950CD

Name	Register Bit	Cell Type	Device ID
TX_JTAG_TXDATA0[0]	24	IN_CELL	0x0x153950CD
TX_JTAG_TXCLK_SRC3	23	OUT_CELL	0x0x153950CD
RX_JTAG_RXDATA3[3]	22	OUT_CELL	0x0x153950CD
RX_JTAG_RXDATA3[2]	21	OUT_CELL	0x0x153950CD
RX_JTAG_RXCLK3	20	OUT_CELL	0x0x153950CD
RX_JTAG_RXDATA3[1]	19	OUT_CELL	0x0x153950CD
RX_JTAG_RXDATA3[0]	18	OUT_CELL	0x0x153950CD
TX_JTAG_TXCLK_SRC2	17	OUT_CELL	0x0x153950CD
RX_JTAG_RXDATA2[3]	16	OUT_CELL	0x0x153950CD
RX_JTAG_RXDATA2[2]	15	OUT_CELL	0x0x153950CD
RX_JTAG_RXCLK2	14	OUT_CELL	0x0x153950CD
RX_JTAG_RXDATA2[1]	13	OUT_CELL	0x0x153950CD
RX_JTAG_RXDATA2[0]	12	OUT_CELL	0x0x153950CD
TX_JTAG_TXCLK_SRC1	11	OUT_CELL	0x0x153950CD
RX_JTAG_RXDATA1[3]	10	OUT_CELL	0x0x153950CD
RX_JTAG_RXDATA1[2]	9	OUT_CELL	0x0x153950CD
RX_JTAG_RXCLK1	8	OUT_CELL	0x0x153950CD
RX_JTAG_RXDATA1[1]	7	OUT_CELL	0x0x153950CD
RX_JTAG_RXDATA1[0]	6	OUT_CELL	0x0x153950CD
TX_JTAG_TXCLK_SRC0	5	OUT_CELL	0x0x153950CD
RX_JTAG_RXDATA0[3]	4	OUT_CELL	0x0x153950CD
RX_JTAG_RXDATA0[2]	3	OUT_CELL	0x0x153950CD
RX_JTAG_RXCLK0	2	OUT_CELL	0x0x153950CD
RX_JTAG_RXDATA0[1]	1	OUT_CELL	0x0x153950CD
RX_JTAG_RXDATA0[0]	0	OUT_CELL	0x0x153950CD

Note 1: When set high, INTB will be set to high impedance.

Note 2: Each output cell has its own output enable (OEB_*)

Note 3: 153 is the first bit in the boundary scan chain, and 0 is the first bit out of the boundary scan chain.

12.3 Boundary Scan Cells

In the following diagrams, CLOCK-DR is equal to TCK when the current controller state is SHIFT-DR or CAPTURE-DR, and unchanging otherwise. The multiplexer in the center of the diagram selects one of four inputs, depending on the status of select lines G1 and G2. The ID Code bit is as listed in the Boundary Scan Register table located above.

Figure 10 Input Observation Cell (IN_CELL)

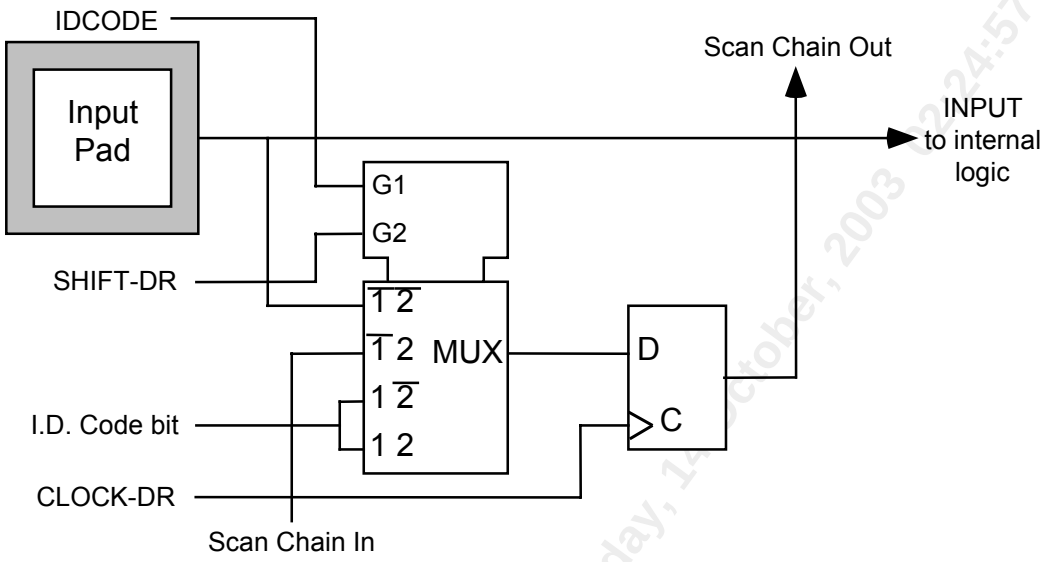


Figure 11 Output Cell (OUT_CELL)

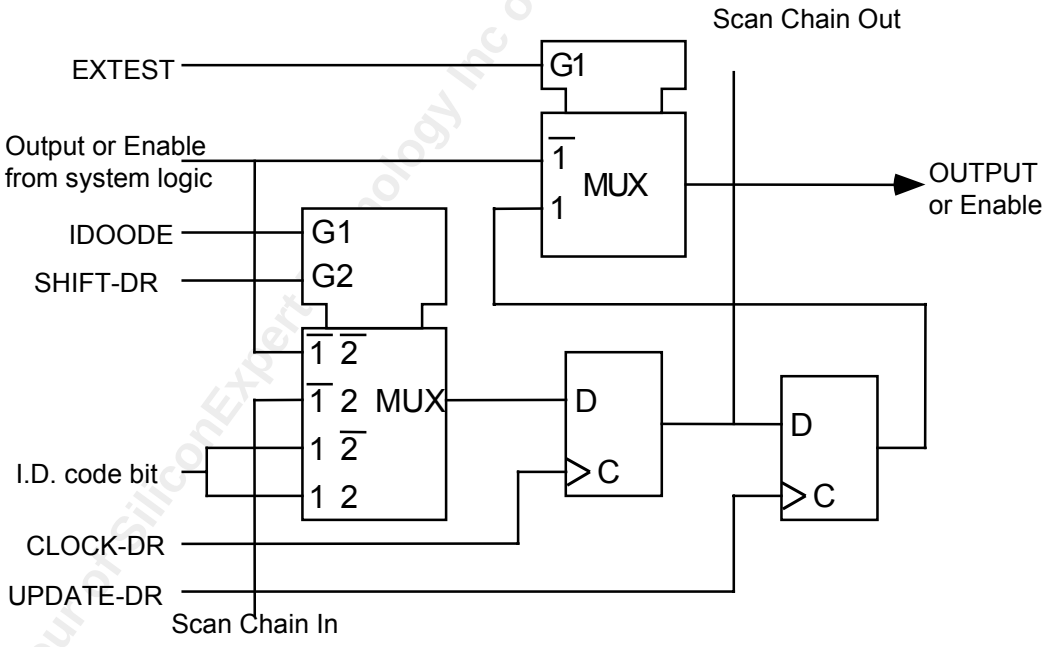


Figure 12 Bidirectional Cell (IO_CELL)

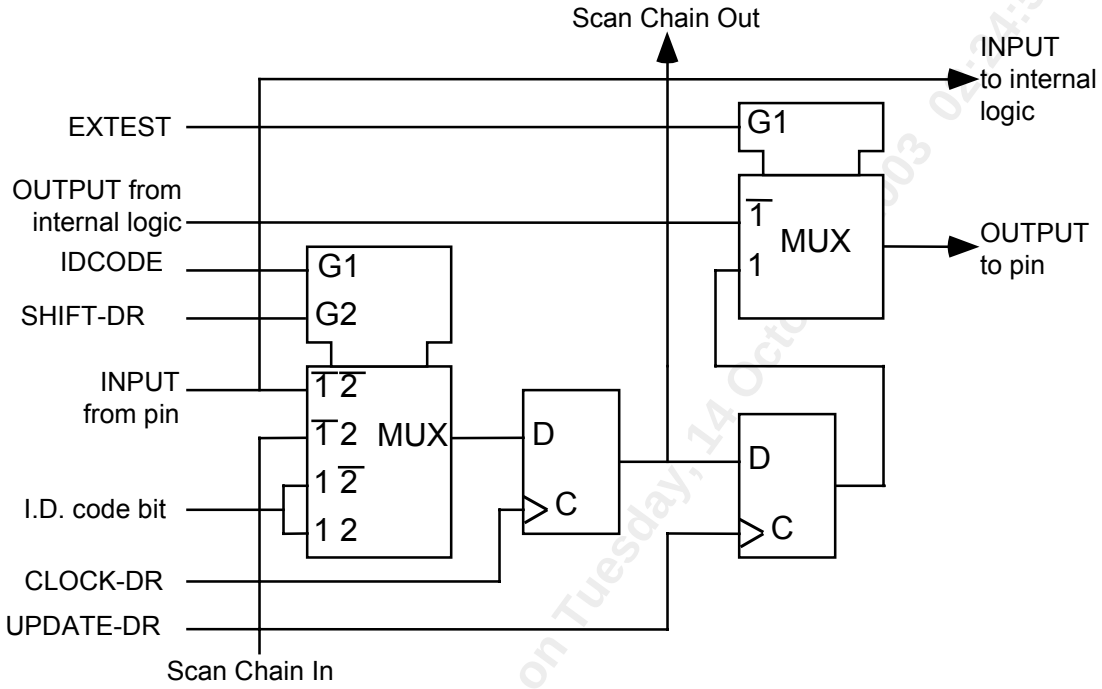
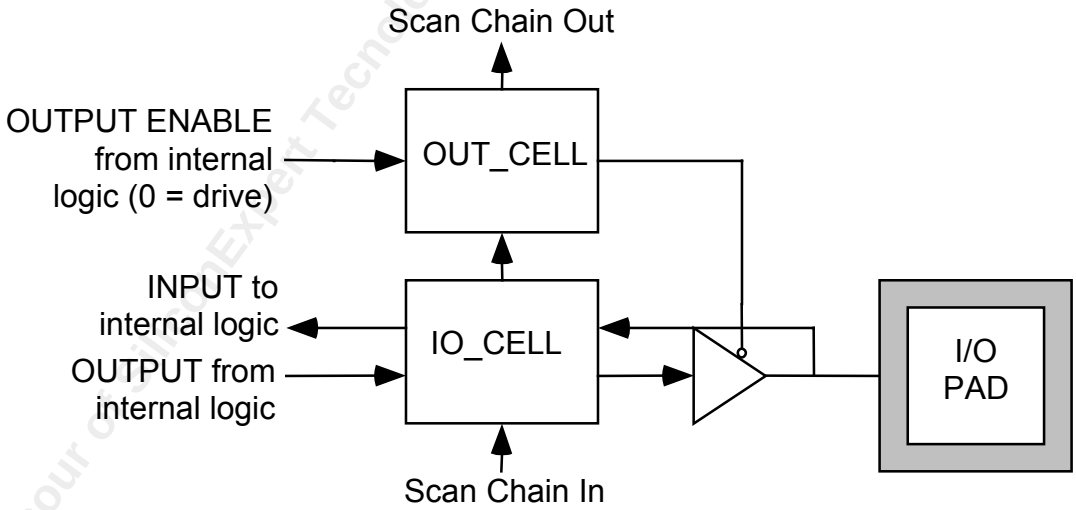


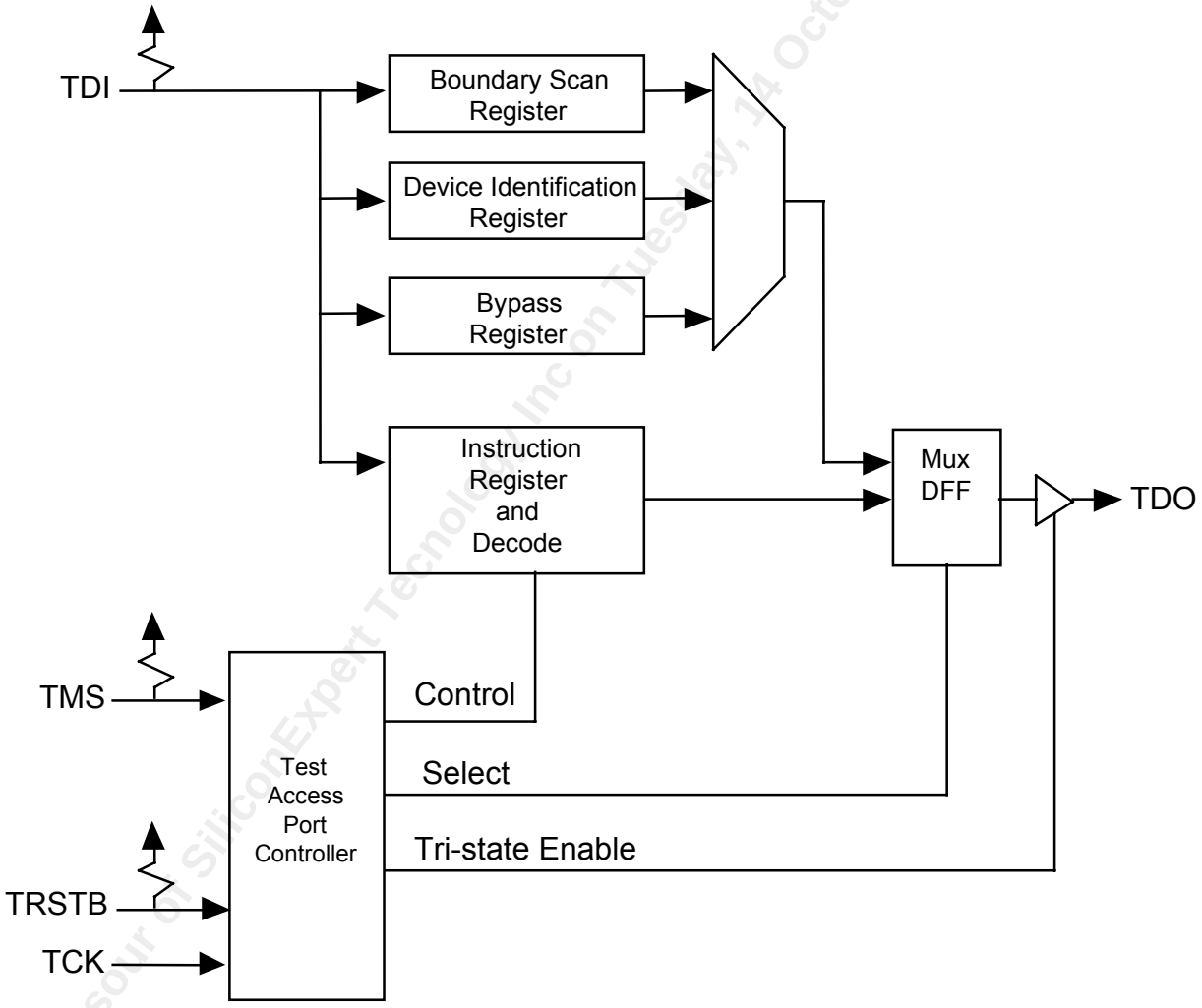
Figure 13 Layout of Output Enable and Bidirectional Cells



12.4 JTAG Control

The CRSU 4x2488 supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The Test Access Port (TAP) consists of the five standard pins, TRSTB, TCK, TMS, TDI and TDO used to control the TAP controller and the boundary scan registers. The TRSTB input is the active-low reset signal used to reset the TAP controller. TRSTB should be tied to RSTB if the JTAG interface is not used. TCK is the test clock used to sample data on input, TDI and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states. The basic boundary scan architecture is shown below.

Figure 14 Boundary Scan Architecture



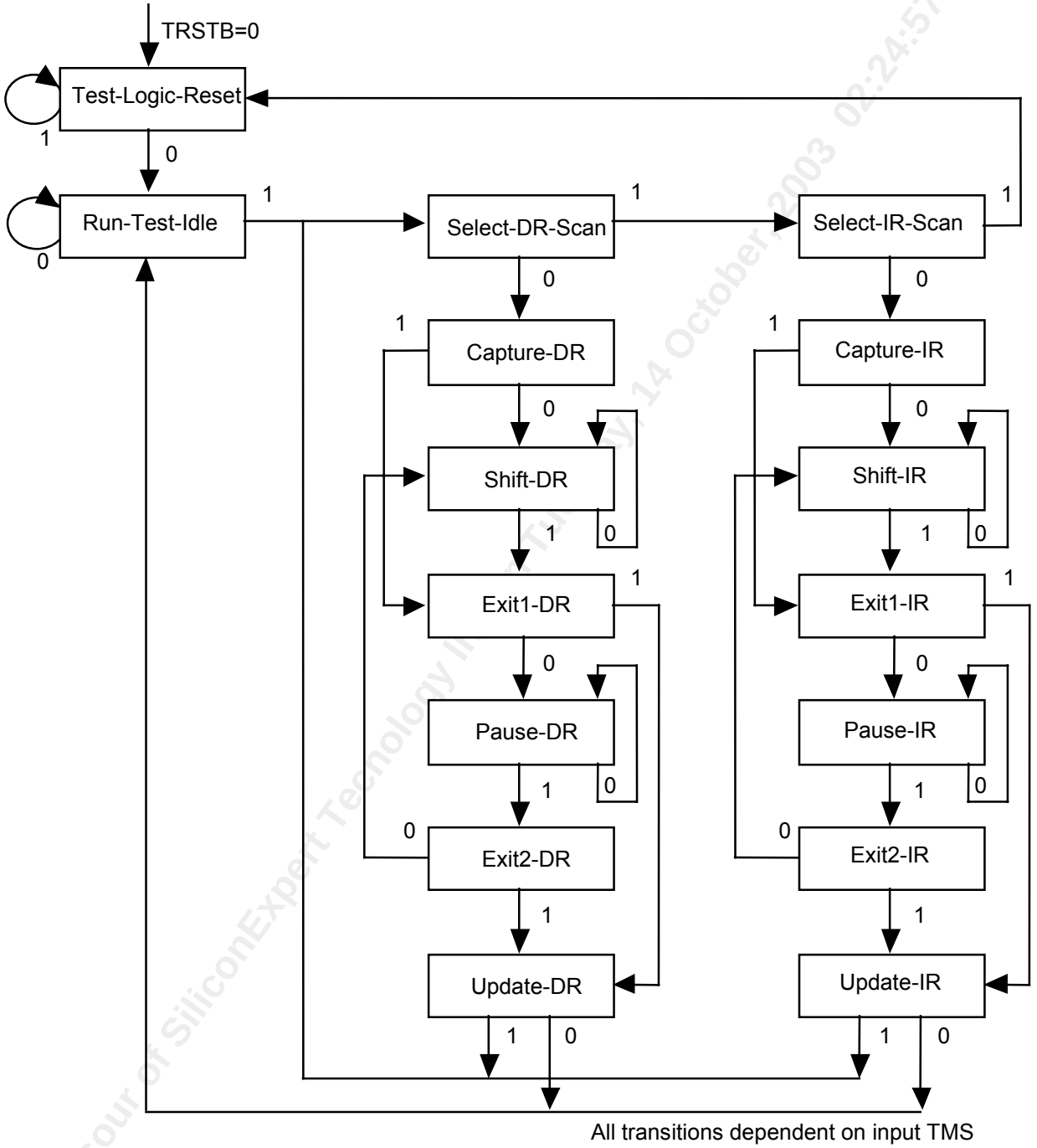
The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single-bit delay from primary input, TDI to primary output, TDO. The device identification register contains the device identification code.

The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register place in series with device inputs and outputs. Using the boundary scan register, all digital inputs can be sampled and shifted out on primary output, TDO. In addition, patterns can be shifted in on primary input, TDI and forced onto all digital outputs.

12.4.1 TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary input, TMS. The finite state machine is described below.

Figure 15 TAP Controller Finite State Machine



12.4.2 States

Test-Logic-Reset

The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for 5 TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

Run-Test-Idle

The run test/idle state is used to execute tests.

Capture-DR

The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

Shift-DR

The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-DR

The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

Capture-IR

The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

Shift-IR

The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-IR

The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

Boundary Scan Instructions

The following is a description of the standard instructions. Each instruction selects a serial test data register path between input, TDI and output, TDO.

12.4.3 Instructions

BYPASS

The bypass instruction shifts data from input, TDI to output, TDO with one TCK clock period delay. The instruction is used to bypass the device.

EXTEST

The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is place between input, TDI and output, TDO. Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

SAMPLE

The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

IDCODE

The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

STCTEST

The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan register. The code can then be shifted out output, TDO using the Shift-DR state.

13 Operation

13.1 Initialization Settings

13.1.1 TRSP Register settings:

Register 1050 TRSP Configuration

LREIEN Bit 10: Must be set to logic 0 when the transmit SONET path is enabled.

APSEN Bit 9: Must be set to logic 0 when the transmit SONET path is enabled. Not setting this to logic 0 will cause errors in the FEC operation or in the Line overhead bytes of the frame.

Register 1052H, 1062H, 1072H and 1082H TRSP Error Insertion.

B2DISABLE Bit 8 : Must be set to logic 1 if the FEC encoder is enabled.

13.2 System side interface issues

13.2.1 B1 Byte Recalculated

The CRSU 4x2488 performs all of the section terminating tasks of the SONET frame and some of the line terminating tasks. This results in the SONET frame transmitted and received on the QSFI-4 interface being modified from the line frame. When the FEC encoder/decoder is enabled the downstream framer should be aware the CRSU 4x2488 performs descrambling on the received frame and checks the B1 and B2 bytes. Because the B1 byte is calculated over the scrambled frame the B1 byte passed over the QSFI-4 interface will not be correct. The downstream framer should disable B1 checks.

13.2.2 Line side data frequency out of specification issues

If the line side optical received signal deviates by more than 1000ppm, the CRU cannot maintain a lock on the receive data and will switch between recovered and reference clock. The corresponding QSFI rxclkn becomes unstable as it is derived from the CRU.

13.3 QSFI-4 Common Electrical Interface Overview

The CRSU 4x2488 QSFI-4 Port is based on the OIF SFI-4 Electrical interface. The QFSI-4 is realized as a 4xOC48 interface, not an OC192 Electrical interface described in the OIF SFI-4 Electrical interface specification. Each OC48 4-bit data interface has it's own clock which is independent of the other OC48 4-bit data and clock. This differs from the OIF SFI-4 Electrical which has a 16-bit data interface and one clock.

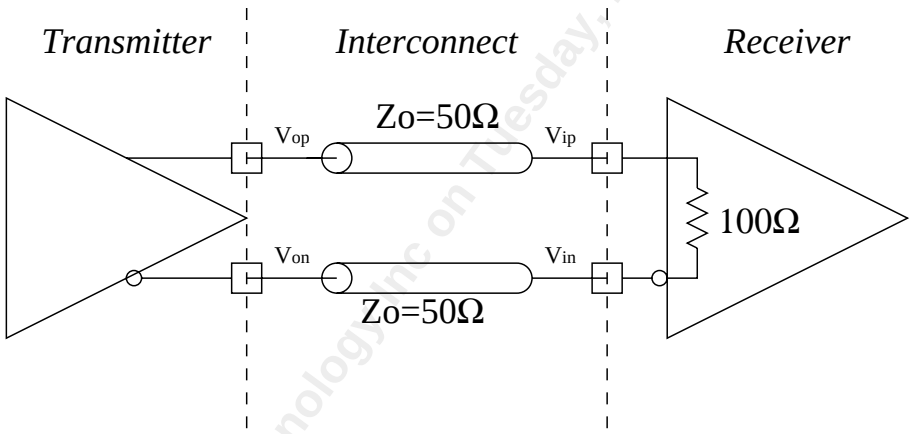
The interface implements a quad 4-bit nominal 622.08 Mb/s LVDS link enabling an aggregate of 9953.28 Mb/s transfer in each direction.

A reference clock of 77.76MHz is required which is generated internally from the CRSU 4x2488 CSU Channel 0. If channel 0 CSU is held in reset, the QSFI-4 LVDS interface will not be compliant to IEEE 1596.3-1996 standard and correct functionality cannot be assured.

Each 4-bit 622 Mb/s LVDS interface can transfer a single STS-48 aggregate data stream. Each link is an independent channel and cannot be combined inside the CRSU 4x2488 to form a concatenated STS-192 data stream.

A generic LVDS link according to IEEE 1596.3-1996 is illustrated below. The transmitter drives a differential signal through a pair of 50Ω characteristic interconnects, such as board traces, backplane traces, or short lengths of cable. The receiver presents a 100Ω differential termination impedance to terminate the lines. Included in the standard is sufficient common-mode range for the receiver to accommodate as much as 925mV of common-mode ground difference.

Figure 16 Generic LVDS Link Block Diagram



Complete SERDES transceiver functionality is provided. Eight-bit parallel data is sampled by the link rate divided-by-8 clock (77.76MHz SYSCLK) and then serialized at the link rate on the LVDS output pins by a 622.08 MHz clock synthesized from the REFCLK. Serial link rate LVDS data is sampled and de-serialized to 8-bit parallel data.

At the system level, reliable operation will be obtained if proper signal integrity is maintained through the signal path and the receiver requirements are respected. Namely, a worst case eye opening of 0.7UI and 100mV differential amplitude is needed. These conditions should be achievable with a system architecture consisting of board traces, two sets of back-plane connectors and up to 1m of back-plane interconnects. This assumes proper design of 100Ω differential lines and minimization of discontinuities in the signal path. The output differential amplitude is approximately 350mV.

The LVDS system is comprised of the LVDS Receiver (RXLVDS), LVDS Transmitter (TXLVDS) and Transmitter LVDS Reference (TXLVREF) blocks.

13.3.1 LVDS Receiver (RXLVDS)

The RXLVDS ABC is a 675 Mb/s Low Voltage Differential Signalling (LVDS) Receiver according to the IEEE 1596.3-1996 LVDS Specification.

The RXLVDS ABC accepts up to 675 Mb/s LVDS signals from the transmitter, amplifies them, converts them to digital signals and passes them to a Serial-In Parallel-Out (SIPO) converter. As per to the IEEE 1596.3-1996 specification, the RXLVDS has a differential input sensitivity better than 100mV.

13.3.2 Serial-In Parallel-Out (SIPO)

The SIPO is a fully integrated serial to parallel converter which is used to convert a serial 675 Mb/s data stream to an 8-bit 77.76 MHz data stream. The first bit received is placed in the most significant bit (bit 7) of the byte and the last bit received is placed in the least significant bit (bit 0) of the byte.

13.3.3 LVDS Transmitter (TXLVDS)

The TXLVDS is a 675 Mb/s Low Voltage Differential Signalling (LVDS) Transmitter according to the IEEE 1596.3-1996 LVDS Specification except the rise and falls times which are OIF-SFI4-01.0 compliant. The TXLVDS accepts 675 Mbit/s of differential data from the PISO circuit and transmits the data off-chip as a low voltage differential signal. The TXLVDS uses the reference current and voltage from the TXLVREF to control the output differential voltage amplitude and the output common-mode voltage.

13.3.4 Parallel-In Serial-Out (PISO)

The PISO is a fully integrated parallel to serial converter which is used to convert a parallel 8-bit 77.76 MHz data stream to a serial 675 Mb/s data stream. The Most significant bit (bit 7) of the byte is transmitted first and the least significant bit (bit 0) of the byte is transmitted last.

13.3.5 LVDS Transmit Reference (TXLVREF)

The TXLVREF provides the voltage and current references for all LVDS transmitters.

13.4 Transport Overhead Bytes

A1, A2: The frame alignment bytes (A1, A2) locate the SONET frame in the STS-48c (STM-16c) serial stream.

J0 The J0 byte is currently defined as the STS-48c (STM-16c) section trace byte for SONET/SDH. J0 byte is not scrambled by the frame synchronous scrambler.

Z0: The Z0 bytes are currently defined as the STS-48c (STM-16c) section growth bytes for SONET/SDH. Z0 bytes are not scrambled by the frame synchronous scrambler.

B1: The section bit interleaved parity byte provides a section error monitoring function.

In the transmit direction, the CRSU 4x2488 calculates the B1 byte over all bits of the previous frame after scrambling. The calculated code is then placed in the current frame before scrambling.

In the receive direction, the CRSU 4x2488 calculates the B1 code over the current frame and compares this calculation with the B1 byte received in the following frame. B1 errors are accumulated in an error event counter.

D1-D3: The section data communications channel provides a 192 kbit/s data communications channel for network element to network element communications.

H1,H2: The pointer value bytes locate the path overhead column in the SONET/SDH frame. The CRSU 4x2488 does not generate or modify the H1 or H2 byes.

H3: The pointer action bytes contain synchronous payload envelope data when a negative stuff event occurs. The all zeros pattern is inserted in the transmit direction. This byte is ignored in the receive direction unless a negative stuff event is detected.

B2: The line bit interleaved parity bytes provide a line error monitoring function.

In the transmit direction, the CRSU 4x2488 calculates the B2 values. The calculated code is then placed in the next frame.

In the receive direction, the CRSU 4x2488 calculates the B2 code over the current frame and compares this calculation with the B2 code received in the following frame. Receive B2 errors are accumulated in an error event counter.

K1,K2: The K1 and K2 bytes provide the automatic protection switching channel. The K2 byte is also used to identify line layer maintenance signals. Line RDI is indicated when bits 6, 7, and 8 of the K2 byte are set to the pattern '110'. Line AIS is indicated when bits 6, 7, and 8 of the K2 byte are set to the pattern '111'.

In the transmit direction, the CRSU 4x2488 provides register control for the K1 and K2 bytes.

In the receive direction, the CRSU 4x2488 provides register access to the filtered APS channel. Protection switch byte failure alarm detection is provided. The K2 byte is examined to determine the presence of the line AIS, or the line RDI maintenance signals

D4-D12: The line data communications channel provides a 576 kbit/s data communications channel for network element to network element communications.

S1: The S1 byte provides the synchronization status byte. Bits 5 through 8 of the synchronization status byte identifies the synchronization source of STS-48c (STM-16c) signal. Bits 1 through 4 are currently undefined.

In the transmit direction, the CRSU 4x2488 provides register control for the synchronization status byte.

In the receive direction, the CRSU 4x2488 provides register access to the synchronization status byte.

Z1: The Z1 bytes are located in the second and third STS-1's locations of an STS-48c (STM-16c) and are allocated for future growth.

M1: The M1 byte is located in the third STS-1 location of a STS-48c (STM-16c) and provides a line far end block error function for remote performance monitoring.

Z2: The Z2 bytes are located in the first and second STS-1's locations of a STS-12c (STM-4c) and are allocated for future growth.

In the transmit direction, Z2 byte is internally generated. The number of B2 errors detected in the previous interval is inserted.

In the receive direction, a legal Z2 byte value is added to the line FEBE event counter.

13.5 SBER Bit Error Rate Monitor

The SBER Bit Error Rate Monitor (BERM) block counts and monitors line BIP errors over programmable periods of time (window size). It can monitor to declare an alarm or to clear it if the alarm is already set. A different threshold must be used to declare or clear the alarm, whether or not those two operations are performed at the same BER. The following tables list the recommended content of the SBER BERM registers (1184H to 1193H) for different speeds (STS-N) and bit error rates (BER). Both BERM Register types, SF and SD, are equivalent and are programmed similarly. In a normal application they will be set to monitor different bit error rates.

When the appropriate SF/SD CMODE bit in register 1180H is set to logic '1' monitoring for the alarm clear condition is performed using a window size that is 8 times longer than the declaration window size. When the SF/SD CMODE bit is set to logic '0' the alarm clear monitoring will use a window size equal to the declaration window size. In all cases the clearing threshold is calculated for a BER that is 10 times lower than the declaration BER, as required in the references. The tables indicate the declare BER, the evaluation period and the recommended CMODE and associated thresholds.

The Saturation threshold is not listed in the table, and is programmed with the value 0xFFFFFF by default, deactivating saturation. Saturation capabilities are provided to allow the user to address issues associated with error bursts. It enables the user to determine a ceiling value at which the error counters will saturate, letting error bursts pass through within a frame or sub window period.

Since the monitoring algorithm is based on a pseudo-sliding window containing 8 sub intervals, the time required to declare or clear an alarm can take up to 9 sub accumulation periods (SAP). The following tables thus consider that each SAP must take a value lower or equal to $1/9^{th}$ of the timing constraint, in frames.

Table 15 Recommended BERM settings for different data and BER rates, meeting Bellcore Objectives

STS	Monitored Declare BER	Objective met for Switching Time (s)	SF/SD CMODE	SF/SD SAP (hex)	SF/SD DECTH (hex)	SF/SD CLRTH (hex)
1	10^{-3}	0.008	0	00000007	0000A1	00002B
1	10^{-4}	0.040	0	00000023	000091	000019
1	10^{-5}	0.300	0	0000010A	000074	000014
1	10^{-6}	3.000	0	00000A6A	000075	000014
1	10^{-7}	30.000	0	0000682A	000075	000014
1	10^{-8}	250.000	0	0003640E	000060	000011
1	10^{-9}	2000.000	0	001B2071	00004B	00000F
3	10^{-3}	0.008	0	00000007	0001FB	000074
3	10^{-4}	0.013	0	0000000B	000088	000018
3	10^{-5}	0.100	0	00000058	000073	000014
3	10^{-6}	1.000	0	00000378	000075	000014
3	10^{-7}	10.000	0	000022B8	000075	000014
3	10^{-8}	83.000	0	00012031	00005F	000011
3	10^{-9}	667.000	0	00090BF8	00004B	00000F
12	10^{-3}	0.008	0	00000007	000828	0001AE
12	10^{-4}	0.008	0	00000007	00016E	000036
12	10^{-5}	0.025	0	00000016	000073	000014
12	10^{-6}	0.250	0	000000DE	000075	000014
12	10^{-7}	2.500	0	000008AE	000075	000014
12	10^{-8}	21.000	0	000048EA	000061	000012
12	10^{-9}	167.000	0	000243DC	00004B	00000F
48	10^{-3}	0.008	0	00000007	002116	000677
48	10^{-4}	0.008	0	00000007	0005F8	0000C1
48	10^{-5}	0.008	0	00000007	000095	000019
48	10^{-6}	0.063	0	00000037	000074	000014
48	10^{-7}	0.625	0	0000022B	000075	000014
48	10^{-8}	5.200	0	0000120E	000060	000011
48	10^{-9}	42.000	0	000091D5	00004C	00000F

STS	Monitored Declare BER	Objective met for Switching Time (s)	SF/SD CMODE	SF/SD SAP (hex)	SF/SD DECTH (hex)	SF/SD CLRTH (hex)
192	10^{-3}	0.008	0	00000007	008547	00195E
192	10^{-4}	0.008	0	00000007	001860	0002D7
192	10^{-5}	0.008	0	00000007	000280	000053
192	10^{-6}	0.016	0	0000000E	000076	000014
192	10^{-7}	0.156	0	0000008A	000074	000014
192	10^{-8}	1.300	0	00000483	000060	000011
192	10^{-9}	10.400	0	0000241C	00004B	00000F

Table 16 Recommended BERM settings for different data and BER rates, meeting Bellcore and ITU requirements

STS	Monitored Declare BER	Requirement met for Switching Time (s)	SF/SD CMODE	SF/SD SAP (hex)	SF/SD DECTH (hex)	SF/SD CLRTH (hex)
1	10^{-3}	0.01	0	00000008	0000B2	000034
1	10^{-4}	0.10	0	0000002B	0000AB	000021
1	10^{-5}	1.00	0	00000192	0000AB	000020
1	10^{-6}	10.00	0	00000F98	0000AB	00001F
1	10^{-7}	100.00	0	00009BD6	0000AB	00001F
1	10^{-8}	1,000.00	0	00061647	0000AB	00001F
1	10^{-9}	10,000.00	0	003CDEAD	0000AB	00001F
3	10^{-3}	0.01	0	00000008	000238	00008A
3	10^{-4}	0.10	0	0000002B	00022B	000055
3	10^{-5}	1.00	0	00000192	00022B	000051
3	10^{-6}	10.00	0	00000F98	00022B	000050
3	10^{-7}	100.00	0	00009BD6	00022B	000050
3	10^{-8}	1,000.00	0	00061647	00022B	000050
3	10^{-9}	10,000.00	0	003CDEAD	00022B	000050
12	10^{-3}	0.01	0	00000008	00093C	0001F7
12	10^{-4}	0.10	0	0000002B	00091D	00012C
12	10^{-5}	1.00	0	00000192	000922	00011C
12	10^{-6}	10.00	0	00000F98	000922	00011B

STS	Monitored Declare BER	Requirement met for Switching Time (s)	SF/SD CMODE	SF/SD SAP (hex)	SF/SD DECTH (hex)	SF/SD CLRTH (hex)
12	10^{-7}	100.00	0	00009BD6	000922	00011A
12	10^{-8}	1,000.00	0	00061647	000922	00011A
12	10^{-9}	10,000.00	0	003CDEAD	000922	00011A
48	10^{-3}	0.01	0	00000008	0025A5	00077B
48	10^{-4}	0.10	0	0000002B	002554	000465
48	10^{-5}	1.00	0	00000192	00256F	000426
48	10^{-6}	10.00	0	00000F98	002570	000420
48	10^{-7}	100.00	0	00009BD6	002571	00041F
48	10^{-8}	1,000.00	0	00061647	002571	00041F
48	10^{-9}	10,000.00	0	003CDEAD	002571	00041F
192	10^{-3}	0.01	0	00000008	0097FA	001D2C
192	10^{-4}	0.10	0	0000002B	00970C	0010FD
192	10^{-5}	1.00	0	00000192	009789	001004
192	10^{-6}	10.00	0	00000F98	00978F	000FEB
192	10^{-7}	100.00	0	00009BD6	009792	000FE9
192	10^{-8}	1,000.00	0	00061647	009793	000FE9
192	10^{-9}	10,000.00	0	003CDEAD	009793	000FE9

Important Notice:

The user should NOT use CMODE = 1 mode when working with Bellcore or ITU requirements for the evaluation periods. In this case the clearing time (8 times declare time) would not conform to the requirements (where clearing time requirement = declare time requirement). For the same reason, the user should also avoid using CMODE = 1 with Bellcore objectives when dealing with STS-1 or any detection threshold = 10^{-3}.

The user should note that a probability of 99% was assumed as the probability that the switch initiation time (declaring) is below the Bellcore requirement. Since the Bellcore specification is vague regarding this issue (“must be very close to 1.0”), the approximation with 0.99 is sufficient and lets the Bellcore requirements be identical to the ITU requirements.

The user should also note that the Bellcore objectives are stricter than Bellcore and ITU requirements upon detection and clearing times. But Bellcore and ITU requirements are stricter than Bellcore objectives upon detection and clearing probability for a given BER (99% vs 95% for Bellcore objectives).

13.6 Clocking Operations

Register 000EH: Clock Control contains device clock control bits. These bits allow digital clocks to be killed. Depending on the configurations being used, clocks can be killed in unused digital blocks to reduce power consumption.

Section 17.1 Power Requirements contains register settings for operating modes and the power measurements for those modes of operation.

13.7 Looptime Operation

When loop time operation is employed the transmit csu uses a clock recovered from the receive data stream for it's reference. When the receive channel is locked to data, both transmit and receive channels will be frequency locked. When the CRU is not locked to data state (register 1103 bit 6 DOOLV = 1'b1), the CSU automatically uses the reference clock as it's reference.

Looptime operation should be used during all line side loopback configurations.

To assert a channel into looptime operation the following registers must be set as follows

to configure channel 0

Register 000DH: Diagnostic Loopback and ICO control

Bit	Type	Function	
Bit 2	R/W	ICO_CTRL_1	0
Bit 1	R/W	ICO_CTRL_0	1

Register 10A1H: TXLI CSU Control

Bit	Type	Function	
Bit 7	R/W	LOOPTIMEB	0
Bit 6	R/W	LF_RESISTOR[1]	0
Bit 5	R/W	LF_RESISTOR[0]	0
Bit 3	R/W	DIVIDE_RATIO	0
Bit 1	R/W	CHARGE_PUMP[1]	0
Bit 0	R/W	CHARGE_PUMP[0]	1

13.8 System side serial Loopback Operation

Provides a diagnostic loopback of data applied to the transmit QSFI-4 to the receive QSFI-4 pins. i.e. TXDATAn[3:0] +/- to RXDATAn[3:0] +/-. This loopback operation is performed in the TXLI and RXLI tsb's.

- loopback configuration is valid in all bypass and non bypass modes.
- operates in non loop-time configuration only.

- TXDATAn[3:0] +/- data is also transmitted on txd+/-

to configure channel 0

Register RXLI 1102H: CRU Control

Bit	Type	Function	
Bit 7	R/W	SDLE	1

13.9 System side Parallel Loopback operation

Provides a loopback of data applied to the transmit QSFI-4 to the receive QSFI-4 pins. i.e. TXDATAn[3:0] +/- to RXDATAn[3:0] +/-. This loopback operation occurs between the output of transmit STLI and receive SRLI.

- transmit and receive must be configured in non-bypass mode
- receive channel cru in lock to reference mode
- transmit channel in looptime or non looptime configuration
- TXDATAn[3:0] +/- data is also transmitted on txd+/-

to configure channel 0

Register RXLI 1102H: CRU Control

Bit	Type	Function	
Bit 10	R/W	LOCK_TO_REF	1

Register 000CH: Diagnostic Bypass Modes

Bit	Type	Function	
Bit 7	R/W	RX_BYPASS_CH3	0
Bit 6	R/W	RX_BYPASS_CH2	0
Bit 5	R/W	RX_BYPASS_CH1	0
Bit 4	R/W	RX_BYPASS_CH0	0
Bit 3	R/W	TX_BYPASS_CH3	0
Bit 2	R/W	TX_BYPASS_CH2	0
Bit 1	R/W	TX_BYPASS_CH1	0
Bit 0	R/W	TX_BYPASS_CH0	0

Register 000DH: Diagnostic Bypass Modes

Bit	Type	Function	
Bit 4	R/W	SPLE_CH0	1

13.10 Line Side Parallel Loopback Operation

Provides a diagnostic loopback of data applied to the line side receive RXDn +/- input pins to the transmit line side TXDn +/- output pins.

- loopback configuration is valid in all bypass and non bypass modes.
- operates in looptime configuration only
- RXDn +/- received data is also output on QSFI-4 interface pins RXDATAn[3:0]

to configure channel 0

Register 000DH: Diagnostic Loopback and ICO control

Bit	Type	Function	
Bit 2	R/W	ICO_CTRL_1	0
Bit 1	R/W	ICO_CTRL_0	1

Register 10A1H: TXLI CSU Control

Bit	Type	Function	
Bit 15	R/W	RECCLK_SEL	0
Bit 7	R/W	LOOPTIMEB	0
Bit 6	R/W	LF_RESISTOR[1]	0
Bit 5	R/W	LF_RESISTOR[0]	0
Bit 3	R/W	DIVIDE_RATIO	0
Bit 1	R/W	CHARGE_PUMP[1]	0
Bit 0	R/W	CHARGE_PUMP[0]	1

Register TXLI 10A0H: TXLI Control

Bit	Type	Function	
Bit 3	R/W	LPLE_TX	1

Register RXLI 1103H: RXLI CRU clock training and Configuration

Bit	Type	Function	
Bit 9	R/W	LPLE_RX	1

13.11 Line Side, same Channel Loopback Operation

To configure the device to loopback data from the line side receive to line side transmit on the same channel.

This loopback configuration is

- This loopback configuration is valid in all bypass and non bypass modes.
- used in looptime mode only
- RXDn +/- received data is also output on QSFI-4 interface pins RXDATAn[3:0]

to configure channel 0

Register 000DH: Diagnostic Loopback and ICO control

Bit	Type	Function	
Bit 2	R/W	ICO_CTRL_1	0
Bit 1	R/W	ICO_CTRL_0	1

Register 10A1H: TXLI CSU Control

Bit	Type	Function	
Bit 15	R/W	RECCLK_SEL	0
Bit 7	R/W	LOOPTIMEB	0
Bit 6	R/W	LF_RESISTOR[1]	0
Bit 5	R/W	LF_RESISTOR[0]	0
Bit 3	R/W	DIVIDE_RATIO	0
Bit 1	R/W	CHARGE_PUMP[1]	0
Bit 0	R/W	CHARGE_PUMP[0]	1

Register 000FH: Bypass and Loop-across

Bit	Type	Function	
Bit 13	R/W	LBEN_CH1	0
Bit 12	R/W	LBEN_CH0	1
Bit 9	R/W	CHLBEN_CH1	0
Bit 8	R/W	CHLBEN_CH0	0

13.12 Line side, Channel to Channel Loopback Operation

The device can be configured to loopback channel 0 RXD to channel 1 TXD pins, channel 1 RXD to channel 0 TXD pins. Likewise, we can configure channel 2 RXD to channel 3 TXD pins, channel 3 RXD to channel 2 TXD pins. If the system side QSFI-4 interface is not used we can disable it to reduce power consumption (register 00013H bit 11).

This loopback configuration is

- valid in all bypass and non bypass modes.
- used in looptime mode only
- RXDn +/- received data is also output on QSFI-4 interface pins RXDATAn[3:0]

to configure channel 0 & channel 1 loopback the following registers should be programmed.

Register 000DH: Diagnostic Loopback and ICO control

Bit	Type	Function	
Bit 2	R/W	ICO_CTRL_1	0
Bit 1	R/W	ICO_CTRL_0	1

Register 10A1H: TXLI CSU Control

Bit	Type	Function	
Bit 15	R/W	RECCLK_SEL	1
Bit 7	R/W	LOOPTIMEB	0
Bit 6	R/W	LF_RESISTOR[1]	0
Bit 5	R/W	LF_RESISTOR[0]	0
Bit 3	R/W	DIVIDE_RATIO	0
Bit 1	R/W	CHARGE_PUMP[1]	0
Bit 0	R/W	CHARGE_PUMP[0]	1

Register 12A1H: TXLI CSU Control

Bit	Type	Function	
Bit 15	R/W	RECCLK_SEL	1
Bit 7	R/W	LOOPTIMEB	0
Bit 6	R/W	LF_RESISTOR[1]	0
Bit 5	R/W	LF_RESISTOR[0]	0
Bit 3	R/W	DIVIDE_RATIO	0
Bit 1	R/W	CHARGE_PUMP[1]	0
Bit 0	R/W	CHARGE_PUMP[0]	1

Register 000FH: Bypass and Loop-across

Bit	Type	Function	
Bit 13	R/W	LBEN_CH1	1
Bit 12	R/W	LBEN_CH0	1
Bit 9	R/W	CHLBEN_CH1	1
Bit 8	R/W	CHLBEN_CH0	1

13.13 Interrupt Service Routine

The CRSU 4x2488 will assert INTB to logic 0 when a condition which is configured to produce an interrupt occurs. To find which condition caused this interrupt to occur, the procedure outlined below should be followed:

1. Read the CRSU 4x2488 Master Interrupt Status registers (0002H – 000AH). The bits point to the functional block(s) which caused the hardware interrupt. For instance, if the Channel 0 RRMP block caused the interrupt, the RRMP_INT_0 bit will be logic 1 in register 0002H. These bits get cleared when the underlying interrupt condition is cleared.

2. Find the register address of the corresponding block which caused the interrupt and read its Interrupt Status registers. The interrupt functional block and interrupt source identification register bits from steps 1 and 2 are cleared once these register has been read and the interrupt(s) identified.

3. Service the interrupt(s).

4. If the INTB pin is still logic 0, then there are still interrupts to be serviced and steps 1 to 3 need to be repeated. Otherwise, all interrupts have been serviced. Wait for the next assertion of INTB.

13.14 Using the Performance Monitoring Features

The performance monitor counters within the different blocks are provided for performance monitoring purposes. The RRMP, RIFD, and SBER all contain performance monitor registers. The counters have been sized to not saturate if polled every second.

Each block's counters can be accumulated independently if one of the registers which contain the latched counter values is written to. A device update of all the counters can be done by writing to the CRSU 4x2488 Global Performance Monitor Update register (register 0000H). After this register is written to, the TIP bit in this register can be polled to determine when all the counter values have been transferred and are ready to be read.

13.14.1 Required Reset Sequence

After digital reset, and before starting any software routines to capture performance monitor count values, a write to register 0x0000 should be executed to initiate a global performance monitor count update. Then, the TIP bit in register 0x0000 should be monitored after 32 REFCLK clock periods. If it is logic 1, a software reset (done by setting and then clearing DRESET for all channels in register 0x0001) should be done to clear a TIP lock-up condition. Repeat this sequence until TIP is read to be logic 0.

If this reset routine is not followed, there is a minute chance that the RRMPs', or RIFDs' performance monitor counters, and the TIP register bit will start up in a lock-up condition and not operate properly.

13.15 Transmit FEC Encoder Error Insertion

This test feature allows errors to be inserted into the Transmitted SONET Frame by the inversion of up to four bytes in each row of each frame. Individual bits cannot be inverted, only full bytes. Overall control is provided by the INJECT bit, Register 1041H bit 4. Setting the INJECT to logic ‘1’ will force the FEC encoder to inject the errors defined by the INSERT_ROW[3:0] register 1042H, and PARAM_A_n[10:0] and PARAM_B_n[1:0] registers 1042H, 1043H, 1044H and 1045H, into the row specified by INSERT_ROW[3:0] bits register 1041H. The INJECT bit can be polled and when set to logic ‘0’, the FEC Encoder can be programmed to inject the next desired error. The INJECT bit clears on the last clock cycle of the row prior to the row specified by INSERT_ROW[3:0] bits, so an entire row-time is available to poll and re-program the host programmable registers 1041H through 1045H. One row time is given by the formula:

1080 clock cycles / 77.76 * 5 = 69 Register read/write cycles @ 20 MHz.

Each of the host programmable TIFE Error Insertion Registers specifies a single byte error with an enable, INSERT_EN_n at bit 15 of each register. If INSERT_EN_n is set to logic '1', then the byte defined by INSERT_ROW[3:0], PARAM_A_n[10:0], and PARAM_B_n[1:0] will be inverted when INJECT is set to logic ‘1’. The TIFE Error Insertion Registers must all be written before writing INJECT with logic ‘1’, and not written again until INJECT is read as logic ‘0’. Setting any of the INSERT_EN_n to logic ‘0’ turns off the error insertion for that TIFE Error Insertion Register.

To invert byte K of row P, one of host TIFE Error Injection Registers must be written such that

- PARAM_A_n = (((K-1) mod 16) mod 4) + 4* ((K-1) div 16).
- PARAM_B_n = 3-((K-1) mod 16) div 4.

Where 4320 <= K <= 1 and 8 <= P <= 0. The results of the above formulas must be converted to Hexadecimal form before being written to the PARAM_A_n[10:0] and PARAM_B_n[1:0] fields.

With this write complete, TIFE Control Register 1041H, must be written such that

- INSERT_ROW[3:0] = P-1
- INJECT = ‘1’.

Alternatively, bytes in an STS-N (N = 48) frame can be defined by the vector S (A, B, C) where A (1 to 9) represents the row number, B (1 to 90 * 3) represents a multi-column number and C (1 to N / 3) represents the depth of interleave within the multi-column. For example, the first A2 byte in row 1 of an STS-48 frame has the number S (1,4,1), while the last A2 byte has the number S (1,6,16).

To invert byte S (A, B, C), one of the TIFE Error Insertion registers must be written such that

- PARAM_A_n = ((C-1) mod 4) + 4 * (B-1).
- PARAM_B_n = (C-1) div 4.

The results of the above formulas must be converted to Hexadecimal form before being written to the PARAM_A_n[10:0] and PARAM_B_n[1:0] fields.

With this write complete, TIFE Control Register 1041H must be written such that

- INSERT_ROW[3:0] = A-1
- INJECT = '1'.

As an example, the following will invert bytes 8,9,10 of row 5; inverting byte 24 is disabled.

Register Number	Register Value (Binary)	Field Value (Hex)
1041H	1 000000 0000 10100	HS_EN asserted, INJECT asserted, INSERT_ROW = 4
1042H	00 000000000000 00	INSERT_EN_0 = 0, PARAM_A_0 = 7, PARAM_B_0 = 1
1043H	10 000000000001 01	INSERT_EN_0 = 1, PARAM_A_1 = 3, PARAM_B_0 = 1
1044H	10 000000000010 01	INSERT_EN_0 = 1, PARAM_A_2 = 0, PARAM_B_0 = 2
1045H	10 000000000011 01	INSERT_EN_0 = 1, PARAM_A_3 = 1, PARAM_B_0 = 2

14 Board Design Recommendations

The following documents provide a useful reference for design recommendations:

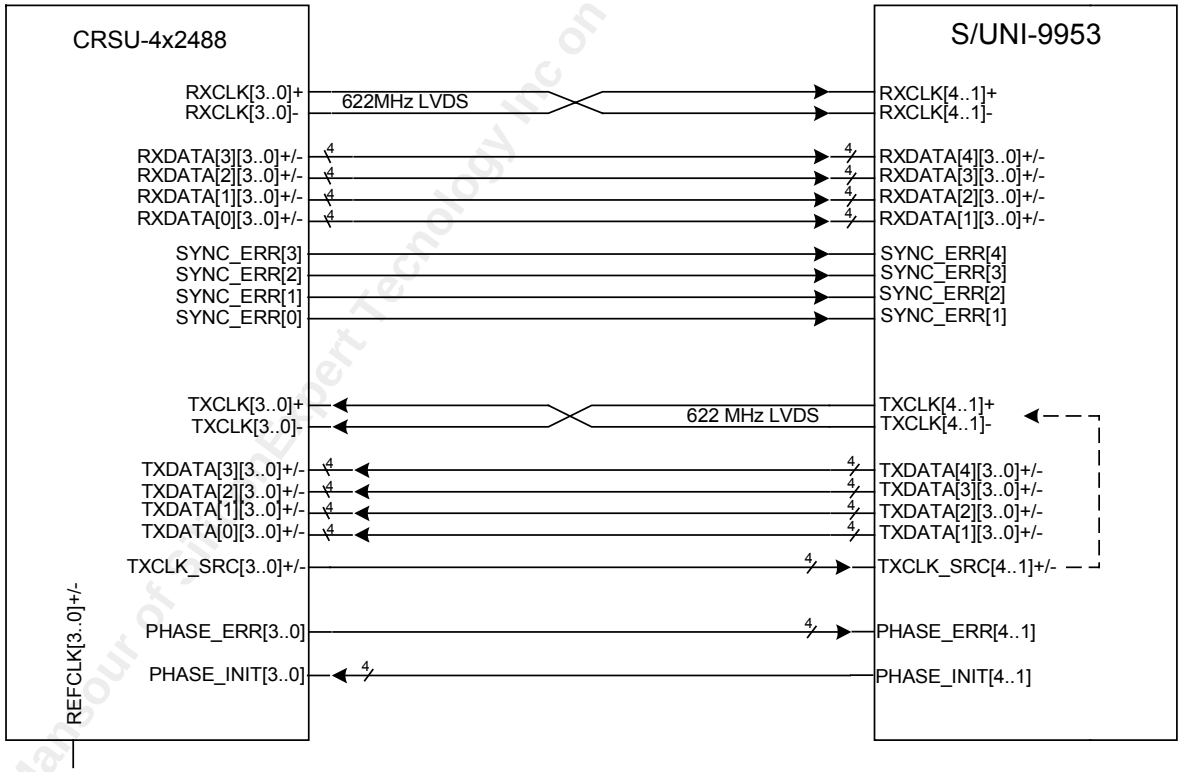
- 16xOC-48 Line Card-Reference Design issue 1 (PMC-2010469)
- Signal Integrity for PMC-Sierra 3.125/2.488/1.5GBIT/S Links (PMC-2010750)

14.1 Interfacing the CRSU 4x2488 to the S/UNI-9953 or SPECTRA-9953

The QSFI-4 Slave interface on the S/UNI-9953 and SPECTRA-9953 devices supports both a single channel OC-192 or a four channel OC-48 SERDES interface. In 4xOC-48 mode, the 16 bit data bus is separated into four separate busses, 4 bits wide. All clocking signals are provided for each channel and each interface operates independently of one another.

The CRSU 4x2488 device can be directly connected to the S/UNI-9953 without any additional logic. Figure 17 shows the connections for this interface.

Figure 17 CRSU 4x2488 to S/UNI-9953 Interface



In this application the interface connections are identical to the OC-192 configuration except that there are four independent four bit wide interfaces. The clock and control signals are dedicated for each channel.

Please note the signal numbering differences between the CRSU 4x2488 QSFI-4 interface and the S/UNI-9953 (or SPECTRA-9953) interface. Bit 3 on the CRSU should be wired to Bit 4 on the S/UNI-9953; 2 to 3 and so on as shown in Figure 17.

14.2 Power Supplies

14.2.1 QSFI-4 Interface Power Supply Decoupling Recommendations

The power supply decoupling recommendations for the CRSU 4x2488 are provided in the PMC-Sierra Applications note: Power Supply Filtering Recommendations for the 10G Chess Devices, PMC-2011065, Issue 1, July 11, 2001.

14.2.2 2.488 GHz Line Side Power Supply Decoupling Recommendations

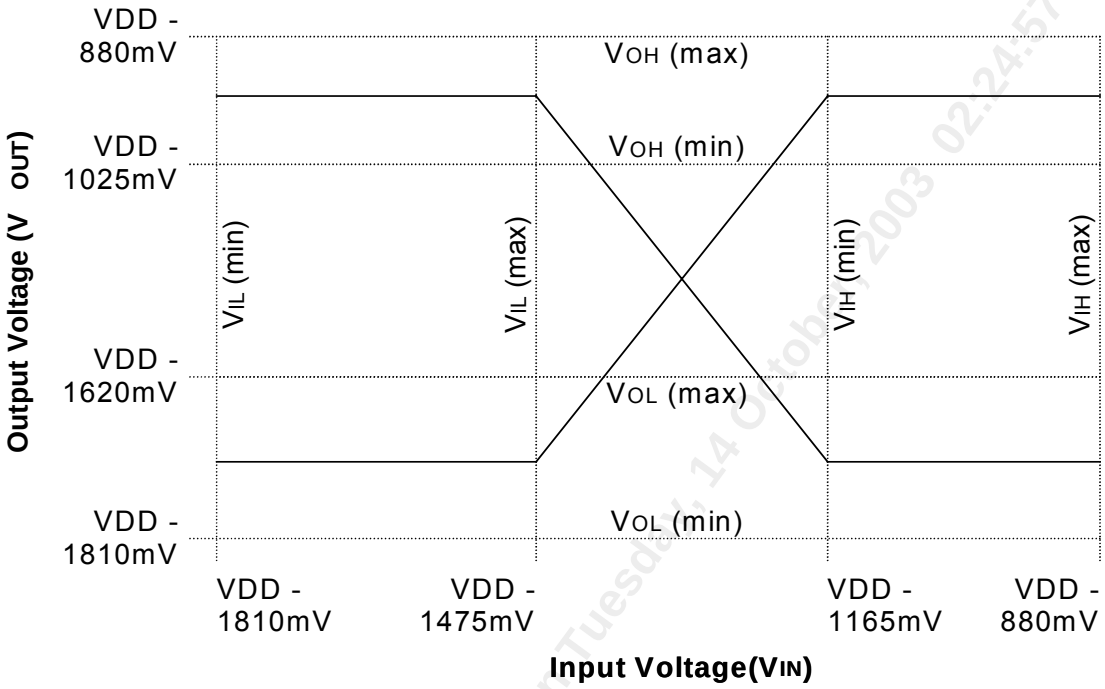
The power supply decoupling recommendations for the CRSU 4x2488 are provided in the PMC-Sierra Applications note: Power Supply Filtering Recommendations for the 10G Chess Devices, PMC-2011065, Issue 1, July 11, 2001.

14.3 Interfacing to ODL Devices

14.3.1 Output Levels

The CRSU 4x2488 is targeting for CML compatible input and output level characteristics. The CRSU 4x2488 generates outputs which have approximately 2/3rd of 100k ECL/PECL swing, but are compatible with the requirements of most Optical Modules as shown in Table 17. Figure 18 shows DC ECL/PECL output levels and their limits. We see that output levels are referenced to a positive power supply, VDD (VDD=0V for ECL and is typically 2.5V, 3.3V or 5V for PECL). Therefore, regardless of the value of VDD, the typical value of VOH is required to be 952.5 mV below VDD and the typical value of VOL is required to be an additional 762.5 mV below that.

Figure 18 PECL Levels (100K Characteristics)



There are no hard specifications for CML, but the signal swing is typically about half that of the ECL/PECL levels (≈800mVppd[1] - the signal swing and common mode depend on the resistor size, amount of current and the positive voltage supply). The lower pulse amplitudes lead to lower cross talk, EMI and noise transients. Thus each device that claims CML compatibility must be looked at carefully to insure interoperability with other devices.

Table 17 compares the CRSU 4x2488 Rx and Tx signal levels a few ODLs (note ODL Rx's connect to CRSU 4x2488 Rx's and ODL Tx's connect to CRSU 4x2488 Tx's).

Table 17 CRSU 4x2488 and ODL Amplitudes

Device	Min	Typ.	Max
Standard ECL/PECL levels	1.19Vppd	1.525Vppd	1.86Vppd
Typical CML levels		800mVppd	
CRSU 4x2488 Tx (standard output amplitude[1])	900mVppd	1000mVppd	1100mVppd
CRSU 4x2488 Tx (low output amplitude[2])	465mVppd	533mVppd	600mVppd
CRSU 4x2488 Rx	400mVppd[3]		2Vppd

[1] Vppd: Peak-to-peak differential voltage (typically equals 2 x single-ended peak-to-peak).

Device	Min	Typ.	Max
Lucent Tx (1417K4A)	300mVppd	-	1.6Vppd
Lucent Rx (1417K4A)	600mVppd	-	1Vppd
Sumitomo Tx SDM-7128-XC	900mVppd	-	2.4Vppd
Sumitomo Rx SDM-7128-XC	400mVppd	-	2.3Vppd
Sumitomo Tx SCM-6028-XL	0.8Vppd	-	2Vppd
Sumitomo Rx SCM-6028-XL	400mVppd	-	2.3Vppd
HP HFCT-Tx HFCT-5404D	400mVppd	-	1.8Vppd
HP HFCT-Rx HFCT-5404D	600mVppd	-	No Spec
Hatachi Tx HTR6540	300mVppd		1.2Vppd
Hatachi Rx HTR6540	640mVppd	800mVppd	1.0Vppd

Notes:

1. TXLI Control/Status Register 10A0H,12A0H,14A0H and 16A0H, Bit 6 = '0' (default)
2. TXLI Control/Status Register 10A0H,12A0H,14A0H and 16A0H, Bit 6 = '1'
3. Jitter tolerance will be compromised at input amplitudes below the minimum specified. Thus going below this limit is not recommended.

As can be seen, the CRSU 4x2488 Tx must be correctly programmed (in general the reduced Tx output amplitude should be used, (register 10A0 bit 6 channel 0)) to be able to inter-operate with the ODLs. Some ODLs claim to be able to tolerate Tx PECL levels, but this will limit their Rx optical range, thus for best operation care must be taken to insure the correct levels are sent to the ODL.

14.3.2 Termination Scheme

The CRSU 4x2488 is to be AC coupled and double terminated, see Figure 19 to Figure 21 below for several connects. Note that while the CRSU 4x2488 could be DC coupled to a 3.3V CML ODL on the Tx side, **it has not been tested, thus is <u>NOT</u> recommended.**

Figure 19 CRSU 4x2488 Tx Termination Scheme #1

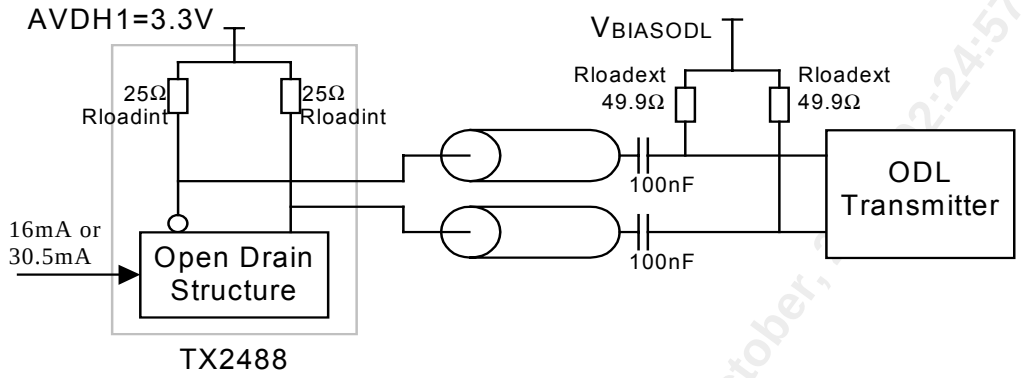


Figure 20 CRSU 4x2488 Tx Termination Scheme #2

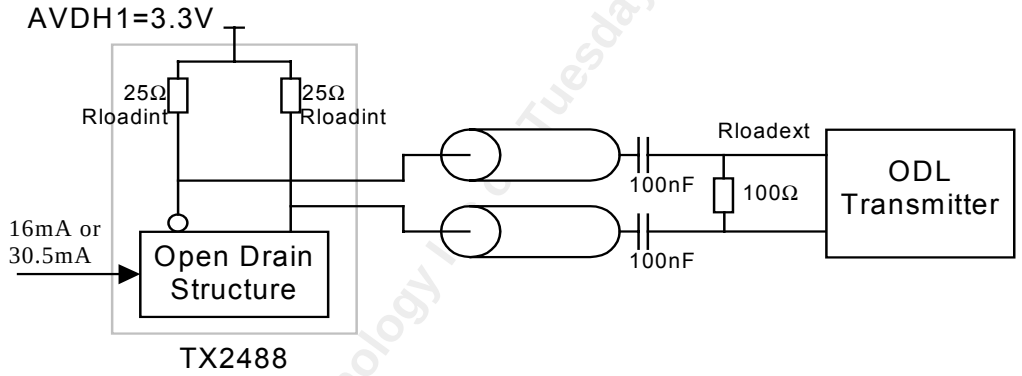
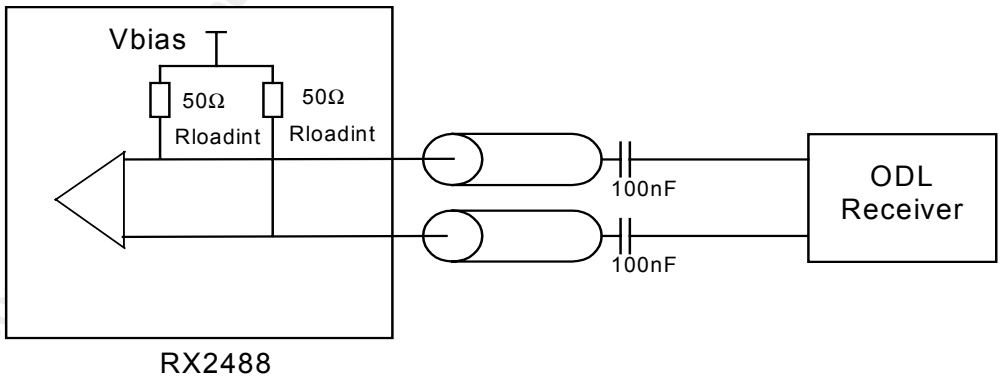


Figure 21 CRSU 4x2488 Rx Termination Scheme



15 Functional Timing

15.1 QSFI-4 Interface Timing

This section shows *the* functional relationship between inputs and outputs. No propagation delays are shown.

The CRSU 4x2488 contains four independent 622 MHz (nominal) interfaces to transfer the line data to an external Framer. Source synchronous timing is used in both directions. The serial data received on the line side spread out across four lines on the QSFI-4 interface. The most significant bit received on the line side is transferred by the most significant bit (bit 3) of the quarter mode QSFI-4 data bus. Figure 22 shows the relationship between the data received on the line interface and the data sent on the QSFI-4 RXDATA interface.

Figure 22 Receive Side Timing Diagram

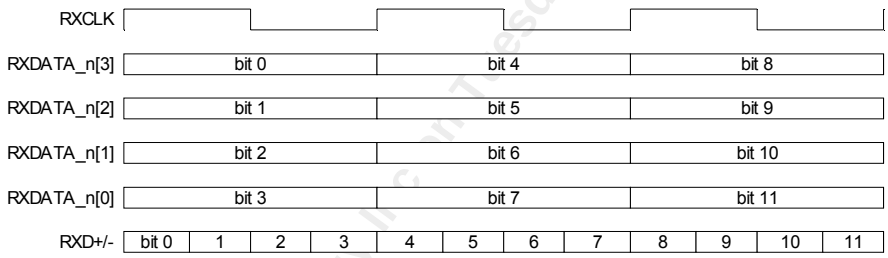
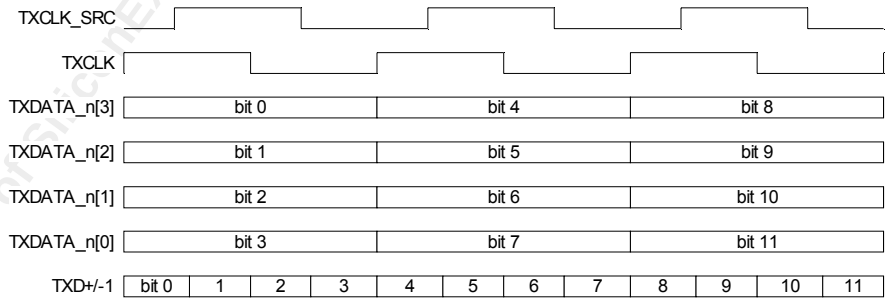


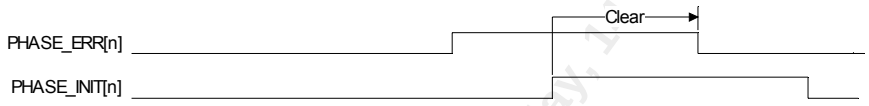
Figure 23 shows the relationship between the data received on the QSFI-4 TXDATA bus the data transmitted on the line interface.

Figure 23 Transmit Side Timing Diagram



Two signals are used to control the operation of the QSFI-4 interface: PHASE_INIT[n] and PHASE_ERR[n]. The PHASE_ERR[n] is used to indicate that state of the CRSU 4x2488 internal QSFI-4 Transmit FIFO. When PHASE_ERR is active it indicates that the FIFO as under flowed or overflowed. The error condition is caused by the a difference in frequency between the TXCLK_SRC and the TXCLK. When the frequency difference is within specifications the framer can indicate this by pulsing PHASE_INIT[n] high for 5 microseconds. Assertion of PHASE_INIT will hold read and write pointers to the same fifo address, allowing read and write operations. Deassertion of PHASE_INIT will allow the write and read pointer to advance with a buffer zone between read and write locations. The PHASE_ERR[n] is cleared by the assertion of the PHASE_INIT[n] signal. Figure 24 shows the relationship between the PHASE_ERR[n] signal and the PHASE_INIT[n].

Figure 24 QSFI-4 Error Indication Timing Diagram



16 Absolute Maximum Ratings

Maximum rating are the worst case limits that the device can withstand without sustaining permanent damage. They are not indicative of normal mode operation conditions.

Table 18 Absolute Maximum Ratings

Specification	Minimum	Maximum	Notes
Storage Temperature	-40°C	+125°C	
3.3 V Supply Voltage (V_{DDO}, V_{AVDH}, V_{QAVD})	VDDI-0.5	4.2V	
1.8 V Supply Voltage (V_{DDI}, V_{AVDL})	-0.5V	2.2V	
Voltage on Any Digital Pin	-0.5V	V_{DDO}+0.5V	
Voltage on Any LVDS Pin	-0.5V	V_{AVDH}+0.5V	
Voltage on any PECL/CML Compatible Pin	-0.5V	V_{AVDH} + 0.5V	
Static Discharge Voltage	-1000 V	+1000 V	
Latch-Up Current	-100 mA	+100 mA	
DC Input Current	-20 mA	+20 mA	
Maximum Overshoot on Output pins	-2V	VDDO + 2V	1 and 2
Input pad overshoot tolerance	-2V	VDDO + 2V	1 and 2
Lead Temperature		+225°C	
Absolute Maximum Junction Temperature Under bias (correct operation not necessarily guaranteed)	-40°C	+125°C	

Notes

1. Most output pins require termination circuitry.
2. Overshoot duration is 10ns at 100 mA Max.

17 Power Information

17.1 Power Requirements

Table 19 Power Requirements

Conditions	Parameter	Typ[1,3]	High[4]	Max[2]	Units
SERDES Mode (default mode) KILL_RX_CLK[3:0] = 1 KILL_TX_CLK[3:0] = 1 KILL_RRMP_CLK = 1 KILL_RIFD_CLK = 1 RX_BYPASS = 1 TX_BYPASS = 1 ANALOG_QSFI-4_ENB = 0	IDDOP (1.8V)	1.803	—	2.457	A
	IDDOP (3.3V)	0.472	—	0.565	A
	Total Power	4.804	5.563	—	W
PMON Mode KILL_RX_CLK[3:0] = 0 KILL_TX_CLK[3:0] = 0 KILL_RRMP_CLK = 0 KILL_RIFD_CLK = 0 RX_BYPASS = 0 TX_BYPASS = 0 ANALOG_QSFI-4_ENB = 0	IDDOP (1.8V)	2.495	—	3.403	A
	IDDOP (3.3V)	0.487	—	0.585	A
	Total Power	6.099	7.086	—	W
PMON only KILL_RX_CLK[3:0] = 0 KILL_TX_CLK[3:0] = 0 KILL_RRMP_CLK = 0 KILL_RIFD_CLK = 1 RX_BYPASS = 1 TX_BYPASS = 0 ANALOG_QSFI-4_ENB = 0	IDDOP (1.8V)	1.990	—	2.712	A
	IDDOP (3.3V)	0.466	—	0.558	A
	Total Power	5.119	5.936	—	W
REGENERATOR Mode KILL_RX_CLK[3:0] = 0 KILL_TX_CLK[3:0] = 0 KILL_RRMP_CLK = 0 KILL_RIFD_CLK = 1 RX_BYPASS = 0 TX_BYPASS = 0 ANALOG_QSFI-4_ENB = 1	IDDOP (1.8V)	1.391	—	1.896	A
	IDDOP (3.3V)	0.332	—	0.397	A
	Total Power	3.599	4.172	—	W
REGENERATOR Mode **Sonet Bypass** KILL_RX_CLK[3:0] = 1 KILL_TX_CLK[3:0] = 1 KILL_RRMP_CLK = 1 KILL_RIFD_CLK = 1 RX_BYPASS = 1 TX_BYPASS = 1 ANALOG_QSFI-4_ENB = 1	IDDOP (1.8V)	0.899	—	1.225	A
	IDDOP (3.3V)	0.328	—	0.393	A

Conditions	Parameter	Typ[1,3]	High[4]	Max[2]	Units
	Total Power	2.700	3.115	—	W
REGENERATOR Mode	IDDOP (1.8)	1.000	—	1.363	A
PMON ONLY	IDDOP (3.3V)	0.327	—	0.391	A
KILL_RX_CLK[3:0] = 0	Total Power	2.879	3.326	—	W
KILL_TX_CLK[3:0] = 1					
KILL_RRMP_CLK = 0 KILL_RIFD_CLK = 1 RX_BYPASS = 1 TX_BYPASS = 1 ANALOG_QSFI-4_ENB = 1					

Notes

1. Typical IDD values are calculated as the mean value of current under the following conditions: typically processed silicon, nominal supply voltage, T_J=60 °C, outputs loaded with 30 pF (if not otherwise specified), and a normal amount of traffic or signal activity. These values are suitable for evaluating typical device performance in a system
2. Max IDD values are currents guaranteed by the production test program and/or characterization over process for operating currents at the maximum operating voltage and operating temperature that yields the highest current (including outputs loaded to 30 pF, unless otherwise specified)
3. Typical power values are calculated using the formula:

   Power = ∑i(VDDNomi x IDDTypi)

   Where i denotes all the various power supplies on the device, VDDNomi is the nominal voltage for supply i, and IDDTypi is the typical current for supply i (as defined in note 1 above). These values are suitable for evaluating typical device performance in a system
4. High power values are a “normal high power” estimate and are calculated using the formula:

   Power = ∑i(VDDMaxi x IDDHighi)

   Where i denotes all the various power supplies on the device, VDDMaxi is the maximum operating voltage for supply i, and IDDHighi is the current for supply i. IDDHigh values are calculated as the mean value plus two sigmas (2σ) of measured current under the following conditions: T_J=105° C, outputs loaded with 30 pF (if not otherwise specified). These values are suitable for evaluating board and device thermal characteristics

17.2 Power Sequencing

Due to ESD protection structures in the pads it is necessary to exercise caution when powering a device up or down. ESD protection devices behave as diodes between power supply pins and from I/O pins to power supply pins. Under extreme conditions, incorrect power sequencing may damage these ESD protection devices or trigger latch up.

The recommended power supply sequencing is as follows:

1. VDDO power must be supplied either before VDDI or simultaneously with VDDI.

2. AVDH can be applied either before or after VDDO, but must be applied either before or simultaneously with VDDI and AVDL. In operation, the differential voltage measured between AVDH supplies and VDDO_DC must be less than 0.5 volt. The relative power sequencing of the multiple AVDH power supplies is not important.

3. AVDL must be applied after AVDH and VDDO, and either before or after VDDI. Or, AVDL can be applied simultaneously with VDDO, AVDH, and VDDI.

4. I/Os get driven after all the supplies have been powered. Otherwise, the I/Os must be current limited to 20 mA.

5. Power down the device in the reverse sequence.

18 D.C. Characteristics

T_a = -40°C to T_j = +125°C, V_{DD} = $VDD_{typical}$ ± 5%
(Typical Conditions: T_A = 25°C, V_{DDI} = 1.8V, V_{DDO} = 3.3V, V_{AVDH} = 3.3V, V_{AVDL} = 1.8V, V_{QAVD} = 3.3V)

Table 20 D.C. Characteristics (CMOS/TTL)[1]

Symbol	Parameter	Min	Typ	Max	Units	Conditions
VDDI	Power Supply	1.71	1.8	1.89	Volts	
VDDO	Power Supply	3.14	3.3	3.47	Volts	
VAVDH	Power Supply	3.14	3.3	3.47	Volts	
VAVDL	Power Supply	1.71	1.8	1.89	Volts	
VQAVD	Power Supply	3.14	3.3	3.47	Volts	
VIL	Input Low Voltage	-0.5	-	0.8	Volts	Guaranteed Input Low voltage. V_{OUT} <= $V_{OL(max)}$. Note 2.
VIH	Input High Voltage	2.0	-	V_{DDO}+0.5V	Volts	Guaranteed Input High voltage. V_{OUT} >= $V_{OH(min)}$. Note 3.
VOL	Output or Bi-directional Low Voltage		-	0.2	Volts	Guaranteed output Low voltage at $V_{DDO} = V_{min}$, VI = V_{IL} and IOL= 100 uA
			-	0.4	Volts	Guaranteed output Low voltage at $V_{DDO} = V_{min}$, VI = V_{IL} and IOL= 1 mA
			-	0.6	Volts	Guaranteed output Low voltage at $V_{DDO} = V_{min}$, VI = V_{IL} and IOL= 2 mA
VOH	Output or Bi-directional High Voltage	2.9	-		Volts	Guaranteed output High voltage at $V_{DDO} = V_{min}$, VI = V_{IH} and IOH= 100 uA
		2.4	-		Volts	Guaranteed output High voltage at $V_{DDO} = V_{min}$, VI = V_{IH} and IOH= 1 mA
		1.9	-		Volts	Guaranteed output High voltage at $V_{DDO} = V_{min}$, VI = V_{IH} and IOH= 2 mA
VT+	Reset Input High Voltage	2.2	-	-	Volts	Applies to RSTB and TRSTB only.
VT-	Reset Input Low Voltage	-	-	0.8	Volts	Applies to RSTB and TRSTB only.
VTH	Reset Input Hysteresis Voltage	-	0.5	-	Volts	Applies to RSTB and TRSTB only.
IILPU	Input Low Current	+20	+83	+200	µA	VIL = GND. Notes 4 and 6.

Symbol	Parameter	Min	Typ	Max	Units	Conditions
IIHPU	Input High Current	-10	0	+10	µA	VIH = VDD. Notes 4 and 6.
IIL	Input Low Current	-10	0	+10	µA	VIL = GND. Notes 5 and 6.
IIH	Input High Current	-10	0	+10	µA	VIH = VDD. Notes 5 and 6.
VICM	LVDS Input Common-Mode Range	0		2.4	V	
|VIDM|	LVDS Input Differential Sensitivity	20		100	mV	
RIN	LVDS Differential Input Impedance	85	100	115	Ω	
VODM	LVDS Output Differential Voltage (single-ended output voltage p-p)	250	425	600	mV	RLOAD=100Ω ±1% Note 11.
VOCM	LVDS Output Common-Mode Voltage	1125	1200	1275	mV	RLOAD=100Ω ±1%
|ΔVODM|	Change in |VODM| between “0” and “1”			25	mV	RLOAD=100Ω ±1%
ΔVOCM	Change in VOCM between “0” and “1”			25	mV	RLOAD=100Ω ±1%
ISP, ISN	LVDS Short-Circuit Output Current			10	mA	Drivers shorted to ground
ISPN	LVDS Short-Circuit Output Current			10	mA	Drivers shorted together
VOA, CML	CML Output Amplitude TXLI Control/Status Register, Bit 6 = ‘0’ (default)	0.90	1.0	1.1	Vppd	Differential Peak-to-Peak Voltage (Tx) Min: at -40ºC, VAVDH(min), VAVDL(min) Max: at 125ºC, VAVDH(max), VAVDL(max)
ISPN	TXLI Control/Status Register, Bit 6 = ‘1’	0.704	0.800	0.896	Vppd	
$V_{IA, PECL}$	PECL Input Amplitude	0.4		2.0	Vppd	Differential Peak-to-Peak Voltage (Rx)
CIN	Input Capacitance		5		pF	tA=25°C, f = 1 MHz
COUT	Output Capacitance		5		pF	tA=25°C, f = 1 MHz
CIO	Bi-directional Capacitance		5		pF	tA=25°C, f = 1 MHz

Notes on D.C. Characteristics

1. This table define the thresholds that allows CMOS input pads to be compatible for the TTL input thresholds of the input only pad. See notes (2) and (3)

2. The threshold of logic low is specified as the CMOS's V_{IL} max that is compatible with the TTL's V_{IL} or 0.8V in all cases of V_{DD}.
3. The threshold of logic high is specified as the minimum TTL's V_{IH} or 2V that insure the compatibility with all CMOS's V_{IH} in all cases of V_{DD}.
4. Input pin or bi-directional pin with internal pull-up resistor.
5. Input pin or bi-directional pin without internal pull-up resistor
6. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).
7. Total of the current on all AVDH pins for a single channel, excluding the QSFI-4 interface. To obtain the total current for the device this number must be multiplied by 4. The following signals carry the AVDH current for Channel 0: QAVD, AVDH_CRU_0, AVDH_TX_0 and AVDH_CSU_0.
8. Total of the current on all AVDH_QSFIM pins for the QSFI-4 interface, excluding all line side analog circuitry.
9. Total of the current on all AVDL pins for a single channel, excluding the QSFI-4 interface. To obtain the total current for the device this number would need to be multiplied by 4. The following signal carries all the AVDL current for Channel 0: AVDL_0.
10. Total of the current on all AVDL_ QSFIM pins for the QSFI-4 interface, excluding all line side analog circuitry.
11. This is a subset of the range allowed, since a larger swing is encouraged but not required (OIF99.102.5).

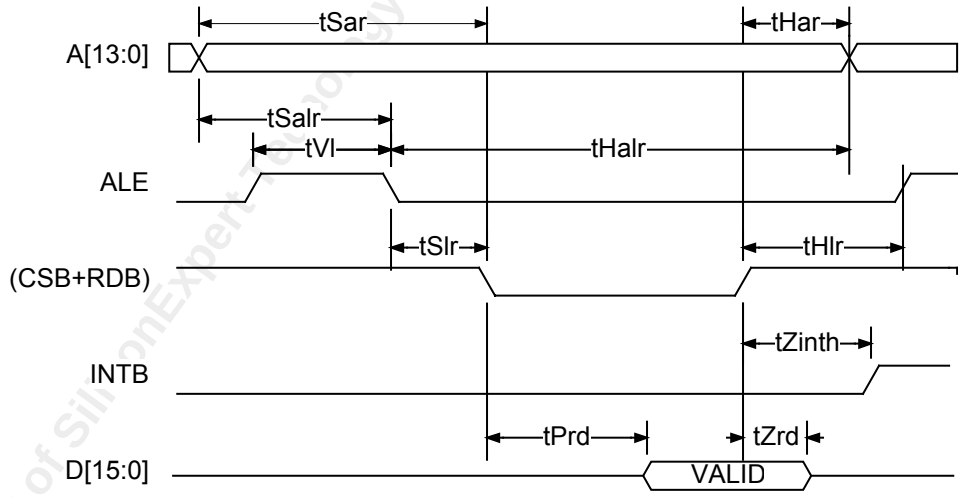
19 A.C. Timing Characteristics

19.1 Microprocessor Interface Timing Characteristics

Table 21 Microprocessor Interface Read Access

Symbol	Parameter	Min	Max	Units
TS_{AR}	Address to Valid Read Set-up Time	10		ns
TH_{AR}	Address to Valid Read Hold Time	5		ns
tS_{ALR}	Address to Latch Set-up Time	10		ns
tH_{ALR}	Address to Latch Hold Time	10		ns
tV_{L}	Valid Latch Pulse Width	5		ns
tS_{LR}	Latch to Read Set-up	0		ns
tH_{LR}	Latch to Read Hold	5		ns
tP_{RD}	Valid Read to Valid Data Propagation Delay		70	ns
tZ_{RD}	Valid Read Negated to Output Tri-state		20	ns
tZ_{INTH}	Valid Read Negated to INTB High		50	ns

Figure 25 Intel Microprocessor Interface Read Timing



Notes on Microprocessor Interface Read Timing

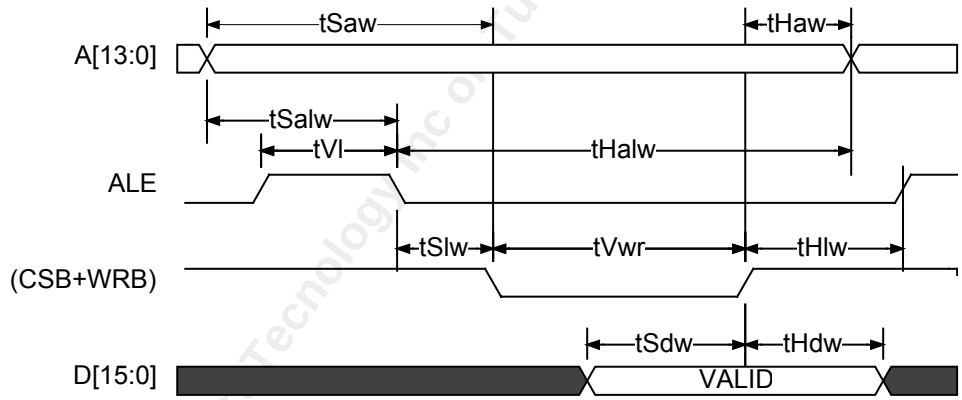
1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[15:0]).
3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.
4. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tS_{ALR}, tH_{ALR}, tV_L, tS_{LR}, and tH_{LR} are not applicable.
5. Parameter tH_{AR} is not applicable if address latching is used.
6. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
7. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

Table 22 Microprocessor Interface Write Access

Symbol	Parameter	Min	Max	Units
tS_{AW}	Address to Valid Write Set-up Time	10		ns
tS_{DW}	Data to Valid Write Set-up Time	25		ns
tS_{ALW}	Address to Latch Set-up Time	10		ns
tH_{ALW}	Address to Latch Hold Time	10		ns
tV_{L}	Valid Latch Pulse Width	5		ns
tS_{LW}	Latch to Write Set-up	0		ns
tH_{LW}	Latch to Write Hold	5		ns
tH_{DW}	Data to Valid Write Hold Time	5		ns
thaw	Address to Valid Write Hold Time	5		ns
tV_{WR}	Valid Write Pulse Width	40		ns

Figure 26 Intel Microprocessor Interface Write Timing



Notes on Microprocessor Interface Write Timing

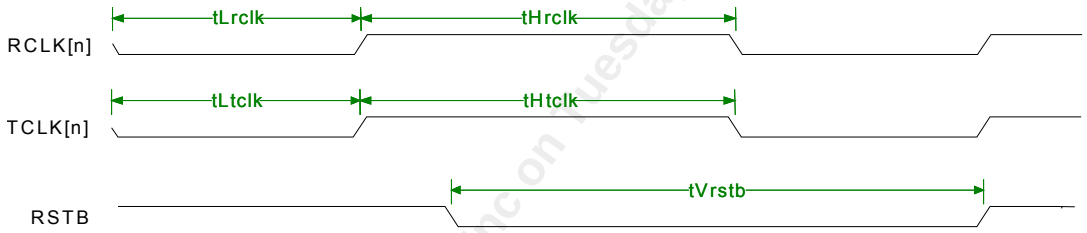
1. A valid write cycle is defined as a logical OR of the CSB and the WRB signals.
2. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tS_{ALW}, tH_{ALW}, tV_{L}, tS_{LW}, and tH_{LW} are not applicable.
3. Parameter tH_{AW} is not applicable if address latching is used.
4. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
5. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt

19.2 Reset Timing

Table 23 System Miscellaneous Timing

Symbol	Description	Min	Typ	Max	Units
$RCLK_{FREQ}$	RCLK Frequency (77.76 MHz Nominal)	62.25		84.375	MHz
$TCLK_{FREQ}$	TCLK Frequency (77.76 MHz Nominal)	62.25		84.375	MHz
tH_{RCLK}, tH_{TCLK}	RCLK high pulse width	0.4*CLK_{FREQ}		0.6*CLK_{FREQ}	
tL_{RCLK}, tL_{TCLK}	TCLK low pulse width	0.4*CLK_{FREQ}		0.6*CLK_{FREQ}	
tV_{RSTB}	RSTB input pulse width	2			ms

Figure 27 System Miscellaneous Timing Diagram Timing

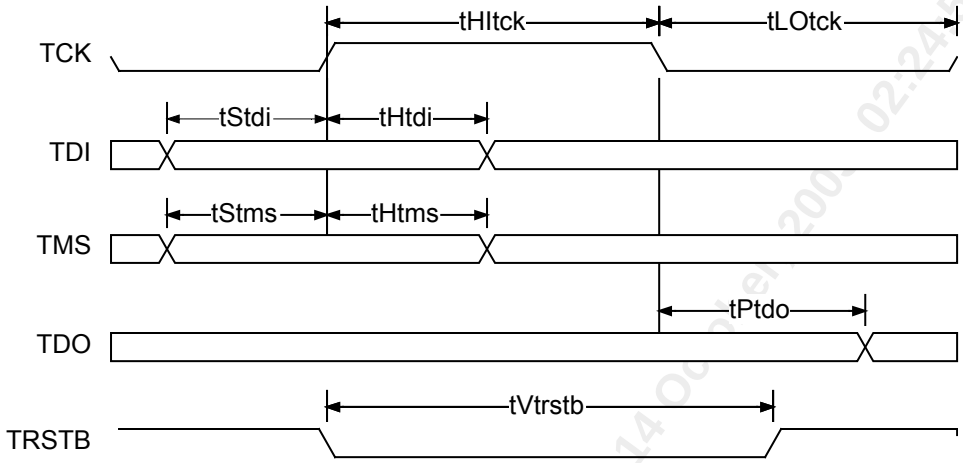


19.3 JTAG Timing

Table 24 JTAG Port Interface (Figure 28)

Symbol	Description	Min	Max	Units
fTCK	TCK Frequency		4	MHz
tHITCK	TCK HI Pulse Width	100		ns
tLOTCK	TCK LO Pulse Width	100		ns
tSTMS	TMS Set-up time to TCK	25		ns
tHTMS	TMS Hold time to TCK	25		ns
tSTDI	TDI Set-up time to TCK	25		ns
tHTDI	TDI Hold time to TCK	25		ns
tPTDO	TCK Low to TDO Valid	2	25	ns
tVTRSTB	TRSTB Pulse Width	100		ns

Figure 28 JTAG Port Interface Timing



Notes on Input Timing

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Notes on Output Timing

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Maximum and minimum propagation delays are measured with a 30 pF load.

19.4 QSFI-4 Timing

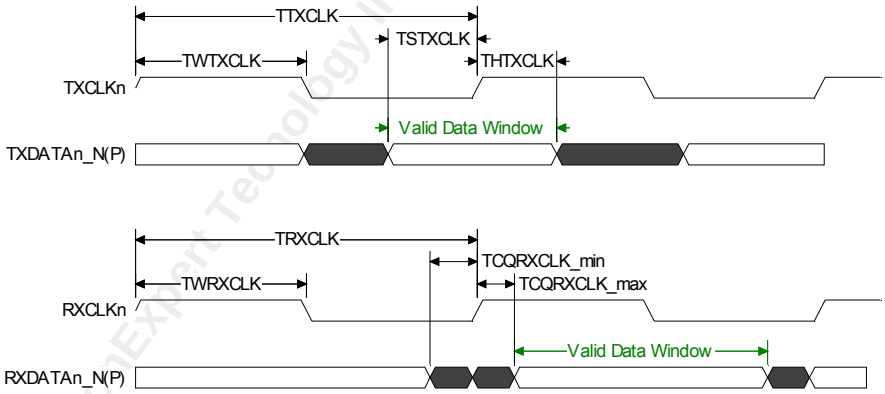
Table 25 QSFI-4 Interface Timing

Symbol	Description	Min	Typ	Max	Units
fTXCLK	TXCLK Frequency (nominally 622.08MHz)	600		675	MHz
TTXCLK	TXCLK period (nominally 1.608 ns)	1.667		1.481	ns
TWTXCLK	TXCLK duty cycle (TH_TXCLK/TL_TXCLK)	40		60	%
TR	rise time (20%-80%). Note 1	100		250	ps
TF	fall time (20%-80%). Note 1	100		250	ps
TSTXCLK	TXDATA Setup time	300			ps
THTXCLK	TXDATA hold time	300			ps
fRXCLK	RXCLK Frequency (nominally 622.08MHz)	600		675	MHz
TRXCLK	RXCLK period (nominally 1.608 ns)	1.667		1.481	ns
TWRXCLK	RXCLK duty cycle (TH_RXCLK/TL_RXCLK)	45		55	%
TCQRXCLK	RXDATA propagation delay	-200		200	ps

QSFI-4 Interface Timing Notes

1. txclk, rxclk, txdata and rxdata rise and fall time driving a 1pf capacitive load.

Figure 29 QSFI-4 Master Interface Timing



19.5 OC-48 Interface Timing Characteristics

Table 26 OC-48 Interface Timing

Symbol	Description	Min	Typ	Max	Units
Frefclk	Required frequency for REFCLK_P and REFCLK_N inputs (Bellcore spec for +/- 20ppm clock sources. STS-48/STM-16); all conditions. Note 1	155.517	155.52	155.523	MHz
Tref, rise	Rise time for REFCLK_P and REFCLK_N inputs; all conditions	-	-	1	ns
Tref, fall	Fall time for REFCLK_P and REFCLK_N inputs; all conditions	-	-	1	ns
DCref	Duty Cycle for REFCLK_P and REFCLK_N inputs; all conditions	45	50	55	%
Tref_rms_jit	RMS Jitter acceptable on REFCLK_P and REFCLK_N inputs (12KHz – 20MHz jitter band) to meet SONET jitter generation spec; all conditions	-	-	1	ps
Tref_pk_jit	Peak-to-Peak Jitter acceptable on REFCLK_P and REFCLK_N inputs (12KHz – 20MHz jitter band) to meet SONET jitter generation spec; all conditions	-	-	10	ps
rb	Bit rate for OC-48 compatible transmit and receive data		2.48832 = 16 x Frefclk		Gb/s
Jrms	Output RMS jitter (12kHz to 20MHz).		0.007	0.008	UI

OC48 Interface Timing Notes

1. CSU can enter a lock up condition if reference clock is interrupted. A CSU or hardware reset will be required to exit this condition. CSU lock up condition can be confirmed if register 10A0H: TXLI Control/Status (for channel 0) bit 1, ROOL_V is logic 1. To apply a channel 0 CSU reset assert register 10A1 bit 13 to logic 1 for several hundred milliseconds, then back to logic 0. Read reference out of lock status register 10A0 bit 1 that ROOL_V is logic 0 for correct operation.

20 Ordering Information

Table 27 Ordering Information

PART NO.	DESCRIPTION
PM5395-BI	580-pin Ultra Ball Grid Array (UBGA)

21 Thermal Information

This product is designed to operate over a wide temperature range when used with a heat sink and is suited for outside plant equipment[1].

Table 28 Outside Plant Thermal Information

Maximum long-term operating junction temperature (T_J) to ensure adequate long-term life.	105°C
Maximum junction temperature (T_J) for short-term excursions with guaranteed continued functional performance[2]. This condition will typically be reached when the local ambient temperature reaches 85°C.	125°C
Minimum ambient temperature (T_A)	-40°C

Table 29 Device Compact Model[3]

Junction-to-Case Thermal Resistance, θ_{JC}	0.13°C/W
Junction-to-Board Thermal Resistance, θ_{JB}	3.6°C/W

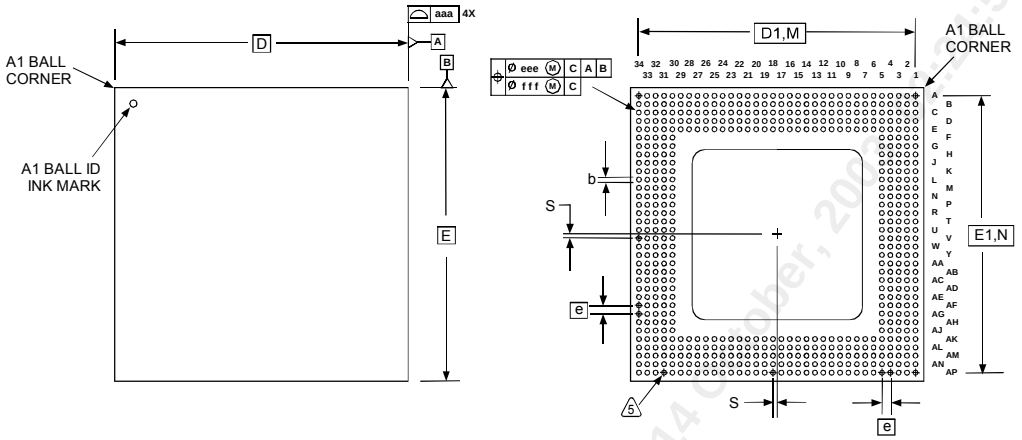
Table 30 Heat Sink Requirements

$\theta_{SA}+\theta_{CS}$[4]	The sum of θ_{SA} + θ_{CS} must be less than or equal to: $[(105 - T_A) / P_D] - \theta_{JC}]$ °C/W where: T_A is the ambient temperature at the heat sink location P_D is the operating power dissipated in the package
	θ_{SA} and θ_{CS} are required for long-term operation

Notes

1. Short-term is understood as the definition stated in Bellcore Generic Requirements GR-63-Core
2. $\Theta_{JC,}$ the junction-to-case thermal resistance is a measured nominal value + 2 sigma. Θ_{JB}, the junction-to-board thermal resistance is obtained by simulating conditions described in JEDEC Standard, JESD 51
3. Θ_{SA} is the thermal resistance of the heat sink to ambient. Θ_{CS} is the thermal resistance of the heat sink attached material
4. The actual ΘSA required may vary according to the air speed at the location of the device in the system with all the components in place

22 Mechanical Information



NOTES: 1) ALL DIMENSIONS IN MILLIMETER.
2) DIMENSION aaa DENOTES PACKAGE BODY PROFILE.
3) DIMENSION bbb DENOTES PARALLEL.
4) DIMENSION ddd DENOTES COPLANARITY.
5) DIAMETER OF SOLDER MASK OPENING IS 0.45 +/- 0.025 MM (SMD).

PACKAGE TYPE : 580 THERMALLY ENHANCED BALL GRID ARRAY - UBGA																
BODY SIZE : 35 x 35 x 1.47 MM																
Dim.	A	A_1	A_2	D	D_1	E	E_1	M,N	b	e	aaa	bbb	ddd	eee	f f f	S
Min.	1.32	0.40	0.92	-	-	-	-	-	0.50	-	-	-	-	-	-	-
Nom.	1.47	0.50	0.97	35.00 BSC	33.00 BSC	35.00 BSC	33.00 BSC	34x34	0.63	1.00 BSC	-	-	-	-	-	-
Max.	1.62	0.60	1.02	-	-	-	-	-	0.70	-	0.20	0.25	0.20	0.30	0.10	0.05

Notes