ICs for Communications

PCI Interface for Telephony/Data Applications

PITA-2

PSB 4610 Version 2.2

Preliminary Data Sheet   01.00

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Attention please!

Organization of this Data Sheet

- **Chapter 1, Features**
  Describes the general features of the PITA-2.

- **Chapter 2, Typical Applications with the PITA-2**
  Describes typical applications that can be realized with the PITA-2.

- **Chapter 3, Construction of the PITA-2**
  Shows a block diagram and describes the interfaces and their functions.

- **Chapter 4, Communication with the PITA-2**
  Describes the PCI bus interface of the PITA-2.

- **Chapter 5, Communication with External Components**
  Gives a general description of the local bus interfaces of the PITA-2.

- **Chapter 6, Power Management**
  Describes the power management functions (including D3cold) of the PITA-2.

- **Chapter 7, Reset and Interrupts**
  Describes the requirements for reset and the behaviour of the PITA-2.

- **Chapter 8, Pinning**
  Describes the pins, types of pins and the characteristics of the interfaces.

- **Chapter 9, Electrical Characteristics**
  Describes electrical maximum ratings and electrical characteristics.

- **Chapter 10, Package Outlines**
  Describes the package outlines.

- **Chapter 11, Configuration Space Register of the PITA-2**
  Contains descriptions of the Configuration Space Registers of the PITA-2.

- **Chapter 12, Internal Register of the PITA**
  Contains descriptions of the Internal Registers of the PITA-2.

- **Chapter 13, Abbreviations**
  Describes abbreviations occuring in this data sheet.

- **Chapter 14, Index**

Important Notes about this Data Sheet

What's New?

The organization of the structure follows the guidelines of *Information Mapping*®.

What is *Information Mapping*®?

This is a research based method for the

– analysis
– structure
– presentation

of user-orientated manuals.

Major Changes

Instead of the used chapters with mono causal descriptions you now get

– all information
– for a scope
– under the corresponding heading.

The Intention

This Data Sheet is intended to be

– easily surveyed
– increasingly readable
– customized applicable
– practice-orientated
– offering the quickest possible way to the required information.

Table of Contents

Table of Contents **Page**

Introduction

What is the PITA-2?

The PITA-2 is a cost-effective PCI bridge for industrial and communication applications. It supports dual cards and D3cold power management.

The PITA-2 can be used in

- PCI ISDN cards.

- PCI hardware modems.

- PCI software modems.

- Industrial PCI bridge applications.

Interfaces of the PITA-2

The PITA-2 offers the following interfaces:

Interfaces	to find in
PCI Master/Target Controller	see chapter 4.2 on page 22
Serial DMA Interface	see chapter 5.1 on page 34
Parallel Interface	see chapter 5.2 on page 78

The PITA-2 offers the following interfaces:

Interfaces	to find in
General Purpose I/O Interface	see chapter 5.3 on page 97
SPI EEPROM Interface	see chapter 5.4 on page 115

1 Features

Compliant with

- PC 99 (PCI requirements)
- PCI Bus Specification Version 2.2
- PCI Power Management Specification Version 1.1

Highlights

- Dual Card support (3.3V and 5V signaling environment)
- Extensive Power Management Features (including D3cold)
- Automatic Configuration with Customer Specific Values

Interfaces

- PCI Master Target Interface
  - PCI 2.2 compliant
  - 32 bit
  - 33 MHz
- Serial Interface
  - Supports IOM-2 Modes
  - Supports serial interface to the ALIS chip-set family
  - DMA Controller for serial communication
  - 16 word FIFOs for each direction
- Parallel Interface
  with chip select logic supporting up to three external components
- General Purpose I/O Interface
  with interrupt capability
- SPI^{TM} Interface
  for optional EEPROM

Compatibility

- ALIS V2.1 PSB 4596
- ALIS V3.X PSB 4596
- ISDN IOM-2 Components, e.g.:
  - IEC-Q family
  - SBCX, SBCX-X
- Components consisting of a parallel multiplexed or non multiplexed Intel/ Infineon Interface, e.g:
  - IPAC, IPAC-X
  - ISAC-S, ISAC-SX, ISAC-SX TE

2 Typical Applications with the PITA-2

Overview

Besides all the applications that require only a simple PCI interface there are some applications which the PITA-2 is especially suited for.

Simple applications benefit from the easy configuration of the PITA-2, the extensive power management support and the standard interfaces on the local bus side.

Telecommunication applications (e.g modems) benefit from the integrated master DMA controller as well as the IOM-2/GCI bus interface.

This allows for easy connection of most telecommunications transceivers and substantially reduces the CPU workload.

Furthermore the PITA-2 fully supports D3cold state.

This allows the PC to enter a deep sleep state and still be able to react to an incoming call at the same time.

ISDN-S Interface Application with the IPAC
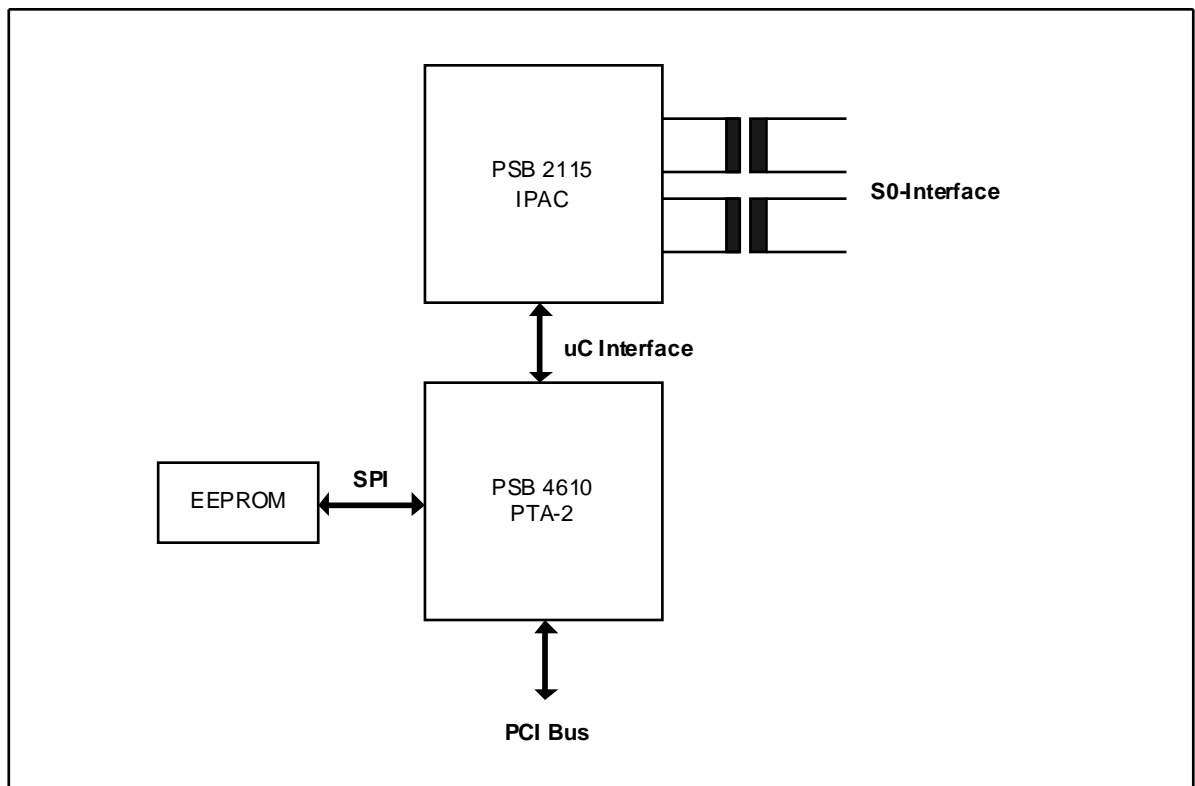
ISDN-U Interface Application with the 3PAC and IEC-Q TE
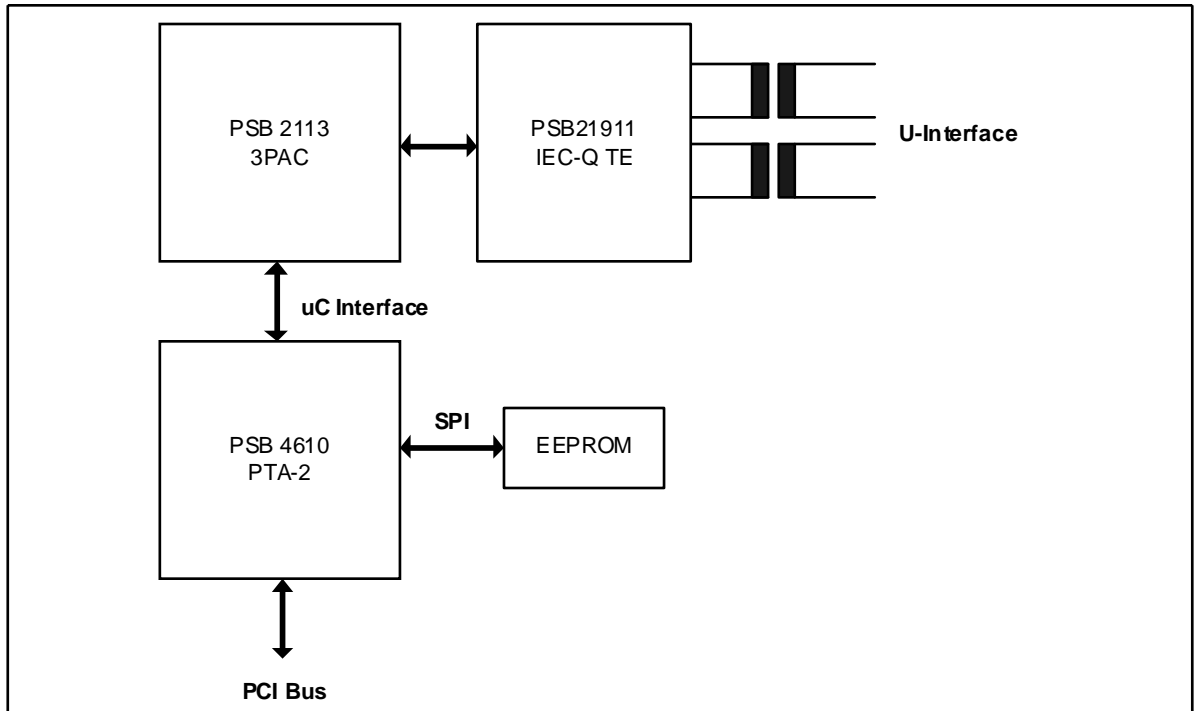
3 Construction of the PITA-2

Overview

The PITA-2 provides a Peripheral Component Interconnect (PCI) bus interface which acts as a bridge between the PCI bus and the different controllers and interfaces:

- The Parallel Interface Control supports up to three external devices.
- The Serial Interface is controlled by the internal DMA Controller; serial communication uses transmit and receive FIFOs.
- The EEPROM for configuration of the PITA-2 and customer specific data storage.
- The General Purpose I/O Interface.

Block Diagram of the PITA-2
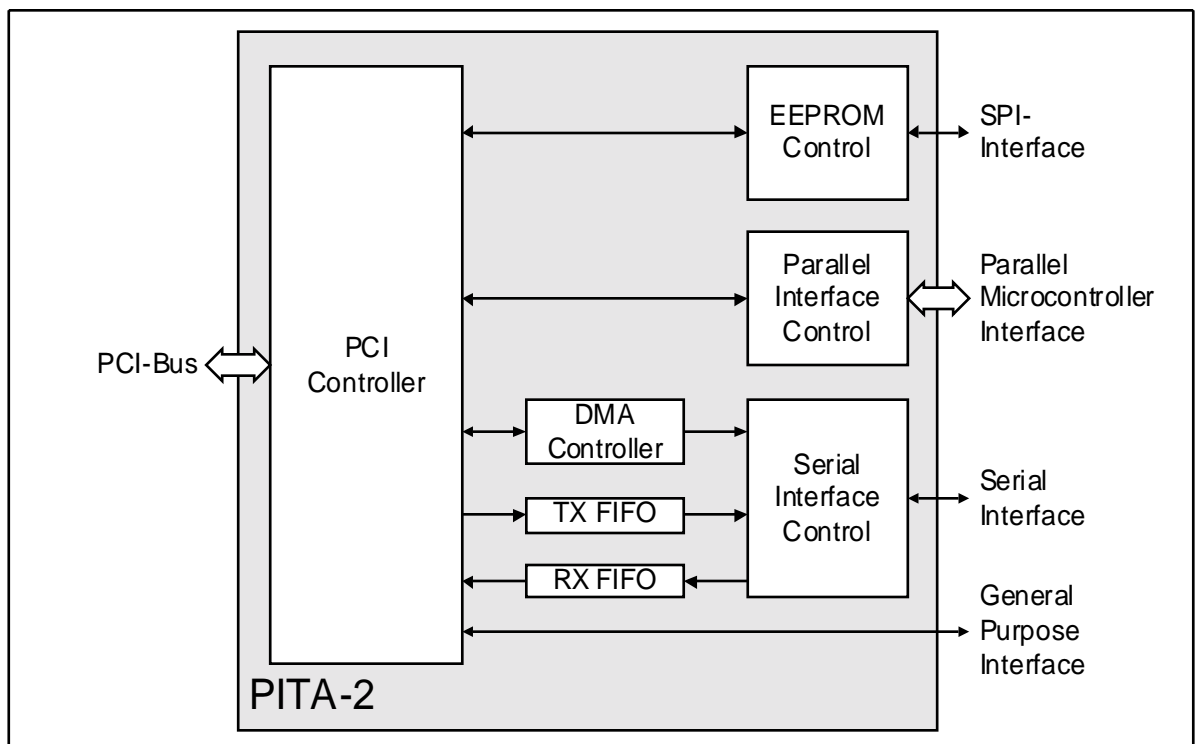
Description of the single Blocks

Name	provides	supports	Notes
PCI Bus Control	• a 32 bit interface at speeds up to 33 MHz • Bus Master DMA capability for data passing through the Serial Interface • Target capability for data passing through the Parallel Interface	• D0 • D1 • D2 • D3hot and D3cold • 5V environment • 3.3V environment • Vaux supply	
Parallel Interface Control		Chips with a Infineon/ Intel Standard Parallel Interface, including: • ISDN devices • Modems DSPs • Industrial devices	Three prede-coded chip sel-ect lines Can be used for pinstrap-ping the subsy-stem/ subsystem vendor ID
Serial Interface Control		Chips with a serial interface, including: • Analog voice codecs • Analog modem codecs • IOM-2 devices.	Transmit and receive data are held in separate 16 word FIFOs.

Description of the single Blocks (cont'd)

Name	provides	supports	Notes
EEPROM Control	• additional information, such as – the Subsystem ID – the Subsystem Vendor ID – extensive power management information	All EEPROMs with SPI interface	This is an optional feature that can be used to customize the PITA-2 configuration at start up.
General Purpose I/O Interface	• GP outputs • GP inputs • GP interrupt inputs		It can be configured to act as • Input pins • Output pins • Interrupt pins. Can be used for pinstrapping the subsystem ID

4   Communication with the PITA-2

For communication with the PITA-2 the following blocks are used:

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PCI Configuration Space	11
PCI Master/Target Controller	22
Interrupt Control Register - Retry Counter	31

4.1   PCI Configuration Space

Overview

4.1.1 Information about the PCI Configuration Space

Description

The PCI Configuration Space contains information about

• the PCI device
• the requested address space in the memory space of the PCI system.

The address space includes 64 32-bit registers where the first 16 registers build the configuration space header (00h-3Ch, refer to "Configuration Space Register of the PITA-2" on page 173)

Construction of the PCI Configuration Space

31 24	23 16	15 8	7 0	
Device ID		Vendor ID		00h
Status		Command		04h
Class Code			Revision ID	08h
BIST	Header Type	Latency Timer	Cach Line Size	0Ch
Base Address Register 0 (Internal Registers)				10h
Base Address Register 1 (Parallel Interface)				14h
Base Address Register 2 (unused)				18h
Base Address Register 3 (unused)				1Ch
Base Address Register 4 (unused)				20h
Base Address Register 5 (unused)				24h
CardBus CIS Pointer				28h
Subsystem ID		Subsystem Vendor ID		2Ch
Expansion ROM Base Address				30h
Reserved			Cap_Ptr	34h
Reserved				38h
Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	3Ch
Power Management Capabilities		Next Item Pointer	Capability ID	40h
Data	Bridge Support	PMCSR		44h
Power Data Register 1				48h
Power Data Register 2				4Ch
Power Data Register 3				50h
Unused Configuration Space Registers				54h
CardBus CIS				58h
Unused Configuration Space Registers				5Ch

shaded fields loaded during
initialization if EEPROM is connected

Description of Register Types

Type	Description
PE	• read only via PCI • these bits are initialized by pinstrapping during PCI reset or by the optional EEPROM
H	• read only via PCI • hardwired
RC	• read clear via PCI • these bits are set by the internal logic • these bits can be read out and reset by writing logical "1" to them • writing logical "0" doesn't influence the states of these bits
RW	• read write via PCI • these bits can be read out and written via the PCI bus
E	• read only via PCI • these bits are initialized to a default value during PCI reset or by the optional EEPROM

4.1.2 Access to the PCI Configuration Space

Description

The PITA-2 supports single 32 bit data transactions for the access to the PCI Configuration Space.

Special Qualities

Name	Description
Subsystem ID	• lower 4 bits can be set via pinstrapping if no EEPROM is used • with external EEPROM the complete 16 bit value can be loaded for the Subsystem ID
Subsystem Vendor ID	• 16 bit ID of the card manufacturer • has to be applied for at the PCI Special Interest Group • can be set via pinstrapping during reset if no EEPROM is used • can be loaded from external EEPROM
CardBus CIS Pointer	is not supported by the PITA-2, although it is implemented in the PCI Configuration Space

4.1.3   Base Address Register

Base Address Registers 0 - 5

Base Address Register	Description
Base Address Register 0	• the lower 12 bits are hardwired to "0" • occupies an address space of 4K • allows access to the internal registers of the PITA-2
Base Address Register 1	• the lower 12 bits are hardwired to "0" • allows continuous read and write operations for access to the parallel interface • occupies an address space of 4K • address space is logically segmented in 4x1K address blocks
Base Address Register 2 - 5	not used

Structure of the Address Space of Base Address Register 1

Address Space	Access to
3FFh - 000h	device 1 on the parallel interface ($\overline{CS0}$)
7FFh - 400h	device 2 on the parallel interface ($\overline{CS1}$)
BFFh - 800h	device 3 on the parallel interface ($\overline{CS2}$)
FFFh - C00h	not used

Configuration Space Register: 04h

Bit 1	Memory_Access_Enable
Type	RW
Default Value	0b
Description	Only if this bit is set to '1', the PCI interface will react on transactions to the base address registers BAR (all Base Address Registers are defined as memory mapped).

Configuration Space Register: 10h

Bit 31:12	Base Address Register 0
Type	RW
Default Value	0000h
Bit 11:00	Base Address Register 0
Type	H
Value	000h
Description	BAR0 contains the base address of an address space in the PCI main memory through which the internal registers of the PITA-2 can be accessed.

Configuration Space Register: 14h

Bit 31:12	Base Address Register 1
Type	RW
Default Value	0000h
Bit 11:00	Base Address Register 1
Type	H
Value	000h
Description	BAR1 contains the base address of a 4-kilobyte address space in the PCI main memory through which the parallel micro controller interface of the PITA-2 can be accessed.

Configuration Space Register: 18h

Bit 31:0	Base Address Register 2
Type	H
Value	0000 0000h
Description	Base Address Register 2 is not supported.

Configuration Space Register: 1Ch

Bit 31:0	Base Address Register 3
Type	H
Value	0000 0000h
Description	Base Address Register 3 is not supported.

Configuration Space Register: 20h

Bit 31:0	Base Address Register 4
Type	H
Value	0000 0000h
Description	Base Address Register 4 is not supported.

Configuration Space Register: 24h

Bit 31:0	Base Address Register 5
Type	H
Value	0000 0000h
Description	Base Address Register 5 is not supported.

4.1.4 Other Registers of the PCI Configuration Space

Configuration Space Register: 28h

Bit 31:0	CardBus CIS Pointer
Type	H
Value	0000 002C0h
Description	Unused

Bit 31:28	ROM_Image_Number
Type	H
Value	0000b
Description	Unused

Bit 27:3	Address_Space_Offset
Type	H
Value	000054h
Description	Unused

Bit 2:0	Address_Space_Indicator
Type	H
Value	000b
Description	Unused

Note

The CardBus function is not supported in this version of the PITA-2.

Configuration Space Register: 2Ch

Bit 31:20	Subsystem ID
Type	E
Default Value	000h
Bit 19:16	Subsystem ID
Type	PE
Value	Pinstrap value or EEPROM value
Description	Identifies a specific board of a manufacturer on which the PITA-2 is used. The 4 LSBs will be set by pinstrapping GP0-3 during PCI reset if no EEPROM is used and the complete 16 bit register can be loaded if the optional EEPROM is used.

Bit 15:0	Subsystem Vendor ID
Type	PE
Value	Pinstrap value or EEPROM value
Description	Marks of the Vendor of the board on which the PITA-2 is used. This register will be set by pinstrapping PAD0-7 and PA0-7 during PCI reset if no EEPROM is used or configured from a connected EEPROM. This ID is allocated by the PCI SIG.

4.2 PCI Master/Target Controller

Introduction

The interface of the PCI bus is represented by the PCI Master/Target Controller. This controller is part of the PITA-2.

The PCI Master/Target Controller supports

- several types of transactions,
- Base Address Registers 0 and 1.

The PCI Master/Target Controller

- has a "Medium Device Select" behavior,
- truncates burst transactions at the end of the first dataphase.

4.2.1   Supported PCI Commands

PCI Master Controller:

PCI Command	Transaction Type
Memory Read	single transfer
Memory Write	single transfer

PCI Target Controller:

PCI Command	Transaction Type
Memory Read	single transfer
Memory Read Multiple	mapped on Memory Read
Memory Read Line	mapped on Memory Read
Memory Write	single transfer
Memory Write and Invalidate	mapped on Memory Write
Configuration Read	single transfer
Configuration Write	single transfer

Overview

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Transaction Type Burst Write	27
Transaction Type Fast Back to Back	29

Note

The following timing diagrams are meant as an example and show transactions to and from the PCI configuration space.

4.2.2   Transaction Type Burst Read

Description

- Asserting $\overline{\text{IRDY}}$ and $\overline{\text{STOP}}$ at the first dataphase leads to the disconnection (Disconnect-B) of the burst read transaction by the PITA-2.
- $\overline{\text{STOP}}$ is asserted until $\overline{\text{FRAME}}$ is deasserted.
- Deassertion of $\overline{\text{FRAME}}$ means that $\overline{\text{STOP}}$ and $\overline{\text{DEVSEL}}$ together are deasserted.

Timing Diagram

Configuration Space Register: 04h

Bit 26:25	DEVSEL_Timing
Type	H
Value	01b
Description	'01' = medium timing, i.e. the DEVSEL signal will be asserted from the PCI interface with the second positive PCI clock edge after $\overline{\text{FRAME}}$ was asserted on the PCI bus by a master.

4.2.3   Transaction Type Burst Write

Description

- Asserting $\overline{\text{IRDY}}$ and $\overline{\text{STOP}}$ at the first dataphase leads to the disconnection (Disconnect-B) of the burst write transaction by the PITA-2.
- $\overline{\text{STOP}}$ is asserted until $\overline{\text{FRAME}}$ is deasserted.
- Deassertion of $\overline{\text{FRAME}}$ means that $\overline{\text{STOP}}$ and $\overline{\text{DEVSEL}}$ together are deasserted.

Timing Diagram

Configuration Space Register: 04h

Bit 26:25	DEVSEL_Timing
Type	H
Value	01b
Description	'01' = medium timing, i.e. the DEVSEL signal will be asserted from the PCI interface with the second positive PCI clock edge after $\overline{\text{FRAME}}$ was asserted on the PCI bus by a master.

4.2.4 Transaction Type Fast Back to Back

Description

With the fast back to back transaction a PCI Master Controller can perform

- several write transactions
- a read transaction as last transaction

without setting the PCI bus to IDLE state in between or releasing the bus to another master.

At the end of a transaction:

- The Master asserts the $\overline{\text{FRAME}}$ signal and at the same time the $\overline{\text{TRDY}}$ signal is deasserted.

The transaction is answered with a RETRY signal by the PITA-2

- if the parallel interface is included in the fast back to back transaction
- <u>and</u> the parallel interface is still busy.

Timing Diagram
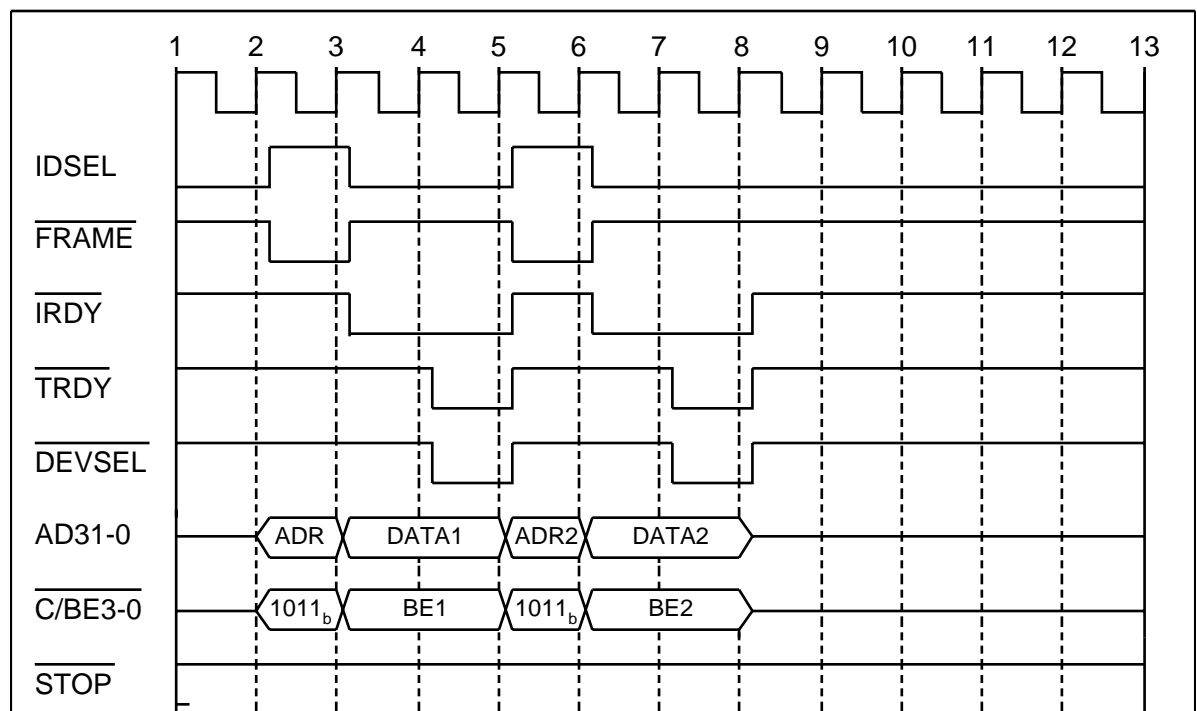
Configuration Space Register: 04h

Bit 23	Fast_Back_To_Back_Capability
Type	H
Value	1b
Description	The PITA-2 supports fast back-to-back.

Bit 9	Fast_Back_To_Back_Enable
Type	H
Value	0b
Description	The PITA-2 itself generates no fast back-to-back transactions.

4.3   Interrupt Control Register - Retry Counter

Description

- Part of the PCI Master Target Controller
- Functionality:
1. Disconnection of the PCI Master transaction with Retry by the addressed PCI Slave.
2. Decrement of the counter.
3. The Retry_Counter_Int bit is set.
4. An interrupt will be generated if the Retry_Counter_Enable bit is set.
5. The PCI Master starts the transaction again.

Internal Register: 00h

Bit 27	RETRY_Counter_Down_Int_En
Type	RW
Default Value	0b
Description	Enable for the Retry_Counter_Down interrupt bit

Bit 11	Retry_Counter_Int
Type	RC
Default Value	0b
Description	If a PCI Master initiated transaction is retried from a PCI Slave with the number of retries defined in the Retry_Counter register, this interrupt bit is set by the PCI interface.

Internal Register:1Ch

Bit 23:16	Retry Count Register
Type	RW
Default Value	00h
Description	Hold the number of retries for a single PCI master transaction before the PITA-2 will assert an interrupt (if enabled).
	As an example, if this register is programmed with the value 4, the PITA-2 will retry a single PCI transaction up to four times as a master before it asserts an interrupt. The PITA-2 will continue to retry the transaction until it succeeds or the software decides to abort the whole transaction.

5 Communication with External Components

Introduction

This chapter describes the interfaces for communication with devices on the local bus side (i.e. not the PCI bus side).

Interfaces

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General Purpose I/O Interface	97
SPI EEPROM Interface	115

5.1 Serial DMA Interface

Introduction

The serial DMA interface is used in different modes to transmit and receive 16 bit/ 32 bit data frames. These data frames have different content and structures:

- Data
- Data/Voice and Command
- Data/Voice and Command for two codecs
- Different time slots on IOM-2.

Usage of the Serial DMA Interface

The serial DMA interface is clocked by default with the internally generated clock (DCL = PCI clock divided by 40).

The Ser_Clock_Set bit must be set in the Serial Clock Select register to '1' when the interface shall work in ALIS V3.X or IOM-2 mode

Resetting this bit can result in an unknown behavior of the FIFOs and the serial controller.

The serial DMA interface is fully controlled by the DMA controller.

Overview

5.1.1   DMA Controller

Overview

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5.1.2 Information about the DMA Controller

Description

For the control of the DMA Controller, three register are implemented in the internal registers:

- The Circular Buffer Start Address is a 4-kbyte aligned PCI address which points to a 4-kbyte circular buffer in the PCI main memory. All DMA read/write transactions between host and PITA will be processed via this 4-kbyte address space.
- The DMA Control register includes the 6-bit parameter DMA Select which is used to define the mode for the next DMA transfer. With the DMA_Start bit the DMA transfer can be started and stopped.
- The contents of the DMA Write Count Register is interpreted as a threshold for the write transfers from the DMA controller.

Function of the DMA Controller

Phase	Function
1	DMA_Start bit is set in the DMA Control Register and a DMA transfer is started as defined in the DMA Select Register.
2	The DMA controller loads the Circular Buffer Start Address to its Actual Circular Buffer Pointer.
3	The DMA controller fills the TX FIFO by reading 15 times through the PCI interface (PCI master mode) from the circular buffer.
4	The DMA controller signals the end of the initial sequence.
5	The DMA controller increments the Actual Circular Buffer Pointer by 4 each read transfer.
6	The DMA controller loads the contents of the 12 bit DMA Write Count Register to its internal 12 bit DMA write counter.
7	After the first 15 read transfers in the beginning of the 16th read transfer the DMA controller starts the normal DMA algorithm.

Function of the DMA Algorithm

Phase	Function
1	The DMA controller reads the 16th data word from the current address in the circular buffer (Actual Circular Buffer Pointer) to the internal TX FIFO.
2	The DMA controller writes the first received 16-bit data word from the RX FIFO to the same address in the circular buffer.
3	The DMA controller increments the Actual Buffer Pointer by 4.
4	The DMA controller reads the 17th data word from the current address in the circular buffer (Actual Circular Buffer Pointer) to the internal TX FIFO.
5	The DMA controller writes the second received 16-bit data word from the RX FIFO to the same address in the circular buffer.
6	The DMA controller increments the Actual Buffer Pointer by 4.
7	and so on

DMA Write Counter

After each write transaction from the RX FIFO to the buffer the internal DMA write counter is incremented by 1. If this counter reaches '0' an interrupt is generated and the counter is loaded again with the contents of the DMA Write Counter Register.

The internal DMA write counter is decremented every two write transactions as long as two 16 bit values per FSC frame are transferred in the following modes:

- 32 bit frame mode
- dual modem mode
- modem+voice mode
- IOM-2 mode 2 and 3.

DMA_Start bit

- The reset of the DMA_Start bit stops the DMA transfer immediately.
- The assertion of the DMA_Start bit resets the TX and RX FIFO's.
  This means that all FIFO data is lost when the DMA transfer is stopped.

Data in the Circular Buffer

Since no data is written from the RX FIFO to the circular buffer for the first 15 addresses, the first interrupt after the DMA_Start assertion means that the received data is available in the circular buffer on address

- 003Ch to 003Ch + [DMA Write Count]: 16 bit frame modes
- 003Ch to 0003Ch + 2 x [DMA Write Count]: 32 bit frame modes.

During normal data transfer every interrupt means that received data is available in the circular buffer on address

- [end address from last interrupt] to [end address from last interrupt] + [DMA Write Count]: 16 bit frame modes
- [end address from last interrupt] to [end address from last interrupt] + 2 x [DMA Write Count]: 32 bit frame modes

Example for DMA controlled Data Transfer via Circular Buffer

The status of the DMA controller:

16 bit frame access mode (ALIS V2.1 mode/IOM-2 mode 1) when three data frames are already written to the TX line.
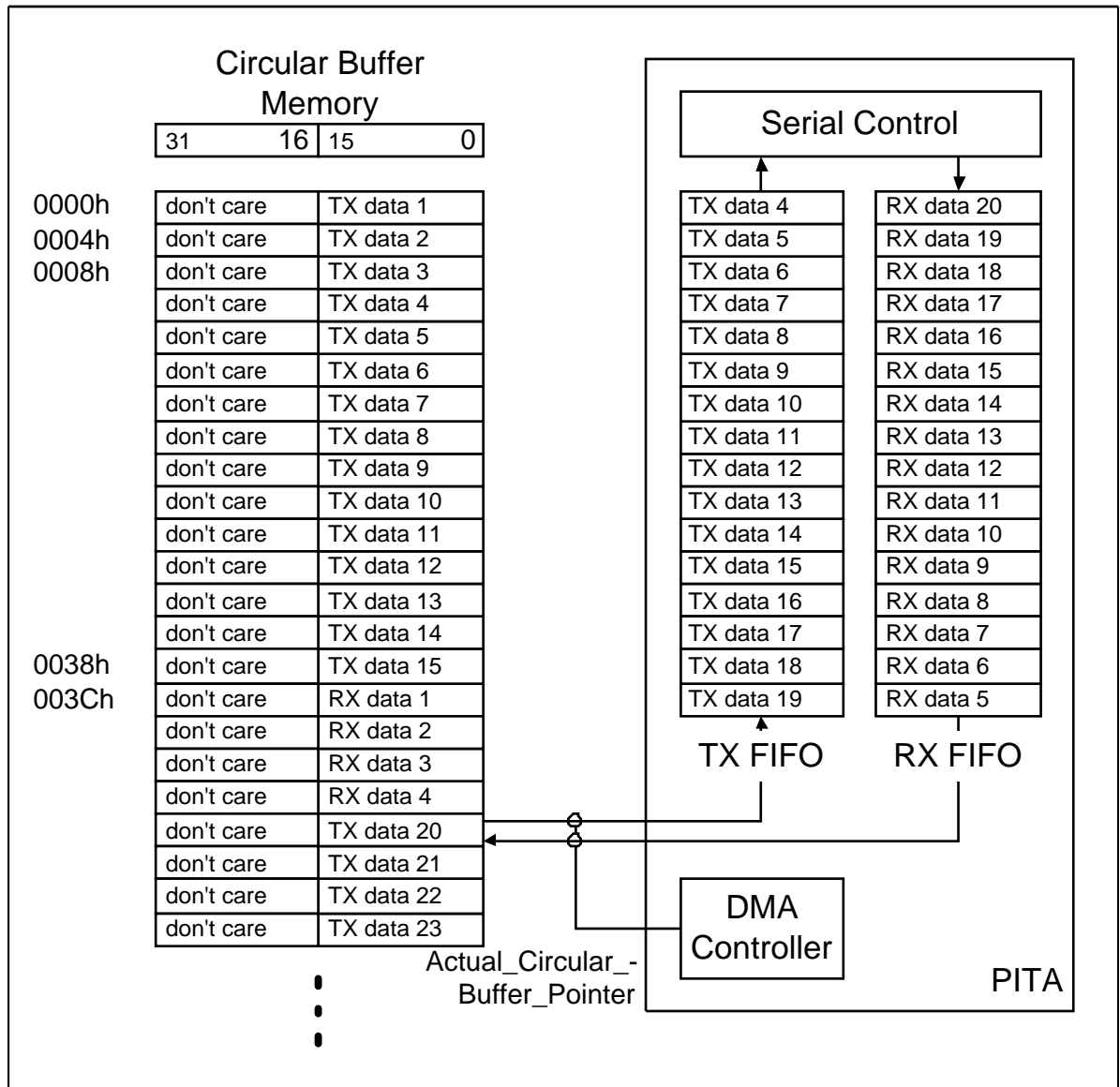
5.1.3 Internal Registers of the DMA Controller

Internal Registers: 00h

Bit 26	FIFO_Overflow_Empty_Int_En
Type	RW
Default Value	0b
Description	Enable for the FIFO_Overflow_Empty interrupt bit

Bit 25	DMA_Write_Counter_Overflow_Int_En
Type	RW
Default Value	0b
Description	Enable for the DMA_Write_Counter_Overflow interrupt bit.

Bit 24	DMA_Write_Counter_Int_En
Type	RW
Default Value	0b
Description	Enable for the DMA_Write_Counter interrupt bit.

Bit 10	FIFO_Overflow_Empty_Int
Type	RC
Default Value	0b
Description	During a DMA transfer the serial controller was unable to write received data to the RX FIFO because is was already full or the serial controller was unable to send data after the rising FSC edge because of empty TX FIFO.

Internal Registers: 00h (cont'd)

Bit 9	DMA_Write_Counter_Overflow_Int
Type	RC
Default Value	0b
Description	This bit is set if the internal DMA write counter is counted down while the DMA_Write_Counter_Int bit is still active. This means that the interrupt generated by the DMA_Write_Counter_Int bit is not yet processed.

Bit 8	DMA_Write_Counter_Int
Type	RC
Default Value	0b
Description	This bit is set if the number of data, defined in the DMA Write Count Register is written through the PCI interface. In the 32-bit modes (dual modem, modem+voice, IOM-2 mode 2, IOM-2 mode 3) this bit is set if the number of data pairs defined in the DMA Write Count Register is transferred through the PCI interface.

Internal Registers: 04h

Bit 31:0	DMA Control Register
Bit 31:9	Reserved
Type	H
Value	0000000h
Description	Reserved

Bit 8	DMA_Start
Type	RW
Default Value	0b
Description	By asserting this bit a DMA transfer between the circular buffer and the serial DMA interface using internal RX/TX FIFOs is started. This bit is reset by the host if the DMA transfer is to be finished.

Bit 7:6	Reserved
Type	H
Value	00b
Description	Reserved

Internal Registers: 04h (cont'd)

Bit 5:0	DMA Select
Type	RW
Default Value	000000b
Description	Used to define the mode for the next DMA transfer: – Mode 1 ('000001'): Single Modem Mode V2.1 – Mode 2 ('000010'): Single Modem Mode V3.X – Mode 3 ('000100'): Dual Modem/Modem+Voice Mode V3.X – Mode 4 ('001000'): IOM-2 Mode 1 – Mode 5 ('010000'): IOM-2 Mode 2 – Mode 6 ('100000'): IOM-2 Mode 3 With the DMA_Start bit the DMA transfer can be started or stopped.

Internal Registers: 08h

Bit 31:12	Circular Buffer Start Address
Type	RW
Default Value	000000h
Bit 11:0	Circular Buffer Start Address
Type	H
Value	000h
Description	• 4-kbyte aligned PCI address which points to a 4-kbyte circular buffer in the PCI main memory. • All DMA read/write transactions between the host and the PITA are processed via this 4-kbyte address space.

Internal Register: 0Ch

Bit 31:02	Actual Circular Buffer Pointer
Type	R
Value	31-12 equal to 31-12 of Register 08, 11-02 actual address
Bit 1:0	Actual Circular Buffer Pointer
Type	H
Value	00b
Description	By reading this register the software has access to the PCI address in the DMA circular buffer address pointer. The bits 31-12 are equal the contents of the Circular Buffer Start Address Register. The bits 11-0 represent the actual dword address in the circular buffer.

Internal Register: 1Ch

Bit 11:0	DMA Write Count Register
Type	RW
Default Value	000h
Description	

5.1.4   IOM-2 Mode 1

Transmission and Reception of Data in the Circular Buffer
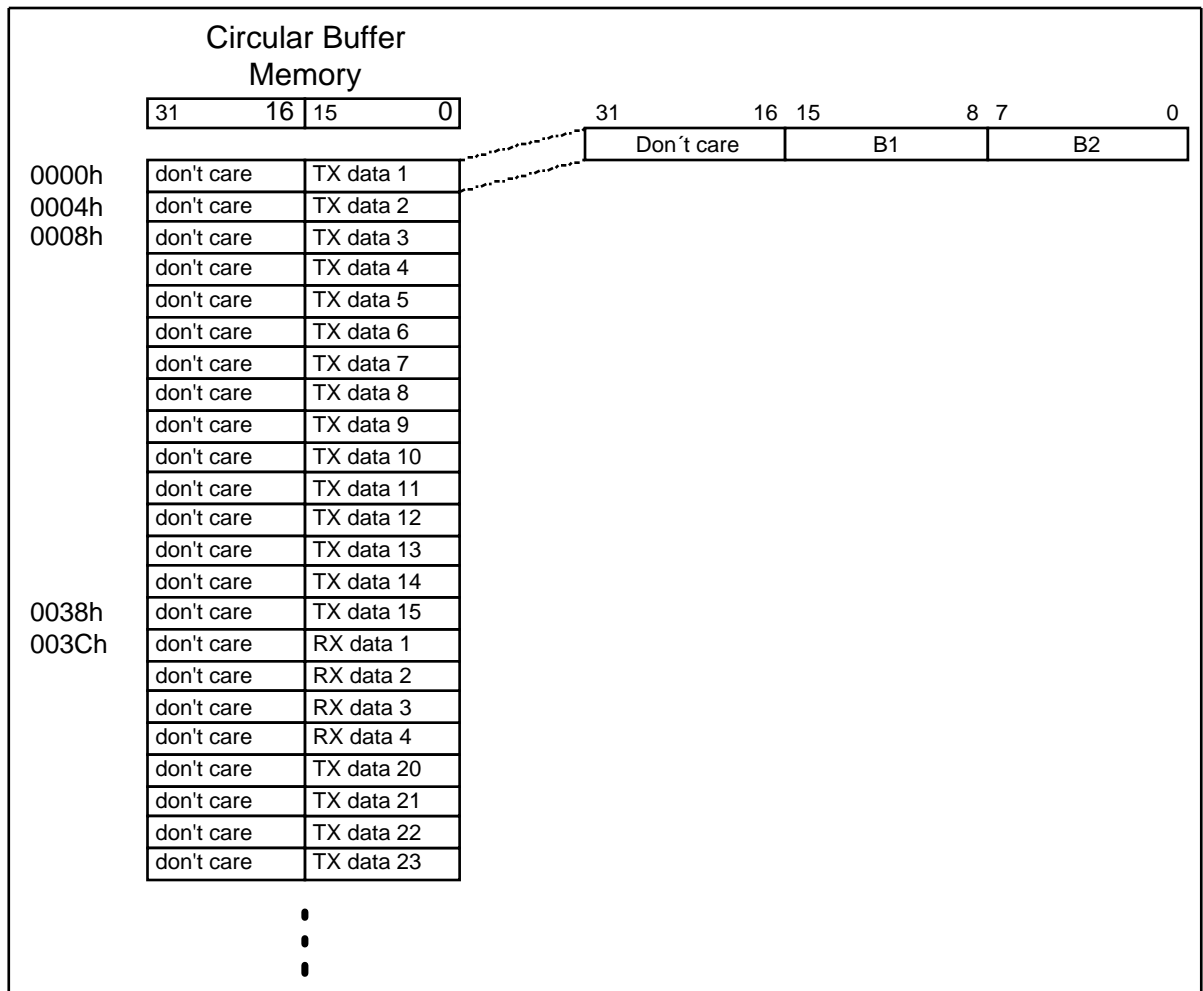
	Circular Buffer Memory					
	31 16	15 0	31 16	15 8	7 0	
			Don´t care	B1	B2	
0000h	don't care	TX data 1				
0004h	don't care	TX data 2				
0008h	don't care	TX data 3				
	don't care	TX data 4				
	don't care	TX data 5				
	don't care	TX data 6				
	don't care	TX data 7				
	don't care	TX data 8				
	don't care	TX data 9				
	don't care	TX data 10				
	don't care	TX data 11				
	don't care	TX data 12				
	don't care	TX data 13				
	don't care	TX data 14				
0038h	don't care	TX data 15				
003Ch	don't care	RX data 1				
	don't care	RX data 2				
	don't care	RX data 3				
	don't care	RX data 4				
	don't care	TX data 20				
	don't care	TX data 21				
	don't care	TX data 22				
	don't care	TX data 23				

Data in Circular Buffer and on Serial DMA Interface

Direction	Data in Circular Buffer	Data on Serial DMA Interface
Transmit	Bits from circular buffer: [31:16] = don't care [15:8] = B1 [7:0] [7:0] = B2 [7:0]	Write to serial DMA interface: B1 [7:0] B2 [7:0]

Data in Circular Buffer and on Serial DMA Interface (cont'd)

Direction	Data in Circular Buffer	Data on Serial DMA Interface
Receive	Bits to circular buffer: [31:16] = don't care [15:8] = B1 [7:0] [7:0] = B2 [7:0]	Read from serial DMA interface: B1 [7:0] B2 [7:0]

Timing Diagram

Internal Registers: 04h

Bit 5:0	DMA Select
Type	RW
Default Value	000000b
Description	The DMA Control Register includes the 6 bit parameter DMA Select. Used to define the mode for the next DMA transfer: **Mode 4 ('001000'): IOM-2 Mode 1** With the DMA_Start bit the DMA transfer can be started or stopped.

Internal Register: 20h

Bit 1	DCL_Out_En
Type	RW
Default Value	0b
Description	Bit 1='0': The DCL signal is configured as input, i.e. not driven by the PITA.

Bit 0	Serial_Clock_Select
Type	RW
Default Value	0b
Description	Bit 0='1': The serial controller is driven with the external DCL input clock.

5.1.5 IOM-2 Mode 2

Transmission and Reception of Data in the Circular Buffer

Circular Buffer Memory

	31 ... 16	15 ... 0

0000h	don't care	TX data 1
0004h	don't care	TX data 2
0008h	don't care	TX data 3
	don't care	TX data 4
	don't care	TX data 5
	don't care	TX data 6
	don't care	TX data 7
	don't care	TX data 8
	don't care	TX data 9
	don't care	TX data 10
	don't care	TX data 11
	don't care	TX data 12
	don't care	TX data 13
	don't care	TX data 14
0038h	don't care	TX data 15
003Ch	don't care	RX data 1
	don't care	RX data 2
	don't care	RX data 3
	don't care	RX data 4
	don't care	TX data 20
	don't care	TX data 21
	don't care	TX data 22
	don't care	TX data 23

31 ... 16	15 ... 8	7 ... 0
Don´t care	B1	B2

31 ... 16	15 ... 8	7 ... 0
Don´t care	Monitor 0	D, C/I, MR, MX

Data in Circular Buffer and on Serial DMA Interface

Direction	Buffer Offset	Data in Circular Buffer	Data on Serial DMA Interface
Transmit	0, 2, 4, ...	Bits from circular buffer: [31:16] = don't care [15:8] = B1 [7:0] [7:0] = B2 [7:0]	Write to serial DMA interface: B1 [7:0] B2 [7:0]

Data in Circular Buffer and on Serial DMA Interface (cont'd)

Direction	Buffer Offset	Data in Circular Buffer	Data on Serial DMA Interface
Transmit	1, 3, 5, ...	Bits from circular buffer: [31:16] = don't care [15:8] = Monitor 0 [7:0] [7:0] = D,C/I0,MR,MX [7:0]	Write to serial DMA interface: Monitor 0 [7:0] D,C/I0,MR,MX [7:0]
Receive	0, 2, 4, ...	Bits to circular buffer: [31:16] = don't care [15:8] = B1 [7:0] [7:0] = B2 [7:0]	Read from serial DMA interface: B1 [7:0] B2 [7:0]
	1, 3, 5, ...	Bits to circular buffer: [31:16] = don't care [15:8] = Monitor 0 [7:0] [7:0] = D,C/I0,MR,MX [7:0]	Read from serial DMA interface: Monitor 0 [7:0] D,C/I0,MR,MX [7:0]

Timing Diagram

Internal Registers: 04h

Bit 5:0	DMA Select
Type	RW
Default Value	000000b
Description	The DMA Control Register includes the 6 bit parameter DMA Select. Used to define the mode for the next DMA transfer: **Mode 5 ('010000'): IOM-2 Mode 2** With the DMA_Start bit the DMA transfer can be started or stopped.

Internal Register: 20h

Bit 1	DCL_Out_En
Type	RW
Default Value	0b
Description	Bit 1='0': The DCL signal is configured as input, i.e. not driven by the PITA.

Bit 0	Serial_Clock_Select
Type	RW
Default Value	0b
Description	Bit 0='1': The serial controller is driven with the external DCL input clock.

5.1.6   IOM-2 Mode 3

Transmission and Reception of Data in the Circular Buffer
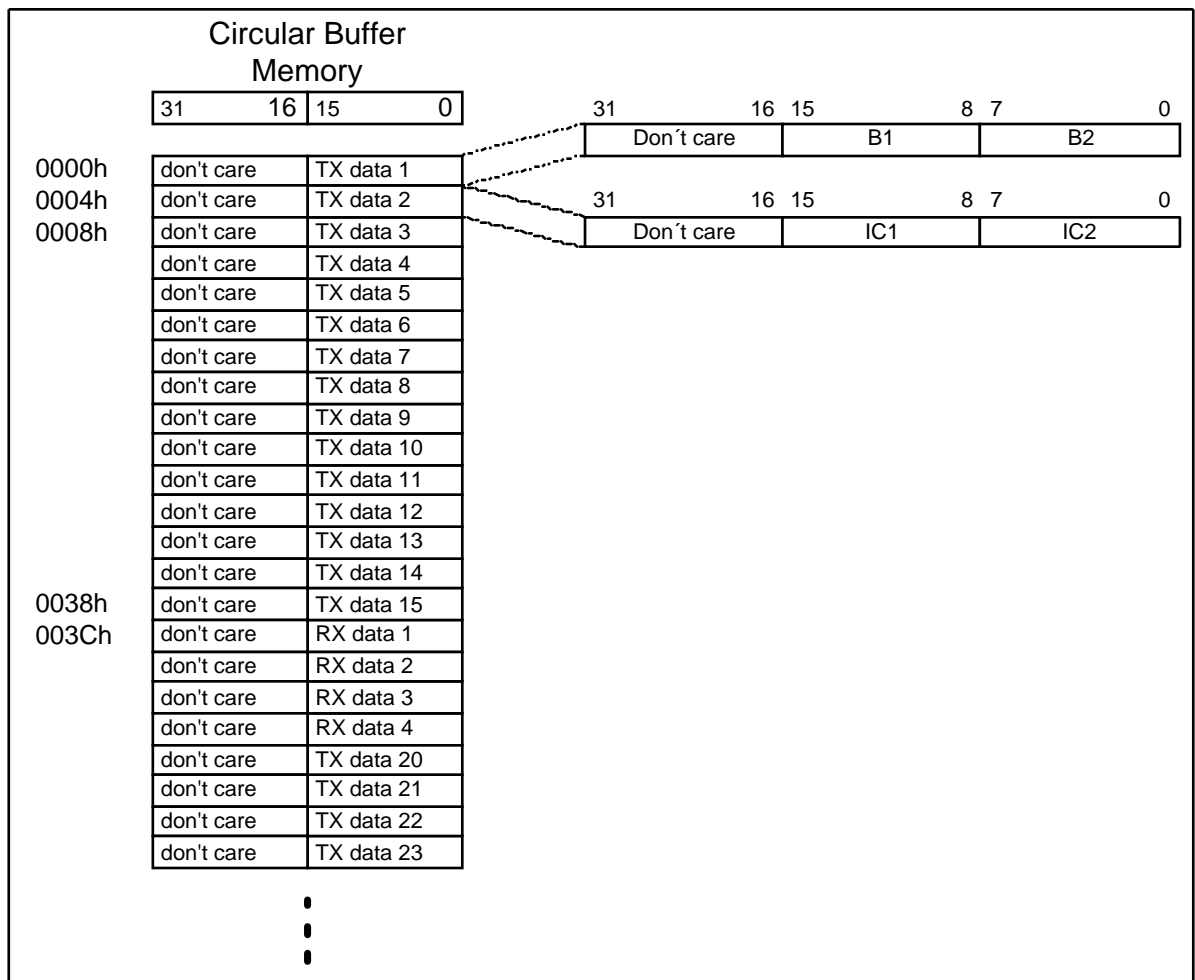
Data in Circular Buffer and on Serial DMA Interface

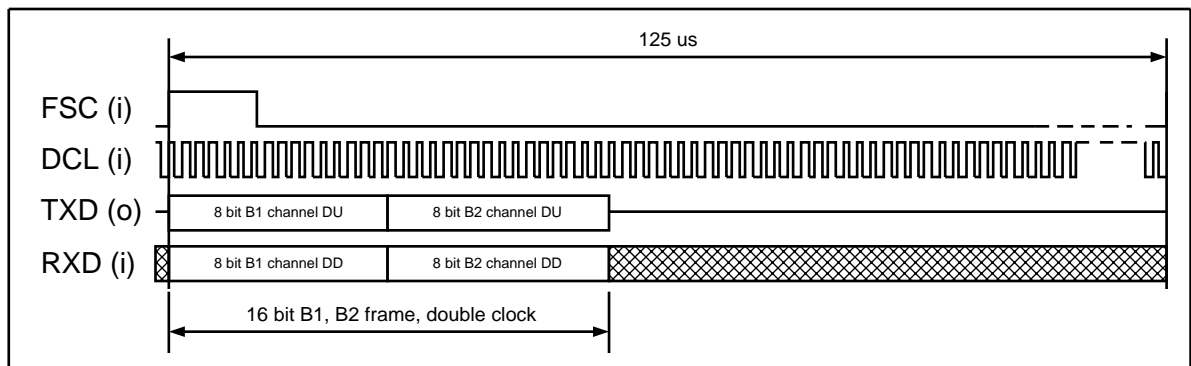| Direction	Buffer Offset	Data in Circular Buffer	Data on Serial DMA Interface
Transmit	0, 2, 4, ...	Bits from circular buffer: [31:16] = don't care [15:8] = B 1 [7:0] [7:0] = B 2 [7:0]	Bits to serial DMA interface: B 1 [7:0] B 2 [7:0]

Data in Circular Buffer and on Serial DMA Interface (cont'd)

Direction	Buffer Offset	Data in Circular Buffer	Data on Serial DMA Interface
Transmit	1, 3, 5, ...	Bits from circular buffer: [31:16] = don't care [15:8] = IC1 [7:0] [7:0] = IC2 [7:0]	Write to serial DMA interface: IC1 [7:0] IC2 [7:0]
Receive	0, 2, 4, ...	Bits to circular buffer: [31:16] = don't care [15:8] = B1 [7:0] [7:0] = B2 [7:0]	Read from serial DMA interface: B1 [7:0] B2 [7:0]
	1, 3, 5, ...	Write to circular buffer: [31:16] = don't care [15:8] = IC1 [7:0] [7:0] = IC2 [7:0]	Read from serial DMA interface: IC1 [7:0] IC2 [7:0]

Timing Diagram

Internal Registers: 04h

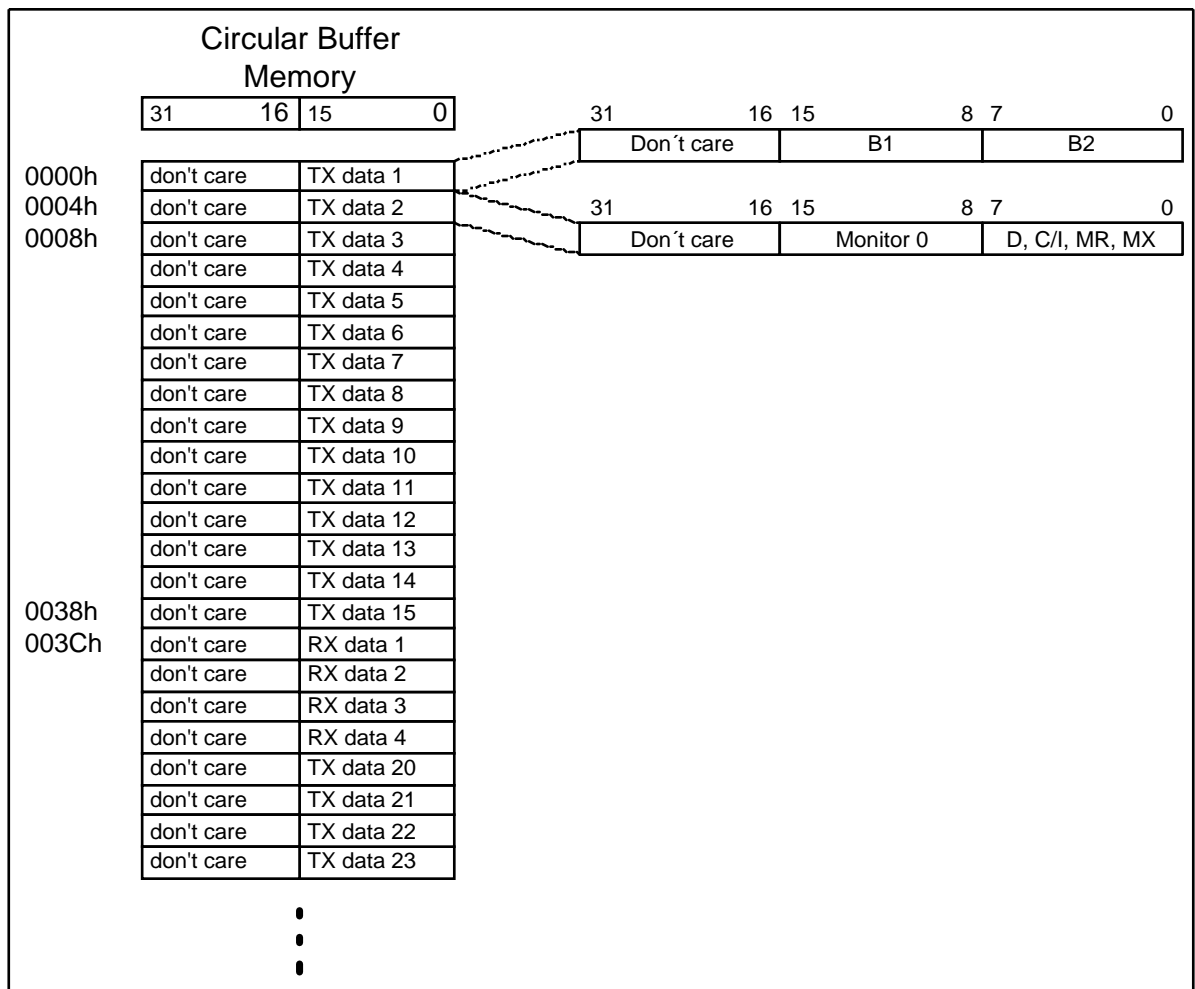|	
Bit 5:0	DMA Select
Type	RW
Default Value	000000b
Description	The DMA Control Register includes the 6 bit parameter DMA Select. Used to define the mode for the next DMA transfer: **Mode 6 ('100000'): IOM-2 Mode 3** With the DMA_Start bit the DMA transfer can be started or stopped.

Internal Register: 20h

Bit 1	DCL_Out_En
Type	RW
Default Value	0b
Description	Bit 1='0': The DCL signal is configured as input, i.e. not driven by the PITA.

Bit 0	Serial_Clock_Select
Type	RW
Default Value	0b
Description	Bit 0='1': The serial controller is driven with the external DCL input clock.

5.1.7   IOM-2 Modes - Supplementary Description

Selection of IOM-2 Time Slots

The MISC register contains four bits. They are used for masking the time slot on IOM-2.

If Bx_MSK (x := [1,4]) is set:

- The corresponding value from the TX FIFO is not written to the DU line.
- FFh is written to this time slot.
- In IOM-2 mode 1 the bits B3_MSK and B4_MSK have no effect.
- Data is always transferred from the IOM-2 time slot to the RX-FIFO.

Timing Diagram for all IOM-2 Modes
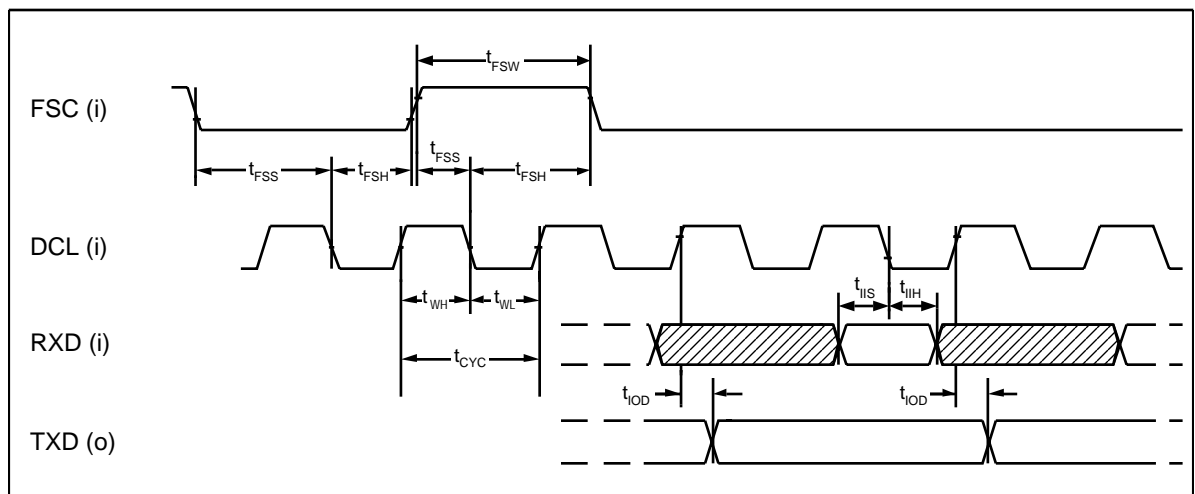
Abbreviations for the Timing Diagram

Parameter	Symbol	Limit Values		Unit
		min.	**max.**	
FSC pulse width	t_{FSW}	40		ns
FSC setup time	t_{FSS}	40		ns
FSC hold time	t_{FSH}	40		ns
DCL cycle time	t_{CYC}	244		ns
DCL HIGH time	t_{WH}	100		ns
DCL LOW time	t_{WL}	100		ns
IOM output data delay	t_{IOD}		100	ns
IOM input data setup	t_{IIS}	20		ns
IOM input data hold	t_{IIH}	20		ns

Figure of the MISC Register B1 - B4 Mask Bits

MISC Register:	B1_MSK	B2_MSK	B3_MSK	B4_MSK
IOM-2 Mode 1	B1	B2		
IOM-2 Mode 2	B1	B2	Monitor 0	D,C/I0,MR,MX
IOM-2 Mode 3	B1	B2	IC1	IC2
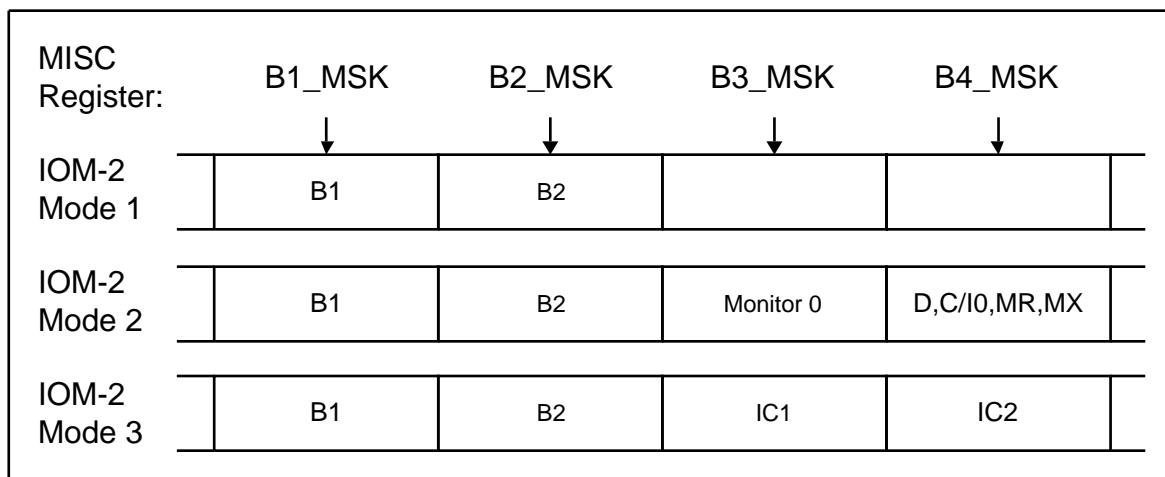
Masking of IOM-2 Time slots (Example for IOM-2 Mode 2)
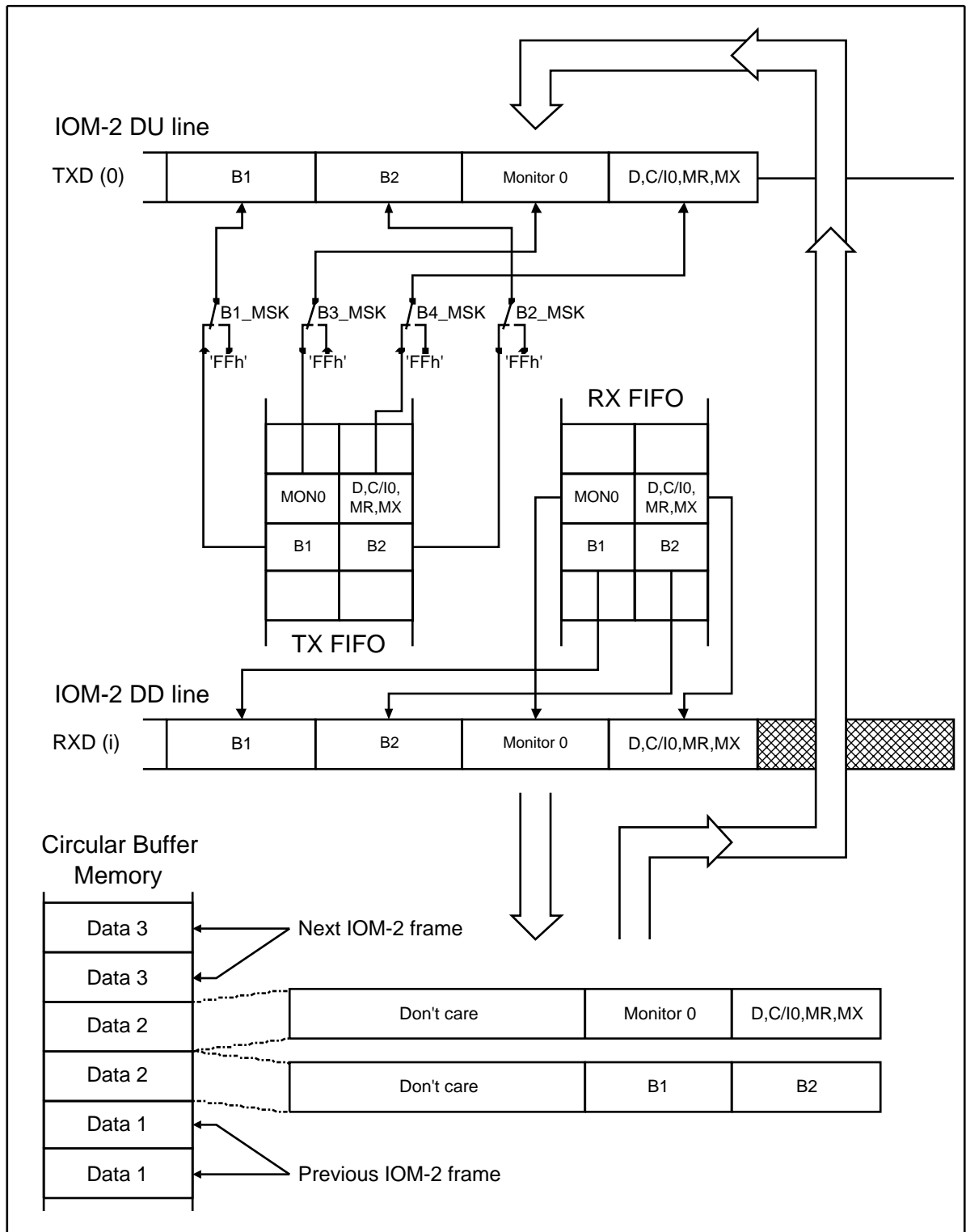
Internal Register: 1Ch

Bit 31:0	MISC (Miscellaneous Register)

Bit 31	IOM_B1_masking
Type	RW
Default Value	0b
Description	Bit 31='0': Byte B1 is generated out of the circular buffer. Bit 31='1': FFh is transmitted on the B1 time slot.

Bit 30	IOM_B3_masking
Type	RW
Default Value	0b
Description	Bit 30='0': Byte B2 is generated out of the circular buffer. Bit 30='1': FFh is transmitted on the B2 time slot.

Bit 29	IOM_Monitor_0 / IC1_masking
Type	RW
Default Value	0b
Description	Bit 29='0': Byte Monitor 0 or IC1 is generated out of the circular buffer. Bit 29='1': FFh is transmitted on the Monitor/IC1 time slot. Monitor is used in IOM-2 mode 2. IC1 is used in IOM-2 mode 3.

Internal Register: 1Ch (cont'd)

Bit 28	IOM_Supl_masking / IC2_masking
Type	RW
Default Value	0b
Description	Address:='0': Byte D, C/I0, MR, MX or IC2 is generated out of the circular buffer. Address:='1': FFh is transmitted on the D, C/I0, MR, MX or IC2 time slot. D, C/I0, MR, MX: Used in IOM-2 mode 2. IC2: Used in IOM-2 mode 3

5.1.8 Single Modem Mode V2.1

Data in Circular Buffer and on Serial DMA Interface

Direction	Data in Circular Buffer	Data on Serial DMA Interface
Transmit	Bits from circular buffer: [31:16] = don't care [15:0] = data frame [15:0]	Write to serial DMA interface: data frame [15:0]
Receive	Bits to circular buffer: [31:16] = don't care [15:0] = data frame [15:0]	Read from serial DMA interface: data frame [15:0]

Timing diagrams
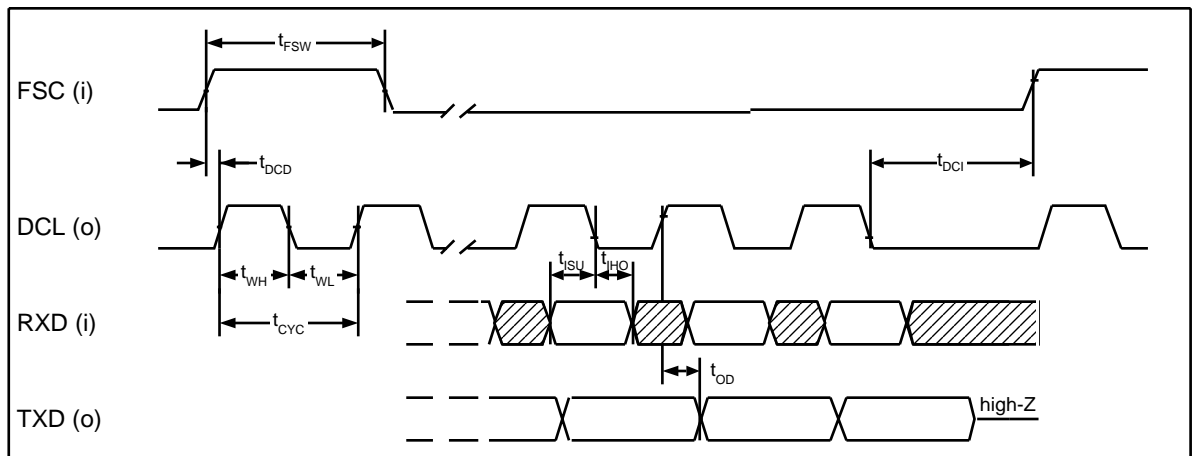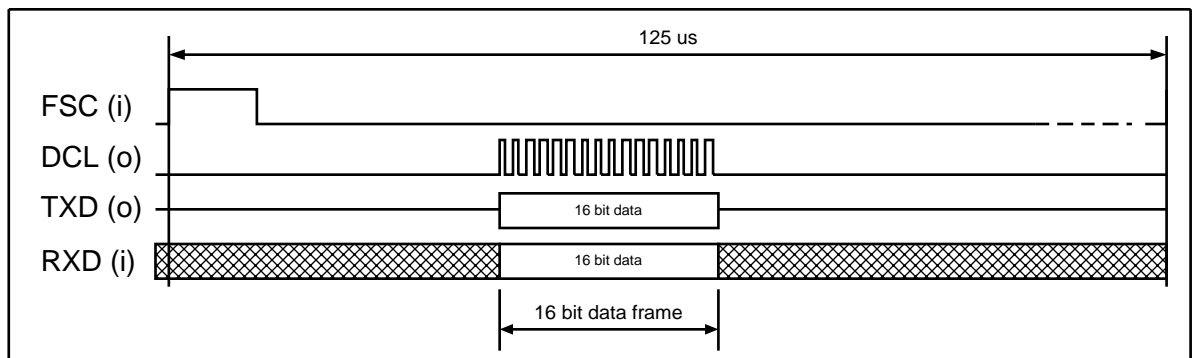
Abbreviations for the Timing Diagram

Parameter	Symbol	PCI Clock Cycles	Limit Values			Unit
			min.	typ.	max.	
FSC pulse width	t_{FSW}		40			ns
DCL delay	t_{DCD}	16	480			ns
DCL idle time	t_{DCI}			105		µs
DCL cycle time	t_{CYC}	40		1200		ns
DCL HIGH time	t_{WH}	20		600		ns
DCL LOW time	t_{WL}	20		600		ns
DCL duty cycle			45	50	55	%
Input data setup	t_{ISU}		10			ns
Input data hold	t_{IHO}		10			ns
Output data delay	t_{OD}				10	ns

Configuration of the Single Modem Mode V2.1 after a System/Soft Reset

- The configuration of the PSB4596 V2.1 in single modem mode is realized by software using the 4-bit General Purpose I/O Interface of the PITA (See "General Purpose I/O Interface" on page 97.).
- After a system/soft reset the FSC is an input pin both for
  - the PITA
  - the ALIS V2.1
- After a system reset the DCL_Out_En bit must be set to '1' by the host.

PITA Configuration for ALIS V2.1 after a System Reset

Serial DMA Interface Mode	Ser_Clock_Sel (clock input to Serial DMA interface)		DCL_Out_En (DCL Direction)	
ALIS V2.1	0	PCI clock/40	1	DCL output

Note

A Pull Down resistor is required on the board to avoid a floating FSC signal in this situation.

Internal Registers: 04h

Bit 5:0	DMA Select
Type	RW
Default Value	000000b
Description	The DMA Control Register includes the 6 bit parameter DMA Select. Used to define the mode for the next DMA transfer: **Mode 1 ('000001'): Single Modem Mode V2.1** With the DMA_Start bit the DMA transfer can be started or stopped.

Internal Register: 20h

Bit 1	DCL_Out_En
Type	RW
Default Value	0b
Description	Bit 1='1': The DCL signal is output (open drain) and driven by the PITA.

Bit 0	Serial_Clock_Select
Type	RW
Default Value	0b
Description	Bit 0='0': The serial controller is driven with the clock signal generated by the internal clock divider.

5.1.9 Single Modem Mode ALIS V3.X

Overview

Overview	Page
Information about the Single Modem Mode ALIS V3.X	65
Internal Registers of the Single Modem Mode V3.X	67

5.1.9.1 Information about the Single Modem Mode ALIS V3.X

Data in Circular Buffers, on Serial DMA Interface

Direction	Data in Circular Buffer	Data on Serial DMA Interface
Transmit	Read from circular buffer: [31:16]= don't care [15:0] = data frame [15:0]	Write to serial DMA interface: data frame [15:0]
Receive	Write to circular buffer: [31:16]= don't care [15:0] = data frame [15:0]	Read from serial DMA interface: data frame [15:0]

Timing Diagram
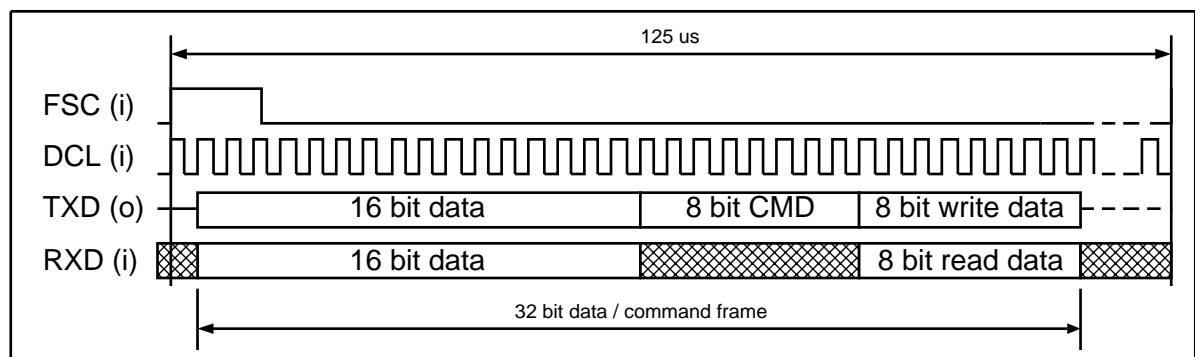
Note

> The timing characteristics of the serial DMA interface in Single modem mode V3.X mode are identical to the IOM-2 modes with the only difference that the DCL signal is not a double bit clock, but a single bit clock, similar to Single Modem mode V2.1.

Configuration of the Single Modem Mode V3.X after a System/Soft Reset

- Realized by starting the DMA transfer.
  - Separate from this transfer the command byte and command data byte are written to the ALIS Command Registers in the PITA on addresses 10h.
- After a system/soft reset the single modem mode V3.X is in the multiplexed mode because the non multiplexed mode is not supported.
- The ALIS V3.X needs some time after an external reset until it has stabilized FSC and DCL. Furthermore as the PITA-2 does not automatically asserts SRST as a response to a PCI reset the following procedure is recommended to start the communication with the ALIS V3.X:
  - Assert $\overline{\text{SRST}}$ by resetting bit 25 of internal register 025h
  - Deassert $\overline{\text{SRST}}$ by setting bit 25 of internal register 025h
  - Wait 500ms
- After this procedure the ALIS V3.X is ready for receiving the first command

PITA Configuration for ALIS V3.X after a System Reset

Serial DMA Interface Mode	Ser_Clock_Sel (clock input to Serial DMA interface)		DCL_Out_En (DCL Direction)	
ALIS V3.X	1	DCL input clock	0	DCL_Out _En
2×ALIS V3.X	1		0	
ALIS V3.X + second codec	1		0	

5.1.9.2 Internal Registers of the Single Modem Mode V3.X

Internal Registers: 04h

Bit 5:0	DMA Select
Type	RW
Default Value	000000b
Description	The DMA Control Register includes the 6 bit parameter DMA Select. Used to define the mode for the next DMA transfer: **Mode 2 ('000010'): Single Modem Mode V3.X** With the DMA_Start bit the DMA transfer can be started or stopped.

Internal Register: 10h

Bit 31:0	ALIS Command Register 1
Description	This command register is used for the first command structure in the FSC time slot by the serial controller.

Bit 31:25	Reserved
Type	H
Value	0b
Description	Reserved

Internal Register: 10h (cont'd)

Bit 24	New_ALIS_Command_1
Type	RW
Default Value	0b
Description	Bit 24='1': The host has written a new command to the ALIS Command Resister 1. Bit 24='0': Last command written to the ALIS Command Register 1 by the host is processed and the received data is available in the ALIS Received Data 1 register. This bit is set by software if there is a new command in the ALIS Command 1 Register. After the serial DMA interface has transmitted the new command and the received data is written to the ALIS_Received_Data_1 bits, this bit is reset by the serial DMA interface.

Bit 23:16	ALIS_Received_Data_1
Type	RW
Default Value	00h
Description	During a DMA transfer in mode 2 or 3 every time a new command is transferred through the serial DMA interface, the received data is fetched and saved in this register. New command means: The command was written through the PCI interface to the ALIS command register. Transferring a NOP command (FFh or 00h) leads to skipping of the received data.

Internal Register: 10h (cont'd)

Bit 15:8	ALIS_Command_1
Type	RW
Default Value	00h
Description	During a DMA transfer in mode 2 or 3 the contents of this register are transferred as command through the serial DMA interface. After transferring the new command through the serial DMA interface, the register is set to NOP (FFh).

Bit 7:0	ALIS_Transmit_Data_2
Type	RW
Default Value	00h
Description	During a DMA transfer in ALIS V3.x mode 2 or 3 the contents of this register are transferred as data through the serial DMA interface.

Internal Register: 14h

Bit 31:0	ALIS Command Register 2
Default Value	00000000h

Bit 31:25	Reserved
Type	H
Default Value	000h
Description	Reserved

Bit 24	New_ALIS_Command_2
Type	RW
Default Value	0b
Description	Bit 24='1': The host has written a new command to the ALIS Command 2 Register. Bit 24='0': Last command written to the ALIS Command 2 Register by the host is processed and the received data is available in the ALIS Received Data 2 Register. This bit is set by software if there is a new command in the ALIS Command 2 Register. After the serial controller has transmitted the new command and the received data is written in the ALIS Received Data 2 Register, this bit is reset by the serial controller.

Internal Register: 14h (cont'd)

Bit 23:16	ALIS_Received_Data_2
Type	RW
Default Value	00h
Description	During a DMA transfer in mode 3 every time a new command is transferred through the serial DMA interface, the received data is fetched and saved in this register. New command means: The command was written through the PCI interface to the ALIS V3.X command register. If only a NOP command (FFh or 00h) is transferred the received data is skipped.

Bit 15:8	ALIS_Command_2
Type	RW
Default Value	00h
Description	During a DMA transfer in mode 3 the contents of this register are transferred as command through the serial DMA interface. After transferring the new command through the serial DMA interface, the register is set to NOP (FFh).

Bit 7:0	ALIS_Transmit_Data_2
Type	RW
Default Value	00h
Description	During a DMA transfer in mode 3 the contents of this register are transferred as data through the serial interface.

Internal Register: 20h

Bit 1	DCL_Out_En
Type	RW
Default Value	0b
Description	Bit 1='0': The DCL signal is input and driven by the PITA.

Bit 0	Serial_Clock_Select
Type	RW
Default Value	0b
Description	Bit 0='1': The serial controller is driven with the external DCL input clock.

5.1.10 Dual Modem/Modem+Voice Mode

Description

- The PITA transmits and receives two 32 bit frames per FSC time slot.
- Each 32 bit frames consists of 16 bit data and 16 bit command/data information.
- For each of the 32 bit frames the 16 bit transmitted data is read out of the TX FIFO.
- The 16 bit transmitted data is written to the RX FIFO.
- The command read/write data for the first 32 bit frame is read out/written to the ALIS Command Register 1 (10h)
- The command read/write data for the second 32 bit frame is read out/written to the ALIS Command Register 2 (14h).
- The internal DMA write counter is incremented every second write transfer to the circular buffer.
- A new frame transmission starts if the FSC is sampled '1' at a negative edge of the DCL signal.
- The PITA starts driving the TXD line with the first bit of the transmitted data at the next positive DCL edge.
- During the transmission the rising DCL edge indicates the start of a bit on the TXD while the falling edge of the DCL is used to latch the RXD signal.
- The PITA stops driving the TXD signal with the positive DCL edge when bit 32 of the first or second transmitted frame is on the TXD line.

Data Organization in the Circular Buffer

	Circular Buffer Memory						
	31 ... 16	15 ... 0		31 ... 16	15	8 7	0
				Don´t care		TX Data 1 Modem 1	
0000h	don't care	TX data 1					
0004h	don't care	TX data 2		31 ... 16	15	8 7	0
0008h	don't care	TX data 3		Don´t care		TX Data 1 Modem 2	
	don't care	TX data 4					
	don't care	TX data 5					
	don't care	TX data 6					
	don't care	TX data 7					
	don't care	TX data 8					
	don't care	TX data 9					
	don't care	TX data 10					
	don't care	TX data 11					
	don't care	TX data 12					
	don't care	TX data 13					
	don't care	TX data 14					
0038h	don't care	TX data 15					
003Ch	don't care	RX data 1					
	don't care	RX data 2					
	don't care	RX data 3					
	don't care	RX data 4					
	don't care	TX data 20					
	don't care	TX data 21					
	don't care	TX data 22					
	don't care	TX data 23					

Timing Diagram for the Dual Modem Mode

125 us

FSC (i)

DCL (i)

TXD (o) — 16 bit data | 8 bit CMD | 8 bit write data | 16 bit data | 8 bit CMD | 8 bit write data

RXD (i) — 16 bit data | 8 bit read data | 16 bit data | 8 bit read data

32 bit data / command frame | 32 bit data / command frame

Timing Diagram for the Dual Modem+Voice Mode
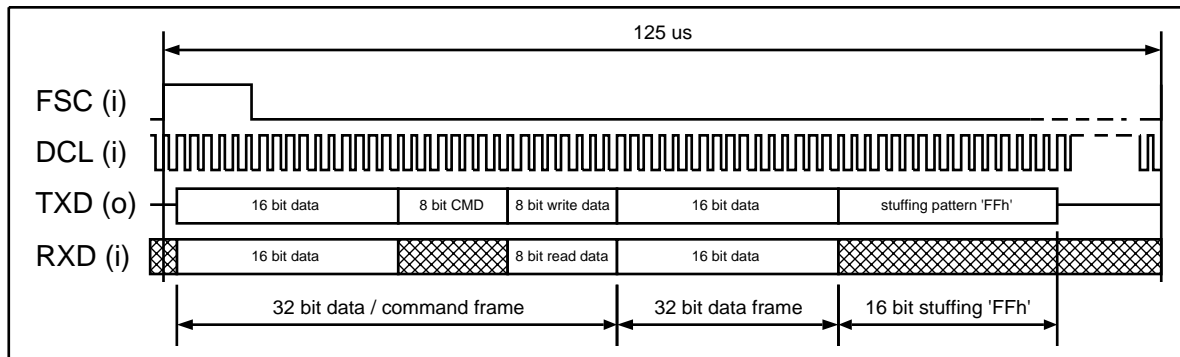
Description of the Timing Diagram

- The second 32 bit frame only consists of the 16 bit voice data.
- The voice data is read out the TX FIFO.
- The voice data is transmitted through the serial DMA interface (MSB first).
- During this transmission the received 16 bit voice data (MSB first) is written to the RX FIFO.

Internal Registers: 04h

Bit 5:0	DMA Select
Type	RW
Default Value	000000b
Description	The DMA Control Register includes the 6 bit parameter DMA Select. Used to define the mode for the next DMA transfer: **Mode 3 ('000100'): Single Dual Modem/Modem + Voice Mode V3.X** With the DMA_Start bit the DMA transfer can be started or stopped.

5.1.11   Loop Back Mode

___

Description

If Loop_Back_Mode is set to '1' transmit data is transferred from the TX FIFO back to the RX FIFO.

___

Mode Diagram

Internal Register: 28h

Bit 0	Loop_Back_Mode
Type	RW
Default Value	0b

Description	• Bit 0='0': The serial controller transmits and receives data/ commands through the serial DMA interface (normal operation mode).
	• Bit 0='1': The serial controller is in loop back mode.
	   – The serial DMA interface reads the data in the transmitting FIFO and writes them in the receiving FIFO.
	   – No data/command transmission will take place on the serial DMA interface.
	   – The serial DMA interface is clocked with the defined Ser_Clock_Sel bit.

5.2 Parallel Interface

Description

The PITA has an 8 bit parallel interface to support three external components.

This parallel interface is implemented in multiplexed and non multiplexed mode.

It works in Infineon/Intel bus mode.

The parallel interface is by default in the non multiplexed mode.

Internal Register: 1Ch

Bit 26	Parallel_interface_mode
Type	RW
Default Value	0b
Description	0: non multiplexed mode 1: multiplexed mode

Bit 24	Softreset_parallel_mode
Type	RW
Default Value	0b
Description	0: Deactivates the reset signal PRST to the application. 1: Activates the high active reset signal PRST to the application.

Mapping between PCI Data and Parallel Interface Data

Data on the PCI bus AD31-0	PCI Byte Enables $\overline{\text{C/BE3-0}}$	Data on the Parallel Interface Data bus PAD7-0
AD[31-8] = Don't Care AD[7-0] = Parallel Interface Data	"XXX0"	PAD[7-0] = AD[7-0]
AD[31-8] = Don't Care AD[7-0] = Parallel Interface Data	"XXX1"	No transaction, PCI interface disconnects with Target Abort.

Address Mapping of the 4-kbyte PCI Address Space to the Parallel Interface

Address on the PCI address bus AD11-0	Chip Select on the parallel interface	Address on the parallel interface address bus PAD7-0 = AD9-2 (mux mode) PA7-0 = AD9-2 (non-mux mode)
3FFh - 000h	$\overline{\text{CS0}}$	FFh - 00h
7FFh - 400h	$\overline{\text{CS1}}$	FFh - 00h
BFFh - 800h	$\overline{\text{CS2}}$	FFh - 00h
FFFh - C00h	none	(not used)

Modes and Timing of the Parallel Interface

5.2.1   ALE after System Reset

Timing Diagram

Description

Both ALE and PRST are high during $\overline{RST}$ and remain high for a maximum of 4 cycles after $\overline{RST}$ goes deasserted.

5.2.2   ALE after internal Software Reset

Timing Diagram
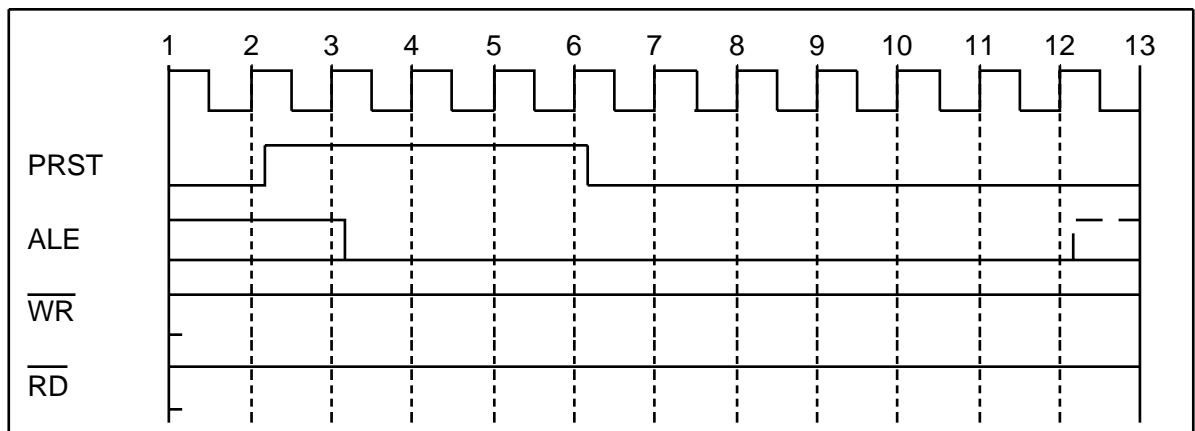
Description

- After the internal Soft Reset is deasserted the same behavior as in „ALE after System Reset" generated.
- The soft reset bit in the internal registers can only be set or reset if the parallel interface is in idle state.
- If ALE is high before PAR_RST is asserted, it goes to low one cycle after PRST and takes the new value depending on the PAR_MOD bit in the 6th cycle after PRST is deasserted.

5.2.3 ALE after setting the Parallel Interface Mode Bit

Timing Diagram
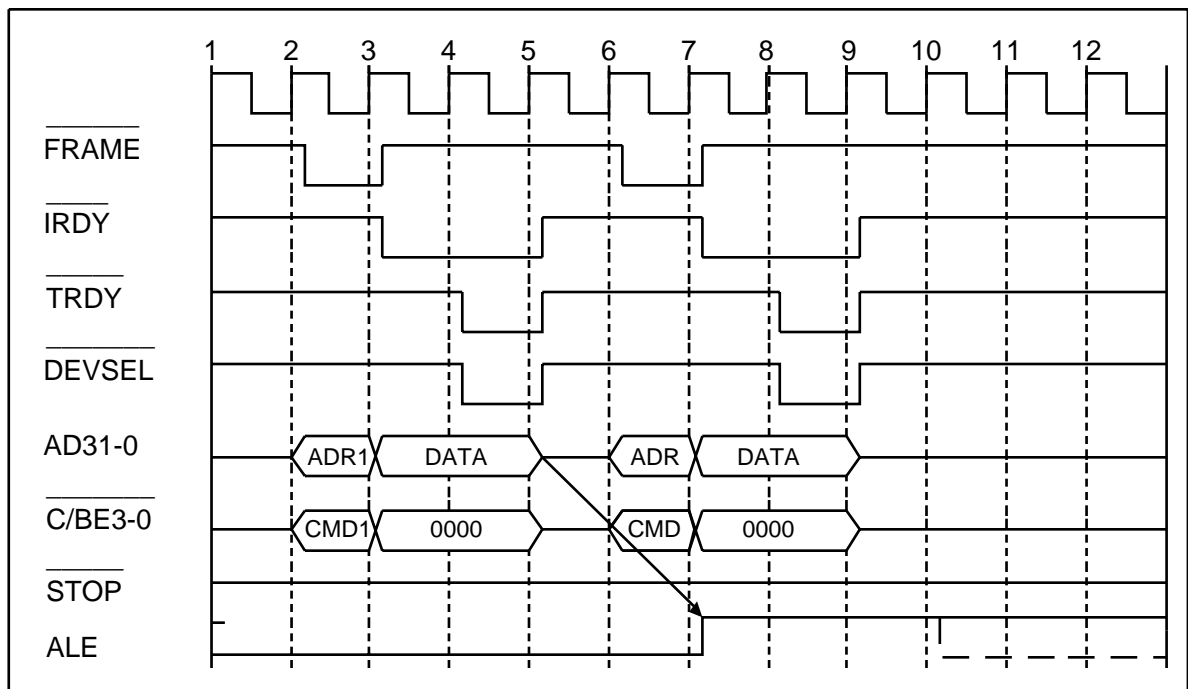
Description

- The parallel interface is in non multiplexed mode by default.
- To set the parallel interface into multiplexed mode:
  The Parallel_Interface_Mode bit has to be set to '1' after reset.
- Two PCI clocks after finishing this data phase the ALE signal is asserted.

5.2.4 Non Multiplexed Mode (Write Transaction)
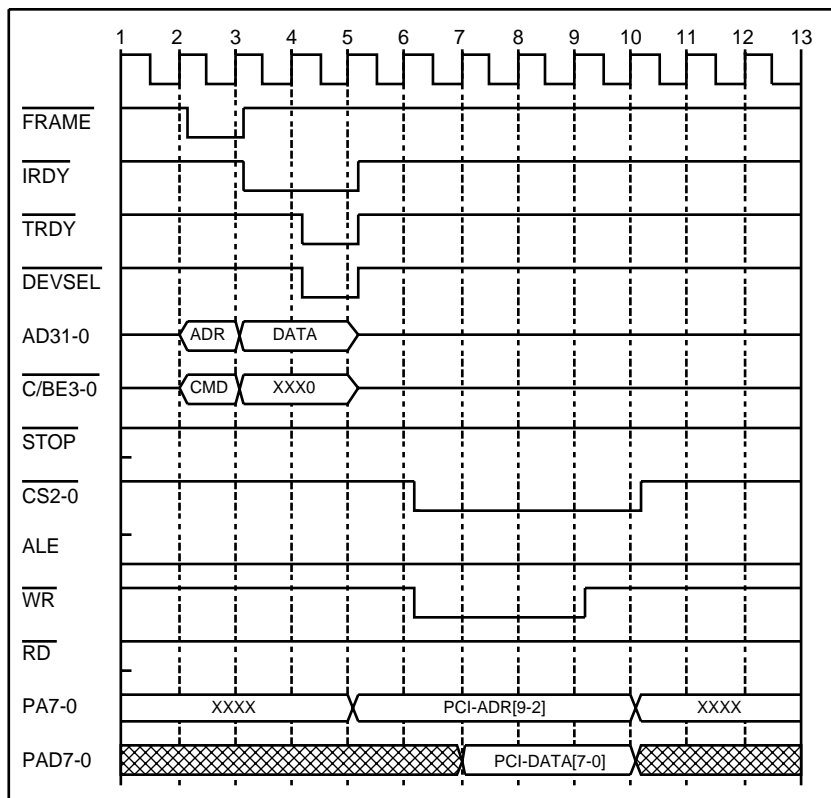
Timing Diagram

Description

- After the address phase on the PCI bus (clock3) and the $\overline{C/BE0}$=0 verification the address decoding phase of the target (clocks 3 to 4) is active.
- The byte address for the transaction on the parallel interface is generated out of the PCI address AD9-2 by mapping it to the parallel interface address bus PA7-0.
- One PCI clock after the PCI data phase is finished the data from the PCI bus is placed on the data bus PAD7-0 (clock 5) and the write transaction starts.
- The data is placed from the PCI bus on PAD7-0 asserting the $\overline{WR}$ signal and a $\overline{CS2\text{-}0}$ signal.
- A new access to the parallel interface could be accepted with an address phase at clock 9. Any access before would be cancelled with Retry because the PCI Interface is processing the last access.

Example

As an example the value 0A4h shall be written at address 005h of the device connected to $\overline{CS1}$. In this example the Base Address Register 1 (BAR1) shall contain the address 20004000h.

- $\overline{CS1}$ is activated for the address space 400h to 7FFh. Therefore the device's address space starts at PCI address BAR1+400h= 20004400h.
- Only the lower byte of each 32bit word transferred to and from the PITA-2 over the PCI bus is used for the parallel interface. Therefore the relative PCI address is four times the relative device address: rel. PCI address = four times 005h = 014h.
- The absolute PCI address for the data transfer is BAR1+400h+014h=20004414h.
- Only the low byte of a 32 bit data word matters, the upper three bytes are ignored by the PITA-2. In order to write the value 0A4h the data word 000000A4 can be written to PCI address 20004414h.

5.2.5 Non Multiplexed Mode (Read Transaction)
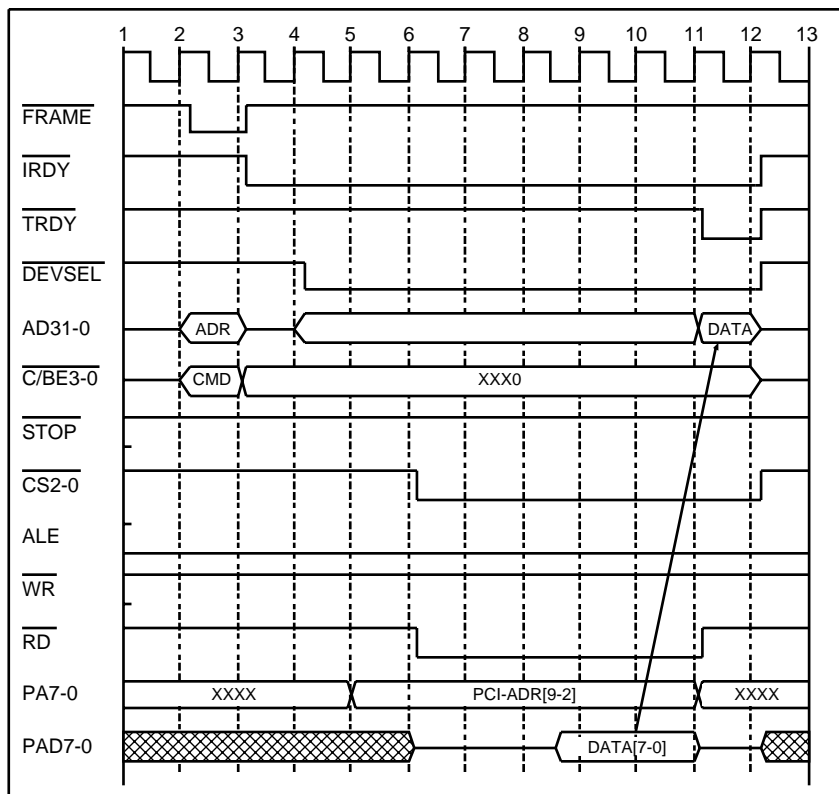
Timing Diagram

Description

- After the address phase on the PCI bus (clock3) and the $\overline{C/BE0}$=0 verification the address decoding phase of the target (clocks 3 to 4) is active.
- The byte address for the transaction on the parallel interface is generated out of the PCI address AD9-2 by mapping it to the parallel interface address bus PA7-0 (clock 5).
- The following PCI clock asserts the signals $\overline{RD}$ and $\overline{CS2\text{-}0}$.
- After 5 clocks the $\overline{RD}$ signal is deasserted.
- The data from PAD7-0 is fetched.
- With the next clock the data is placed on the PCI bus and the data phase is finished by deasserting the $\overline{TRDY}$ signal.
- The 8 bit data from the parallel interface is placed an the last significant byte of the PCI data bus AD7-0.

5.2.6 Multiplexed Mode (Write Transaction)
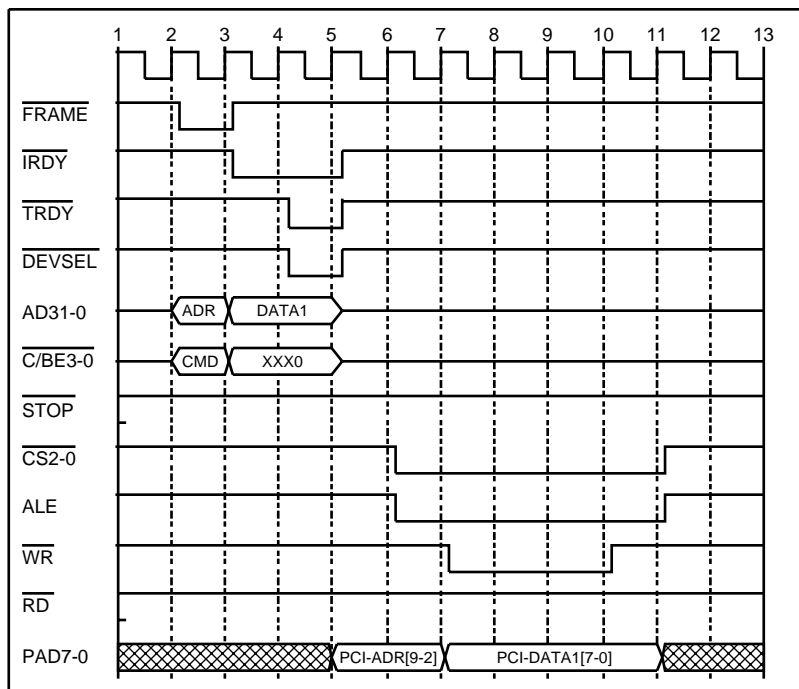
Timing Diagram

Description

- After the address phase on the PCI bus (clock 3) and the $\overline{\text{C/BE0}}$=0 verification the address decoding phase of the target (clocks 3 to 4) is active.
- The byte address for the transaction on the parallel interface address is generated out of the PCI address AD9-2 by mapping it to the parallel interface address bus PA7-0.
- One PCI clock after the PCI data phase is finished the data from the PCI bus is placed on the data bus PAD7-0 (clock 5) and the write transaction starts.
- The data is placed from the PCI bus on PAD7-0 asserting the $\overline{\text{CS2-0}}$ signal.
- The ALE signal is deasserted.
- With the following PCI clock the data from the PCI bus is placed on PAD7-0 (clock5).
- The $\overline{\text{WR}}$ signal is asserted.
- A new access to the parallel interface could be accepted with an address phase at clock 11. Any access before would be cancelled with Retry because the PCI Interface is processing the last access.

5.2.7 Multiplexed Mode (Read Transaction)
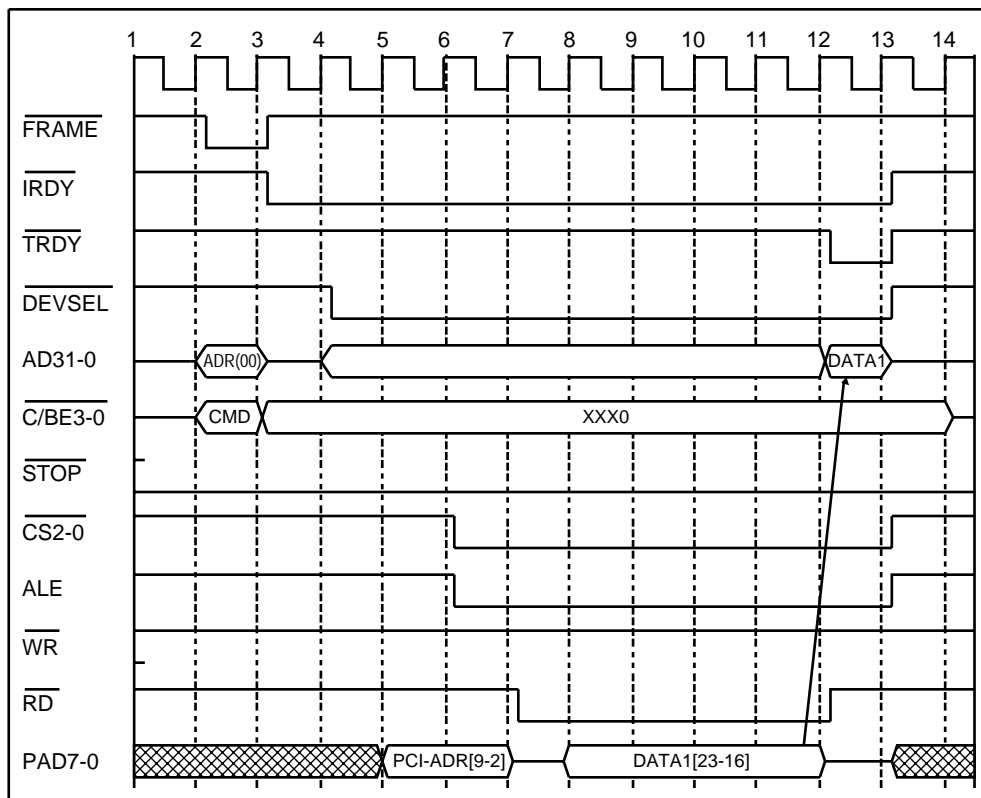
Timing Diagram

Description

- After the address phase on the PCI bus (clock 3) $\overline{\text{and the C/BE0}}$=0 verification the address decoding phase of the target (clocks 3 to 4) is active.
- The byte address for the transaction on the parallel interface is generated out of the PCI address AD9-2 by mapping it to the parallel interface address bus PA7-0 (clock 5).
- The following PCI clock asserts the ALE signal.
- After 2 clocks the ALE signal is deasserted.
- The address is held for one more clock.
- After 5 clocks the $\overline{\text{RD}}$ signal is deasserted.
- At the same time the data is latched in die PCI output registers.
- $\overline{\text{TRDY}}$ is asserted on the PCI bus to finish the data phase.
- At the next clock the $\overline{\text{CS2-0}}$ and ALE signals are deasserted.

5.2.8   Transaction Disconnect with Target Abort

Timing Diagram
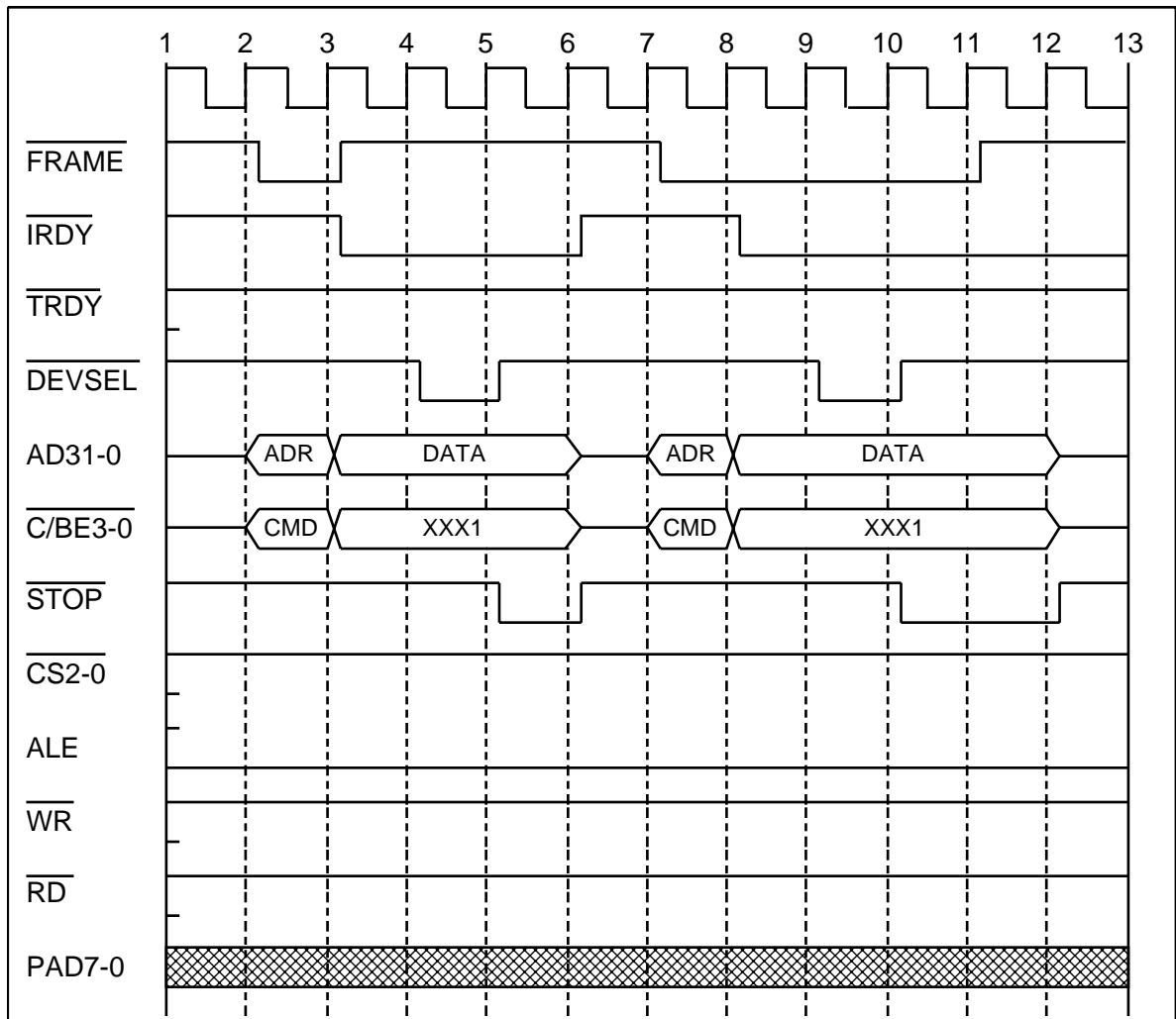
Description

$\overline{\text{C/BE0}}$ = 1: No transaction is started on selected parallel interface, due to the wrong byte enable. The PCI Master Target Controller disconnects the transaction with target abort.

Configuration Space Register: 04h

Bit 30	System_Error_Signaled
Type	RC
Default Value	0b
Description	This bit is set by the PITA's PCI Master, if the master asserts the system error signal on the PCI bus. This occurs if a transaction initiated by the PITA is disconnected with target abort.

Bit 29	Master_Abort_Detected
Type	RC
Default Value	0b
Description	If no fast/medium/slow or subtractive slave reacts to a PCI transaction initiated by the PCI Master, the master will discard the transaction and set this bit.

Bit 28	Master_Abort_Detected
Type	RC
Default Value	0b
Description	If a PCI transaction initiated by the PCI Master is disconnected with Target Abort, the PCI master will set this bit. The PCI Master is not allowed to start a new PCI transaction, until this bit is deasserted.

Configuration Space Register: 04h (cont'd)

Bit 27	Target_Abort_Signaled
Type	RC
Default Value	0b
Description	This bit is set by the PCI interface if a transaction was disconnected with Target Abort. The PITA will disconnect transactions with Target Abort if illegal byte enables are detected.

Bit 8	System_Error_Enable
Type	RW
Default Value	0b
Description	If this bit is asserted, the PCI Master will assert the System Error Signal ($\overline{SERR}$) if it receives a target abort during a transaction initiated by itself.

Bit 2	Master_Enable
Type	RW
Default Value	0b
Description	If this bit is set to '0' the PCI Master is not allowed to start any transaction on the PCI Bus.

5.2.9 Transaction Termination with Retry

Description'

Retry means that the PITA finishes a transaction without a data transfer by asserting the signal $\overline{\text{STOP}}$, because the parallel interface processes another transaction.

The PCI Master Target Controller has to repeat the transaction until a slave accepts the transaction with data transfer or target abort. This sequence is invisible for the software.

Timing Diagram
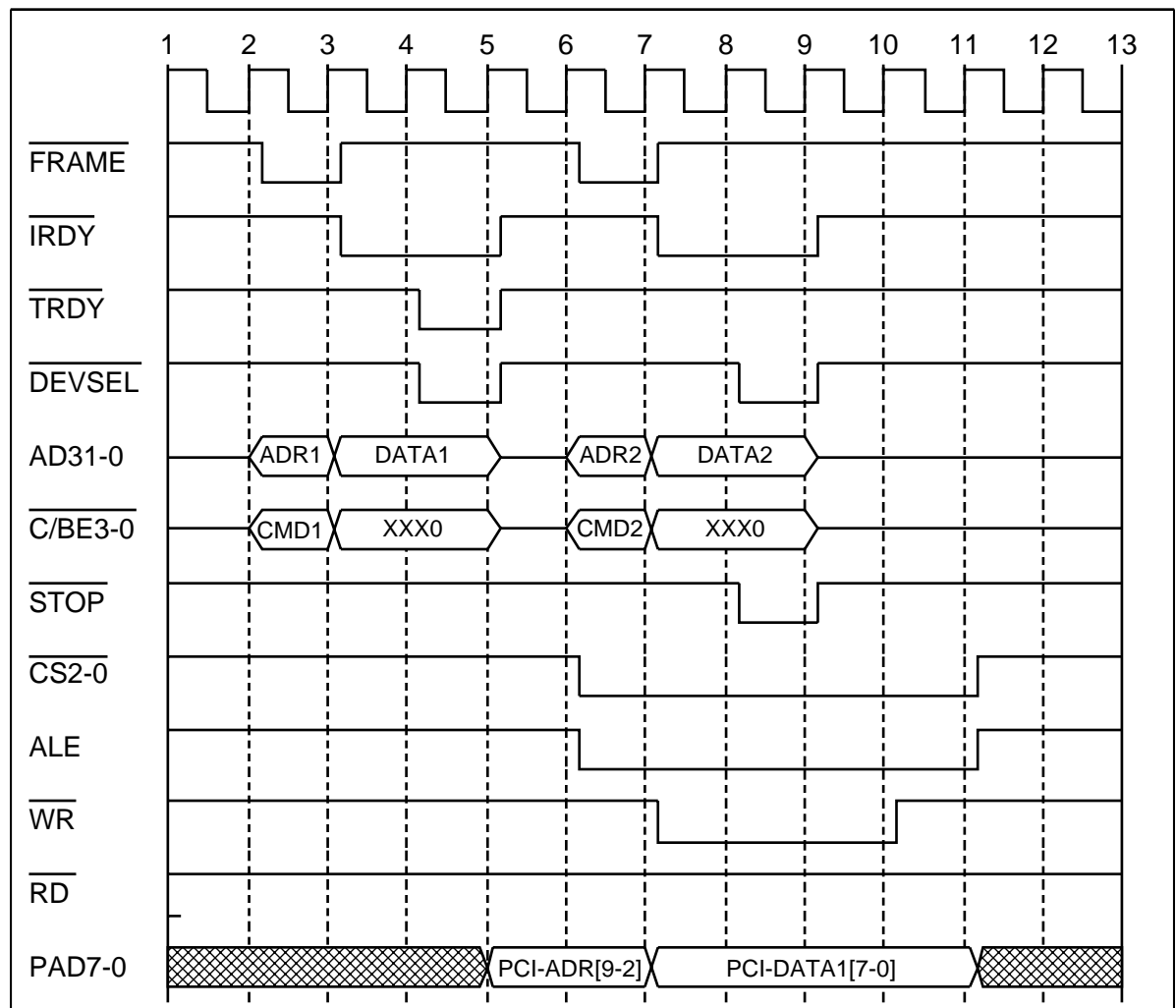
Explanation of ADR/CMD and ADR2/CMD2

ADR/CMD: The PCI Master Target Controller accepts the write transaction

ADR2/CMD2: The second transaction is retried.

5.2.10　Timing of the Parallel Interface

Read Timing
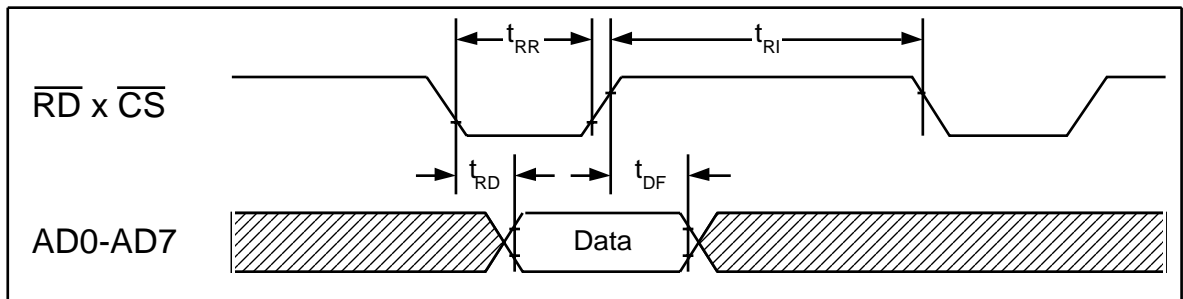
Write Timing
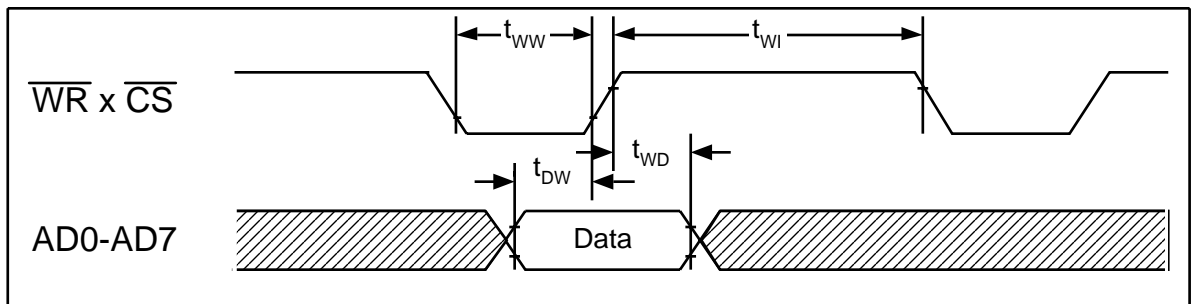
Multiplexed Address Timing
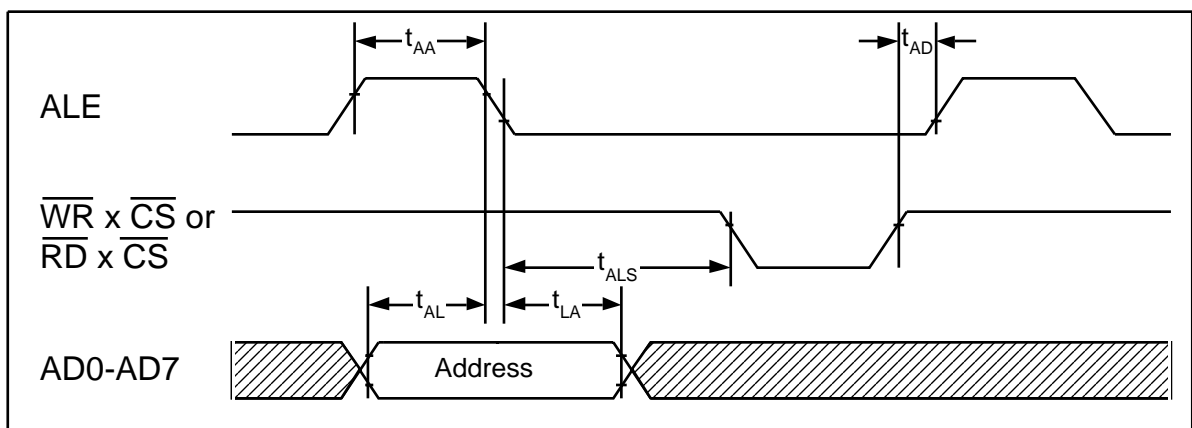
Non Multiplexed Address Timing
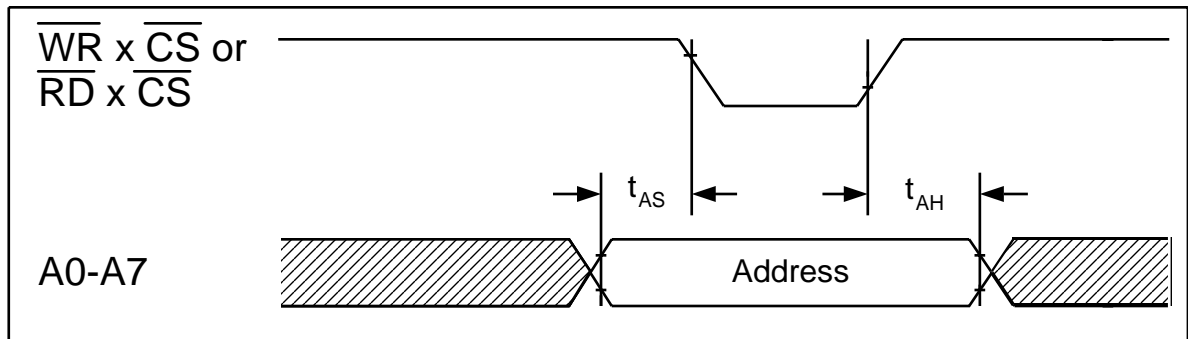
Application Reset and Interrupt Timing
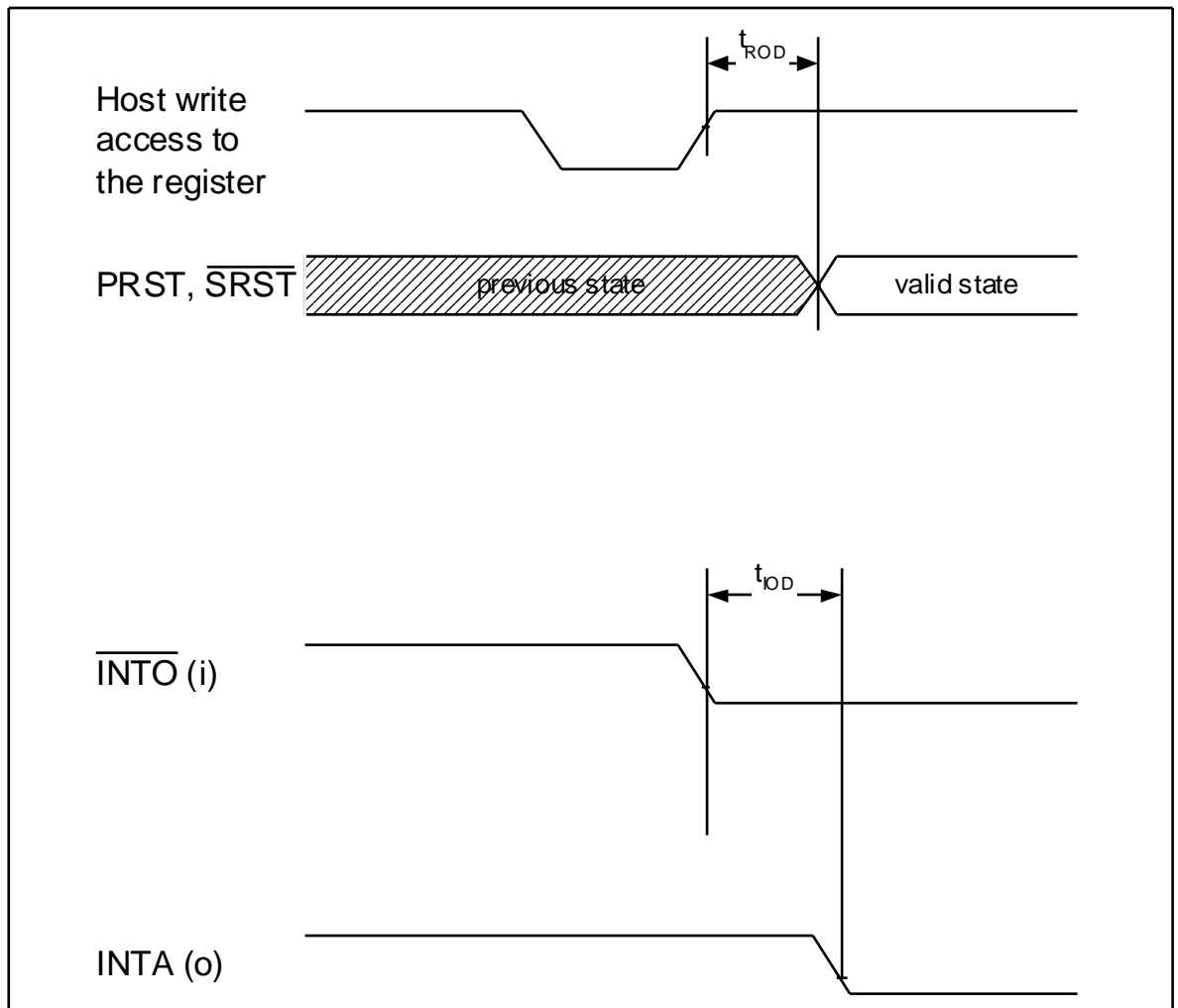
Abbreviations of the Timing Diagrams

Parameter	Symbol	PCI Clock Cycles	Limit Values		Unit
			min.	max.	
ALE pulse width	t_{AA}	5	150		ns
Address setup time to ALE	t_{AL}	1	30		ns
Address hold time from ALE	t_{LA}	1	30		ns
Address latch setup time to $\overline{WR}$, $\overline{RD}$	t_{ALS}	1	30		ns
Address setup time	t_{AS}	1	30		ns
Address hold time	t_{AH}	1	30		ns
ALE guard time	t_{AD}	1	30		ns
$\overline{RD}$ pulse width	t_{RR}	5	150		ns
Data output delay from $\overline{RD}$	t_{RD}	5		150	ns
Data float from $\overline{RD}$	t_{DF}	1		30	ns
$\overline{RD}$ control interval	t_{RI}	5	150		ns
$\overline{W}$ pulse width	t_{WW}	3	90		ns
Data setup time to $\overline{W}$ x $\overline{CS}$	t_{DW}	2	60		ns
Data hold time $\overline{W}$ x $\overline{CS}$	t_{WD}	1	30		ns
$\overline{W}$ control interval	t_{WI}	3	90		ns
Reset Output Delay	t_{ROD}	3		90	ns
Interrupt Output Delay	t_{IOD}	2		60	ns

5.3 General Purpose I/O Interface

Overview

5.3.1 Information about the GP I/O Interface

Description

For additional access to external devices with a slow interface behavior a 4 bit General Purpose I/O interface is implemented in the PITA.

Pinning

Pin	Pin Name	General Purpose I/O Function	SPI EEPROM Function
2	GP0	I/O/Int.	SO
3	GP1	I/O/Int.	SI
4	GP2	I/O/Int.	SCK
5	GP3	I/O/Int.	–

Application Interrupt

- The PCI interface supports a separate interrupt input with programmable polarity.
- The four pins of the general purpose I/O interface can be used as additional interrupt inputs.
- Each of these five interrupts has an Interrupt_Enable bit and an Interrupt_Control_Status bit.
- For the separate input the enable an polarity bits are located in the Interrupt Control Register.
- For the General Purpose I/O the enable bits are located in the Interface Control Register.

Control Registers for GPx Pins

Register	Register Bit	Description
Interrupt Control Register - ICR	GPx_INT	GP Interrupt Status
GP I/O Interface Control Register	GPx_INT_En	GP Interrupt Enable
	GPx_OUT_En	GP Output Enable
	GPx_OUT	GP Output Value
	GPx_IN	GP Input Value

5.3.2   Timing of the GP I/O Interface

Timing Diagram
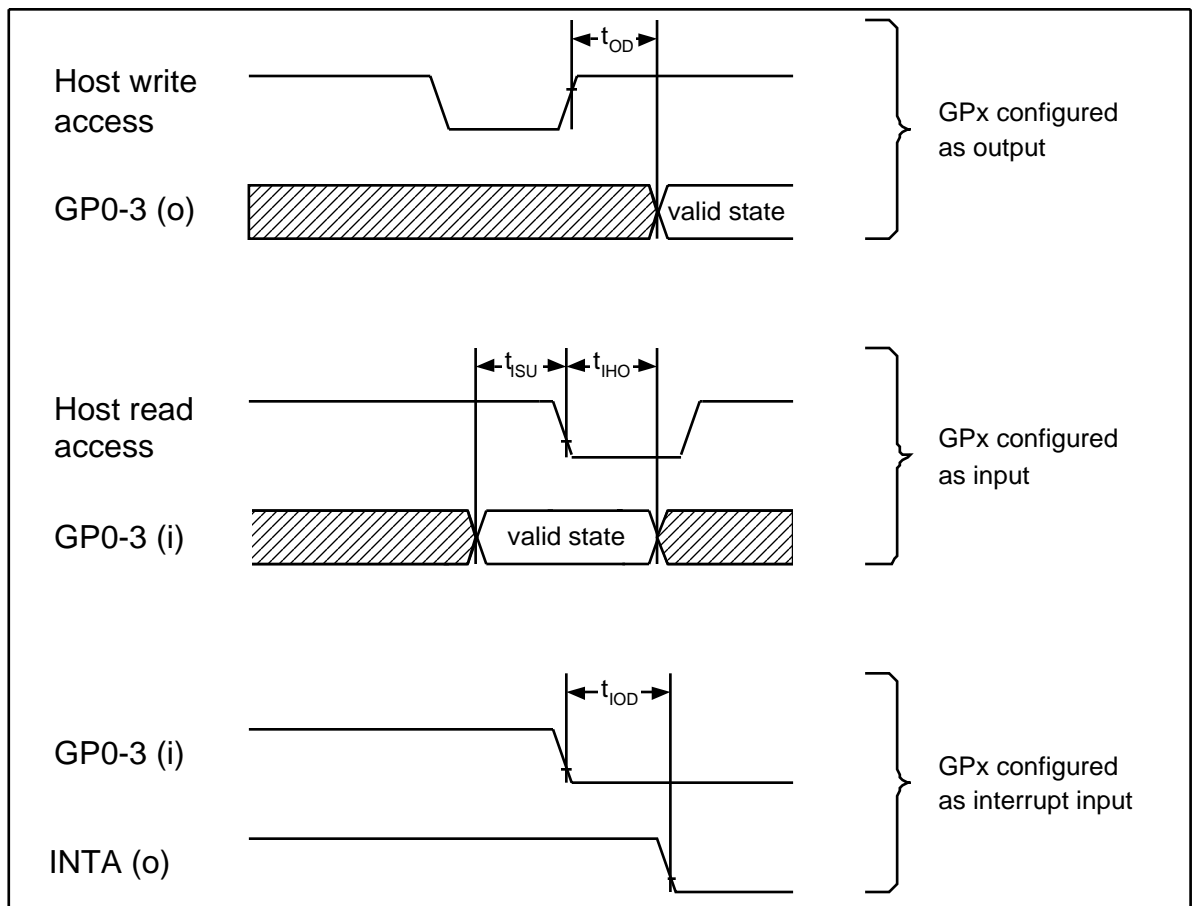
Abbreviations of the Timing Diagram

Parameter	Symbol	Limit Values		Unit
		min.	**max.**	
GPx Output Data Delay	t_{OD}		90	ns
GPx Input Data Setup	t_{ISU}	30		ns
GPx Input Data Hold	t_{IHO}	30		ns
GPx Interrupt Output Delay	t_{IOD}		90	ns

5.3.3   Internal Registers of the GP I/O Interface

Internal Register: 00h

Bit 5	GP3_INT
Type	RC
Default Value	0b
Description	The GP3 pin can be used as 'active low' interrupt input if GP3_Int_En='1' and GP3_Out_En='0'. The bit is set to '1' if both are true and low is detected at this pin.

Bit 4	GP2_INT
Type	RC
Default Value	0b
Description	The GP2 pin can be used as 'active low' interrupt input if GP2_Int_En='1' and GP2_Out_En='0'. The bit is set to '1' if both are true and low is detected at this pin.

Bit 3	GP1_INT
Type	RC
Default Value	0b
Description	The GP1 pin can be used as 'active low' interrupt input if GP1_Int_En='1' and GP1_Out_En='0'.

Internal Register: 00h (cont'd)

Bit 2	GP0_INT
Type	RC
Default Value	0b
Description	The GP0 pin can be used as 'active low' interrupt input if GP0_Int_En='1' and GP0_Out_En='0'.

Internal Register: 18h

Bit 27	GP3_Int_En
Type	RW
Default Value	0b
Description	Bit 27='1': GP3 is configured as input, the pin is used as an interrupt input with GP3_Int_en as corresponding bit in the Interrupt Control Register. Bit 27='1': GP3 is not used as an interrupt pin.

Bit 26	GP2_Int_En
Type	RW
Default Value	0b
Description	Bit 26='1': GP2 is configured as input, the pin is used as an interrupt input with GP2_Int_en as corresponding bit in the Interrupt Control Register. Bit 26='0': GP2 is not used as an interrupt pin.

Internal Register: 18h (cont'd)

Bit 25	GP1_Int_En
Type	RW
Default Value	0b
Description	Bit 25='1': GP1 is configured as input, the pin is used as an interrupt input with GP1_Int_en as corresponding bit in the Interrupt Control Register. Bit 25='0': GP1 is not used as an interrupt pin.

Bit 24	GP0_Int_En
Type	RW
Default Value	0b
Description	Bit 24='1': GP0 is configured as input, the pin is used as an interrupt input with GP0_Int_en as corresponding bit in the Interrupt Control Register. Bit 24='0': GP0 is not used as an interrupt pin.

Bit 19	GP3_Out_En
Type	RW
Default Value	0b
Description	Bit 19='1': GP_3 is configured as output pin. Bit 19='0': GP_3 is configured as input pin.

Bit 18	GP2_Out_En
Type	RW
Default Value	0b
Description	Bit 18='1': GP_2 is configured as output pin. Bit 18='0': GP_2 is configured as input pin.

Internal Register: 18h (cont'd)

Bit 17	GP1_Out_En
Type	RW
Default Value	0b
Description	Bit 17='1': GP_1 is configured as output pin. Bit 17='0': GP_1 is configured as input pin.

Bit 16	GP0_Out_En
Type	RW
Default Value	0b
Description	Bit 16='1': GP_0 is configured as output pin. Bit 16='0': GP_0 is configured as input pin.

Bit 11	GP3_IN
Type	R
Description	Actual Value on the GP3 pin (pin feedback)

Bit 10	GP2_IN
Type	R
Description	Actual Value on the GP2 pin (pin feedback)

Bit 9	GP1_IN
Type	R
Description	Actual Value on the GP1 pin (pin feedback)

Internal Register: 18h (cont'd)

Bit 8	GP0_IN
Type	R
Description	Actual Value on the GP0 pin (pin feedback)

Bit 3	GP3_OUT
Type	RW
Default Value	0b
Description	The GP3 pin is driven with the value written to this output register if the GP3_OUT_En is set to '1'.

Bit 2	GP2_OUT
Type	RW
Default Value	0b
Description	The GP2 pin is driven with the value written to this output register if the GP2_OUT_En is set to '1'.

Bit 1	GP1_OUT
Type	RW
Default Value	0b
Description	The GP1 pin is driven with the value written to this output register if the GP1_OUT_En is set to '1'.

Internal Register: 18h (cont'd)

Bit 0	GP0_OUT
Type	RW
Default Value	0b
Description	The GP0 pin is driven with the value written to this output register if the GP0_OUT_En is set to '1'.

5.3.4   Input Mode

___

Description

For using a general purpose I/O pin as input pin, the control register must be configured as follows:

GPx_OUT_En = '0'   (Output disabled)

GPx_INT_En   = '0'   (Interrupt disabled)

(x := [0, 3])

Description of the internal register 18h on page 102.

The GPx_OUT and GPx_INT bits can be treated as don't care in this mode. The current signal value at the pin GPx can be read from register bit GPx_IN.

___

Internal Structure of a GPx Input Pin
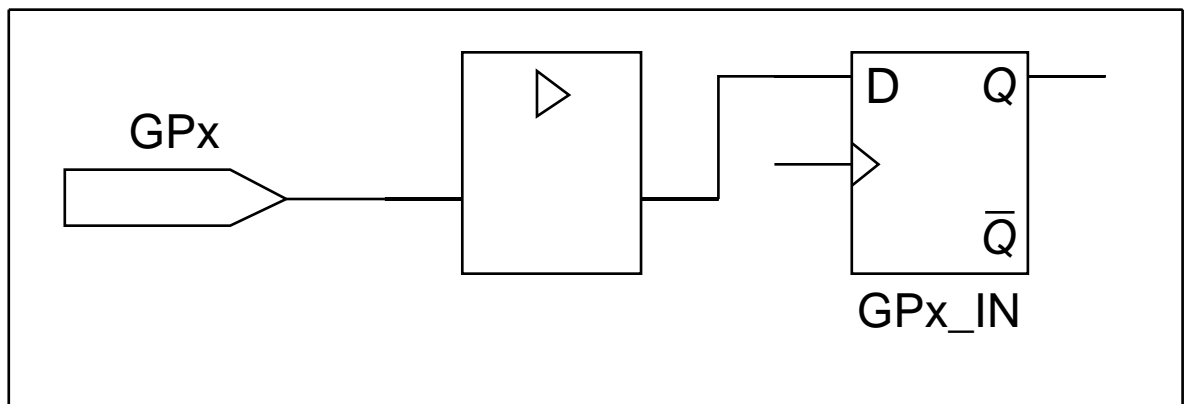
GPx

D   Q

$\overline{Q}$

GPx_IN

___

Timing Diagram

t_{ISU} t_{IHO}

Host read access

GP0-3 (i)   valid state

GPx configured as input

___
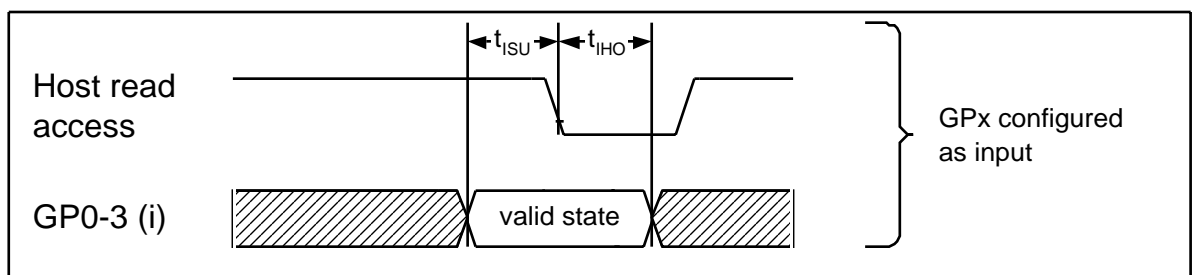
Abbreviations of the Timing Diagram

Parameter	Symbol	Limit Values		Unit
		min.	**max.**	
GPx Input Data Setup	t_{ISU}	30		ns
GPx Input Data Hold	t_{IHO}	30		ns

5.3.5   Output Mode

___

Description

For using a general purpose I/O pin as output pin, the control register must be configured as follows:

GPx_OUT_En = '1'   (Output enabled)

GPx_INT_En   =   'don't care'

$(x := [0, 3])$

Description of the internal register 18h on page 102.

The GPx_IN and GPx_INT register bits can be treated as don't care in this mode. The GPx pin will drive the connected signal line with the value defined in the GPx_OUT register bit, which is programmed by the host.

___

Internal Structure of a GPx Output Pin
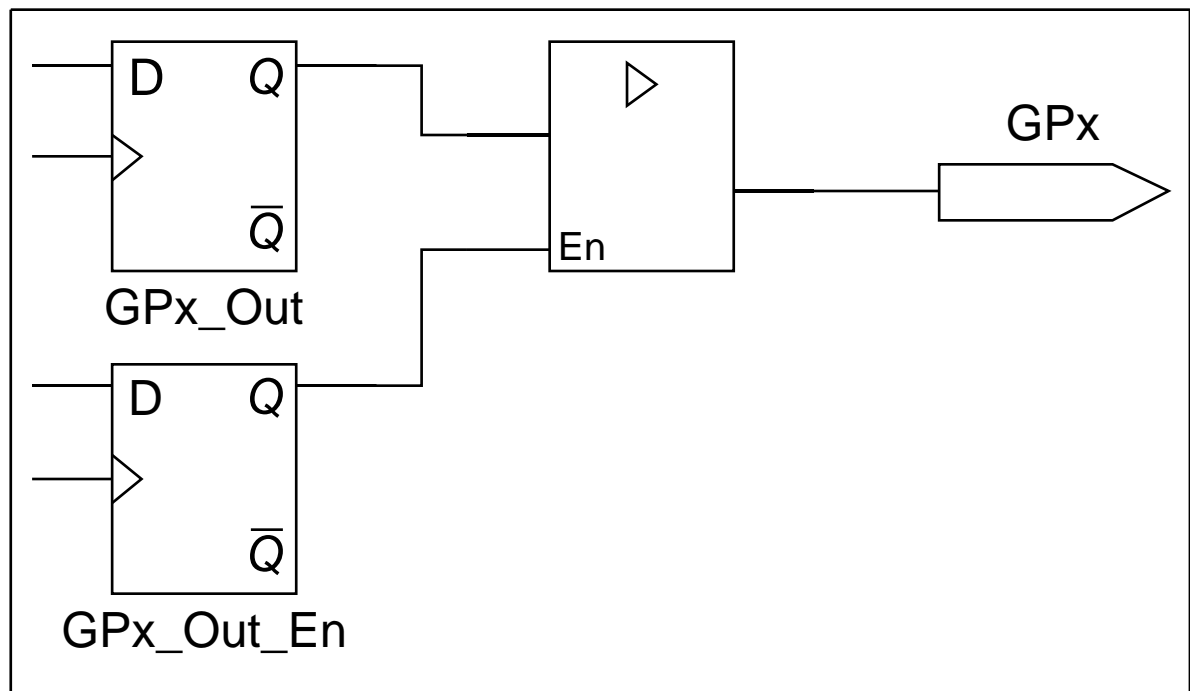
Timing Diagram
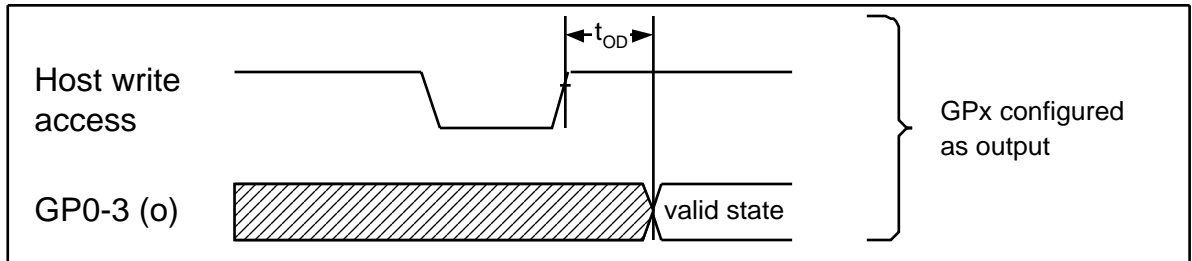
Abbreviation of the Timing Diagram

Parameter	Symbol	Limit Values		Unit
		min.	**max.**	
GPx Output Data Delay	t_{OD}		90	ns

5.3.6   Interrupt Mode

Description

For using a general purpose I/O pin as output pin, the control register must be configured as follows:

GPx_OUT_En = '1'   (Output disabled)

GPx_INT_En   = '1'   (Interrupt enabled)

(x := [0, 3])

Description of the internal register 18h on page 102.

The GPx_OUT register bit can be treated as don't care in this mode. The GPx pin acts as an active low interrupt input pin.

If the device detects '0' at the GPx pin

- the GPx_INT register is set to '1'
- an interrupt on the PCI bus is generated
- the current state of the GPx pin can be read from GPx_IN bit or can be treated as don't care.

Internal Structure of a GPx Interrupt Input pin
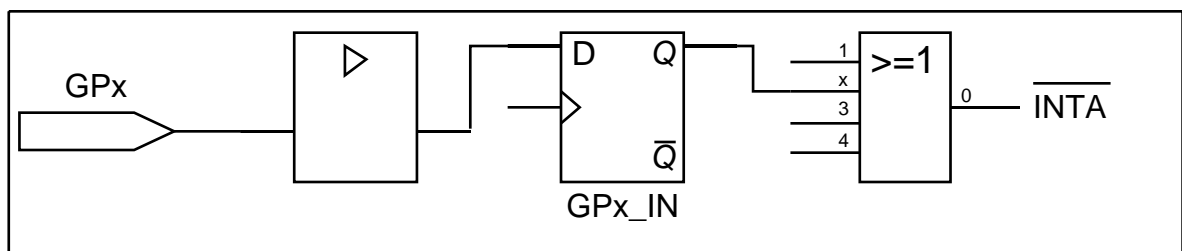
Timing Diagram
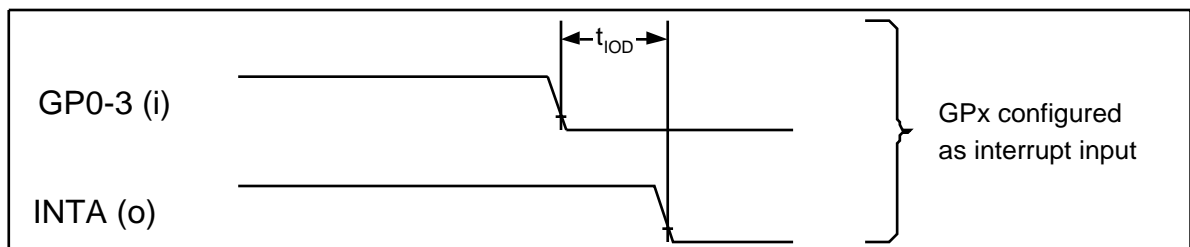
Abbreviation of the Timing Diagram

Parameter	Symbol	Limit Values		Unit
		min.	**max.**	
GPx Interrupt Output Delay	t_{IOD}		90	ns

5.3.7 Usage of the GP I/O Interface as ALIS V2.1 Control Interface

The serial control interface of the ALIS V2.1 can be realized by software using the General Purpose I/O pins.

The GP3 pin is used as $\overline{CS}$ pin while the other three GPx pins are shared with the SPI EEPROM Interface.

The $\overline{INT0}$ pin of the PITA can be programmed to be active on a H level. Therefore this pin can be connected directly to the INT pin of the ALIS.

The GP3 pin is driven high during the automatic EEPROM configuration phase after a system reset to disable the ALIS V2.1 control interface.

Description

PITA Signals		ALIS Signals	Description
GP3	Out	CS	Chip select (active low), for enabling the PSB4596 Control Interface.
GP2	Out	DCLK	Clock signal for the Control Interface. (PSB4596 accepts 1 kHz to 1024 kHz)
GP1	In	DOUT	Data input for PITA, data output from PSB4596. Data input is latched at the negative DCLK edge.
GP0	Out	DIN	Data output from PITA, data input for PSB4596. Data output changes with the rising DCLK edge.
$\overline{INT0}$	In	INT	Interrupt signal (high active)
SRST	Out	RESET	Reset signal (low active)

Timing Diagram for a Write Transaction with two Data Bytes transmitted
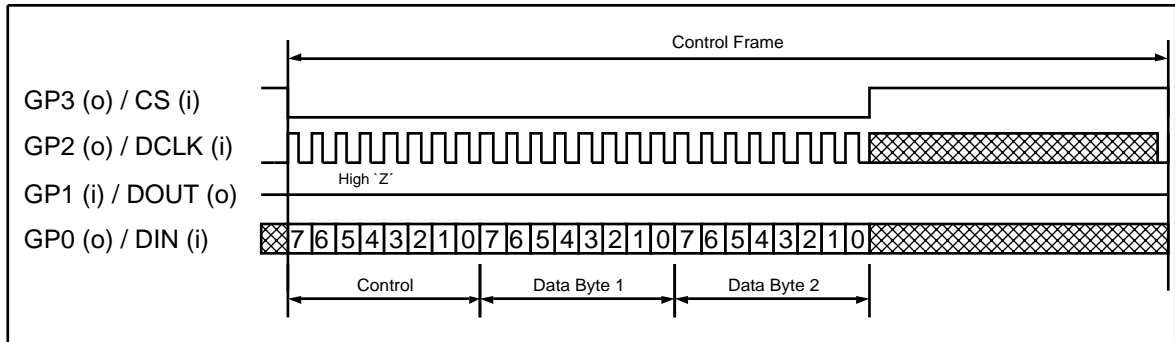
Timing Diagram for a Read Access with one Data Byte received via DOUT
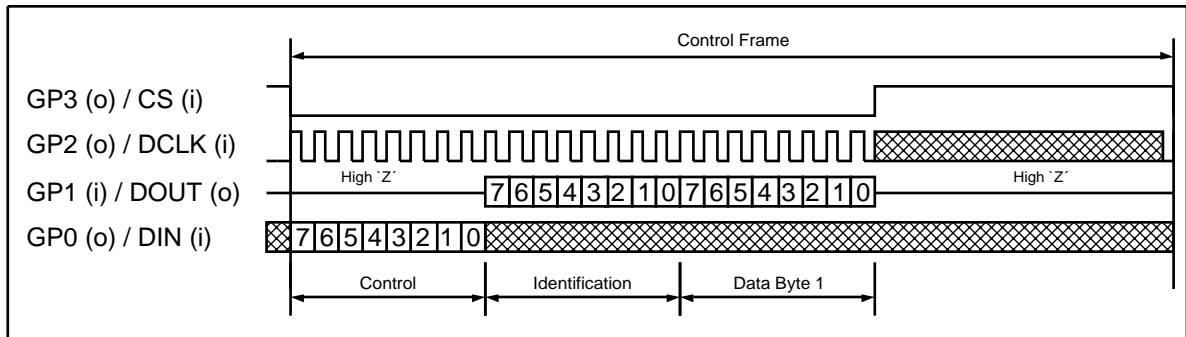
5.4 SPI EEPROM Interface

Overview

5.4.1 Information about the SPI EEPROM Interface

Description

Three pins are used to provide an SPI^TM-compatible serial interface to a 256 x 8 bit EEPROM. These pins also do double-duty as part of the General Purpose Interface. Two other pins are also used to select the EEPROM chip and to enable/disable the automatic reconfiguration of the configuration space by the EEPROM. This would occur after a system reset.

The EEPROM can be used for:

- Automatic reconfiguration of the PITA.
- Customer specific purposes (e.g. storage of serial board numbers).

Automatic reconfiguration of the PITA

Parts of the PCI Configuration Space can be configured with data from this external EEPROM after system reset. The following sequence is processed by the PITA:

- The PITA checks:
  - Whether the ELD (EEPROM_Load) pin is clamped to '1'.
  - Whether the first byte in the EEPROM (address location 00h) is AAh.
- If the first step was successful, the PITA starts:
  - Reading out four bytes starting with address 01h.
  - Writing the read values in the configuration space address 00h.
  - Reading out the next four bytes.
  - Writing the read values in the configuration space address 04h.
  - And so on.

Note

During the configuration phase, all access to the PCI interface are answered with 'Retry' by the PITA.

Using the EEPROM for customer specific purposes

The contents of the EEPROM can be programmed by writing a command to the EEPROM Control Register and initiating a read/write transaction to the EEPROM.

Note

If the automatic reconfiguration of the PITA is used (ELD pin clamped to '1'), only those addresses in the EEPROM not mapped to the PCI configuration space should be used.

Starting a read or write transaction

The contents of the EEPROM can be programmed by writing a command to the EEPROM Control Register and initiating a read/write transaction to the EEPROM.

- The host writes
  - The EEPROM Command value before the next EEPROM transfer is started.
  - The EEPROM Byte Address value for read or write access.
  - The EEPROM Data value for the 'Write Status Register' and 'Write Data to Memory Array'.
- The host sets the EEPROM_Start bit.
- If the EEPROM interface detects the asserted EEPROM_Start bit; it
  - Interprets the EEPROM Command.
- Starts the read or write transaction to the connected EEPROM.
- If the transactions are started via the EEPROM Control register, then the EEPROM interface does not check for a connected EEPROM.

After finishing the transaction:

- The EEPROM control module:
  - Deasserts the EEPROM_Start bit.
  - Generates an interrupt in the EEPROM Control Int Register, if the EEPROM_Control_Int_en bit is set to '1'.
- If The EEPROM Command Register is set to RDSR or READ, then the value of the EEPROM is available in the EEPROM Data Register.

Connection of an ALIS V2.1 device to the Serial Control Interface

For the connection of an ALIS V2.1 device to the Serial Control Interface of the PITA the GP3 pin is additionally used as low active chip select signal CS to the ALIS V2.1.

The GP3 pin is always driven 'high' and therefore the ALIS V2.1 interface is inactive during the phase of automatic initialization of the PCI Configuration Space.

5.4.2 Timing of the SPI EEPROM Interface

Timing Diagram
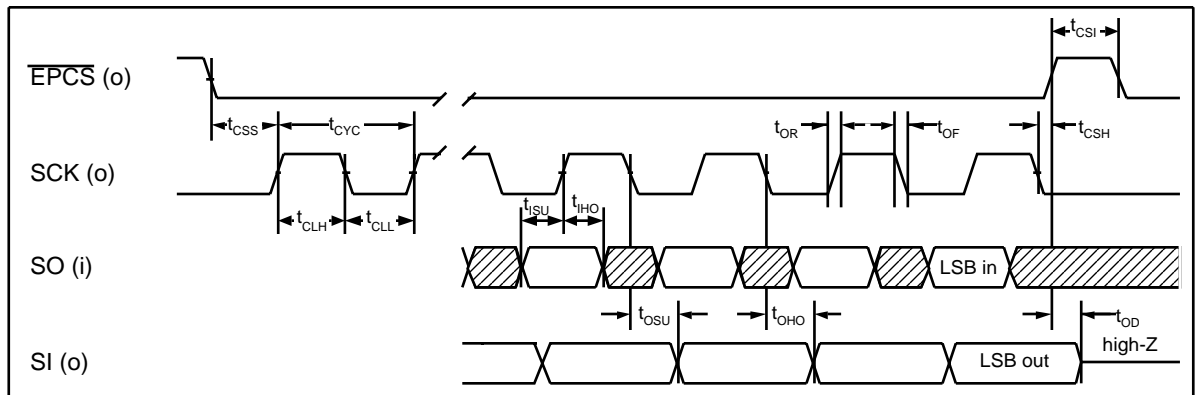
Abbreviations of the Timing Diagram

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Chip Select Setup Time	t_{CSS}	500		ns
Chip Select Hold Time	t_{CSH}	500		ns
Chip Select Inactive	t_{CSI}	500		ns
Clock Cycle Time	t_{CYC}	1000		ns
Clock HIGH Time	t_{CLH}	410		ns
Clock LOW Time	t_{CLL}	410		ns
Clock Output Rise Time	t_{OR}		2	µs
Clock Output Fall Time	t_{OF}		2	µs
Input Data Setup Time	t_{ISU}	100		ns
Input Data Hold Time	t_{IHO}	100		ns
Output Data Setup Time	t_{OSU}		500	ns

Abbreviations of the Timing Diagram (cont'd)

Parameter	Symbol	Limit Values		Unit
		min.	**max.**	
Output Data Hold Time	t_{OHO}	0	500	ns
Output Disable Time	t_{OD}		500	ns
Write Cycle Time	t_{WC}		10	ms

Note

The SCK is a strobed clock signal (i.e. it is only active as long as valid data is transferred on SI/SO line) and output data is written on the falling edge and input data is latched on the rising edge. Although the first SCK edge is positive, the PITA drives the first valid bit on SI (output) with the falling edge of $\overline{\text{EPCS}}$, so the minimum setup time with respect to the first SCK rising edge is guaranteed.

5.4.3   Internal Registers for the SPI EEPROM Interface

Internal Register: 00h

Bit 28	EEPROM_Control_Int_En
Type	RW
Default Value	0b
Description	Enable for the EEPROM_Control_Int interrupt bit

Bit 12	EEPROM_Control_Int
Type	RC
Default Value	0b
Description	The EEPROM_Control_Int_En bit and the EEPROM are set to '1' if the transaction is finished.

Internal Register: 24h

Bit 31:0	EEPROM Control Register
Default Value	00000000h

Bit 24	EEPROM_Start
Type	RW
Default Value	0b
Description	Bit 24='1': An EEPROM transaction is started with the EEPROM Command, EEPROM Data and EEPROM Byte Address. BIT 24='0': An EEPROM transaction can be started.

Internal Register: 24h (cont'd)

Bit 23:16	EEPROM Command
Type	RW
Default Value	00h
Description	The following SPI commands are supported: '00000110': WREN Set Write Enable Latch '00000100': WRDI Reset Write Enable Latch '00000101': RDSR Read Status Register '00000001': WRSR Write Status Register '00000011': READ Read Data from Memory Array '00000010': WRITE Write Data to Memory Array 'OTHERS': No action

Bit 15:8	EEPROM Byte Address
Type	RW
Default Value	00h
Description	Byte Address for the next EEPROM read or write transaction.

Bit 7:0	EEPROM Data
Type	RW
Default Value	00h
Description	• Transaction with a read command: After the transaction has been finished this register contains the byte that has been read from the EEPROM. • Transaction with a write command: The contents of this register will be written to the EEPROM Byte Address if the connected EEPROM after the EEPROM_Start bit is set.

6 Power Management

Overview

6.1 Information about the Power Supply Concept

Three different Power Supplies

The PITA-2 has three different power supplies. It may be helpful for the system design to understand the scope of each of these supplies.

- **VIO**
  This supply is internally connected to all signals intended for the PCI bus (pin numbers 8-12, 16-60 and 64).
  VIO can be either 3.3V or 5V and is derived from the VIO supply of the PCI bus. This supply has an effect on the thresholds of the input structure in order to comply with the PCI bus specification. Therefore the PITA-2 can be operated in either 5V or 3.3V signaling environment as specified in the PCI Local Bus Specification Revision 2.2

- **VDD3**
  This supply powers the same pins as listed for VIO. It is used for the output drivers of the PCI bus signals and must be limited to 3.3V at all times (even when VIO is 5V). This supply does not power the internal logic of the PITA-2. It does, however, power the local bus signals (pin numbers 1-7, 65-74, 76-87 and 90-100). If this supply is present the input signals on the local bus signals can be as high as 5V.

- **VAUX**
  This supply also powers the local bus signals (pin numbers 1-7, 65-74, 76-87 and 90-100) as well as the internal logic. This power supply is 3.3V only. If this supply is not present, the PITA-2 can not generate a PME event, the output voltage on any of the above mentioned signals is undefined and the input voltage at any of these pins must not exceed VAUX by more than 0.3V.
  If this supply is present, then the PITA is fully operational and the input signals on the local bus signals can be as high as 5V.

Summary Information

Supply	Voltage	Comment
VIO	3.3V or 5V	For PCI bus only, affects input threshold, almost no current. Should be present at all times.
VDD3	3.3V	For PCI and local bus, decouples internal logic from PCI bus. Should be present at all times except D3cold. If present, the local bus signals can tolerate 5V.
VAUX	3.3V	Supplies internal logic, must be present for 5V tolerance of local (non PCI signals) input signals. Can be switched off when D3cold is not supported.

6.1.1 Information about the Power Management States

Description

The PITA-2 supports the Power Management states D0, D1, D2, D3hot and D3cold.

The PITA-2 can assert the $\overline{PME}$ signal even if the PCI clock (CLK) is not running. Furthermore the PITA-2 has a separate power supply (Vaux) which meets the power constraints (20 mA) for the PCI Vaux supply (disabled slots). Therefore the PITA-2 fully supports the D3cold state.

A separate Application Note describes a power supply circuitry for a D3cold enabled PITA-2.

Please note that bits 8 (PME_En) and 15 (PME_Status) of configuration space register 44h are not affected by a PCI reset. This behavior allows the PCI device driver to determine the PCI device(s) that signalled the PME event.

D0

- The D0 state represents the default state of the internal logic after a system reset.
- After a system reset the PCI interface has to be initialized before being used.
- The PITA-2 responds only to configuration accesses while not completely initialized.
- After initialization the PITA-2 is fully operational.

D1

- D1 is a light sleep state.
- The PITA-2 supports the D1 state by default if this state is not disabled by an EEPROM configuration.
- The PITA-2 PCI function can be set to the D1 state by software.
- The PITA-2 PCI function only responds to PCI configuration accesses.
- All accesses to the memory spaces defined by the Base Address Registers are disabled.
- The only PCI bus operation the PCI interface is allowed to initiate is the assertion of the $\overline{PME}$ signal.
- Transition to D0 by software is possible.

D2

- By default the support of the D2 state is disabled in the PITA-2.
- D2 can be enabled by configuration by an EEPROM.
- Same state behavior as described for the state D1.

D3

- Same state behavior as described for the state D1.
- The only legal state transitions from D3 to D0 are:
  - by software reset; the software has to perform a fully reinitialization of the PCI function including the PCI Configuration Space.
  - by system reset

D3hot

- Power and clock are still available to the PITA-2.
- Power and clock can be returned to D0 by software.
- State behavior as described for the state D3.

D3cold (Standby)

- D3cold is a "power off" state.
- The PCI clock is turned off.
- The PCI bus power V_{cc} has been disconnected.
- As long as the PITA-2 is supplied with power on the Vaux pins it can still assert PME.
- The PITA-2 can assert $\overline{\text{PME}}$ even if the PCI clock is not available.

6.1.2 Considerations about Power Consumption and Reporting

Definitions

First of all it is important to distinguish between a PCI component and a PCI device.

The **PCI component** is the circuitry that is interfacing the PCI bus. As an example the PITA-2 is a PCI bus component.

The **PCI device** is the circuitry designed to perform a specific function (e.g. a modem) including the PCI component.

Therefore for all power consumption calculations or measurements it is important to add up the power requirements of all the circuitry that is active in a given state.

Furthermore it is important to distinguish between PCI slots that are disabled and those that are enabled.

Power Consumption

A **disabled** PCI slot may draw up to 20 mA from power supply VAUX. A PCI device which occupies a disabled slot does not have to support D3cold state. As the PITA-2 draws a maximum of 19 mA it can be left connected to VAUX all the time provided that the external circuitry is switched off (by using the PME_En signal).

An **enabled** PCI slot may consume up to 375 mA when in D3cold state. This leaves enough headroom (356 mA) for external circuitry to trigger the PITA-2 for a PME event.

Reporting

The PCI Bus Power Management Interface Specification specifies two ways that allow the operating system or other software to determine the power consumption of a PCI device:

• Coarse reporting by register 40h:8-6 (Aux_Current)
• Extended reporting by using the data select mechanism

The PITA-2 supports both ways. It is up to the PCI device designer to choose the reporting mechanism and also which values are reported.

Extended reporting overrides coarse reporting.

Coarse Reporting

This mechanism is implemented by the Aux Current field (register 40h). It is only possible to report a single range for the max. current drawn by the PCI device and this range only applied for state D3cold.

Assignments

8	7	6	Max. Current (mA)
1	1	1	375
1	1	0	320
1	0	1	270
1	0	0	220
0	1	1	160
0	1	0	100
0	0	1	55
0	0	0	0 (self powered)

Extended Reporting

This mechanism allows a detailed power consumption reporting. It is possible to report individual power limits for each power state. Furthermore there is no predefined range which may fit more or less but all values can be specified by the PCI designers as needed.

The actual data is retrieved by first selecting a specific item (e.g. D2 Power Consumed) by writing a select code into the Data Select field in register 44h. Then the PITA-2 mirrors the selected values to the Data and the Data Scale field of register 44h. The software can then read these two values. The table below shows the way the Data Scale field should be interpreted for single function PCI devices.

Data Selected — Data Reported

Data Select	Data Reported
0	D0 Power Consumed
1	D1 Power Consumed
2	D2 Power Consumed
3	D3 Power Consumed
4	D0 Power Dissipated
5	D1 Power Dissipated
6	D2 Power Dissipated
7	D3 Power Dissipated

Note

The unit for all values is Watts.

The Data Scale field modifies the value of the Data field as follows:

Data Scale	Modifier
0	Unknown
1	x 0.1
2	x 0.01
3	x 0.001

The actual data can be stored in the external EEPROM. At reset the PITA-2 loads the data into the appropriate registers.

6.1.3 Configuration Space Registers of the Power Management

Configuration Register related to Power Management

There are basically two types of configuration registers related to power management:

• Control Registers
• Data Registers

The control registers (40h and 44h) define the capabilities and the behavior of the PITA-2. As an example bit 26 in register 40h defines whether the PITA-2 supports D2 or not.

The data registers (48h, 4Ch and 50h) reflect the power consumption of the whole PCI device for eight different configurations. A configuration is selected by a value in the data select field of register 44h. The corresponding value is then placed into the data field of register 44h.

The actual values have no effect on the operation or power consumption of the PITA-2. These values are calculated or measured by the PCI device designer and can be stored in the external EEPROM. Please note that the PCI device includes all external circuitry and usually consists not only of the PITA-2.

Register 34h is merely a pointer to the first register of the power management configuration space and hardwired to 40h.

Configuration Space Register: 34h

Bit 31:8	Reserved
Type	H
Value	000000h
Description	Reserved

Bit 7:0	Cap_Ptr
Type	H
Value	40h
Description	The Capabilities Pointer points to the first Power Management Register in the PCI Configuration Space.

Configuration Space Register: 40h

Bit 31:0	Power Management Capabilities (PMC)

Bit 31	PME_Support_D3cold
Type	E
Default Value	0b
Description	0: PME cannot be asserted in state D3cold 1: PME can be asserted in state D3cold

Bit 30	PME_Support_D3hot
Type	E
Default Value	0b
Description	0: PME cannot be asserted in state D3hot 1: PME can be asserted in state D3hot

Bit 29	PME_Support_D2
Type	E
Default Value	0b
Description	0: PME cannot be asserted in state D2 1: PME can be asserted in state D2

Configuration Space Register: 40h (cont'd)

Bit 28	PME_Support_D1
Type	E
Default Value	1b
Description	0: PME cannot be asserted in state D1 1: PME can be asserted in state D1

Bit 27	PME_Support_D0
Type	E
Default Value	0b
Description	0: PME cannot be asserted in state D0 1: PME can be asserted in state D0

Bit 26	D2_Support
Type	E
Default Value	0b
Description	• Not supported from the PITA-2 by default. • Support can be enabled by EEPROM.

Bit 25	D1_Support
Type	E
Default Value	1b
Description	• The PITA-2 supports the D1 Power state by default. • Can be disabled by EEPROM.

Configuration Space Register: 40h (cont'd)

Bit 24:22	Aux Current
Type	E
Default Value	000b
Description	This field can be used to report the VAUX current drawn by the PCI device if the Data Register in register 44h is not used. If the Data Register is used, this field must read 000b. Otherwise the following assignments apply: 001: up to 55mA 010: up to 100mA 011: up to 160 mA 100: up to 220 mA 101: up to 270 mA 110: up to 320 mA 111: up to 375 mA

Bit 21	DSI (Device Specific Initialization)
Type	E
Value	1b
Description	Indicates that the PITA-2 requires a specific initialization sequence following the transition to D0 state (uninitialized).

Bit 20	Reserved
Type	H
Value	0b
Description	Reserved

Configuration Space Register: 40h (cont'd)

Bit 19	PME_Clock
Type	E
Default Value	0b
Description	The PITA-2 can assert PME without a running clock. Whether this bit must be set is therefore dependant on the external circuitry that triggers the PITA-2 for a PME event. 0: no clock required 1: clock required

Bit 18:16	Version
Type	E
Default Value	010b
Description	The value 010b indicates that the device complies with the Revision 1.1 of the PCI Power Management Interface Specification.

Bit 15:8	Next_Item_Ptr
Type	H
Value	00h
Description	No next item

Bit 7:0	Capabiltity_ID
Type	H
Value	01h
Description	Indicates that the data structure is currently pointed to the PCI Power Management data structure.

Configuration Space Register: 44h

Bit 31:24	DATA_Register
Type	H
Value	00h
Description	Depending on the Data_Select field (Bit 12:9) parts of the Power Data register (48h) are mapped to this register.

Bit 23:16	PMCSR_BSE (Bridge support extension)
Type	H
Value	00h
Description	not used

Bit 15	PME_Status
Type	RC
Default Value	none (sticky bit)
Description	This bit is set when the PCI interface asserts the $\overline{PME}$ signal independent of the state of the PME_EN bit.

Bit 14:13	Data_Scale
Type	H
Value	00b
Description	Depending on the Data_Select field (Bit 12:9) parts of the Power_Data register are mapped to this register.

Configuration Space Register: 44h (cont'd)

Bit 12:9	Data_Select
Type	RW
Default Value	0h
Description	• Values from 0 - 7 are supported: Parts of the Power_Data register are mapped to the DATA register and the Data_Scale field. • Values from 8 - 15: Zero values are mapped to the DATA register and the Data_Select field.

Bit 8	PME_En
Type	RW
Default Value	none (sticky bit)
Description	Enables or disables the PITA-2 to assert the $\overline{\text{PME}}$ signal. PME_En='0': Assertion of the $\overline{\text{PME}}$ signal is disabled. PME_En='1': The device is enabled to assert the $\overline{\text{PME}}$ signal.

Bit 7:2	Reserved
Type	H
Value	00h
Description	Reserved

Configuration Space Register: 44h (cont'd)

Bit 1:0	Power_State
Type	RW
Default Value	00b
Description	Power_State='00': D0 state (supported by the PITA-2) Power_State='01': D1 state (supported by the PITA-2) Power_State='10': D2 state (not supported by default) Power_State='11': D3hot state (supported by the PITA-2).

Configuration Space Register: 48h

Bit 31:30	Reserved
Type	H
Value	00b

Bit 29:28	Data Scale for Data Select = 2
Type	E
Default Value	00b
Description	This value is mapped to the Data Scale field of register 44h when Data Select (also in register 44h) is set to 2.

Bit 27:20	Data for Data Select = 2
Type	E
Default Value	00h
Description	This value is mapped to the Data field of register 44h when Data Select (also in register 44h) is set to 2.

Bit 19:18	Data Scale for Data Select = 1
Type	E
Default Value	00b
Description	This value is mapped to the Data Scale field of register 44h when Data Select (also in register 44h) is set to 1.

Configuration Space Register: 48h (cont'd)

Bit 17:10	Data for Data Select = 1
Type	E
Default Value	00h
Description	This value is mapped to the Data field of register 44h when Data Select (also in register 44h) is set to 1.

Bit 9:8	Data Scale for Data Select = 0
Type	E
Default Value	00b
Description	This value is mapped to the Data Scale field of register 44h when Data Select (also in register 44h) is set to 0.

Bit 7:0	Data for Data Select = 0
Type	E
Default Value	00h
Description	This value is mapped to the Data field of register 44h when Data Select (also in register 44h) is set to 0.

Configuration Space Register: 4Ch

Bit 31:30	Reserved
Type	H
Value	00h

Bit 29:28	Data Scale for Data Select = 5
Type	E
Default Value	00b
Description	This value is mapped to the Data Scale field of register 44h when Data Select (also in register 44h) is set to 5.

Bit 27:20	Data for Data Select = 5
Type	E
Default Value	00h
Description	This value is mapped to the Data field of register 40h when Data Select (also in register 44h) is set to 5.

Bit 19:18	Data Scale for Data Select = 4
Type	E
Default Value	00b
Description	This value is mapped to the Data Scale field of register 44h when Data Select (also in register 44h) is set to 4.

Configuration Space Register: 4Ch (cont'd)

Bit 17:10	Data for Data Select = 4
Type	E
Default Value	00h
Description	This value is mapped to the Data field of register 44h when Data Select (also in register 44h) is set to 4.

Bit 9:8	Data Scale for Data Select = 3
Type	E
Default Value	00b
Description	This value is mapped to the Data Scale field of register 44h when Data Select (also in register 44h) is set to 3.

Bit 7:0	Data for Data Select = 3
Type	E
Default Value	00h
Description	This value is mapped to the Data field of register 44h when Data Select (also in register 44h) is set to 3.

Configuration Space Register: 50h

Bit 31:20	Reserved
Type	H
Value	00b

Bit 19:18	Data Scale for Data Select = 7
Type	E
Default Value	00b
Description	This value is mapped to the Data Scale field of register 44h when Data Select (also in register 44h) is set to 7.

Bit 17:10	Data for Data Select = 7
Type	E
Default Value	00h
Description	This value is mapped to the Data field of register 44h when Data Select (also in register 44h) is set to 7.

Bit 9:8	Data Scale for Data Select = 6
Type	E
Default Value	00b
Description	This value is mapped to the Data Scale field of register 44h when Data Select (also in register 44h) is set to 6.

Configuration Space Register: 50h (cont'd)

Bit 7:0	Data for Data Select = 6
Type	E
Default Value	00h
Description	This value is mapped to the Data field of register 44h when Data Select (also in register 44h) is set to 6.

6.1.4 Electrical Characteristics

Vaux Power Supply in different Power Management Modes

State	Typ	Max
D0		19 mA
D1		19 mA
D2		19 mA
D3hot		19 mA
D3cold		19 mA

Description of the Table

The table above shows the current drawn by the V_{aux} power supply in different power management modes. The PITA-2 meets the 20mA limit defined for D3cold disabled PCI slots.

6.1.5   Design Hints

D3cold

For a design that supports D3cold it is important to check all signals on the local bus side of the PITA-2 that may be affected by a missing Vdd3.

As during D3cold Vdd3 will drop to zero all pins that are strapped to Vdd3 either directly or by a pullup will also drop to zero.

Therefore it is strongly recommended to strap pins on the local bus side of the PITA-2 to Vaux instead.

This is especially important for the test pin (pin 1) of the PITA-2. If this pin is not kept at a high level during D3cold the PITA-2 will not be able to reliably assert PME#.

Pins that can cause an interrupt ($\overline{\text{INT0}}$ and GP0-GP3) should also be checked to avoid unwanted PME# events.

6.1.6 Compatibility Issues

Supported Designs by PITA

The PITA-2 supports designs which are compliant to the **PCI Local Bus Specification Revision 2.2** and the **PCI Bus Power Management Interface Specification Revision 1.1**.

Potential Compatibility Problem

The only potential compatibility problem arises if the PITA-2 is used in a design which:

- uses the $\overline{\text{PME}}$ signal
- does not support D3cold

In this case it may be tempting to connect the Vaux power supply of the PITA-2 directly to the 3.3V signal of the PCI connector and likewise directly connect the $\overline{\text{PME}}$ signal of the PITA-2 to the PME# signal of the PCI connector.

However, such a design may affect a PCI system, which:

- supports Vaux
- has at least one device with D3cold support connected

Under these circumstances the following unwanted behavior may happen:

The PCI system enters D3cold and the PCI bus enters state B3. In this state the supply power 3.3V is disabled while Vaux remains active. As the PITA-2 is connected to the 3.3V supply its own supply Vaux will also float. The $\overline{\text{PME}}$ signal of the PITA-2 has an internal clamp diode which will limit the voltage on $\overline{\text{PME}}$ to about Vaux+0.7V.

Therefore it is likely that the PITA-2 will pull down the PME# signal and therefore block all other D3cold compliant devices on the bus.

This behavior can be easily avoided by implementing Vaux detection and power switching as the PITA-2 meets the power supply requirements for PCI slots that do not support D3cold but have Vaux power supply.

If the PCI device cannot generate a PME event at all it is best to leave the PME# signal of the PCI connector not connected.

7 Reset and Interrupts

7.1 Reset

Introduction

After each power up the PITA-2 must be reset. This reset is necessary to establish a well defined state for all subsequent actions. This chapter informs about:

- reset phases
- external signals affected by reset
- internal registers affected by reset
- pinstrapping
- automatic reconfiguration

Reset Phases

The PITA-2 can be only reset by pulling the $\overline{\text{RST}}$ signal low and then high while the PITA-2 is powered up. There is no provision for a power on reset. Furthermore the PITA-2 requires seven clock cycles after the rising edge of the $\overline{\text{RST}}$ signal.

After the rising edge the PITA-2 may start the automatic reconfiguration. During this process it copies the contents of an external EEPROM into selected fields of the configuration space registers. Automatic reconfiguration is entered when signal ELD is strapped to H. Otherwise the PITA-2 will skip this phase.

External Signals

All PCI signals are floated as long as the $\overline{RST}$ signal is low.

Significant input signals (GPIO0-GPIO3, PA0-PA7, PAD0-PAD7 and ELD) must remain stable at least six clock cycles after the rising edge of the $\overline{RST}$ signal.

The signal PRST is forced to low (inactive state) at the rising edge of $\overline{RST}$.

The signal $\overline{SRST}$ is forced to high (inactive state) at the rising edge of $\overline{RST}$.

Usually both signals have not been active before the $\overline{RST}$ signal has been asserted. Therefore no signal change will usually happen at both $\overline{SRST}$ and PSRT. As a consequence components which are connected to one of these signals are not automatically reset by a PCI reset. This behavior is desirable when these components remain active during D3cold because after a wake up the SW driver can obtain valuable information from these devices about the reason for a wake up.

On the other hand, for a complete initialization of the PCI device the SW driver must perform a reset for these devices by specifically programming the internal registers of the PITA-2.

Internal Registers

All internal register fields that are affected by an external reset are marked by a default value in the register description. This default value may be overridden by the optional automatic reconfiguration process.

After an external reset the PITA-2 allows only configuration space accesses. Furthermore the PITA-2 will abort configuration space accesses until it has completed the reset sequence (including the optional automatic reconfiguration process). Therefore the SW driver will not be able to read any incorrect transient value from any configuration space register.

For the power management the following bits are not affected by an external reset (sticky bits):

* configuration space 44h:8
* configuration space 44h:15
* internal register 18h:24-27

The reason for this behavior is that the PITA-2 supports the D3cold state and thus must be able to assert a $\overline{PME}$ signal even while $\overline{RST}$ is low.

Pinstrapping

Pinstrapping is used for:

• Loading the Subsystem Vendor ID.
• Loading the least significant 4 bits of the Subsystem ID to the PCI Configuration Space.

Several output pins from the parallel micro controller interface and the general purpose I/O interface are implemented as tristate output pins.

During PCI reset they are driven in tristate mode and the external logic value is latched in the Subsystem ID (4 LSBs) and the Subsystem Vendor ID. This means that the signals on board, connected to these pins, must be forced with pullup/pulldown resistors to the desired value if they are not driven by the PITA-2.

Signal Name	Usage during PCI Reset (pinstrapping)
PAD(7:0)	Subsystem Vendor ID(15:8)
PA(7:0)	Subsystem Vendor ID(7:0)
GP3	Subsystem ID(3)
GP2	Subsystem ID(2)
GP1	Subsystem ID(1)
GP0	Subsystem ID(0)

Automatic reconfiguration of the PITA-2 with the serial EEPROM

The PITA-2 can also be configured by the EEPROM after system reset. Pinstrap values are overwritten by this process if the procedure described in "Automatic reconfiguration of the PITA" on page 116 was successful.

The PITA-2 will abort PCI configuration accesses during automatic reconfiguration.

7.2 Interrupts

Introduction

The PITA-2 can generate an interrupt on the PCI signal $\overline{\text{INTA}}$

- external, asynchronous event (e.g. an incoming call)
- internal, synchronous event (e.g. an EEPROM access finished))

General Notes

The PITA-2 can only assert $\overline{\text{INTA}}$ if the following requirements are met:

- PITA-2 is in D0 or D1 state
- the interrupt source is enabled by setting the corresponding interrupt enable bit in internal register 00h (ICR).
- the event has occurred

Once $\overline{\text{INTA}}$ has been asserted by the PITA-2 it will stay active until a write transaction to the internal register ICR occurs. After this write transaction has occurred the PITA-2 deasserts the signal $\overline{\text{INTA}}$.

The PITA-2 will immediately after this write transaction assert $\overline{\text{INTA}}$ again if either of the following conditions holds:

- not all interrupt reporting bits have been cleared
- the requirements for asserting an interrupt still hold

The former condition usually arises when more than one source has been activated and the interrupt handler reacts to the events sequentially.

The latter condition usually arises if an external event has occurred a second time while the interrupt handler is still processing the first occurrence of this event.

Reporting bits within the internal register ICR can only be cleared by writing a logical 1 at the bits that shall be cleared. A read access to this register does not clear any bit nor does it affect any signal.

External Events

For external events either the dedicated $\overline{\text{INT0}}$ pin or one of the General Purpose IO pins (GP0-GP3) can be used. The following table shows how to program the PITA-2 in order to activate one or more of these pins for interrupts.

Programming of the PITA-2

Source	Enabled by	Reported by	Active Level
$\overline{\text{INT0}}$	00h:INT0_EN=1 00h:INT0_POL=1	00h:INT0=1	H
$\overline{\text{INT0}}$	00h:INT0_EN=1 00h:INT0_POL=0	00h:INT0=1	L
GP0	00h:GP0_INT=1 18h:GP0_INT_EN= 1 18h:GP0_OUT_EN = 0	00h:GP0_INT=1	L
GP1	00h:GP1_INT=1 18h:GP1_INT_EN= 1 18h:GP1_OUT_EN = 0	00h:GP1_INT=1	L
GP2	00h:GP2_INT=1 18h:GP2_INT_EN= 1 18h:GP2_OUT_EN = 0	00h:GP2_INT=1	L
GP3	00h:GP3_INT=1 18h:GP3_INT_EN= 1 18h:GP3_OUT_EN = 0	00h:GP3_INT=1	L

Internal Events

The following internal events can trigger an interrupt when enabled:

- an EEPROM command has finished
- the programmed number of writes to the DMA buffer has occurred
- FIFO overflow (receive failure)
- FIFO underflow (transmit failure)
- the PCI retry counter has expired (too many retries for a single transfer)

Summation of the used Bits in Register ICR

Event	Enabled by	Reported by
EEPROM command finished	00h:28=1	00h:12=1
DMA watermark reached	00h:24=1	00h:8=1
FIFO overflow	00h:25=0	00h:9=1
FIFO underflow	00h:26=1	00h:10=1
PCI retries expired	00h:27=1	00h:11=1

EEPROM Command finished & DMA Watermark reached

The EEPROM command finished and the DMA watermark reached interrupts are normal events.

FIFO Overflow & FIFO Underflow

The FIFO overflow and FIFO underflow events indicate a fatal error which may result in a communication failure. The actual impact of these events depends on the error detection and error correction capabilities of the communication protocol of the application.

PCI Retries expired

The PCI retries expired event is not a normal event but is not necessarily a fatal event. If the PITA-2 reports this event the following has happened:

- The DMA controller has requested a data word transfer to/from the FIFO.
- The PITA-2 has requested the PCI bus for the transfer.
- The PITA-2 has been granted the PCI bus.
- The PITA-2 has initiated the transfer <n> times but the PCI target has aborted the transfer each time. <n> is the number programmed in internal register 1Ch:23:16.

At this point the PITA-2 releases the PCI bus and reports the event. However, as the DMA data transfer request is not satisfied the PITA-2 will request the PCI bus again for the same data transfer until the request is satisfied. Depending on the PCI target this may either have no effect (data delivered in time finally) or a fatal event may happen (FIFO overflow/underflow).

Caution

It is important to bear in mind that in D3cold state Vdd3 will vanish. For devices that support D3cold it is therefore strongly recommended to strap low active interrupt sources (e.g. GP0-GP3) not to Vdd3 but to Vaux instead.

8 Pinning

PITA-2 Pinout

This illustration shows the numbered pins and their respective signals:

PITA-2
T-QFP-100-10
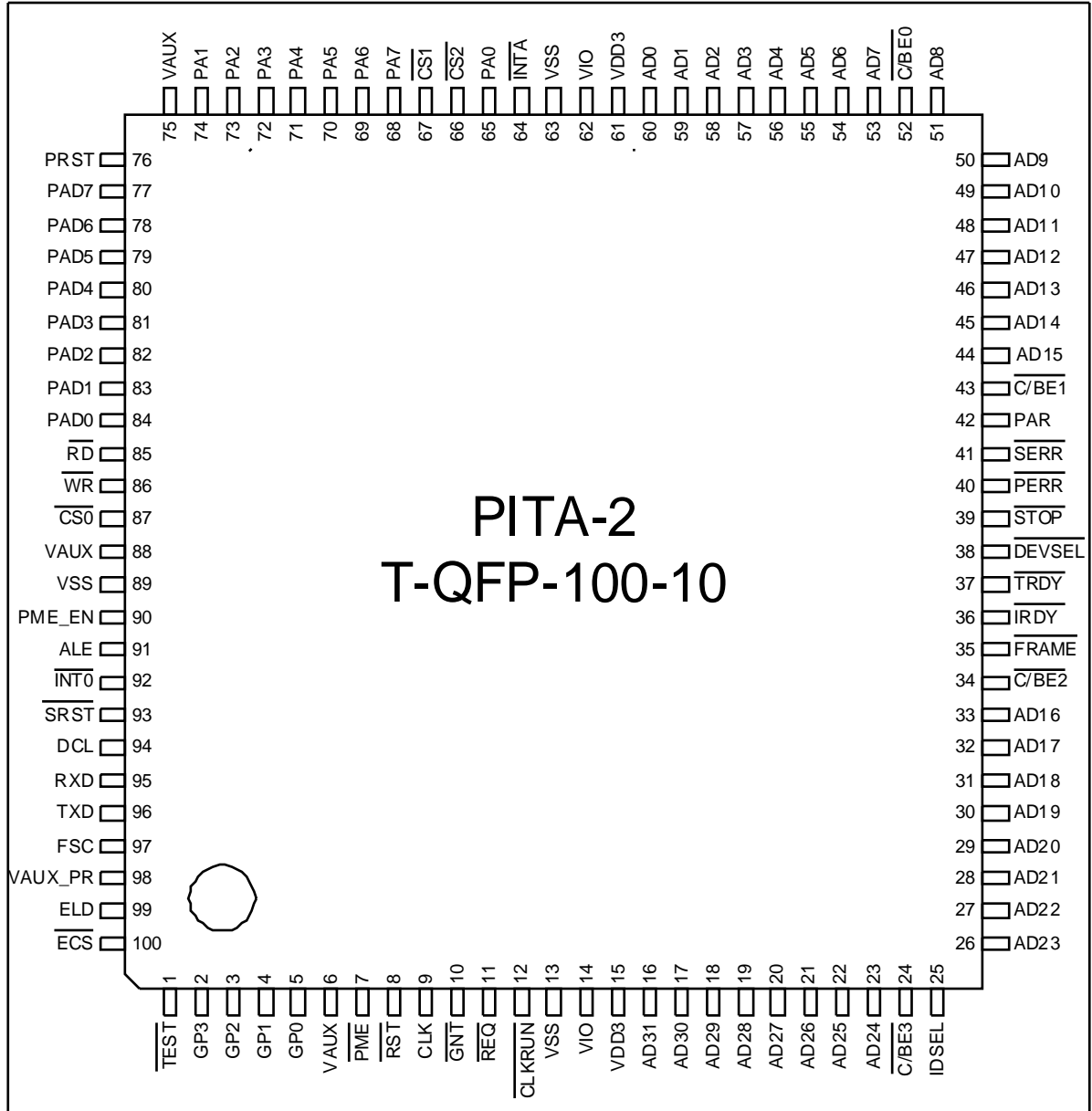
Overview

The following table lists the interfaces and their respective pins:

Interface	Total	In	Out	I/O	Page
PCI bus	52	4	5	43	158
Parallel Interface	23	3	14	8	159
Serial Interface	5	2	2	1	161
GP I/O Interface	4	0	0	4	162
Special EEPROM Signals	2	1	1	0	163
Power Management	2	1	1		

Description of PIN Types

Type	Description
O/PS	Output Pin/Pin Strap Pin
I	Input Pin
IO	Bidirectional Input/Output Pin
OD	Open Drain

This table lists the Pins Characteristics of the PCI Bus

Pin No.	Signal Name	Pin Count	Type	Function
9	CLK	1	I	PCI - Clock (max. 33 MHz)
8	$\overline{\text{RST}}$	1	I	PCI - Reset
16 - 23, 26 - 33, 44 - 51, 53 - 60	AD(31:0)	32	IO	PCI - Address-/Data bus
24, 34, 43, 52	$\overline{\text{C/BE}}$(3:0)	4	IO	PCI - Command/Byte Enable Bus (Byte Enables are low active)
42	PAR	1	IO	PCI - Parity
64	$\overline{\text{INTA}}$	1	OD	PCI - Interrupt Signal
25	IDSEL	1	I	PCI - Initialization Device Select Signal For CardBus boards this signal must set to '1'
35	$\overline{\text{FRAME}}$	1	IO	PCI - Frame
36	$\overline{\text{IRDY}}$	1	IO	PCI - Initiator Ready
37	$\overline{\text{TRDY}}$	1	IO	PCI -Target Ready
38	$\overline{\text{DEVSEL}}$	1	IO	PCI - Device Select
39	$\overline{\text{STOP}}$	1	IO	PCI - Stop
11	$\overline{\text{REQ}}$	1	OTS	PCI - Bus Request
10	$\overline{\text{GNT}}$	1	I	PCI - Bus Grant

This table lists the Pins Characteristics of the PCI Bus (cont'd)

Pin No.	Signal Name	Pin Count	Type	Function
40	$\overline{\text{PERR}}$	1	IO	PCI - Parity Error
41	$\overline{\text{SERR}}$	1	OD	PCI - System Error
7	$\overline{\text{PME}}$	1	OD	PCI - Power Management Event
12	$\overline{\text{CLKRUN}}$	1	I	Clock Run

This table lists the Pins Characteristics of the Parallel Interfaces

Pin No.	Signal Name	Pin Count	Type	Function
76	PRST	1	O	Active high reset
66, 67, 87	$\overline{\text{CS}}$(2:0)	3	O	Chip Select Signals for three devices connected to the parallel micro controller interface.
84 - 77	PAD(7:0)	8	IO	- Multiplexed Bus Mode: Address/Data bus for the parallel interface. - Non-Multiplexed Bus Mode: Data bus for the parallel interface.

This table lists the Pins Characteristics of the Parallel Interfaces (cont'd)

Pin No.	Signal Name	Pin Count	Type	Function
74 - 68, 65	PA(7:0)	8	O/PS	- Multiplexed Bus Mode: Not used; pins can be left not connected. - Non-Multiplexed Bus Mode: Address bus for the parallel interface.
91	ALE	1	O	Address Latch Enable Signal, active high. In non-multiplexed mode the ALE input of peripheral devices must be connected to VSS.
86	$\overline{\text{WR}}$	1	O	Write Signal, active low
85	$\overline{\text{RD}}$	1	O	Read Signal, active low
92	$\overline{\text{INT0}}$	1	I	Standard active low interrupt input for connected devices, which is forwarded to the PCI interface ($\overline{\text{INTA}}$).

This table list the Pins Characteristics of the Serial Interface

Pin No.	Signal Name	Pin Count	Type	Function
93	$\overline{\text{SRST}}$	1	O	Active low reset output.
97	FSC	1	I	Frame Synchronization Clock signal, 8 kHz.
94	DCL	1	I O (OD)	Serial Data Clock Signal. The direction of this pin can be controlled by the DCL_Out_En bit in the internal registers. By default this pin is input. For PSB4596 V2.1 mode, this pin must configured as output (open drain), for all other modes this pin must be input.
95	RXD	1	I	Serial Data Input Signal
96	TXD	1	O (OD)	Serial Data Output Signal

This table lists the Pins Characteristics of the General Purpose I/O Interface

Pin No.	Signal Name	Pin Count	Type	Function
2	GP3	1	IO	General Purpose I/O Pin 3 This pin is driven high during the automatic EEPROM configuration if ELD = '1'.
3	GP2	1	IO	General Purpose I/O Pin 2 Serial EEPROM Interface: SCK - Serial Clock Signal.
4	GP1	1	IO	General Purpose I/O Pin 1 Serial EEPROM Interface: SO - Serial Data Output from EEPROM (input to the PITA-2).
5	GP0	1	IO	General Purpose I/O Pin 0 Serial EEPROM Interface: SI - Serial Data Input to the EEPROM (output from the PITA-2).

This table lists the Pins Characteristics of the Special EEPROM Signals

Pin No.	Signal Name	Pin Count	Type	Function
99	ELD	1	I	EEPROM Load '1' -> EEPROM Configuration is enabled. '0' -> EEPROM Configuration is disabled.
100	$\overline{ECS}$	1	O	EEPROM Chip Select (SPI Signal)

This table lists the Pins Characteristics of the Power Management

Pin No.	Signal Name	Pin Count	Type	Function
90	PME_EN	1	O	Reflects the state of the PME_EN bit. Can be used to power down all external logic that is not needed in state D3.
98	VAUX_PR	1	I	Indicates that Vaux is present.

This table lists the Pins Characteristics of the Power Supply

Pin No.	Signal Name	Pin Count	Type	Function
15, 61	VDD3	5	I	Positive Power Supply 3.3V ± 10%
6, 75, 88	Vaux	3	I	Positive Power Supply 3.3V ± 10%
14, 62	VIO	2	I	IO Voltage Supply (either 3.3V or 5V)
13, 63, 89	VSS	3	I	Ground 0V

9   Electrical Characteristics

Overview:

Overview	Page
Absolute Maximum Ratings	167
DC Characteristics	168

Pin Groups

The PITA-2 has two different kind of pins:

- **PCI Pins** (8-12, 16-60 and 64)
  These pins are powered by VDD3 and VIO and are intended for connection to the PCI bus.

- **Local Pins** (1-5, 7, 65-74, 76-87 and 90-100)
  These pins are powered by VAUX or VDD3 (one power supply is sufficient) and are intended for connection to the local signal of the PCI device.

The AC and DC specification for these two groups are may be different and are therefore listed in separate tables for each group.

9.1   Absolute Maximum Ratings

This Table shows the Parameters for the Absolute Maximum Ratings

Parameter		Limit Values	Unit
Voltage on PCI pins with respect to ground	V_{S1}	-0.5 to $V_{IO} + 0.5$	V
Voltage on local pins with respect to ground	V_{S2}	-0.3 to 5.5	V
Ambient temperature under bias	T_A	0 to 70	°C
Storage temperature	T_{stg}	-65 to 150	°C
Maximum voltage on VIO	V_{DD}	7	V
Maximum voltage on VDD3 and VAUX	V_{DD}	4.6	V

Note:

Stresses above those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device.

Exposure to conditions beyond those indicated in the recommended operational conditions of this specification may affect device reliability.

This is a stress rating only and functional operation of the device under these conditions or at any other condition beyond those indicated in the operational conditions of this specification is not implied.

9.2   DC Characteristics

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Description

The DC characteristics of the PITA-2 are given in three separate tables:

• PCI pins, 5V signaling environment (VIO = 5V)
• PCI pins, 3.3V signaling environment (VIO = 3.3V)
• Local pins

___

Conditions

5V Signaling Environment

T_A = 0 to 70 °C; V_{IO} = 4.75V to 5.25V, V_{aux} and V_{DD3} = 3.0V to 3.6V, V_{SS} = 0 V

3.3V Signaling Environment

T_A = 0 to 70 °C; V_{IO}, V_{aux} and V_{DD3} = 3.0V to 3.6V, V_{SS} = 0 V

___

DC Characteristics PCI Pins (5V Signaling Environment)

Parameter	Sym	Limit Values		Unit	Test Condition	Rem.
		min	**max**			
Input High Voltage	V_{IH}	2.0	V_{IO}+ 0.5	V		
Input Low Voltage	V_{IL}	−0.5	0.8	V		
Input High Leakage Current	I_{IH}		70	uA	Vin = 2.7V	1)
Input Low Leakage Current	I_{IL}		-70	uA	Vin = 0.5V	2)
Output High Voltage	V_{OH}	2.4		V	I_{OH} = −2mA	
L-output voltage	V_{OL}		0.55	V	I_{OL} = 3/6 mA	3)
Input Pin Capacitance	C_{IN}		10	if		
Pin Inductance	L_{PIN}		20	nH		
PME# Input Leakage	I_{OFF}		1	uA	Vout below 5.25V VDD3 off/floating	

1) except for $\overline{\text{CLKRUN}}$ which is internally pulled down (I_{LIh} = 500 uA
2) except for $\overline{\text{CLKRUN}}$ which is internally pulled down (I_{LIh} = 500 uA
3) 6mA for $\overline{\text{FRAME}}$, $\overline{\text{TRDY}}$, $\overline{\text{IRDY}}$, $\overline{\text{DEVSEL}}$, $\overline{\text{STOP}}$, $\overline{\text{SERR}}$, $\overline{\text{PERR}}$, $\overline{\text{LOCK}}$ and $\overline{\text{INTA}}$

DC Characteristics PCI Pins (3.3V Signaling Environment)

Parameter	Sym	Limit Values		Unit	Test Condition	Rem.
		min	max			
Input High Voltage	V_{IH}	$0.5V_{IO}$	$V_{IO}+0.5$	V		
Input Low Voltage	V_{IL}	-0.5	$0.3V_{IO}$	V		
Input Leakage Current	I_{IL}	-10	10	uA	$0 < Vin < V_{IO}$	1)
Output High Voltage	V_{OH}	$0.9V_{IO}$		V	$I_{OH} = -0.5$ mA	
L-output voltage	V_{OL}		$0.1V_{IO}$	V	$I_{OL} = 1.5mA$	
Input Pin Capacitance	C_{IN}		10	pF		
Pin Inductance	L_{PIN}		20	nH		
PME# Input Leakage	I_{OFF}		1	uA	Vout below 3.6V VDD3 off/ floating	

1) except for $\overline{CLKRUN}$ which is internally pulled down (I_{Llh} = 500 uA

DC Characteristics Local Pins

Parameter	Sym	Limit Values		Unit	Test Condition	Rem.
		min	max			
Input High Voltage	V_{IH}	2.4	5.25	V		
Input Low Voltage	V_{IL}	−0.3	0.8	V		
Input Leakage Current	I_{IL}	-10	10	uA		
Output High Voltage	V_{OH}	2.4		V	$I_{OH} = -2\,mA$	
L-output voltage	V_{OL}		0.4	V	$I_{OL} = 2\,mA$	

10 Package Outlines

1) Does not include plastic or metal protrusion of 0.25 max. per side

11 Configuration Space Register of the PITA-2

Overview

11.1 Description of the Register Types

Description of the Register Types

Type	Description
PE	• read only via PCI • these bits are initialized by pinstrapping during PCI reset or by the optional EEPROM
H	• read only via PCI • hardwired
RC	• read clear via PCI • these bits are set by the internal logic • these bits can be read out and reset by writing logical "1" to them • writing logical "0" doesn't influence the states of these bits
RW	• read write via PCI • these bits can be read out and written via the PCI bus
E	• read only via PCI • these bits are initialized to a default value during PCI reset or by the optional EEPROM

11.2 Configuration Space Registers

00h

Ad.	Bit	Type	Default Value	Register Name	Page
00h	31:16	E	2104h	Device ID	185
	15:0	E	110Ah	Vendor ID of Siemens AG.	185

04h

Ad.	Bit	Type	Default Value	Register Name	Page
04h	31:0		0290 0000h	PCI Status Register	185
	31	RC	0b	Parity Error Detected	185
	30	RC	0b	System Error Signaled	90
	29	RC	0b	Master Abort Detected	90
	28	RC	0b	Target Abort Detected	90
	27	RC	0b	Target Abort Signaled	90
	26:25	H	01b	DEVSEL Timing	26 28
	24	RC	0b	Data Parity Error Reported	185
	23	H	1b	Fast Back-to-Back Capability	30
	22	H	0b	User Defined Functions	185
	21	H	0b	66 MHz Capability	185

04h (cont'd)

Ad.	Bit	Type	Default Value	Register Name	Page
	20	E	1b	Capabilities	185
	19:16	H	0000b	Reserved	185
	15:0			Command Register	185
	15:10	H	000000b	Reserved	185
	9	H	0b	Fast Back-to-Back Enable	30
	8	RW	0b	System Error Enable	90
	7	H	0b	Address/Data Stepping Enable (not used)	185
	6	RW	0b	Parity Error Response	185
	5:3	H	000b	The PITA-2 does not support the Special Cycle Command.	185
	2	RW	0b	Master Enable	90
	1	RW	0b	Memory Access Enable	17
	0	H	0b	I/O Access Enable	185

08h

Ad.	Bit	Type	Default Value	Register Name	Page
08h	31:8	E	028000h	Class Code/PCI network device	188
	7:0	E	02h	Revision ID	188

0Ch

A d.	Bit	Type	Default Value	Register Name	Page
0Ch	31:24	H	00h	BIST	189
	23:16	H	00h	Header Type	189
	15:8	H	00h	Master Latency Timer	189
	7:0	H	00h	Cache Line Size	189

10h

A d.	Bit	Type	Default Value	Register Name	Page
10h	31:0 31:12 11:0	 RW H	00000000h	Base Register 0	17

14h

A d.	Bit	Type	Default Value	Register Name	Page
14h	31:0 31:12 11:0	 RW H	00000000h	Base Register 1	18

18h

Ad.	Bit	Type	Default Value	Register Name	Page
18h	31:0	H	00000000h	Base Address Register 2 (not used)	18

1Ch

Ad.	Bit	Type	Default Value	Register Name	Page
1Ch	31:0	H	00000000h	Base Address Register 3 (not used)	18

20h

Ad.	Bit	Type	Default Value	Register Name	Page
20h	31:0	H	00000000h	Base Address Register 4 (not used)	19

24h

Ad.	Bit	Type	Default Value	Register Name	Page
24h	31:0	H	00000000h	Base Address Register 5 (not used)	19

28h

Ad.	Bit	Type	Default Value	Register Name	Page
28h	31:0		0000 02C0	CardBus CIS Pointer	20
	31:28	H	0000b	ROM Image Number	20
	27:3	H	000054h	Address Space Offset	20
	2:0	H	000b	Address Space Indicator	21

2Ch

Ad.	Bit	Type	Default Value	Register Name	Page
2Ch	31:20	E	000h	Subsystem ID	21
	19:16	PE	pinstrap value or EEPROM-value		
	15:0	PE	pinstrap value or EEPROM-value	Subsystem Vendor ID	21

30h

Ad.	Bit	Type	Default Value	Register Name	Page
30h	31:0	H	00000000h	Reserved	190

34h

Ad.	Bit	Type	Default Value	Register Name	Page
34h	31:8	H	00h	Reserved	132
	7:0	H	40h	Capabilities Pointer	132

38h

Ad.	Bit	Type	Default Value	Register Name	Page
38h	31:0	H	00000000h	Reserved	190

3Ch

Ad.	Bit	Type	Default Value	Register Name	Page
3Ch	31:24	E	00h	Max_Lat	191
	23:16	E	00h	Min_Gnt	191
	15:8	H	01h	Interrupt pin	191

3Ch (cont'd)

Ad.	Bit	Type	Default Value	Register Name	Page
	7:0	RW	FFh	Interrupt Line	191

40h

Ad.	Bit	Type	Default Value	Register Name	Page
40h	31:0		1222 0001	Power Management Capabilities (PMC)	133
	31:30	E	00b	PME_Support	133
	29:28	E	01b		
	27	E	0b		
	26	E	0b	D2_Support	133
	25	E	1b	D1_Support	133
	24:22	E	000b	Aux Current	133
	21	E	1b	DSI	133
	20	H	0b	Reserved	133
	19	E	0b	PME Clock	133
	18:16	E	010b	Version The value 010b indicates that the device complies with the Revision 1.1 of the PCI Power Management Interface Specification.	133
	15:8	H	00h	Next Item Ptr	133
	7:0	H	01h	Capability ID	133

44h

Ad.	Bit	Type	Default Value	Register Name	Page
44h	31:24	H	00h	DATA Register	137
	23:16	H	00h	PMCSR_BSE Bridge Support Extensions	137
	15	RC	0b	PME Status	137
	14:13	H	00b	Data Scale	137
	12:9	RW	0h	Data Select	137
	8	RW	0b	PME_En	137
	7:2	H	00h	Reserved	137
	1:0	RW	00b	Power State	137

48h

Ad.	Bit	Type	Default Value	Register Name1	Page
48h	31:0			Power Data Register 1	140
	31:30	H	00b	Reserved	140
	29:28	H/EW	00b	Data_Scale in Data_Select = 2	140
	27:20	H/EW	00h	DATA in Data_Select = 2	140
	19:18	H/EW	00b	Data_Scale in Data_Select = 1	140
	17:10	H/EW	00h	DATA in Data_Select = 1	140

48h (cont'd)

Ad.	Bit	Type	Default Value	Register Name1	Page
	9:8	H/EW	00b	Data_Scale in Data_Select = 0	140
	7:0	H/EW	00h	DATA in Data_Select = 0	140

4Ch

Ad.	Bit	Type	Default Value	Register Name	Page
4Ch	31:0			Power Data Register 2	142
	31:30	H	00b	Reserved	142
	29:28	E	00b	Data_Scale in Data_Select = 5	142
	27:20	E	00h	DATA in Data_Select = 5	142
	19:18	E	00b	Data_Scale in Data_Select = 4	142
	17:10	E	00h	DATA in Data_Select = 4	142
	9:8	E	00b	Data_Scale in Data_Select = 3	142
	7:0	E	00h	DATA in Data_Select = 3	142

50h

Ad.	Bit	Type	Default Value	Register Name	Page
50h	31:0			Power Data Register 3	144
	31:20	H	000h	Reserved	144
	19:18	E	00b	Data_Scale in Data_Select = 7	144
	17:10	E	00h	Data_Value in Data_Select = 7	144
	9:8	E	00b	Data_Scale in Data_Select = 6	144
	7:0	E	00h	Data_Value in Data_Select = 6	144

54h

Ad.	Bit	Type	Default Value	Register Name	Page
54h	31:0	H	00h	CardBus CIS	192

11.3 Registers which do not occur elsewhere in the Data Sheet

00h

Bit 31:16	Device ID
Type	E
Default Value	2104h
Description	Identifies the PITA-2 within all PCI devices from Siemens Semiconductors.

Bit 15:0	Vendor ID
Type	E
Default Value	110Ah
Description	110A is the Vendor ID of Siemens AG.

04h

Bit 31:0	PCI Status Register
Default Value	02900000h

Bit 31	Parity_Error_Detected
Type	RC
Default Value	0b
Description	This bit is set, if a parity error is detected during a transaction with the PITA-2. This is done independently from the status of the 'Parity Error Response' bit.

04h (cont'd)

Bit 24	Data_Parity_Error_Reported
Type	RC
Default Value	0b
Description	The PCI Master asserts this bit if it detects the $\overline{PERR}$ signal on the PCI bus asserted during a PCI transaction initiated by itself.

Bit 22	User_Defined_Functions
Type	H
Value	0b
Description	The PITA-2 has no user defined functions.

Bit 21	66_MHz_Capability
Type	H
Value	0b
Description	The PITA-2 is not a 66 MHz device (0 - 33 MHz supported.)

Bit 20	Capabilities
Type	E
Default Value	1b
Description	If this bit is set, the PCI device has additional capabilities defined in the PCI Configuration Space Header. Additional capabilities can be found in the Cap_Ptr under address 34h.

04h (cont'd)

Bit 19:16	Reserved
Type	H
Default Value	0000b
Description	

Bit 15:0	Command Register

Bit 15:10	Reserved
Type	H
Default Value	000000b
Description	

Bit 7	Address/Data_Stepping_Enable
Type	H
Default Value	0b
Description	not used

Bit 6	Parity_Error_Response
Type	RW
Default Value	0b
Description	If this bit is set to '1', the PCI interface reports data parity errors by asserting the $\overline{\text{PERR}}$ signal.

04h (cont'd)

Bit 5:3	
Type	H
Value	000b
Description	The PITA-2 does not support the Special Cycle Command. The PITA-2 does not generate Memory Write and invalidate transactions. The PITA-2 does not support VGA Palette snooping.

Bit 0	I/O_Access_Enable
Type	H
Default Value	0b
Description	The PCI interface does not support I/O commands.

08h

Bit 31:8	Class_Code
Type	H or EW
Default Value	028 000h
Description	PCI network device

Bit 7:0	Revision ID
Type	H
Default Value	02h
Description	Revision of the PCI device

0Ch

Bit 31:24	BIST
Type	H
Default Value	00h
Description	The PITA-2 has no built-in self test.

Bit 23:16	Header_Type
Type	H
Default Value	00h
Description	

Bit 15:8	Master_Latency_Timer
Type	H
Default Value	00h
Description	Unused

Bit 7:0	Cache_Line_Size
Type	H
Default Value	00h
Description	The PITA-2 does not support the cache line size register because it supports only single data transactions.

30h

Bit 31:0	Reserved
Type	H
Default Value	0000 0000h
Description	Reserved

38h

Bit 31:0	Reserved
Type	H
Default Value	0000 0000h
Description	

3Ch

Bit 31:24	Max_Lat
Type	E
Default Value	00h
Description	Set to '0' because only single data transactions are supported.
Bit 23:16	Mint_Gnt
Type	E
Default Value	00h
Description	Set to '0' because only single data transactions are supported.

Bit 15:8	Interrupt_Pin
Type	H
Default Value	01h
Description	As a single function device, the PITA-2 uses the INTA signal.

Bit 7:0	Interrupt_Line
Type	RW
Default Value	FFh
Description	These Bits show the interrupt line which is used by this system. For a x86 system the value FF means unknown. These registers are written during the initialization of the operating system.

54h

Bit 31:0	Cardbus_CIS
Type	H
Value	00h
Description	Not supported by PITA-2

12   Internal Register of the PITA

Overview

	Page
Description of the Register Types	194
Internal Register	195
Registers which do not occur elsewhere in the Data Sheet	202

12.1 Description of the Register Types

Description of the Register Types

Type	Description
R	**read only**
RC	**read clear** • these bits are set by the internal logic • these bits can be read out and reset by writing logical "1" to them • writing logical "0" doesn't influence the states of these bits
RW	**read write** • these bits can be read out and written via the PCI bus

12.2 Internal Register

00h

A d.	Bit	Type	Default Value	Register Name	Page
00h	31:0		00000000h	ICR - Interrupt Control Register	202
	31:29	R	000b	Reserved	202
	28	RW	0b	EEPROM_Control_Int_En	121
	27	RW	0b	Retry_Counter_Down_ Int_En	31
	26	RW	0b	FIFO_Overflow_Empty_ Int_En	41
	25	RW	0b	DMA_Write_Counter_ Overflow_Int_En	41
	24	RW	0b	DMA_Write_Counter_Int_ En	41
	23:18	R	000000b	Reserved	202
	17	RW	0b	INT0_En	202
	16	RW	0b	INT0_Pol	202
	15:13	R	000b	Reserved	202
	12	RC	0b	EEPROM_Control_Int	121
	11	RC	0b	Retry_Counter_Int	31
	10	RC	0b	FIFO_Overflow_Empty_ Int	41
	9	RC	0b	DMA_Write_Counter_ Overflow_Int	41
	8	RC	0b	DMA_Write_Counter_Int	41

00h (cont'd)

Ad.	Bit	Type	Default Value	Register Name	Page
	7:6	R	0b	Reserved	202
	5	RC	0b	GP3_INT	101
	4	RC	0b	GP2_INT	101
	3	RC	0b	GP1_INT	101
	2	RC	0b	GP0_INT	101
	1	RC	0b	INT0	202

04h

Ad.	Bit	Type	Default Value	Register Name	Page
04h	31:0		00000000h	DMA Control Register	43
	31:09	R	0000000h	Reserved	43
	8	RW	0b	DMA Start	43
	7:6	R	00b	Reserved	43
	5:0	RW	000000b	DMA Select - all modes IOM-2 Mode 1 IOM-2 Mode 2 IOM-2 Mode 3 Single Modem Mode V2.1 Single Modem Mode V3.X Dual Modem+Voice Mode	43 48 52 55 63 67 75

08h

Ad.	Bit	Type	Default Value	Register Name	Page
08h	31:12	RW	00000h	Circular Buffer Start Address	45
	11:0	R	000h		

0Ch

Ad.	Bit	Type	Default Value	Register Name	Page
0Ch	31:00	R	00000000h	Actual Circular Buffer Pointer	45

10h

Ad.	Bit	Type	Default Value	Register Name	Page
10h	31:0		00000000h	ALIS Command Register 1	67
	31:25	R	00h	Reserved	67
	24	RW	0b	New_ALIS_Command_1	67
	23:16	RW	00h	ALIS_Received_Data_1	67
	15:8	RW	00h	ALIS_Command_1	67
	7:0	RW	0b	ALIS_Transmit_Data_1	67

14h

Ad.	Bit	Type	Default Value	Register Name	Page
14h	31:0		00000000h	ALIS Command Register 2	70
	32:25	R	000h	Reserved	70
	24	RW	0b	New_ALIS_Command_2	70
	23:16	RW	00h	ALIS_Received_Data_2	70
	15:8	RW	00h	ALIS_Command_2	70
	7:0	RW	00h	ALIS_Transmit_Data_2	70

18h

Ad.	Bit	Type	Default Value	Register Name	Page
18h	31:0		00000000h	GP I/O Interface Control Register	102
	31:28	R	0h	Reserved	102
	27	RW	0b	GP3_Int_En	102
	26	RW	0b	GP2_Int_En	102
	25	RW	0b	GP1_Int_En	102
	24	RW	0b	GP0_Int_En	102
	23:20	R	0000b	Reserved	102
	19	RW	0b	GP3_Out_En	102
	18	RW	0b	GP2_Out_En	102

18h (cont'd)

Ad.	Bit	Type	Default Value	Register Name	Page
	17	RW	0b	GP1_Out_En	102
	16	RW	0b	GP0_Out_En	102
	15:12	R	0000b	Reserved	102
	11	R	-	GP3_IN	102
	10	R	-	GP2_IN	102
	9	R	-	GP1_IN	102
	8	R	-	GP0_IN	102
	7:4	R	0000b	Reserved	102
	3	RW	0b	GP3_OUT	102
	2	RW	0b	GP2_OUT	102
	1	RW	0b	GP1_OUT	102
	0	RW	0b	GP0_OUT	102

1Ch

Ad.	Bit	Type	Default Value	Register Name	Page
1Ch	31:0		00000000h	MISC - Miscellaneous Register	59
	31	RW	0b	IOM B1 Masking	59
	30	RW	0b	IOM B2 Masking	59
	29	RW	0b	IOM MON0/IC1 Masking	59
	28	RW	0b	IOM D+C/I0+MR+MX / IC2 Masking	59

1Ch (cont'd)

Ad.	Bit	Type	Default Value	Register Name	Page
	27	RW	1b	Serial Interface Buffer Mode	204
	26	RW	0b	Parallel Interface Mode	78
	25	RW	1b	Soft reset Serial Interface	204
	24	RW	0b	Soft reset Parallel Interface	78
	23:16	RW	00h	Retry Count Register	32
	15:12	R	0000b	Reserved	204
	11:0	RW	0000h	DMA Write Count Register	46

20h

Ad.	Bit	Type	Default Value	Register Name	Page
20h	31:0		00000000h	Serial Clock Select Register	
	31:2	R	00000000h	Reserved	
	1	RW	0b	DCL_Out_En	49 52 55 64 72
	0	RW	0b	Serial_Clock_Sel	49 52 55 64 72

24h

Ad.	Bit	Type	Default Value	Register Name	Page
24h	31:0		00000000h	EEPROM Control Register	121
	31:25	R	0000h	Reserved	121
	24	RW	0b	EEPROM Start	121
	23:16	RW	00h	EEPROM Command	121
	15:8	RW	00h	EEPROM Byte Address	121
	7:0	RW	00h	EEPROM Data	121

28h

Ad.	Bit	Type	Default Value	Register Name	Page
28h	31:0		00000000h	DMA TEST Register	204
	31:01	R	00000000h	Reserved	204
	0	RW	0b	Loop_Back_Mode	77

12.3 Registers which do not occur elsewhere in the Data Sheet

00h

Bit 31:0	ICR - Interrupt Control Register
Default Value	00000000h
Description	The interrupt enable bits for GP3-0 are placed in the GP I/O Interface Control Register. All interrupt enables are high active: Int_En='0' -> corresponding interrupt (bit) is disabled Int_En='1' -> corresponding interrupt (bit) is enables

Bit 31:29	Reserved
Type	R
Value	000b

Bit 23:18	Reserved
Type	R
Value	000000b

Bit 17	INT0_En
Type	RW
Default Value	RW
Description	Enable for the INT0 interrupt bit.

00h (cont'd)

Bit 16	INT0_POL
Type	RW
Default Value	0b
Description	Polarity of INT0 active level 0: L-Level 1: H-level

Bit 23:18	Reserved
Type	R
Value	000000b

Bit 1	INT0
Type	RC
Default Value	0b
Description	An interrupt is detected on pin $\overline{\text{INT0}}$.

Bit 0	Reserved
Type	R
Value	0b

1Ch

Bit 27	Serial Interface Buffer Mode
Type	RW
Value	1b
Description	0: The TXD pin is configured as PUSH/PULL output pin. 1: The TXD pin is configured as OPEN DRAIN output pin.

Bit 25	Soft Reset Serial Interface
Type	RW
Default Value	1b
Description	0: Activates the low active reset signal $\overline{SRST}$ to the application. 1: Deactivates the reset signal $\overline{SRST}$ to the application. Before asserting this bit the DMA_Start bit has to be reset.

28h

Bit 31:0	DMA Test Register
Default Value	00000000h

Bit 31:1	Reserved
Type	R
Default Value	00000000h

13 Abbreviations

AC	Alternating Current.
A/D	Analog to digital.
ADC	Analog to digital converter.
ALE	Address latch enable.
ALIS	Analog Line Interface Solution. Chip set consisting of PSB4595 and PSB4596.
DC	Direct Current.
DCL	Double Bit Clock. (In this context, only in the IOM-2 modes of the serial interface of the PITA, single bit in all other modes).
DMA	Direct Memory Access.
DD	Data Downstream.
DU	Data Upstream.
EEPROM = E^2PROM	Electrically erasable programmable read only memory.
FIFO RX FIFO TX FIFO	First in first out.
FSC	Frame Sync.
I/O	In/out.
IOM	ISDN Oriented Modular.
ISDN	Integrated Services Digital Network.
MSB	Most Significant Bit.
PITA	PCI Interface for Telephony/Data Applications.
PCI	Peripheral Component Interconnect.
RXD	Receive Direction.
TXD	Transmit Direction.

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