DATA SHEET

LXT359

JUNE 1999
Revision 2.1

Integrated T1 LH/SH Transceiver for DS1/DSX-1/CSU or NTU/ISDN PRI Applications

General Description

The LXT359 is a T1 Primary rate, combination transceiver for T1 long and short-haul applications. It operates over (22 AWG) twisted-pair cable for 0 to 6 kft and offers Line Build-Outs and pulse equalization settings for all T1 applications including D4 Channel bank.

The LXT359 provides both a serial port for microprocessor control and a hardware control mode for stand alone operation. It incorporates crystal-less digital jitter attenuation in either the transmit or receive data path starting at 3 Hz. B8ZS encoding/decoding and unipolar or bipolar data I/O are available. It provides loss of signal monitoring and a variety of diagnostic loopback modes.

The LXT359 uses an advanced double-poly, double-metal fabrication process and requires only a single 5-volt power supply.

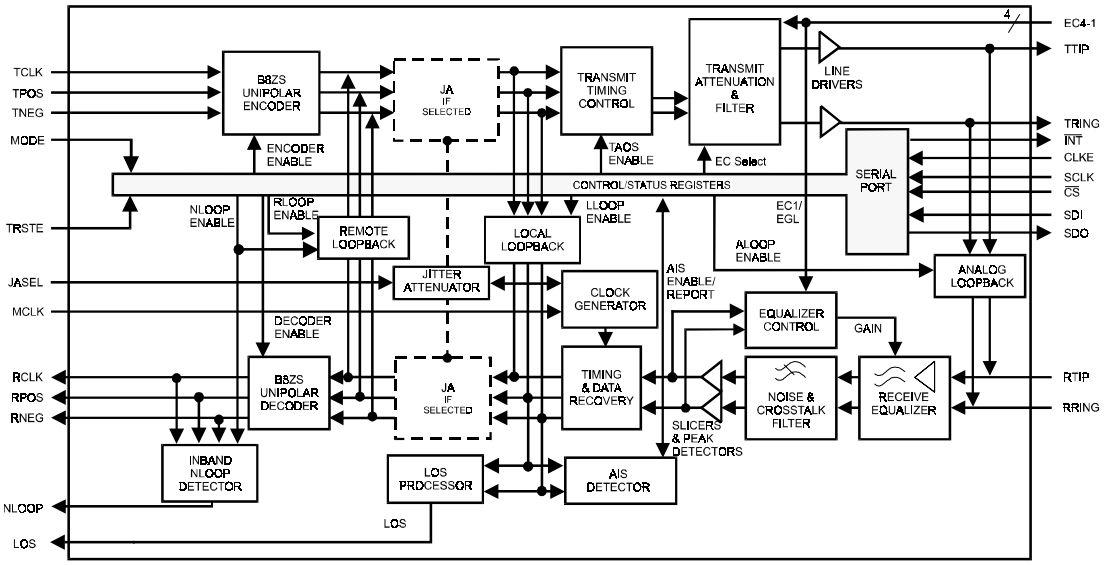
Applications

- HDSL access systems
- ISDN Primary Rate Interface (ISDN PRI)
- CSU interface to T1 service
- T1 LAN/WAN bridge/routers
- D4 Channel bank and newer generation DLC

Features

- Fully integrated transceiver for Long or Short-Haul T1 interfaces
- Crystal-less digital jitter attenuation
- Select either transmit or receive path
- No crystal or high speed external clock required
- Meet or exceed specifications in ANSI T1.403 and T1.408; ITU I.431, T1.102 and AT&T Pub 62411
- Selectable receiver sensitivity – fully restores the received signal after transmission through a cable with attenuation of either 0 to 26 dB, or 0 to 36 dB @ 772 kHz
- Five Pulse Equalization Settings for T1 short-haul applications (DSX-1)
- 6V output signal for D4 Channel bank
- Four Line Build-Outs for T1 long-haul applications from 0 dB to -22.5 dB
- LOS processor per ANSI T1.231
- Selectable unipolar or bipolar data I/O and B8ZS encoding/decoding
- Local, remote, analog and inband network loopback generation and detection
- Serial-interface for microprocessor control
- Available in 28-pin PLCC, 44-pin PQFP and 44-pin LQFP packages

LXT359 Block Diagram



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PIN ASSIGNMENTS AND SIGNAL DESCRIPTIONS

Figure 1: LXT359 Hardware Controlled Bipolar Mode Pin Assignments

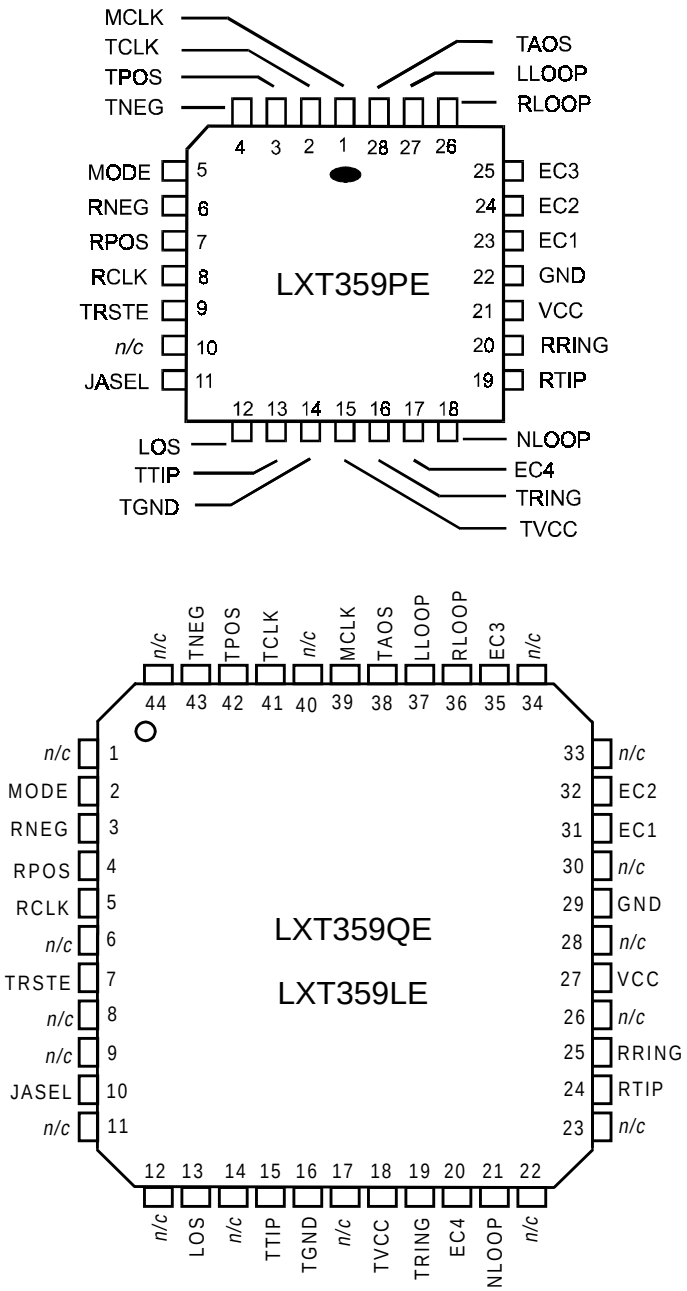


Table 1: LXT359 Clock and Data Pins by Mode[1]

Pin #		Bipolar	Unipolar	Pin #		Bipolar	Unipolar
PLCC	QFP			PLCC	QFP		
1	39	MCLK		13	15	TTIP	
2	41	TCLK		14	16	TGND	
3	42	TPOS	TDATA	15	18	TVCC	
4	43	TNEG	INSBPV	16	19	TRING	
6	3	RNEG	BPV	19	24	RTIP	
7	4	RPOS	RDATA	20	25	RRING	
8	5	RCLK		21	27	VCC	
				22	29	GND	

1. Data pins change based on whether external or internal QRSS mode is active. Clock pins remain the same in both Hardware and Host modes.

Table 2: LXT359 Control Pins by Mode

Pin #		Hardware Modes	Host Modes	Pin #		Hardware Modes	Host Modes
PLCC	QFP	Unipolar/ Bipolar	Unipolar/ Bipolar	PLCC	QFP	Unipolar/ Bipolar	Unipolar/ Bipolar
5	2	MODE	MODE	25	35	EC3	SDO
9	7	TRSTE	TRSTE	17	20	EC4	*Low*
11	10	JASEL	*Low*	18	21	NLOOP	NLOOP
12	13	LOS	LOS	26	36	RLOOP	$\overline{CS}$
23	31	EC1	$\overline{INT}$	27	37	LLOOP	SCLK
24	32	EC2	SDI	28	38	TAOS	CLKE

Table 3: LXT359 Hardware Controlled Bipolar Mode Signal Descriptions

Pin #		Symbol	I/O[2]	Description
PLCC	QFP			
1[1]	39[1]	MCLK	DI	**Master Clock**. Connect to 1.544 MHz. MCLK input requires an external, independent clock signal to generate internal clocks. Required accuracy is better than ± 50 ppm with a typical duty cycle of 50%. Upon Loss of Signal (LOS), RCLK is derived from MCLK.
2[1]	41[1]	TCLK	DI	**Transmit Clock**. 1.544 MHz input. Transceiver samples TPOS and TNEG on the falling edge of TCLK
3 4	42 43	TPOS TNEG	DI	**Transmit Data – Positive and Negative**. In the Bipolar I/O mode, these pins are the positive and negative sides of a bipolar input pair. Data to be transmitted onto the twisted-pair line is input at these pins. Table 4 describes Unipolar Mode functions.
5[1]	2	MODE	DI	**Mode Select**. Connecting MODE Low puts the LXT359 in the Hardware Mode. In Hardware Mode, the serial interface is disabled and hardwired pins are used to control configuration and report status. Connecting MODE to Midrange[3] activates the Hardware Mode and enables the B8ZS encoder/decoder and Unipolar Mode. Connecting MODE High puts the LXT359 in the Host Mode. In the Host Mode, the serial interface controls the LXT359 and displays its status.
6 7	3 4	RNEG RPOS	DO	**Receive Data – Negative and Positive**. In the Bipolar I/O mode, these pins are the positive and negative sides of a bipolar output pair. Data recovered from the line interface is output on these pins. A signal on RNEG corresponds to receipt of a negative pulse on RTIP/RRING. A signal on RPOS corresponds to receipt of a positive pulse on RTIP/RRING. RNEG/RPOS outputs are Non-Return-to-Zero. Both outputs are stable and valid on the rising edge of RCLK. Refer to Table 4 for Unipolar Mode function descriptions.
8	5	RCLK	DO	**Recovered Clock**. The clock recovered from the line input signal is output on this pin. Under LOS conditions there is a smooth transition from the RCLK signal (derived from the recovered data) to the MCLK signal at the RCLK output.
9	7	TRSTE	DI	**Tristate**. Connecting TRSTE High forces all output pins to a high impedance state. Connecting TRSTE Low sets LXT359 to the Hardware Bipolar Mode. Connecting TRSTE to Midrange[3] enables the Unipolar Mode. (See Table 4 for Unipolar function descriptions.)
10	–	*n/c*	–	*No connection. Leave this pin floating.*

1. These pins do not change function as the operating mode changes. Tables 4 and 5 do not describe these pins.
2. I/O column entries: DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output.
3. Midrange is a voltage level such that 2.3 V ≤ Midrange ≤ 2.7 V or the pin may float.
4. Pins 1, 6, 8, 9, 11, 12, 14, 17, 22, 23, 26, 28, 30, 33, 34, 40, and 44 are not connected (*n/c*).

Table 3: LXT359 Hardware Controlled Bipolar Mode Signal Descriptions – continued

Pin #		Symbol	I/O[2]	Description
PLCC	QFP			
11	10	JASEL	DI	**Jitter Attenuation Select**. Selects jitter attenuation location. Connecting JASEL High activates the jitter attenuator in the receive path. Connecting JASEL Low activates the jitter attenuator in the transmit path. Connecting JASEL to Midrange[3] disables jitter attenuation.
12	13	LOS	DO	**Loss of Signal Indicator**. LOS goes High on receipt of 175 consecutive spaces and returns Low when the received signal reaches a mark density of 12.5% (determined by receipt of 16 marks within a sliding window of 128 bits with fewer than 100 consecutive zeros). The transceiver outputs received marks on RPOS and RNEG even when LOS is High.
13[1] 16[1]	15[1] 19[1]	TTIP TRING	AO	**Transmit Tip and Ring**. Differential Driver Outputs. These outputs are designed to drive a 50 - 200 Ω load. The transformer and line matching resistors should be selected to give the desired pulse height and return loss performance.
14[1]	16[1]	TGND		**Ground** return for the transmit drivers power supply TVCC.
15[1]	18[1]	TVCC	DI	**+5 VDC Power Supply** input for the transmit drivers. TVCC must not vary from VCC by more than ± 0.3 V.
17	20	EC4	DI	**Equalization Control 4**. Used along with EC3-1 pins for Pulse Equalization and LBO settings.
18[1]	21[1]	NLOOP	DO	**Network Loopback Detection**. If the LXT359 is configured to detect Network Loopback (NLOOP) (by connecting the RLOOP pin to Midrange[3]), this pin goes High when an Inband Network Loopback has been activated by the reception of a 00001 pattern for five seconds. NLOOP is reset by reception of 001 for five seconds, or by activation of RLOOP.
19[1] 20[1]	24[1] 25[1]	RTIP RRING	AI	**Receive Tip and Ring**. The AMI signal received from the line is applied at these pins. A 1:1 transformer is required. Data and clock from the signal applied at these pins are recovered and output on the RPOS/RNEG, and RCLK pins.
21[1]	27[1]	VCC		**+5 VDC Power Supply** for all circuits except the transmit drivers. (Transmit drivers are supplied by TVCC.)
22[1]	29[1]	GND		**Ground** return for power supply VCC.
23 24 25	31 32 35	EC1 EC2 EC3	DI	**Equalization Control 1-3**. EC1-3 (along with the EC4 pin) define the Pulse Equalization, Line Build Outs and Equalizer Gain Limit settings. See Table 6 for additional details.

1. These pins do not change function as the operating mode changes. Tables 4 and 5 do not describe these pins.
2. I/O column entries: DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output.
3. Midrange is a voltage level such that 2.3 V ≤ Midrange ≤ 2.7 V or the pin may float.
4. Pins 1, 6, 8, 9, 11, 12, 14, 17, 22, 23, 26, 28, 30, 33, 34, 40, and 44 are not connected (*n/c*).

Table 3: LXT359 Hardware Controlled Bipolar Mode Signal Descriptions – continued

Pin #		Symbol	I/O[2]	Description
PLCC	QFP			
26	36	RLOOP	DI	**Remote Loopback.** When held High, the clock and data inputs from the framer (TPOS/TNEG or TDATA) are ignored and the data received from the twisted-pair line is transmitted back onto the line at the RCLK frequency. During remote loopback, the device ignores the in-line encoders/decoders. Connecting this pin to Midrange enables Network Loopback. See Figure 6.
27	37	LLOOP	DI	**Local Loopback**. When held High, the data on TPOS and TNEG loops back digitally to RPOS and RNEG outputs (through JA if enabled). Connecting this pin to Midrange[3] enables Analog Loopback (TTIP and TRING are looped back to RTIP and RRING). See Figures 3, 4, and 5.
28	38	TAOS	DI	**Transmit All Ones**. When held High the transmit data inputs are ignored and the LXT359 transmits a stream of 1's at the TCLK frequency. (If TCLK is not supplied, MCLK is the transmit clock reference.) TAOS is inhibited during Remote Loopback. Connecting this pin to Midrange enables QRSS pattern generation and detection. See Figure 3 and 8.

1. These pins do not change function as the operating mode changes. Tables 4 and 5 do not describe these pins.
2. I/O column entries: DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output.
3. Midrange is a voltage level such that 2.3 V ≤ Midrange ≤ 2.7 V or the pin may float.
4. Pins 1, 6, 8, 9, 11, 12, 14, 17, 22, 23, 26, 28, 30, 33, 34, 40, and 44 are not connected (*n/c*).

Table 4: LXT359 Hardware Controlled Unipolar Mode Signal Assignments[1]

Pin #		Symbol	I/O[2]	Description
PLCC	QFP			
3	42	TDATA	DI	**Transmit Data**. Unipolar input for data to be transmitted onto the twisted-pair line.
4	43	INSBPV	DI	**Insert Bipolar Violation**. This pin is sampled on the falling edge of TCLK to control Bipolar Violation Insertions in the transmit data stream. A Low-to-High transition is required to insert subsequent BPVs.
6	3	BPV	DO	**Bipolar Violation.** BPV goes High to report receipt of a bipolar violation from the line. This is an NRZ output, valid on the rising edge of RCLK.
7	4	RDATA	DO	**Receive Data**. RDATA is a unipolar NRZ output of data recovered from the line interface. In Hardware Mode RDATA is stable and valid on the rising edge of RCLK.

1. For description of pins not shown in this table: see Table 3.
2. I/O column entries: DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output.

Table 5: LXT359 Host Controlled Bipolar Mode Signal Assignments

Pin #		Symbol	I/O[1]	Description
PLCC	QFP			
5	2	MODE	DI	**Mode**. Connecting MODE High puts the LXT359 in Host Mode. In Host Mode, the serial interface controls the LXT359 and displays its status.
6 7	3 4	RNEG RPOS	DO	**Received Data–Negative and Positive**. In the Bipolar I/O Mode, these pins are the negative and positive sides of a bipolar output pair. The transceiver outputs the data recovered from the line interface on these pins. A signal on RNEG corresponds to receipt of a negative pulse on RTIP/RRING. A signal on RPOS corresponds to receipt of a positive signal on RTIP/RRING. RNEG/RPOS outputs are Non-Return-to-Zero (NRZ). CLKE determines the clock edge at which these outputs are stable and valid. See Figure 14.
9	7	TRSTE	DI	**Tristate**. Connecting TRSTE High forces all output pins to high-impedance state. Connect this pin Low for normal operation.
10	–	n/c	–	*Not connected.*
11	10	n/c	–	*Connect Low.*
17	20	n/c	–	*Connect Low.*
18	21	NLOOP	DO	**Network Loopback**. This pin goes High when an Inband Network Loopback has been activated.
23	31	$\overline{\text{INT}}$	DO	**Interrupt** (Active Low–Maskable). $\overline{\text{INT}}$ goes Low to flag the host when the LOS, NLOOP or AIS changes state. $\overline{\text{INT}}$ is an open drain output which requires a connection to power supply VCC through a resistor. Reset $\overline{\text{INT}}$ by writing a one to the respective bit in the Interrupt Clear Register.
24	32	SDI	DI	**Serial Data Input**. Input port for the 16-bit serial address/command and data word. The LXT359 samples SDI on the rising edge of SCLK. See Figures 15 and 16.
25	35	SDO	DO	**Serial Data Output**. If CLKE is High, SDO is valid on the rising edge of SCLK. If CLKE is Low, SDO is valid on the falling edge of SCLK. This pin goes to a high-impedance state when the serial port is being written to or when $\overline{\text{CS}}$ is High. See Figure 16.
26	36	$\overline{\text{CS}}$	DI	**Chip Select** (Active Low). This input is used to access the serial interface. For each read or write operation, $\overline{\text{CS}}$ must transition from High to Low, and remain Low.
27	37	SCLK	DI	**Serial Clock**. This clock is used to write data to or read data from the serial interface registers. The clock frequency can be any rate up to 1.544 MHz.
28	38	CLKE	DI	**Clock Edge**. Setting CLKE High causes RPOS and RNEG to be valid on the falling edge of RCLK, with SDO valid on the rising edge of SCLK. Setting CLKE Low makes RPOS and RNEG valid on the rising edge of RCLK and SDO valid on the falling edge of SCLK.

1. I/O column entries: DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output.

FUNCTIONAL DESCRIPTION

The LXT359 is a fully integrated PCM transceiver for long or short-haul, 1.544 Mbps (T1) applications allowing full-duplex transmission of digital data over existing twisted-pair installations. It interfaces with two twisted-pair lines (one pair each for transmit and receive) through standard pulse transformers and appropriate resistors.

The figure on the front page of this Data Sheet shows a block diagram of the LXT359. Control of the chip is via either a serial microprocessor port or, in Hardware Mode, via individual pin settings. It also provides a high-precision, crystal-less jitter attenuator. The user may place it in the transmit or receive path, or bypass it completely.

The transceiver meet or exceed FCC and AT&T specifications for CSU and DSX-1 applications, as well as ANSI T1, requirements.

Initialization

During power up, the transceiver remains static until the power supply reaches approximately 3 V. On crossing this threshold, the device begins a 32 ms reset cycle to calibrate the Phase Lock Loops (PLL). The transceiver uses a reference clock to calibrate the PLL; the transmitter reference is TCLK, and the receiver reference clock is MCLK. MCLK is mandatory for chip operation and must be an independent free running jitter free reference clock.

Reset Operation

Reset clears and sets all registers to 0 and resets the status and state machines for LOS and NLOOP blocks. In Hardware Mode, holding pins RLOOP, LLOOP and TAOS High for at least one clock cycle resets the device. Writing a 1 to the bit CR2.RESET commands reset in Host Mode. Allow 32 ms for the device to settle after removing all reset conditions.

Transmitter

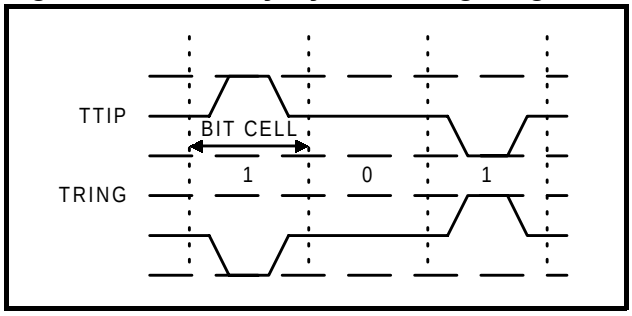
Digital Data Interface

Input data for transmission onto the line is clocked serially into the device at the TCLK rate. TPOS and TNEG are the bipolar data inputs. TDATA accepts unipolar data. (Setting the TRSTE pin to Midrange enables Hardware Unipolar Mode.) Input data may pass through either the Jitter Attenuator or B8ZS encoder or both. Bit CR1.ENCENB = 1 enables B8ZS encoding in Host Mode. In Hardware Mode, connecting the MODE pin to Midrange selects zero suppression coding. The transmit clock (TCLK) supplies input synchronization. The Test Specifications section defines the transmit timing requirements for TCLK and the Master Clock (MCLK).

Output Drivers

The transceivers transmit data as a 50% line code as shown in Figure 2. Activating the line driver only during a mark reduces power consumption. The output driver is disabled during transmission of a space. Biasing of the transmit DC level is on-chip.

Figure 2: 50% Duty Cycle Coding Diagram



Idle Mode

Transmit Idle Mode is a normal operational mode (as opposed to modes) which allows multiple transceivers to be connected to a single line for redundant applications. TTIP and TRING remain in a high impedance state when TCLK is not present. Remote or Dual Loopback, TAOS or any internal transmit patterns temporarily disable the high impedance state as will detection of Network Loop Up code in the receive direction.

Pulse Shape

The Equalizer Control inputs (EC4-1) determine the transmitted pulse shape as specified in Table 6. In Host Mode, the I/O port controls the EC*x* values. In Hardware Mode, four individual pins provide the EC*x* inputs.

Shaped pulses meeting various T1 specifications are applied to the AMI line driver for transmission onto the line at TTIP and TRING. The transceivers produce DSX-1 pulses for short-haul T1 applications (settings from 0 dB to +3.0 dB), D-4 channel bank pulses for short-haul T1 appli-

cations and DS1 pulses for long-haul T1 applications (settings from 0 dB to -22.5 dB). Refer to the Test Specifications section for pulse mask specifications.

Receiver

A 1:1 transformer provides the interface to the twisted-pair line. Recovered data is output at RPOS/RNEG (RDATA in Unipolar Mode), and the recovered clock is output at RCLK. The Test Specifications section shows receiver timing.

Receive Equalizer

The receive equalizer processes the signal received at RTIP and RRING. The equalizer control (EC*x*) input pins or register bits determine the maximum gain applied at the equalizer. With EC1 Low, up to 36 dB of gain may be applied. When EC1 is High, 26 dB is the gain limit to provide an increased noise margin in shorter loop operations.

The receiver can accurately recover signals with up to 36 dB of cable attenuation (from 2.4 V).

Data Recovery

The transceiver filters the equalized signal and applies it to the peak detector and data slicers. The peak detector samples the inputs and determines the maximum value of the received signal. The data slicers are set at 50% of the peak value to ensure optimum signal-to-noise performance.

After processing through the data slicers, the received signal goes to the data and timing recovery section, then to the B8ZS decoder (if selected) and to the receive monitor. The data and timing recovery circuits provide input jitter tolerance significantly better than required by AT&T Pub 62411. See the Test Specifications section.

Digital Data Interface

In either Host or Hardware Control Mode the recovered data goes to the Loss of Signal (LOS) Monitor. The jitter attenuator circuit may be enabled or disabled in the receive data path or the transmit path. Received data may be routed to the B8ZS decoder (if selected). Finally, the device may send the digital data to the framer as either unipolar or bipolar data.

When transmitting unipolar data to the framer, the device reports receiving bipolar violations by driving the BPV pin High.

Jitter Attenuation

A Jitter Attenuation Loop (JAL) with an Elastic Store (ES) provides jitter attenuation as shown in the Test Specifications section. The JAL requires no special circuitry, such as an external quartz crystal or high-frequency clock (higher than the line rate). Its timing reference is the master clock, MCLK.

In Hardware Control Mode the ES is a 32 x 2-bit register. Setting the JASEL pin High places the JA circuitry in the received data path; setting JASEL Low places the JA in the transmit data path; tying it to Midrange disables the JA.

In Host Mode, bit CR1.JASEL0 enables or disables the JA circuit. With bit CR1.JASEL0 = 1, bit CR1.JASEL1 controls the JA circuit placement (see Table 11).

The device clocks data into the ES using either TCLK or Receiver Recovered Clock depending on whether the JA circuitry is in the transmit or receive data path, respectively. Data is shifted out of the elastic store using the dejittered clock from the JAL. When the FIFO is within two bits of overflowing or underflowing, the ES adjusts the output clock by $^1/_8$ of a bit period. The ES produces an average delay of 16 bits in the associated data path. When the Jitter Attenuator is in the receive path, the output RCLK transitions smoothly to MCLK in the event of an LOS condition.

Table 6: Equalizer Control Input Settings

EC4	EC3	EC2	EC1[1]	Function	Pulse	Cable	Gain	Coding[2]
0	0	0	0	T1 Long Haul	0.0 dB pulse	100 Ω TP	36 dB	B8ZS
0	0	1	0	T1 Long Haul	-7.5 dB pulse	100 Ω TP	36 dB	B8ZS
0	1	0	0	T1 Long Haul	-15.0 dB pulse	100 Ω TP	36 dB	B8ZS
0	1	1	0	T1 Long Haul	-22.5 dB pulse	100 Ω TP	36 dB	B8ZS
0	0	0	1	T1 Long Haul	0.0 dB pulse	100 Ω TP	26 dB	B8ZS
0	0	1	1	T1 Long Haul	-7.5 dB pulse	100 Ω TP	26 dB	B8ZS
0	1	0	1	T1 Long Haul	-15.0 dB pulse	100 Ω TP	26 dB	B8ZS
0	1	1	1	T1 Long Haul	-22.5 dB pulse	100 Ω TP	26 dB	B8ZS
1	0	0	1	D4 Short Haul	6V pulse	100 Ω TP	12 dB	B8ZS
1	0	1	1	T1 Short Haul	0-133 ft / 0.6 dB	100 Ω TP	12 dB	B8ZS
1	1	0	0	T1 Short Haul	133-266 ft / 1.2 dB	100 Ω TP	12 dB	B8ZS
1	1	0	1	T1 Short Haul	266-399 ft / 1.8 dB	100 Ω TP	12 dB	B8ZS
1	1	1	0	T1 Short Haul	399-533 ft / 2.4 dB	100 Ω TP	12 dB	B8ZS
1	1	1	1	T1 Short Haul	533-655 ft / 3.0 dB	100 Ω TP	12 dB	B8ZS

1. EC1 sets the receive equalizer gain (EGL) during T1 long-haul operation.
2. When enabled.

Diagnostic Mode Operation

Diagnostic modes as shown in Table 7. In Hardware Mode, the diagnostic modes are selected by a combination of pin settings. In Host Mode, the diagnostic modes are selected by writing appropriate bits in the Diagnostic Control Register.

Table 7: Diagnostic Mode Availability

Diagnostic Mode	Availability[1]		Host Mode Maskable[2]
	Hardware	Host	
Loopback Modes			
Local Loopback (LLOOP)	Yes	Yes	No
Analog Loopback (ALOOP)	Yes	Yes	No
Remote Loopback (RLOOP)	Yes	Yes	No
In-band Network Loopback (NLOOP)	Yes	Yes	Yes
Dual Loopback (DLOOP)	Yes	Yes	No
Internal Data Pattern Generation and Detection			
Transmit All Ones (TAOS)	Yes	Yes	No
In-band Loop up/down Code Generator	No	Yes	No
Error Insertion and Detection			
Bipolar Violation Insertion (INSBPV)	Yes	Yes	No
Bipolar Violation Detection (BPV)	Yes	Yes	No
Alarm Condition Monitoring			
Receive Loss of Signal (LOS) Monitoring	Yes	Yes	Yes

1. In Hardware Control Mode, a combination of pin settings selects the Diagnostics Modes; in Host Control Mode, writing appropriate bits in the Control Registers selects the Diagnostic Modes.
2. Host Control Mode allows interrupt masking by writing a “1” to the corresponding bit in the Interrupt Clear Register. Hardware Control Mode has no interrupt masking feature.

Loopback Modes

Local Loopback

See Figures 3 and 4. In Hardware Mode, Local Loopback (LLOOP) is selected by tying LLOOP High; in Host Mode, by setting CR2.ELLOOP to 1. LLOOP inhibits the receiver circuits. The transmit clock and data inputs (TCLK and TPOS/TNEG or TDATA) loop back through the jitter attenuator (if enabled) and show up at RCLK and RPOS/RNEG or RDATA. Note that during LLOOP, the JASEL input is strictly an Enable/Disable control, i.e. it does not affect the placement of the JAL. If JA is enabled, it is active in the loopback circuit. If JA is bypassed, it is not active in the loopback circuit.

The transmitter circuits are unaffected by LLOOP. LXT359 transmits the TPOS/TNEG or TDATA inputs (or a stream of 1's if TAOS is asserted) normally. When used in this mode, the transceiver can function as a stand-alone jitter attenuator.

Figure 3: TAOS with LLOOP *(JA Selected)*

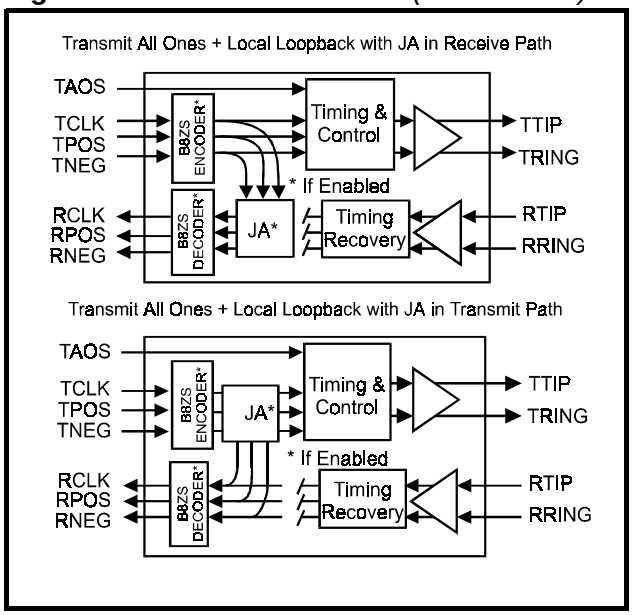
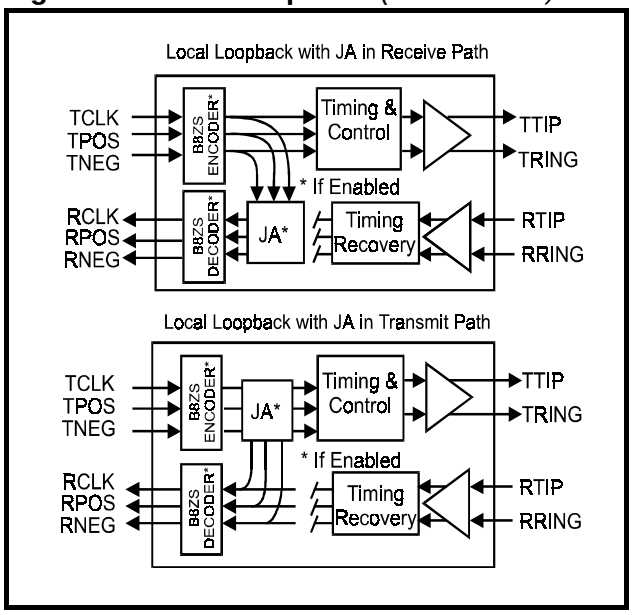


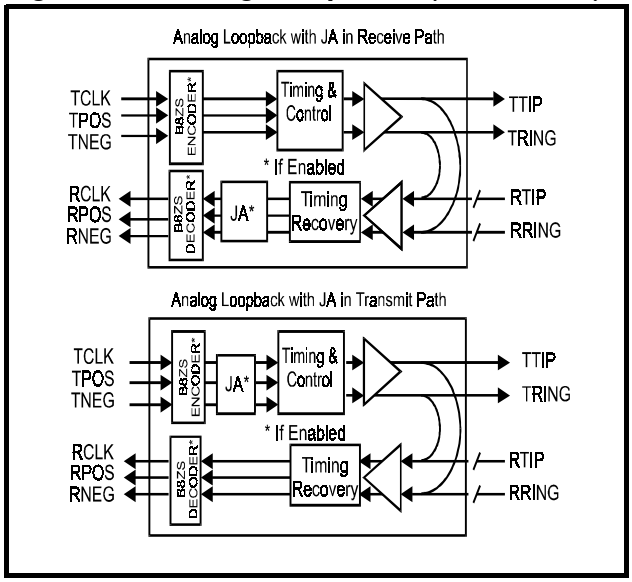
Figure 4: Local Loopback *(JA Selected)*



Analog Loopback

See Figure 5. Analog Loopback (ALOOP) exercises the maximum number of functional blocks. ALOOP operation disconnects the RTIP/RRING inputs from the line and routes the transmit outputs back into the receive inputs. This tests the encoders/decoders, jitter attenuator, transmitter, receiver and timing recovery sections. In Hardware Mode, tying pin 27 to Midrange commands Analog Loopback; in Host Mode, writing a 1 to bit CR2.EALOOP enables the function. The ALOOP function overrides all other loopback modes.

Figure 5: Analog Loopback *(JA Selected)*



Remote Loopback

See Figure 6. In Remote Loopback (RLOOP) mode, the device ignores the transmit data and clock inputs (TCLK and TPOS/TNEG or TDATA), and bypasses the in-line encoders/decoders. The RPOS/RNEG or RDATA outputs loop back through the transmit circuits to TTIP and TRING at the RCLK frequency. The RLOOP command does not affect the receiver circuits which continue to output the RCLK and RPOS/RNEG or RDATA signals received from the twisted-pair line. In Host Mode, command RLOOP by writing a 1 to bit CR2.ERLOOP. In Hardware Mode, RLOOP is commanded by setting pin 26 High.

Network Loopback

Network Loopback (NLOOP) can be initiated only when the Network Loopback detect function is enabled. In Host Mode, writing a 1 to CR2.ENLOOP enables NLOOP detection. In Hardware Mode, setting RLOOP to Midrange enables Network Loopback detection.

With NLOOP detection enabled, the receiver looks for the NLOOP data patterns (00001 = enable, 001 = disable) in the input data stream. When the receiver detects an NLOOP enable data pattern repeated for a minimum of five seconds, the device enables RLOOP. The device responds to both framed and unframed NLOOP patterns. Once NLOOP detection is enabled at the chip and activated by the appropriate data pattern, it is identical to Remote Loopback (RLOOP). NLOOP is disabled by receiving the 001 pattern for five seconds, or by activating RLOOP or ALOOP, or by disabling NLOOP detection. The device goes into Dual Loopback Mode (DLOOP) in the case where it detects both the NLOOP and LLOOP functions.

Dual Loopback

See Figure 7. To select Dual Loopback (DLOOP), set both RLOOP and LLOOP High in Hardware Mode or set bits CR2.ERLOOP and CR2.ELLOOP to 1 in Host Mode. In DLOOP mode, the transmit clock and data inputs (TCLK and TPOS/TNEG or TDATA) loop back through the Jitter Attenuator (unless disabled) to RCLK and RPOS/RNEG or RDATA. The data and clock recovered from the twisted-pair line loop back through the transmit circuits to TTIP and TRING without jitter attenuation.

Figure 6: Remote Loopback *(JA Selected)*

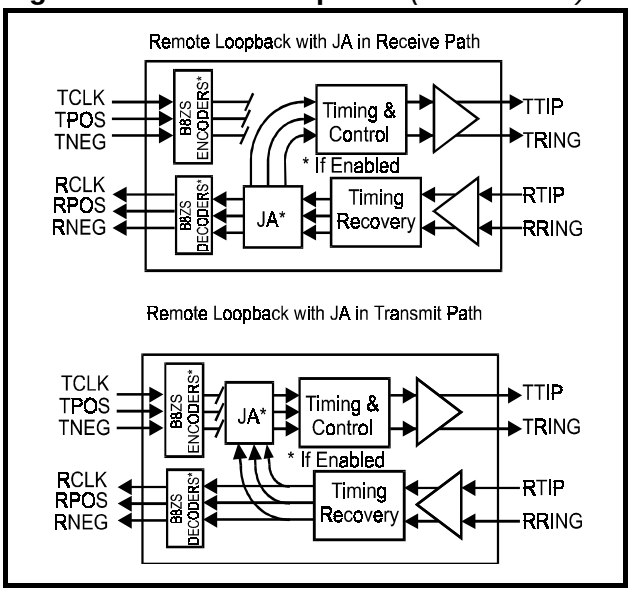
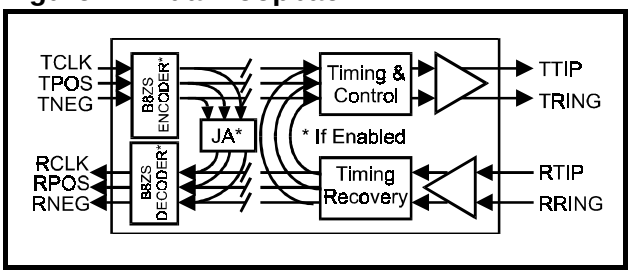


Figure 7: Dual Loopback

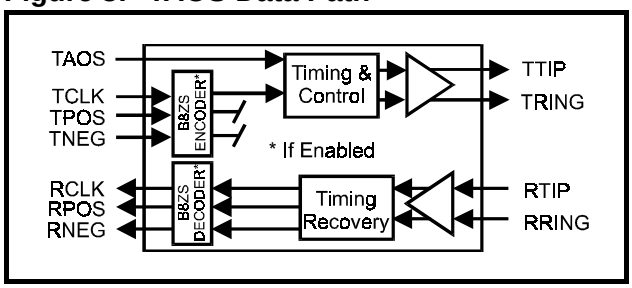


Internal Pattern Generation and Detection

Transmit All Ones

See Figure 8. In Transmit All Ones (TAOS) Mode the transceiver ignores the TPOS and TNEG inputs and transmits a continuous stream of 1's at the TCLK frequency. (With no TCLK, the TAOS output clock is MCLK.) This can be used as the Alarm Indication Signal (AIS–also called the Blue Alarm). In Host Mode, TAOS is commanded by writing a 1 to bit CR2.ETAOS. In Hardware Mode setting pin 28 High does so. Both TAOS and Local Loopback can occur simultaneously as shown in Figure 3, but Remote Loopback inhibits TAOS. When both TAOS and LLOOP are active, TCLK and TPOS/TNEG loop back to RCLK and RPOS/RNEG through the jitter attenuator (if enabled), and an all ones pattern goes to TTIP/TRING.

Figure 8: TAOS Data Path



In-Band Network Loop Up or Down Code Generator

In Host Mode, LXT359 can transmit in-band Network Loop Up or Loop Down code. The Loop Up code is 00001; Loop Down code is 001. A Loop Up code transmission occurs when Control Register #2 bits EPAT0 = 1 and EPAT1 = 0. A Loop Down code transmission requires that both EPAT0 and EPAT1 = 1.

Error Insertion and Detection

Bipolar Violation Insertion *(INSBPV)*

In Unipolar Mode, both Hardware and Host Modes provide for Bipolar Violation Insertion (INSBPV). Choosing Unipolar Mode configures pin 4 as INSBPV. Bipolar violation insertion requires a Low-to-High transition on INSBPV. Sampling occurs on the falling edge of TCLK. When INSBPV goes High a BPV is inserted on the next available mark except in the four following situations:

- Zero suppression (B8ZS) is not violated
- If LLOOP and TAOS are both active, the BPV is looped back to RNEG/BPV indicator and the line driver transmits all ones with no violation
- BPV insertion is disabled with RLOOP (remote loopback) active
- BPV insertion is disabled with NLOOP asserted (pin 10 High)

With the LXT359 configured to transmit internally generated data patterns (QRSS or NLOOP), a BPV can be inserted on the transmit pattern independent of whether the device is in the unipolar or bipolar mode of operation.

Alarm Condition Monitoring

Loss of Signal *(LOS)*

The count increments with each received 0 and the counter resets to 0 on receipt of a 1. When the count reaches n=0s, the LOS flag goes High, and the MCLK replaces the recovered clock at the RCLK output in a smooth transition.

When the received signal has 12.5% 1's (16 marks in a sliding 128-bit period, with fewer than 100 consecutive 0s), the LOS flag returns Low and the recovered clock replaces MCLK at the RCLK output in another smooth transition.

During LOS, the device sends received data to the RPOS/RNEG pins (or RDATA in Unipolar Mode). LXT359 reports an LOS condition on the LOS pin in Hardware Mode. In Host Mode, the LOS bit in the Performance Status Register goes High to indicate an LOS condition and will interrupt the host controller if so programmed.

Operating Modes

The LXT359 operates in either Hardware or (Serial Port) Host Mode. In the Hardware Mode, individual pins control the transceiver.

The logic level at the MODE pin sets the mode of operation. In Host Mode, a microprocessor controls the device through a data interface.

Hardware Mode Operation

The LXT359 operates in Hardware Mode when MODE is set to Midrange or Low. In Hardware Mode individual pins access and control the transceiver. The outputs (RPOS/RNEG or RDATA) are valid on the rising edge of RCLK.

There are some advanced functions provided only in Host Mode. Interrupt ($\overline{INT}$) and CLKE functions are some of the features available in Host Mode.

Table 8: Control and Operational Mode Selection for LXT359 Transceiver

Input to Pin[1]		Mode of Operation						
Mode	**TRSTE**	**Hardware**	**Software**	**Unipolar**	**Bipolar**	**AMI Encoder Decoder**	**B8ZS Encoder Decoder**	**All Outputs Tristated**
Low	Low	On	Off	Off	On	Off[3]	Off	No
Low	High	On	Off	Off	On	Off[3]	Off	Yes
Low	Open	On	Off	On	Off	On	Off	No
High[2]	Low	Off	On	x	x	x	x	No
High[2]	High	Off	On	x	x	x	x	Yes
High[2]	Open	Off	On	x	x	x	x	No
Open	Low	On	Off	On	Off	Off	On	No
Open	High	On	Off	On	Off	Off	On	Yes
Open	Open	On	Off	On	Off	Off	On	No

1. Open is either a midrange voltage or the pin is floating.
2. In Software Mode, the contents of register CR1 determine the operation mode.
3. Encoding is done externally.

Host Mode Operation

The LXT359 operates in Host Mode when MODE is set High. In Host Mode a microprocessor accesses and controls the transceiver through a data port using the internal registers. The outputs (RPOS/RNEG or RDATA) are valid on the rising edge of RCLK.

The host processor/controller can completely configure the device as well as get a full diagnostic/status report through the SIO or PIO. Only the clocks and data for Bipolar Mode and BPV/Logic Error insertions for Unipolar need to be provided directly to the input pins. Similarly, the recovered clock, data, and BPV are available only at output pins. All other mode settings and diagnostic information are available through the data port.

Table 9 shows the address used by the SIO to access each register on the LXT359. Table 10 summarizes the control and status registers and labels each bit they contain. Tables 11 through 15 identify the bits in each register.

Table 9: Serial Port Register Addresses

Register		Address[1]
Name	Abbr	Serial Port (A7-A1)
Control #1	CR1	x010000
Control #2	CR2	x010001
Interrupt Clear	ICR	x010011
Transition Status	TSR	x010100
Performance Status	PSR	x010101
Equalizer Status	ESR	x010110

Table 10: Register Addresses and Bit Names

Register		Type	Bit							
Name			7	6	5	4	3	2	1	0
Control #1	CR1	R/W	JASEL1	JASEL0	ENCEB	UNIENB	EC4	EC3	EC2	EC1
Control #2	CR2	R/W	RESET	EPAT1	EPAT0	ETAOS	ENLOOP	EALOOP	ELLOOP	ERLOOP
Interrupt Clear	ICR	R/W	*reserved*[1]	*reserved*[1]	*reserved*[1]	reserved[1]	*reserved*[1]	*reserved*[1]	CNLOOP	CLOS
Transition Status	TSR	R	ESUNF	ESOVR	*reserved*[1]	reserved[1]	*reserved*[1]	TAIS	TNLOOP	TLOS
Performance Status	PSR	R	reserved[1]	*reserved*[1]	*reserved*[1]	reserved[1]	*reserved*[1]	AIS	NLOOP	LOS
Equalizer Status	ESR	R	LAIN7	LAIN6	LAIN5	LAIN4	*reserved*[2]	*reserved*[1]	*reserved*[1]	*reserved*[1]

1. In write registers, bits labeled *reserved* should be set to 0 (except as in note 3 below) for normal operation and ignored in read only registers.

Table 11: Control Register #1 *Read/Write, Address (A7-A1) = x010000*

Bit	Name	Function	Jitter Attenuation		
			JASEL0	JASEL1	Position
0	EC1	Set the Equalizer Control codes (see Table 6).	1	0	Transmit
1	EC2		1	1	Receive
2	EC3		0	X	disabled
3	EC4				
4	UNIENB	Enables Unipolar I/O Mode and insertion/detection of BPVs.			
5	ENCENB	Enables B8ZS encoders/decoders; device enters Unipolar Mode and pins 3, 4, 6 and 7 change to their unipolar functions.			
6	JASEL0	Jitter Attenuation Mode, selects jitter attenuation circuitry position in data path or disables it. See right hand section of table for values. ↗			
7	JASEL1				

Table 12: Control Register #2 *Read/Write, Address (A7-A1) = x010001*

Bit	Name	Function	Pattern		
			EPAT0	EPAT1	Selected
0	ERLOOP[1]	Enables Remote Loopback (RLOOP)	0	0	Transmit TPOS/TNEG
1	ELLOOP[1]	Enables Local Loopback (LLOOP)			
2	EALOOP	Enables Analog Loopback (ALOOP)	1	0	In-band Loop Up Code 00001
3	ENLOOP	Enables Network Loopback Detection (NLOOP)	1	1	In-band Loop Down Code 001
4	ETAOS	Enables Transmit All Ones (TAOS)			
5	EPAT0	Enables loop code transmission. See right hand section of table for values. ↗			
6	EPAT1				
7	RESET	RESET = 1 resets device state and all registers.			

1. To enable Dual Loopback (DLOOP), set both ERLOOP = 1, ELLOOP = 1.

Table 13: Interrupt Clear Register *Read/Write, Address (A7-A1) = x010011*

Bit	Name	Function[1]
0	CLOS	Clears/Masks LOS Interrupt.
1	CNLOOP	Clears/Masks NLOOP Interrupt.
2	—	*reserved-ignore.*
3	—	*reserved-ignore.*
4	—	*reserved-ignore.*
5	—	*reserved-ignore.*
6	—	*reserved-ignore.*
7	—	*reserved-ignore.*

1. Leaving a 1 of in any of these bits masks the associated interrupt.

Table 14: Transition Status Register *Read Only, Address (A7-A1) = x010100*

Bit	Name	Function
0	TLOS	Loss of Signal (LOS) has changed since last clear LOS interrupt occurred.
1	TNLOOP	NLOOP has changed since last clear NLOOP interrupt occurred.
2	—	*reserved-ignore.*
3	—	*reserved-ignore.*
4	—	*reserved-ignore.*
5	—	*reserved-ignore.*
6	—	*reserved-ignore.*
7	—	*reserved-ignore.*

Table 15: Performance Status Register *Read Only, Address (A7-A1) = x010101*

Bit	Name	Function
0	LOS	Loss of Signal (LOS) Status.
1	NLOOP	Network Loop (NLOOP) Status.
2	AIS	Alarm Indicator Status.
3	—	*reserved-ignore.*
4	—	*reserved-ignore.*
5	—	*reserved-ignore.*
6	—	*reserved-ignore.*
7	—	*reserved–ignore.*

Table 16: Equalizer Status Register *Read Only, Address (A7-A1) = x010110*

Bit	Name	Function
0	—	*reserved–ignore* (Least Significant Bit).
1	—	*reserved–ignore.*
2	—	*reserved–ignore.*
3	—	*reserved–ignore.*
4	LATN4	Receive Line Attenuation Indicators. Convert this binary output to a decimal number and multiply by 2.9 dB to determine the approximate cable attenuation as seen by the receiver. For instance, if LATN7-4 = 1010_{BIN} (= 10_{DEC}), then the receiver is seeing a signal attenuated by approximately 29 dB (2.9 dB x 10) of cable.
5	LATN5	
6	LATN6	
7	LATN7	

Serial Port Operation

The LXT359 operates in Host Mode when the MODE pin is set High. Figure 9 shows the SIO data structure. The registers are accessible through a 16-bit word: an 8-bit Command/Address byte (bits R/$\overline{W}$ and A1-A7) and a subsequent 8-bit data byte (bits D0-7). Bit R/$\overline{W}$ determines whether a read or a write operation occurs. Bits A6-1 in the Command/Address byte address specific registers (the address decoder ignores bit A7). The data byte depends on both the value of bit R/$\overline{W}$ and the address of the register as set in the Command/Address byte.

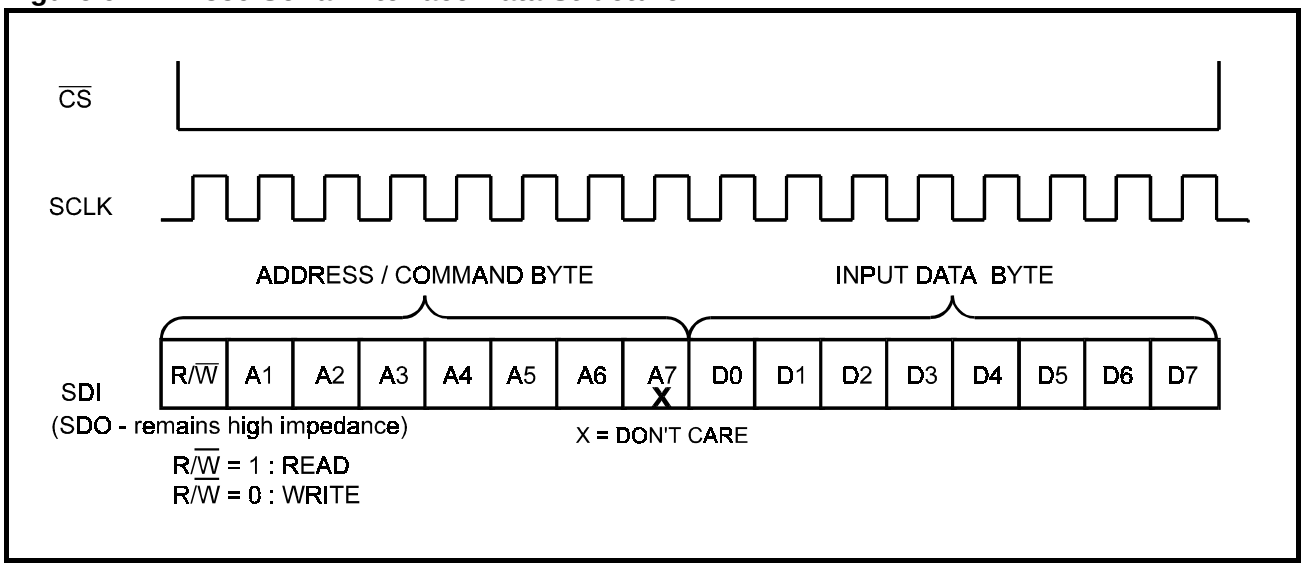
Host Mode provides a latched interrupt output ($\overline{INT}$). A change in the state of any of the following bits in the Performance Status Register will drive $\overline{INT}$ Low: LOS or NLOOP. An interrupt will also occur when there is an elastic store overflow or underflow. When the interrupt has occurred, the $\overline{INT}$ output pin is pulled Low. The output stage of each $\overline{INT}$ pin consists only of a pull-down device, so each one requires an external pull-up resistor. The interrupt is cleared when the interrupt condition no longer exists, and the host processor writes a 1 to the respective interrupt causing bit(s) in the Interrupt Register. Leaving a 1 in any of these interrupt status bits masks that interrupt.

Host Mode also allows control of the serial data and receive data output timing. The clock edge (CLKE) signal determines when the outputs are valid, relative to the Serial Clock (SCLK) or RCLK as shown in Table 17.

Table 17: CLKE Settings

CLKE	Output	Clock	Valid Edge
Low	RPOS	RCLK	Rising
	RNEG	RCLK	Rising
	SDO	SCLK	Falling
High	RPOS	RCLK	Falling
	RNEG	RCLK	Falling
	SDO	SCLK	Rising

Figure 9: LXT359 Serial Interface Data Structure



APPLICATION INFORMATION

Table 18: Recommended Transformers for LXT359

Tx/Rx	Turns Ratio	Part Number	Manufacturer
Tx	1:2	PE-65351	Pulse Engineering
		PE-65771	
		0553-5006-IC	Bell-Fuse
		66Z-1308	Fil-Mag
		671-5832	Midcom
		67127370	Schott Corp
		67130850	
		TD61-1205D	HALO (combination Tx/Rx set)
		TG26-1205NI	HALO (surface mount dual transformer 1CT:2CT & 1CT:2CT)
		TG48-1205NI	HALO (surface mount dual transformer 1CT:2CT & 1:1)
		16Z5946	Vitec
Rx	1:1	FE 8006-155	Fil-Mag
		671-5792	Midcom
		PE-64936	Pulse Engineering
		PE-65778	
		67130840	Schott Corp
		67109510	
		TD61-1205D	HALO (combination Tx/Rx set)
		16Z5936	Vitec
		16Z5934	

Figure 10: Typical T1 LXT359 Hardware Mode Application

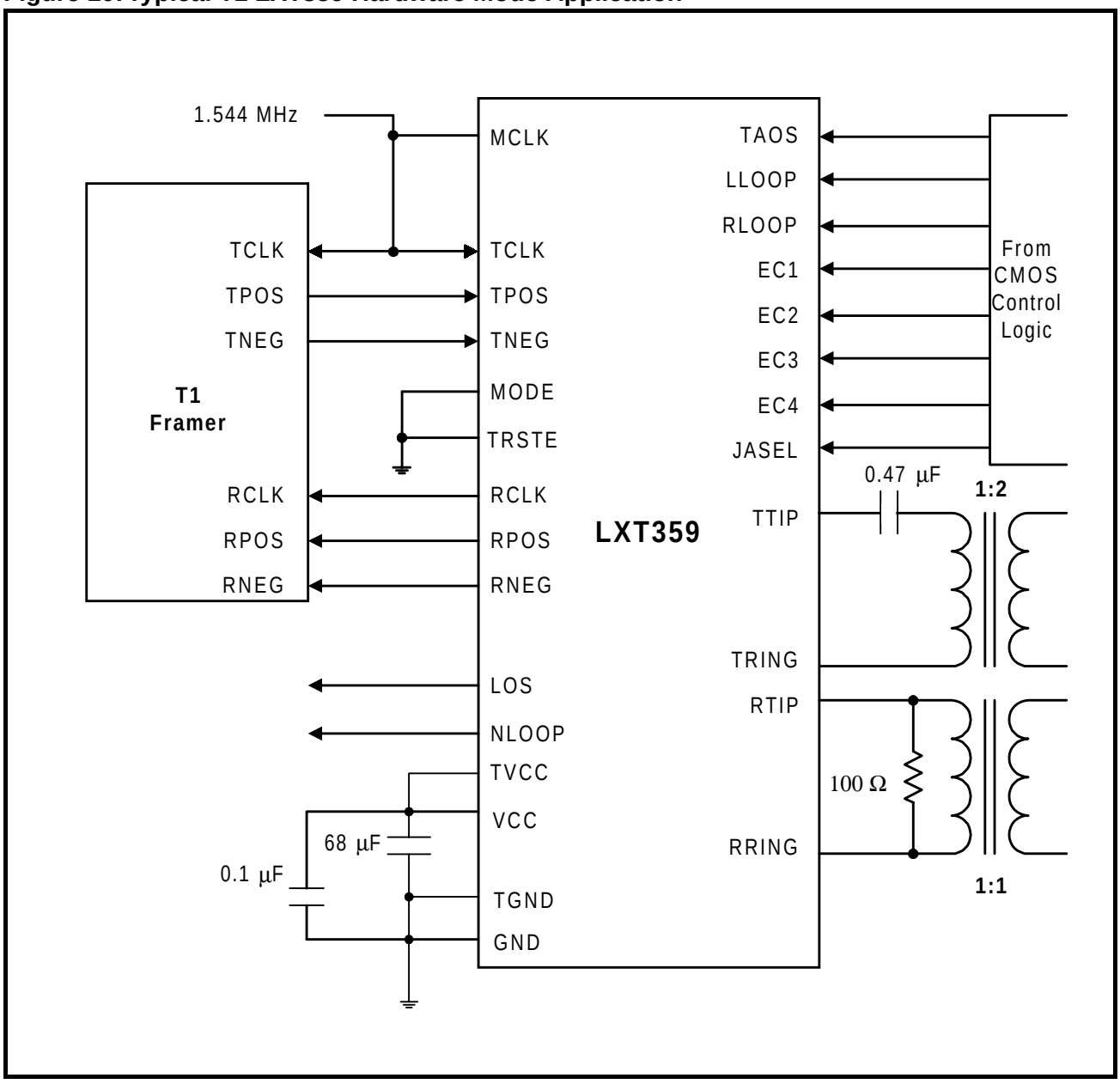
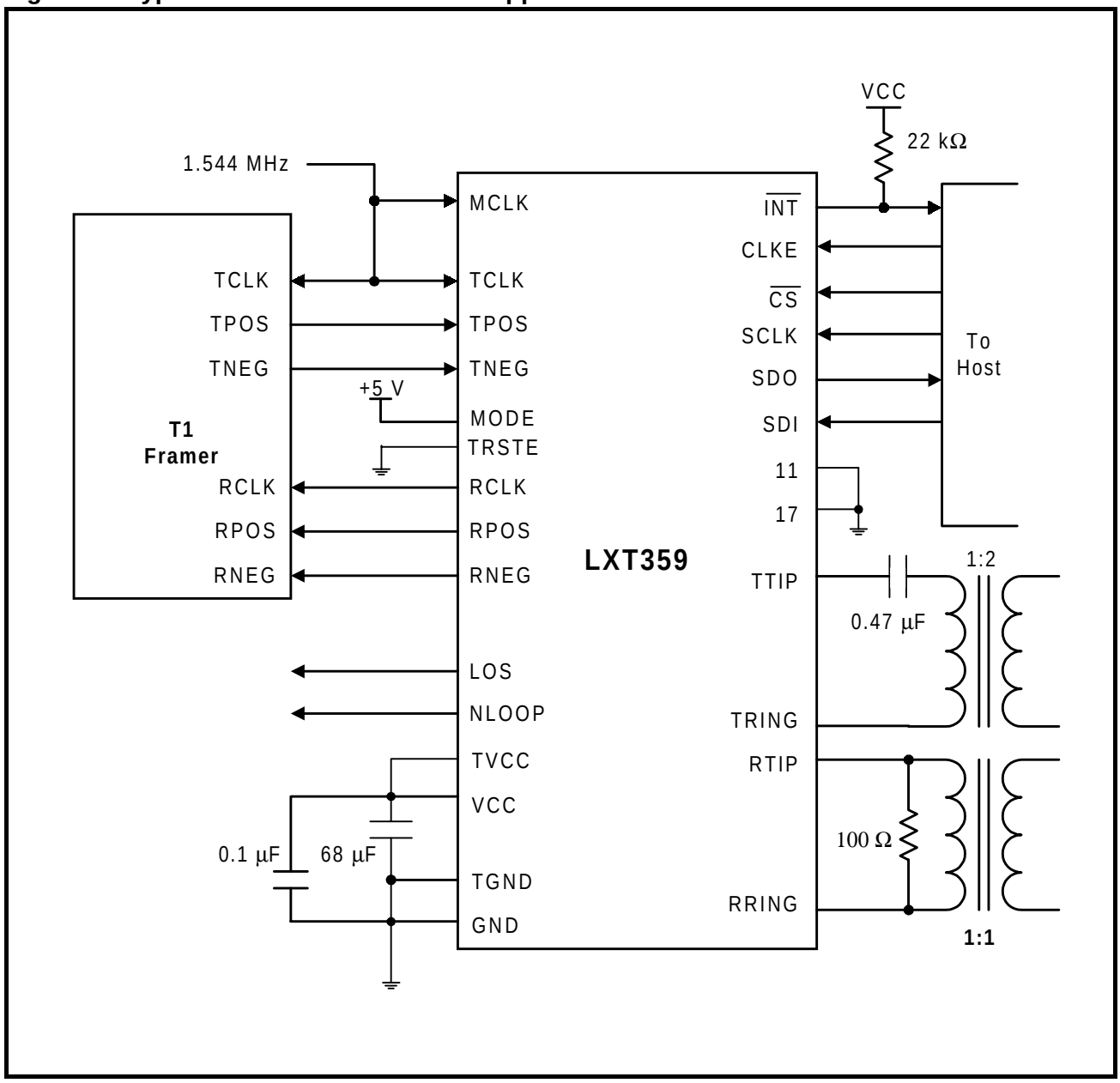


Figure 11: Typical T1 LXT359 Host Mode Application



TEST SPECIFICATIONS

NOTE

The minimum and maximum values in Tables 19 to 25 and Figures 12 through 18 represent the performance specifications of the LXT359 and are guaranteed by test, except where noted by design.

Table 19: Absolute Maximum Ratings

Parameter	Sym	Min	Max	Units
DC supply (reference to GND)	V_{CC}, TV_{CC}	–	6.0	V
Input voltage, any pin [1]	V_{IN}	GND -0.3 V	V_{CC} + 0.3 V	V
Input current, any pin [2]	I_{IN}	- 10	10	mA
Storage Temperature	T_{STG}	-65	150	° C

CAUTION

Operation at these limits may permanently damage the device.
Normal operation at these extremes is not guaranteed.

1. TVCC and VCC must not differ by more than 0.3 V during operation. TGND and GND must not differ by more than 0.3 V during operation.
2. Transient currents of up to 100 mA will not cause SCR latch-up. TTIP, TRING, TVCC, and TGND can withstand continuous currents of up to 100 mA.

Table 20: Operating Conditions/Characteristics

Parameter			Sym	Min	Typ[1]	Max	Units	Test Conditions
DC Supply [2]			V_{CC}, TV_{CC}	4.75	5.0	5.25	V	
Ambient Operating Temperature			T_A	-40	–	85	° C	
Total Power Dissipation[3]	T1	Short Haul/ D4	P_D	–	435	575	mW	100% mark density
		Long Haul	P_D	–	325	425	mW	100% mark density

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. TVCC and VCC must not differ by more than 0.3 V.
3. Power dissipation while driving 25 Ω load over operating range for T1 operation. Includes power dissipation on device and load. Digital levels are within 10% of the supply rails and digital outputs driving a 50 pF capacity load.

Table 21: LXT359 Digital Characteristics *(Ta = -40 to 85 °C, V+ = 5.0 V ± 5%, GND = 0 V)*

Parameter		Sym	Min	Typ	Max	Units	Test Conditions
High level input voltage [1,2] (pins 1-4, 17, 23-25)[4]		V_{IH}	2.0	–	–	V	
Low level input voltage [1,2] (pins 1-4, 17, 23-25)[4]		V_{IL}	–	–	0.8	V	
High level output voltage [1,2] (pins 6-8, 10, 12, 23, 25)[4]		V_{OH}	2.4	–	–	V	I_{OUT} = 400 µA
Low level output voltage [1,2] (pins 6-8, 10, 12, 23, 25)[4]		V_{OL}	–	–	0.4	V	I_{OUT} = 1.6 mA
High level input voltage [3] (pins 5, 9, 11, 26-28)[4]		V_{IH}	3.5	–	–	V	
Midrange input voltage [3] (pins 5, 9, 11, 26-28)[4]		V_{IM}	2.3	–	2.7	V	
Low level input voltage [3] (pins 5, 9, 11, 26-28)[4]	Host Mode	V_{IL}	–	–	0.8	V	
	H/W Mode	V_{IL}	–	–	1.5	V	
Input leakage current		I_{LL}	0	–	±50	µA	
Three-state leakage current [1] (all outputs)		I_{3L}	0	–	±10	µA	
TTIP/TRING leakage current (pins 13, 16)[4]		I_{TR}	–	–	±1.2	mA	in Idle and Power Down
AMI output pulse amplitude		–	2.4	3.0	3.6	V	R_L = 100 Ω
D4 output pulse amplitude		–	–	6.0	–	V	

1. Functionality of pin 23 and 25 depends on mode. See Host Mode and Hardware Mode description.
2. Output drivers will output CMOS logic levels into CMOS loads.
3. As an alternative to supplying 2.3 - 2.7 V to these pins, they may be left open.
4. Referenced pin numbers are for the PE package only. Refer to Figure 1 for corresponding QE or LE package pin numbers.

Figure 12: 1.544 MHz T1 Pulse (DS1 and DSX-1) *(See Table 22)*

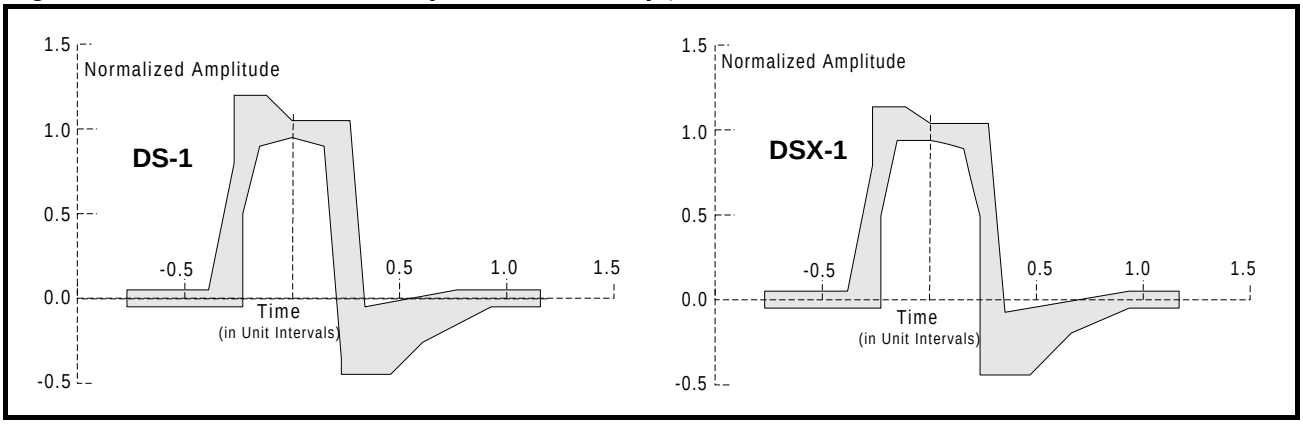


Table 22: 1.544 MHz T1 Pulse Mask Corner Point Specifications

DS1 Template *(per ANSI T1. 403-1995)*				**DSX-1 Template** *(per ANSI T1. 102-1993)*			
Minimum Curve		**Maximum Curve**		**Minimum Curve**		**Maximum Curve**	
Time *(UI)*	**Amplitude**	**Time** *(UI)*	**Amplitude**	**Time** *(UI)*	**Amplitude**	**Time** *(UI)*	**Amplitude**
-0.77	-0.05	-0.77	0.05	-0.77	-0.05	-0.77	0.05
-0.23	-0.05	-0.39	0.05	-0.23	-0.05	-0.39	0.05
-0.23	0.50	-0.27	0.80	-0.23	0.50	-0.27	0.80
-0.15	0.90	-0.27	1.20	-0.15	0.95	-0.27	1.15
0.0	0.95	-0.12	1.20	0.0	0.95	-0.12	1.15
0.15	0.90	0.0	1.05	0.15	0.90	0.0	1.05
0.23	0.50	0.27	1.05	0.23	0.50	0.27	1.05
0.23	-0.45	0.34	-0.05	0.23	-0.45	0.35	-0.07
0.46	-0.45	0.77	0.05	0.46	-0.45	0.93	0.05
0.61	-0.26	1.16	0.05	0.66	-0.20	1.16	0.05
0.93	-0.05	–	–	0.93	-0.05	–	–
1.16	-0.05	–	–	1.16	-0.05	–	–

Table 23: Master and Transmit Clock Timing Characteristics *(Figure 13)*

Parameter	Sym	Min	Typ[1]	Max	Units	Notes
Master clock frequency	MCLK	–	1.544	–	MHz	must be supplied
Master clock tolerance	MCLKt	–	±50	–	ppm	
Master clock duty cycle	MCLKd	40	–	60	%	
Transmit clock frequency	TCLK	–	1.544	–	MHz	
Transmit clock tolerance	TCLKt	–	–	±100	ppm	
Transmit clock duty cycle	TCLKd	10	–	90	%	
TPOS/TNEG to TCLK setup time	t_{SUT}	50	–	–	ns	
TCLK to TPOS/TNEG hold time	t_{HT}	50	–	–	ns	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 13: Transmit Clock Timing

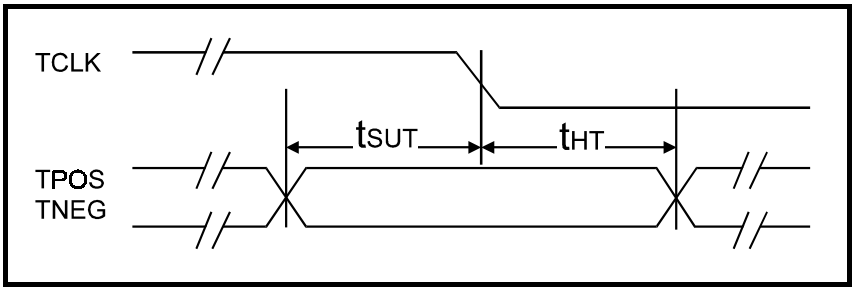


Table 24: Receive Timing Characteristics for *(See Figure 14)*

Parameter	Sym	Min	Typ[1]	Max	Units
Receive clock duty cycle [2, 3]	RLCKd	40	50	60	%
Receive clock pulse width [2, 3]	tPW	–	648	–	ns
Receive clock pulse width high	tPWH	–	324	–	ns
Receive clock pulse width low[1,3]	tPWL	260	324	388	ns
RPOS/RNEG to RCLK rising time	tSUR	–	274	–	ns
RCLK rising to RPOS/RNEG hold time	tHR	–	274	–	ns

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. RCLK duty cycle widths will vary according to extent of received pulse jitter displacement. Max and Min RCLK duty cycles are for worst case jitter conditions.
3. Worst case conditions guaranteed by design only.

Figure 14: Receive Clock Timing

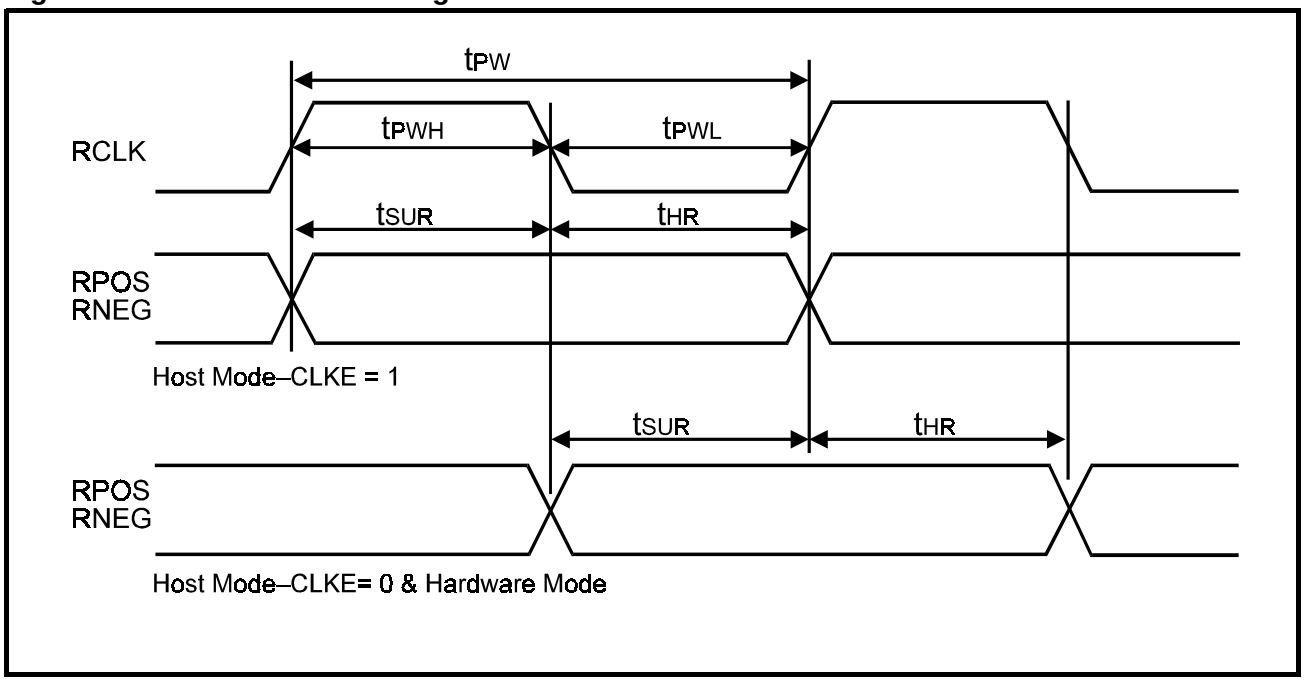


Table 25: LXT359 Serial I/O Timing Characteristics *(See Figures 15 and 16)*

Parameter	Sym	Min	Typ[1]	Max	Units	Parameter
Rise/fall time—any digital output	tRF	–	–	100	ns	Load 1.6 mA, 50 pF
SDI to SCLK setup time	tDC	50	–	–	ns	
SCLK to SDI hold time	tCDH	50	–	–	ns	
SCLK low time	tCL	240	–	–	ns	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 25: LXT359 Serial I/O Timing Characteristics *(See Figures 15 and 16)* – continued

Parameter	Sym	Min	Typ[1]	Max	Units	Parameter
SCLK high time	tCH	240	–	–	ns	
SCLK rise and fall time	tR, tF	–	–	50	ns	
$\overline{CS}$ falling edge to SCLK rising edge	tCC	50	–	–	ns	
Last SCLK edge to $\overline{CS}$ rising edge	tCCH	50	–	–	ns	
$\overline{CS}$ inactive time	tCWH	250	–	–	ns	
SCLK to SDO valid time	tCDV	–	–	200	ns	
SCLK falling edge or $\overline{CS}$ rising edge to SDO high-Z	tCDZ	–	100	–	ns	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 15: LXT359 Serial Data Input Timing Diagram

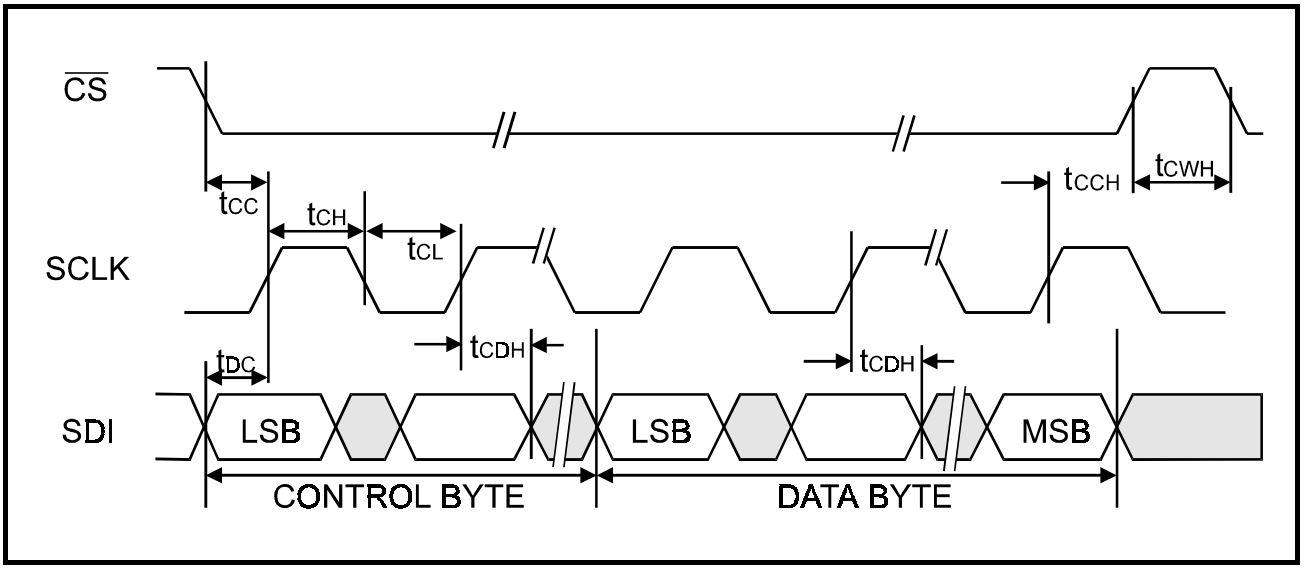


Figure 16: LXT359 Serial Data Output Timing Diagram

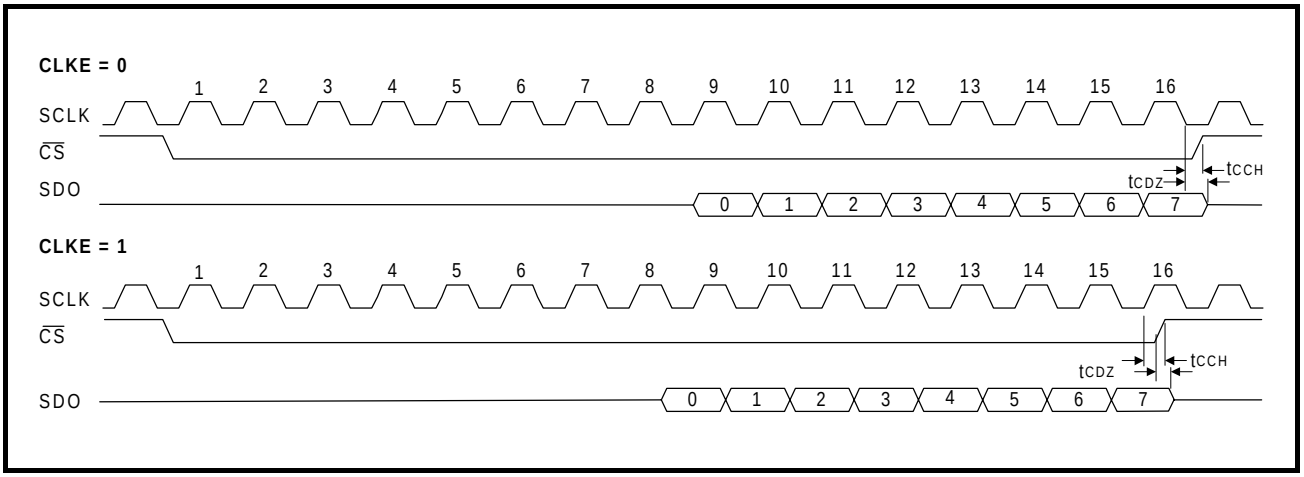


Figure 17: Jitter Tolerance *(Typical)*

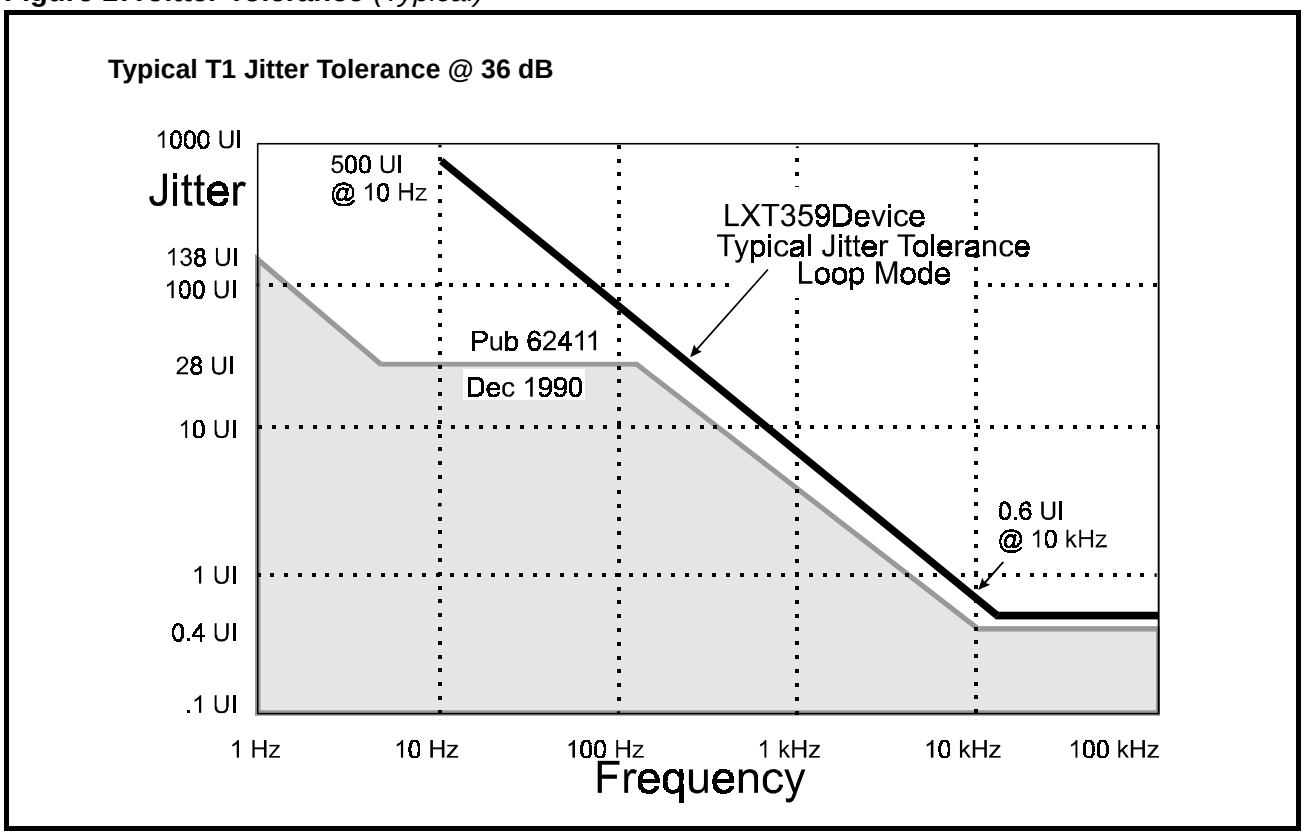
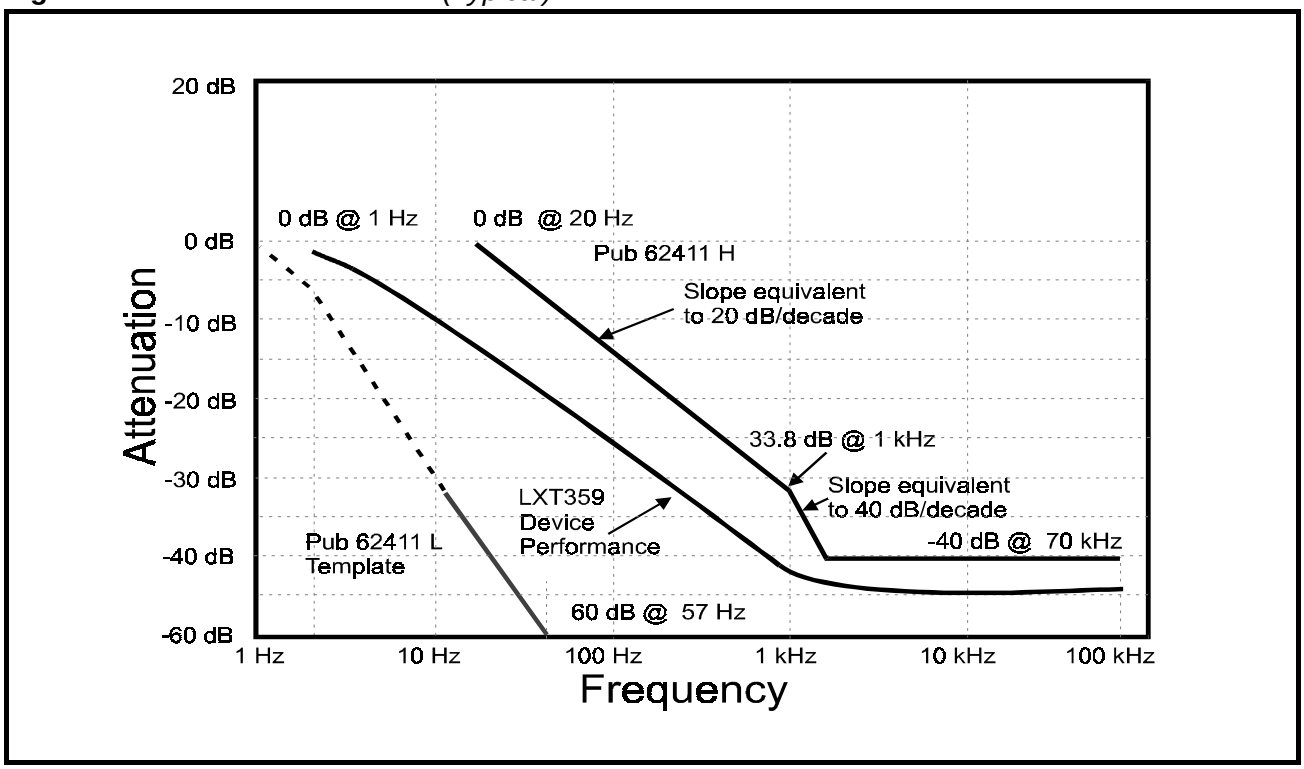


Figure 18: T1 Jitter Attenuation *(Typical)*

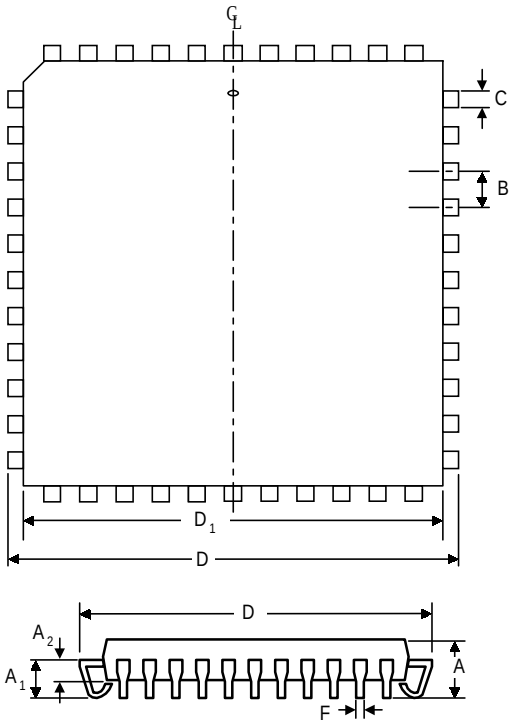


MECHANICAL SPECIFICATIONS

Figure 19: Plastic Leaded Chip Carrier Specifications

28-Pin PLCC

- Part Number LXT359PE
- Extended Temperature Range (-40 °C to 85 °C)



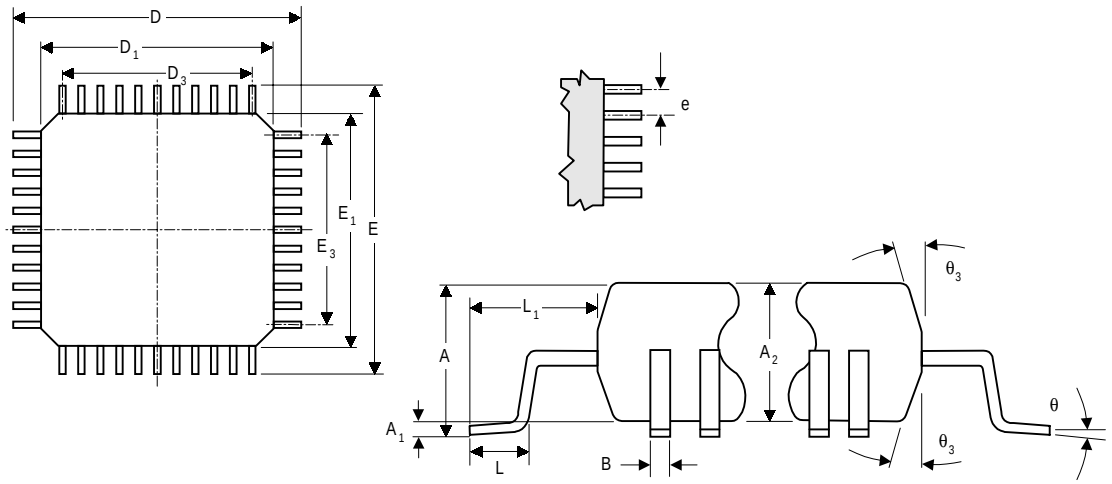
Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	0.165	0.180	4.191	4.572
A1	0.090	0.120	2.286	3.048
A2	0.062	0.083	1.575	2.108
B	.050 BSC[1] (nominal)		1.27 BSC[1] (nominal)	
C	0.026	0.032	0.660	0.813
D	0.485	0.495	12.319	12.573
D1	0.450	0.456	11.430	11.582
F	0.013	0.021	0.330	0.533

1. BSC—Basic Spacing between Centers

Figure 20: Plastic Quad Flat Pack Specifications

44-Pin PQFP

- Part Number LXT359QE
- Extended Temperature Range (-40 °C to 85 °C)



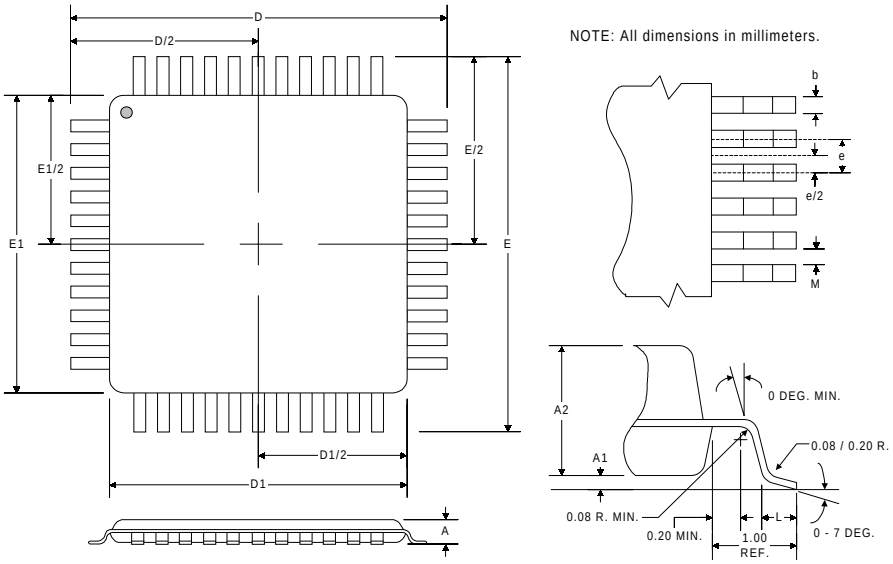
Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	–	0.096	–	2.45
A1	0.010	–	0.25	–
A2	0.077	0.083	1.95	2.10
B	0.012	0.018	0.30	0.45
D	0.510	0.530	12.95	13.45
D1	0.390	0.398	9.90	10.10
D3	0.315 BSC[1] (nominal)		8.00 BSC[1] (nominal)	
E	0.510	0.530	12.95	13.45
E1	0.390	0.398	9.90	10.10
E3	0.315 BSC[1] (nominal)		8.00 BSC[1] (nominal)	
e	0.031 BSC[1] (nominal)		0.80 BSC[1] (nominal)	
L	0.029	0.041	0.73	1.03
L1	0.063 BSC[1] (nominal)		1.60 BSC[1] (nominal)	
θ3	5°	16°	5°	16°
θ	0°	7°	0°	7°

1. BSC—Basic Spacing between Centers

Figure 21: Low Profile Quad Flat Package Specifications

44-Pin LQFP

- Part Number LXT359LE
- Extended Temperature Range (-40 °C to 85 °C)



Dimension[1]	Millimeters		
	Minimum	Nominal	Maximum
A	-	-	1.60
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
D	12.00 (basic spacing between centers)		
D1	10.00 (basic spacing between centers)		
E	12.00 (basic spacing between centers)		
E1	10.00 (basic spacing between centers)		
e	0.80 (basic spacing between centers)		
L	0.45	0.60	0.75
M	0.15	-	-

1. See JEDEC Publication for additional specifications.

NOTES

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