Data Sheet

VSC9182

64x64 STS-12/STM-4 TSI Switch Fabric

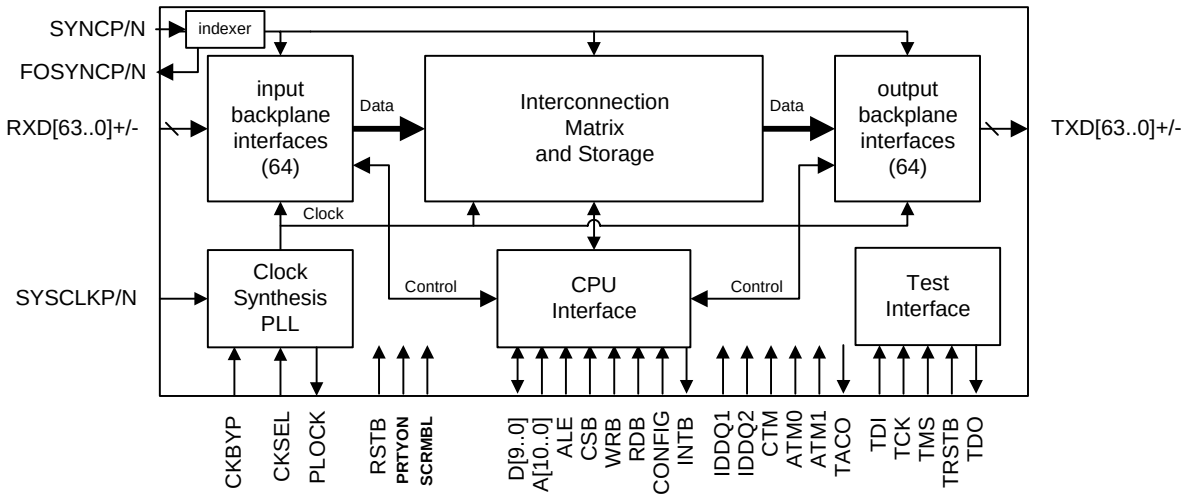
Features

- 64x64 STS-12/STM-4 TSI Switch with Non-blocking 768x768 STS-1 Switch Matrix
- Supports Both Multicast and Broadcast
- Serial LVDS 622Mb/s High-Speed Interface with PECL/CML Compatibility and Retiming
- 50MHz 11-Bit Microprocessor Interface
- IEEE P1149.1 Test Access Port
- Compatible with VSC918x Pointer Processors
- Integrated Clock Synthesis with a Choice of Two Reference Frequencies
- AIS and Unequipped Signal Insertion
- LOS Detection, Input Parity Checking and Output Parity Insertion; Scrambling and Descrambling
- Hitless Reconfiguration of TSI Mapping
- Single +3.3V Power Supply
- Compliant with Relevelant SONET/SDH Requirements as Stated in ANSI T1.105, Bellcore GR-253-CORE and ITU-T G.707
- Thermally-Enhanced 37.5mm 480 BGA Package

General Description

The VSC9182 is a 64x64 STS-12/STM-4 Time Slot Interchange Switch IC for Cross Connection and Ring Protection Switching of STS(n) tributaries. All STS-12/STM-4 inputs and outputs are differential serial signals running at 622.08Mb/s for efficiency in switch card and system backplane design. Using the STS-192/STM-64 Pointer Processor and Frame Aligner IC (VSC9186) and four VSC9182 devices in parallel, a 16x16 STS-192/STM-64 switch can be constructed.

Block Diagram



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Features Summary

Interconnection Matrix

- Time & Space Switches any STS-(n) [n= 1, 3c, 12c] signal of an incoming STS-12 into any byte position of any STS-12 output
- Single Stage non-blocking structure of the switch allows for Multicast and Full Broadcast
- Hitless Switching: programming is queued and takes effect after user intervention during the next frame boundary
- Unequipped or AIS signals can be substituted into any of the outgoing STS-1 time slots.
- Provides a capability to read out the switch configuration (address map)

Input Backplane Interface

- Serial 622.08Mb/s differential LVDS STS-12/STM-4 inputs
- Receives 64 serial 622.08Mb/s STS-12/STM-4 line channels (these 64 input signals are presumed frequency synchronous and frame aligned to within +/- 3 time slots of the system SYNC input)
- Provides on-chip data recovery deskewing functionality to bit-align, byte-align and frame-align all incoming STS-12s (within the above tolerance) to the local clock
- Flags Out-of-Frame (OOF), Loss-of-Signal (LOS) and parity errors
- Checks byte-interleaved parity of incoming data versus B1 byte of following frame
- Inserts unequipped or AIS when channel is in OOF, LOS or unprovisioned state and inhibits alarms
- Optionally descrambles SONET-scrambled incoming data

Output Backplane Interface

- Serial 622.08Mb/s differential LVDS STS-12/STM-4 outputs
- Optionally inserts byte-interleaved parity into B1 byte of following frame
- Optionally SONET scrambles outgoing data
- Optionally inserts AIS or unequipped on a per-channel, per-time-slot basis

CPU Interface

- Generic microprocessor (CPU) interface used for device configuration and status checking
- 10-bit data bus and 11-bit address bus
- Interrupt output pin to signal status changes of internal alarms

Test Interface

- IEEE P1149.1 test access port controls external boundary scan

Clock Synthesis PLL

- Monolithic PLL clock multiplier with 8x and 32x multiplication ratios available

Functional Description

Interconnection and Programming

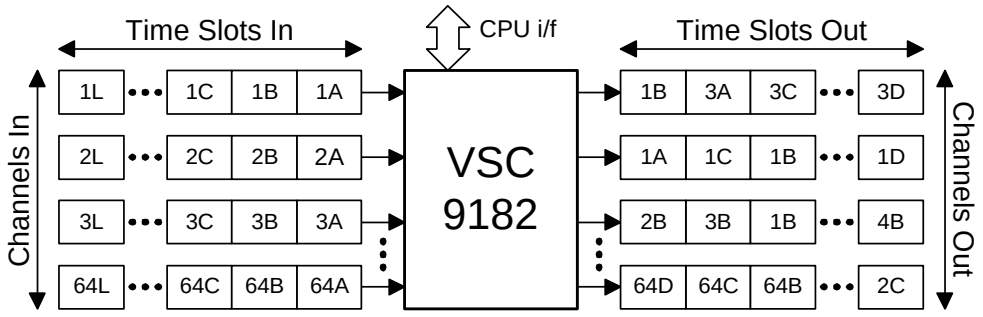
Rearrangement in time (across time-slots) and space (across physical channels) is performed by filling the program memory for each time-slot in each output channel with the address of the input channel and time slot from which it will take its data (see *Internal Register Address Map*). There are 64 channels with 12 time-slots each, for 768 possible input or output addresses. There are no restrictions on the input selected by each output. Each output time slot may also be filled with a AIS or UNEQ signal by programming the low order D[3:0] bits to select an internally generated bit sequence.

Programming is performed via the CPU interface port by presenting the output channel and time-slot address on A[10:0], the input channel and time slot address on D[9:0] and pulsing WRB. A rising edge on WRB transfers the program information to a first layer register in the program memory. The programming does not take effect until the CONFIG pin is asserted and the next frame boundary is received (signaled by the SYNC input). The switch may be programmed continuously but the new map will not take effect until the user asserts the CONFIG signal. The new switch configuration is loaded and implemented within the A1/A2 boundary of the incoming STS-12s. Since this occurs during the period where all the data contains the identical framing bytes, no data is lost and the switching is “hitless.” The current address map may be read back by presenting the Output channel and time-slot address on A[10:0], releasing the D[9:0] signals and lowering RDB, causing the contents of the register to appear at D[9:0].

Note that a CONFIG signal can be generated by a rising edge on CONFIG or by writing a value ‘1’ to the SOFTCONFIG register (A[10:0] = 7FF’h). The input pin CONFIG is logically OR’ed internally with a pulse generator initiated by the SOFTCONFIG register.

The switch matrix reconfiguration effects of the CONFIG signal can be delayed by up to 15 frames. The contents of the DELAY register determine the number of frames to be transmitted after receiving the CONFIG signal before reconfiguring the switch matrix.

Functional Diagram



Clock Synthesis

The monolithic on-chip Phase Lock Loop (PLL) synthesizes the internal 622MHz clock from the reference provided on SYSCLK. The CLKSEL pin selects a multiplication ratio of 8 or 32, allowing a 78MHz or 19MHz reference to be used. The PLOCK pin provides an indication that the PLL is locked for test purposes. This pin may be sampled by the user to confirm that the PLL has locked after some period of time. The CKBYP pin puts the chip into vector test mode when high, passing SYSCLK to the internal clock instead of the synthesized clock.

Synchronization

The on-board frame alignment logic uses the SYNC input to provide indication of the framing boundary. The synchronization block uses an over-sampling technique to find and use an optimal sampling relationship between the internal clock and SYNC.

Once SYNC has been located, the frame indexing logic will assume that all the incoming serial data streams contain framing boundaries that start within +/- 3 byte times (38.4ns) of the rising edge of SYNC. The framing boundary is defined as the transition between the payload of frame N-1 and the A1 byte stream of frame N. The SYNC pulse may be any length shorter than a SONET frame and greater than approximately one byte period (11ns). Re-applying SYNC before a complete frame has elapsed will force re-synchronization.

The relative position of the SYNC input to the RXD[63:0] inputs can be shifted by setting an offset value in the configuration registers. The default position is to expect the SYNC input to be aligned to the frame boundary, but this may be shifted by setting the contents of the SYNC_OFFSET registers. The expected position of the SYNC input can be shifted along the full length of the incoming frame with channel level granularity by computing the appropriate fine and coarse values of SYNC_OFFSET.

The SYNC circuitry operates using a ‘flywheel’ timing where a single SYNC pulse resets the internal counters, and additional pulses are not necessary. A periodic SYNC pulse will be generated internally using the last transition on the SYNC input. Therefore, the user can provide a single SYNC pulse when reframe is necessary or may provide a 125µs periodic pulse. If a periodic SYNC pulse is established, the rising edge of SYNC cannot vary by more than +/-6.4ns.

Input Data Alignment

The input serial data must be synchronous to a multiple of SYSCLK, but can have an unknown phase relationship to the internal 622MHz clock. Bit alignment is performed on each input channel to find an optimal sampling instant to recover the data. The inputs are demultiplexed and placed in an elastic store, and read out some time later synchronous to the master on-chip byte clock.

Data phase may drift during normal operation. The inputs can tolerate up to +/- 3.0UI (4.8ns) of wander. The alignment circuitry can compensate for wander due to environmental factors, and the user is responsible to provision the aligners in a way appropriate to their system.

Input Framing

At an instant dictated by the on-chip frame indexing circuitry (synchronized to the SYNC signal), the contents of the elastic store are examined for the boundary between the A1 and A2 SONET framing bytes. When three A1 bytes followed by three A2 bytes are found (hexadecimal F6F6F6282828), its position and bit-rotation are recorded to enable read-out of the input data such that all bytes arriving on all channels are aligned. Before the framing pattern is located, any provisioned channel (see ‘provisioning’ below) will have a ‘1’ in its OOF

register. When the framing pattern is located in two consecutive frames, the OOF register will be set to '0.' Once in frame, if the expected 6-byte framing pattern is not found in the appropriate location for four consecutive frames, the OOF register will be set to '1.' The payload of the receive channel will be set to all '1's with an A1/A2 boundary (AIS) during OOF if OOF/LOS-AIS is not disabled via the OOF/LOS register disable bit (see *Register Map*). Outputs that are mapped to this port will receive the AIS signal in the selected time slots.

Output In-Band Signaling

The VSC9182 can send a fixed byte message from its output ports designed to signal an impending configuration change to the port card. The message byte and location of this byte is user programmable.

Asserting the CONFIG pin causes the byte stored in the CHANGE register to be inserted in location CHANGE_LOC for a single frame on all outputs. This insertion takes place before scrambling and B1 calculation, but after TSI switching. Following frames transmit the byte stored in the NORMAL register until another CONFIG signal is received. Note: In-Band Signaling overrides AIS/UNEQ for the selected byte.

Parity Checking and Insertion

System-internal parity checking is available to verify integrity of the serial links to and from the TSI. The first B1 byte (second row, first byte position in the frame) is expected to contain the byte-interleaved parity computed on the previous frame's data (after scrambling, if used). This computation is done on-chip and compared to the B1 byte in the following frame. If a discrepancy is found, the parity error register in that channel is set to '1' and an interrupt is generated if the channel is provisioned. Reading the affected register will reset the parity error register for that frame to '0' and de-assert INTB.

The output backplane interface inserts the byte-interleaved parity computed on the previous frame's data (after switching and scrambling, if used) into the outgoing data at the first B1 position. This feature may be disabled by tying the PRTYON pin low, which will leave the first B1 position in the outgoing data untouched.

Alternatively, parity checking can be enabled or disabled by setting the soft parity control register (see General Configuration Registers). Disabling parity checking requires both the PRTYON pin to be set low and the control register be set to '0.'

All parity detection and generation are in conformance with ANSI T1.105, Bellcore GR-253-CORE and ITU-T G.707 specifications.

Descrambling/Scrambling

When the SCRMBL pin is tied high, SONET descrambling is performed on the incoming data after de-serialization and prior to switching. SCRMBL high also causes SONET scrambling to be performed on the outgoing data after switching and before serialization. The $1 + X^6 + X^7$ polynomial is used for scrambling and descrambling. No scrambling is performed on the first row of overhead bytes (A1, A2, J0), which corresponds to the first 36 bytes in an OC-12 frame. The scrambling sequence is re-started on the first byte of payload following the unscrambled bytes and continues until the start of the next frame.

Alternatively, scrambling can be enabled or disabled by setting the soft scramble control register (see *General Configuration Registers*). Disabling SONET scrambling requires both the SCRMBL pin to be set low and the control register be set to '0.'

All scrambling and descrambling are in conformance with ANSI T1.105, Bellcore GR-253-CORE and ITU-T G.707 specifications.

LOS Alarm

If a provisioned channel experiences 16 or more consecutive bytes with no bit transitions, its LOS register is set to '1.' The channel LOS register will reset to '0' upon the presence of input transitions, and a '0' will be written to that aligner's LOS register. The payload of the receive channel will be set to the AIS code (all '1's except the A1 and A2 bytes) during LOS if OOF/LOS-AIS is not disabled via the OOF/LOS register disable bit (see *Register Map*). Outputs that are mapped to this port will receive the AIS signal in the selected time slots. Note: When the aligner is in standby state the clock to the LOS detector is shut off so it holds its last value.

Provisioned Status/Bit Alignment Control

The provisioning register is used to enable/disable used/unused inputs and control the power status of the alignment circuitry in each channel. Writing a '1' to the LSB-0 of the provisioning register will disable that input, suppress interrupts, and source an unequipped signal. Writing a '1' to the LSB+1 of the provisioning register will hold the aligner in a standby state. Setting and subsequently clearing the LSB+1 can be used to re-initialize the aligner if it fails to re-acquire the input signal after a major interruption of the input. Therefore, the four possible states of the provisioning register are:

Register Value	*Result*
000h	Provisioned, Aligner ON
001h	Unprovisioned, Aligner ON
002h	Provisioned, Aligner STANDBY
003h	Unprovisioned, Aligner STANDBY

An input channel may be marked un-provisioned by writing a '1' to the LSB of its provisioning register. This will disable Parity Error INTB interrupts originating from that input channel. The payload of the receive channel will be set to the unequipped code (all '0's except the A1, A2 and H1 bytes). Outputs that are mapped to this port will receive the all '0's unequipped signal in the selected time slots. Unprovisioned inputs cannot pass traffic, but if the aligners are powered, will align incoming data and update values in the input status registers for OOF, LOS, and parity. This allows a user to determine the health of a new connection before provisioning it.

Provisioned inputs retime the serial input with the system clock and demultiplex its contents to the alignment circuitry. The aligner enables the circuitry that finds the optimum retiming point in the received 622MHz data eye as well as using the SYNC input to detect the presence of the A1/A2 boundary within the +/- 3 byte specification.

Output Data Alignment

All TXD[63:0] outputs are frame aligned and synchronous with the FOSYNC output. There is a pipeline delay through the VSC9182 of approximately 23 byte times (23 x 8/622MHz) +/-2 bit times. FOSYNC is aligned to the start of the STS-12 frame, allowing this signal to be forwarded to a second and third VSC9182 for three layer Clos switching architectures.

Interrupt Servicing

Interrupt sequences are not accompanied by an indication of which input is causing the interrupt, therefore it is necessary to read back all registers in order to determine the location of the fault and reset the interrupt condition. An external CPU should read back the entire status register memory when an interrupt takes place.

INTB toggles low whenever a parity error register toggles high. Reading the changed register causes INTB to return to a logic '1.' Reading a parity error register resets it to '0.' Writing the contents of this register has no effect.

Interrupts can be disabled on a per channel basis. Unprovisioned inputs do not generate interrupts, and the user can mask interrupt generation on a per channel and per alarm basis by writing the aligner register map appropriately. Writing a '1' to the D2 location of a parity status register will prevent INTB from being asserted if there is a change of state.

While OOF and LOS interrupt generation is no longer supported, it does exist. The OOF and LOS Interrupt Masking Status bits should be set to '1' for all provisioned input channels to prevent unwanted INTB events from occurring.

Test Access Port

The test access port provides external boundary scan capability for board-level test. The VSC9182 TAP uses the IEEE 1149.1 standard TAP controller state machine as the interface to external boundary scan. The TAP controller makes state transitions by sampling TMS on the rising edge of TCK. Lowering TRSTB will place the state machine in the initial state (Test-Logic-Reset). The VSC9182 TAP implements the EXTEST, SAMPLE/PRELOAD and BYPASS instructions. The VSC9182 TAP does not implement the optional ID Code function. The instruction register is two bits in length, and the command codes are shown in Table 1. A scan definition file may be obtained by contacting the factory. Please consult the IEEE 1149.1 for additional information on TAP use and implementation.

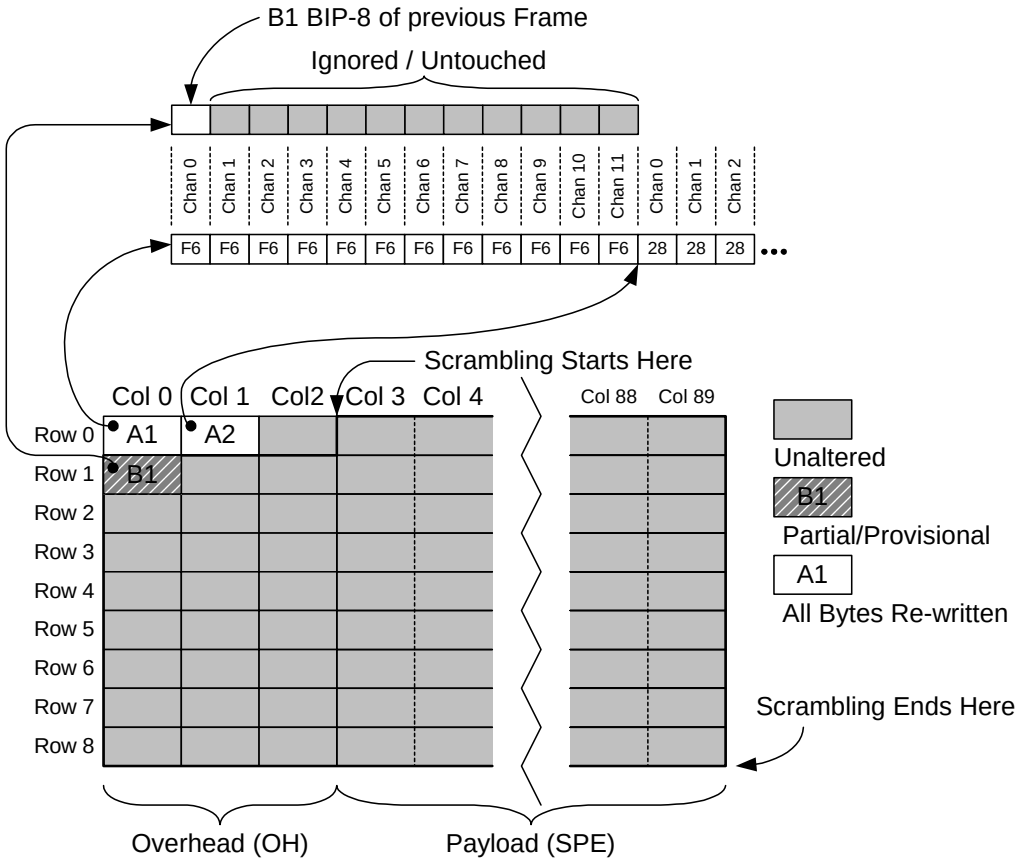
Table 1: TAP Instruction Codes

Instruction Code	*Instruction*
00	EXTEST
01	SAMPLE/PRELOAD
01, 11	BYPASS

Frame Structure

The VSC9182 accepts and produces the STS-12 frame structure shown in Figure 1. Scrambling/descrambling and insertion of B1 are optional, as described previously. A1 and A2 bytes are always overwritten in the outgoing data. Aside from the A1/A2 byte, the VSC9182 will pass the TOH transparently.

Figure 1: STS-12 Frame Structure



Recommended Startup Sequence

The following sequence may be used to initially set up the device starting at power-on:

1. Apply power
2. Apply SYSCLK (and SYNC if available)
3. Bring or Hold RSTB low
4. Wait at least 100µs for PLL to lock (confirm via PLOCK pin or PLOCK register)
5. Bring RSTB high
6. Program the following (in any order):
   SYNC coarse and fine offset (if not using default)
   Soft SCRMBL control (set to '0' if external pin control is used)
   Soft PRTYON control (set to '0' if external pin control is used)
   NORMAL value (if used)
   CHANGE value (if used)
   CHANGE_LOC value (if used)
   Configuration DELAY value (if used)
7. Read back above registers to confirm (if desired)
8. Set the desired Alarm interrupt masks (LOS, OOF, Parity) for all input channels, via their status registers and set whether an LOS or OOF state will generate AIS via the AIS Disable bit in the OOF/LOS register
9. Set the desired provisioning state of each input channel
   It is recommended that all channels be set unprovisioned and all aligners be set in standby on startup.
10. Read all input status registers twice to update current and history bits and confirm masking state
11. Write the initial connection map to all switch configuration registers
12. Apply SYNC if not already applied
13. Raise CONFIG to request reconfiguration
14. Read back all switch configuration registers to confirm reconfiguration (if desired)

Recommended Channel Provisioning Sequence

If the recommendation in item 9 above is followed, the following can be used to locate all active data channels on startup:

1. Set all aligners active, leaving all input channels unprovisioned
2. Wait two full frames (250µs)
3. For each input channel:
   a) Read LOS alarm status; if Current status is high, move to next channel
   b) Read OOF alarm status; if Current status is high, move to next channel
   c) If neither alarm was high, provision channel

Package Pin Descriptions

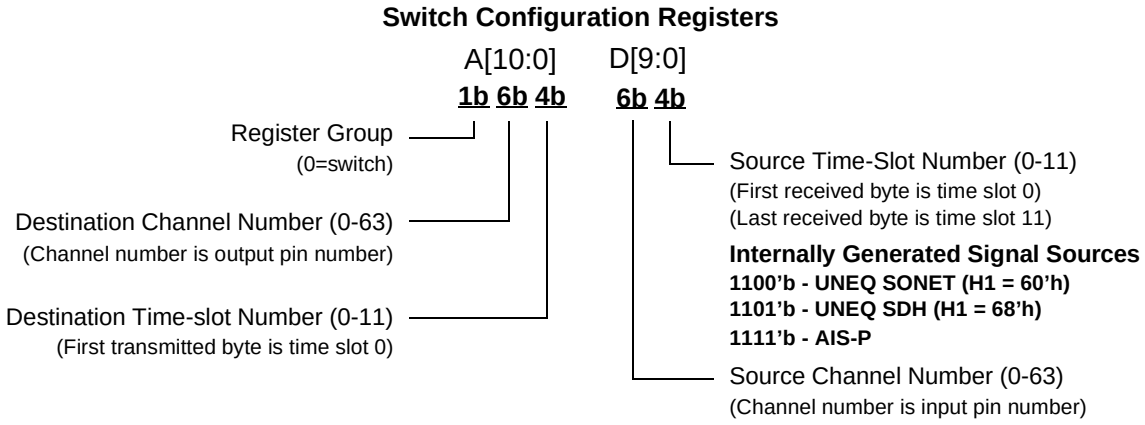
Table 2: Pin Definitions

Signal	*Name*	*IO*	*Type*	*Description*
RXD[63:0]P/N	STS-12/STM-4 serial Line (receive) inputs	I	622Mb/s LVDS	These signals carry the incoming serial 622.08 Mb/s STS-12/ STM-4 Line (receive) data streams. There are 100Ω terminations from true to complement.
TXD[63:0]P/N	STS-12/STM-4 serial Line (Transmit) outputs	O	622Mb/s LVDS	These signals carry the outgoing serial 622.08 Mb/s STS-12/ STM-4 Line (transmit) data streams.
SYSCLKP/N	System Clock	I	78MHz LVDS	Local system clock to which the incoming STS-12/STM-4 data streams are synchronous. SYSCLKP can be driven with a single ended CMOS signal (See *Termination Schemes*).
CLKSEL	System Clock Select	I	CMOS	Select pin to select the PLL multiplication factor. CLKSEL=1 gives a factor of 32 (19.44MHz F_{REF}) while CLKSEL=0 gives a factor of 8 (77.76MHz F_{REF}). The CLKSEL signal has an internal pull-up resistor.
PLOCK	PLL Lock Detect	O	CMOS	Provides an indication that the PLL is locked when high. The value of PLOCK may also be read by accessing the PLOCK register.
SYNCP/N	System Sync	I	LVDS	The frame boundaries of the incoming STS-12/STM-4 data streams should be aligned to this system SYNC input. A fixed offset value can be programmed in the SYNC_OFFSET register. SYNCP or SYNCN can be driven with a single ended CMOS signal (See *Termination Schemes*).
FOSYNCP/N	Sync Forward	O	LVDS	Latency-corrected SYNC output for cascading multiple VSC9182s. Aligned with the frame boundary of the TXD[63:0] output.
D[9:0]	Data Bus	B	50MHz CMOS	This bidirectional data bus is used to transfer data for microcontroller read/write access to internal program and status registers. The D[9:0] signals have internal pull-up resistors.
A[10:0]	Address Bus	I	50MHz CMOS	This address bus selects specific internal registers during register read/write access.The A[10:0] signals have internal pull-up resistors.
ALE	Address Latch Enable	I	50MHz CMOS	This signal controls internal latching of the address bus signals. When low the data bus D[9:0] is latched internally as the address. The A10 pin is still used in this mode to carry the MSB of addresses. When ALE is high the internal address bus latches are transparent and address is taken from A[10:0]. This signal will allow for interfacing to a multiplexed address/data bus, or can be disconnected or tied high for non multiplexed mode. The ALE signal has an internal pull-up resistor.
$\overline{CSB}$	Chip Select (active low)	I	50MHz CMOS	This signal must always be asserted during register read/write access cycles. The $\overline{CSB}$ signal has an internal pull-up resistor.

Signal	Name	IO	Type	Description
$\overline{\text{WRB}}$	Write Signal (active low)	I	50MHz CMOS	This signal is used for register write operations. The D[9:0] value is written into the register selected by A[10:0] when $\overline{\text{WRB}}$ and $\overline{\text{CSB}}$ are both asserted (low). The $\overline{\text{WRB}}$ signal has an internal pull-up resistor.
$\overline{\text{RDB}}$	Read Signal (active low)	I	50MHz CMOS	This signal is used for register read operations. The content of the register selected by A[10:0] is driving D[9:0] when $\overline{\text{RDB}}$ and $\overline{\text{CSB}}$ are both asserted (low).The $\overline{\text{RDB}}$ signal has an internal pull-up resistor.
$\overline{\text{RSTB}}$	Reset Signal (active low)	I	<1MHz CMOS	This signal provides (asynchronous) reset of the device. The device is held in a reset state while the $\overline{\text{RSTB}}$ signal is low. All CMOS outputs are tri-state when RSTB is asserted. RSTB should be asserted once the PLL is locked to align all the output interface blocks and initialize alarms. The $\overline{\text{RSTB}}$ signal has an internal pull-up resistor.
$\overline{\text{INTB}}$	Interrupt Signal (active low)	O	50MHz CMOS	This signal is asserted to indicate any occurrence of a parity error on any provisioned input channel. The $\overline{\text{INTB}}$ signal becomes inactive when the source of the interrupt has been cleared by reading the corresponding register.
CONFIG	Program Enable	I	50MHz CMOS	This signal must be asserted after transferring program data to the internal registers. Program changes take effect at the next frame boundary after CONFIG is asserted (high), or take effect after the number of frame boundaries indicated in the DELAY register. CONFIG is an asynchronous input with no setup/hold dependencies on other signals. CONFIG can also be asserted through writing the register location SOFTCONFIG while holding CONFIG low.The CONFIG signal has an internal pull-up resistor.
TDI	Test Data Input	I	<1MHz CMOS	The signal carries test data into the device via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an internal pull-up resistor.
TCK	Test Clock	I	<1MHz CMOS	This signal provides timing for test operations that are carried out using the IEEE P1149.1 test access port. TCK has an internal pull-up resistor.
TMS	Test Mode Select	I	<1MHz CMOS	This signal controls the test operations that are carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an internal pull-up resistor.
$\overline{\text{TRSTB}}$	Test Reset (active low)	I	<1MHz CMOS	This signal (active low) provides an asynchronous test access port reset via the IEEE P1149.1 test access port. $\overline{\text{TRSTB}}$ has an internal pull-up resistor.
TDO	Test Data Output	O	<1MHz CMOS	This signal carries data out of the device via the IEEE P1149.1 test access port. TDO changes following the rising edge of TCK.
TACO	Test Clock Output	O	78MHz CMOS	Test Clock Output. Leave unconnected. Do not route on PCB.

Signal	*Name*	*IO*	*Type*	*Description*
SCRMBL	Scrambler Control	I	<1MHz CMOS	This signal controls whether the backplane interfaces use SONET input descrambling and output scrambling (SCRMBL=1), or pass the signals through unscrambled (SCRMBL=0). Scrambling can also be enabled or disabled by writing to the scramble soft control registers while holding SCRMBL low. Disabling SONET scrambling requires both the SCRMBL pin to be set low and the control register be set to '0.' The SCRMBL signal has an internal pull-up resistor.
PARITYON	Parity Insert Control	I	<1MHz CMOS	This signal controls whether the output backplane interfaces insert the calculated parity from the previous frame into the first B1 position of the current frame. When low, the B1 position is left unaltered. B1 insertion can also be enabled by writing a '1' to the parity control register while holding PARITYON low. Disabling parity checking requires both the PARITYON pin to be set low and the control register be set to '0.' The PARITYON signal has an internal pull-up resistor.
CKBYP	Clock Bypass Control	I	<1MHz CMOS	CKBYP=1 puts the chip into vector test mode by using SYSCLK as the clock instead of the PLL output. The CKBYP signal has an internal pull-up resistor.
IDDQ1	Power Down	I	<1MHz CMOS	IDDQ1=1 shuts off all static power and dynamic activity associated with even inputs and outputs as well as the control circuitry. The IDDQ1 signal has an internal pull-up resistor.
IDDQ2	Power Down	I	<1MHz CMOS	IDDQ2=1 shuts off all static power and dynamic activity associated with odd inputs and outputs. The IDDQ2 signal has an internal pull-up resistor.
ATM0	A-Test-Mode 0	I	CMOS	Test Use Only; User must tie to logic low or GND. ATM0 has an internal pull-up resistor.
ATM1	A-Test-Mode 1	I	CMOS	Test Use Only; User must tie to logic low or GND. ATM1 has an internal pull-up resistor.
CTM	C-Test-Mode	I	CMOS	Test Use Only; User must tie to logic low or GND. CTM has an internal pull-up resistor.
AVDD	Analog VDD	P		Quiet Positive supply for PLL
AVSS	Analog VSS	G		Quiet Ground for PLL
VDD		P		General positive supply pins
VSS		G		General ground pins

Internal Register Address Maps



A[10]	*A[9:4]*	*A[3:0]*	*Description*
0'b	000000'b	0000'b	Address of TXDAT0, Time Slot 0's source data
0'b	000000'b	0001'b	Address of TXDAT0, Time Slot 1's source data
0'b	000000'b	...	...
0'b	000000'b	1011'b	Address of TXDAT0, Time Slot 11's source data
0'b	000001'b	0000'b	Address of TXDAT1, Time Slot 0's source data
0'b	000001'b	...	...
0'b	000001'b	1011'b	Address of TXDAT1, Time Slot 11's source data
0'b	...	...	...
0'b	...	...	...
0'b	111111'b	1011'b	Address of TXDAT63, Time Slot 11's source data

Notes on Output Time Slot Assignment

The value D[3:0] represents the SERIAL order received on the selected input, and not the standard SONET/SDH multiplexing hierarchy. A setting of 3'd would indicate a map to the fourth channel received serially on the input selected by D[9:4], not the SONET/SDH time slot assignment.The D[3:0] assignment has no relation to SONET/SDH time slot values.

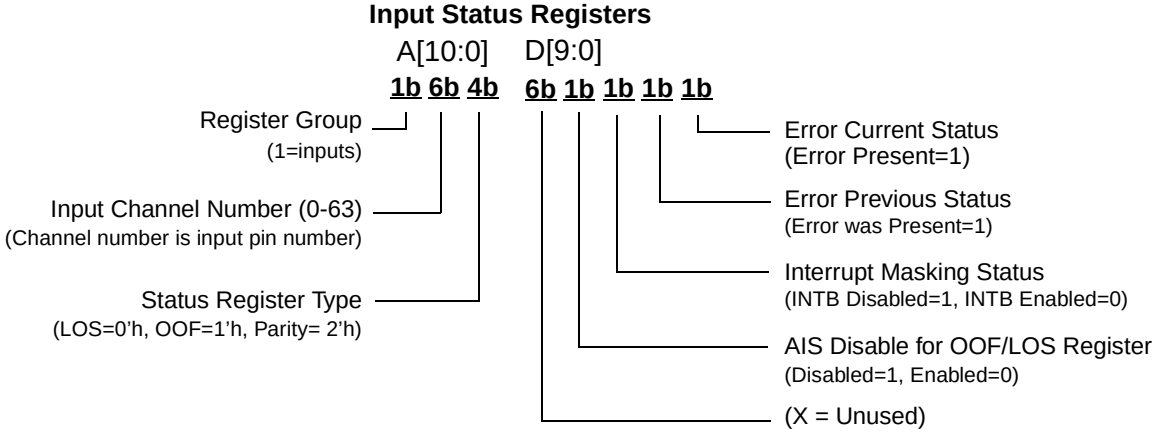
Internally-Generated Signal Sources

Programming D[3:0] to UNEQ or AIS-P selects an internal signal source that fills the addressed time slot with a framed all 1's pattern (AIS-P) or a framed all 0's pattern (UNEQ). The SONET/SDH mode UNEQ substitutes a special H1 byte value instead of an all 0's pattern.

Note that these D[3:0] values would normally represent time slot 12'd, 13'd and 15'd, which do not exist in the incoming STS-12 signals. Therefore, the values of D[9:4] are 'X' when D[3:0] is set to select an internal signal source.

When activating an internal signal source, the change does not take effect during the frame boundary as it does for standard channel/time slot connections. If the internally-generated signal sources are activated during a reprogramming operation that involves two or more stages of VSC9182 devices, truncation of data may occur because data is cut off along one path before the new path is established. It is recommended that the internally-generated signal sources only be used in the final stage of a multi-stage fabric. If desired, unused time slots in the earlier stages of a multi-stage fabric may be set to internally-generated signal sources with a second configuration operation after all the active data paths have been established.

Input Status Registers



A[10]	*A[9:4]*	*A[3:0]*	*Description*
1'b	000000'b	0000'b	LOS status for input channel 0
1'b	000001'b	0000'b	LOS status for input channel 1
1'b	...	...	...
1'b	111111'b	0000'b	LOS status for input channel 63
1'b	000000'b	0001'b	OOF status for input channel 0
1'b	000001'b	0001'b	OOF status for input channel 1
1'b	...	0001'b	...
1'b	111111'b	0001'b	OOF status for input channel 63
1'b	000000'b	0010'b	Parity status for input channel 0
1'b	000001'b	0010'b	Parity status for input channel 1
1'b	...	0010'b	...
1'b	111111'b	0010'b	Parity status for input channel 63

The input status registers may be read to observe the status of LOS, OOF and parity alarms. Each type of interrupt in each input channel may be masked individually by writing a '1' to the Interrupt Masking Status bit (see above). LOS and OOF interrupts for all provisioned input channels should be masked since their interrupt generation is no longer supported. In order to observe the current and previously read alarms, both current and

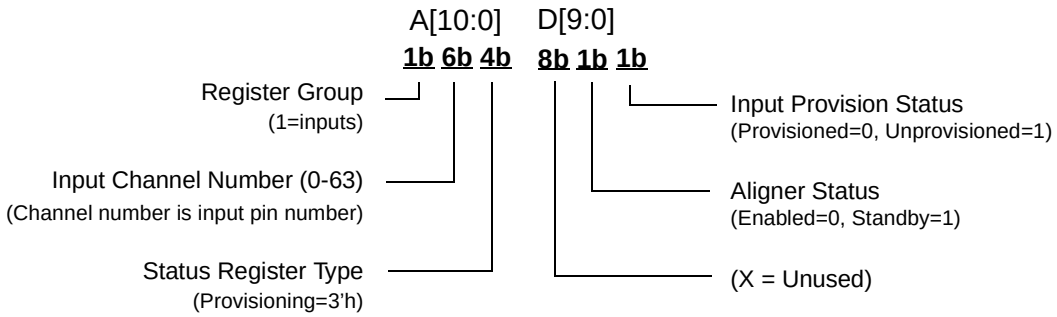
history bits are provided (see Table 3). For parity alarms, an interrupt is generated for each errored frame, and only the value of the Current Status bit and Masking Status bits are meaningful. Writing to the error status bits will have no effect. Note: For latching or clearing the alarm status bytes the address bits must be stable before RDB goes low.

Table 3: Input Status Register Current and History Bits

D[1:0]	*Meaning*
00	Alarm stable since last read; no alarm present
01	Alarm changed one or more times since last read, last transition was 0-1
10	Alarm changed one or more times since last read, last transition was 1-0
11	Alarm stable since last read; alarm is still present

NOTE: When the aligner is in standby state the clock to the LOS detector is shut off so it holds its last value.

Input Provisioning Registers

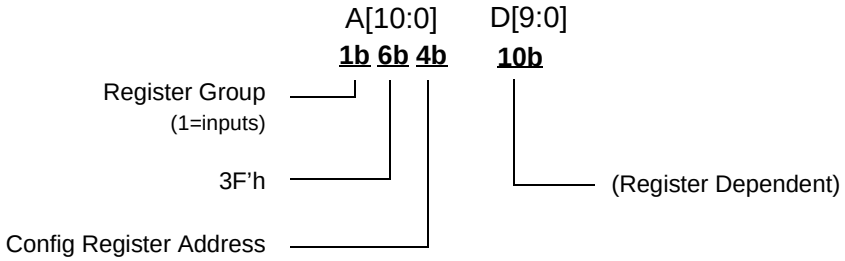


A[10]	*A[9:4]*	*A[3:0]*	*Description*
1'b	000000'b	0011'b	Provision and aligner status for input channel 0
1'b	000001'b	0011'b	Provision and aligner status for input channel 1
1'b	...	0011'b	...
1'b	111111'b	0011'b	Provision and aligner status for input channel 63

The input provisioning registers can be used to indicate which channels are active. A channel in the *unprovisioned* state will send the *Unequipped* code (all zeroes with valid A1/A2 sequences and H1 = 68'h) to the switch core, and will be incapable of generating any interrupts. The LOS, OOF and Parity alarms will still function normally in this state.

The bit aligner can be shut off on unused channels. This is done by writing a '1' to the Aligner Power Status bit.

General Configuration Registers



GENERAL CONFIGURATION REGISTERS			
A[10]	***A[9:4]***	***A[3:0]***	***Description***
1'b	111111'b	0110'b	COARSE_SYNC_OFFSET- Binary value that indicates offset of SYNC input as a function of row and column locations. Valid settings range from 000'h to 329'h (809'd or 1100101001'b), corresponding to the 810 row/column locations in a SONET/SDH frame. A value of 0'h indicates the A1 byte location, 05C'h (92'd) indicates the F1 location (Row 2, Column 3), or 11E'h would indicate the byte in the 4th frame row and 17th column. Default value is 000'h.
1'b	111111'b	0111'b	FINE_SYNC_OFFSET-Binary value that indicates offset of SYNC input as a function of time slots. COARSE_SYNC_OFFSET specifies frame location for SYNC, and FINE_SYNC_OFFSET specifies in which of the 12 time slots the SYNC should take place. Valid settings range from 000'h to 00B'h (11'd or 1011'b), corresponding to the 12 time slots locations in the STS-12 input. A COARSE_SYNC_OFFSET value of 05C'h (92'd) and FINE_SYNC_OFFSET value of 005'h would indicate that the VSC9182 should expect an external SYNC transition at the instant that the 6th time slot of the F1 byte location (Row 2, Column 3) was being received through the RXD[63:0] inputs, and allow the device to anticipate the arrival of the A1/A2 boundary at the appropriate later time. Default value is 000'h.
1'b	111111'b	1000'b	CHANGE - Byte transmitted for a single frame following a CONFIG signal on all 64 outputs in overhead location specified by CHANGE_LOC. Default value is FF'h (this is an 8-bit value, bits 9 and 8 are meaningless).
1'b	111111'b	1001'b	NORMAL - Byte transmitted in overhead location specified by CHANGE_LOC. This byte will be replaced for one transmitted frame by the CHANGE byte when a CONFIG signal is received. Default value is 00'h (this is an 8-bit value, bits 9 and 8 are meaningless).

GENERAL CONFIGURATION REGISTERS			
A[10]	***A[9:4]***	***A[3:0]***	***Description***
1'b	111111'b	1010'b	CHANGE_LOC - Location of NORMAL and CHANGE bytes in the outgoing TXD[63:0] signals. D[9:6] contain the row value (Valid settings: 0'h to 8'h), D[5:4] contain the column value (Valid settings: 0'h to 2'h) and D[3:0] contain the channel value (Valid settings: 0'h to B'h). A value of (0001)(00)(0001)'b (Row 2, Column 1, Channel 2) would cause the CHANGE and NORMAL bytes to be transmitted immediately following the B1 byte location. A value of (0000)(10)(0000)'b sets CHANGE_LOC to the J0 byte. Writing a value of 3FF'h ((1111)(11)(1111)'b) to this location disables the in-band messaging features and is automatically set following a device reset. Note that 3FF'h is an invalid location value.
1'b	111111'b	1011'b	DELAY - Allows the user to specify a programming delay measured in received frames from the time CONFIG is issued to when the switch configuration takes place. Valid settings range from 000'h to 00F'h, where the value indicates the number of complete frames to receive before switch configuration. A value of 000'h indicates that the change should take place at the next received frame boundary. A value of 002'h would indicate that two complete STS-12 frames should be received prior to re-configuration on the third received frame boundary. Additional CONFIG pulses are ignored during the delay period. Default setting is 000'h.
1'b	111111'b	1100'b	SCRMBL Soft Control. Writing a '1' to D[0] enables input descrambling and output scrambling. A value of '1' on the SCRMBL pin overrides this register. There is no default value. If not using scrambling, this register must be written with a '0.'
1'b	111111'b	1101'b	PRTYON Soft Control. Writing a '1' to D[0] enables output B1 parity insertion. A value of '1' on the PRTYON pin overrides this register. There is no default value. If not using parity insertion, this register must be written with a '0'.
1'b	111111'b	1110'b	PLOCK Status Register. Reading this register will give the status of the PLL (locked= '1' on D[0:2]) as an alternate method to observing the PLOCK pin. Bits D[4:7] will also provide the revision ID code. Rev A/B would read 307'h, Rev C would read 337'h, and Rev D would read 347'h (when the PLL is locked). Writing to this register has no effect.
1'b	111111'b	1111'b	SOFTCONFIG.Writing a 1 to D[0] has the same effect as asserting the external CONFIG pin, and generates an internal CONFIG pulse- there is no need to re-write a '0' following a '1.' Reading back this register will always give 3FF'h.

Absolute Maximum Ratings(1)

Power Supply Voltage (V_{DD}) Potential to GND ..... -0.5V to +3.8V
DC Input Voltage (LVDS inputs) ..... -0.5V to V_{DD} + 0.5V
DC Input Voltage Across LVDS input terminations ..... -1.2V to +1.2V
DC Input Voltage (CMOS inputs) ..... -0.5V to V_{DD} + 0.5V
DC Output Voltage (LVDS outputs) ..... -0.5V to V_{DD} + 0.5V
DC Output Voltage (CMOS outputs) ..... -0.5V to V_{DD} + 0.5V
Output Current (CMOS outputs) ..... +/-50mA
Output Current (LVDS outputs) ..... +/-50mA
Case Temperature Under Bias ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C

NOTE: (1) Caution: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Recommended Operating Conditions

Core Power Supply Voltage (V_{DD}) ..... +3.3V±5%
Operating Temperature Range(T)(1) ..... 0°C to 105°C

NOTE: (1) Lower limit of specification is ambient temperature and upper limit is case temperature.

ESD Rating

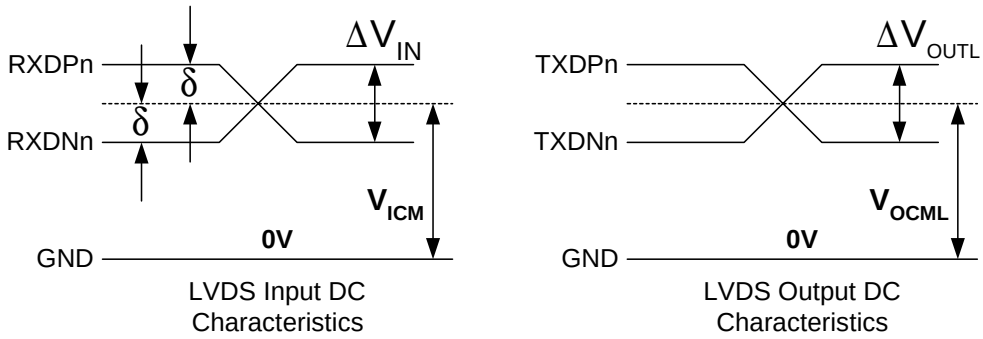
Proper ESD procedures should be used when handling this product. The VSC9182 is rated to 1000V based on the human body model.

Table 4: LVDS and CMOS Inputs and Outputs

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{OH}	Output HIGH Voltage (CMOS)	V_{DD}-0.35		V_{DD}	V	$I_{OH(DC)}$ = -2mA
V_{OL}	Output LOW Voltage (CMOS)	0		0.25	V	$I_{OL(DC)}$ = 2mA
V_{IH}	Input HIGH Voltage (CMOS)	2.0		V_{DD}	V	
V_{IL}	Input LOW Voltage (CMOS)	0		1.0	V	
I_{IT}	Input Current (CMOS)(1)			65	µA	0V< V_{IN} < V_{DD}
V_{OCML}	Output Common-Mode Range (LVDS)	1.0		1.5	V	100Ω across outputs
ΔV_{OUTL}	Output Voltage Swing (LVDS)	250		600	mV	100Ω across outputs
R_{OUT}	Output Driver Impedance (LVDS)		100		Ω	
V_{ICM}	Input Common-Mode Range (LVDS)(2)	δ		V_{DD} - δ	V	δ =ΔV_{IN} / 2
ΔV_{IN}	Input Voltage Swing (LVDS)(2)	100		1000	mV	
R_{IN}	Input Termination Resistance	80		120	Ω	True to complement

NOTES: (1) All CMOS inputs have internal pull-up resistors with a maximum pull-up current of 65µA. (2) The input receiver can handle most LVPECL and CML signals as well as LVDS.

Figure 2: LVDS CMOS Inputs and Outputs



Power Dissipation

Table 5: Power Supply Currents

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
I_{DD}	V_{DD} Current on Cold Startup			5.3	A	V_{DD} = 3.465V, T_A= 0°C, outputs loaded
P_D	Power Dissipation for thermal design			16	W	V_{DD} = 3.465V, T_C = 105°C, outputs loaded

AC Characteristics

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
F_{REF0}	SYSCLK Frequency, for CLKSEL=0	-1%	19.44	+1%	MHz	
F_{REF1}	SYSCLK Frequency, for CLKSEL=1	-1%	77.76	+1%	MHz	
t_{LOCK}	PLL Lock Time			100	µs	From SYSCLK applied
F_{LBW}	PLL Loop Bandwidth			$F_{REF}/10$		
F_{DATA}	Input or output data rate on RXD[63:0] and TXD[63:0]	-1%	622.08	+1%	Mb/s	F_{DATA} is a multiple of SYSCLK
t_{OCRF}	CMOS output rise/fall times	2.5		5	ns	20pF load, 10%-90%
t_{ORF}	LVDS output rise/fall times			600	ps	20%-80% into 50Ω t-lines
t_{IRF}	LVDS input rise/fall times			800	ps	20%-80%
t_{JO}	Peak-to-peak jitter at output, unfiltered			250	ps	PLL locked, scrambled data
t_{AD}	Delay from change in ADDR[10:0] to Data valid on DATA[9:0]	13		25	ns	20pF load
t_{RD}	Delay from falling edge of RDB or CSB to Data valid on DATA[9:0]	11		23	ns	
t_{sWRB}	Setup time from ADDR[10:0] or DATA[9:0] to rising edge of WRB or CSB	6			ns	
t_{hWRB}	Hold time from rising edge of WRB or CSB to ADDR[10:0] or DATA[9:0]	2			ns	
t_{PWC}	Pulse width (high or low) on RDB, WRB, ALE, CSB, CONFIG	10			ns	
t_{sUA}	Setup time from DATA[9:0] to falling edge of ALE with muxed bus	5			ns	
t_{hUA}	Hold time of DATA[9:0] after falling edge of ALE with multiplexed bus	2			ns	
t_Z	Delay from RDB or CSB rising to tri-state on DATA[9:0]	2		5	ns	20pF load
t_{DSYNC}	Delay from SYNC rising edge to frame start in incoming data	-38.4		+38.4	ns	
t_{VSYNC}	Maximum SYNC edge variation	-6.4		+6.4	ns	
t_{PWSYNC}	Pulse width (high) of SYNC signal	11.0		62500	ns	
$t_{DFOSYNC}$	Delay from SYNC to FOSYNC	290		298	ns	
$t_{PWFOSYNC}$	Pulse width of FOSYNC output	11.5		14.0	ns	
t_{PRST}	Pulse width (low) of RSTB	50			ns	
t_{PTRST}	Pulse width (low) of TRSTB	50			ns	
t_{sTDI}	Setup time from TDI to TCK rising	3			ns	
t_{hTDI}	Hold time of TDI after TCK rising	2			ns	
t_{sTMS}	Setup time from TMS to TCK rising	3			ns	
t_{hTMS}	Hold time of TMS after TCK rising	2			ns	
t_{TDO}	Delay from TCK fall to TDO change	2		5	ns	20pF load
t_{TCK}	TCK period	100			ns	

Timing Diagrams

Figure 3: Program Timing—Separate Address and Data (leave ALE pin HIGH)

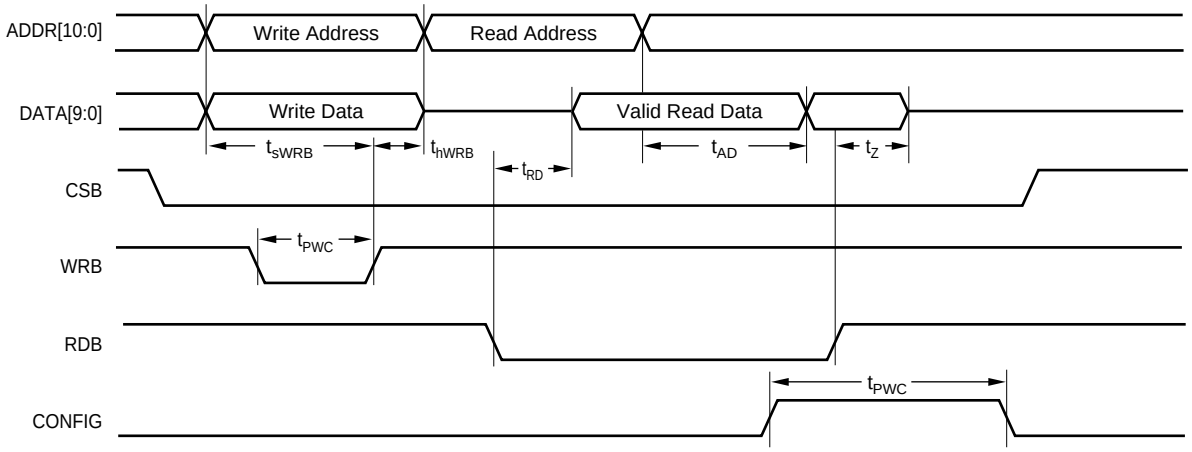


Figure 4: Program Timing—Multiplexed Address and Data

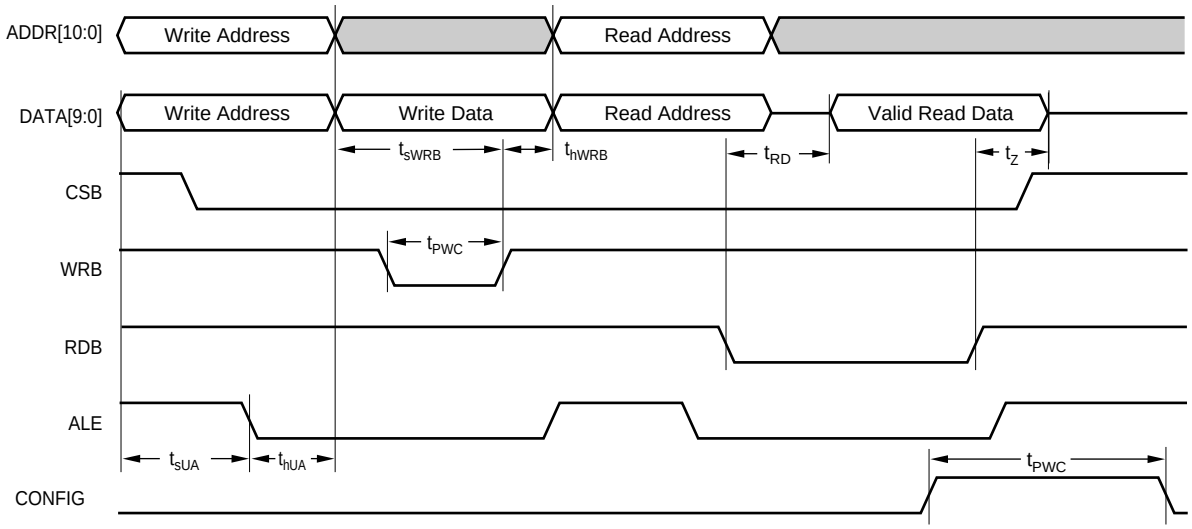


Figure 5: Test Access Port Timing

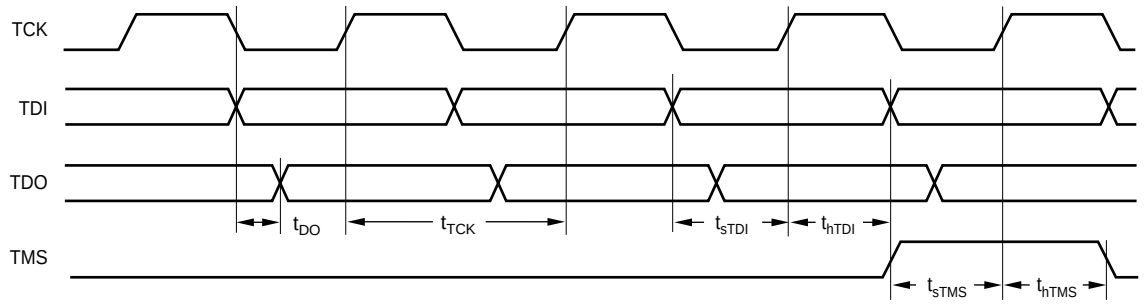


Figure 6: Synchronization Timing

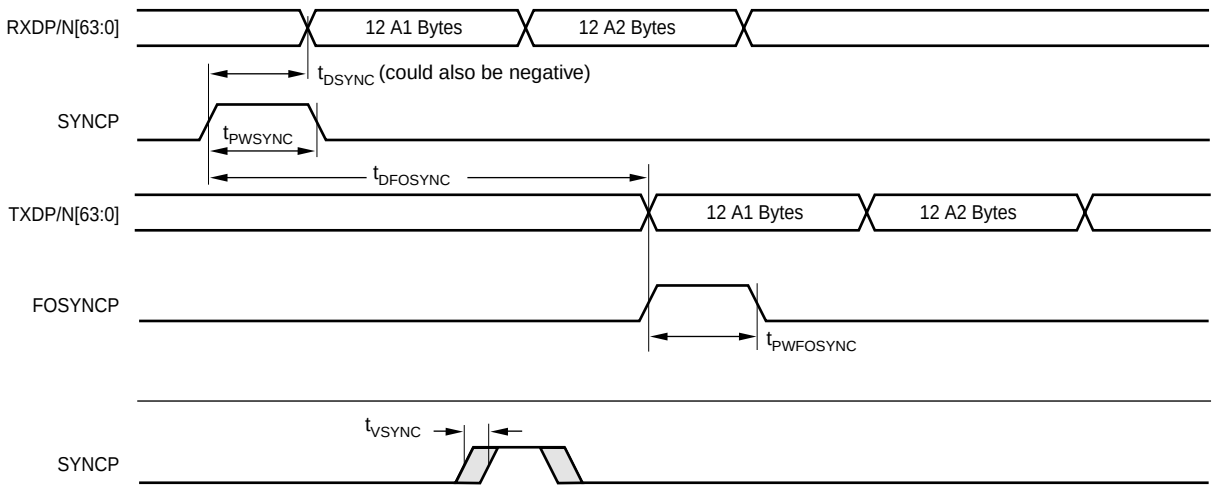
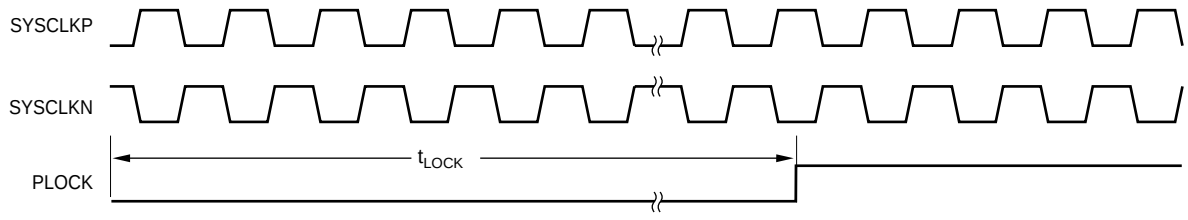
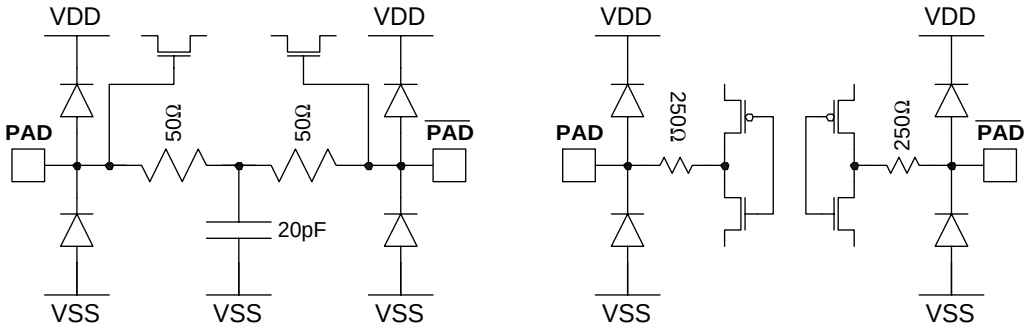


Figure 7: PLL Lock Timing



I/O Equivalent Circuits

Figure 8: High-Speed Input/Output



Termination Schemes

Figure 9: Standard (LVDS)

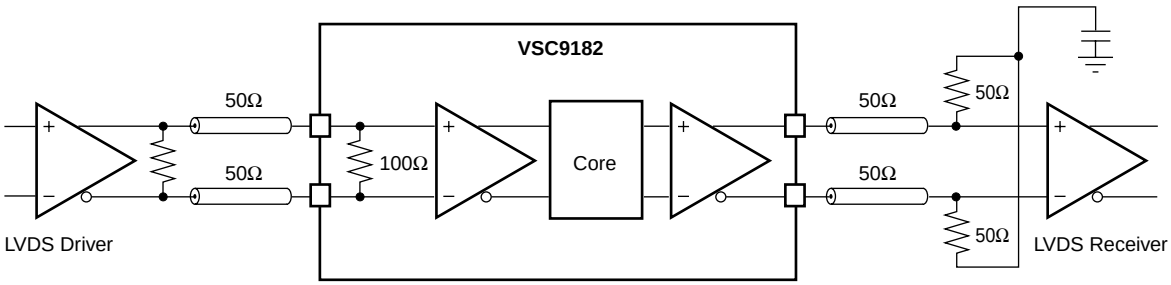


Figure 10: Other Differential Drivers and/or Receivers

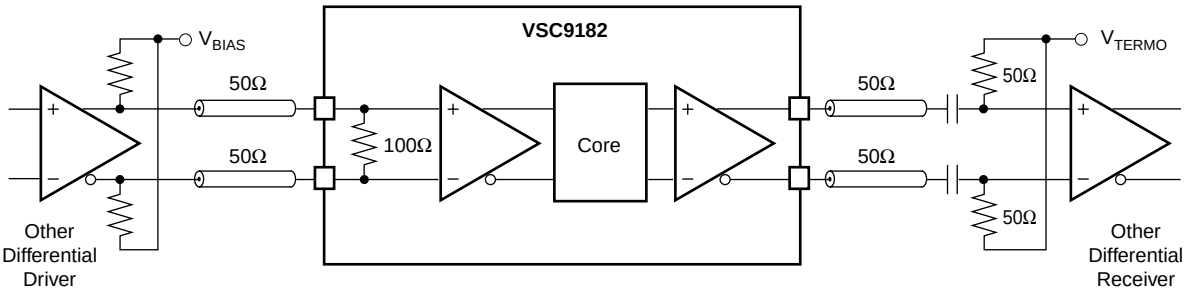
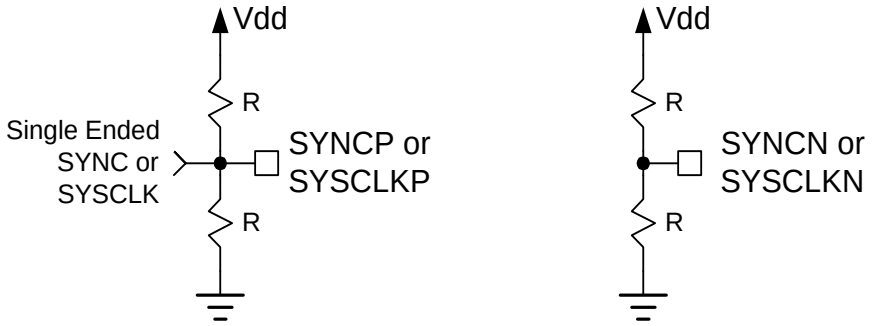


Figure 11: Interfacing SYNCP/N and SYSCLKP/N to Single-Ended CMOS



The above network (Figure 11) should be externally attached to each true and complement pin in order to interface SYNCP/N or SYSCLKP/N to single-ended 3.3V CMOS signals. The true input should then be driven.

The four resistors shown should be of the same value; the value R should be between 140Ω and 365Ω. The 140Ω value will result in an impedance-matched (50Ω) termination with a current load of +/-7mA, while the 365Ω value will result in the minimum current load (3.6mA) while still providing adequate drive levels to the chip input.

Package Pin Descriptions

Table 6: Pin Identifications

Signal Name	*Pin*	*Level*	*Function*
RXDN0	E23	LVDS	High-Speed Data Input Channel 0 complement
RXDN1	AJ23	LVDS	High-Speed Data Input Channel 1 complement
RXDN2	A23	LVDS	High-Speed Data Input Channel 2 complement
RXDN3	AE23	LVDS	High-Speed Data Input Channel 3 complement
RXDN4	E22	LVDS	High-Speed Data Input Channel 4 complement
RXDN5	AJ22	LVDS	High-Speed Data Input Channel 5 complement
RXDN6	A22	LVDS	High-Speed Data Input Channel 6 complement
RXDN7	AE22	LVDS	High-Speed Data Input Channel 7 complement
RXDN8	E21	LVDS	High-Speed Data Input Channel 8 complement
RXDN9	AJ21	LVDS	High-Speed Data Input Channel 9 complement
RXDN10	A21	LVDS	High-Speed Data Input Channel 10 complement
RXDN11	AE21	LVDS	High-Speed Data Input Channel 11 complement
RXDN12	E20	LVDS	High-Speed Data Input Channel 12 complement
RXDN13	AJ20	LVDS	High-Speed Data Input Channel 13 complement
RXDN14	A20	LVDS	High-Speed Data Input Channel 14 complement
RXDN15	AE20	LVDS	High-Speed Data Input Channel 15 complement
RXDN16	E19	LVDS	High-Speed Data Input Channel 16 complement
RXDN17	AJ19	LVDS	High-Speed Data Input Channel 17 complement
RXDN18	A19	LVDS	High-Speed Data Input Channel 18 complement
RXDN19	AE19	LVDS	High-Speed Data Input Channel 19 complement
RXDN20	E18	LVDS	High-Speed Data Input Channel 20 complement
RXDN21	AJ18	LVDS	High-Speed Data Input Channel 21 complement
RXDN22	A18	LVDS	High-Speed Data Input Channel 22 complement
RXDN23	AE18	LVDS	High-Speed Data Input Channel 23 complement
RXDN24	E17	LVDS	High-Speed Data Input Channel 24 complement
RXDN25	AJ17	LVDS	High-Speed Data Input Channel 25 complement
RXDN26	A17	LVDS	High-Speed Data Input Channel 26 complement
RXDN27	AE17	LVDS	High-Speed Data Input Channel 27 complement
RXDN28	E16	LVDS	High-Speed Data Input Channel 28 complement
RXDN29	AJ16	LVDS	High-Speed Data Input Channel 29 complement
RXDN30	A16	LVDS	High-Speed Data Input Channel 30 complement
RXDN31	AE16	LVDS	High-Speed Data Input Channel 31 complement
RXDN32	E15	LVDS	High-Speed Data Input Channel 32 complement
RXDN33	AJ15	LVDS	High-Speed Data Input Channel 33 complement
RXDN34	A15	LVDS	High-Speed Data Input Channel 34 complement

RXDN35	AE15	LVDS	High-Speed Data Input Channel 35 complement
RXDN36	E14	LVDS	High-Speed Data Input Channel 36 complement
RXDN37	AJ14	LVDS	High-Speed Data Input Channel 37 complement
RXDN38	A14	LVDS	High-Speed Data Input Channel 38 complement
RXDN39	AE14	LVDS	High-Speed Data Input Channel 39 complement
RXDN40	E13	LVDS	High-Speed Data Input Channel 40 complement
RXDN41	AJ13	LVDS	High-Speed Data Input Channel 41 complement
RXDN42	A13	LVDS	High-Speed Data Input Channel 42 complement
RXDN43	AE13	LVDS	High-Speed Data Input Channel 43 complement
RXDN44	E12	LVDS	High-Speed Data Input Channel 44 complement
RXDN45	AJ12	LVDS	High-Speed Data Input Channel 45 complement
RXDN46	A12	LVDS	High-Speed Data Input Channel 46 complement
RXDN47	AE12	LVDS	High-Speed Data Input Channel 47 complement
RXDN48	E11	LVDS	High-Speed Data Input Channel 48 complement
RXDN49	AJ11	LVDS	High-Speed Data Input Channel 49 complement
RXDN50	A11	LVDS	High-Speed Data Input Channel 50 complement
RXDN51	AE11	LVDS	High-Speed Data Input Channel 51 complement
RXDN52	E10	LVDS	High-Speed Data Input Channel 52 complement
RXDN53	AJ10	LVDS	High-Speed Data Input Channel 53 complement
RXDN54	A10	LVDS	High-Speed Data Input Channel 54 complement
RXDN55	AE10	LVDS	High-Speed Data Input Channel 55 complement
RXDN56	E9	LVDS	High-Speed Data Input Channel 56 complement
RXDN57	AJ9	LVDS	High-Speed Data Input Channel 57 complement
RXDN58	A9	LVDS	High-Speed Data Input Channel 58 complement
RXDN59	AE9	LVDS	High-Speed Data Input Channel 59 complement
RXDN60	E8	LVDS	High-Speed Data Input Channel 60 complement
RXDN61	AJ8	LVDS	High-Speed Data Input Channel 61 complement
RXDN62	A8	LVDS	High-Speed Data Input Channel 62 complement
RXDN63	AE8	LVDS	High-Speed Data Input Channel 63 complement
RXDP0	D23	LVDS	High-Speed Data Input Channel 0 true
RXDP1	AH23	LVDS	High-Speed Data Input Channel 1 true
RXDP2	B23	LVDS	High-Speed Data Input Channel 2 true
RXDP3	AF23	LVDS	High-Speed Data Input Channel 3 true
RXDP4	D22	LVDS	High-Speed Data Input Channel 4 true
RXDP5	AH22	LVDS	High-Speed Data Input Channel 5 true
RXDP6	B22	LVDS	High-Speed Data Input Channel 6 true
RXDP7	AF22	LVDS	High-Speed Data Input Channel 7 true
RXDP8	D21	LVDS	High-Speed Data Input Channel 8 true
RXDP9	AH21	LVDS	High-Speed Data Input Channel 9 true

RXDP10	B21	LVDS	High-Speed Data Input Channel 10 true
RXDP11	AF21	LVDS	High-Speed Data Input Channel 11 true
RXDP12	D20	LVDS	High-Speed Data Input Channel 12 true
RXDP13	AH20	LVDS	High-Speed Data Input Channel 13 true
RXDP14	B20	LVDS	High-Speed Data Input Channel 14 true
RXDP15	AF20	LVDS	High-Speed Data Input Channel 15 true
RXDP16	D19	LVDS	High-Speed Data Input Channel 16 true
RXDP17	AH19	LVDS	High-Speed Data Input Channel 17 true
RXDP18	B19	LVDS	High-Speed Data Input Channel 18 true
RXDP19	AF19	LVDS	High-Speed Data Input Channel 19 true
RXDP20	D18	LVDS	High-Speed Data Input Channel 20 true
RXDP21	AH18	LVDS	High-Speed Data Input Channel 21 true
RXDP22	B18	LVDS	High-Speed Data Input Channel 22 true
RXDP23	AF18	LVDS	High-Speed Data Input Channel 23 true
RXDP24	D17	LVDS	High-Speed Data Input Channel 24 true
RXDP25	AH17	LVDS	High-Speed Data Input Channel 25 true
RXDP26	B17	LVDS	High-Speed Data Input Channel 26 true
RXDP27	AF17	LVDS	High-Speed Data Input Channel 27 true
RXDP28	D16	LVDS	High-Speed Data Input Channel 28 true
RXDP29	AH16	LVDS	High-Speed Data Input Channel 29 true
RXDP30	B16	LVDS	High-Speed Data Input Channel 30 true
RXDP31	AF16	LVDS	High-Speed Data Input Channel 31 true
RXDP32	D15	LVDS	High-Speed Data Input Channel 32 true
RXDP33	AH15	LVDS	High-Speed Data Input Channel 33 true
RXDP34	B15	LVDS	High-Speed Data Input Channel 34 true
RXDP35	AF15	LVDS	High-Speed Data Input Channel 35 true
RXDP36	D14	LVDS	High-Speed Data Input Channel 36 true
RXDP37	AH14	LVDS	High-Speed Data Input Channel 37 true
RXDP38	B14	LVDS	High-Speed Data Input Channel 38 true
RXDP39	AF14	LVDS	High-Speed Data Input Channel 39 true
RXDP40	D13	LVDS	High-Speed Data Input Channel 40 true
RXDP41	AH13	LVDS	High-Speed Data Input Channel 41 true
RXDP42	B13	LVDS	High-Speed Data Input Channel 42 true
RXDP43	AF13	LVDS	High-Speed Data Input Channel 43 true
RXDP44	D12	LVDS	High-Speed Data Input Channel 44 true
RXDP45	AH12	LVDS	High-Speed Data Input Channel 45 true
RXDP46	B12	LVDS	High-Speed Data Input Channel 46 true
RXDP47	AF12	LVDS	High-Speed Data Input Channel 47 true
RXDP48	D11	LVDS	High-Speed Data Input Channel 48 true

RXDP49	AH11	LVDS	High-Speed Data Input Channel 49 true
RXDP50	B11	LVDS	High-Speed Data Input Channel 50 true
RXDP51	AF11	LVDS	High-Speed Data Input Channel 51 true
RXDP52	D10	LVDS	High-Speed Data Input Channel 52 true
RXDP53	AH10	LVDS	High-Speed Data Input Channel 53 true
RXDP54	B10	LVDS	High-Speed Data Input Channel 54 true
RXDP55	AF10	LVDS	High-Speed Data Input Channel 55 true
RXDP56	D9	LVDS	High-Speed Data Input Channel 56 true
RXDP57	AH9	LVDS	High-Speed Data Input Channel 57 true
RXDP58	B9	LVDS	High-Speed Data Input Channel 58 true
RXDP59	AF9	LVDS	High-Speed Data Input Channel 59 true
RXDP60	D8	LVDS	High-Speed Data Input Channel 60 true
RXDP61	AH8	LVDS	High-Speed Data Input Channel 61 true
RXDP62	B8	LVDS	High-Speed Data Input Channel 62 true
RXDP63	AF8	LVDS	High-Speed Data Input Channel 63 true
TXDN0	G5	LVDS	High-Speed Data Output Channel 0 complement
TXDN1	G29	LVDS	High-Speed Data Output Channel 1 complement
TXDN2	G1	LVDS	High-Speed Data Output Channel 2 complement
TXDN3	G25	LVDS	High-Speed Data Output Channel 3 complement
TXDN4	H5	LVDS	High-Speed Data Output Channel 4 complement
TXDN5	H29	LVDS	High-Speed Data Output Channel 5 complement
TXDN6	H1	LVDS	High-Speed Data Output Channel 6 complement
TXDN7	H25	LVDS	High-Speed Data Output Channel 7 complement
TXDN8	J5	LVDS	High-Speed Data Output Channel 8 complement
TXDN9	J29	LVDS	High-Speed Data Output Channel 9 complement
TXDN10	J1	LVDS	High-Speed Data Output Channel 10 complement
TXDN11	J25	LVDS	High-Speed Data Output Channel 11 complement
TXDN12	K5	LVDS	High-Speed Data Output Channel 12 complement
TXDN13	K29	LVDS	High-Speed Data Output Channel 13 complement
TXDN14	K1	LVDS	High-Speed Data Output Channel 14 complement
TXDN15	K25	LVDS	High-Speed Data Output Channel 15 complement
TXDN16	L5	LVDS	High-Speed Data Output Channel 16 complement
TXDN17	L29	LVDS	High-Speed Data Output Channel 17 complement
TXDN18	L1	LVDS	High-Speed Data Output Channel 18 complement
TXDN19	L25	LVDS	High-Speed Data Output Channel 19 complement
TXDN20	M5	LVDS	High-Speed Data Output Channel 20 complement
TXDN21	M29	LVDS	High-Speed Data Output Channel 21 complement
TXDN22	M1	LVDS	High-Speed Data Output Channel 22 complement
TXDN23	M25	LVDS	High-Speed Data Output Channel 23 complement

TXDN24	N5	LVDS	High-Speed Data Output Channel 24 complement
TXDN25	N29	LVDS	High-Speed Data Output Channel 25 complement
TXDN26	N1	LVDS	High-Speed Data Output Channel 26 complement
TXDN27	N25	LVDS	High-Speed Data Output Channel 27 complement
TXDN28	P5	LVDS	High-Speed Data Output Channel 28 complement
TXDN29	P29	LVDS	High-Speed Data Output Channel 29 complement
TXDN30	P1	LVDS	High-Speed Data Output Channel 30 complement
TXDN31	P25	LVDS	High-Speed Data Output Channel 31 complement
TXDN32	R5	LVDS	High-Speed Data Output Channel 32 complement
TXDN33	R29	LVDS	High-Speed Data Output Channel 33 complement
TXDN34	R1	LVDS	High-Speed Data Output Channel 34 complement
TXDN35	R25	LVDS	High-Speed Data Output Channel 35 complement
TXDN36	T5	LVDS	High-Speed Data Output Channel 36 complement
TXDN37	T29	LVDS	High-Speed Data Output Channel 37 complement
TXDN38	T1	LVDS	High-Speed Data Output Channel 38 complement
TXDN39	T25	LVDS	High-Speed Data Output Channel 39 complement
TXDN40	U5	LVDS	High-Speed Data Output Channel 40 complement
TXDN41	U29	LVDS	High-Speed Data Output Channel 41 complement
TXDN42	U1	LVDS	High-Speed Data Output Channel 42 complement
TXDN43	U25	LVDS	High-Speed Data Output Channel 43 complement
TXDN44	V5	LVDS	High-Speed Data Output Channel 44 complement
TXDN45	V29	LVDS	High-Speed Data Output Channel 45 complement
TXDN46	V1	LVDS	High-Speed Data Output Channel 46 complement
TXDN47	V25	LVDS	High-Speed Data Output Channel 47 complement
TXDN48	W5	LVDS	High-Speed Data Output Channel 48 complement
TXDN49	W29	LVDS	High-Speed Data Output Channel 49 complement
TXDN50	W1	LVDS	High-Speed Data Output Channel 50 complement
TXDN51	W25	LVDS	High-Speed Data Output Channel 51 complement
TXDN52	Y5	LVDS	High-Speed Data Output Channel 52 complement
TXDN53	Y29	LVDS	High-Speed Data Output Channel 53 complement
TXDN54	Y1	LVDS	High-Speed Data Output Channel 54 complement
TXDN55	Y25	LVDS	High-Speed Data Output Channel 55 complement
TXDN56	AA5	LVDS	High-Speed Data Output Channel 56 complement
TXDN57	AA29	LVDS	High-Speed Data Output Channel 57 complement
TXDN58	AA1	LVDS	High-Speed Data Output Channel 58 complement
TXDN59	AA25	LVDS	High-Speed Data Output Channel 59 complement
TXDN60	AB5	LVDS	High-Speed Data Output Channel 60 complement
TXDN61	AB29	LVDS	High-Speed Data Output Channel 61 complement
TXDN62	AB1	LVDS	High-Speed Data Output Channel 62 complement

TXDN63	AB25	LVDS	High-Speed Data Output Channel 63 complement
TXDP0	G4	LVDS	High-Speed Data Output Channel 0 true
TXDP1	G28	LVDS	High-Speed Data Output Channel 1 true
TXDP2	G2	LVDS	High-Speed Data Output Channel 2 true
TXDP3	G26	LVDS	High-Speed Data Output Channel 3 true
TXDP4	H4	LVDS	High-Speed Data Output Channel 4 true
TXDP5	H28	LVDS	High-Speed Data Output Channel 5 true
TXDP6	H2	LVDS	High-Speed Data Output Channel 6 true
TXDP7	H26	LVDS	High-Speed Data Output Channel 7 true
TXDP8	J4	LVDS	High-Speed Data Output Channel 8 true
TXDP9	J28	LVDS	High-Speed Data Output Channel 9 true
TXDP10	J2	LVDS	High-Speed Data Output Channel 10 true
TXDP11	J26	LVDS	High-Speed Data Output Channel 11 true
TXDP12	K4	LVDS	High-Speed Data Output Channel 12 true
TXDP13	K28	LVDS	High-Speed Data Output Channel 13 true
TXDP14	K2	LVDS	High-Speed Data Output Channel 14 true
TXDP15	K26	LVDS	High-Speed Data Output Channel 15 true
TXDP16	L4	LVDS	High-Speed Data Output Channel 16 true
TXDP17	L28	LVDS	High-Speed Data Output Channel 17 true
TXDP18	L2	LVDS	High-Speed Data Output Channel 18 true
TXDP19	L26	LVDS	High-Speed Data Output Channel 19 true
TXDP20	M4	LVDS	High-Speed Data Output Channel 20 true
TXDP21	M28	LVDS	High-Speed Data Output Channel 21 true
TXDP22	M2	LVDS	High-Speed Data Output Channel 22 true
TXDP23	M26	LVDS	High-Speed Data Output Channel 23 true
TXDP24	N4	LVDS	High-Speed Data Output Channel 24 true
TXDP25	N28	LVDS	High-Speed Data Output Channel 25 true
TXDP26	N2	LVDS	High-Speed Data Output Channel 26 true
TXDP27	N26	LVDS	High-Speed Data Output Channel 27 true
TXDP28	P4	LVDS	High-Speed Data Output Channel 28 true
TXDP29	P28	LVDS	High-Speed Data Output Channel 29 true
TXDP30	P2	LVDS	High-Speed Data Output Channel 30 true
TXDP31	P26	LVDS	High-Speed Data Output Channel 31 true
TXDP32	R4	LVDS	High-Speed Data Output Channel 32 true
TXDP33	R28	LVDS	High-Speed Data Output Channel 33 true
TXDP34	R2	LVDS	High-Speed Data Output Channel 34 true
TXDP35	R26	LVDS	High-Speed Data Output Channel 35 true
TXDP36	T4	LVDS	High-Speed Data Output Channel 36 true
TXDP37	T28	LVDS	High-Speed Data Output Channel 37 true

TXDP38	T2	LVDS	High-Speed Data Output Channel 38 true
TXDP39	T26	LVDS	High-Speed Data Output Channel 39 true
TXDP40	U4	LVDS	High-Speed Data Output Channel 40 true
TXDP41	U28	LVDS	High-Speed Data Output Channel 41 true
TXDP42	U2	LVDS	High-Speed Data Output Channel 42 true
TXDP43	U26	LVDS	High-Speed Data Output Channel 43 true
TXDP44	V4	LVDS	High-Speed Data Output Channel 44 true
TXDP45	V28	LVDS	High-Speed Data Output Channel 45 true
TXDP46	V2	LVDS	High-Speed Data Output Channel 46 true
TXDP47	V26	LVDS	High-Speed Data Output Channel 47 true
TXDP48	W4	LVDS	High-Speed Data Output Channel 48 true
TXDP49	W28	LVDS	High-Speed Data Output Channel 49 true
TXDP50	W2	LVDS	High-Speed Data Output Channel 50 true
TXDP51	W26	LVDS	High-Speed Data Output Channel 51 true
TXDP52	Y4	LVDS	High-Speed Data Output Channel 52 true
TXDP53	Y28	LVDS	High-Speed Data Output Channel 53 true
TXDP54	Y2	LVDS	High-Speed Data Output Channel 54 true
TXDP55	Y26	LVDS	High-Speed Data Output Channel 55 true
TXDP56	AA4	LVDS	High-Speed Data Output Channel 56 true
TXDP57	AA28	LVDS	High-Speed Data Output Channel 57 true
TXDP58	AA2	LVDS	High-Speed Data Output Channel 58 true
TXDP59	AA26	LVDS	High-Speed Data Output Channel 59 true
TXDP60	AB4	LVDS	High-Speed Data Output Channel 60 true
TXDP61	AB28	LVDS	High-Speed Data Output Channel 61 true
TXDP62	AB2	LVDS	High-Speed Data Output Channel 62 true
TXDP63	AB26	LVDS	High-Speed Data Output Channel 63 true
A0	AG6	CMOS	Control (see Pin Definitions)
A1	AF6	CMOS	Control (see Pin Definitions)
A2	AE6	CMOS	Control (see Pin Definitions)
A3	AH6	CMOS	Control (see Pin Definitions)
A4	AJ6	CMOS	Control (see Pin Definitions)
A5	AG7	CMOS	Control (see Pin Definitions)
A6	AF7	CMOS	Control (see Pin Definitions)
A7	AE7	CMOS	Control (see Pin Definitions)
A8	AH7	CMOS	Control (see Pin Definitions)
A9	AJ7	CMOS	Control (see Pin Definitions)
A10	AF24	CMOS	Control (see Pin Definitions)
ALE	AC27	CMOS	Control (see Pin Definitions)
ATM0	E6	CMOS	Test (see Pin Definitions)

ATM1	F3	CMOS	Test (see Pin Definitions)
CKBYP	D6	CMOS	Test (see Pin Definitions)
CLKSEL	F5	CMOS	Control (see Pin Definitions)
CONFIG	AD27	CMOS	Control (see Pin Definitions)
CSB	AJ24	CMOS	Control (see Pin Definitions)
CTM	F4	CMOS	Test (see Pin Definitions)
D0	AD1	CMOS	Control (see Pin Definitions)
D1	AD2	CMOS	Control (see Pin Definitions)
D2	AD5	CMOS	Control (see Pin Definitions)
D3	AD4	CMOS	Control (see Pin Definitions)
D4	AD3	CMOS	Control (see Pin Definitions)
D5	AC1	CMOS	Control (see Pin Definitions)
D6	AC2	CMOS	Control (see Pin Definitions)
D7	AC5	CMOS	Control (see Pin Definitions)
D8	AC4	CMOS	Control (see Pin Definitions)
D9	AC3	CMOS	Control (see Pin Definitions)
FOSYNCN	F27	LVDS	Control (see Pin Definitions)
FOSYNCP	F26	LVDS	Control (see Pin Definitions)
IDDQ1	AC28	CMOS	Test (see Pin Definitions)
IDDQ2	AC29	CMOS	Test (see Pin Definitions)
INTB	AC25	CMOS	Control (see Pin Definitions)
PLOCK	B7	CMOS	Control (see Pin Definitions)
PRTYON	C6	CMOS	Control (see Pin Definitions)
RDB	AH24	CMOS	Control (see Pin Definitions)
RSTB	AC26	CMOS	Control (see Pin Definitions)
SCRMBL	A7	CMOS	Control (see Pin Definitions)
SYNCN	F28	LVDS	Control (see Pin Definitions)
SYNCP	F25	LVDS	Control (see Pin Definitions)
SYSCLKN	F2	LVDS	Control (see Pin Definitions)
SYSCLKP	F1	LVDS	Control (see Pin Definitions)
TACO	F29	CMOS	Test (see Pin Definitions)
TCK	D24	CMOS	JTAG (see Pin Definitions)
TDI	C24	CMOS	JTAG (see Pin Definitions)
TDO	A24	CMOS	JTAG (see Pin Definitions)
TMS	E24	CMOS	JTAG (see Pin Definitions)
TSTRSTB	B24	CMOS	JTAG (see Pin Definitions)
WRB	AE24	CMOS	Control (see Pin Definitions)
VDD	G27	3.3V	Positive Power Supply
VDD	AB27	3.3V	Positive Power Supply

VDD	C22	3.3V	Positive Power Supply
VDD	C21	3.3V	Positive Power Supply
VDD	C20	3.3V	Positive Power Supply
VDD	C19	3.3V	Positive Power Supply
VDD	C18	3.3V	Positive Power Supply
VDD	C17	3.3V	Positive Power Supply
VDD	C16	3.3V	Positive Power Supply
VDD	C15	3.3V	Positive Power Supply
VDD	AA27	3.3V	Positive Power Supply
VDD	C14	3.3V	Positive Power Supply
VDD	C13	3.3V	Positive Power Supply
VDD	C12	3.3V	Positive Power Supply
VDD	C11	3.3V	Positive Power Supply
VDD	C10	3.3V	Positive Power Supply
VDD	AD26	3.3V	Positive Power Supply
VDD	C9	3.3V	Positive Power Supply
VDD	C8	3.3V	Positive Power Supply
VDD	C7	3.3V	Positive Power Supply
VDD	G3	3.3V	Positive Power Supply
VDD	Y27	3.3V	Positive Power Supply
VDD	H3	3.3V	Positive Power Supply
VDD	J3	3.3V	Positive Power Supply
VDD	K3	3.3V	Positive Power Supply
VDD	L3	3.3V	Positive Power Supply
VDD	M3	3.3V	Positive Power Supply
VDD	N3	3.3V	Positive Power Supply
VDD	P3	3.3V	Positive Power Supply
VDD	R3	3.3V	Positive Power Supply
VDD	T3	3.3V	Positive Power Supply
VDD	U3	3.3V	Positive Power Supply
VDD	W27	3.3V	Positive Power Supply
VDD	V3	3.3V	Positive Power Supply
VDD	W3	3.3V	Positive Power Supply
VDD	Y3	3.3V	Positive Power Supply
VDD	AA3	3.3V	Positive Power Supply
VDD	AB3	3.3V	Positive Power Supply
VDD	AG8	3.3V	Positive Power Supply
VDD	AG9	3.3V	Positive Power Supply
VDD	V27	3.3V	Positive Power Supply

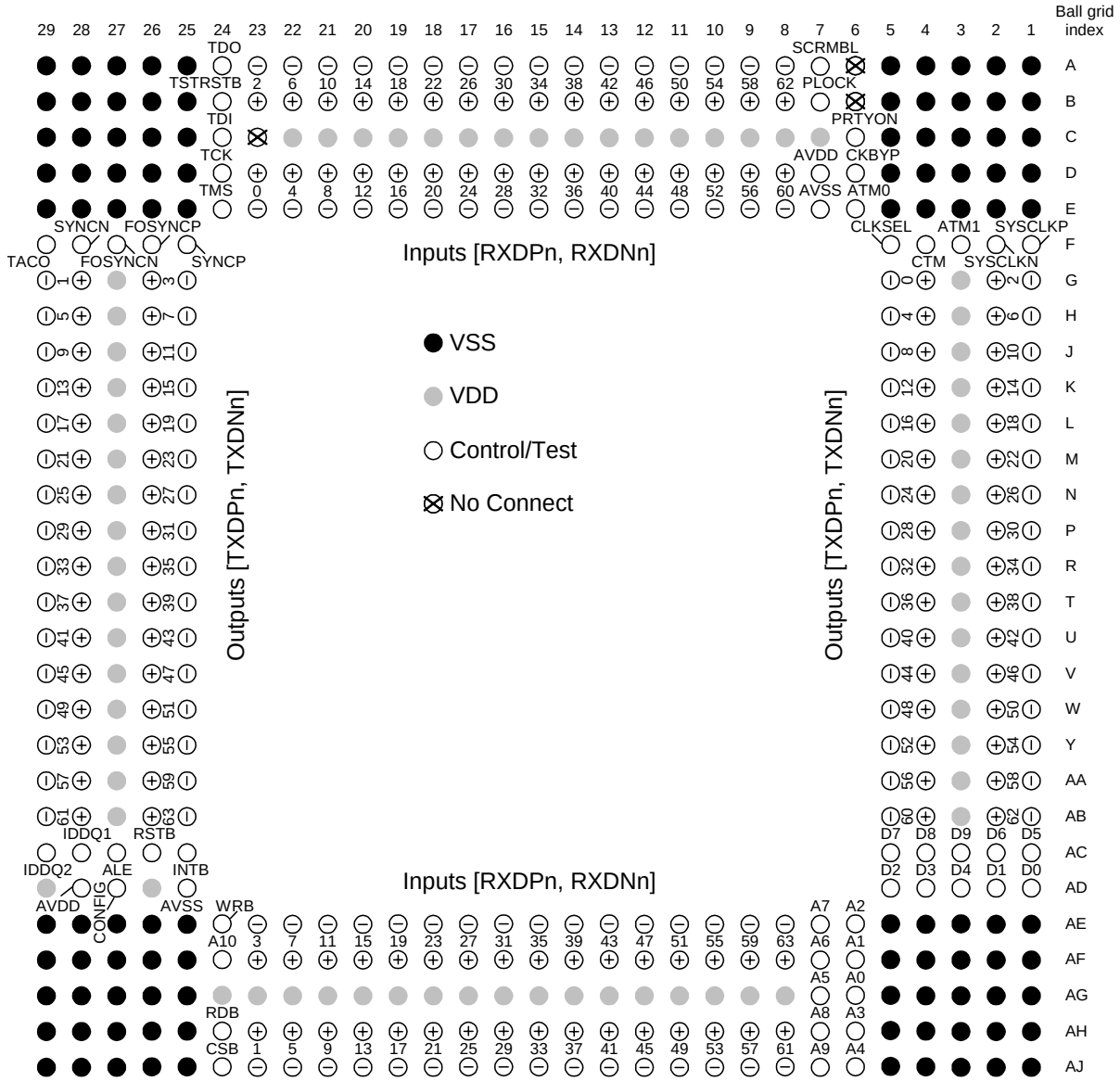
VDD	AG10	3.3V	Positive Power Supply
VDD	AG11	3.3V	Positive Power Supply
VDD	AG12	3.3V	Positive Power Supply
VDD	AG13	3.3V	Positive Power Supply
VDD	AG14	3.3V	Positive Power Supply
VDD	AG15	3.3V	Positive Power Supply
VDD	AG16	3.3V	Positive Power Supply
VDD	AG17	3.3V	Positive Power Supply
VDD	AG18	3.3V	Positive Power Supply
VDD	AG19	3.3V	Positive Power Supply
VDD	U27	3.3V	Positive Power Supply
VDD	AG20	3.3V	Positive Power Supply
VDD	AG21	3.3V	Positive Power Supply
VDD	AG22	3.3V	Positive Power Supply
VDD	AG23	3.3V	Positive Power Supply
VDD	AG24	3.3V	Positive Power Supply
VDD	T27	3.3V	Positive Power Supply
VDD	AD29	3.3V	Positive Power Supply
VDD	R27	3.3V	Positive Power Supply
VDD	P27	3.3V	Positive Power Supply
VDD	N27	3.3V	Positive Power Supply
VDD	M27	3.3V	Positive Power Supply
VDD	L27	3.3V	Positive Power Supply
VDD	K27	3.3V	Positive Power Supply
VDD	J27	3.3V	Positive Power Supply
VDD	H27	3.3V	Positive Power Supply
VSS	A1	GND	Ground
VSS	A2	GND	Ground
VSS	A25	GND	Ground
VSS	A26	GND	Ground
VSS	A27	GND	Ground
VSS	A28	GND	Ground
VSS	A29	GND	Ground
VSS	A3	GND	Ground
VSS	A4	GND	Ground
VSS	A5	GND	Ground
VSS	AE1	GND	Ground
VSS	AE2	GND	Ground
VSS	AE25	GND	Ground

VSS	AE26	GND	Ground
VSS	AE27	GND	Ground
VSS	AE28	GND	Ground
VSS	AE29	GND	Ground
VSS	AE3	GND	Ground
VSS	AE4	GND	Ground
VSS	AE5	GND	Ground
VSS	AF1	GND	Ground
VSS	AF2	GND	Ground
VSS	AF25	GND	Ground
VSS	AF26	GND	Ground
VSS	AF27	GND	Ground
VSS	AF28	GND	Ground
VSS	AF29	GND	Ground
VSS	AF3	GND	Ground
VSS	AF4	GND	Ground
VSS	AF5	GND	Ground
VSS	AG1	GND	Ground
VSS	AG2	GND	Ground
VSS	AG25	GND	Ground
VSS	AG26	GND	Ground
VSS	AG27	GND	Ground
VSS	AG28	GND	Ground
VSS	AG29	GND	Ground
VSS	AG3	GND	Ground
VSS	AG4	GND	Ground
VSS	AG5	GND	Ground
VSS	AH1	GND	Ground
VSS	AH2	GND	Ground
VSS	AH25	GND	Ground
VSS	AH26	GND	Ground
VSS	AH27	GND	Ground
VSS	AH28	GND	Ground
VSS	AH29	GND	Ground
VSS	AH3	GND	Ground
VSS	AH4	GND	Ground
VSS	AH5	GND	Ground
VSS	AJ1	GND	Ground
VSS	AJ2	GND	Ground

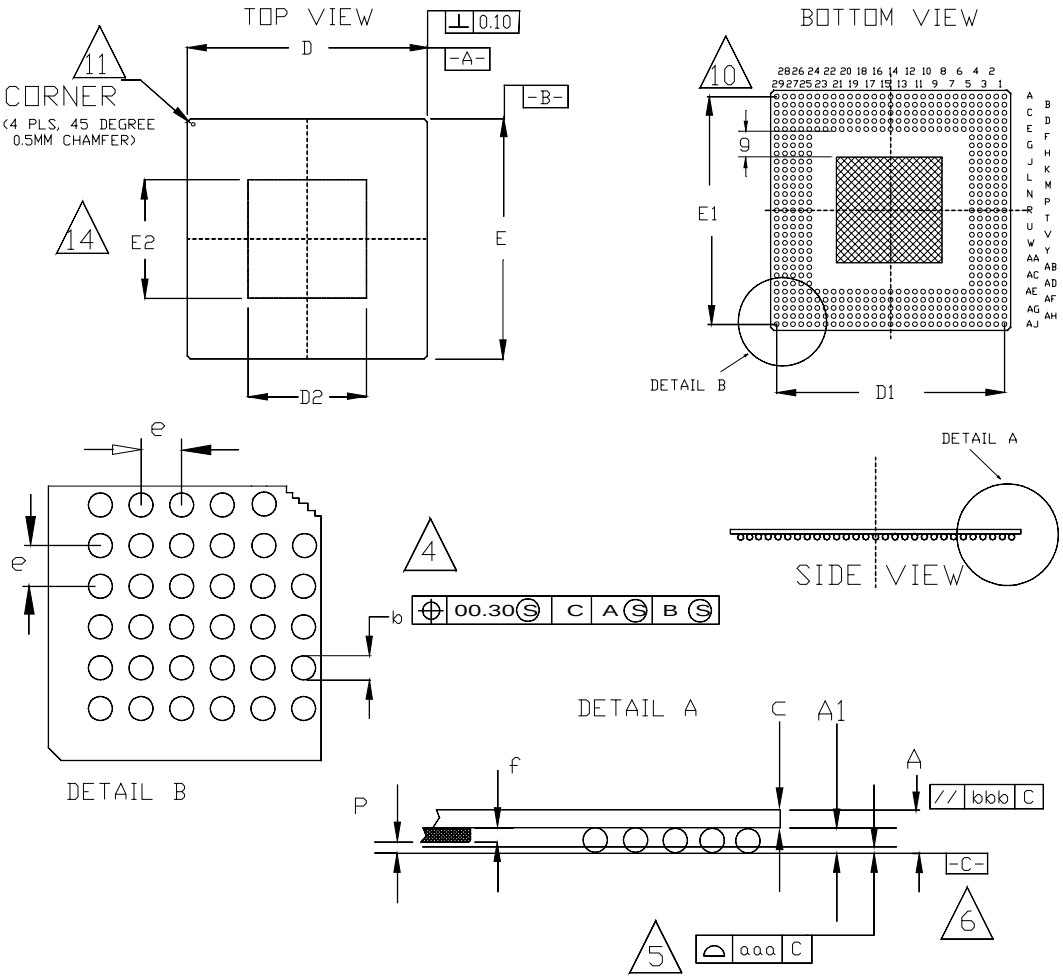
VSS	AJ25	GND	Ground
VSS	AJ26	GND	Ground
VSS	AJ27	GND	Ground
VSS	AJ28	GND	Ground
VSS	AJ29	GND	Ground
VSS	AJ3	GND	Ground
VSS	AJ4	GND	Ground
VSS	AJ5	GND	Ground
VSS	B1	GND	Ground
VSS	B2	GND	Ground
VSS	B25	GND	Ground
VSS	B26	GND	Ground
VSS	B27	GND	Ground
VSS	B28	GND	Ground
VSS	B29	GND	Ground
VSS	B3	GND	Ground
VSS	B4	GND	Ground
VSS	B5	GND	Ground
VSS	C1	GND	Ground
VSS	C2	GND	Ground
VSS	C25	GND	Ground
VSS	C26	GND	Ground
VSS	C27	GND	Ground
VSS	C28	GND	Ground
VSS	C29	GND	Ground
VSS	C3	GND	Ground
VSS	C4	GND	Ground
VSS	C5	GND	Ground
VSS	D1	GND	Ground
VSS	D2	GND	Ground
VSS	D25	GND	Ground
VSS	D26	GND	Ground
VSS	D27	GND	Ground
VSS	D28	GND	Ground
VSS	D29	GND	Ground
VSS	D3	GND	Ground
VSS	D4	GND	Ground
VSS	D5	GND	Ground
VSS	E1	GND	Ground

VSS	E2	GND	Ground
VSS	E25	GND	Ground
VSS	E26	GND	Ground
VSS	E27	GND	Ground
VSS	E28	GND	Ground
VSS	E29	GND	Ground
VSS	E3	GND	Ground
VSS	E4	GND	Ground
VSS	E5	GND	Ground
AVDD1	D7	3.3V	Analog Positive Power Supply
AVDD2	AD28	3.3V	Analog Positive Power Supply
AVSS1	E7	GND	Analog Ground
AVSS2	AD25	GND	Analog Ground
NC1	C23	---	No Connect
NC2	A6	---	No Connect
NC3	B6	---	No Connect

Pin Diagram - Bottom View



Package Information - 37.5mm 480 BGA



DIMENSIONAL REFERENCES			
REF.	MIN.	NOM.	MAX.
A	1.45	1.55	1.65
A1	0.60	0.65	0.70
D	37.30	37.50	37.70
D1	35.56 (BSC.)		
E	37.30	37.50	37.70
E1	35.56 (BSC.)		
b	0.65	0.75	0.85
c	0.85	0.90	0.95
f	0.30	0.35	0.40
M	29		
N	480		
aaa			0.15
bbb			0.15
e	1.27 TYP.		
P	0.15		
9	0.40		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. "e" REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
3. "M" REPRESENTS THE BASIC SOLDER BALL MATRIX SIZE, AND SYMBOL "N" IS THE MAXIMUM ALLOWABLE NUMBER OF BALLS AFTER DEPOPULATING.
4. "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO PRIMARY DATUM -C-
5. DIMENSION "aaa" IS MEASURED PARALLEL TO PRIMARY DATUM -C-
6. PRIMARY DATUM -C- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
7. PACKAGE SURFACE SHALL BE BLACK OXIDE.
8. ENCAPSULANT SIZE MAY VARY WITH DIE SIZE.
9. SUBSTRATE MATERIAL BASE IS COPPER.
10. BILATERAL TOLERANCE ZONE IS APPLIED TO EACH SIDE OF PACKAGE BODY
11. 45 DEG. 0.5 mm CHAMFER CORNER AND WHITE DOT FOR PIN1 IDENTIFICATION.

Thermal Considerations

This package has been enhanced with a copper heat slug to provide a low thermal resistance path from the die to the exposed surface of the heat spreader. The thermal resistance is shown in Table 7.

Table 7: Thermal Resistance

Symbol	*Description*	*°C/W*
θ_{JC}	Thermal resistance from junction-to-case.	0.15
θ_{CA}	Thermal resistance from case-to-ambient with no airflow or heatsink, including conduction through the leads.	7.2

Thermal Resistance with Airflow and Heatsink

It is necessary to use a heatsink with this device. The 37.5mm BGA was selected for its superior thermal performance and commercially available heatsinks. Heatsink vendors typically quote the thermal resistance of their products as a function of airflow. The maximum case temperature of the VSC9182 is 105°C, which requires the following heatsink performance for a given ambient temperature (T_A) environment.

Table 8: Required Heatsink Thermal Resistance

T_A (°C)	θ_{CA} (°C/W)
50	3.4
55	3.1
60	2.8
65	2.5
70	2.2
75	1.9

Please contact your Vitesse Applications Engineer for suggested heatsink solutions.

Ordering Information

The order number for this product is formed by a combination of the device number, and package type.

VSC9182 **XX**

Device Type
VSC9182:
64x64 STS-12/STM-4 TSI Switch Fabric

Package
UG: 480 TBGA, 37.5mm

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