MB86964

ETHERNET CONTROLLER WITH 10BASE-T TRANSCEIVER
PRELIMINARY DATA SHEET

FUJITSU

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FEATURES

- Fully compliant with ISO/ANSI/IEEE 8802-3 specifications
- Provides generic interface to industry-standard microprocessor busses (X86, 680X0 and RISC)
- High-performance packet-buffer architecture pipelines data for highest throughput
- On-chip buffer management controls buffer pointers to reduce software overhead and improve performance
- Hash filter for multicast packet reception
- Power down mode to reduce power dissipation in battery-powered equipment
- Two network ports, AUI and 10BASE-T, with automatic port selection
- Integrated pulse shaper and transmit and receive filters for 10BASE-T
- Automatic polarity detection and correction on twisted-pair cable
- Selectable 150Ω and 100Ω termination for transmitting on shielded or unshielded twisted-pair cable, respectively
- Low-power CMOS technology
- Single 5-volt power supply
- 100-pin plastic shrink quad flat package (SQFP100)

GENERAL DESCRIPTION

The MB86964 is a high-performance, highly integrated single-chip device that incorporates a network controller with buffer management, Manchester encoder/decoder, 10BASE-T transceiver with on-chip transmit and receive filters, and generic bus interface for industry-standard microprocessor busses. The MB86964 allows implementation of adapter solutions with a minimum of additional support chips. Its generic bus interface makes it ideal for use on daughter and motherboards, as well as VESA Local Bus (VL Bus). It also can be easily integrated onto device controller and communication boards as an embedded LAN adapter.

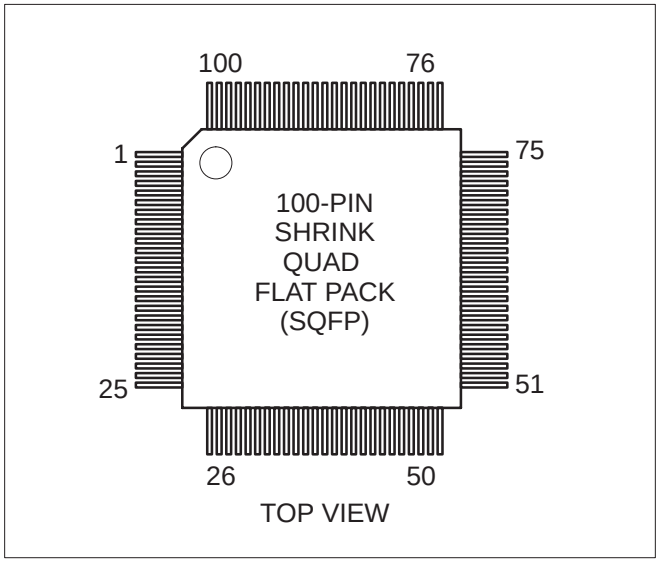
The buffer management architecture of the MB86964 allows packet data to flow through an external SRAM buffer memory acting as an elastic buffer. On-chip FIFOs, together with the SRAM buffer, pipeline both transmit and receive packets through the system for maximum performance and minimum overhead to the host microprocessor. All receive and transmit pointers are managed automatically by the device to reduce software overhead and increase packet processing speed. The MB86964's transmit buffer is programmable as a single 2-kbyte bank or as two banks of 2, 4, or 8 kbytes each. These buffers can store multiple data packets, allowing the MB86964 to transmit all of them following a single transmit command, thereby offering greater design flexibility and throughput. A ring buffer that can be sized from 4 to 30 kbytes, depending on the size of the SRAM, acts as a large elastic FIFO buffer to capture the bursts of receive packets.

The MB86964 performs pulse shaping and filtering internally, which eliminates the need for external filtering components and reduces overall system cost. The twisted pair interface is compatible with shielded and unshielded cables and provides outputs for transmit, collision and link test LED indicators. The twisted pair receive threshold can be reduced to allow an extended range between nodes in low-noise environments. Its wide range of features makes the MB86964 the ideal device for 10BASE-T twisted-pair Ethernet applications.

Possible configurations for the system bus interface include I/O mapping, memory mapping and DMA access, or a combination of these. With a 20 Mbyte/s bandwidth, the MB86964 system bus interface allows use of full throughput capacity of its packet-buffering architecture. The MB86964's bus modes are programmable, thereby providing 8- or 16-bit data path width and big or little endian byte-ordering, permitting efficient data interface with most microprocessors and higher-level protocols.

The MB86964, which is furnished in a space-efficient 100-pin plastic shrink quad flat package, is fabricated using Fujitsu's high-speed, low-power CMOS process.

PIN CONFIGURATION



LOGIC CONVENTION

Unless otherwise noted, a positive logic (active high) convention is assumed throughout this document, whereby the presence at a pin of a higher, more-positive voltage (nominally 5 VDC) causes assertion of the signal. An overbar, e.g., $\overline{RDY}$, indicates that the signal is asserted in the low state (nominally 0 volts). Dual-function pins have their alternate function enclosed in parentheses, e.g., RDY($\overline{RDY}$). Whenever a signal is separated into numbered bits, e.g., BD7, BD6, BD5, BD4, BD3, BD2, BD1 and BD0, the family of bits may also be shown collectively, e.g., as BD<7:0>.

PIN ASSIGNMENTS

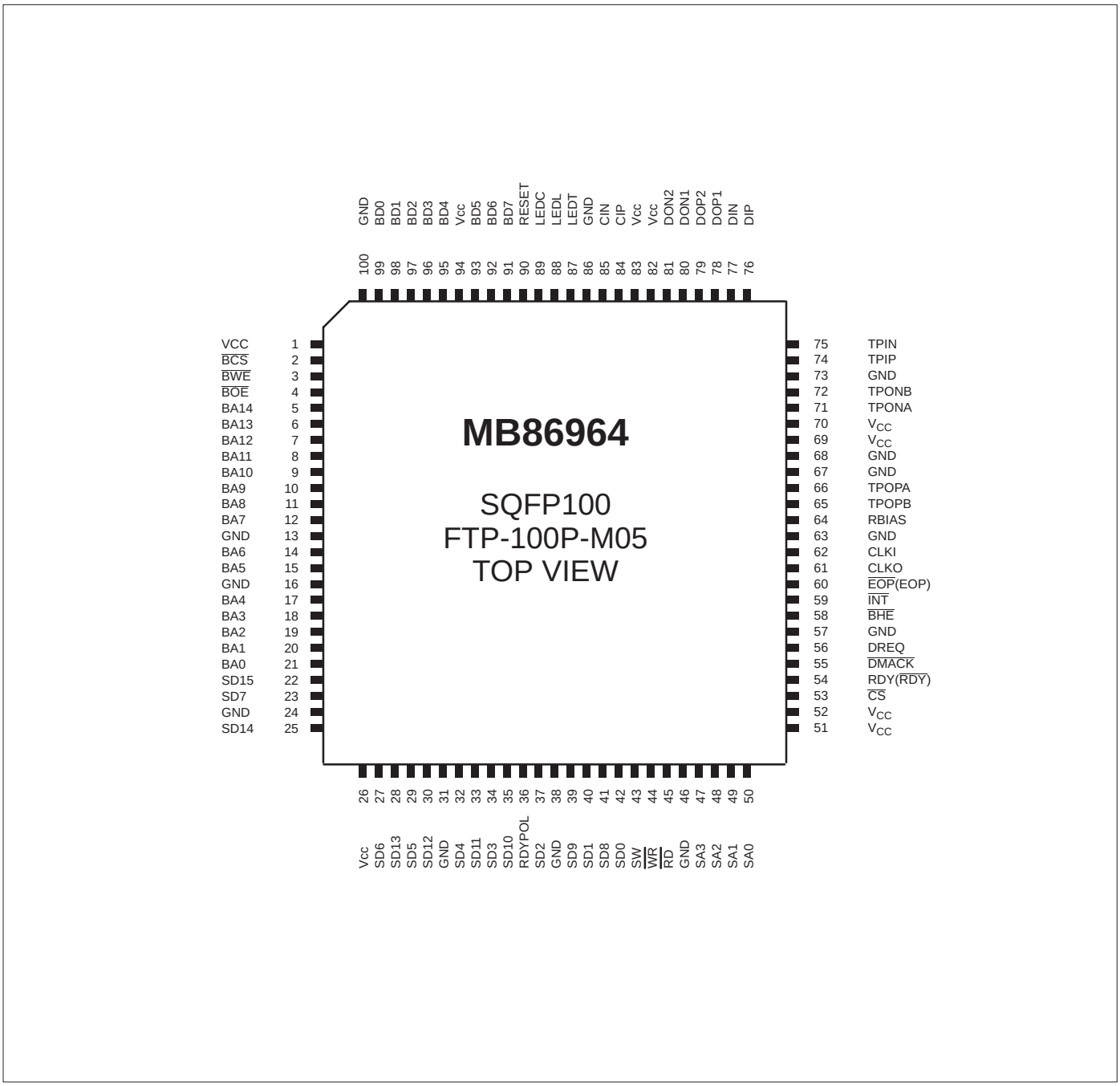


Figure 1. MB86964 Pin Assignments

PIN DESCRIPTIONS

System Bus Interface Pins

PIN NO.	SYMBOL	TYPE	DESCRIPTION
22, 25, 28, 30, 33, 35, 39, 41, 23, 27, 29, 32, 34, 37, 40, 42	SD<15:0>	I/O	**SYSTEM DATA:** All data, command, and status transfers take place over this bus.
47-50	SA<3:0>	I	**SYSTEM ADDRESS**: Selects an internal register or port for read/write operations.
58	$\overline{BHE}$	I	**BUS HIGH ENABLE:** Active low. This pin is the byte/word control line. It is used only when the MB86964 is configured for a 16-bit data bus by the SB/$\overline{SW}$ bit, DLCR6<5>. It allows word, upper byte only or lower byte only transfers. Address pin SA0 is used with $\overline{BHE}$ for byte or word transfers as follows:

SB/$\overline{SW}$	$\overline{BHE}$	SA0	FUNCTION
0	0	0	Word transfer
0	0	1	Byte transfer on upper half of data bus (SD15-8)
0	1	0	Byte transfer on lower half of data bus (SD7-0)
0	1	1	Reserved
1	X	X	Byte transfer (SD7-0)

53	$\overline{CS}$	I	**CHIP SELECT**: Active low signal used to select the MB86964.
90	RESET	I	**CHIP RESET:** Resets the chip's buffer memory pointers and initializes internal registers and logic.
45	$\overline{RD}$	I	**READ STROBE:** Active low signal from the system bus which indicates that the current bus cycle is a read operation.
44	$\overline{WR}$	I	**WRITE STROBE:** Active low signal from the system bus which indicates that the current bus cycle is a write operation.
56	DREQ	O	**DMA REQUEST:** Issued to the external DMA controller to indicate that the MB86964 is ready to transfer data. Used for both read and write operations.
60	$\overline{EOP}$(EOP)	I	**END OF PROCESS:** When asserted by the DMA controller, indicates that the current DMA process has completed. Asserted state is programmed via DLCR7<1>. See also DCLR4<2>.
55	$\overline{DMACK}$	I	**DMA ACKNOWLEDGE:** Active low signal which indicates that the DMA controller is ready to transfer data between the host system and the MB86964's buffer memory.
59	$\overline{INT}$	O	**INTERRUPT REQUEST:** Active low signal indicates that the MB86964 requires host attention after successful transmission or reception of a packet, after the completion of a DMA cycle, or if any error conditions occur.
54	RDY($\overline{RDY}$)	O	**READY:** This signal indicates to the host that MB86964 is ready to complete the requested read or write operation. The asserted state of this pin is programmed by RDYPOL, pin 36.
43	SW	O	**SYSTEM WORD BUS WIDTH:** When low, the system bus interface is programmed to operate in 8-bit mode; when high,16-bit mode is selected. Inverse of the value programmed in DLCR6<5>.
36	RDYPOL	I	**READY LINE POLARITY SELECT:** Controls asserted state of the RDY($\overline{RDY}$) signal at pin 54, where low selects active low READY ($\overline{RDY}$) and high selects active high READY (RDY).

Buffer Memory Interface Pins

PIN NO.	SYMBOL	TYPE	DESCRIPTION
91-93, 95-99	BD<7:0>	I/O	**BUFFER MEMORY DATA BUS:** Data lines between the SRAM buffer memory and the MB86964.
5-12, 14, 15, 17-21	BA<14:0>	O	**BUFFER MEMORY ADDRESS BUS:** These lines address up to 32 kbytes of buffer memory.
2	$\overline{BCS}$	O	**BUFFER RAM CHIP SELECT:** Active low signal that is the chip select for the buffer memory.
3	$\overline{BWE}$	O	**BUFFER WRITE ENABLE:** Active low write enable signal generated during buffer memory write cycles.
4	$\overline{BOE}$	O	**BUFFER OUTPUT ENABLE:** Active low output enable signal generated during buffer memory read cycles.

Power and Transceiver Interface Pins

PIN NO.	SYMBOL	TYPE	DESCRIPTION
1, 26, 51, 52, 69, 70, 82, 83, 94	V_{CC}	I	**POWER SUPPLY**: +5 Volts ± 5%, for analog and digital circuits.
13, 16, 24, 31, 38, 46, 57, 63, 67, 68, 73, 86, 100	GND	I	**GROUND**: Digital and analog ground.
78, 79 80, 81	DOP1, 2 DON1, 2	O O	**AUI TRANSMIT PAIR:** A differential output driver pair for the AUI transceiver DO circuits; output is Manchester-encoded. DOP1 should be tied to DOP2 and DON1 should be tied to DON2 on the circuit board.
76 77	DIP DIN	I I	**AUI RECEIVE PAIR:** A differential input driver pair for the AUI transceiver DI circuits; input is Manchester-encoded.
84 85	CIP CIN	I I	**AUI COLLISION PAIR:** A differential input driver pair for the AUI transceiver CI circuits. The input is collision signalling or signal-quality error (SQE).
66, 65 71, 72	TPOPA, B TPONA, B	O O	**TWISTED-PAIR OUTPUTS:** Differential driver output pairs to the twisted-pair cable. The output is pre-equalized so that no external filter is required.
74 75	TPIP TPIN	I I	**TWISTED-PAIR INPUT:** A differential input pair from the twisted-pair cable.
89	LEDC	O	**COLLISION LED:** Open-drain driver for the collision indicator. Output is pulled low during collision.
88	LEDL	I/O	**LINK LED:** Open-drain driver for ”link test pass” LED. Output pulls low during link test pass. If externally tied low, forces internal circuitry to ”Link Pass” state.
87	LEDT	O	**TRANSMIT LED:** Open-drain driver for the transmit indicator. Output is pulled low during transmit.
64	RBIAS	I	**BIAS RESISTOR**: Controls the bias of the operating circuit; connect to ground via a 12.4kΩ ±1% resistor.
61* 62*	CLKO CLKI	O I	**CRYSTAL OSCILLATOR:** A 20-MHz crystal must be connected between these pins. (See figure 4.)

* CLKO: Leave unconnected if an external clock is used
CLKI: Input for an external 20MHz clock source

FUNCTIONAL DESCRIPTION

The MB86964 comprises five major functional blocks: system interface, buffer controller, transmitter, receiver and control and status registers, as illustrated in Figure 2. The MB86964's receive and transmit sections fully implement the ISO/ANSI/IEEE 8802-3 CSMA/CD specification for 10 megabit per second Ethernet. The transmitter assembles data packets for transmission and the receiver disassembles received data packets. On-chip Ethernet protocol functions include: automatic generation and stripping of the 64-bit preamble, generation and verification of 32-bit cyclic redundancy check (CRC), collision resolution by binary exponential backoff and retransmission, several modes of address recognition, error detection and reporting, and serial/parallel and parallel/serial conversions.

TYPICAL APPLICATION

Figure 3 is a block diagram illustrating use of the MB86964 in an embedded Ethernet adapter application. One or two 8-bit bidirectional transceivers (if required) provide data buffering between the MB86964 and the 8- or 16-bit system bus. A single 8 or 32 kbyte SRAM implements the local packet buffer. The MB86964 provides interfaces to 100- or 150-ohm twisted pair (10BASE-T) as well as direct AUI capability (10BASE5). An optional coaxial transceiver interface provides additional capability for Thin Ethernet (10BASE2) networks. The MB86964 directly drives three LEDs which provide indication of operational status.

As shown in the typical application, the MB86964 allows a highly integrated system configuration. The MB86964's architecture and high level of integration facilitate packet management and storage, and eliminate the need for a local microprocessor. The MB86964 connects with the host system bus to provide command and status interfaces as well as packet data access. The host processor can directly access command and status registers mapped into the host I/O or memory space. Data packets to be transmitted to the network initially transfer from host memory through a register in the MB86964 into the dedicated buffer memory where they are temporarily stored until transmitted. Buffer memory initially stores received data packets that are later transferred to the host memory.

For detailed design information on a typical adapter board application, refer to the Hardware Reference Manual included in the DK86964 Designer's Kit which is available for purchase from your authorized Fujitsu Microelectronics sales representative or distributor. Please check the "How to Buy" section @ www.fujitsumicro.com/buy/buy.html or contact the Customer Response Center @ 1–800–866–8608 for more details.

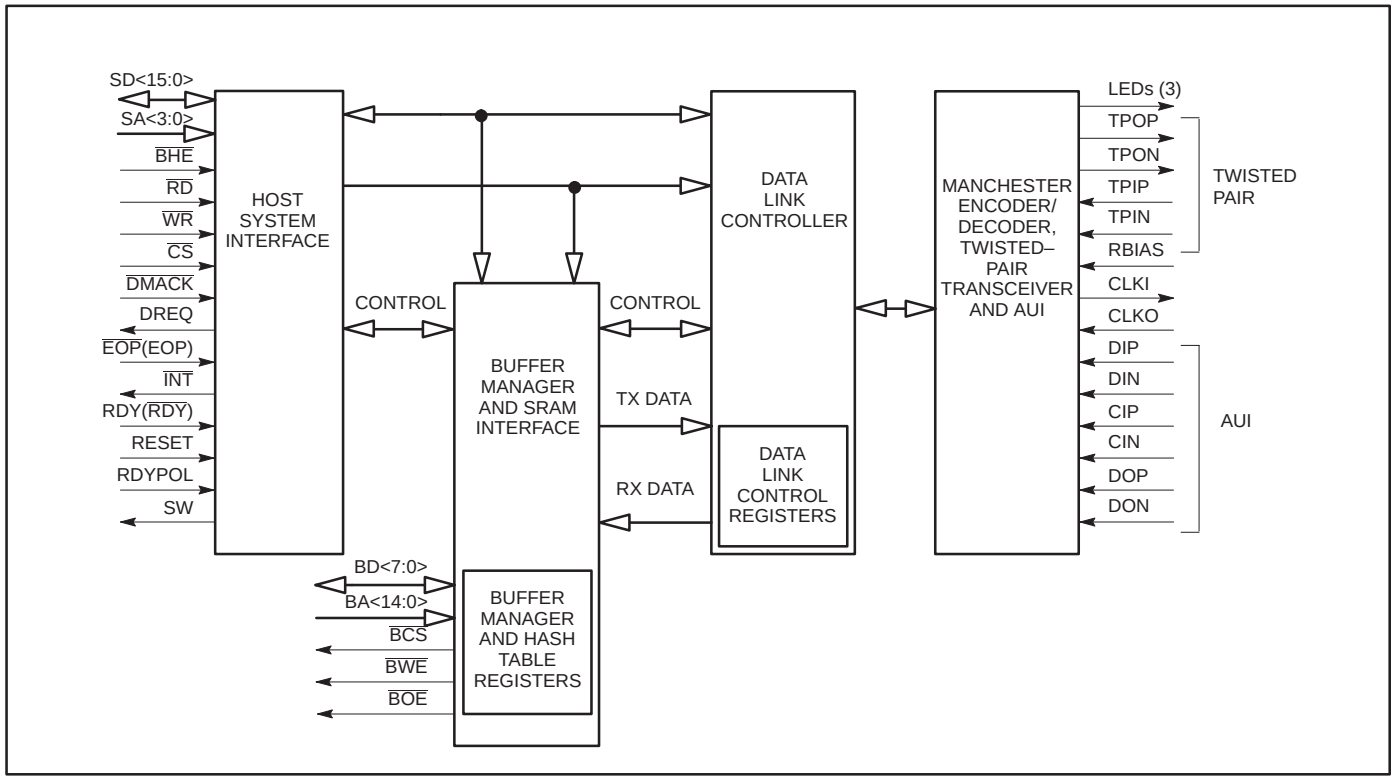


Figure 2. MB86964 Block Diagram

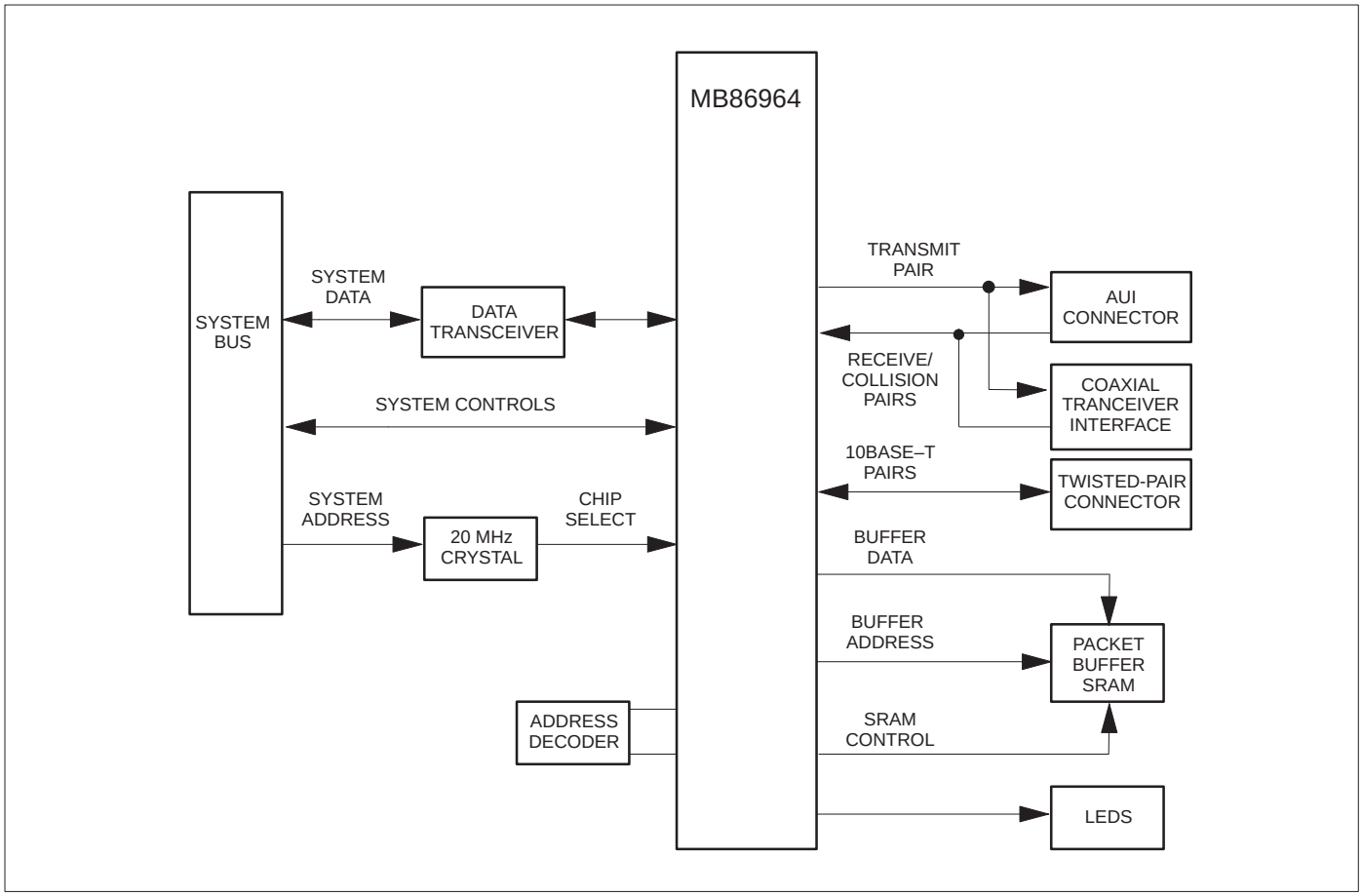


Figure 3. Typical Application, Block Diagram

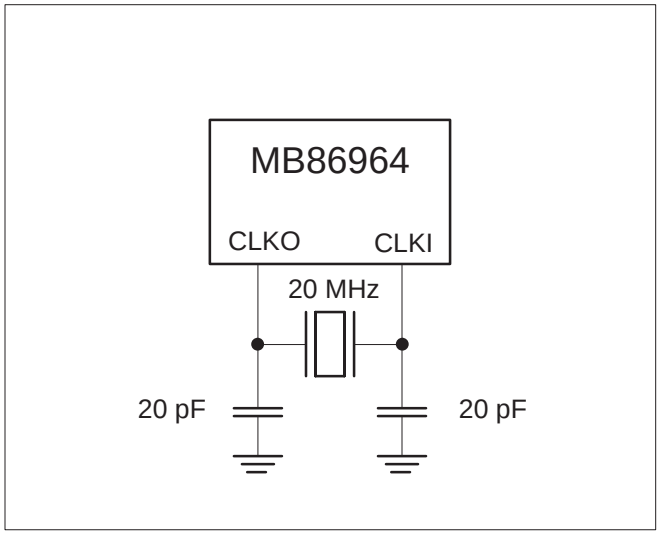


Figure 4. Crystal Oscillator Connection

CRYSTAL OSCILLATOR

The clock rate of 10 Mbits/s specified by the international LAN standard, ISO/ANSI/IEEE 8802-3, is derived from an on-chip oscillator that is controlled by a 20 MHz crystal connected across pins 61 and 62 (CLKO and CLKI). Capacitance specified by the crystal manufacturer must be connected as shown in Figure 4 to stabilize the effects of stray capacitance that may vary crystal frequency. The 20 MHz clock also serves as an internal phase-locked loop (PLL) reference for decoder clock recovery. Internal clocks shut down when the $\overline{\text{PWRDN}}$ bit, DLCR7<5>, is asserted for power down mode.

Use a crystal with the following specifications: quartz (AT-cut); 20-MHz; frequency acurracy of ±50ppm at 25° C and ±100ppm at 0°C to 70°C; parallel resonant with 20 pF-load in fundamental mode. Possible vendors include: Ecliptek Corp. (Costa Mesa, CA), p/n ECSM 20.000M; and M-tron Industries, Inc. (Yankton, SD), p/n MP-1 and MP-2.

LOCAL BUFFER CONFIGURATIONS

The MB86964 is designed to operate with local buffer which holds packets received from the host processor prior to transmission and assembles packets received from the network before they are delivered to the host processor. The buffer is implemented by using a single byte-wide SRAM whose size is selected via DLCR6<1> as 8 kbytes (DLCR6<1> = 0) or 32 kbytes DLCR6<1> = 1).

See Buffer Access section for information on how the host accesses the buffer memory.

POWER DOWN MODE

When the MB86964 is not in use, the power down feature reduces power consumption by shutting off all internal clocks. This feature is invoked by first setting the $\overline{\text{DLC\_EN}}$ bit, DLCR6<7>, high, thus disabling the receiver and transmitter, and then by setting the $\overline{\text{PWRDN}}$ bit, DLCR7<5>, low. The power down mode terminates by setting the $\overline{\text{PWRDN}}$ bit high (writing a one to DLCR7<5>) or by performing a hardware reset. Contents of all registers are maintained during power down and remain unchanged, except if power down mode is terminated by a hardware reset.

SYSTEM INTERFACE

General

The system interface provides the interface logic necessary to connect to an x86, RISC or 680X0-type microprocessor bus. The interface supports 8- and 16-bit bus widths and byte or word transfers. The data path width between the host and the MB86964 is controlled via DLCR6<5>. When this bit is a '1', the system bus interface is programmed to operate in 8-bit mode; when it is a '0', 16-bit mode is selected. The inverse of the programmed value appears at pin 43, SW. The interface defaults to 8-bit mode after a hardware reset, thus initial access to the chip must utilize 8-bit data transfers. The data is supplied MSB or LSB first (big or little endian), according to the setting of the M..L/$\overline{\text{L..M}}$ bit, DLCR7<0>. The setting of this bit only affects data transfers between the host and the buffer memory; data transfers between the host and the other MB86964 registers are not affected by the setting of the M..L/$\overline{\text{L..M}}$ bit. The MB86964 supports I/O-mapped operation and burst or single-transfer DMA modes. An interrupt request output, pin 59, informs the CPU of transmit and receive status conditions requiring host processing.

Byte-Order Control

Byte-order control provided by Most..Least/Least..Most bit, DLCR7<0>, provides compatibility with various higher-level protocols, such as TCP/IP and XNS. These protocols may have a different order for transmission of the bytes within a word. When M..L/$\overline{\text{L..M}}$ is low, the least-significant byte of the word transmits first, followed by the most-significant. When M..L/$\overline{\text{L..M}}$ is set high, the byte order reverses. This feature applies only when the system bus operates in 16-bit (word) mode.

The byte-order control works by reversing, or not reversing, the bytes of all words as they pass between the buffer memory and the system bus. Thus all data stored in the transmit buffer or retrieved from the receive buffer is affected, including non-transmitted headers. This control bit does not affect the MB86964 registers other than the Buffer Memory Port registers, BMPR8 and BMPR9. When using this feature, ensure the reversal of header information as well as packet data in the software driver code. See Table 1 for examples of using least..most and most..least byte ordering.

Register Access

The MB86964 includes four sets of user-accessible registers, all of which are accessible as bytes or words. Each register set contains eight registers.

Direct access is available to two sets of registers in the device's register set at a time, via register addresses 00H through 0FH. The Data Link Control Registers set (DLCR0 - DLCR7) is always accessible via addresses 00H to 07H. Access to one of the remaining three sets is accomplished by programming the register bank select bits, DLCR7<3:2>. This selects the register set accessible via addresses 08H to 0FH. The bank-switched registers are the Node ID set , DLCR7 - DLCR15, (for setting the Ethernet Address and performing TDR diagnostics), the Hash Table set, HT8 - HT15, (for setting up multicast address filtering) and the Buffer Memory Port set, BMPR7 - BMPR15. During operation (excluding initialization or diagnostics), the Buffer Memory Port set should normally be selected.

Table 1. Byte Ordering

DATA <15:8>	DATA <7:0>
FOR TRANSMIT PACKET	
LEAST. . . . MOST	
Transmit Length, high byte	Transmit Length, low byte
Destination Address, 2nd byte	Destination Address, 1st byte
Source Address, 2nd byte	Source Address, 1st byte
Length Field, low byte*	Length Field, high byte*
Data Field, 2nd byte	Data Field, 1st byte
MOST . . . . LEAST	
Transmit Length, low byte*	Transmit Length, high byte*
Destination Addr, 1st byte	Destination Addr, 2nd byte
Source Addr, 1st byte	Source Addr, 2nd byte
Length Field, high byte	Length Field, low byte
Data Field, 1st byte	Data Field, 2nd byte
FOR RECEIVE PACKET	
LEAST. . . . MOST	
Unused, reserved	Receive Packet Status
Receive Length, high byte	Receive Length, low byte
Destination Address, 2nd byte	Destination Address, 1st byte
Source Address, 2nd byte	Source Address, 1st byte
Length Field, low byte*	Length Field, high byte*
Data Field, 2nd byte	Data Field, 1st byte
MOST . . . . LEAST	
Receive Packet Status	Unused; reserved
Receive Length, low byte*	Receive Length, high byte*
Destination Addr, 1st byte	Destination Addr, 2nd byte
Source Addr, 1st byte	Source Addr, 2nd byte
Length Field, high byte	Length Field, low byte
Data Field, 1st byte	Data Field, 2nd byte

Items shown with an astertisk are in numerically reversed byte order

Buffer Access

The Buffer Memory Port register pair BMPR8 and BMPR9 provide 8- or 16-bit data access to the receive and transmit buffers through on-chip FIFOs. To eliminate the need for complicated directional control, FIFOs are dedicated to each direction of data transfer. Writing to the transmit buffer can be interleaved with reading from the receive buffer, with the MB86964 automatically maintaining buffer memory pointers, thus relieving the host of that task. The Buffer Memory port register pair is at address 08H when DLCR7<3:2> are programmed to ’10’ to select the Buffer Memory Port register set. When using DMA, the buffer memory port is automatically selected when the DMA Acknowledge input, $\overline{\text{DMACK}}$, is asserted. The host accesses are byte-wide when the system is configured for byte-wide operation and word-wide when the system interface is configured for word-wide operation. In the latter mode, byte-wide access to the buffer memory port is not supported.

Data can transfer from the host memory to the transmit buffer, or from the receive buffer to host memory by using string moves, single-transfer programmed I/O moves, or DMA. Select the method that yields the highest system-level efficiency. A rapid transfer process results in best performance. Slow transfer can result in poor throughput and performance, and cause the receive buffer to overflow and lose packets.

DMA Operation

The MB86964 supports single-cycle and burst DMA operation for data transfers between the host and the packet buffer. Handshaking between the MB86964 and the external DMA controller is accomplished by the DREQ and $\overline{\text{DMACK}}$ signals. The end of process input, pin 60, when asserted by the system DMA controller during a transfer cycle, terminates DMA activity

after completion of the current cycle. If a DMA interrupt (DLCR3<5>) is enabled, the MB86964 generates an interrupt after completion of DMA activity.

Usually only one DMA operation will be run at a time, although the MB86964 could run two interleaving operations, one reading and one writing. There is only one DMA EOP bit, and only one DREQ pin and one $\overline{\text{DMACK}}$ pin, so most hosts could not support more than one DMA operation at a time.

DMA Write (Transmit)

Setting the TX DMA Enable bit, BMPR12<0>, enables DMA transfer of data packets from the host memory to the MB86964 transmit buffer. The DMA burst control bits, BMPR13<1:0>, set the maximum number of data transfer cycles (bytes or words) in a single bus acquisition to be 1, 4, 8, or 12. The MB86964, when ready to accept data from the host, sets the DMA request output, DREQ, and the host responds by asserting DMA acknowledge, $\overline{\text{DMACK}}$, followed by Write Strobe, $\overline{\text{WR}}$, and placing data on the data bus. The MB86964 asserts the RDY($\overline{\text{RDY}}$) output when ready to complete the current data-transfer cycle. (The assertive states of the RDY($\overline{\text{RDY}}$) output and the EOP($\overline{\text{EOP}}$) input are independently programmable.) The MB86964 accepts the data byte/word into its bus write FIFO and later moves it into buffer memory. At the close of a transfer cycle, the host negates $\overline{\text{WR}}$. In burst mode and depending on the value of the $\overline{\text{DREQ EXTND}}$ bit, DLCR4<2>, the MB86964 negates DREQ at the next-to-last or last transfer cycle of the burst. The host DMA then completes the last one or two transfer cycles and negates $\overline{\text{DMACK}}$ to terminate the burst. To start another burst, the MB86964 reasserts DREQ.

The DMA controller asserts the end of process input, EOP($\overline{\text{EOP}}$), concurrent with the last required data-transfer cycle to indicate completion of the entire transfer process. This action sets the DMA EOP status bit, DLCR1<5>, and discontinues further data requests from the MB86964. The MB86964 will also generate an interrupt if the DMA EOP interrupt enable bit, DLCR3<5>, is high. The host can use this interrupt to begin action to close the process. The host should reset the MB86964 DMA logic and clear the interrupt by writing 00H to BMPR12.

Note: DMA EOP, DLCR1<5> must be cleared to close the transmit DMA process before attempting another DMA process. This is accomplished by writing 00H to BMPR12. When this is done, the DMA EOP bit will clear automatically, clearing the EOP status and interrupt, (if enabled) so it is not necessary to clear the interrupt separately.

After finishing the loading of packets into the buffer, the host initiates packet transmission. This is done by loading the number of packets to be transmitted into the Transmit Start Register, BMPR10<6:0>, and asserting the Transmit Start bit, TX START, of the same register, BMPR10<7>.

DMA Read (Receive)

The MB86964 indicates that it has received packets and stored them in the packet buffer with status bits or interrupts. Before attempting to transfer a packet from the buffer, the host processor should read the RX BUF EMPTY bit, DLCR5<6>. If this bit is 0, there are one or more packets ready for transfer in the receive buffer. After reading each packet, the host will check this bit again to see if there are more.

Prior to beginning the transfer of a packet from the receive buffer to host memory via DMA, the host must first read the four-byte receive packet header from the buffer to obtain the packet status and the length of the packet in bytes. Calculating from the packet length the number of DMA cycles needed to read the packet, the host will load that number into the cycle counter of the host DMA controller. Next, RX DMA EN, BMPR12<1>, is set to high to enable DMA read operation to transfer the packet to host memory. The DMA burst control bits, BMPR13<1:0>, set the maximum number of data transfer cycles (bytes or words) in a single bus acquisition to be 1, 4, 8, or 12. When it is ready to begin, the MB86964 asserts its DMA Request output, DREQ. The host responds by asserting DMA Acknowledge, $\overline{\text{DMACK}}$, followed by the Read Strobe, $\overline{\text{RD}}$. The MB86964 will assert its RDY($\overline{\text{RDY}}$) output when it has placed the byte/word on the data bus and is ready to complete the data transfer cycle. The system memory will accept the data, then the host negates $\overline{\text{RD}}$. The MB86964 shifts the data down in its bus read FIFO, then moves its internal read pointer to point to the next byte/word in the buffer, moving it into the FIFO.

In burst mode and depending on the value of the $\overline{\text{DREQ EXTND}}$ bit, DLCR4<2>, the MB86964 negates DREQ at the next-to-last or last transfer cycle of the burst. The host DMA then completes the last one or two transfer cycles and negates $\overline{\text{DMACK}}$ to terminate the burst. The MB86964 reasserts DREQ to repeat the process if it can transfer more data after the host negates $\overline{\text{DMACK}}$. The DMA controller asserts the end of process input, EOP($\overline{\text{EOP}}$) concurrent with the last byte/word data transfer to indicate completion of the entire process. The MB86964 then stops requesting more DMA cycles.

When EOP($\overline{\text{EOP}}$) is asserted by the host DMA controller, the DMA EOP bit, DLCR1<5>, will be set high, and an interrupt will also be generated, provided it is enabled by a high in the associated interrupt enable bit, DLCR3<5>. This interrupt can be used by the host to initiate the final actions to close the DMA process. The interrupt is cleared and the DMA is disabled and reset by writing 00H to the DMA Enable Register, BMPR12.

Note: Clearing RX DMA EN must be done to close the receive DMA process before attempting another DMA process. This is accomplished by writing 00H to BMPR12. When this is done, the DMA EOP bit will clear automatically, clearing the EOP status and interrupt, so it is not necessary to clear the interrupt separately.

After completion of the DMA process, RX DMA EN must be reasserted when the host wants to begin reading another packet from the receive buffer by using DMA.

BUFFER CONTROLLER

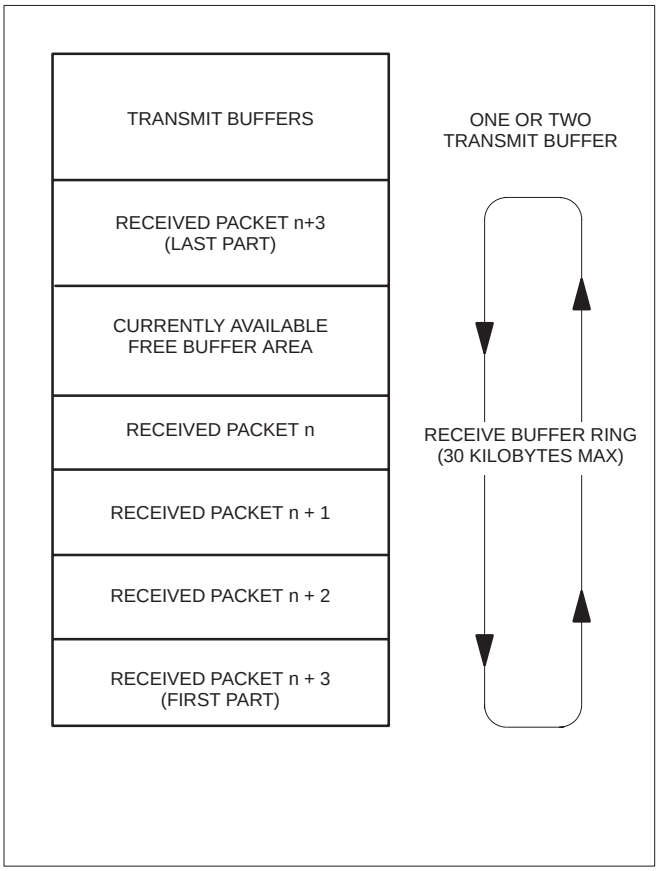


Figure 5. Buffer Memory Organization

General

The MB86964 uses a dedicated buffer memory, organized as shown in Figure 5, for intermediate storage of packets to be transmitted, and of packets received from the network. The MB86964 can operate with 8 or 32 kilobytes of total buffer memory, including both transmit and receive spaces. Memory partitioning into transmit and receive sections is controlled by the system software. The total size of the transmit buffer space can be up to 16 kilobytes. The buffer memory not used for the transmitter is used for the receiver, and is automatically configured as a ring buffer. Packets are stored head-to-toe in the receive buffer, as they are in the transmit buffer. However, each packet in the receive buffer is aligned on an eight-byte boundary. As packets are being stored in the receive buffer, as the end of the linear addressing space is reached, the chip's receive write pointer automatically wraps around to the top of the receive addressing range to make a seamless ring. The receive read pointer does the same as the packets are read out to the system. By programming the sizes allocated to transmit and receive buffers, an optimum usage of the memory can be selected according to the demands of a particular application.

The buffer controller keeps track of buffer memory partitioning and allocation and updates internal address pointers automatically for the tasks of transmit, retransmit, receive, rejection of packets with errors and data transfers to and from the host. The host and its drivers are thus relieved of buffer management functions, making the MB86964 easy to operate and substantially reducing software requirements. Packets with errors are normally automatically rejected by the MB86964 as are packets shorter than the IEEE minimum length packet of 60 bytes, excluding Preamble and CRC. Since these tasks can be done faster in hardware than in software, this not only off-loads the host system, but it also speeds up the communication processes, yielding higher throughput. As a result, the MB86964 can typically win benchmark performance tests over competing controllers.

Arbitration of Buffer Access

The buffer controller automatically prioritizes and services requests for access to memory from the transmitter, receiver and host system. The MB86964's arbitration mechanism, illustrated in Figure 6, interleaves accesses to the buffer memory so that the operation appears to be simultaneous: data can be written to or read from the buffer memory by the host via Buffer Memory Port Register 8 (BMPR8), while data is being read from the buffer by the transmitter and/or written in for storage by the receiver. Each interface, whether host system or network access, appears to be served independently by the controller. Each interface has an associated FIFO to provide time for the buffer interleaving. Thus, packet data is pipelined through the system for highest performance and throughput, and the buffer controller supports all the cases of simultaneous access to the buffer memory as follows:

1. Data from the network is stored in the receive buffer.
2. The host retreives packets from the receive buffer.
3. The host loads packet data into the transmit buffer.

4. The transmitter obtains data for transmission from the transmit buffer.

5. Any combination of the above can occur concurrently.

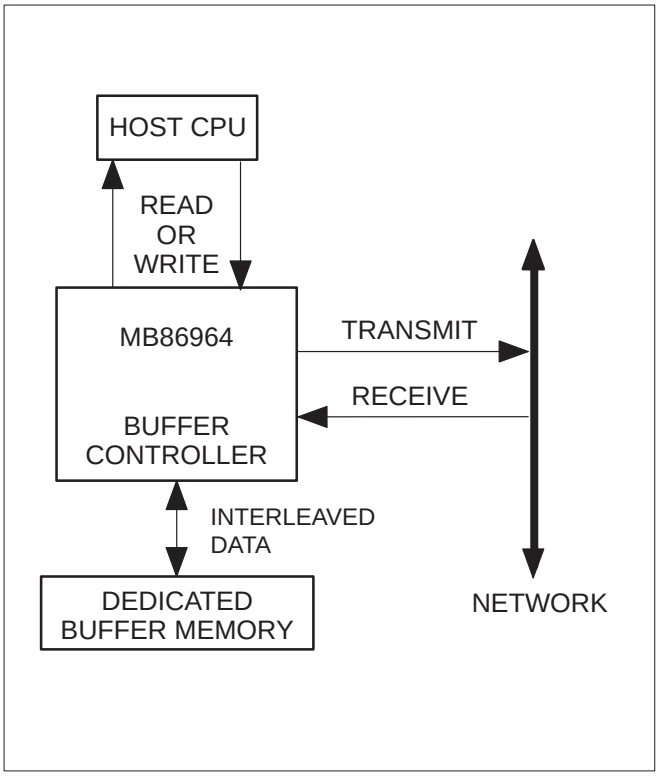


Figure 6. Simultaneous Access to Buffer Memory

Transmit Buffer

The section of the memory used by the transmitter can be configured by programming the Transmitter Buffer Size control bits, DLCR6<3:2>. Configurations include a single buffer 2 kilobytes long, or a pair of banks, each either 2, 4 or 8 kilobytes long, as illustrated in Figure 7. Within each buffer or bank, one or more packets can be written by the system until the available space is too small for another packet. When a single transmit buffer is used, the system and the transmitter time-share the use of the buffer. When two buffers are used, the system can load packets into one of the buffers while the contents of the other are being transmitted. Using dual buffers and loading multiple packets for 'packet chaining' gives the highest rate of transmission.

At reset, internal pointers are initialized to point to the beginning of one of the transmit buffers. Each time the host writes data to the buffer via the Buffer Memory Port Register, an internal pointer is advanced to the next memory location within the transmit buffer. Once a data byte/word is written, it cannot be read and the internal pointer cannot be reversed.

When the host completes loading the transmit buffer, it writes the number of packets it has loaded into TX PKT CNT, BMPR10<6:0> and sets the transmit start bit, BMPR10<7>. When this occurs, the MB86964 will switch banks and will start transmitting at the earliest opportunity. Another automatically-managed pointer, the transmit read pointer, sequences through the bank being transmitted to read the packet data into the transmitter through its FIFO. If a collision occurs, the packet will be automatically retransmitted after a pseudo-random waiting interval called the backoff interval. If there are multiple packets in the buffer, the MB86964 will continue down the list until all are transmitted. Upon reaching the end of the list or chain of packets, the transmitter will stop, update its status bits and, if enabled, generate an interrupt. The details of this operation are described in the section on packet transmission.

Transmit Packet Header

As shown in Figure 8, each packet within one transmit bank is separated by a non-transmitted, two-byte header containing an 11-bit value which specifies the length of the associated packet in bytes. The length specification includes only what is stored in the buffer (shown in the figure as 'DATA'), which are the Destination ID, Source ID, Length, and Data fields of the packet. It does not include the Preamble and CRC fields which are generated by the MB86964 as it transmits the packet, and therefore are not stored in the buffer.

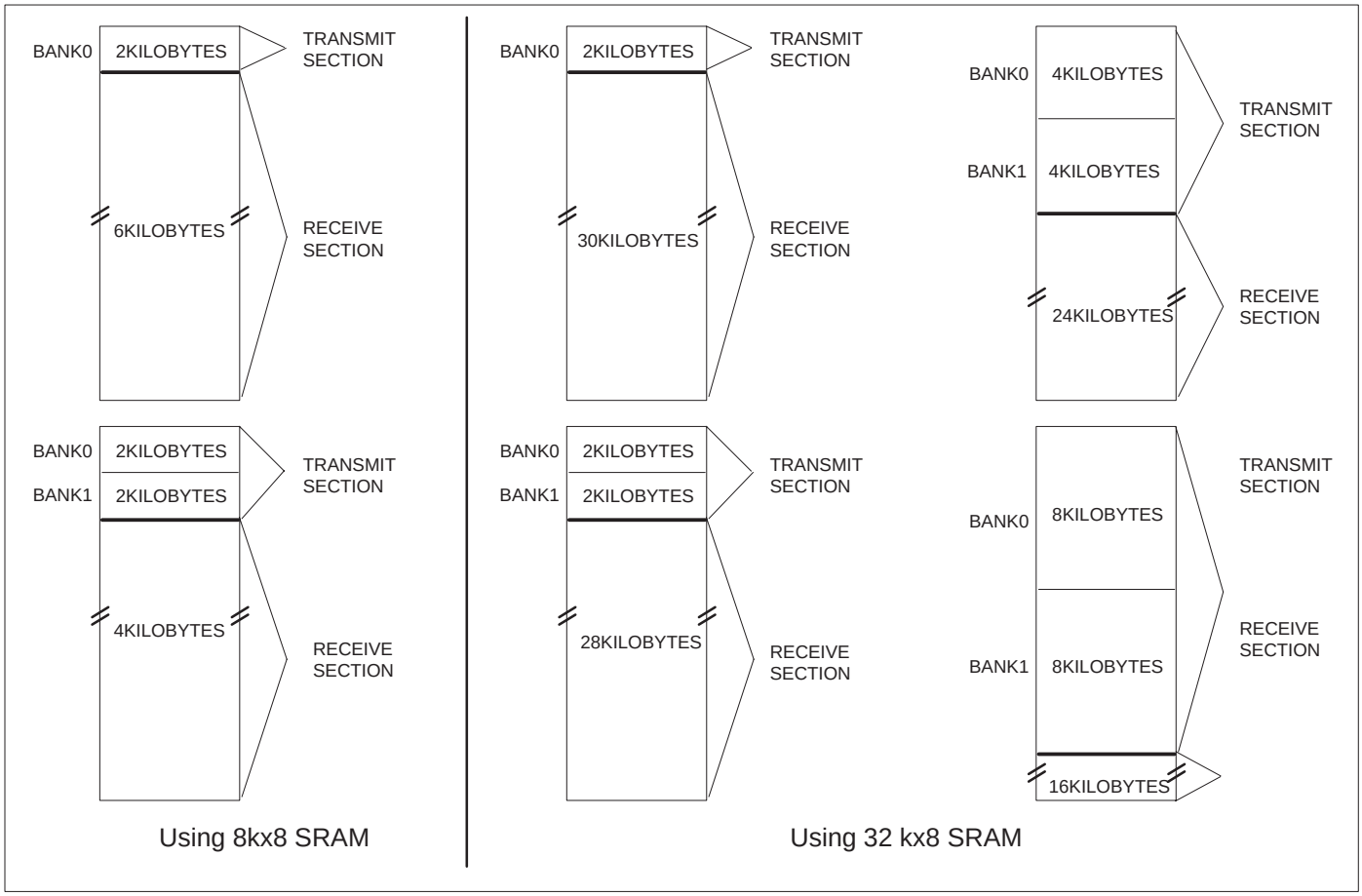


Figure 7. Transmit Buffer Configurations

Receive Buffer

Once initialized and enabled, the receiver will automatically load any error-free incoming packets which pass the address filter into the receive buffer through an on-chip FIFO. An interrupt can be provided to alert the host processor that a packet is available in the buffer. The host processor can read out received packets as they become available. Continuous reception can continue as long as the receive buffer does not become full. If the host processor reads the receive packets from the buffer promptly, the buffer will not fill up. If overflow does occur, the receiver will stop and an interrupt will be generated to indicate the problem. If this occurs, the buffer should be emptied so that reception can resume. As soon as space becomes available in the receive buffer, the receiver will automatically resume reception.

The receive buffer size can vary between a maximum of 30 kilobytes when 2 kilobytes are allocated for the transmit section and a 32 kilobyte SRAM is used, to a minimum of 4 kilobytes if 4 kilobytes are allocated for the transmit section and an 8 kilobyte SRAM is used. The receive section dynamically allocates space for each individual incoming data packet, aligning each at an eight-byte 'page' boundary. Each received packet is preceded by a four byte header which provides packet status and the length of that data packet. The data packets are linked or chained by internal pointers which use the length value in the packet header to calculate the starting address of the next packet. This buffer format is shown in Figure 9. Since the MB86964 controls its dedicated buffer memory, FIFO size and depth are unimportant in this architecture, and need not be considered in system timing considerations.

A status bit in one of the MB86964's internal registers informs the host when one or more packets are resident in the receive buffer and available to be read. The host retrieves these packets from the buffer memory by successive reads of BMPR8. Once a data byte/word is read from the buffer memory, internal pointers are advanced to the next byte/word. As data is thus read by the system, that memory becomes available for reception of new packets. The MB86964 automatically rejects an incoming packet if there is not enough buffer space to fully receive that packet. Therefore, there is no chance for packets already received to be 'overrun' by incoming packets.

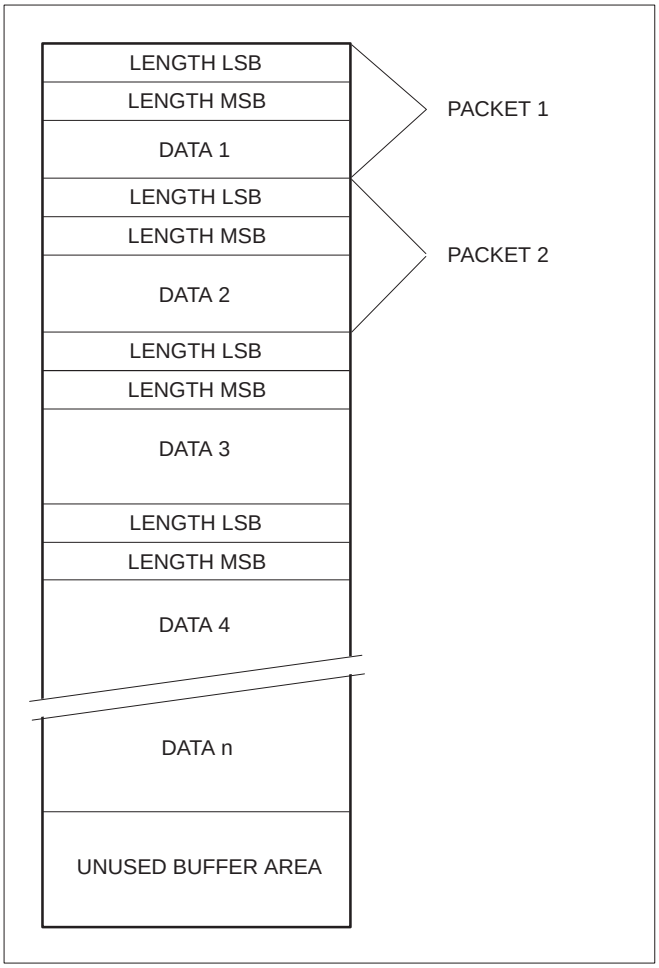


Figure 8. Transmit Buffer Detail

When DLCR5<5>, the ACPT BAD PKTS bit, is set to a '0' (disabled), detection of a bad incoming packet causes the MB86964 to release the buffer space in which that packet is contained and to reset its internal pointers so as to use that space for the next incoming packet. If this bit is set to a '1', a packet with a CRC or alignment error will be accepted and the appropriate error bits in the status field of its header will be set. The same applies to DLCR5<3>, ACPT SHORT PKTS, which when high allows retention of packets below 60 bytes in length, excluding Preamble and CRC (which is shorter than IEEE 802.3 minimum packet size).

Skip Packet

Writing a '1' to BMPR14<2> commands the buffer controller to skip the balance of the current receive packet in memory. The bit can then be read to determine whether the skip process is complete (within 300 ns). If there is another packet, the bit returns to 0 when the chip is ready to read the next packet.

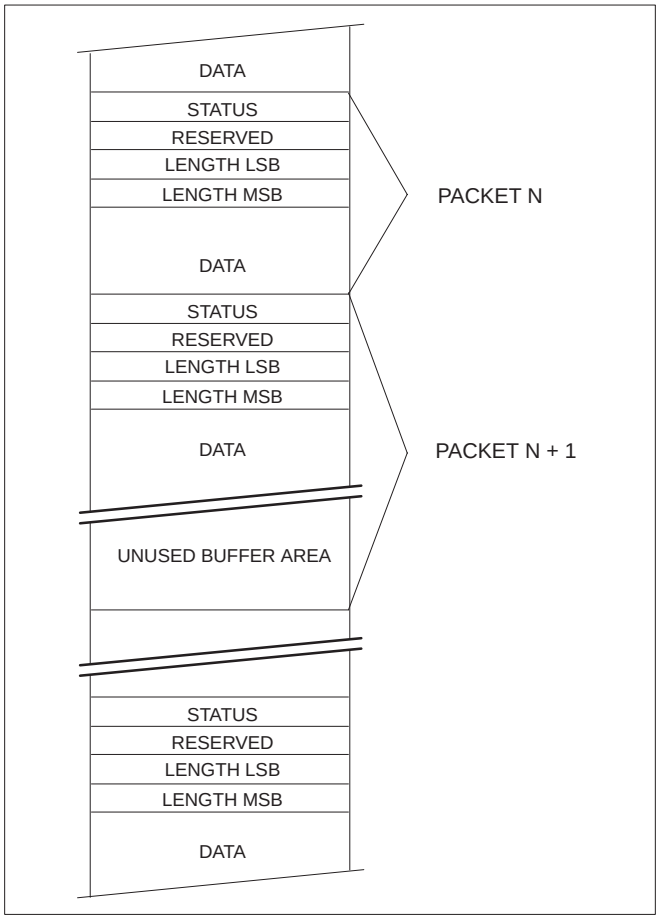


Figure 9. Receive Buffer Detail

Receive Packet Header

The receive packet header contains four bytes and is stored in the receive buffer preceding each packet. The receive packet header comprises one byte of packet status, an unused byte and two bytes (11 bits) for packet length. Bits 1 through 4 of the status byte are an image of the same bits in the Receive Status Register, DLCR1, with respect to the packet that follows. Bit 5 is the GOOD PKT bit, which when set to 1 indicates that no errors were detected in the packet. Bits 0, 6 and 7 are unused and are always set to 0. See Table 2.

The length stored in bytes 3 and 4 of the header specifies the length of the portion of the packet stored in the buffer. This length specification is in bytes, regardless of whether the system interface is programmed for byte or word mode. During reception, the MB86964 strips the Preamble field and checks and strips the CRC field, so, as is the case for the transmit buffer, those fields of the packet are not stored in the buffer. The length specification thus includes only the Destination ID, Source ID, Length, and Data fields of the incoming packet.

Table 2. Receive Packet Header Status Indications

CONDITION	N/A (BIT 7)	N/A (BIT 6)	GOOD PKT (BIT 5)	RMT 0900H (BIT 4)	SHORTP KT ERR (BIT 3)	ALIGN ERR (BIT 2)	CRC ERR (BIT 1)	N/A (BIT 0)
GOOD PACKET	0	0	1	0/1	X	X	X	X
PACKET WITH ERROR	0	0	0	0/1	0/1	0/1	0/1	X

0/1 indicates that the value of the bit will be 0 or 1 depending on the condition of the packet. An 'X' indicates that the value should be ignored

TRANSMITTER CIRCUITS

Circuits within the transmitter include a transmitter state machine, a small FIFO for pipelining the packet data, preamble generator, CRC generator, parallel to serial converter, backoff generator, interpacket gap timer and time domain reflectometer (TDR) counter. Additional circuits involved in packet transmission are described in the Transceiver section of this document.

The transmitter state machine provides sequencing of events for the transmitter, including idle, preamble, data, CRC, interpacket gap, jam and backoff. It detects various transmit error conditions and sets appropriate bits within the DLCR registers.

The pipeline FIFO provides elastic buffering that the buffer controller can load with data to be transmitted. The chip's CRC generator calculates the 32-bit CRC on the destination and source address, the length field and the data field as specified by the ISO/ANSI/IEEE 8802-3 specification for Ethernet. This value is appended to the end of the packet when it is transmitted.

Media Access Control

The MB86964 transmitter state machine implements the Carrier Sense, Multiple Access with Collision Detection (CSMA/CD) network media-access protocol. The MB86964 monitors the network for any other node's carrier, and defers transmission (collision avoidance) while other nodes are transmitting, except when $\overline{\text{EN\_TX\_DEFER}}$, DLCR4<0>, is high. Collision detection handles collisions that may still occur when two nodes separated on the network begin transmitting at nearly the same time. All nodes monitor the network for collisions and, when involved in one, transmit a 32-bit jam signal to reinforce the collision and then terminate transmission. After waiting a pseudo-random backoff interval, generated as described below, the node automatically retries transmission of the packet.

Packets on the network must be separated by at least 9.6 microseconds, the 'interpacket gap' (IPG) during which the network medium is specified to be idle. The MB86964 transmitter state machine measures this IPG starting from the end of a packet on the network, and does not attempt to transmit until the end of the IPG. If carrier reappears on the network during the first two-thirds of the IPG, the MB86964 resets the timer to re–time the IPG from the end of the new transmission. Such an event can occur during a collision, since data and carrier indications can be corrupted by the superimposition of the two packets. During the last one-third of the IPG, the MB86964 ignores the occurrence of a carrier indication, in accordance with 8802-3, to ensure fairness and equality in access to the network. Thus, if one station begins transmission slightly ahead of another, there is no advantage to the earlier start. Both nodes transmit, a collision occurs, and backoff interval differentials resolve the media-access contention.

Transmit Packet Processing

To transmit one or more packets, the host system first loads the packet(s), preceded by a two-byte header giving their lengths, into a transmit buffer by writing the data to the Buffer Memory Port Register, BMPR8. Only the destination address, source address, length and data fields of the packets are loaded by the system. After the packets are loaded into the transmit buffer, the system turns the transmitter on to initiate transmission. Observing the media access protocol, the MB86964 defers transmitting to carrier from other nodes, minimum interpacket gap intervals and backoff intervals, if any, and then begins to serialize the data. It generates the Preamble field at the beginning, and calculates and appends the CRC field at the end. Figure 10 illustrates the standard packet format. The serialized signal is routed to the transceiver section which encodes the data into the required Manchester code, appends an end-of-packet delimiter, and outputs the data on the selected network interface port (AUI or 10BASE-T).

The transmitter transmits the packets in the transmit buffer in the order in which they were loaded. If a collision is detected by the transceiver, the transmitter automatically retransmits the packet until successful or until 16 consecutive attempts have ended in collision. In the latter case, depending on the mode selection made at initialization time, the transmitter continues to try to transmit the same packet starting again with a collision count of zero, skips the current packet and tries to transmit the next packet starting with a collision count of zero, or halts and waits for instruction from the host. In the last case, the host can elect to terminate transmission attempts by setting $\overline{\text{DLC\_EN}}$, DLCR6<7> to one, continue to attempt to transmit the same packet (collision counter reset), or skip the current packet and try to transmit the next packet (collision count is zero).

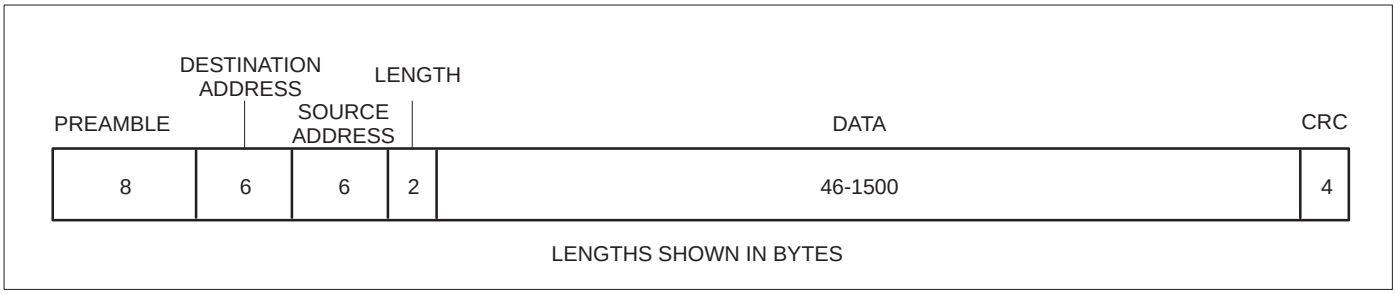


Figure 10. Packet Format

Backoff Generator

A 17-bit pseudo-random number generator clocked at the 10 MHz bit rate provides the collision backoff function. Distances between stations become part of the randomizing function. The number generator is sampled at the time of collision, masking all but the appropriate number of bits specified by the 8802-3 backoff algorithm. This value is then counted down at the slot-time rate (512 bit times) to generate the backoff interval. For a first collision, only one bit is used, giving a backoff of either 51.2 microseconds or 0. For a second consecutive collision, two bits are used, and so forth, up to ten bits. From the tenth to the 16th collisions, 10 bits are used. This generates a pseudo-random backoff interval of from 0 to 52.38 ms, the so-called 'binary exponential backoff' for collisions per the 8802-3 standard.

Transmit Error Processing

The MB86964 provides four transmit error status bits in its Transmit Status Register (DLCR0) for reporting the four possible transmit errors. The errors are: 1) loss of carrier during transmission, which usually indicates a medium fault or a collision, 2) collision, 3) 16 consecutive collisions and 4) jabber error, which occurs if the length of a single transmission substantially exceeds the time required to transmit a maximum length packet conforming to the standard. The latter three can be enabled separately to generate interrupts.

A status bit in the Transmit Status Register is set in case a collision terminates transmission. Collision counter DLCR4<7:4>, automatically increments after each collision up to the sixteenth collision, at which time it rolls over to zero. Another status bit indicates that sixteen consecutive attempts to transmit a packet have been made and all have been terminated by collision. The occurrence of 16 collisions may indicate a network problem, such as a disconnected cable or terminator, that produces false collisions. While rare, 16 collisions may normally occur.

Time Domain Reflectometry

When a node transmits, a short or open on the network causes a reflected signal to the node receiver, which can sometimes be detected. The reflection causes failure of the carrier sense or detection of a false collision. An open on the network may cause a false collision, whereas a short usually causes loss of carrier sense. Time domain reflectometry (TDR) allows estimates of the distance along the network cable from the node to the fault.

The MB86964 is equipped with a special counter to perform the TDR function. The contents of the counter after any transmission can be determined by reading the Time Domain Reflectometry registers, DLCR14 (the least-significant byte) and DLCR15 (the most-significant byte). Only the lower 14 bits of the counter are equipped, which is more than is needed for an IEEE or Ethernet LAN. The top two bits, DLCR15<7:6>, are always 0. The TDR counter counts the actual number of bits transmitted for each packet before a collision indication, carrier loss indication or completion of transmission, whichever comes first. A complete transmission with no error indications clears the TDR counter. The elapsed time represents twice the signal delay from node to fault.

To perform the TDR fault test, first enable interrupts for TX DONE, by setting DLCR2<7> high. An alternative to using the interrupt is to poll the TX DONE bit, looking for a high level. Set the 16 Collisions Register, BMPR11, to 07H for this test (no halt, skip-failed packet). Clear status bits by writing 0FF86H to the Receive and Transmit Status registers. Next, try to transmit a packet length of 600 or more bits. Up to 16 attempts may be made automatically, if collisions are indicated. Upon completion of the transmission attempts, TX DONE goes high, generating an interrupt if so enabled. When this occurs, read the Transmit Status register and the TDR register.

Interpreting the Results

If the count is zero, no fault was detected. If the count is greater than zero, but smaller than the packet length, a cable fault may exist. If the count is less than 525, a real collision may have occurred during the test. Real collisions normally occur within the first 65 bytes of the packet, including preamble. Note the error status bits, COL and CR LOST. COL high suggests a cable open, whereas CR LOST suggests a short. Repeat the measurement several times, discarding any anomalous values, and average the remaining measurements. A cluster of readings at about the same value is a strong indicator of a valid fault measurement. If such a cluster of readings occurs, multiply the average of the cluster by 39 feet to estimate the distance from the node to the fault. [39 feet = (100 ns x 0.8 x 186,282 miles/second x 5280 feet/mile)/2; this assumes the network is mostly coaxial cable with signal propagation speed of approximately 0.8 x C, the speed of light.]

RECEIVER CIRCUITS

The receiver includes a receive state machine, serial-to-parallel conversion, pipe-line FIFO, preamble recognition, bit and byte-framing, address filtering, CRC and other error checking. Additional circuits involved in packet reception are described in the Transceiver section of this document.

The receiver state machine provides sequencing of events for the receiver, including idle, busy, address filtering, and data storage, detects receive error conditions and sets appropriate bits within the DLC registers. A small data FIFO provides elastic buffering for synchronization with the buffer controller timing and buffering of data while the buffer controller is servicing other buffer memory access requests.

Monitoring the Network

Whenever the data link section is enabled ($\overline{\text{DLC\_EN}}$ bit, DLCR6<7>, is set to zero), the MB86964 constantly monitors the network for carrier. Signals that exceed the AC and DC squelch thresholds of the transceiver cause the internal carrier sense line to assert, which in turn causes the receiver to attempt to receive a packet. (The transmitter also uses the carrier sense function to defer to transmissions from other nodes.)

The receiver monitors the serial data stream from the transceiver for the end-of-preamble bit pattern, a four-bit pattern of 1011 ending the preamble's pattern of alternating ones and zeros. This pattern also provides byte and field synchronization for the receiver; the bit immediately following the end of preamble is the first bit of the first byte of the packet's destination address field.

When packet transmission is unflawed, carrier sense remains asserted for the duration of the packet, negating just after the last bit of the CRC field is received, when the transceiver detects the end-of-packet symbol at the end of the packet. Loss of carrier sense at any other time may also result from a collision or other network problems.

Address Filtering

A receive packet can be filtered by applying selectable criteria to the contents of its Destination Address field, which is the first data-bearing field following immediately after the Preamble. There are several control bits in the MB86964's registers which provide programmablility of the filter criteria. The contents of the Destination Address field can be of three basic types. The first data type which can occur in this 48-bit field is a single node address, the unique, single-node address, globally registered with the IEEE. This data type is indicated by a "0" in the first bit position of the address. The second type is the multicast address, an address for a pre-defined group of nodes, for example, NetWare 4.0 file servers. The multicast address is indicated by a "1" in the first bit position of the address. The MB86964 filters multicast addresses using a hash function and a 64-bit hash table. Thirdly, a broadcast address is defined as a special case of the multicast address which addresses all nodes on the local network. This address value consists of all "1"s. The MB86964 provides programmable address filtering logic for each of these address types.

Among the address filtering selections possible with the MB86964 are the following examples:

1. All Pass (no filtering)
2. Node address and broadcast packets only
3. Node address xxx.xxx, multicast addresses yyy.yyy and zzz.zzz and broadcast packets only

Hash Table

The Hash Table provides a way to filter incoming multicast packets so the host processor need not process packets that are not of interest. The principle behind this filtering process is based on the arrangement of a large number of elements of an array, or database, to facilitate searching for elements associated with a given key or datum. The hash function is a mathematical or logical function that maps all elements in a domain onto a smaller domain called the hash table.

Assume this hashing function as an example: treat the multicast address as a nonnegative 48-bit integer, divide this number by 64 and take the remainder. This function maps all multicast addresses into a 64-element hash table because the remainder must be an integer between 0 and 63. Applying this hashing function results in taking the least-significant six bits of the multicast address as an integer. In the hash table, for each element, 0 through 63, a single bit is stored to indicate if the address is accepted (1) or rejected (0). If, for example, the node belongs to three multicast groups, only three or fewer of the hash table elements store ones, and the rest store zeroes. The scheme allows the acceptance of any number of addresses, including all of them. However, while this filters out most nonspecific addresses, there may be addresses not of interest used on the network that also fall into the accept elements, so filtering may be imperfect.

The actual hashing function used in the MB86964 is to calculate the CRC on the multicast address and to store the most-significant six bits of this calculation in a register . The six bits are used to address the elements of the hash table: the three MSBs are used as the Hash Table register address, and the three LSBs are used as the bit address within a register byte. If the addressed Hash Table element yields a '1' and the packet is a multicast packet (first bit of destination address equals 1), and it passes the error filters, the packet will be accepted. The hash filter criteria are only used on multicast addresses, which all start with a one. Node IDs that start with a zero are not filtered by the hash filter. The broadcast address, a special case of the multicast set wherein all the bits are ones, is accepted anyway unless the Reject All Packets mode is selected.

The hash filter is used only when the Address Filter mode select bit AF1 is 1 and mode select bit AF0 is 0, selecting the Node ID, Broadcast, Multicast + Hash Table mode. Hash Table registers should only be accessed when the Receiver is disabled, i.e., when $\overline{\text{DLC\_EN}}$ is high, to avoid interaction with the Receiver. There are eight bytes of registers in the Hash Table containing 64 one-bit elements, as shown in the table 7. Software code examples showing how to calculate entries for the Hash Table are available through Fujitsu sales offices.

Receive Packet Processing

As a packet arrives from the network, its destination address field is tested for the various address filter criteria selected by the Address Filter Mode bits, DLCR5<1:0>, and the Hash Table. Only if the address meets the filter criteria selected will the packet be accepted for storage in the receive buffer. In addition, the packet must be error-free, unless the chip has been enabled to receive flawed packets for diagnostic purposes. If these conditions are met, the packet reception results in the packet being stored in the buffer, its 4-byte header being updated at the end of reception, the RBUF EMPTY status bit, DLCR5<6>, being cleared, the RX PKT status bit, DLCR1<7>, being set high and an interrupt being generated if so enabled. The last four bytes of the packet are the CRC field and are checked for correct CRC. The CRC bytes are not transferred to the Receive Buffer. If the packet has an error and reception of such packets has not been enabled, it will be discarded and pointers will be reset to reuse the same portion of the receive buffer for the next packet to arrive. If a flawed packet is accepted for storage for diagnostic purposes, its error(s) will be reported in the status byte of its header (see Receive Packet Header section).

Receive Error Processing

Status bits in the receive status register are set to indicate errors associated with packet reception. These errors are: 1) bus read error, which occurs if the host system attempts to read from an empty receive buffer (this need never occur if the RX BUF EMPTY bit is checked), 2) short packet error, 3) alignment error (incomplete byte fragment at end of packet), 4) CRC error and 5) buffer overflow, which occurs if the receive buffer space is insufficient to hold the entire received packet (the receive controller automatically removes such packets from the receive buffer and packets already stored in the buffer are not lost). Each of these receive error conditions may optionally generate an interrupt. None of these errors requires special host processing or intervention, other than optional tallying of the error for network management purposes.

TRANSCEIVER

The MB86964's transceiver section provides the electrical interface for DB15 (AUI) and RJ45 (10BASE-T) connections to the Ethernet local area network. Its functions include Manchester encoding and decoding of serial data streams to the transmitter and from the receiver, level conversion, collision detection, signal quality error (SQE) and link integrity testing, jabber control, loopback, and automatic correction of polarity reversal on the twisted-pair input. Pulse shaping and filtering functions eliminate the need for external filtering components and thus reduce overall system cost. Also provided are outputs for transmit, collision and link test pass LEDs, and compatibility with shielded and unshielded twisted-pair cables. Receive threshold can be reduced to allow an extended range between nodes in low-noise environments. Programmable functions are controlled via BMPR13. Transceiver status is presented in BMPR15.

Data Encoder

The encoder converts the serialized NRZ data from the transmitter to Manchester code, the format used on the network medium. In Manchester code a one is represented as a bit cell (nominally 100-nanoseconds) starting with a low, ending with a high, with a low-to-high transition at the midpoint; Manchester code for a zero is the inverse.

The encoder also monitors the state of the internal transmit enable signal from the transmitter section and appends an end-of-packet symbol (illegal Manchester code) to the data stream when that signal is negated at the end of the CRC field of the transmitted packet.

Transmitter Circuits

The transceiver's transmitter section receives the encoded data from the Manchester encoder and transfers it to either the AUI cable via the the DO circuit or the twisted-pair network via the TPO circuit. Advanced integrated pulse-shaping and filtering produces an output signal that is predistorted and prefiltered to meet the 10BASE-T jitter template on the TPON and TPOP pins, so that no external filters are required.

During idle periods, the MB86964 transmits link integrity test pulses on the TPO circuit if $\overline{\text{LINK\_TEST\_EN}}$, BMPR13<5>, is asserted and the AUI/$\overline{\text{TP}}$ port select bit, BMPR13<4> is set for twisted-pair (TP) operation (or if the transceiver is set for automatic port selection via BMPR13<3> and the TP port is auto-selected). The MB86964 is programmed for either shielded (150Ω) or unshielded (100Ω) twisted-pair through the STP/$\overline{\text{UTP}}$ bit BMBR13<2>.

Jabber Control

An on-chip watchdog timer prevents the chip from locking into a continuous transmit mode. When a transmission exceeds the maximum time limit (specified for the MB86964 as 20 to 150 msec), the watchdog timer disables the transmit and loopback functions and asserts the JABBER error status bit, DLCR0<3>, generating an interrupt if so enabled. Before the MB86964 can exit the jabber state, the transmit data circuit must remain idle for between 0.25 and 0.75 seconds.

SQE Test

The transceiver supports the signal quality error (SQE) test function specified in the standard. After every successful transmission on the 10BASE-T network, the MB86964 transceiver section transmits the SQE signal to the controller for 10±5 bit times over the internal CI circuit. BMPR15<1> reflects the status of this SQE test.

Receive Input Circuits

Valid received signals from the twisted-pair network connection (the TPI circuit) or from the AUI network connection (the DI circuit) pass through on-chip filters to the data decoder. No external filters are required.

An internal intelligent squelch function discriminates noise from link test pulses and valid data streams. The receiver is activated only by valid data streams above the squelch level and with proper timing. If the differential signal at the TPI or the DI circuit inputs falls below 75% of the threshold level (unsquelched) for eight bit times (typical), the receiver enters the idle state. The squelch threshold can be controlled via BMPR13<6>.

Data Decoder

The data decoder section performs three functions on the received data: clock recovery, carrier detection, and Manchester data decoding. Carrier detection is indicated to the receiver section by assertion of the internal carrier sense signal, which occurs shortly after the received data signals appear. Carrier sense status can be monitored via DLCR0<6>. Clock recovery and data separation are accomplished by an internal phase-locked loop. The recovered clock is supplied to the receiver together with the recovered NRZ serial data stream.

Reverse Polarity

The transceiver polarity reverse circuit uses link pulses and end-of-frame data to determine the polarity of the received signal. A reversed polarity condition is detected when eight opposite receive link pulses are detected without receipt of a link pulse of the expected polarity. Reversed polarity is also detected if four frames are received with a reversed start-of-idle. Whenever polarity is reversed, these two counters are reset to zero. If the transceiver enters the link fail state and no valid data or link pulses are received within 96 to 128 milliseconds, polarity resets to the default uninverted condition. If Link Integrity testing is disabled, polarity detection is based only on received data.

The transceiver automatically corrects reversed polarity. Polarity reversal is reported via BMPR15<3>.

Collision Detection

The collision detection function operates on the twisted-pair side of the interface. A collision is defined as the simultaneous presence of valid signals on both the TPI circuit and the TPO circuit. The transceiver reports collisions to the back-end via an internal signal. If the TPI circuit is active while there is activity on the TPO circuit, the TPI data passes to the back-end as received data, disabling normal loopback.

Loopback

The MB86964 provides the automatic local loopback function specified by the 10BASE-T standard for the twisted-pair port. This function is in effect except when the $\overline{\text{LBC}}$ bit, DLCR4<1>, is asserted. Data transmitted by the transmitter is passed through the data encoder, internally looped back within the MB86964 before the TPO drivers to the data decoder and returned to the receiver. This local loopback function is disabled when a data collision occurs, clearing the received data circuit in the transceiver for the data arriving at the twisted-pair inputs. The local loopback is also disabled during the link fail and jabber states.

The MB86964 provides additional loopback testing functions controlled by $\overline{\text{LBC}}$. When the twisted-pair port is selected and $\overline{\text{LBC}}$ is asserted, the loopback is forced regardless of the state of the TPI inputs or link test failure. When the AUI port is selected and $\overline{\text{LBC}}$ is asserted, internal local loopback is enabled. If $\overline{\text{LBC}}$ is negated, no local AUI loopback occurs.

During loopback, data is routed from the transmit buffer to the transmit section of the data link controller, through the Manchester encoder, back through the Manchester decoder, through the receiver section of the data link controller, and is then stored in the receive buffer. Software can then read and check the received packet that has traveled through the MB86964 transmit and receive sections. Receipt of the loopback data into the receive buffer can be disabled by asserting FILTER SELF RX, BMPR14<0>. The transmitted data is blocked from appearing at the network outputs while the MB86964 is in forced loopback mode ($\overline{\text{LBC}}$ asserted).

Link Integrity Test

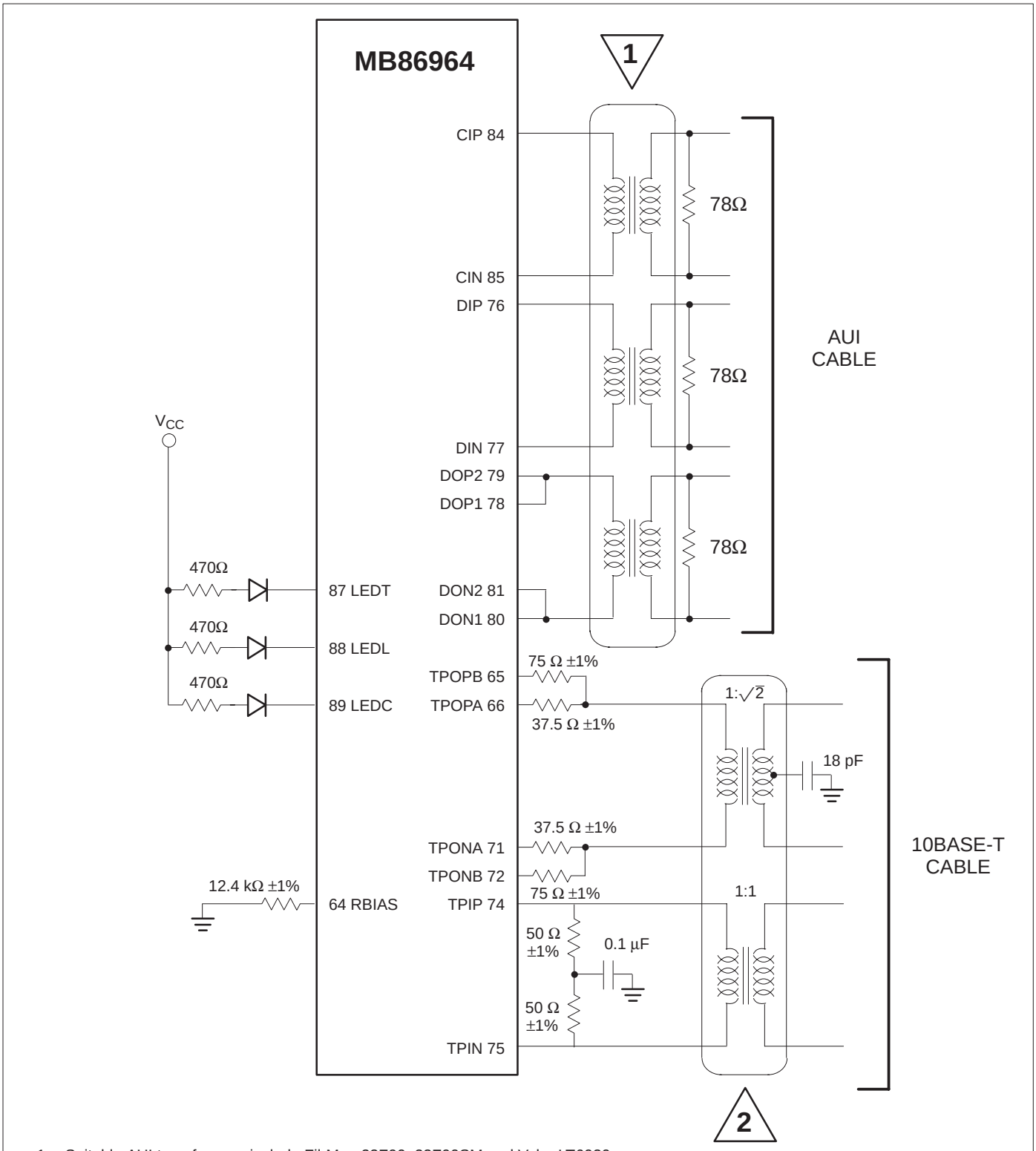
The link integrity test determines the status of the receive side twisted-pair cable. Link integrity testing is enabled when $\overline{\text{LINK\_TEST\_EN}}$, BMPR13<5>, is set low. When enabled, the receiver recognizes the link integrity pulses transmitted in the absence of receive traffic. If no serial data stream or link integrity pulses are detected within 50 to 150 milliseconds, the MB86964 enters a link-fail state and disables the transmit and automatic local loopback functions. The MB86964 ignores any link integrity pulse with an interval less than 2 to 7 milliseconds. The MB86964 remains in the link-fail state until it detects either a serial data packet or two or more link integrity pulses.

Remote Signaling

The MB86964 transmits standard link pulses that meet the 10BASE-T specification. However, the MB86964 encodes additional status information into the link pulse by varying the link-pulse timing; this is referred to as remote signaling. By using alternate pulse intervals, the MB86964 signals three conditions: Remote Linkdown, Remote Jabber, and Remote Signaling Capability. The MB86964 also recognizes these alternate pulse intervals when received from a remote unit. Remote status conditions are indicated as RLD, BMPR15<7>, RJAB, BMPR15<5>, and RMT PORT, BMPR15<4>.

Connecting to the Network

Figure 11 shows typical connections between the MB86964's twisted pair and AUI ports and the network.



1. Suitable AUI transformers include Fil-Mag 23Z90, 23Z90SM and Valor LT6030.
2. Suitable 10BASE-T transformers include Fil-Mag 23Z128, 23Z128SM, Valor PT4069, Pulse Engineering PE–65745, PE–68048, and PE–65454.

Figure 11. Typical TP Port and AUI Port Connections

CONTROL AND STATUS REGISTERS

The control and status registers on the MB86964 are accessed through register addresses 00H through 0FH, and register bank-switching bits RBS1 and RBS0, DLCR7<3:2>. Table 3 summarizes the internal registers and their addresses. In 16-bit mode, even-numbered direct addresses select the registers. For example, address 00H accesses the Transmit and Receive Status registers simultaneously. Transmit Status would be on the low byte and Receive Status on the high byte. Appropriate byte-access processor instructions can access high and low bytes separately.

Tables 4 - 8 summarize the control and status bits within each addressable register, as well as the bits in the receive and transmit packet headers. The registers are descibed more fully in the tables that follow.

The abbreviation that appears in the TYPE column of the following tables are described in the legend below.

TYPE CODE	DESCRIPTION
R	Readable
W	Writable
N	Not used, reserved; write 0 when written.
C	Writing a 1 clears status bit (and interrupt if enabled). Writing a 0 has no effect.
0/1	Initial state after hardware reset.

Table 3. Internal Register Address Map

REGISTER BANK		SYSTEM ADDRESS				REGISTER	
RBS1	RBS0	SA3	SA2	SA1	SA0	NAME	DESCRIPTION
X	X	0	0	0	0	DLCR0	Transmit Status
X	X	0	0	0	1	DLCR1	Receive Status
X	X	0	0	1	0	DLCR2	Transmit Interrupt Enable
X	X	0	0	1	1	DLCR3	Receive Interrupt Enable
X	X	0	1	0	0	DLCR4	Transmit Mode
X	X	0	1	0	1	DLCR5	Receive Mode
X	X	0	1	1	0	DLCR6	Configuration 0
X	X	0	1	1	1	DLCR7	Configuration 1
0	0	1	0	0	0	DLCR8	Node ID 0
0	0	1	0	0	1	DLCR9	Node ID 1
0	0	1	0	1	0	DLCR10	Node ID 2
0	0	1	0	1	1	DLCR11	Node ID 3
0	0	1	1	0	0	DLCR12	Node ID 4
0	0	1	1	0	1	DLCR13	Node ID 5
0	0	1	1	1	0	DLCR14	TDR 0 (LSB)
0	0	1	1	1	1	DLCR15	TDR 1 (MSB)
0	1	1	0	0	0	HT8	Hash Table 0
0	1	1	0	0	1	HT9	Hash Table 1
0	1	1	0	1	0	HT10	Hash Table 2
0	1	1	0	1	1	HT11	Hash Table 3
0	1	1	1	0	0	HT12	Hash Table 4
0	1	1	1	0	1	HT13	Hash Table 5
0	1	1	1	1	0	HT14	Hash Table 6
0	1	1	1	1	1	HT15	Hash Table 7
1	0	1	0	0	0	BMPR8	Buffer Memory Port (LSB)
1	0	1	0	0	1	BMPR9	Buffer Memory Port (MSB)
1	0	1	0	1	0	BMPR10	Transmit Start, Packet Count
1	0	1	0	1	1	BMPR11	16 Collisions Control
1	0	1	1	0	0	BMPR12	DMA Enable
1	0	1	1	0	1	BMPR13	DMA Burst, Transceiver Mode
1	0	1	1	1	0	BMPR14	Filter Self Receive, Transceiver Interrupt Enable
1	0	1	1	1	1	BMPR15	Transceiver Status

Table 4. Control and Status Bits, DLCR0-7

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TX STATUS DLCR0	TX DONE	NET BSY	TX PKT RCD	CR LOST	JABBER	COL	16 COL	0
RX STATUS DLCR1	RX PKT	BUS RD ERR	DMA EOP	RMT 0900H	SHORT PKT ERR	ALIGN ERR	CRC ERR	RX BUF OVRFLO
TX INT ENABLE DLCR2	DONE INT EN	0	0	0	JABBER-INT EN	COL INT EN	16 COL INT EN	0
RX INT ENABLE DLCR3	RX PKT INT EN	BUS RD INT EN	DMA EOP INT EN	RMT INT EN	SHT PKT INT EN	ALIGN INT EN	CRC ERR INT EN	RX BUF INT EN
TX MODE DLCR4	COL CTR 3	COL CTR 2	COL CTR 1	COL CTR 0	0	$\overline{\text{DREQ}}$ $\overline{\text{EXTND}}$	$\overline{\text{LBC}}$	EN TX DEFER
RX MODE DLCR5	0	RX BUF EMPTY	ACPT BAD PKTS	RX SHORT ADDR	ACPT SHORT PKTS	RMT CNTRL EN	AF1	AF0
CONFIG 0 DLCR6	$\overline{\text{DLC\_EN}}$	1	SB/SW	1	TBS 1	TBS 0	BS 1	BS 0
CONFIG 1 DLCR7	CID 1	CID 0	PWRDN	RDYPOL	RBS 1	RBS 0	EOPPOL	M..L / $\overline{\text{L..M}}$

Table 5. Control and Status Bits, BMPR8-15

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BUF MEM PORT (LSB) BMPR8	7	6	5	4	3	2	1	0
BUF MEM PORT (MSB) BMPR9	15	14	13	12	11	10	9	8
TX START BMPR10	TX START	TX PKT CNT 6	TX PKT CNT 5	TX PKT CNT 4	TX PKT CNT 3	TX PKT CNT 2	TX PKT CNT 1	TX PKT CNT 0
16 COLLISIONS BMPR11	0	0	0	0	0	16 COL CNTRL 2	16 COL CNTR L 1	16 COL CNTRL 0
DMA ENABLE BMPR12	0	0	0	0	0	0	RX DMA EN	TX DMA EN
DMA BURST / TXVR MODE BMPR13	1	$\overline{\text{LOWER}}$ $\overline{\text{SQUELCH}}$ $\overline{\text{THRESH}}$	$\overline{\text{LINK\_TEST\_EN}}$	AUI/$\overline{\text{TP}}$	AUTO PORT SEL	STP/$\overline{\text{UTP}}$	BURST 1	BURST 0
FILTER SELF RX BMPR14	RLD INT EN	LLD INT EN	RJAB INT EN	0	0	SKIP PKT	SQE INT EN	FILTER SELF RX
TXVR STATUS BMPR15	RLD	LLD	RJAB	RMT PORT	RXI POL REV	0	SQE	0

Table 6. Control and Status Bits, DLCR8-15

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NODE ID 0 DLCR8	7	6	5	4	3	2	1	0
NODE ID 1 DLCR9	15	14	13	12	11	10	9	8
NODE ID 2 DLCR10	23	22	21	20	19	18	17	16
NODE ID 3 DLCR11	31	30	29	28	27	26	25	24
NODE ID 4 DLCR12	39	38	37	36	35	34	33	32
NODE ID 5 DLCR13	47	46	45	44	43	42	41	40
TDR 0 DLCR14	7	6	5	4	3	2	1	0
TDR 1 DLCR15	N/A (0)	N/A (0)	13	12	11	10	9	8

Table 7. Control and Status Bits, HT8-15

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
HASH TABLE 0 HT8	7	6	5	4	3	2	1	0
HASH TABLE 1 HT9	15	14	13	12	11	10	9	8
HASH TABLE 2 HT10	23	22	21	20	19	18	17	16
HASH TABLE 3 HT11	31	30	29	28	27	26	25	24
HASH TABLE 4 HT12	39	38	37	36	35	34	33	32
HASH TABLE 5 HT13	47	46	45	44	43	42	41	40
HASH TABLE 6 HT14	55	54	53	52	51	50	49	48
HASH TABLE 7 HT15	63	62	61	60	59	58	57	56

Table 8. Status Bits, Packet Buffer Headers

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TRANSMIT PACKET HEADER								
TX LENGTH (LSB) TPH1	7	6	5	4	3	2	1	0
TX LENGTH (MSB) TPH2	N/A (0)	N/A (0)	N/A (0)	N/A (0)	N/A (0)	10	9	8
RECEIVER PACKET HEADER								
PKT STATUS RPH1	N/A (0)	N/A (0)	GOOD PKT	RMT 0900H	SHORT ERR [1]	ALIGN ERR	CRC ERR	N/A (0)
RESERVED RPH2	N/A (0)	N/A (0)	N/A (0)	N/A (0)	N/A (0)	N/A (0)	N/A (0)	N/A (0)
RXLENGTH (LSB) RPH3	7	6	5	4	3	2	1	0
RXLENGTH (MSB) RPH4	N/A (0)	N/A (0)	N/A (0)	N/A (0)	N/A (0)	10	9	8

NOTE:
1. Short Error will be set for packets whose stored length is 3 to 59 bytes.

TRANSMIT STATUS REGISTER

As shown in Table 9, this register provides transmit status for the host processor. The system can enable interrupts based on setting (active high) of bits 7, 3, 2, or 1 of this register by setting the corresponding interrupt enable bits in the Transmit Interrupt Enable register, DLCR4.

Bits 7, 3, 2, and 1 of this register, which can generate interrupts, are cleared by writing a '1' to the bit. Writing '0' to these bits has no effect. Only the MB86964 control logic can set these bits to high. Clearing the bit that causes an interrupt clears the bit and the interrupt. Because two or more status conditions may occur simultaneously, the interrupt routine must read and act on all status conditions that are set.

One method to clear interrupts is to read the contents of the status register, then write the same value back to the register, thus clearing all bits that were set. Another technique is to clear each status bit separately, by writing its mask (interrupt enable) to the register. This might be done as the corresponding interrupt service is performed. Note that wholesale clearing of all status bits by writing FFH to the register is not recommended, because this action may clear a just-set status that has not yet been read by the system. Note also that the transmitter must be idle and TX DONE, DLCR0<7>, must be cleared by writing 1 to it before starting the transmitter by writing 1 to TXSTART, BMPR10<7>.

Table 9. DLCR0 - Transmit Status Register

BIT	SYMBOL	TYPE	DESCRIPTION
7	TX DONE	RC0	**TRANSMIT DONE:** This bit is set high when all packets in the active transmit buffer have been successfully transmitted to the LAN media, or skipped due to excessive collisions. Can generate interrupt if enabled by DLCR2<7>.
6	NET BSY	R	**NET BUSY:** This is a real-time image of the carrier sense signal of the receiver.
5	TX PKT RCD	R0	**TRANSMIT PACKET RECEIVED:** Indicates that a good packet was received shortly after transmission was completed. This is used to indicate self-reception of the packet. This bit is cleared as each transmission begins.
4	CR LOST	R0	**CARRIER LOST:** This bit is set if the receive carrier sense input is negated during a packet transmission. This can be caused by a collision or a shorted LAN medium. It is automatically cleared as each transmission begins.
3	JABBER	RC0	**JABBER:** When active high, indicates excessive transmit length is detected by the JABBER timer. Can generate interrupt if enabled by DLCR2<3>.
2	COL	RC0	**COLLISION:** This bit will assert during transmission of a data packet if a collision occurs on the network. The buffer controller will automatically retransmit the current packet after collisions up to 16 times. The user may read the number of consecutive collisions in collision counter, DLCR4<7:4>. Can generate interrupt if enabled by DLCR2<2>.
1	16 COL	RC0	**16 COLLISIONS:** This bit is set after the sixteenth unsuccessful transmission of the same packet. Can generate interrupt if enabled by DLCR2<1>.
0	0	R0	**RESERVED:** Write 0.

RECEIVE STATUS REGISTER

As shown in Table 10, this register contains eight status bits which can generate interrupts if enabled by the corresponding bit in DLCR3. Five of these bits report the status of the most recently received packet accepted for storage in the receive buffer. Bit 7, RX PKT, is set whenever a new packet is successfully received and stored in the buffer. One bit reports reception of a special packet with 0900H in its type field. Other bits in this register report buffer overflow, DMA end of process, and bus read error. Bits 1, 2 and 3 indicate errors, if any, detected in the packet. If ACPT BAD PKTS bit, DLCR5<5> or ACPT SHORT PKTS bit, DLCR5<3> are set allowing acceptance of a bad packet, these error indicators will be stored in the Status Byte of the Receive Packet Header. If DLCR5<5> and/or DLCR5<3> are both 0, all packets with detected errors are automatically discarded and not stored in the buffer. Bit 4 is also replicated and stored in the packet header status byte which precedes each packet stored in the receive buffer.

The bits in this register, except bit 5, are cleared by writing '1' to the bit. Writing '0' to these bits has no effect. Only internal control logic can set these bits high. Clearing the bit that causes an interrupt clears the bit and the interrupt. Because two or more status conditions can occur simultaneously, the interrupt routine must read and act on all status conditions that are set. One method to clear interrupts is to read the contents of the status register, then write the same value back to the register, thus clearing all bits that were set. Another technique is to clear each status bit separately, by writing its (interrupt enable) mask to the register. This might be done as the corresponding interrupt service is performed. Note that wholesale clearing of all status bits by writing 0FFH to the register is not recommended, because this action may clear a just-set status that has not yet been read by the system.

Table 10. DLCR1 - Receive Status Register

BIT	SYMBOL	TYPE	DESCRIPTION
7	RX PKT	RC0	**RECEIVED PACKET:** Set when a new receive packet is stored in the receive buffer. Can generate interrupt if enabled by DLCR3<7>.
6	BUS RD ERR	RC0	**BUS READ ERROR:** Set when a ready response cannot be issued within 2.4 microseconds after the $\overline{RD}$ signal is asserted. Occurs when reading an empty buffer. Can generate interrupt if enabled by DLCR3<6>.
5	DMA EOP	R0	**DMA END OF PROCESS:** Set when the host DMA asserts the EOP pin indicating that the process is finished. When set, inhibits further assertion of DREQ. Cleared by writing 00H to BMPR12. Can generate interrupt if enabled by DLCR3<5>.
4	RMT CNTRL	RC0	**REMOTE CONTROL PACKET RECEIVED:** This bit is set if DLCR5<2> is set and a packet is received with 0900H in its length/type field (two bytes following the source address, received MSB first). Can generate interrupt if enabled by DLCR3<4>.
3	SHORT PKT ERR	RC0	**SHORT PACKET ERROR:** This bit is set when a packet is received with less than 60 bytes, excluding its preamble and CRC fields. Such a packet usually indicates a collision has truncated its original length, since IEEE 802.3 minimum length is 60 bytes. Can generate interrupt if enabled by DLCR3<3>.
2	ALIGN ERR	RC0	**ALIGNMENT PACKET ERROR:** This bit will assert if a packet is received with an alignment error, meaning there were 1 to 7 extra bits at the end of the packet. Such an occurrence usually indicates a collision, or a faulty transceiver. Can generate interrupt if enabled by DLCR3<2>.
1	CRC ERR	RC0	**CRC PACKET ERROR:** This bit is set if a packet is received with a CRC error. This usually indicates a collision has corrupted the packet. Can generate interrupt if enabled by DLCR3<1>.
0	RX BUF OVRFLO	RC0	**RECEIVE BUFFER OVERFLOW:** This bit will be set if the receive buffer becomes full and must reject a packet for lack of space. Can generate interrupt if enabled by DLCR3<0>.

TRANSMIT INTERRUPT ENABLE REGISTER

As shown in Table 11, this register contains the bits that enable the status bits in DLCR0 to generate interrupts. Only bits 7, 3, 2, and 1 can generate interrupts; the other interrupt enable bits are not used.

RECEIVE INTERRUPT ENABLE REGISTER

As shown in Table 12, this register contains the bits that enable the status bits in DLCR1 to generate interrupts. Refer to Table 13 for information on setting up the various control bits to perform network monitoring and diagnostic functions.

Table 11. DLCR2 - Transmit Interrupt Enable Register

BIT	SYMBOL	TYPE	DESCRIPTION
7	TX DONE INT EN	RW0	**INTERRUPT ENABLE:** When high, enables TX DONE to generate interrupt. Also see DLCR0<7>.
6	0	N0	**RESERVED:** Write 0.
5	0	N0	**RESERVED:** Write 0.
4	0	N0	**RESERVED:** Write 0.
3	JABBER-INT EN	RW0	**INTERRUPT ENABLE:** When high, enables JABBER to generate an interrupt. Also see DLCR0<3>.
2	COL INT EN	RW0	**INTERRUPT ENABLE:** When high, enables COL to generate an interrupt. Also see DLCR0<2>.
1	16 COL INT EN	RW0	**INTERRUPT ENABLE:** When high, enables 16 COL to generate interrupt. Also see DLCR0<1>.
0	0	N0	**RESERVED:** Write 0.

Table 12. DLCR3 - Receive Interrupt Enable Register

BIT	SYMBOL	TYPE	DESCRIPTION
7	RX PKT INT EN	RW0	I**NTERRUPT ENABLE:** When high, enables RX PKT to generate interrupt. Also see DLCR1<7>.
6	BUS ERR INT EN	RW0	**INTERRUPT ENABLE:** When high, enables BUS RD ERR to generate interrupt. Also see DLCR1<6>.
5	DMA EOP INT EN	RW0	**INTERRUPT ENABLE:** When high, enables DMA EOP to generate interrupt. Also see DLCR1<5>.
4	RMT 0900h INT EN	RW0	**INTERRUPT ENABLE:** When high, enables RMT 0900h to generate interrupt. Also see DLCR1<4>.
3	SHT PKT INT EN	RW0	**INTERRUPT ENABLE:** When high, enables SHORT PKT ERR to generate and interrupt. Also see DLCR1<3>.
2	ALIGN ER INT EN	RW0	**INTERRUPT ENABLE:** When high, enables ALIGN ERR to generate interrupt. Also see DLCR1<2>.
1	CRC ERR INT EN	RW0	**INTERRUPT ENABLE:** When high, enables CRC ERR to generate interrupt. Also see DLCR1<1>.
0	RX BF OV INT EN	RW0	I**NTERRUPT ENABLE:** When high, enables RX BUF OVERFLO to generate interrupt. Also see DLCR1<0>.

Table 13. Network Error Monitoring Modes

ACPT BAD PKTS DLCR5<5>	ACPT SHORT PKTS DLCR5<3>	INT EN SHORT PKT ERR DLCR3<3>	INT EN ALIGN ERR DLCR3<2>	INT EN CRC ERR DLCR3<1>	MODE
0	0	X	X	X	Normal operating mode. Only error free packets are saved in the receive buffer. Error interrupts will occur if enabled, when a packet with errors is received.
0	1	0	X	X	Save good packets and short packets if otherwise error-free in buffer. Interrupts only for alignment and CRC errors, if enabled. RX PKT bit DLCR1<7> set high if good or short packet is received.
1	0	0	0	0	Save good packets and packets with short, alignment or CRC errors in buffer. RX PKT bit DLCR1<7> set high if good packet or packet with error is received.
1	1	X	X	X	Not normally used.

TRANSMIT MODE REGISTER

This register, shown in Table 14, contains two control bits associated with transmission, a bit which extends the DMA request and a collision counter. See Table 15 for interpretation of the count value in COL CTR<3:0>.

Table 14. DLCR4 - Transmit Mode Register

BIT	SYMBOL	TYPE	DESCRIPTION
7:4	COL CTR <3:0>	R	**COLLISION COUNT 3 thru 0:** Indicate the number of consecutive collisions encountered by the current transmit packet. Read only. Initial value is not predictable until first packet transmits. See table 17.
3	0	N0	**RESERVED.** Write 0.
2	$\overline{\text{DREQ}}$ $\overline{\text{EXTND}}$	RW1	**DMA REQUEST EXTEND:** When low and DMA mode is in use, extends DMA Request until last transfer cycle. Normally DMA Request terminates after next-to-the-last cycle.
1	$\overline{\text{LBC}}$	RW1	**LOOPBACK CONTROL:** This bit controls encoder/decoder loopback function. A ‘0’ on this bit places MB86964 in internal loopback mode.
0	$\overline{\text{EN\_TX\_DE-FER}}$	RW0	**ENABLE TRANSMIT DEFER:** Program this bit low for normal network operation. When high, the transmitter will not defer to traffic on the network.

Table 15. Collision Count

COLLISION COUNT	16 COL DLCR0<1>	COL CTR3 DLCR4<7>	COL CTR2 DLCR4<6>	COL CTR1 DLCR4<5>	COL CTR0 DLCR4<4>	COL DLCR0<2>
0	0	0	0	0	0	0
1	0	0	0	0	1	1
2	0	0	0	1	0	1
3	0	0	0	1	1	1
4	0	0	1	0	0	1
5	0	0	1	0	1	1
6	0	0	1	1	0	1
7	0	0	1	1	1	1
8	0	1	0	0	0	1
9	0	1	0	0	1	1
10	0	1	0	1	0	1
11	0	1	0	1	1	1
12	0	1	1	0	0	1
13	0	1	1	0	1	1
14	0	1	1	1	0	1
15	0	1	1	1	1	1
16	1	0	0	0	0	1

RECEIVE MODE REGISTER

As shown in Table 16, this register contains six bits that control receiver functions, and one receive buffer status bit.

Status bit RX BUF EMPTY, DLCR5<6>, is necessary to the software routine which reads receive packets from the buffer. It tells the host whether there are any packets in the receive buffer that are complete and ready to read. In a multitasking system, this indicator would be used in conjunction with an interrupt when RX PKT asserts, which means a packet has arrived in memory. The interrupt would be used to start the routine that reads packets from the buffer.

As this routine begins, the interrupt on RX PKT can be disabled to prevent unneeded interrupts. After the first packet is read from the buffer, the RX BUF EMPTY bit would be read to see if more packets have come in (packets may, at times, arrive in bursts). If the buffer is not empty, another packet would be read out, and this procedure repeated until the buffer is empty. After emptying the buffer, the host clears RX PKT, then reenables interrupts on RX PKT, checks the buffer status one more time (because a packet can arrive at any time), then exits to do other tasks. Note that the packet header can reflect acceptance of a short packet (bytes 3 to 59).

Two of the control bits allow reception of packets with certain types of errors. The ACPT BAD PKTS bit, when set, causes the Receiver to retain and store in the buffer packets with CRC, alignment or short-length errors, provided that there was no indication of collision during reception. Likewise, the ACPT SHORT PKTS bit, when set, allows the retention of short packets down to and including only six bytes in length, excluding Preamble and CRC, provided that there was no indication of collision during reception and no alignment or CRC error. Under normal operation, packets with less than 60 bytes, the IEEE 802.3 lower limit, would be discarded. These functions are provided for diagnostic purposes.

Address Filter Mode bits AF1 and AF0 select the destination addresses for which the MB86964 will accept packets for processing. Table 17 provides additional information on the relationship of the setting of these bits with other control bits and how they interact in terms of packet reception.

Table 16. DLCR5 - Receive Mode Register

BIT	SYMBOL	TYPE	DESCRIPTION
7	0	N0	**RESERVED**: Write 0.
6	RX BUF EMPTY	R1	**RECEIVE BUFFER EMPTY:** Status bit which indicates that the receive buffer does not have any complete packets to read.
5	ACPT BAD PKTS	RW0	**ACCEPT BAD PACKETS:** When set high, allows packets with CRC and/or alignment errors or packets that are short to be saved in the receive buffer for analysis. Otherwise such packets would be discarded automatically by the receiver and removed from the buffer.
4	RX SHORT ADDR	RW0	**RECEIVE SHORT ADDRESS:** When set high, instead of customary 48-bit NODE ID address filter, only first 40 bits of NODE ID are compared.
3	ACCPT SHORT PKTS	RW0	**ACCEPT SHORT PACKETS:** When set high, allows short packets (with less than 60 bytes, excluding Preamble and CRC, i.e., below IEEE minimum length) to be saved in the receive buffer. Otherwise such packets would be discarded automatically by the receiver and removed from the buffer.
2	RMT CNTRL EN	RW0	**REMOTE CONTROL ENABLE:** When set high, enables receipt of Remote Control Packets. See DLCR1<4>.
1 0	AF1 AF0	RW1 RW0	**ADDRESS FILTER MODE:** These two bits control the address filtering on incoming packets. Note that self reception of broadcast and multicast packets is prohibited except in accept all packets and loopback modes. When $\overline{\text{LBC}}$ is low (loopback mode), broadcast packets can be self-received, except in reject all packets mode.

AF1	AF0	ACCEPTABLE ADDRESS DESCRIPTIONS
0	1	— NODE ID — Broadcast — Multicast and 2nd-24th bits of NODE ID.
1	0	— NODE ID — Broadcast, — Multicast and Hash Table.
0	0	— Reject all packets.
1	1	— Accept all packets.

Table 17. Reception Destination Address Filtering

RECEIVING FROM OTHER NODES								
AF1	AF0	$\overline{\text{LBC}}$	FILTER SELF RX	NODE ID MATCH[1]		BROADCAST ADDRESS	MUSTICAST PLUS	
DLCR5 <1>	DLCR5 <0>	DLCR4 <1>	BMPR14 <0>	YES	NO		NODE ID <23:1>	HASH TABLE
0	0	X	X	—	—	—	—	—
0	1	0	X	—	—	—	—	—
0	1	1	X	Accept	—	Accept	Accept	—
1	0	0	X	—	—	—	—	—
1	0	1	X	Accept	—	Accept	—	Accept
1	1	0	X	—	—	—	—	—
1	1	1	0	Accept	Accept	Accept	Accept	Accept
1	1	1	1	Accept	Accept	Accept	Accept	Accept
RECEIVING FROM OTHER NODES								
AF1	AF0	$\overline{\text{LBC}}$	FILTER SELF RX	NODE ID MATCH[1]		BROADCAST ADDRESS	MUSTICAST PLUS	
DLCR5 <1>	DLCR5 <0>	DLCR4 <1>	BMPR14 <0>	YES	NO		NODE ID <23:1>	HASH TABLE
0	0	X	X	—	—	—	—	—
0	1	0	X	Accept	—	Accept	Accept	—
0	1	1	X	Accept	—	—	—	—
1	0	0	X	Accept	—	Accept	—	Accept
1	0	1	X	Accept	—	—	—	—
1	1	0	X	Accept	Accept	Accept	Accept	Accept
1	1	1	0	Accept	Accept	Accept	Accept	Accept
1	1	1	1	—	—	—	—	—

1. A NODE ID match occurs when the incoming packet has a destination address whose first bit is a zero, and whose second through forty-eighth bits match bits 1-47 respectiverly of the address stored in the Node ID registers.

CONFIGURATION REGISTERS 0 AND 1

As shown in Tables 18 and 19, system configuration bits are found in these two registers. Among the configuration controls found here are physical memory size, partitioning between transmit and receive buffers, widths of system bus, byte lane control, and power down control. Most configuration parameters are programmed only during initialization, after power start and hardware reset.

Software engineers who want to use the same driver code for the MB86960/64/65 controllers from Fujitsu should note that the driver can determine which chip is being used by reading DLCR7 and DLCR6 after hardware reset. The MB86964 reads 60B6H or 70B6H (60H or 70H for DLCR7 and B6H for DLCR6); the MB86965 reads E0B6H or F0B6H; the MB86960 reads 30B6H or 20B6H.

Power down mode saves power when the MB86964 is not in use. When ready to place the MB86964 chip in power down mode, first write 1 to $\overline{\text{DLC\_EN}}$, DLCR6<7>, to turn off the receiver and transmitter, then write 0 to $\overline{\text{PWRDN}}$, DLCR7<5>. To exit the power down mode, write 1 to $\overline{\text{PWRDN}}$. Register contents are preserved, unless the chip is hardware reset. Hardware reset also terminates the power down mode.

Byte ordering determines in which portion of the data bus the high and low bytes of a word are contained. Refer to the System Interface section for additional information.

Table 18. DLCR6 - Configuration Register 0

BIT	SYMBOL	TYPE	DESCRIPTION
7	$\overline{\text{DLC\_EN}}$	RW1	**DATA LINK CONTROL ENABLE** : When low, enables MB86964 receiver and transmitter sections. This bit must be set high during initialization, and set low to enable loopback testing and operation on the network. Program Node ID and Hash Table only when this bit is high.
6	1	RW0	**Must be set to '1'.**
5	SB/$\overline{\text{SW}}$	RW1	**SYSTEM BYTE/WORD BUS WIDTH:** When high, system bus will operate in 8-bit data mode; when low, 16-bit data mode is selected. The inverse of this bit is output on the SW pin.
4	1	RW1	**Must be set to '1'.**
3 2	TBS1 TBS0	RW0 RW1	**TRANSMIT BUFFER SIZE:** Selects size of transmit buffers.

TBS1:TBS0	TRANSMIT BUFFER QUANTITY	SIZE, EACH TX BUFFER (KBYTES)	SIZE, TOTAL TX BUFFER (KBYTES)
00	1	2	2
01	2	2	4
10	2	4	8
11	2	8	16

1 0	BS1 BS0	RW1 RW0	**BUFFER SIZE:** Selects physical size of the SRAM used for the packet buffer.

BS1	BS0	SRAM SIZE (KBYTES)
0	0	8
0	1	Not valid
1	0	32
1	1	Not valid

Table 19. DLCR7 - Configuration Register 1

BIT	SYMBOL	TYPE	DESCRIPTION
7 6	CID 1 CID 0	R0 R1	**CHIP IDENTIFICATION:** A code which identifies this chip as the MB86964.
5	$\overline{\text{PWRDN}}$	RW1	**POWER DOWN**: When set high, enables power to the chip for all functions; when set low, places chip in power down mode for power conservation.
4	RDYPOL	R 0/1	**READY PIN POLARITY:** Reflects the state of RDYPOL mode setting at pin 36.
3 2	RBS 1 RBS 0	RW0 RW0	**REGISTER BANK SELECT:** Provides the indirect address for selecting one of three sets of registers to access when the physical register address is 08H - 0FH. The lower eight registers are not bank-selectable.

RBS1	RBS0	REGISTERS
0	0	DLCR0 ~ DLCR7, DLCR8 ~ DLCR15
0	1	DLCR0 ~ DLCR7, HT8 ~ HT15
1	0	DLCR0 ~ DLCR7, BMPR 8 ~ BMPR15
1	1	Reserved.

1	EOPPOL	RW0	**EOP PIN SIGNAL POLARITY:** When high, the EOP input pin is active-high; when low, $\overline{\text{EOP}}$ is active-low.
0	M..L / $\overline{\text{L..M}}$	RW0	**BYTE ORDER CONTROL**: Selects byte lane ordering for packet data in the buffer (applies only in system word mode). When this bit is high (M..L mode), the first and all odd-numbered bytes of a packet and its header appear on the high byte of the system bus. When low, the first and all odd-numbered bytes of a packet appear on the low byte. Note that header bytes are also swapped. This bit does not effect data transfers to/from the internal registers, except the buffer port registers BMPR8 and BMPR9.

NODE ID REGISTERS

The Node ID Registers are accessed in register bank ”00” at register addresses 08H - 0DH. During node initialization, the unique Ethernet address assigned to the node is loaded into these registers. The first register at 08H corresponds to the first byte to be received as a packet arrives from the network. If the MB86964 is configured via Address Filter bits DLCR5<1:0> to match node ID, the destination address field of an incoming packet is compared with the contents of these registers. The packet is accepted if it passes the error filter and there is a match.

The Node ID registers are readable and writable registers, and should not be accessed while the Receiver is enabled. To avoid interaction with the Receiver, it is recommended that the Node ID registers be written and read only during initialization, before enabling the receiver, i.e., before writing 0 to $\overline{\text{DLC\_EN}}$. The address contained in the Node ID registers is used only for receive (destination) address filtering, not for the source address of outgoing packets. The system provides outgoing packet addresses as part of the packet data. Within each byte, bits are transmitted and received on the network in a least-significant-bit-first order.

TIME DOMAIN REFLECTOMETRY (TDR) COUNTER

The TDR Counter approximately indicates the location of a fault on the network, if one exists. The TDR Count comes from DLCR14 (the least-significant byte) and DLCR15 (the most-significant byte). The top two bits, DLCR15<7:6>, are always 0.

Refer to the transmitter section for additional information on the TDR counter, performing a TDR test and interpreting the results.

BUFFER MEMORY PORT REGISTER

Buffer Memory Port register BMPR8 provides the host with access to buffer memory. Register Bank Select bits RBS1 and RBS0, DLCR7<3:2>, are set to 1 and 0, respectively, to access the buffer memory port and the other control and status registers described in this section.

Writing a byte/word to BMPR8 transfers that data to the currently addressed location in the transmit buffer, and increments the transmit buffer pointer to point to the next byte/word. Reading a byte/word from this port transfers the contents of the currently addressed location in the receive buffer to the host, and increments the receive buffer pointer to point to the next byte/word.

BMPR9 is used only in word mode as the high byte of the word. In word mode, all transfers must be 16-bits wide, as the Buffer Memory Port register does not support byte-wide transfers in this mode. Odd–length packets are transferred to/from the buffer with an arbitrary 'pad byte at the end. All other registers can be accessed word-wide, high-byte-only or low-byte-only.

TRANSMIT START REGISTER

Table 20 describes the Transmit Start register, BMPR10, which contains the TX START bit and the TX PKT CNT bits. Writing a '1' to the TX START bit immediately starts the transmitter. Transmit Packet Count is a seven-bit binary integer written by the host to indicate the number of packets in the transmit buffer to be transmitted. The Transmit Start register should be written only when the transmitter is idle, but can be read at any time. TX START is always read as a '0' after it is written, but the initial value after reset is indeterminate. The TX PKT CNT field also has an indeterminate value after reset.

16 COLLISIONS CONTROL REGISTER

Table 21 describes the 16 Collisions Control register, BMPR11, which controls action taken when each of 16 consecutive attempts to transmit a packet are met with a collision. The 16 Collisions Control register serves as a mode-select register and an action command register. As a mode select register, two functions are selectable: automatic continuation, or halt after 16 collisions. In either case there is an option to continue attempting to transmit the same packet or skip to the next packet. Table 22 describes the values written to this register to set up the various modes and to restart after a halt.

Table 20. BMPR10 – Transmit Start Register

BIT	SYMBOL	TYPE	DESCRIPTION
7	TX START	RW0/1	**TRANSMITTER START:** Writing 1 to this bit commands the transmitter to start transmitting packets loaded into the transmit buffer. Before doing so, the transmitter must be idle (not busy with another buffer). The TX DONE bit, DLCR0<7>, determines the required transmitter status, idle or busy. Writing a '0' has no effect.
6 - 0	TX PKT CNT 6 - 0	RW0/1	**TRANSMIT PACKET COUNT:** A binary integer written by the system to indicate the number of packets contained in the transmit buffer for transmission. This information can be loaded at the same time the TX START bit is set high. As the Transmitter finishes transmitting each packet, this counter is decremented. The value can be read by the system to see how many packets remain to be transmitted.

Table 21. BMPR11 - 16 Collisions Control Register

BIT	SYMBOL	TYPE	DESCRIPTION
7 - 3	N0	N0	**RESERVED:** Write 0.
2	16 COL HALT	RW0	**16 COLLISION HALT:** If this bit is set to '0', transmission halts after 16 consecutive collisions. If this bit is set to '1', the transmitter will continue to make transmission attempts after 16 consecutive collisions.
1	16 COL RESTART	RW0	**16 COLLISION RESTART:** When bit 2 is set to '0' selecting 'halt after 16 collisions', the transmitter can be restarted when it has halted by writing a '1' to this bit. When transmission of a packet begins, this bit is cleared automatically. Serves no function if bit 2 is set to '1' for 'automatic continuation'.
0	16 COL DISCARD	RW0	**16 COLLISION DISCARD**: Selects whether the transmitter will retransmit or discard the current packet after the 16th consecutive collision occurs. When set to 0, the transmitter will continue to retransmit the current packet. When set to 1, the transmitter will discard the current packet and go on to the next packet in the buffer, if there is one, or quit if there are no more packets.

Table 22. Collision Action Codes Written to BMPR11

ACTION CODE	ACTIONS
02H or 03H	**MODE SETUP:** Halt after 16 collisions.
02H	**COMMAND**: Resume transmitting, repeat current packet. For use following a halt. Terminates the halt. Instructs transmitter to resume transmitting, repeating the current packet. The collision counter is reset, allowing up to 16 additional attempts to be made. Transmitter will again halt after 16 collisions.
03H	**COMMAND**: Resume transmitting, skip failed packet. For use following a halt. Terminates the halt. Instructs transmitter to skip the failed packet and resume transmitting with the next packet in the buffer. The collision counter is reset, allowing up to 16 additional attempts to be made. If there is no next packet, the transmitter deactivates, setting TX DONE bit, DLCR0<7>, as it does so. The transmitter halts after 16 collisions.
06H	**MODE SETUP**: Continue automatically after 16 collisions, repeat failed packet. Note that if the network medium disconnects, transmission attempts usually result in false collision detection. Under this condition, this mode causes transmitter to continue attempting transmission of the same packet indefinitely. Interrupt or periodic polling of the status bits could detect this condition.
07H	**MODE SETUP:** Continue automatically after 16 collisions, skip failed packet. Note that this mode results in failure to transmit some packets, because it skips a packet that has had 16 consecutive collisions. While this condition is rare on a healthy network, it does occur occasionally.

DMA ENABLE REGISTER

Table 23 describes the DMA Enable register, BMPR12, a register that enables or clears receive read DMA or transmit write DMA.

Table 23. BMPR12 - DMA Enable Register

BIT	SYMBOL	TYPE	DESCRIPTION
7 - 2	0	N0	**RESERVED**: Write 0.
1	RX DMA EN	RW0	**RECEIVE DMA ENABLE** When set to 0, disables DMA read. When set to 1, enables DMA read.
0	TX DMA EN	RW0	**TRANSMIT DMA ENABLE**: When set to 0, disables DMA write. When set to 1, enables DMA write.

RX DMA EN	TX DMA EN	ACTIONS
0	0	Clear or terminate DMA activity, DMA EOP status bit and associated interrupt, if any. Normally used as response to end of process (DMA EOP) interrupt.
0	1	Enable transmit write DMA.
1	0	Enable receive read DMA.

DMA BURST AND TRANSCEIVER MODE REGISTER

Table 24 describes the DMA Burst and Transceiver Mode register, BMPR13, which selects the burst length for DMA operation and programs the 10BASE-T transceiver modes. Burst length is defined as the number of data transfers occurring during one acquisition of the system bus. After the programmed number of transfers, the bus is released and a new bus arbitration cycle will be started. Each transfer is one word or one byte, depending on System Byte/System Word mode selected via DLCR6<5>.

Table 24. BMPR13 - DMA Burst and Transceiver Mode Register

BIT	SYMBOL	TYPE	DESCRIPTION
7	1	N0	**Reserved.**
6	LOWER SQLCH THRESH	WR0	**LOWER SQUELCH THRESHOLD**: When set to 1, reduces twisted-pair squelch threshold by 4.5 dB. When set to 0, twisted-pair squelch threshold is normal.
5	$\overline{\text{LINK\_TEST\_EN}}$	WR0	**LINK TEST ENABLE**: When set to 1, disables transmit and receive link integrity test functions. When set to 0, enables link integrity test.
4	AUI/$\overline{\text{TP}}$	WR0	**AUI /TP PORT SELECT**: When $\overline{\text{AUTO PORT SEL}}$ECT bit, BMPR13<3>, is set to 1, this bit selects the active network port. When set to 1, the AUI port is selected. When set to 0, the 10BASE-T twisted-pair port is selected.
3	$\overline{\text{AUTO PORT SEL}}$	WR0	**AUTOMATIC PORT SELECTION:** When set to 0, automatic port selection mode is in effect. Defaults to the AUI port if twisted-pair link integrity fails. When set to 1, allows port selection via AUI/$\overline{\text{TP}}$ bit, BMPR13<4>.
2	STP/$\overline{\text{UTP}}$	WR0	**STP/$\overline{\text{UTP}}$ SELECT:** When set to 1, selects 150 Ω termination for shielded twisted pair. When set to 0, selects 100 Ω termination for unshielded twisted pair.
1 0	BURST 1 BURST 0	WR0 WR0	**BURST CONTROL:** Selects the burst length for DMA operation.

BURST 1	BURST 0	BURST LENGTH (TRANSFERS)
0	0	1
0	1	4
1	0	8
1	1	12

FILTER SELF RECEIVE REGISTER

Table 25 describes the Filter Self Receive Register, BMPR14. [Also refer to Table 17 for more information about the Filter Self Receive function.]

Writing a '1' to bit 2 of this register commands the buffer controller to skip the balance of the current receive packet in memory. The bit can then be read to determine that completion of the skip process is complete (within 300 ns). If there is another packet, the bit returns to 0 when the chip is ready to read the next packet or, if there is not another packet, stop reading. Do not use this feature before reading at least four times from the beginning of the packet, nor if there are eight or fewer bytes left of the packet in the buffer; doing so may corrupt the receive buffer pointers.

As shown in the table, this register also provides control for enabling interrupts based on the setting of status bits in BMPR15, the Transceiver Status Register.

Table 25. BMPR14 - Filter Self Receive Register

BIT	SYMBOL	TYPE	DESCRIPTION
7	RLD INT EN	RW0	**INTERRUPT ENABLE:** When high, enables RLD, BMPR15<7>, to generate an interrupt.
6	LLD INT EN	RW0	**INTERRUPT ENABLE:** When high, enables LLD, BMPR15<6>, to generate an interrupt.
5	RJAB INT EN	RW0	**INTERRUPT ENABLE:** When high, enables RJAB, BMPR15<5>,, to generate an interrupt.
4	0	N0	**RESERVED**: Write 0.
3	0	N0	**RESERVED**: Write 0.
2	SKIP PKT	RW0	**SKIP RECEIVED PACKET:** When '1' is written to this bit, flushes remainder of the current received packet. Adjusts the system read pointer to the beginning of the next received packet, if there is one, or to the end of the buffer if there is not.
1	INT EN	RW0	I**NTERRUPT ENABLE:** When high, enables SQE, DLCR15<1>, to generate an interrupt.
0	FILTER SELF RX	RW1	**FILTER SELF RECEIVE**: When set to 1, disables the accept all packets mode self receive function. When set to 0, enables the self receive function in accept all packets mode.

TRANSCEIVER STATUS REGISTER

Table 26 describes the Transceiver Status Register, BMPR15. Writing a '1' to bits <7:3> and <1> of this register clears the respective status condition. Writing '0' to these bits has no effect.

Table 26. BMPR15 -Transceiver Status Register

BIT	SYMBOL	TYPE	DESCRIPTION
7	RLD	RC0/1	**REMOTE LINKDOWN:** When high and bit 4 is also high, indicates that remote 10BASE-T port is in linkdown condition. Can generate interrupts if enabled by interrupt enable bit BMPR14<7>.
6	LLD	RC0/1	**LOCAL LINK DOWN:** When high, indicates that local 10BASE-T port is in link down condition. Can generate interrupts if enabled by interrupt enable bit BMPR14<6>.
5	RJAB	RC0/1	**REMOTE JABBER:** When high and bit 4 is also high, indicates that remote 10BASE-T port is in Jabber condition. Can generate interrupts if enabled by interrupt enable bit BMPR14<5>.
4	RMT PORT	RC0/1	**REMOTE SIGNALING:** When high, indicates that the remote 10BASE-T port has remote function signaling compatible with that of the MB86964. When this is the case, the RLD and RJAB status is valid and is being continuously updated by the remote port. When this bit is low, RLD, and RJAB are meaningless.
3	RXI POL REV	RC0/1	**RXI POLARITY REVERSAL**: When high, indicates reversed polarity on the 10BASE-T receive line.
2	0	N0	**RESERVED**: Write 0.
1	SQE	RC0	**SIGNAL QUALITY ERROR:** When set to 1, indicates detection of SQE. Can generate interrupts if enabled by interrupt enable bit BMPR14<1>.
0	0	N0	**RESERVED**: Write 0.

ELECTRICAL CHARACTERISTICS

All specifications are valid over the Recommended Operating Conditions unless otherwise noted.

OPERATIONAL SPECIFICATIONS

Table 27. Absolute Maximum Ratings

SYMBOL	PARAMETER DESCRIPTION	MINIMUM	MAXIMUM	UNITS
V_{CC}	Supply voltage	– 0.5	6.0	V
V_{IN}	Input voltage	– 0.5	VCC+ 0.5	V
V_{OUT}	Output voltage	– 0.5	VCC + 0.5	V
I_{ODF}	Differential output current on DOP pins		–40	mA
V_{IDC}	Input DC voltage on DIP and CIP	– 0.5	16	V
V_{ODC1}	Output DC voltage on DOP without transformer	– 0.5	14	V
V_{ODC2}	Output DC voltage on DOP with transformer	– 0.5	16	V
T_{BIAS}	Temperature under bias	– 25	+85	° C
T_{STG}	Storage temperature	– 40	+125	° C
P_D	Power dissipation		787.5	mw

Permanent device damage may occur if absolute maximum ratings are exceeded. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. No more than one output may be shorted to ground or VCC at a time for a maximum duration of one second.

Table 28. Recommended Operating Conditions

SYMBOL	PARAMETER DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNITS
V_{DD}	Supply voltage	4.75		5.25	V
V_{IH}	Logic input high voltage	2.4			V
V_{IL}	Logic input low voltage			0.4	V
C_{OSC}	Oscillator load capacitors	12	20	38	pF
R_{BIAS}	Bias resistor from RBIAS pin to ground	12.28	12.4	12.52	kΩ
f_{XTAL}	Crystal oscillator frequency	19.999	20	20.001	MHz
T_A	Operating temperature	0		+70	° C

See figure 11 for recommended terminations for the AUI and twisted-pair ports.

Table 29. DC Specifications

SYMBOL	PARAMETER DESCRIPTION	CONDITIONS	MINIMUM	TYPICAL	MAXIMUM	UNITS
V_{IL}	Low-level input voltage		0.0		0.8	V
V_{IH}	High-level input voltage		2.2		VCC	V
V_{OL1}	Low-level output voltage, SD<15:0> only	I_{OL} = 12 mA	0.0		0.4	V
V_{OH1}	High-level output voltage, SD<15:0> only	I_{OH}= –4 mA	4.2		V_{CC}	V
V_{OL2}	Low-level output voltage, all other digital outputs	I_{OL} = 3.2 mA	0.0		0.4	V
V_{OH2}	High-level output voltage, all other digital outputs	I_{OH} = –2 mA	4.2		VCC	V
I_L	Input leakage current	V_I = 0 – V_{CC}	–10		10	µA
I_{PWRDN}	Power down V_{CC} current	No output loads		4	10	mA
I_{IDLE}	Idle V_{CC} current	No output loads		83	100	mA
I_{CC}	Operating V_{CC} current	No output loads except 10BASE-T network connection		110	150	mA

Table 30. General Capacitance

SYMBOL	PARAMETER DESCRIPTION	MINIMUM	MAXIMUM	UNITS
C_{IN}	Input pin capacitance		16	pF
C_{OUT}	Output pin capacitance		16	pF
$C_{I/O}$	I/O pin capacitance		16	pF
T_A = 25° C, V_{DD} = V_I = 0 volts, and f = 1 megahertz				

Table 31. AUI Electrical Characteristics

SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS
I_{IL}	Input low current[1]			700	µA
I_{IH}	Input high current[1]			-500	µA
Z_{IN}	Receiver input impedance DIP/DIN and CIP/CIN		20		kΩ
V_{OD}	Differential output voltage on DOP/DON	±550		±1200	mV
V_{ACCM}	AC common mode on DOP/DON			±40	mV
V_{DCCM}	DC common mode on DOP/DON	2.4	3.4	4.4	V
V_{SQ}	Differential squelch threshold on DIP/DIN[1]	–300	–220	–140	mV
V_{CM}	Differential common mode voltage on DIP/DIN	–5.25		5.25	V

1. Values are at 25° C and are used for design aid only; not guaranteed and not subject to production testing.

Table 32. Twisted-pair Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	MAXIMUM	UNITS
Z_{OUT}	Transmit output impedance		5		Ω
V_{OD}	Peak differential output voltage at TPOP/TPON	Line impedance = 100 ohms	3.5		V
J_{OUT}	Transmit timing jitter addition Parameter is guaranteed by design; not subject to product testing.	0 line length After line model specified by IEEE 802.3 for 10BASE-T		±8 ±3.5	ns
Z_{IN}	Receive input impedance TPIP/TPIN		20		kΩ
V_{DS}	Differential squelch threshold	BMPR13<6> = 0	420		mV
V_{DSL}	Lower squelch threshold	BMPR13<6> = 1	250		mV

Typical figures are at 25° C and are used for design aid only; not guaranteed and not subject to production testing.

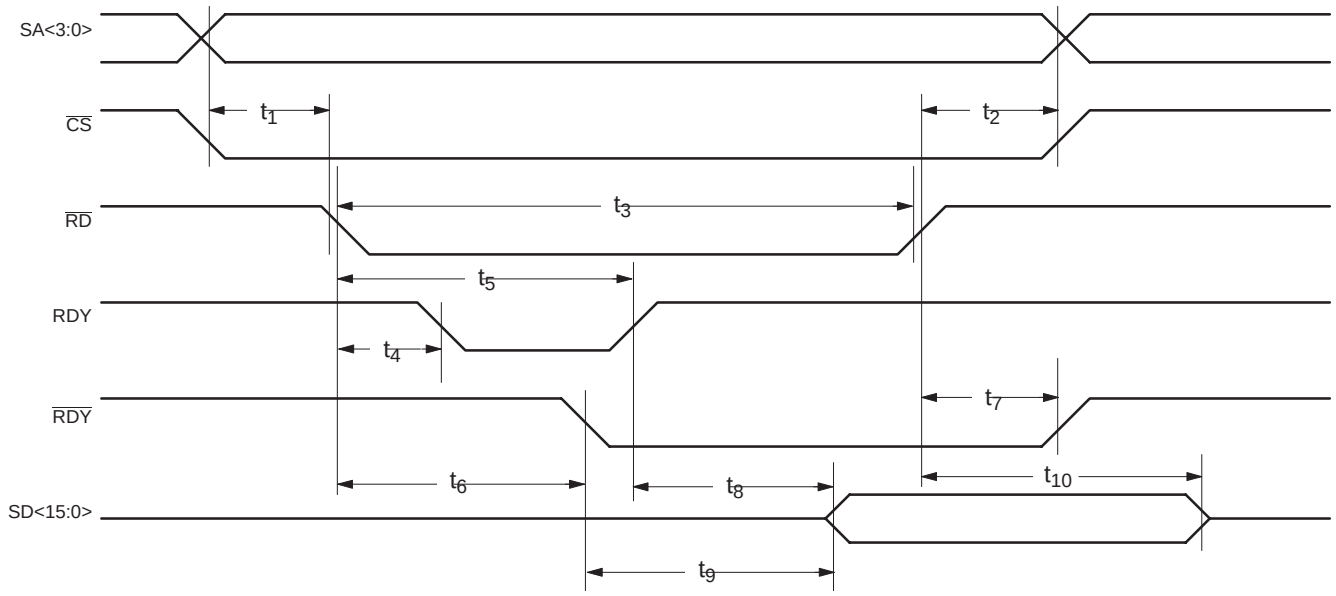
Table 33. Jabber and Link Test Timing

SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS
Jabber Timing	Maximum transmit time Unjab time	20 250		150 750	ms
Link Test Timing	Time between link test pulses Link loss timeout	8 55		24 66	ms

TIMING DIAGRAMS

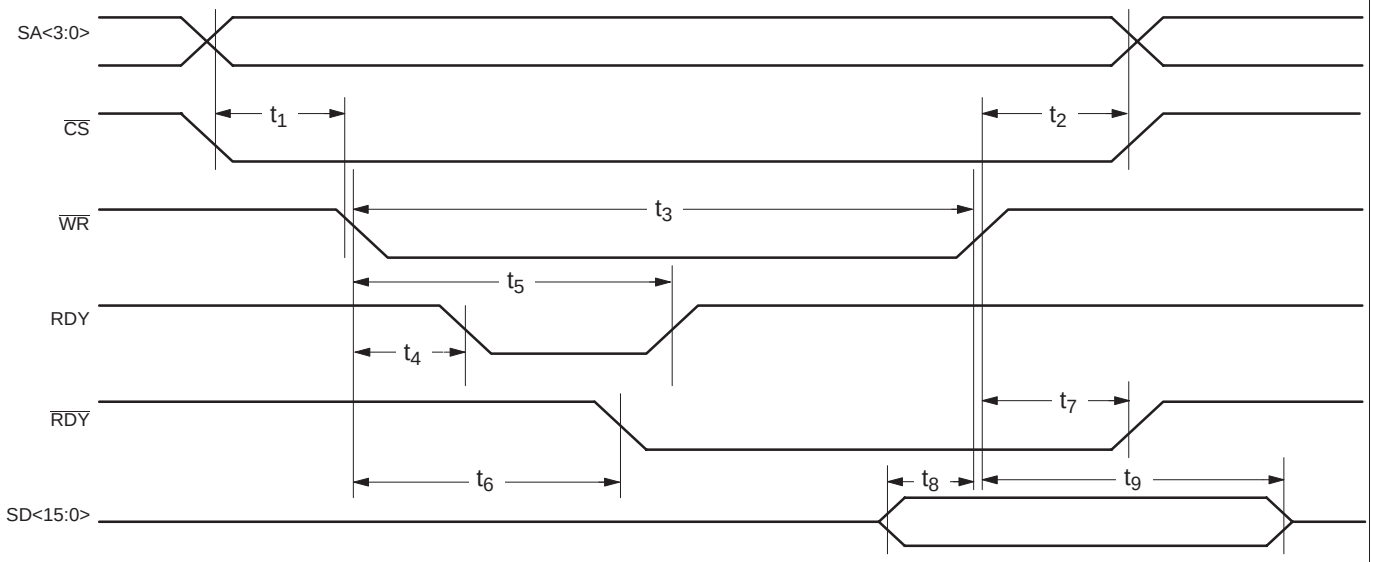
All specifications are valid over the Recommended Operating Conditions unless otherwise noted.

Table 34. Read Cycle



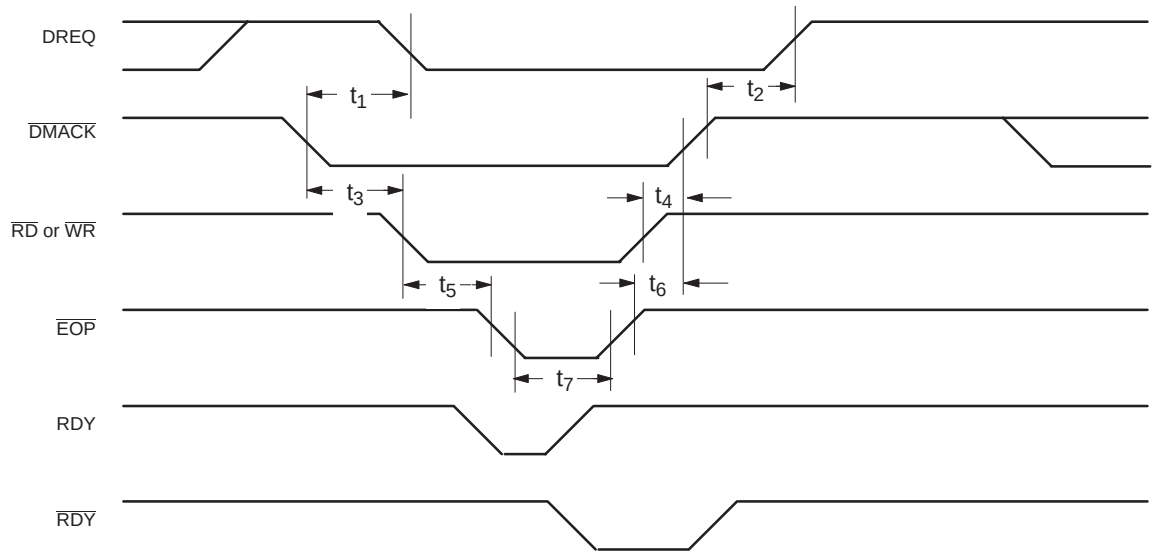
SYMBOL	PARAMETER DESCRIPTION	MINIMUM	MAXIMUM	UNITS
t_1	SA<3:0> valid to $\overline{RD}$ low; $\overline{CS}$ low to $\overline{RD}$ low.	3		ns
t_2	$\overline{RD}$ high to SA<3:0> invalid; $\overline{RD}$ high to $\overline{CS}$ high.	3		ns
t_3	$\overline{RD}$ low pulse width.	30		ns
t_4	$\overline{RD}$ low to RDY low.	0	26	ns
t_5	$\overline{RD}$ low to RDY high.			
	For registers and buffer port when port is ready before the read cycle begins.	0	7	ns
	For port access only, if system attempts to make contiguous system read cycles at less than 100 ns intervals, and the network is busy.	0	175	ns
	For bus read error.	0	2.15	µs
t_6	$\overline{RD}$ low to $\overline{RDY}$ low:			ns
	For all registers.	0	28	ns
	For port access only, if system attempts to make contiguous system read cycles at less than 100 ns intervals, and the network is busy.	0	175	ns
	For bus read error.	0	2.15	µs
t_7	$\overline{RD}$ high to $\overline{RDY}$ high.		28	ns
t_8	RDY high to SD<15:0> valid.		8	ns
t_9	$\overline{RDY}$ low to SD<15:0> valid.		10	ns
t_{10}	$\overline{RD}$ high to SD<15:0> invalid.	15	25	ns

Table 35. Write Cycle



SYMBOL	PARAMETER DESCRIPTION	MINIMUM	MAXIMUM	UNITS
t_1	SA<3:0> valid to $\overline{WR}$ low; $\overline{CS}$ low to $\overline{WR}$ low.	3		ns
t_2	$\overline{WR}$ high to SA<3:0> invalid; $\overline{WR}$ high to $\overline{CS}$ high.	3		ns
t_3	$\overline{WR}$ low pulse width.	36		ns
t_4	$\overline{WR}$ low to RDY low.	0	26	ns
t_5	$\overline{WR}$ low to RDY high:			ns
	For registers and buffer port when port is ready before the write cycle begins.	0	7	ns
	For port access only, if system attempts to make contiguous system write cycles at less than 100-ns intervals, and both the transmitter and receiver are active in loopback reception.	0	175	ns
t_6	$\overline{WR}$ low to $\overline{RDY}$ low.			ns
	For all registers.	0	28	ns
	For port access only, if system attempts to make contiguous system write cycles at less than 100-ns intervals, and transmitter and receiver are active in loopback reception.	0	175	ns
t_7	$\overline{WR}$ high to $\overline{RDY}$ high.		28	ns
t_8	SD<15:0> valid to $\overline{WR}$ high.	5		ns
t_9	$\overline{WR}$ high to SD<15:0> invalid.	6		ns

Table 36. Single-cycle DMA Timing

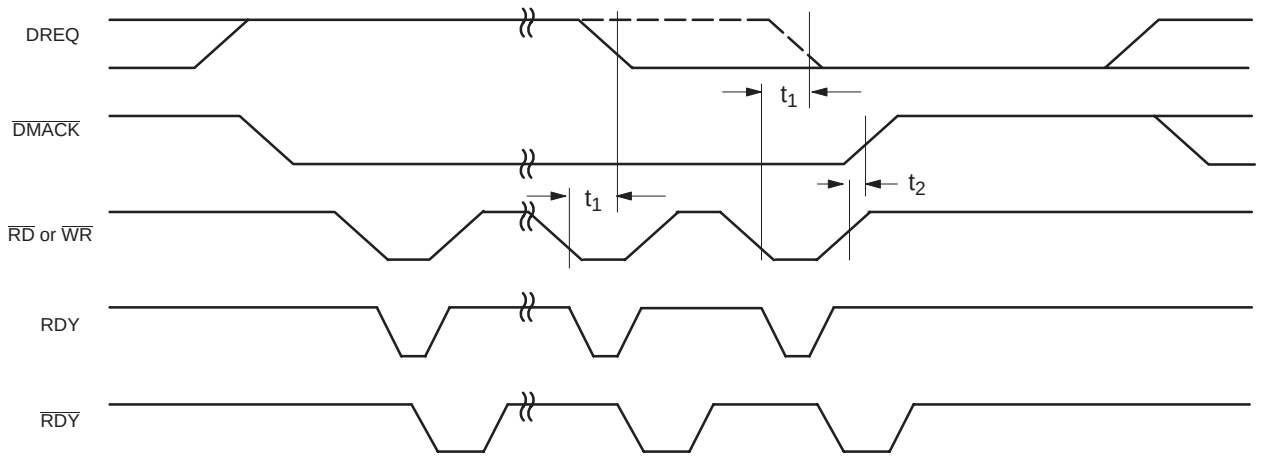


SYMBOL	PARAMETER DESCRIPTION	MINIMUM	MAXIMUM	UNITS
t_1	$\overline{DMACK}$ low to DREQ low	0	21	ns
t_2	$\overline{DMACK}$ high to DREQ high	0	19	ns
t_3	$\overline{DMACK}$ low to $\overline{RD}$ or $\overline{WR}$ low	0		ns
t_4	$\overline{RD}$ or $\overline{WR}$ high to $\overline{DMACK}$ high	3		ns
t_5	$\overline{RD}$ or $\overline{WR}$ low to $\overline{EOP}$ low[2]	0		ns
t_6	$\overline{EOP}$ high to $\overline{DMACK}$ high[2]	3		ns
t_7	$\overline{EOP}$ low pulse width[2]	10		ns

1. All of the $\overline{RD}$, $\overline{WR}$ and $\overline{EOP}$ asserted pulses must fall inside of the $\overline{DMACK}$ asserted pulse. An asserted $\overline{EOP}$ terminates any further DREQ after $\overline{DMACK}$ returns high. The DMA cycle uses $\overline{DMACK}$ as the chip select. $\overline{DMACK}$ overrides SA<3:0>, forcing selection of the buffer memory port in a DMA cycle.

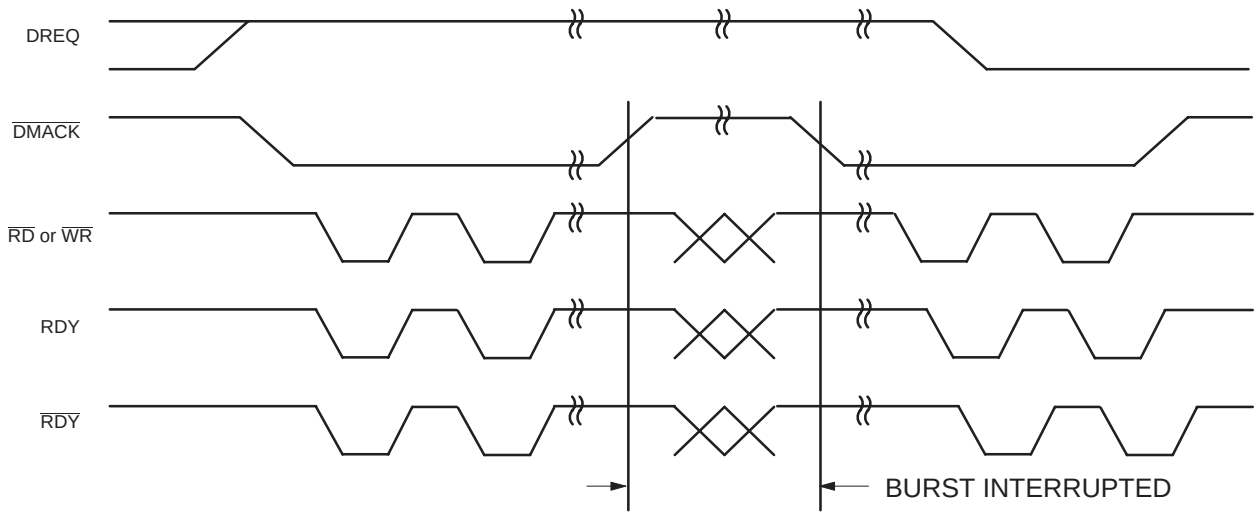
2. Timing shown for $\overline{EOP}$ also applies to EOP when EOP($\overline{EOP}$) is programmed to be asserted high.

Table 37. Burst DMA Timing



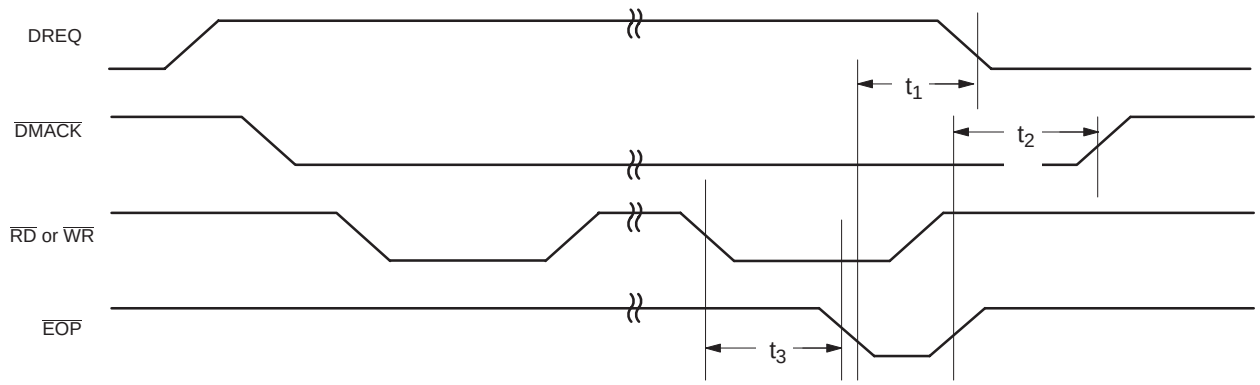
SYMBOL	PARAMETER DESCRIPTION	MINIMUM	MAXIMUM	UNITS
t_1	RD or WR low to DREQ low		32	ns
t_2	RD or WR high to DMACK high	3		ns

All of the RD or WR asserted pulse must fall inside of the DMACK asserted pulse. The DMA cycle uses DMACK as the chip select. DMACK overrides SA<3:0>, forcing selection of the buffer memory port. DREQ goes low during the next-to-last transfer of the burst if DLCR4<2> = 1, and can be extended to the last transfer cycle by setting DLCR4<2> = 0.



Burst can be interrupted by negating DMACK. Burst will resume when DMACK is reasserted.

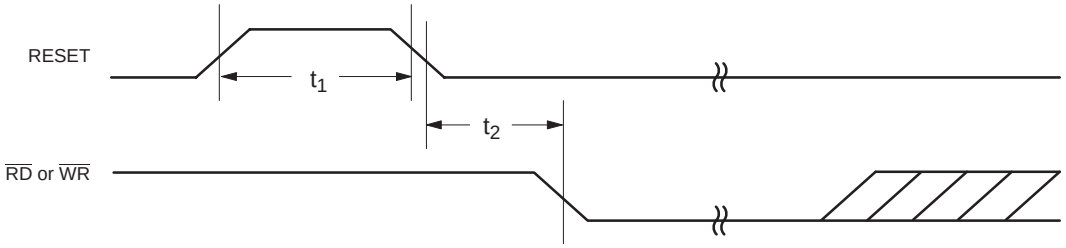
Table 38. Burst DMA terminated by EOP



SYMBOL	PARAMETER DESCRIPTION	MINIMUM	MAXIMUM	UNITS
t_1	$\overline{EOP}$ low to DREQ low	4	28	ns
t_2	$\overline{EOP}$ high to $\overline{DMACK}$ high	3		ns
t_3	$\overline{RD}$ or $\overline{WR}$ low to $\overline{EOP}$ low	0		ns

Timing shown for $\overline{EOP}$ also applies to EOP when EOP($\overline{EOP}$) is programmed to be asserted high.

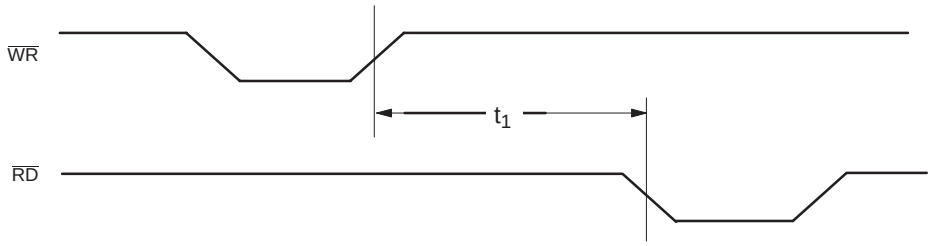
Table 39. RESET Timing



SYMBOL	PARAMETER DESCRIPTION	MINIMUM	MAXIMUM	UNITS
t_1	RESET pulse width	200		ns
t_2	RESET low to first $\overline{RD}$ or $\overline{WR}$ low	300		ns

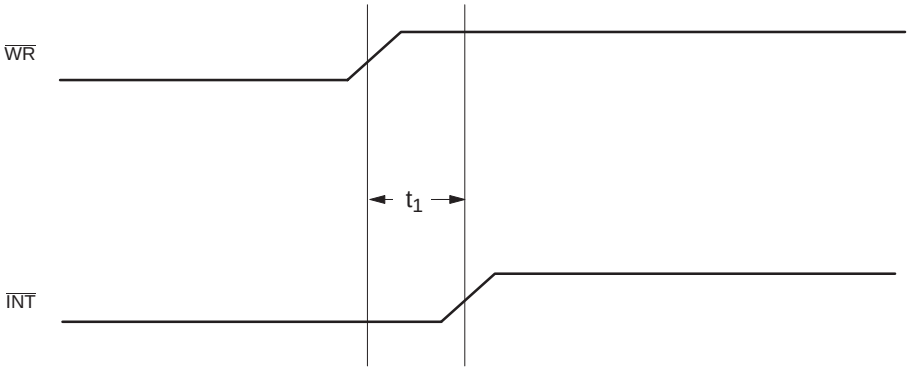
Wait 200 µsec after reset pulse for stabilization of receiver PLL before enabling transmit and receive functions.

Table 40. Skip Packet Timing



SYMBOL	PARAMETER DESCRIPTION	MINIMUM	MAXIMUM	UNITS
t_1	Writing skip packet high to next Buffer Memory Port read	300		ns

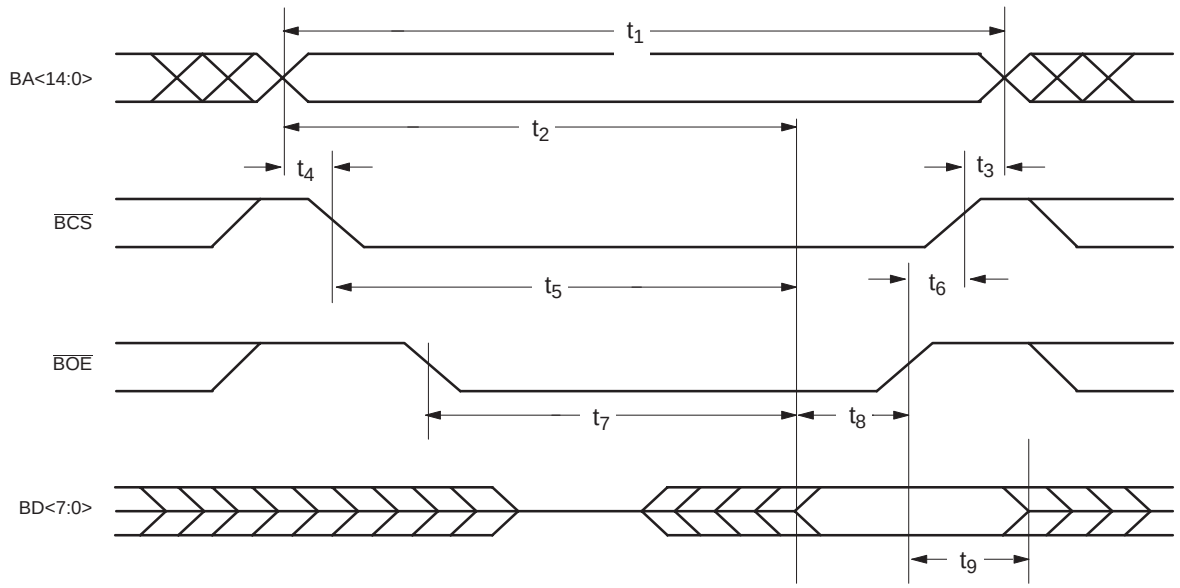
Table 41. INT Clear Timing



NOTE: When writing a command to clear interrupt bit(s), the data transfer takes place after the rising edge of the write pulse.

SYMBOL	PARAMETER DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNITS
t_1	INT signal-clearing delay	30		80	ns

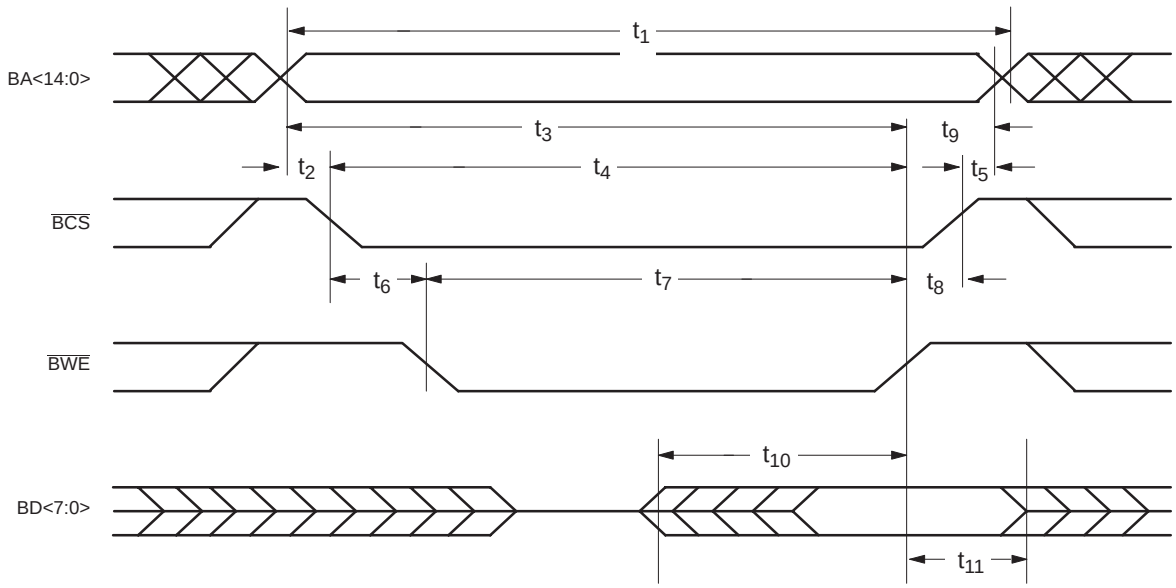
Table 42. SRAM Read Timing



SYMBOL	PARAMETER DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNITS
t_1	Read cycle	95	100	105	ns
t_2	T_{AA}, address access time			81	ns
t_3	$\overline{BCS}$ high to address invalid	0			ns
t_4	Address valid to $\overline{BCS}$ low	0		8	ns
t_5	$T_{AC,}$ chip select access time			81	ns
t_6	$\overline{BOE}$ high to $\overline{BCS}$ high	0		2	ns
t_7	$T_{OE,}$ output enable access time			49	ns
t_8	Data setup time	15			ns
t_9	Data hold time	0			ns

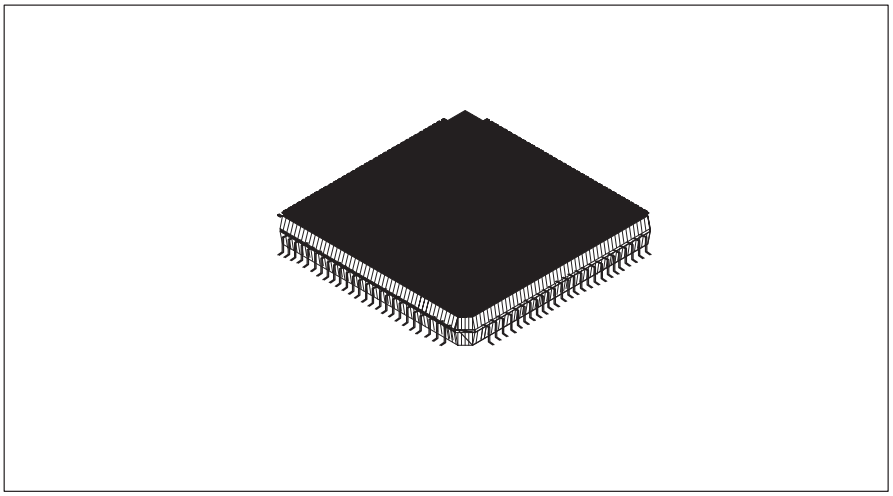
Use SRAM with T_{AA} of 80 ns or less.

Table 43. SRAM Write Timing



SYMBOL	PARAMETER DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNITS
t_1	Write cycle	95	100	105	ns
t_2	Address valid to $\overline{BCS}$ low	2		8	ns
t_3	Address valid to $\overline{BWE}$ high	71			ns
t_4	$\overline{BCS}$ low to $\overline{BWE}$ high	62			ns
t_5	$\overline{BCS}$ high to address invalid	0			ns
t_6	$\overline{BCS}$ low to $\overline{BWE}$ low	0			ns
t_7	$\overline{BWE}$ Pulse Width	60			ns
t_8	$\overline{BWE}$ high to $\overline{BCS}$ high	0			ns
t_9	$\overline{BWE}$ high to address invalid	12			ns
t_{10}	Data setup time	41			ns
t_{11}	Data hold time	14			ns

PACKAGE INFORMATION



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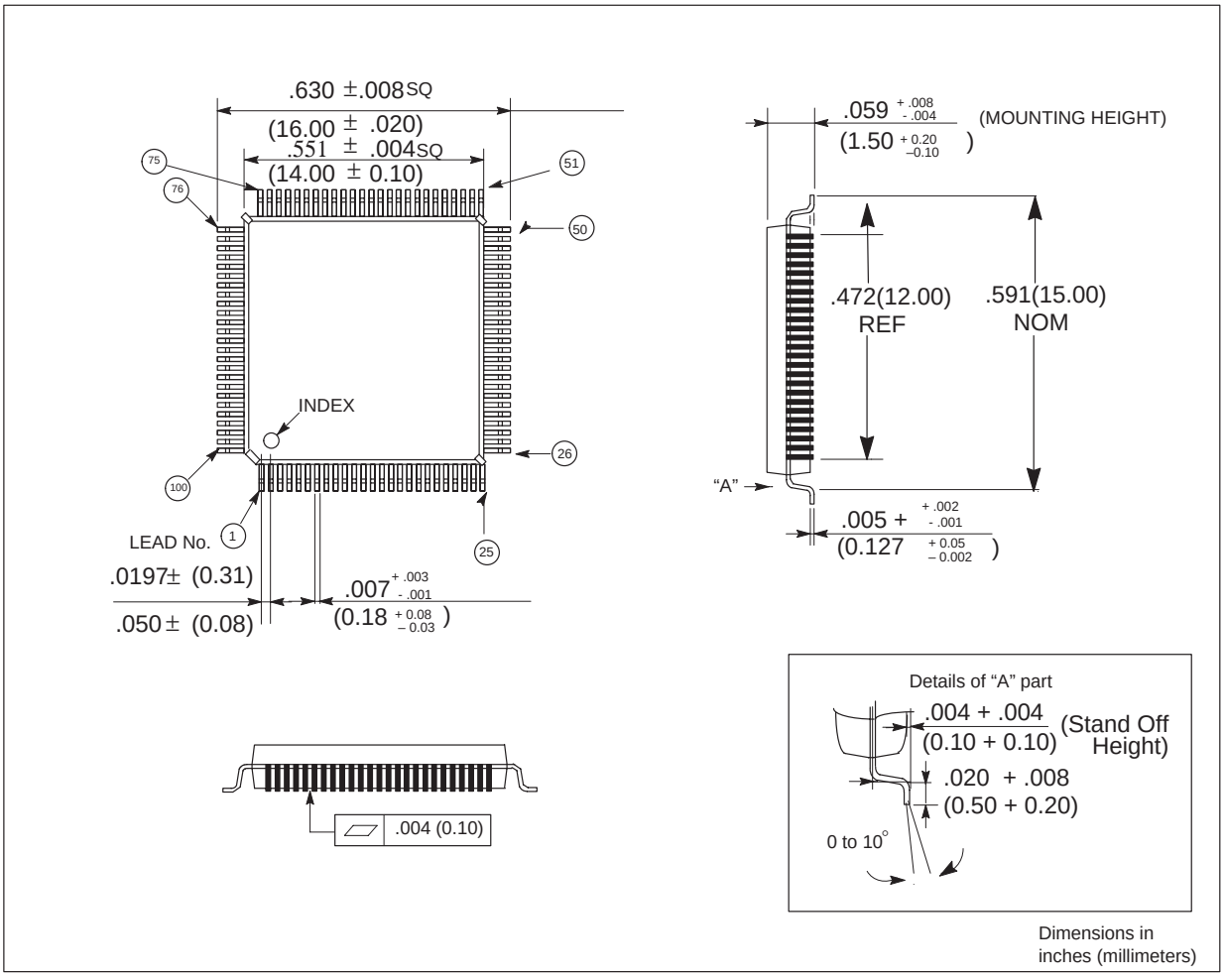

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