FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-12101-2E

MEMORY

CMOS 2 × 128K × 32 SYNCHRONOUS GRAM

MB81G83222-010/-012/-015

**CMOS 2 BANKS OF 131,072-WORDS × 32-BIT
SYNCHRONOUS GRAPHIC RANDOM ACCESS MEMORY**

■ DESCRIPTION

The Fujitsu MB81G83222 is a CMOS Synchronous Graphic Random Access Memory (SGRAM) containing 8,388,608 memory cells accessible in an 32-bit format. The MB81G83222 features a fully synchronous operation referenced to a positive edge clock whereby all operations are synchronized at a clock input which enables high performance and simple user interface coexistence. The MB81G83222 SGRAM is designed to reduce the complexity of using a standard dynamic RAM (DRAM) which requires many control signal timing constraints, and may improve data bandwidth of memory as much as 5 times more than a standard DRAM.

The MB81G83222 is ideally suited for Graphics workstations, laser printers, high resolution graphic adapters, accelerators and other applications where an extremely large memory and bandwidth are required and where a simple interface is needed.

■ ABSOLUTE MAXIMUM RATINGS (See NOTE)

Parameters	Symbol	Value	Unit
Voltage of V_{CC} Supply relative to V_{SS}	V_{CC}, V_{CCQ}	–0.5 to +4.6	V
Voltage at any pin relative to V_{SS}	V_{IN}, V_{OUT}	–0.5 to +4.6	V
Short Circuit Output Current	I_{OUT}	±50	mA
Power Dissipation	P_D	1.2	W
Storage Temperature	T_{STG}	–55 to +125	°C

NOTE: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

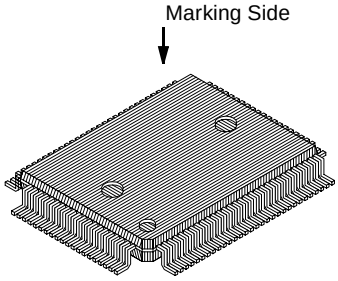
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

■ PRODUCT LINE & FEATURES

Parameter	MB81G83222-010	MB81G83222-012	MB81G83222-015
Clock Frequency	100 MHz max.	84 MHz max.	67 MHz max.
Burst Mode Cycle Time	10 ns min.	12 ns min.	15 ns min.
$\overline{RAS}$ Access Time	58 ns max.	67 ns max.	75 ns max.
$\overline{CAS}$ Access Time	28 ns max.	32 ns max.	35 ns max.
Access Time From Clock (CL=3)	9 ns min.	11 ns min.	12 ns min.
Operating Current (Two banks active)	280 mA max.	245 mA max.	210 mA max.
Power Down Mode Current	2 mA max.		

- Single +3.3V Supply ±10% tolerance
- LVTTL compatible I/O
- 1,024 refresh cycles every 16.4 ms
- Dual bank operation
- Byte control by DQM_0 to DQM_3
- Burst read/write operation and burst read/single write operation capability
- Programmable burst type, burst length, and CAS latency
- 8 column block write function
- Write per bit function (old mask)
- Auto-and Self-refresh
- CKE power down mode
- Output Enable and Input Data Mask

■ PACKAGE



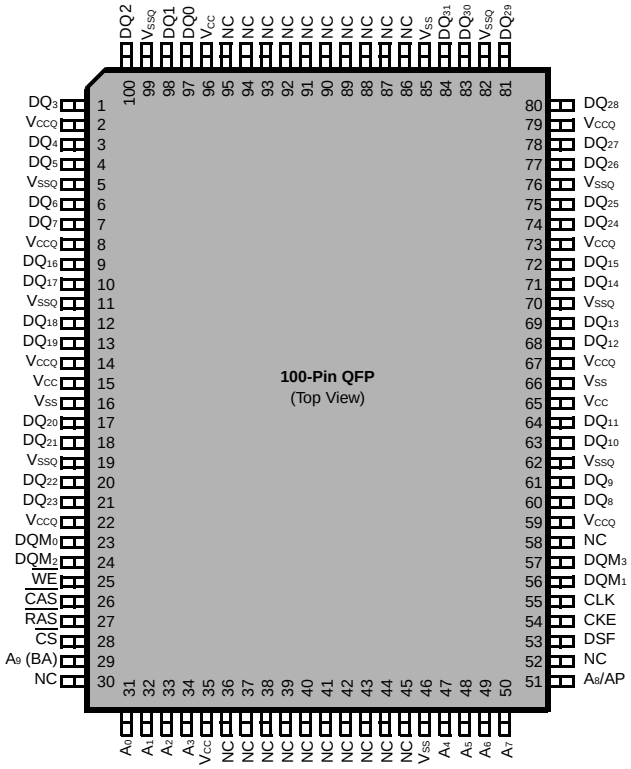
FPT-100P-M15

Plastic QFP Package

Package and Ordering Information

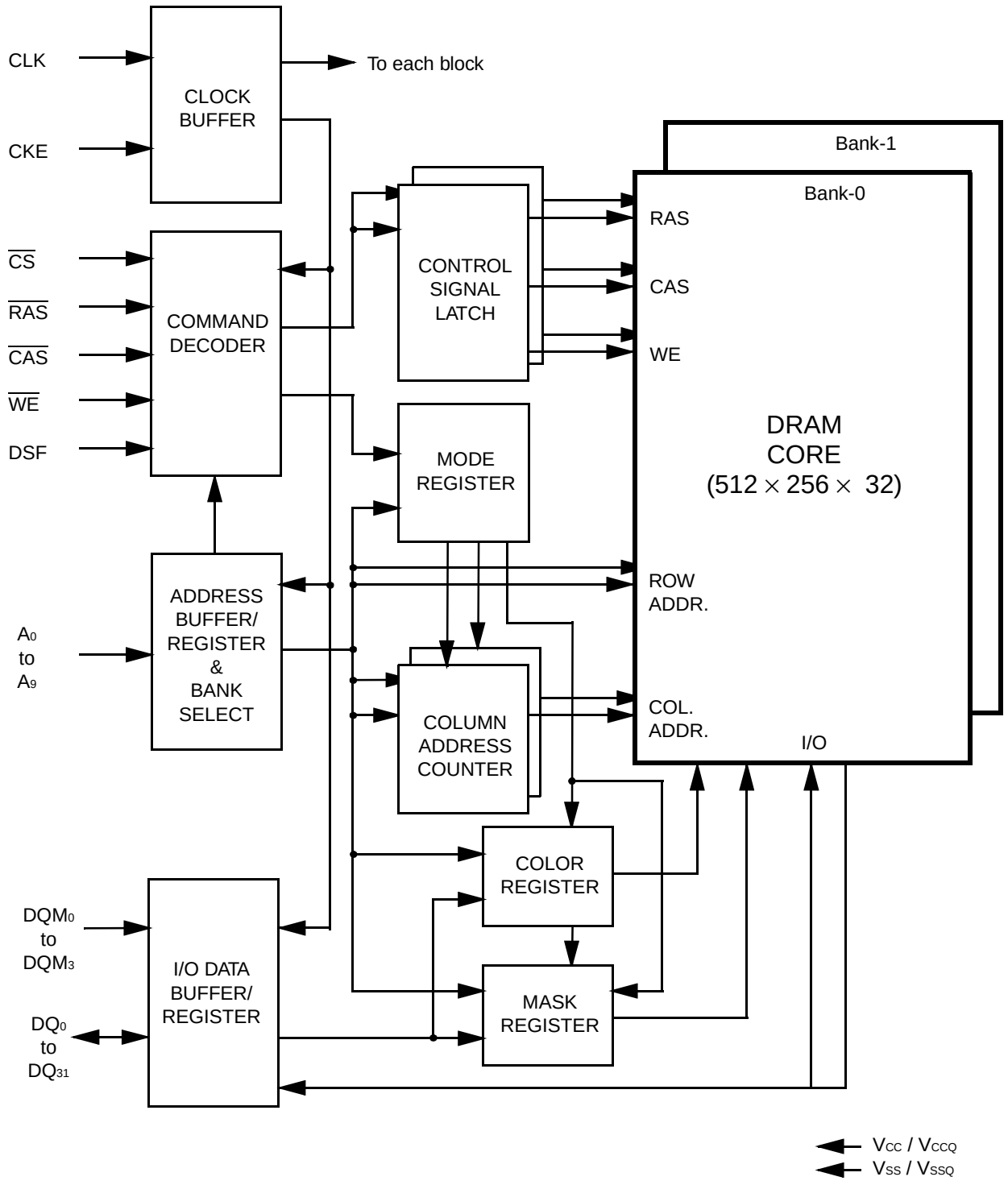
– 100-pin plastic QFP, order as MB81G83222-×××PQ

■ PIN ASSIGNMENTS AND DESCRIPTIONS



Symbol	Description
V_{CC}, V_{CCQ}	Supply Voltage
DQ_0 to DQ_{31}	Data I/O
V_{SS}, V_{SSQ}	Ground
DQM_0 to DQM_3	Input/Output Mask
$\overline{WE}$	Write Enable
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select
DSF	Special Function Enable
A_9 (BA)	Bank Select
AP	Auto Precharge Enable
A_0 to A_7, A_8	Address Input • Row :A_0 to A_8 • Column :A_0 to A_7 (A_8=AP)
NC	No Connection
CKE	Clock Enable
CLK	Clock Input

Fig. 1 - MB81G83222 BLOCK DIAGRAM



■ FUNCTION TRUTH TABLE

COMMAND TRUTH TABLE

Function	Notes	Symbol	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	A_9	A_8	A_7-A_0
			n-1	n								
Device Deselect	5	DESL	H	X	H	X	X	X	X	X	X	X
No Operation	5	NOP	H	X	L	H	H	H	X	X	X	X
Burst Stop	6	BST	H	X	L	H	H	L	L	X	X	X
Read	7	READ	H	X	L	H	L	H	L	V	L	V
Read With Auto-precharge	7	READA	H	X	L	H	L	H	L	V	H	V
Write	7	WRIT	H	X	L	H	L	L	L	V	L	V
Write With Auto-precharge	7	WRITA	H	X	L	H	L	L	L	V	H	V
Block Write	7	BWRIT	H	X	L	H	L	L	H	V	L	V
Block Write with Auto-precharge	7	BWRITA	H	X	L	H	L	L	H	V	H	V
Bank Active (RAS) & WPB Disable	7	ACTV	H	X	L	L	H	H	L	V	V	V
Bank Active (RAS) & WPB Enable	8	ACTVM	H	X	L	L	H	H	H	V	V	V
Precharge Single Bank		PRE	H	X	L	L	H	L	L	V	L	X
Precharge All Banks		PALL	H	X	L	L	H	L	L	X	H	X
Mode Register Set	9, 10	MRS	H	X	L	L	L	L	L	V	L	V
Special Mode Register Set		SMRS	H	X	L	L	L	L	H	L	L	V

Notes:1. V = Valid, L = Logic Low, H = Logic High, X = either L or H.
2. All commands assumes no CSUS command on previous rising edge of clock.
3. All commands are assumed to be valid state transitions.
4. All inputs are latched on the rising edge of clock.
5. NOP and DESL commands have the same effect on the part.
6. BST command is effective only during full column burst read or write.
7. READ, READA, WRIT, WRITA, BWRIT, and BWRITA commands should only be issued after the corresponding bank has been activated (ACTV or ACTVM command). Refer to STATE DIAGRAM.
8. ACTV and ACTVM commands should only be issued after corresponding bank has been precharged (PRE or PALL command).
9. Required after power up.
10. MRS command should only be issued after all banks have been precharged (PRE or PALL command). Refer to STATE DIAGRAM.

■ FUNCTIONAL TRUTH TABLE (Continued)

DQM TRUTH TABLE

Function	Symbol	CKE		DQMi
		n-1	n	
i-th Byte Write Enable / Output Enable	ENBi	H	X	L
i-th Byte Data Mask / Output Disable	MASKi	H	X	H

Notes:1. i=0, 1, 2, 3.
2. DQM_0 for DQ_0 to $_7$, DQM_1 for DQ_8 to $_{15}$, DQM_2 for DQ_{16} to $_{23}$, DQM_3 for DQ_{24} to $_{31}$.

CKE TRUTH TABLE

Current State	Function	Notes	Symbol	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	A_9 (BA)	A_8 (AP)	A_{7-0}
				n-1	n								
Bank Active	Clock Suspend Mode Entry	1	CSUS	H	L	X	X	X	X	X	X	X	X
Any	Clock Suspend continue	1	—	L	L	X	X	X	X	X	X	X	X
Clock Suspend	Clock Suspend Mode Exit		—	L	H	X	X	X	X	X	X	X	X
Idle	Auto-refresh Command	2	REF	H	H	L	L	L	H	L	X	X	X
Idle	Self-refresh Entry	2	SELF	H	L	L	L	L	H	L	X	X	X
Self Refresh	Self-refresh Exit		SELF X	L	H	L	H	H	H	X	X	X	X
				L	H	H	X	X	X	X	X	X	X
Idle	Power Down Entry		PD	H	L	L	H	H	H	X	X	X	X
				H	L	H	X	X	X	X	X	X	X
Prechatge	Power Down Entry		PD	H	L	L	H	H	H	X	X	X	X
				H	L	H	X	X	X	X	X	X	X
Back Active	Power Down Entry	3	PD	H	L	L	L	H	L	L	V	L	X
				H	L	L	L	H	L	L	X	H	X
Power Down	Power Down Exit		—	L	H	L	H	H	H	X	X	X	X
				L	H	H	X	X	X	X	X	X	X

Notes:1. The CSUS command requires that at least one bank is active. Refer to STATE DIAGRAM.
2. REF and SELF commands should only be issued after all banks have been precharged (PRE or PALL command). Refer to STATE DIAGRAM.
3. PD command should be issud after all banks have been precharged (PRE or PALL command). If a bank or all banks are in active state, PD command can be issued in conjuction with PRE or PALL command whichever precharge command makes all banks in idle state.

■ FUNCTIONAL TRUTH TABLE (Continued)

OPERATION COMMAND TABLE (Aplicable to single bank)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	Addr	Command	Function	Notes
Idle	H	X	X	X	X	X	DESL	NOP	
	L	H	H	H	X	X	NOP	NOP	
	L	H	H	L	L	X	BST	NOP	
	L	H	L	H	L	BA, CA, AP	READ/READA	Illegal	
	L	H	L	L	L	BA, CA, AP	WRIT/WRITA	Illegal	
	L	L	H	H	L	BA, RA	ACTV	Bank Active after t_{RCD}	
	L	L	H	L	L	BA, AP	PRE/PALL	NOP	
	L	L	L	H	L	X	REF/SELF	Auto-refresh or Self-refresh	3
	L	L	L	L	L	MODE	MRS	Mode Register Set (Idle after t_{RSC})	3
	L	L	H	H	H	BA, RA	ACTVM	Bank Active & Write Per Bit Enable	
	L	H	L	L	H	BA, CA, AP	BWRIT/ BWRITA	Illegal	
	L	L	L	L	H	SPECIAL MODE	SMRS	Special Mode Register Set (Idle after t_{RSC})	
Bank Active	H	X	X	X	X	X	DESL	NOP	
	L	H	H	H	X	X	NOP	NOP	
	L	H	L	H	L	BA, CA, AP	READ/READA	Begin Read ; Determine AP	
	L	H	H	L	L	X	BST	NOP	
	L	H	L	L	L	BA, CA, AP	WRIT/WRITA	Begin Write ; Determine AP	
	L	L	H	H	L	BA, RA	ACTV	Illegal	2
	L	L	H	L	L	BA, AP	PRE/PALL	Precharge ; Determine Precharge Type	
	L	L	L	H	L	X	REF/SELF	Illegal	
	L	L	L	L	L	MODE	MRS	Illegal	
	L	L	H	H	H	BA, RA	ACTVM	Illegal	
	L	H	L	L	H	BA, CA, AP	BWRIT/ BWRITA	Block Write ; Determine AP	
	L	L	L	L	H	SPECIAL MODE	SMRS	Special Mode Register Set	

■ FUNCTIONAL TRUTH TABLE (Continued)

OPERATION COMMAND TABLE (Continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	Addr	Command	Function	Notes
Read	H	X	X	X	X	X	DESL	NOP (Continue Burst to End → Bank Active)	
	L	H	H	H	X	X	NOP	NOP (Continue Burst to End → Bank Active)	
	L	H	H	L	L	X	BST	Burst Stop →Bank Active (BL=Full Column) NOP (BL=1, 2, 4, 8)	
	L	H	L	H	L	BA, CA, AP	READ/READA	Terminate Burst, New Read ; Determine AP	
	L	H	L	L	L	BA, CA, AP	WRIT/WRITA	Terminate Burst, Start Write ; Determine AP	4
	L	L	H	H	L	BA, RA	ACTV	Illegal	2
	L	L	H	L	L	BA, AP	PRE/PALL	Terminate Burst, Precharge ; Determine Precharge Type	
	L	L	L	H	L	X	REF/SELF	Illegal	
	L	L	L	L	X	MODE/ SPECIAL MODE	MRS/ SMRS	Illegal	
	L	L	H	H	H	BA, RA	ACTVM	Illegal	2
	L	H	L	L	H	BA, CA, AP	BWRIT/ BWRITA	Terminate Burst, Start Block Write ; Determine AP	
Write	H	X	X	X	X	X	DESL	NOP (Continue Burst to End → Write Recovering)	
	L	H	H	H	X	X	NOP	NOP (Continue Burst to End → Write Recovering)	
	L	H	H	L	L	X	BST	Burst Stop → Write Recovering → Bank Active (BL=Full Column) NOP (BL=1, 2, 4, 8)	
	L	H	L	H	L	BA, CA, AP	READ/READA	Terminate Burst, Start Read ; Determine AP	
	L	H	L	L	L	BA, CA, AP	WRIT/WRITA	Terminate Burst, New Write ; Determine AP	4
	L	L	H	H	L	BA, RA	ACTV	Illegal	2
	L	L	H	L	L	BA, AP	PRE/PALL	Terminate Burst, Precharge ; Determine Precharge Type	4
	L	L	L	H	L	X	REF/SELF	Illegal	
	L	L	L	L	X	MODE/ SPECIAL MODE	MRS/ SMRS	Illegal	
	L	L	H	H	H	BA, RA	ACTVM	Illegal	2
	L	H	L	L	H	BA, CA, AP	BWRIT/ BWRITA	Terminate Burst, Start Block Write ; Determine AP	

■ FUNCTIONAL TRUTH TABLE (Continued)

OPERATION COMMAND TABLE (Continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	Addr	Command	Function	Notes
Block Write	H	X	X	X	X	X	DESL	NOP (Continue Burst to End → Write Recovering)	
	L	H	H	H	X	X	NOP	NOP (Continue Burst to End → Write Recovering)	
	L	H	H	L	L	X	BST	Illegal	
	L	H	L	H	L	BA, CA, AP	READ/READA	Illegal	
	L	H	L	L	L	BA, CA, AP	WRIT/WRITA	Illegal	
	L	L	H	H	L	BA, RA	ACTV	Illegal	
	L	L	H	L	L	BA, AP	PRE/PALL	Illegal	
	L	L	L	H	L	X	REF/SELF	Illegal	
	L	L	L	L	X	MODE/ SPECIAL MODE	MRS/ SMRS	Illegal	
	L	L	H	H	H	BA, RA	ACTVM	Illegal	
	L	H	L	L	H	BA, CA, AP	BWRIT/ BWRITA	Illegal	
Read With Auto Precharge	H	X	X	X	X	X	DESL	NOP (Continue Burst to End → Precharge)	
	L	H	H	H	X	X	NOP	NOP (Continue Burst to End → Precharge)	
	L	H	H	L	L	X	BST	Illegal	
	L	H	L	H	L	BA, CA, AP	READ/READA	Illegal	2
	L	H	L	L	L	BA, CA, AP	WRIT/WRITA	Illegal	2
	L	L	H	H	L	BA, RA	ACTV	Other Bank Active, Illegal on same Bank	2
	L	L	H	L	L	BA, AP	PRE/PALL	Illegal	2
	L	L	L	H	L	X	REF/SELF	Illegal	
	L	L	L	L	X	MODE/ SPECIAL MODE	MRS/ SMRS	Illegal	
	L	L	H	H	H	BA, RA	ACTVM	Illegal	
	L	H	L	L	H	BA, CA, AP	BWRIT/ BWRITA	Illegal	

■ FUNCTIONAL TRUTH TABLE (Continued)

OPERATION COMMAND TABLE (Continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	Addr	Command	Function	Notes
Write With Auto Precharge /Block Write With Auto Precharge	H	X	X	X	X	X	DESL	NOP (Continue Burst to End → Write Recovering with Precharge)	
	L	H	H	H	X	X	NOP	NOP (Continue Burst to End → Write Recovering with Precharge)	
	L	H	H	L	L	X	BST	Illegal	
	L	H	L	H	L	BA, CA, AP	READ/READA	Other Bank Read, Illegal on same Bank	2
	L	H	L	L	L	BA, CA, AP	WRIT/WRITA	Other Bank Write, Illegal on same Bank	2
	L	L	H	H	L	BA, RA	ACTV	Illegal	2
	L	L	H	L	L	BA, AP	PRE/PALL	Illegal	2
	L	L	L	H	L	X	REF/SELF	Illegal	
	L	L	L	L	X	MODE/ SPECIAL MODE	MRS/ SMRS	Illegal	
	L	L	H	H	H	BA, RA	ACTVM	Illegal	2
	L	H	L	L	H	BA, CA, AP	BWRIT/ BWRITA	Illegal	
Precharge	H	X	X	X	X	X	DESL	NOP (Idle after t_{RP})	
	L	H	H	H	X	X	NOP	NOP (Idle after t_{RP})	
	L	H	H	L	L	X	BST	Illegal	
	L	H	L	H	L	BA, CA, AP	READ/READA	Illegal	2
	L	H	L	L	L	BA, CA, AP	WRIT/WRITA	Illegal	2
	L	L	H	H	L	BA, RA	ACTV	Illegal	2
	L	L	H	L	L	BA, AP	PRE/PALL	NOP (PALL may affect other bank)	5
	L	L	L	H	L	X	REF/SELF	Illegal	
	L	L	L	L	X	MODE/ SPECIAL MODE	MRS/ SMRS	Illegal	
	L	L	H	H	H	BA, RA	ACTVM	Illegal	2
	L	H	L	L	H	BA, CA, AP	BWRIT/ BWRITA	Illegal	

■ FUNCTIONAL TRUTH TABLE (Continued)

OPERATION COMMAND TABLE (Continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	Addr	Command	Function	Notes
Bank Activating	H	X	X	X	X	X	DESL	NOP (Bank Active after t_{RCD})	
	L	H	H	H	X	X	NOP	NOP (Bank Active after t_{RCD})	
	L	H	H	L	L	X	BST	NOP (Bank Active after t_{RCD})	
	L	H	L	H	L	BA, CA, AP	READ/READA	Illegal	2
	L	H	L	L	L	BA, CA, AP	WRIT/WRITA	Illegal	2
	L	L	H	H	L	BA, RA	ACTV	Illegal	6
	L	L	H	L	L	BA, AP	PRE/PALL	Illegal	2
	L	L	L	H	L	X	REF/SELF	Illegal	
	L	L	L	L	L	MODE	MRS	Illegal	
	L	L	H	H	H	BA, RA	ACTVM	Illegal	
	L	H	L	L	H	BA, CA, AP	BWRIT/ BWRITA	Illegal	
	L	L	L	L	H	SPECIAL MODE	SMRS	Special Mode Registar Set	
Write Recovering /Block Write Recovering	H	X	X	X	X	X	DESL	NOP (Bank Active after t_{WR}/t_{BWC})	
	L	H	H	H	X	X	NOP	NOP (Bank Active after t_{WR}/t_{BWC})	
	L	H	H	L	L	X	BST	NOP (Bank Active after t_{WR}/t_{BWC})	
	L	H	L	H	L	BA, CA, AP	READ/READA	Start Read ; Determine AP	4
	L	H	L	L	L	BA, CA, AP	WRIT/WRITA	New Write ; Determine AP	
	L	L	H	H	L	BA, RA	ACTV	Illegal	2
	L	L	H	L	L	BA, AP	PRE/PALL	Illegal	2
	L	L	L	H	L	X	REF/SELF	Illegal	
	L	L	L	L	X	MODE/ SPECIAL MODE	MRS/ SMRS	Illegal	
	L	L	H	H	H	BA, RA	ACTVM	Illegal	
	L	H	L	L	H	BA, CA, AP	BWRIT/ BWRITA	New Block Write ; Determine AP	

■ FUNCTIONAL TRUTH TABLE (Continued)

OPERATION COMMAND TABLE (Continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	Addr	Command	Function	Notes
Write Recovering with Auto-precharge /Block Write Recovering with Auto-precharge	H	X	X	X	X	X	DESL	NOP (Precharge after t_{RWL}/t_{BWL})	
	L	H	H	H	X	X	NOP	NOP (Precharge after t_{RWL}/t_{BWL})	
	L	H	H	L	L	X	BST	Illegal	
	L	H	L	H	L	BA, CA, AP	READ/READA	Illegal	2
	L	H	L	L	L	BA, CA, AP	WRIT/WRITA	Illegal	2
	L	L	H	H	L	BA, RA	ACTV	Illegal	2
	L	L	H	L	L	BA, AP	PRE/PALL	Illegal	2
	L	L	L	H	L	X	REF/SELF	Illegal	
	L	L	L	L	X	MODE/ SPECIAL MODE	MRS/ SMRS	Illegal	
	L	L	H	H	H	BA, RA	ACTVM	Illegal	2
	L	H	L	L	H	BA, CA, AP	BWRIT/ BWRITA	Illegal	
Refreshing	H	X	X	X	X	X	DESL	NOP (Idle after t_{RC})	
	L	H	H	X	X	X	NOP/BST	NOP (Idle after t_{RC})	
	L	H	L	X	X	X	READ/READA/ WRIT/WRITA/ BWRIT/ BWRITA	Illegal	
	L	L	H	X	X	X	ACTV/ACTVM/ PRE/PALL	Illegal	
	L	L	L	X	X	X	REF/SELF/ MRS/SMRS	Illegal	6
Mode Register Setting	H	X	X	X	X	X	DESL	NOP (Idle after t_{RSC})	
	L	H	H	H	X	X	NOP	NOP (Idle after t_{RSC})	
	L	H	H	L	L	X	BST	Illegal	
	L	H	L	X	X	X	READ/READA/ WRIT/WRITA/ BWRIT/ BWRITA	Illegal	
	L	L	X	X	X	X	ACTV/ACTVM/ PRE/PALL REF/SELF/ MRS/SMRS	Illegal	

■ FUNCTIONAL TRUTH TABLE (Continued)

OPERATION COMMAND TABLE (Continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	Addr	Command	Function	Notes
Special Mode Register Setting	H	X	X	X	X	X	DESL	NOP (Return to original state after t_{RSC})	
	L	H	H	H	X	X	NOP	NOP (Return to original state after t_{RSC})	
	L	H	H	L	L	X	BST	Illegal	
	L	H	L	X	X	X	READ/READA/ WRIT/WRITA/ BWRIT/ BWRITA	Illegal	
	L	L	X	X	X	X	ACTV/ACTVM/ PRE/PALL REF/SELF/ MRS/SMRS	Illegal	

ABBREVIATIONS : RA=Row Adress BA=Bank Address
CA=Column Address AP=Auto Precharge

■ FUNCTIONAL TRUTH TABLE (Continued)

COMMAND TRUTH TABLE FOR CKE

Current State	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	Addr	Function	Notes
Self-refresh	H	X	X	X	X	X	X	X	Invalid	
	L	H	H	X	X	X	X	X	Exit Self-refresh, Idle after t_{RC}	
	L	H	L	H	H	H	X	X	Exit Self-refresh, Idle after t_{RC}	
	L	H	L	H	L	X	X	X	Illegal	
	L	H	L	L	X	X	X	X	Illegal	
	L	L	X	X	X	X	X	X	NOP (Maintain Self-refresh)	
Self-refresh Recovery	H	H	H	X	X	X	X	X	Idel after t_{RC}	
	H	H	L	H	H	X	X	X	Idel after t_{RC}	
	H	H	L	H	L	X	X	X	Illegal	
	H	H	L	L	X	X	X	X	Illegal	
	H	L	H	X	X	X	X	X	Begin Clock Suspend Next Cycle	
	H	L	L	H	H	X	X	X	Begin Clock Suspend Next Cycle	
	H	L	L	H	L	X	X	X	Illegal	
	H	L	L	L	X	X	X	X	Illegal	
	L	H	X	X	X	X	X	X	Exit Clock Suspend Next Cycle	
	L	L	X	X	X	X	X	X	Maintain Clock Suspend	
Power Down	H	X	X	X	X	X	X	—	Invalid	
	L	H	X	X	X	X	X	X	Exit Power Down Mode → Idle	
	L	L	X	X	X	X	X	X	NOP (Maintain Power Down Mode)	
Both Banks Idle	H	H	H	X	X	X	X	—	Refer to the Operation Command Table.	
	H	H	L	H	X	X	X	—	Refer to the Operation Command Table.	
	H	H	L	L	H	X	X	—	Refer to the Operation Command Table.	
	H	H	L	L	L	H	L	X	Auto-refresh	
	H	H	L	L	L	L	H	SPECIAL MODE	Refer to the Operation Command Table.	
	H	H	L	L	L	L	L	MODE	Refer to the Operation Command Table.	
	H	L	H	X	X	X	X	—	Refer to the Operation Command Table.	
	H	L	L	H	X	X	X	—	Refer to the Operation Command Table.	
	H	L	L	L	H	X	X	—	Refer to the Operation Command Table.	
	H	L	L	L	L	H	L	X	Self-refresh	

■ FUNCTIONAL TRUTH TABLE (Continued)

COMMAND TRUTH TABLE FOR CKE (Continued)

Current State	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	Addr	Function	Notes
Both Banks Idle	H	L	L	L	L	L	L	SPECIAL MODE	Refer to the Operation Command Table.	
	H	L	L	L	L	L	L	MODE	Refer to the Operation Command Table.	
	L	X	X	X	X	X	X	X	Power Down	
Any State Other Than Listed Above	H	H	X	X	X	X	X	X	Refer to the Operation Command Table.	
	H	L	X	X	X	X	X	X	Begin Clock Suspend Next Cycle	
	L	H	X	X	X	X	X	X	Exit Clock Suspend Next Cycle	
	L	L	X	X	X	X	X	X	Maintain Clock Suspend	

Notes:1. All entries assume the CKE was High during the proceeding clock cycle and the current clock cycle.
2. Illegal to bank in specified state; entry may be legal in the bank specified by BA, depending on the state of that bank.
3. Illegal if any bank is not idle.
4. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
5. NOP to bank precharging or in idle state.
   May precharge bank spesified by BA (and AP).
6. t_{RRD} must be satisfied for other bank.

■ FUNCTIONAL TRUTH TABLE (Continued)

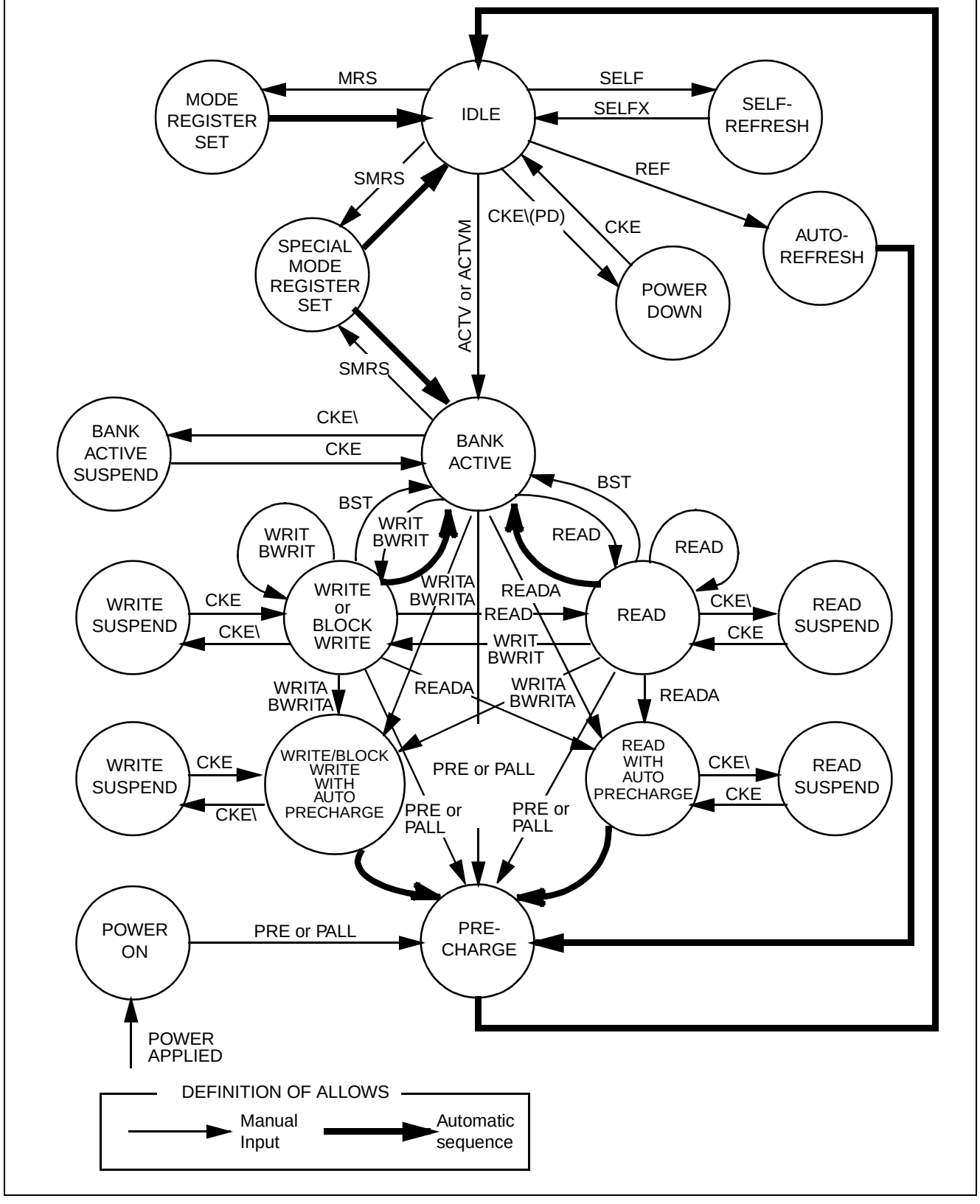
Table 1. : Minimum Clock Latency Or Delay Time for 2 Bank Operation

First command \ Second command (opposite bank)	MRS	SMRS	ACTV (M)	READ	READA	WRIT	WRITA	BWRIT	BWRITA	BST *6	PRE	PALL	REF	SELF
MRS	t_{RSC}	t_{RSC}	t_{RSC}										t_{RSC}	t_{RSC}
SMRS	t_{RSC}	t_{RSC}	t_{RSC}	t_{RSC}	t_{RSC}	t_{RSC}	t_{RSC}	t_{RSC}	t_{RSC}		t_{RSC}	t_{RSC}	t_{RSC}	t_{RSC}
ACTV (M)		1	t_{RRD}	1	1	1	1	1	1	1	1	t_{RAS}		
READ		BL-1 + t_{RSC} *1	1	1	1	1 *1	1 *1	1 *1	1 *1	1	1	1		
READA	BL + t_{RP} *2	BL-1 + t_{RSC} *1	1	BL	BL	BL *1	BL *1	BL *1	BL *1		1	BL	BL + t_{RP} *2	BL + t_{RP} *2
WRIT		BL-1 + t_{RSC} *1	1	1	1	1	1	1	1	1	1	t_{RWL}		
WRITA	BL-1 t_{RWL} t_{RP}	BL-1 + t_{RSC}	1	BL	BL	BL	BL	BL	BL		1	BL-1 t_{RWL} + t_{RP}	BL-1 t_{RWL} + t_{RP}	BL-1 t_{RWL} + t_{RP}
BWRIT		t_{BWC}	1	t_{BWC}	t_{BWC}	t_{BWC}	t_{BWC}	t_{BWC}	t_{BWC}	N/A	1	t_{BWL}		
BWRITA	t_{BWL} + t_{RP}	t_{BWC}	1	t_{BWC}	t_{BWC}	t_{BWC}	t_{BWC}	t_{BWC}	t_{BWC}	N/A	1	t_{BWL}	t_{BWL} + t_{RP}	t_{BWL} + t_{RP}
BST *6		1	1	1		1	1 *7	1	1	N/A	1	1		
PRE	t_{RP} *3	t_{RP} *1	1	1	1	1	1	1	1 *7	1	1	1	t_{RP} *3	t_{RP} *3
PALL *4	t_{RP} *3	t_{RP} *1	t_{RP}								N/A*5	N/A*5	t_{RP} *3	t_{RP} *3
REF	t_{RC}	t_{RC}	t_{RP}										t_{RRD}	t_{RC}
SELF	t_{PDE} + t_{RC}	t_{PDE} + t_{RC}	t_{PDE} + t_{RC}										t_{PDE} + t_{RC}	t_{PDE} + t_{RC}

Notes: 1. Assume no I/O conflict.
2. If $t_{RP} <= t_{CK}$, minimum latency is a sum of BL + CL.
3. Assume output is in High-Z state.
4. Assume PALL command dose not affect any operation on opposite bank.
5. Not applicable after t_{RP}.
6. BST command should be issued only at BL=Full column.
7. BST command should be issued at BL=Full column and single write mode operation.

Illegal Command

Fig. 2 - STATE DIAGRAM (One Bank Operation)



■ FUNCTIONAL DESCRIPTION

SDRAM BASIC FUNCTION

Five major differences between this SGRAM and conventional DRAMs are: synchronized operation, burst mode, mode register, write per bit, and block write.

The **synchronized operation** is the fundamental difference. An SGRAM uses a clock input for the synchronization, where the DRAM is basically asynchronous memory even if it has been using two clocks, $\overline{RAS}$ and $\overline{CAS}$. Each operation of DRAM is determined by their timing phase difference while each operation of SGRAM is determined by commands and all operations are referenced by a positive clock edge. Fig. 4 in page 23 show the basic timing diagram difference.

The **burst mode** is a very high speed access mode utilizing an internal column address generator. Once a column addresses for the first access is set, following addresses are automatically generated by the internal column address counter.

The **mode register** is to justify the SGRAM operation and function into desired system conditions. Referenced in MODE REGISTER TABLE, if a system requires interleave for burst type and two clocks for CAS latency, SDRAM can be configured to those conditions by mode register programming.

The **write per bit** function is to enable selective write operation for each 32 bit I/O. This function is activated by ACTVM command for each bank.

The **block write** function enables writing the same data (logic 0 or 1) into all of the memory cells for eight successive column (8×32 bit) within a selected Row.

CLOCK (CLK) and CLOCK ENABLE (CKE)

All input and output signals of SGRAM use register type buffers. A CLK is used as a trigger for the register and internal burst counter increment. All inputs are latched by a positive edge of CLK. All outputs are validated by the CLK. CKE is a high active clock enable signal. When CKE = Low is latched at a clock input during active cycle, the next clock will be internally masked. During idle state (all banks have been precharged), CKE = Low enters the Power Down mode(standby) and this will make extremely low standby current.

CHIP SELECT ($\overline{CS}$)

$\overline{CS}$ enables all commands inputs, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DSF and address input. When $\overline{CS}$ is high level, command signals are negated but internal operation such as burst cycle will not be suspended. In the small system $\overline{CS}$ can be tied to ground level.

COMMAND INPUT ($\overline{RAS}$, $\overline{CAS}$ $\overline{WE}$, and DSF)

Unlike a conventional DRAM, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, and DSF do not directly imply SGRAM operation, such as Row address strobe by $\overline{RAS}$. Instead, each combination of $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, and DSF input in conjunction with $\overline{CS}$ input at a rising edge of the CLK determines SGRAM operation. Refer to FUNCTION TRUTH TABLE in page 5.

ADDRESS INPUT (A_0 to A_8)

Address input selects an arbitrary location of a total of 131,072 words of each memory cell matrix. A total seventeen of address input signals are required to decode such a matrix with nine Row and eight Column address format. SDRAM adopts an address multiplexer in order to reduce the pin count of the address line. At a Bank Active command (ACTV or ACTVM), nine Row addresses are initially latched and the remainder of eight Column addresses are then latched by a Column address strobe command of either a Read command (READ or READA) or Write command (WRIT, WRITA, BWRIT, or BWRITA).
The A_8/AP pin determines precharge option. Refer to PRECHARGE AND PRECHARGE OPTION in page 21.

BANK SELECT (A_9)

This SGRAM has two banks and each bank is organized as 128K-words by 32-bit.
Bank selection by A_9 occurs at Bank Active command (ACTV or ACTVM) followed by read (READ or READA), write (WRIT, WRITA, BWRIT, or BWRITA), and precharge command (PRE).

■ FUNCTIONAL DESCRIPTION (Continued)

DATA INPUT AND OUTPUT (DQ_0 to DQ_{31})

Input data is latched and written into memory at the clock followed by a write command input. Data output is obtained by the following conditions followed by a read command input:

t_{RAC} **;** from the bank active command when t_{RCD} (min.) is satisfied. (This parameter is reference only.)
t_{CAC} ; from the read command when t_{RCD} is greater than t_{RCD} (min.).
t_{AC} ; from the clock edge after t_{RAC} and t_{CAC}.

The polarity of the output data is identical to that of the input. Valid data time is between access time (determined by the three conditions above) and the next positive clock edge (t_{OH}).

DATA I/O MASK (DQM0 to DQM3)

DQM_0 to DQM_3 are an active high enable input and have an output disable and input mask function. During burst cycle and when $DQM_{0–3}$ = High is latched by a clock, input is masked at the same clock (Write&Block Write Operation) and output will be masked at the second clock later (Read operation) while internal burst counter will increment by one or will go to the next stage depending on burst type.
DQM_0, DQM_1, DQM_2, and DQM_3 controls DQ_0 to DQ_7, DQ_8 to DQ_{15}, DQ_{16} to DQ_{23}, and DQ_{24} to DQ_{31}, respectively.

BURST MODE OPERATION AND BURST TYPE

The burst mode provides faster memory access. The burst mode is implemented by keeping the same Row address and by automatic strobing column address. Access time and cycle time of Burst mode is specified as t_{AC} and t_{CK}, respectively. The internal column address counter operation is determined by a mode register which defines burst type and burst count length from 1 bits to full column of boundary. In order to terminate or to move from the current burst mode to the next stage while the remaining burst count is more than 1, the following combinations will be required:

Current Stage	Next Stage	Method (Assert the Following Command)	
Burst Read	Burst Read	Read command	
Burst Read	Burst Write	1st Step	Mask command (Normally 3 Clock Cycles)
		2nd Step	Write command after l_{OWD}
Burst Write	Burst Write	Write command	
Burst Write	Burst Read	Read command	
Burst Read	Precharge	Precharge command	
Burst Write	Precharge	1st Step	Mask command
		2nd Step	Precharge command after t_{RWL}

■ FUNCTIONAL DESCRIPTION (Continued)

BURST MODE OPERATION AND BURST TYPE (continued)

When the full burst operation is executed at single write mode, auto-precharge command is valid only at write operation. The burst type can be selected either sequential or interleave mode. But only the sequential mode is usable to the full column burst. The sequential mode is an incremental decoding scheme within a boundary address to be determined by burst length, it assigns +1 to the previous (or initial) address until reaching the end of boundary address and then wraps round to least significant address(=0).

Burst Length	Starting Column Address A_2 A_1 A_0	Sequential Mode	Interleave
2	X X 0	0 – 1	0 – 1
	X X 1	1 – 0	1 – 0
4	X 0 0	0 – 1 – 2 – 3	0 – 1 – 2 – 3
	X 0 1	1 – 2 – 3 – 0	1 – 0 – 3 – 2
	X 1 0	2 – 3 – 0 – 1	2 – 3 – 0 – 1
	X 1 1	3 – 0 – 1 – 2	3 – 2 – 1 – 0
8	0 0 0	0 – 1 – 2 – 3 – 4 – 5 – 6 – 7	0 – 1 – 2 – 3 – 4 – 5 – 6 – 7
	0 0 1	1 – 2 – 3 – 4 – 5 – 6 – 7 – 0	1 – 0 – 3 – 2 – 5 – 4 – 7 – 6
	0 1 0	2 – 3 – 4 – 5 – 6 – 7 – 0 – 1	2 – 3 – 0 – 1 – 6 – 7 – 4 – 5
	0 1 1	3 – 4 – 5 – 6 – 7 – 0 – 1 – 2	3 – 2 – 1 – 0 – 7 – 6 – 5 – 4
	1 0 0	4 – 5 – 6 – 7 – 0 – 1 – 2 – 3	4 – 5 – 6 – 7 – 0 – 1 – 2 – 3
	1 0 1	5 – 6 – 7 – 0 – 1 – 2 – 3 – 4	5 – 4 – 7 – 6 – 1 – 0 – 3 – 2
	1 1 0	6 – 7 – 0 – 1 – 2 – 3 – 4 – 5	6 – 7 – 4 – 5 – 2 – 3 – 0 – 1
	1 1 1	7 – 0 – 1 – 2 – 3 – 4 – 5 – 6	7 – 6 – 5 – 4 – 3 – 2 – 1 – 0

FULL COLUMN BURST AND BURST STOP COMMAND (BST)

The full column burst is an option of burst length and available only at sequential mode of burst type. This full column burst mode is repeatedly access to the same column. If burst mode reaches end of column address, then it wraps round to first column address (=0) and continues to count until interrupted by the news read (READ) /write (WRIT/ BWRIT) , precharge (PRE) , or burst stop (BST) command. The selection of auto-precharge option is illegal during the full column burst operation except write command at BURST READ & SINGLE WRITE mode.

The BST command is applicable to terminated the full column burst operation and illegal during the burst operation with length of 1, 2, 4, and 8. If the BST command is asserted during the full column burst mode, its operation is terminated immediately and the internal state moves to Bank Active.

When read mode is interrupted by BST command, the output will be in High-Z.
For the detail rule, please refer to Timing Diagram-8.
When write mode is interrupted by BST command, the data to be applied at the same time with BST command will be ignored.

BURST READ & SINGLE WRITE

The burst read and single write mode provides single word write operation regardless of its burst length. In this mode, burst read operation does not be affected by this mode.

■ FUNCTIONAL DESCRIPTION (Continued)

PRECHARGE AND PRECHARGE OPTION (PRE, PALL)

SGRAM memory is the same as DRAM, requiring precharge and refresh operations. Precharge rewrites the bit line and to reset the internal Row address line and is executed by Precharge command (PRE). With the precharge command, SGRAM will automatically be in idle state after precharge time (t_{RP}).
The precharged bank is selected by combination of A_8 and A_9 when Precharge command is asserted.
If A_8 = High, both banks are precharged regardless of A_9 (PALL). If A_8 = Low, a bank to be selected by A_9 is precharged (PRE). The Auto Precharge enters precharge mode at the end of burst mode of read or write without Precharge command assertion. This Auto Precharge is entered by A_8=High when a read or write command is asserted. Refer to FUNCTION TRUTH TABLE.

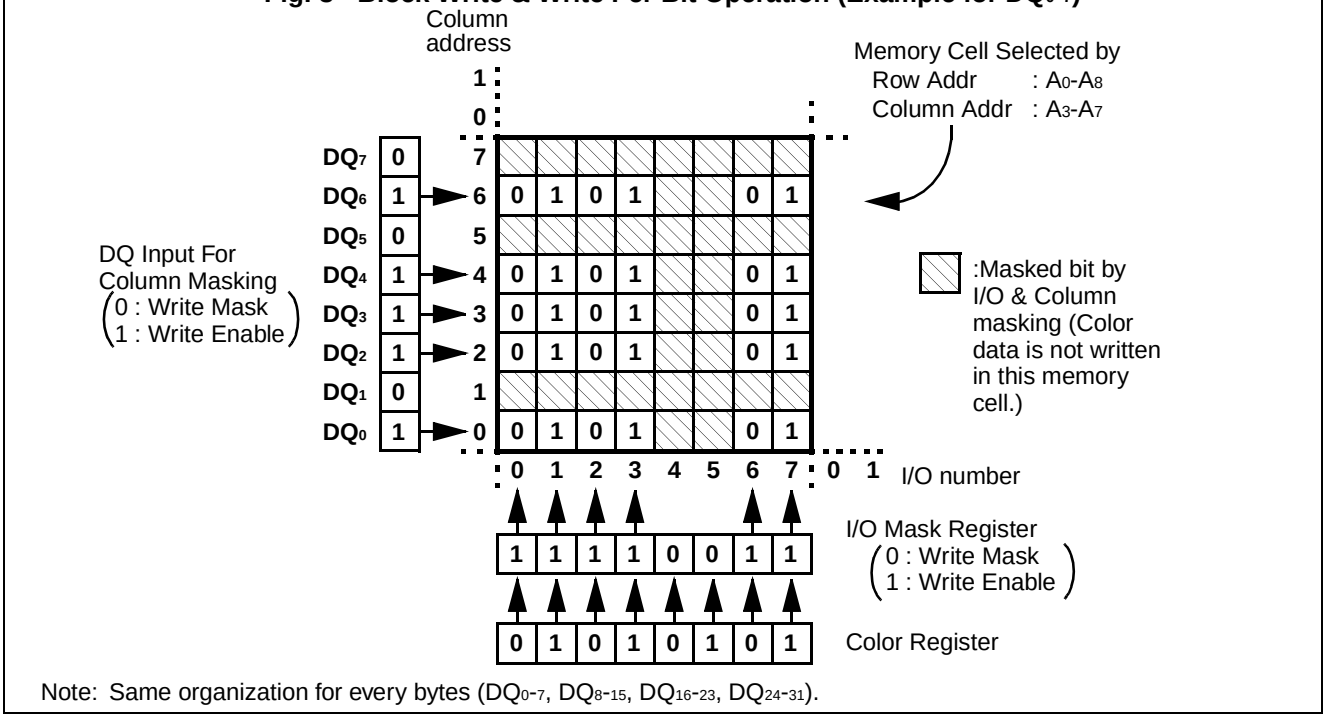
WRITE PER BIT OPERATION (ACTVM)

The write per bit (WPB) is a function to enable selective write operation for each DQ pin. Bank active & WPB enable command (ACTVM) enables WPB operation for the associated bank and ACTV command disables it. Selection of masking I/O should be stored in load mask register (DQi=High : write enable, DQi=Low : write mask) by SMRS command with AS=High. For example, if a mask register bit=Low, the associated data bit is masked when a write command is excused and WPB has been enabled for the bank being written. WPB is applicable to either burst writes, single writes, and block writes. DQM masking is applicable for WPB as well as non-write-per-bit. ACTVM is valid until the associated bank is precharged.

BLOCK WRITE OPERATION (BWRIT, BWRITA)

This command enables to write the same data (logic 0 or 1) in a selected block of eight successive columns (8 × 32 bits) during a single access cycle. The column block is selected by A_3 to A_7 of column address input, and A_0, A_1, and A_2 are ignored and the data to be written is stored in color register by SMRS command with A_6=High.
Column data masking is provided on an individual column basis for each byte of data. The column mask is driven on the DQ pins during block write command. The DQ column mask function is segmented on a per byte basis (i.e. DQ_{0-7} provides the column mask for data byte 0-7, DQ_{8-15}, and so on.). A DQ column mask of H enables the particular column to be written while a value of L disables writing of the data. The relationship between DQ bits and column within the block is logically equivalent within each byte (i.e. DQ0 masks column“0” for data bits [0-7], DQ_8 masks column“0” for data bits [8-15], DQ_1 masks column“1” for data bits [0-7], DQ_9 masks column “1” for data bits [8-15], and so on).

Fig. 3 - Block Write & Write Per Bit Operation (Example for DQ_{0-7})



Note: Same organization for every bytes (DQ_{0-7}, DQ_{8-15}, DQ_{16-23}, DQ_{24-31}).

■ FUNCTIONAL DESCRIPTION (Continued)

BLOCK WRITE OPERATION (BWRIT, BWRITA) (Continued)

The block write is always non-burst, independent of the burst length and burst type that has been programmed into the mode register. Back-to-back block write operation is allowed with the block write cycle time (t_{BWC}) is satisfied.
If WPB was enabled to the bank by ACTVM command, then write-per-bit masking of the color register data is enabled. If WPB was disabled, the write per bit masking of the color register data is disabled. When WPB is enabled, the data in the color register (accessed via special register access), is masked by the data in the mask register (accessed via special register access), a mask register bit=High enables the associated data bit to be written and mask bit=Low disables the associated data bit from being written.
DQM masking provides independent data byte masking during block write exactly the same as it dose during normal write operations, except that the control is extended to the 8 consecutive columns of the block.

AUTO-REFRESH (REF)

Auto-refresh uses the internal refresh address counter. The SGRAM Auto-refresh command (REF) generates Precharge command internally. All banks of SGRAM should be precharged prior to the Auto-refresh command. The Auto-refresh command should also be asserted every 16 μs or a total 1,024 refresh commands within a 16.4 ms period.

SELF-REFRESH ENTRY (SELF)

Self-refresh function provides automatic refresh by an internal timer as well as Auto-refresh and will continue the refresh function until cancelled by Self-refresh Exit command (SELFX).
The Self-refresh is entered by applying an Auto-refresh command in conjunction with CKE = Low (SELF). Once SGRAM enters the self-refresh mode, all inputs except for CKE will be “DON’T CARE” (either logic high or low level state) and outputs will be in a High-Z state. During a self-refresh mode, CKE = Low should be maintained.
Note that a total of 1,024 auto-refresh commands within 1 ms must be asserted prior to the self-refresh mode entry.

SELF-REFRESH EXIT (SELFX)

To exit self-refresh mode, apply minimum 4 clock cycle before CKE brought high, and then the NOP command (NOP) or Deselect command (DESL) should be asserted within one t_{RC} period. Refer to Timing Diagram for the detail.
It is recommended to assert an Auto-refresh command just after the t_{RC} period to avoid the violation of refresh period.
Note that a total of 1,024 auto-refresh commands within 1 ms must be asserted after the self-refresh exit.

MODE REGISTER SET (MRS)

The mode register of SGRAM provides a variety of different operations. The register consists of five operation fields; Burst Length, Burst Type, CAS latency, Test Mode, and Operation Code. Refer to MODE REGISTER TABLE in page 33.
The mode register can be programmed by the Mode Register Set command (MRS). Each field is set by the address line. Once a mode register is programmed, the contents of the register will be held.
The condition of the mode register is undefined after the power-up stage. It is required to set each field after initialization of SGRAM. Refer to POWER-UP INITIALIZATION below.

SPECIAL MODE REGESTER SET (SMRS)

The Special Mode Register Set command (SMRS) is applicable to set the color register for block write operation or to set the mask register for write per bit operation. Color register and mask register is determined by the input level of A_6 and A_5 respectively, and it is illegal to determine both color register and mask register within one command (A_6=A_5=H is illegal). The data to be stored in color register or mask register is input via DQ pins. The SMRS command can be valid during idle or bank active state. Both color register and mask register are not cleared or reset until changed by another SMRS cycle (or part loses power). Refer to the SPECIAL MODE REGISTER TABLE in page 33.

■ FUNCTIONAL DESCRIPTION (Continued)

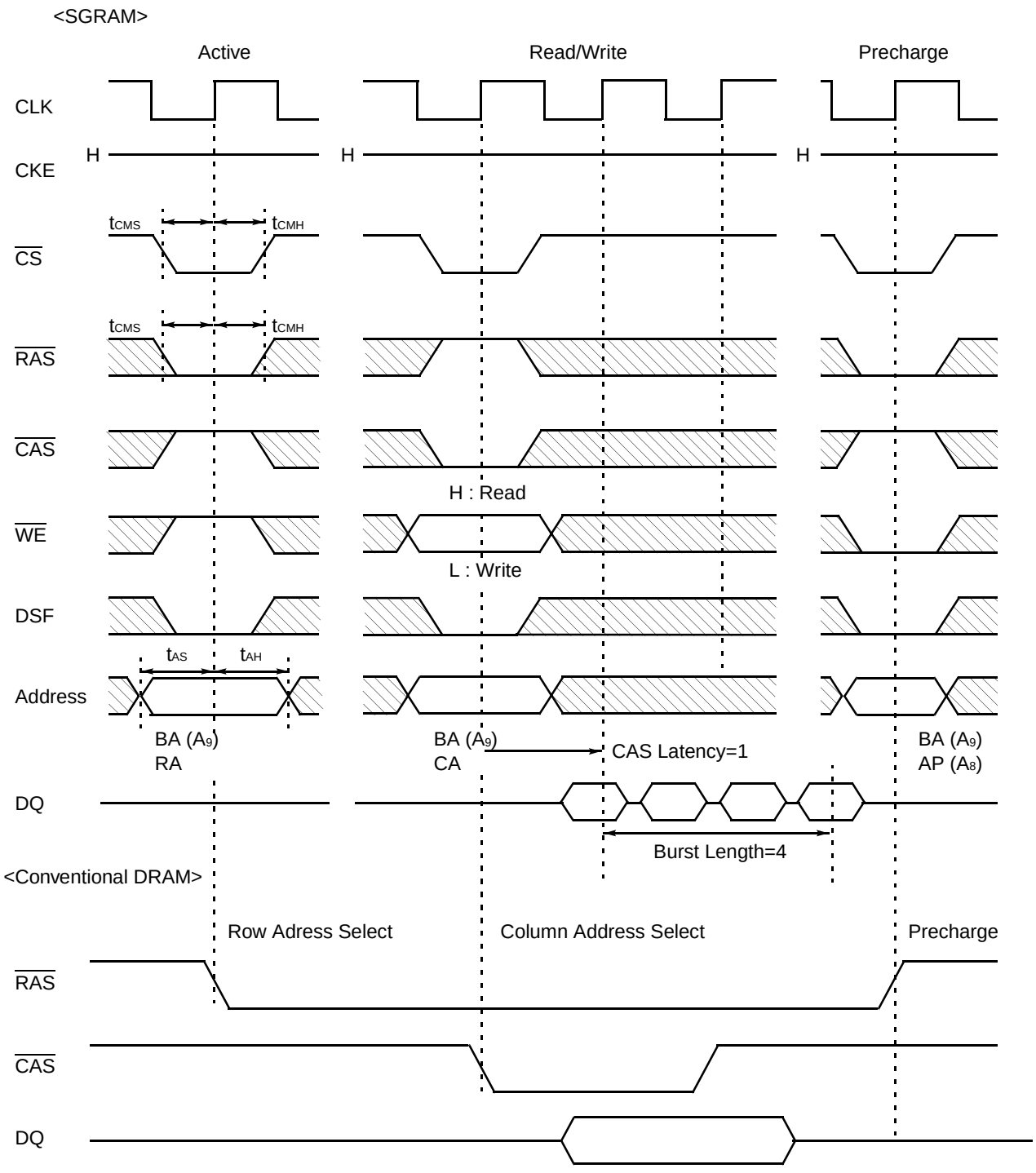
POWER-UP INITIALIZATION

The SGRAM internal condition after power-up will be undefined. It is required to follow the following Power On Sequence to execute read or write operation.

1. Apply power and start clock. Attempt to maintain either NOP or DESL command at the input.
2. Maintain stable power, stable clock, and NOP condition for a minimum of 200 µs.
3. Precharge all banks by Precharge (PRE) or Precharge All command (PALL).
4. Assert minimum of 8 Auto-refresh command(REF).
5. Program the mode register by Mode Register Set command(MRS).

In addition, it is recommended $DQM_{0\text{-}3}$ and CKE to track V_{CC} to insure that output is High-Z state. The Mode Register Set command (MRS) can be set before 8 Auto-refresh command (REF).

Fig. 4 - Basic Timing for Conventional DRAM vs Synchronous Graphic RAM



■ CAPACITANCE

(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance, Address	C_{IN1}	—	5	pF
Input Capacitance, Except for address	C_{IN2}	—	5	pF
I/O Capacitance	$C_{I/O}$	—	7	pF

■ RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Notes	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage		V_{CC}, V_{CCQ}	3.0	3.3	3.6	V
		V_{SS}, V_{SSQ}	0	0	0	V
Input High Voltage	1	V_{IH}	2.0	—	V_{CC} + 0.3	V
Input Low Voltage	2	V_{IL}	–0.3	—	0.8	V
Ambient Temperature		T_A	0	—	70	°C

Notes:1. Overshoot limit : V_{IH}(max.)=V_{CC}+1.3 V with a pullsewidth≤5 ns.

2. Undershoot limit: : V_{IL}(min.)= –1.3 V with a pullsewidth≤5 ns.

■ DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) **Notes 1, 2**

Parameter		Symbol	Conditions	Value		Unit
				Min.	Max.	
Output High Voltage		V_{OH}(DC)	I_{OH} = –2 mA	2.4	—	V
Output Low Voltage		V_{OL}(DC)	I_{OL} = 2 mA	—	0.4	V
Input Leakage Current (Any Input)		I_{LI}	0 V ≤ V_{IN} ≤ V_{CC}; All other pins not under test = 0 V	–10	10	µA
Output Leakage Current		I_{LO}	0 V ≤ V_{IN} ≤ V_{CC}; Data out disabled	–10	10	µA
Operating Current (Average Power Supply Current)	MB81G83222-010	I_{CC1S}	No Burst : t_{CK} = min. t_{RC} = min. One bank active	—	185	mA
	MB81G83222-012				160	
	MB81G83222-015				140	
	MB81G83222-010	I_{CC1D}	No Burst : t_{CK} = min. t_{RC} = min. All banks active	—	280	mA
	MB81G83222-012				245	
	MB81G83222-015				210	
Precharge Standby Current (Power Supply Current)		I_{CC2P}	CKE = V_{IL} All banks idle t_{CK} = min. Power down mode	—	2	mA
	MB81G83222-010	I_{CC2N}	CKE = V_{IH} All banks idle t_{CK} = min.	—	70	mA
	MB81G83222-012				65	
	MB81G83222-015				55	
Active Standby Current (Power Supply Current)		I_{CC3P}	CKE = V_{IL} Any banks active t_{CK} = min.	—	35	mA
	MB81G83222-010	I_{CC3N}	CKE = VI_{H} Any banks active t_{CK} = min.	—	75	mA
	MB81G83222-012				70	
	MB81G83222-015				60	
Burst mode Current (Average Power Supply Current)	MB81G83222-010	I_{CC4}	t_{CK} = min.	—	250	mA
	MB81G83222-012				210	
	MB81G83222-015				175	
Refresh Current #1 (Average Power Supply Current)	MB81G83222-010	I_{CC5S}	Auto-Refresh; t_{CK} = min. t_{RC}=min.	—	155	mA
	MB81G83222-012				135	
	MB81G83222-015				120	
Refresh Current #1 (Average Power Supply Current)	MB81G83222-010	I_{CC5D}	Auto-Refresh; t_{CK} = min. t_{RC}=min. t_{RRD} = min.	—	235	mA
	MB81G83222-012				205	
	MB81G83222-015				175	

■ DC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.) **Notes 1, 2**

Parameter		Symbol	Conditions	Value		Unit
				Min.	Max.	
Refresh Current #2 (Average Power Supply Current)		I_{CC6}	Self-Refresh; CKE = V_{IL}	—	2	mA
Block Write Current (Average Power Supply Current)	MB81G83222-010	I_{CC7}	Block Write; t_{BWC} = min.	—	165	mA
	MB81G83222-012				140	
	MB81G83222-015				115	

■ AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) **Notes 2, 3, 4**

Parameter		Notes	Symbol	MB81G83222-010		MB81G83222-012		MB81G83222-015		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
Clock Period	CAS latency=1		t_{CK}	30	—	35	—	40	—	ns
	CAS latency=2			15		17.5		20		ns
	CAS latency=3			10		12		15		ns
Clock High Time			t_{CH}	3.5	—	4	—	5	—	ns
Clock Low Time			t_{CL}	3.5	—	4	—	5	—	ns
Data-in Setup Time			t_{DS}	3	—	3.5	—	3.5	—	ns
Data-in Hold Time			t_{DH}	1	—	1.5	—	1.5	—	ns
Address Setup Time			t_{AS}	3	—	3.5	—	3.5	—	ns
Address Hold Time			t_{AH}	1	—	1.5	—	1.5	—	ns
CKE Setup Time			t_{CKS}	3	—	3.5	—	3.5	—	ns
CKE Hold Time			t_{CKH}	1	—	1.5	—	1.5	—	ns
Command Setup Time (CS, RAS, CAS, WE, DSF, DQM)			t_{CMS}	3	—	3.5	—	3.5	—	ns
Command Hold Time (CS, RAS, CAS, WE, DSF, DQM)			t_{CMH}	1	—	1.5	—	1.5	—	ns
Access Time from Clock (t_{CK}=min.)	CAS latency=1	5, 6	t_{AC}	—	28	—	32	—	35	ns
	CAS latency=2				13		14.5		16	ns
	CAS latency=3				9		11		12	ns
Output in Low-Z			t_{LZ}	3	—	3	—	3	—	ns
Output in High-Z	CAS latency=1	7	t_{HZ}	4	20	4	24	4	30	ns
	CAS latency=2			4	15	4	17.5	4	20	ns
	CAS latency=3			4	10	4	12	4	15	ns
Output Hold Time			t_{OH}	4	—	4	—	4	—	ns
Time between Refresh			t_{REF}	—	16.4	—	16.4	—	16.4	ms
Transition Time			t_T	0.5	30	0.5	30	0.5	30	ns
Power Down Exit Time			t_{PDE}	12	—	14	—	17	—	ns

■ AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.) **Notes 2, 3, 4**

BASE VALUES FOR CLOCK COUNT/LATENCY

Parameter	Notes	Symbol	MB81G83222-010		MB81G83222-012		MB81G83222-015		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
RAS Cycle Time	8	t_{RC}	90	—	106	—	125	—	ns
RAS Access Time	9	t_{RAC}	—	58	—	67	—	75	ns
CAS Access Time	10, 13	t_{CAC}	—	28	—	32	—	35	ns
RAS Precharge Time		t_{RP}	30	—	36	—	45	—	ns
RAS Active Time		t_{RAS}	60	100000	70	100000	80	100000	ns
RAS to CAS Delay Time	11	t_{RCD}	30	—	35	—	40	—	ns
Write Recovery Time		t_{WR}	10	—	12	—	15	—	ns
Write to Precharge Delay Time		t_{RWL}	15	—	17.5	—	20	—	ns
Block Write to Precharge Delay Time		t_{BWL}	20	—	24	—	30	—	ns
RAS to RAS Bank Active Delay Time		t_{RRD}	20	—	24	—	30	—	ns
Block Write Cycle Time		t_{BWC}	20	—	24	—	30	—	ns
Mode and Special Mode Register Cycle Time		t_{RSC}	20	—	24	—	30	—	ns

CLOCK COUNT FORMULA **Note 13**

$$\text{Clock} \geq \frac{\text{Base Value}}{\text{Clock Period}} \quad \text{(Round off a whole number)}$$

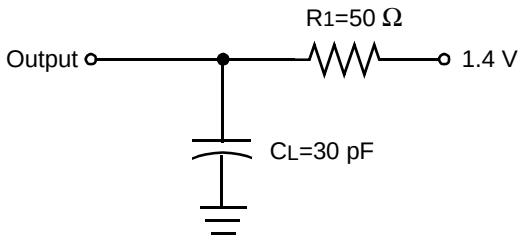
LATENCY - FIXED VALUES

(The latency values on these parameters are fixed regardless of clock period.)

Parameter	Notes	Symbol	MB81G83222-010	MB81G83222-012	MB81G83222-015	Unit
CKE to Clock Disable		I_{CKE}	1	1	1	cycle
DQM to Output in High-Z		I_{DQZ}	2	2	2	cycle
DQM to Input Data Delay		I_{DQD}	0	0	0	cycle
Last Output to Write Command Delay		I_{OWD}	2	2	2	cycle
Write Command to Input Data Delay		I_{DWD}	0	0	0	cycle
Precharge to Output in High-Z Delay	CL = 1	I_{ROH}	1	1	1	cycle
	CL = 2		2	2	2	cycle
	CL = 3		3	3	3	cycle
Burst Stop Command to Output in High-Z Delay	CL = 1	I_{BSH}	1	1	1	cycle
	CL = 2		2	2	2	cycle
	CL = 3		3	3	3	cycle
CAS to CAS Delay (min.)		I_{CCD}	1	1	1	cycle
CAS Bank Delay (min.)		I_{CBD}	1	1	1	cycle

Notes:1. I_{CC} depends on the output termination or load conditions, clock cycle rate, and signal clocking rate; The specified values are obtained with the output open and no termination register.
2. An initial pause (DESL or NOP) of 200 μs is required after power-up followed by a minimum of eight Auto-refresh cycles.
3. AC characteristics assume t_T = 1 ns and 30 pF of capacitive load.
4. 1.4V is the reference level for measuring timing of input signals. Transition times are measured between V_{IH} (min.) and V_{IL} (max.).
5. Assumes t_{RCD} and t_{CAC} are satisfied.
6. t_{AC} also specifies the access time at burst mode except for first access.
7. Specified where output buffer is no longer driven.
8. Actual clock count of t_{RC} (l_{RC}) will be sum of clock count of t_{RAS} (l_{RAS}) and t_{RP} (l_{RP}).
9. t_{RAC} is a reference value. Maximum value is obtained from the sum of t_{RCD} (min.) and t_{CAC} (max.).
10. Assumes t_{RAC} and t_{AC} are satisfied.
11. Operation within the t_{RCD} (min.) ensures that t_{RAC} can be met; if t_{RCD} is greater than the specified t_{RCD} (min.), access time is determined by t_{CAC} or t_{AC}.
12. All base values are measured from the clock edge at the command input to the clock edge for the next command input. All clock counts are calculated by a simple formula: clock count equals base value divided by clock period (round off to a whole number).
13. The l_{CAC} is programmed by the mode register.

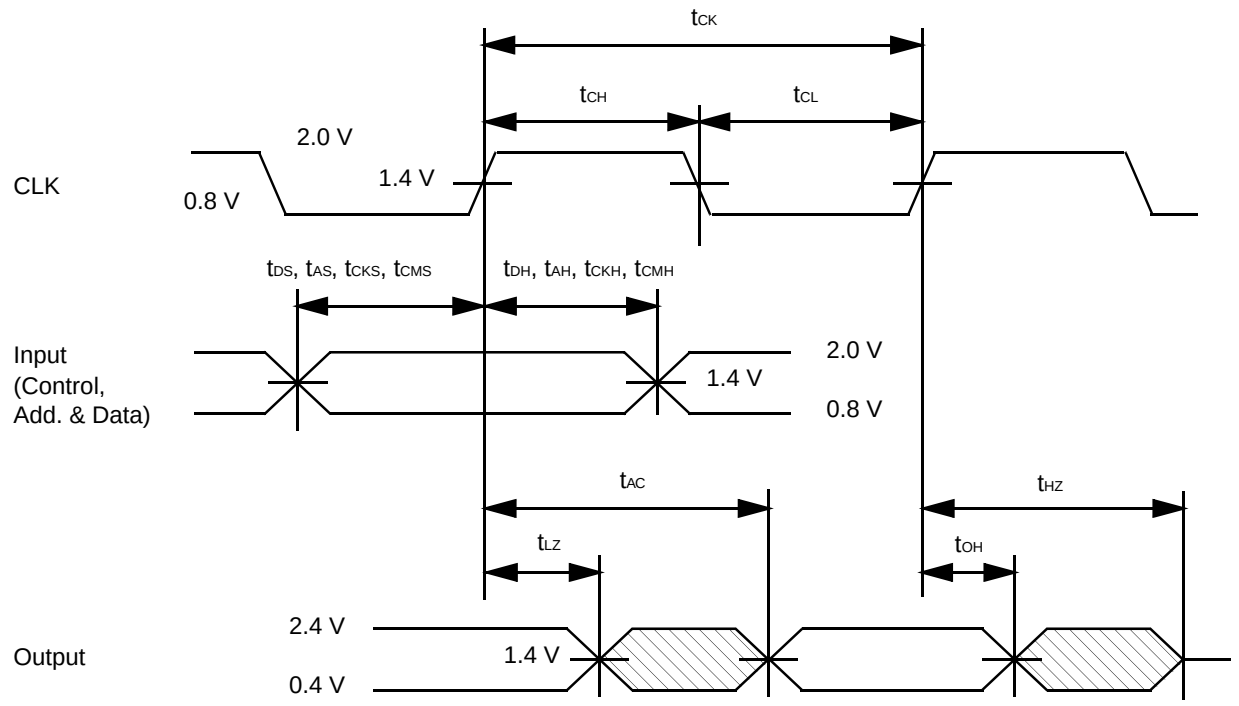
Fig. 5 - Example of AC Test Load Circuit



LVTTL

Note: AC characteristics are measured in this condition. This load circuits are not applicable for V_{OH} and V_{OL}.

Fig. 6 - TIMING DIAGRAM, SETUP, HOLD AND DELAY TIME



Note: Reference level of input signal is 1.4 V for LVTTL.
Access time is measured at 1.4 V for LVTTL.

Fig. 7 - TIMING DIAGRAM, DELAY TIME for Power Down Exit

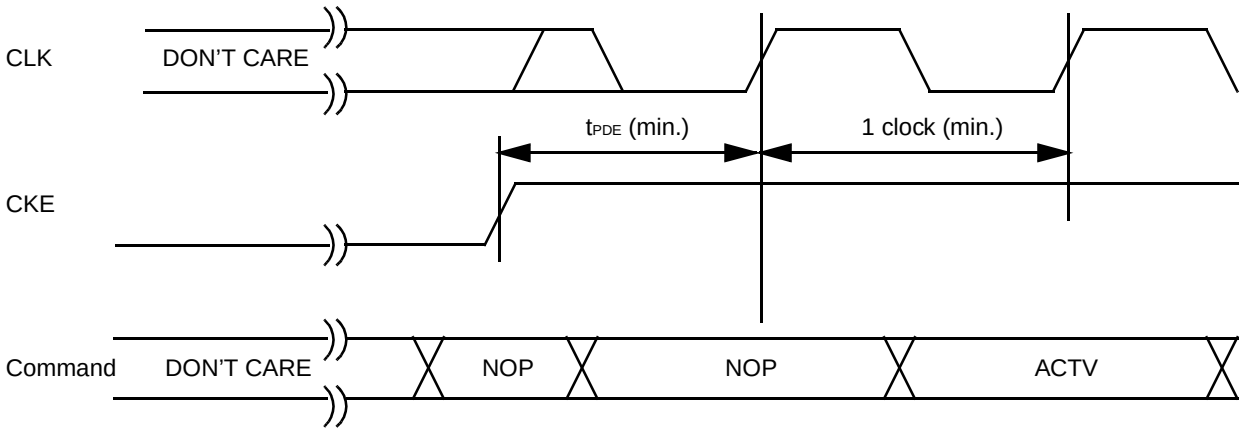
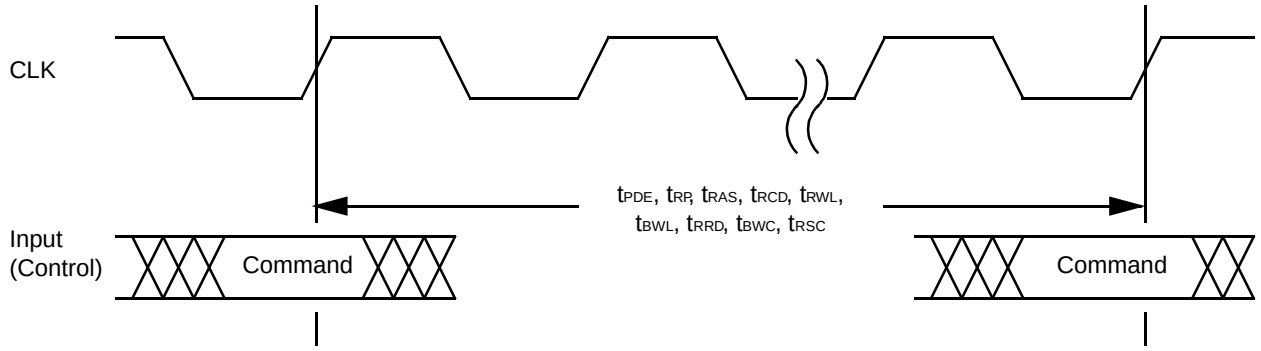
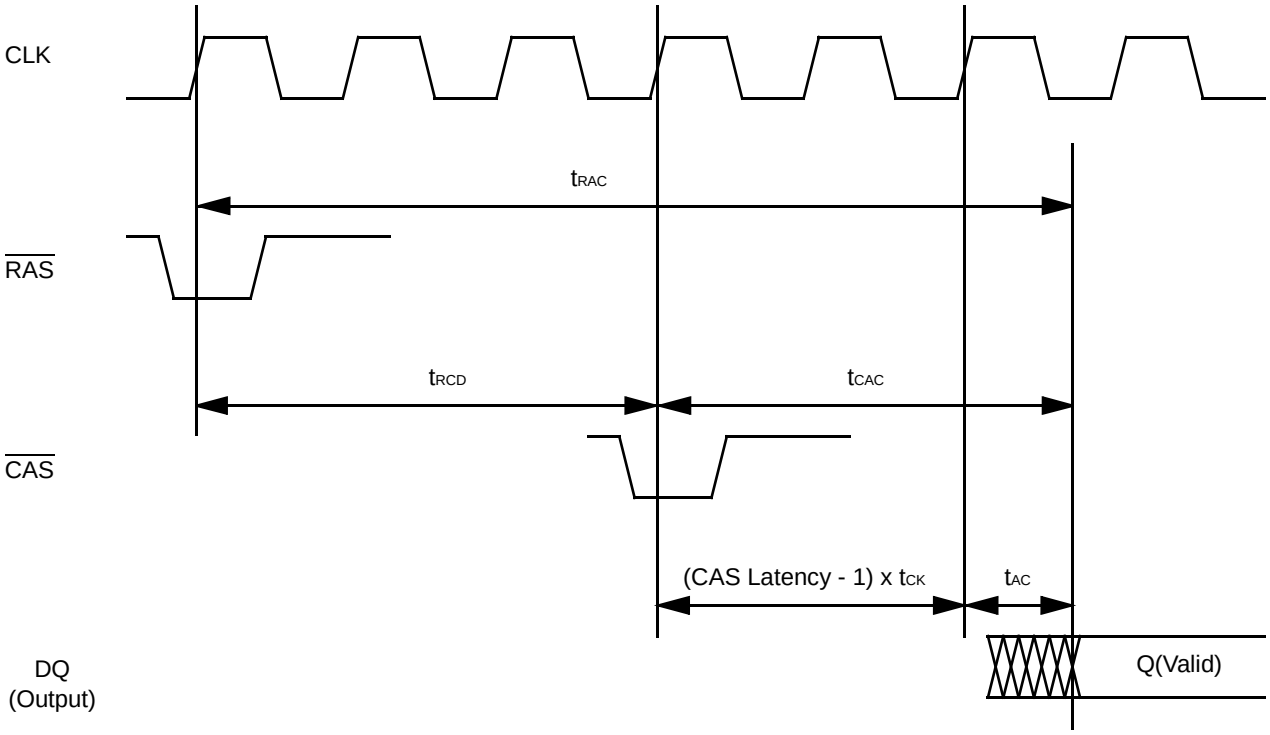


Fig. 8 - TIMING DIAGRAM, PULSE WIDTH



Note: This parameter is a limit value of the rising edge of the clock from one command input to next input.
t_{PDE} is the latency value from the rising edge of CKE.
Measurement reference voltage is 1.4 V.

Fig. 9 - TIMING DIAGRAM, ACCESS TIME



Note: t_{RAC} is a reference value. Data can be obtained after both t_{CAC} and t_{AC} are satisfied.

■ MODE REGISTER TABLE

MODE REGISTER SET

A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	ADDRESS
Op-code	0	0	CL			BT	BL			MODE REGISTER

A_6	A_5	A_4	CAS Latency
0	0	0	Reserved
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

A_2	A_1	A_0	Burst Length	
			BT=0	BT=1
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Full Column	Reserved

A_9	Op-code
0	Burst Read & Burst Write
1	Burst Read & Single Write

A_3	Burst Type
0	Sequential (Wrap round, Binary-up)
1	Interleave (Wrap round, Binary-up)

Note: When A_9=1, burst length at Write is always one regardless of BL value.

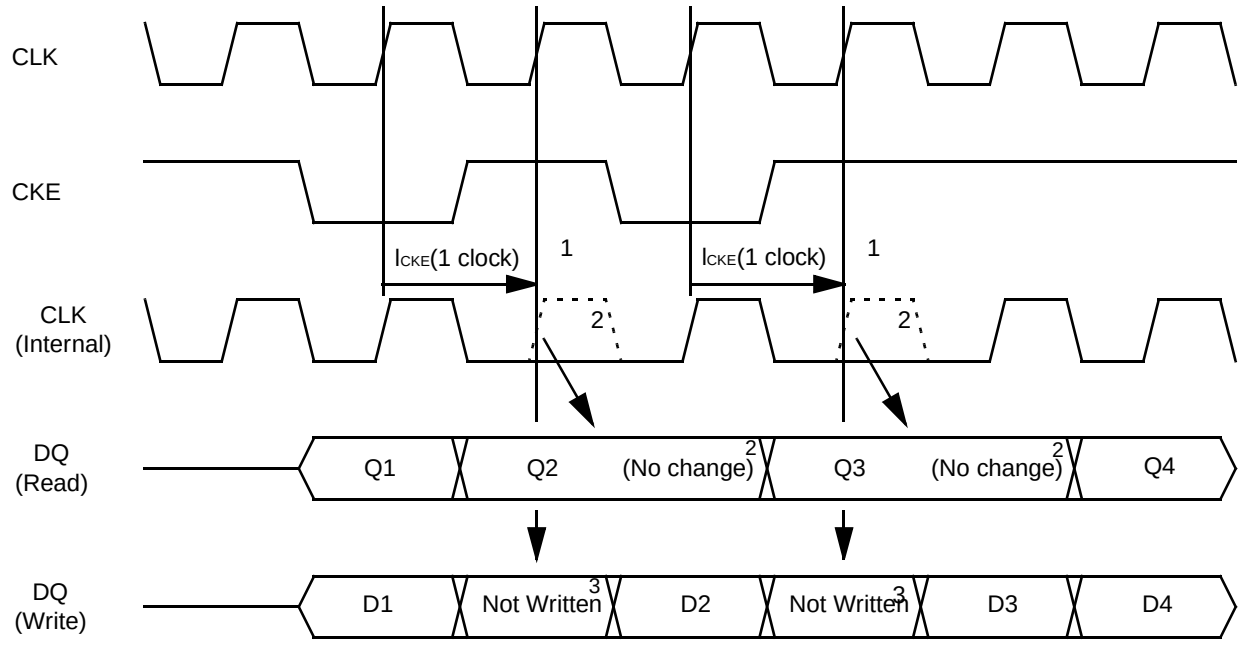
SPECIAL MODE REGISTER SET

A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	ADDRESS
0	0	0	LC	LM	0	0	0	0	0	SPECIAL MODE REGISTER

A_6	Load Color Register
0	Disable
1	Enable

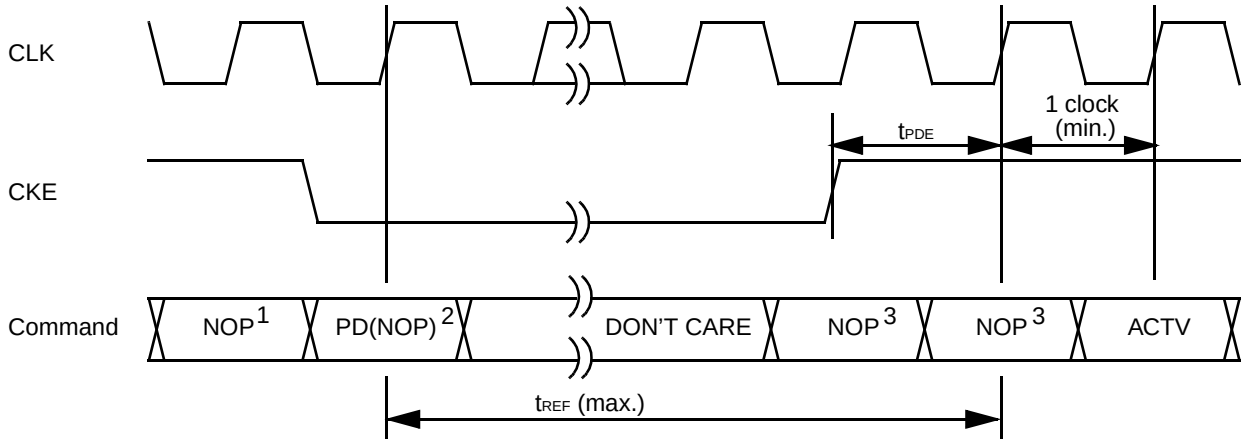
A_5	Load Mask Register
0	Disable
1	Enable

TIMING DIAGRAM-1 : CLOCK ENABLE - READ AND WRITE SUSPEND (@ BL = 4)



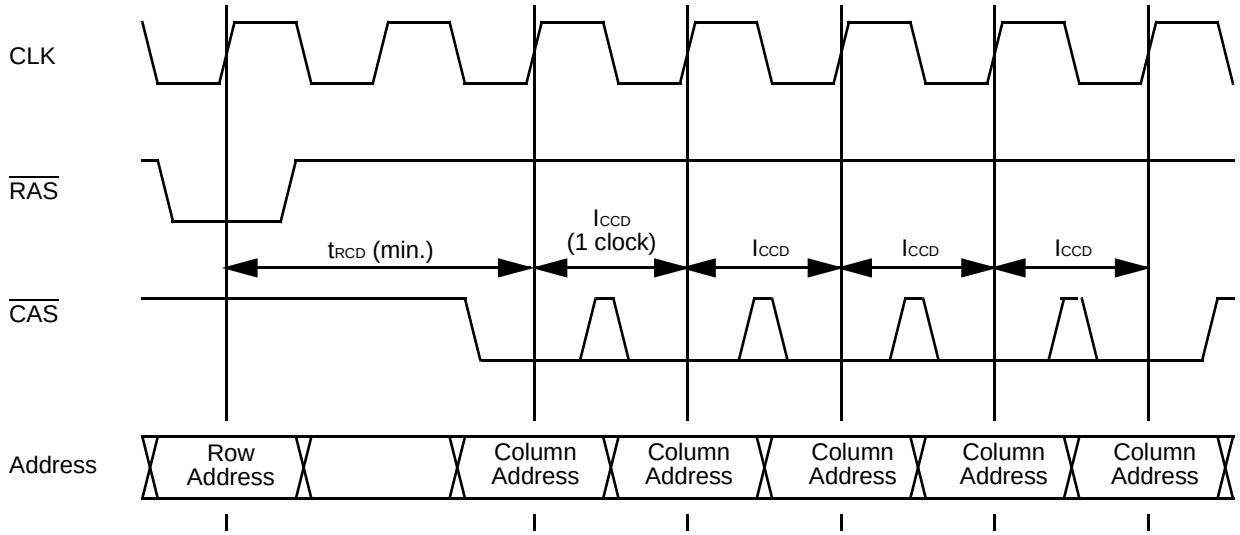
Notes: 1. The latency of CKE (l_{CKE}) is one clock.
2. During read mode, burst counter will not be incremented/decremented at the next clock of CSUS command. Output remain the same data.
3. During the write mode, data at the next clock of CSUS command is ignored.

TIMING DIAGRAM-2 : CLOCK ENABLE - POWER DOWN ENTRY AND EXIT



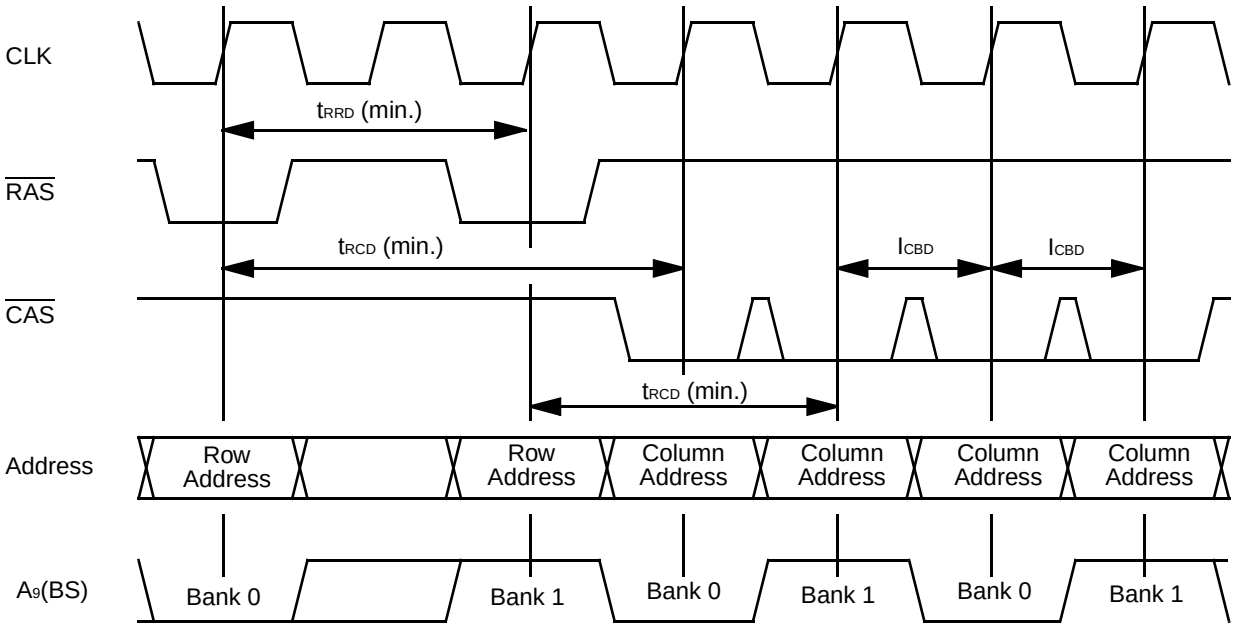
Notes: 1. Precharge command (PRE or PALL) should be asserted if any bank is active and in the burst mode.
2. Precharge command can be posted in conjunction with CKE when burst mode is ended at this clock.
3. The ACTV command can be latched after t_{PDE} (min) + 1clock(min.). It is recommended to apply NOP command in conjunction with CKE. It is also recommended to apply minimum of 4 clocks to stabilize external clock prior to ACTV command.

TIMING DIAGRAM-3 : COLUMN ADDRESS TO COLUMN ADDRESS INPUT DELAY

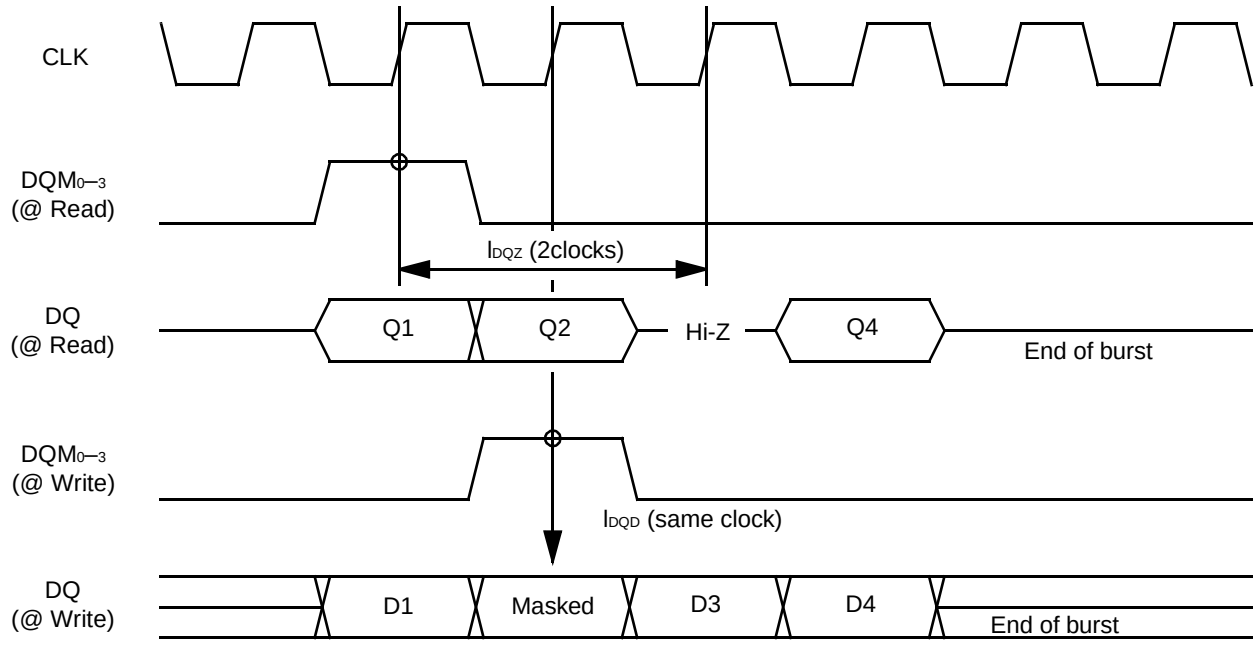


Note: $\overline{CAS}$ to $\overline{CAS}$ address delay can be one or more clock period.

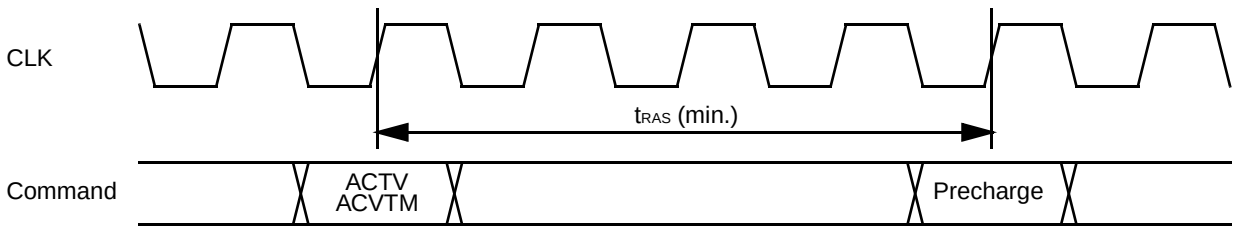
TIMING DIAGRAM-4 : DIFFERENT BANK ADDRESS INPUT DELAY



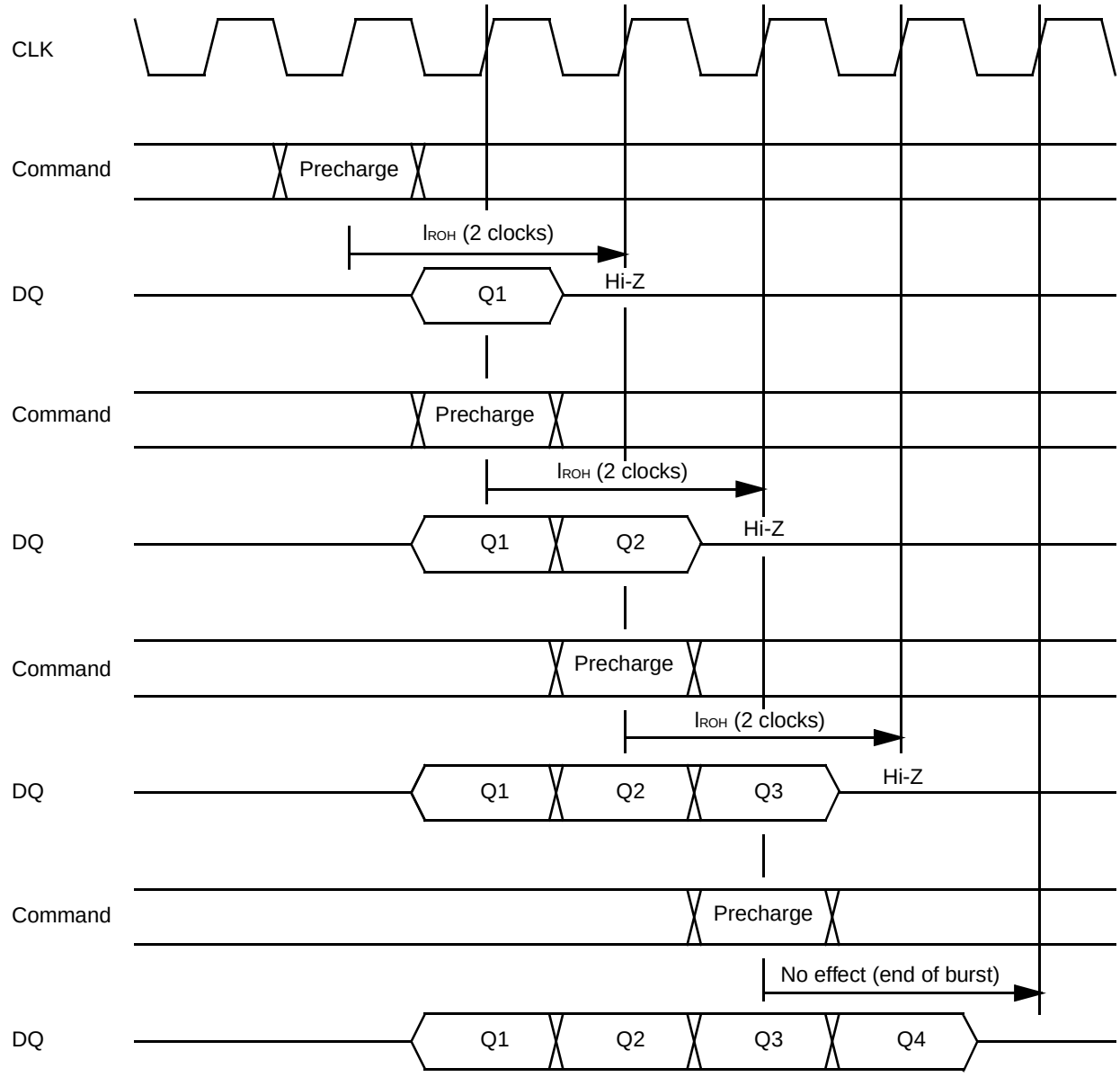
TIMING DIAGRAM-5 : DQM - INPUT MASK AND OUTPUT DISABLE (@ BL=4)



TIMING DIAGRAM-6 : PRECHARGE TIMING (APPLIED TO THE SAME BANK)

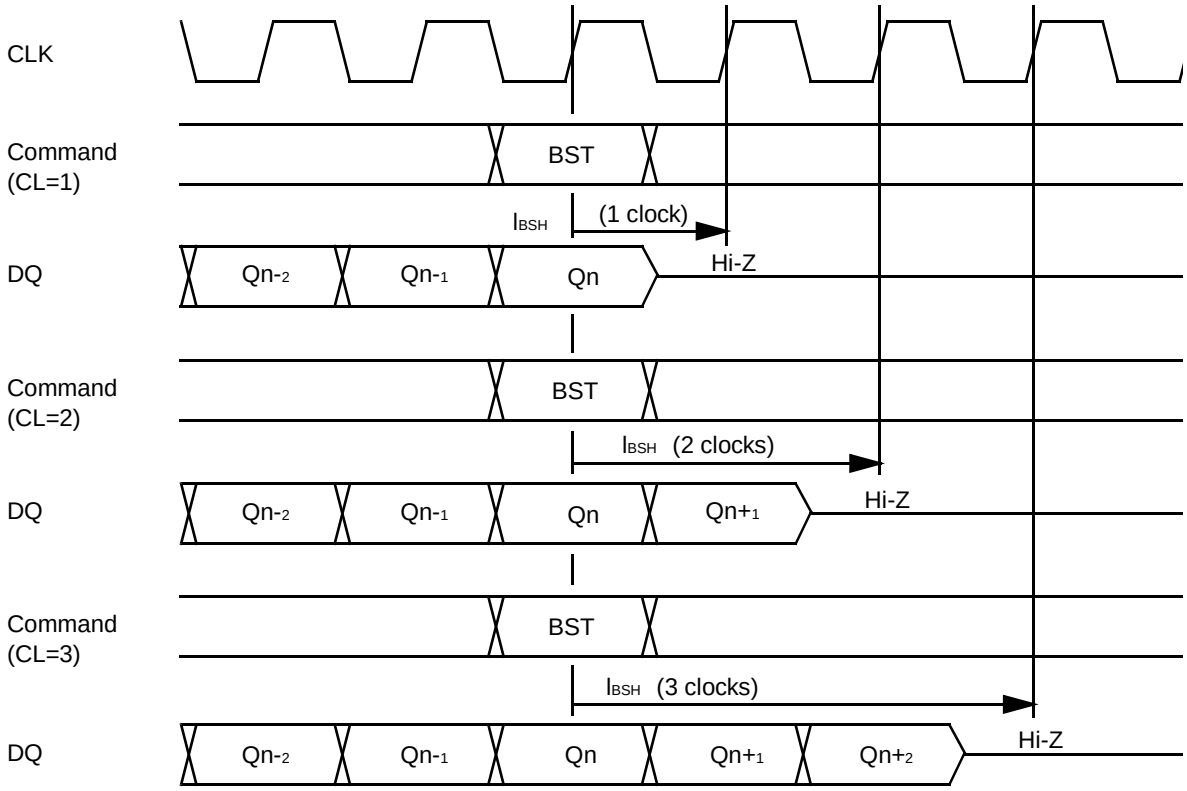


TIMING DIAGRAM-7 : READ INTERRUPTED BY PRECHARGE (Example @ CL=2, BL=4)



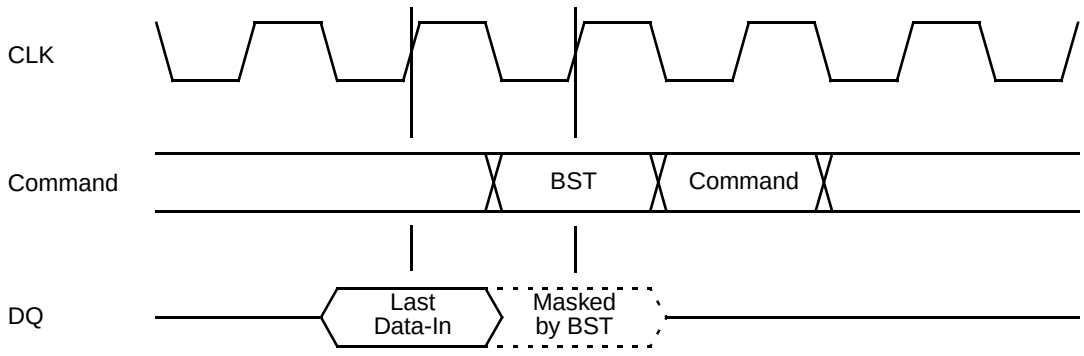
Note: In case of CL=1, the l_{ROH} is 1 clock.
In case of CL=2, the l_{ROH} is 2 clock.
In case of CL=3, the l_{ROH} is 3 clock.

TIMING DIAGRAM-8 : READ INTERRUPTED BY BURST STOP (Example @ BL=Full Column)



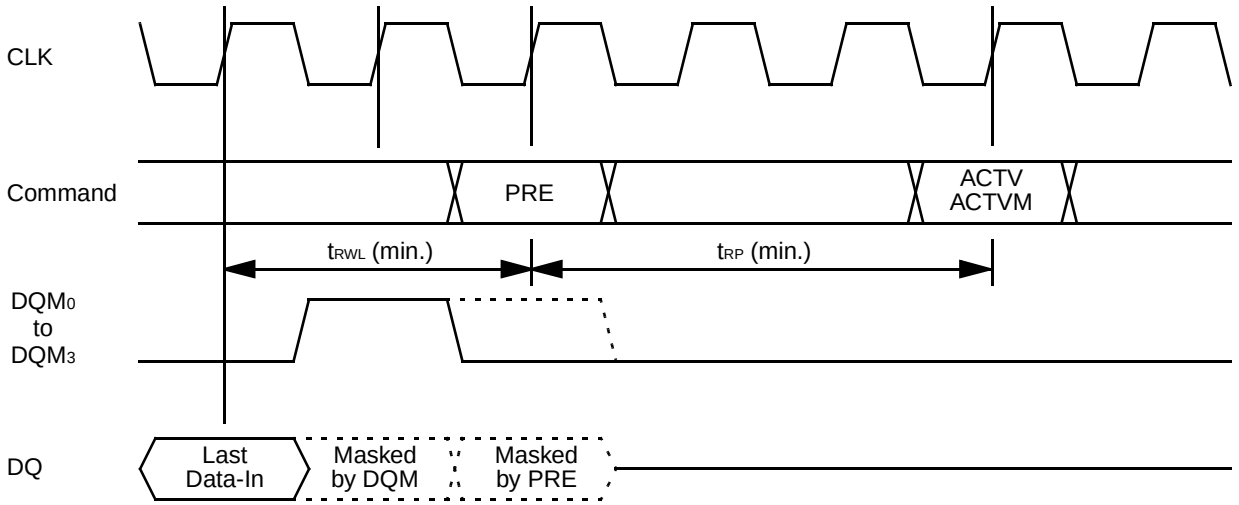
Note: The BST command is applicable to terminated the full column burst operation.
The selection of auto-precharge option is illegal during the full column burst operation except write command at BURST READ & SINGLE WRITE mode.

TIMING DIAGRAM-9 : WRITE INTERRUPTED BY BURST STOP (Example @ CL=2)



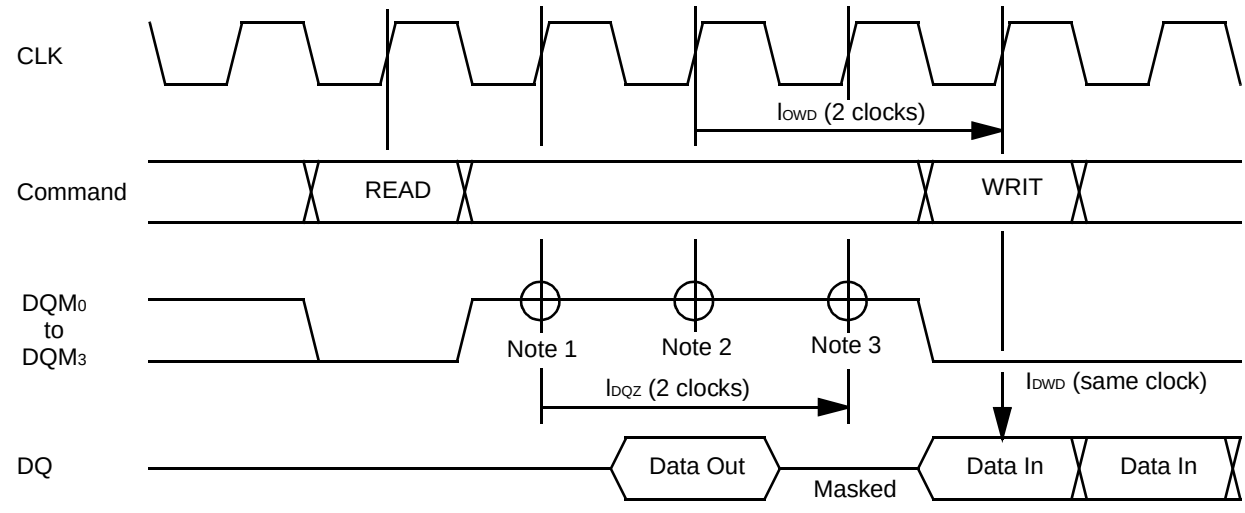
Note: The burst stop command is applicable only to full column burst operation.

TIMING DIAGRAM-10 : WRITE INTERRUPTED BY DQM0~3 & PRECHARGE (Example @ CL=2)



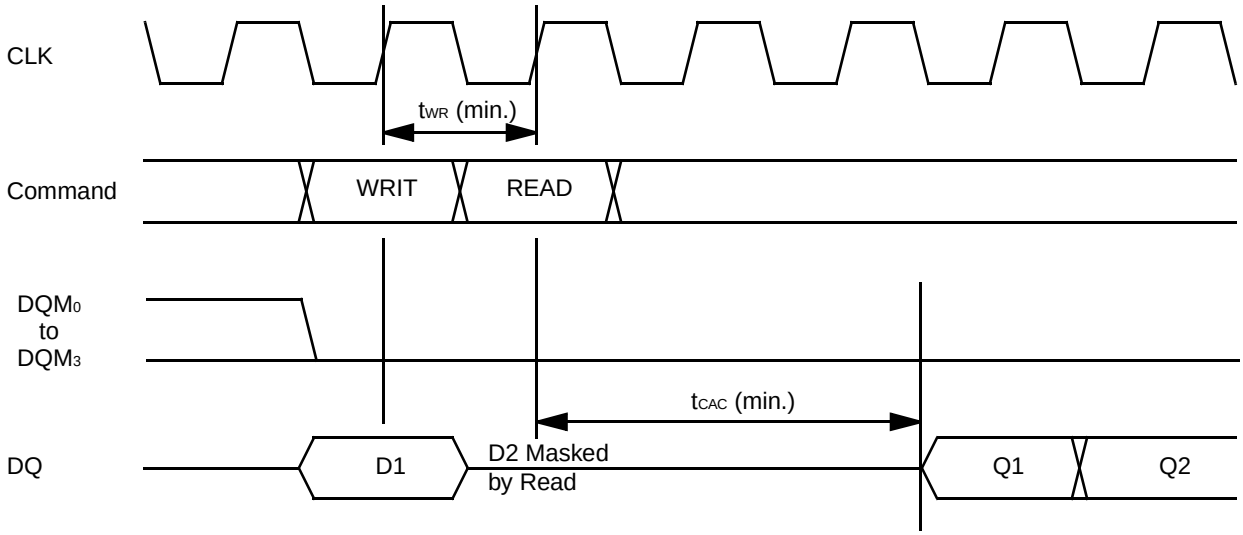
Note: The precharge command (PRE) should only be issued after the t_{RWL} of final data input is satisfied.

TIMING DIAGRAM-11 : READ INTERRUPTED BY WRITE (Example @ CL=2, BL≥4)



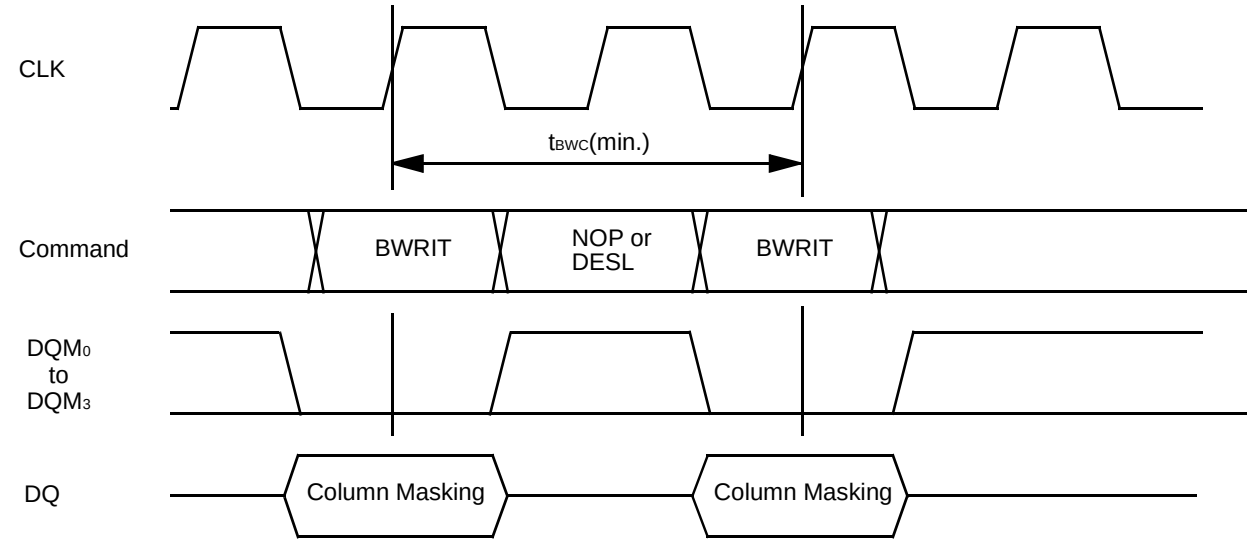
Notes: 1. First $DQM_{0–3}$ makes high impedance state (Hi-Z) between last output and first input data.
2. Second $DQM_{0–3}$ makes internal output data mask to avoid bus contention.
3. Third $DQM_{0–3}$ in illustrated above also makes internal output data mask. If burst read ends (final data output) at or after the second clock of burst write, this third $DQM_{0–3}$ is required to avoid internal bus contention.

TIMING DIAGRAM-12 : WRITE INTERRUPT BY READ TIMING (Example @ CL=3, BL>2)



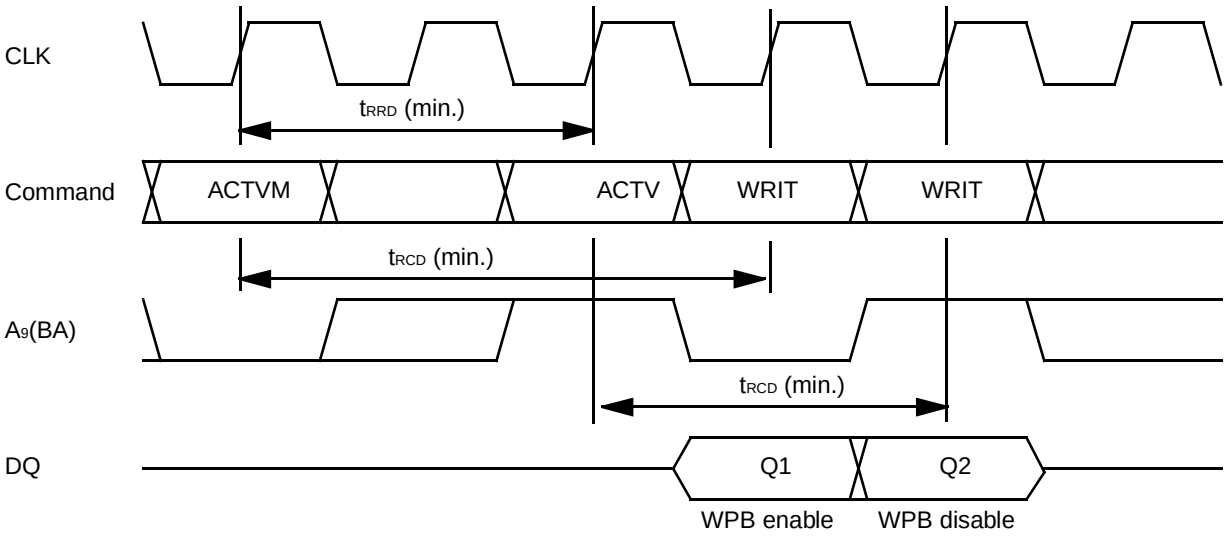
Note: Read command can be asserted at the next cycle of write command.
The write data after read command is masked by read command.

TIMING DIAGRAM-13 : BLOCK WRITE TIMING



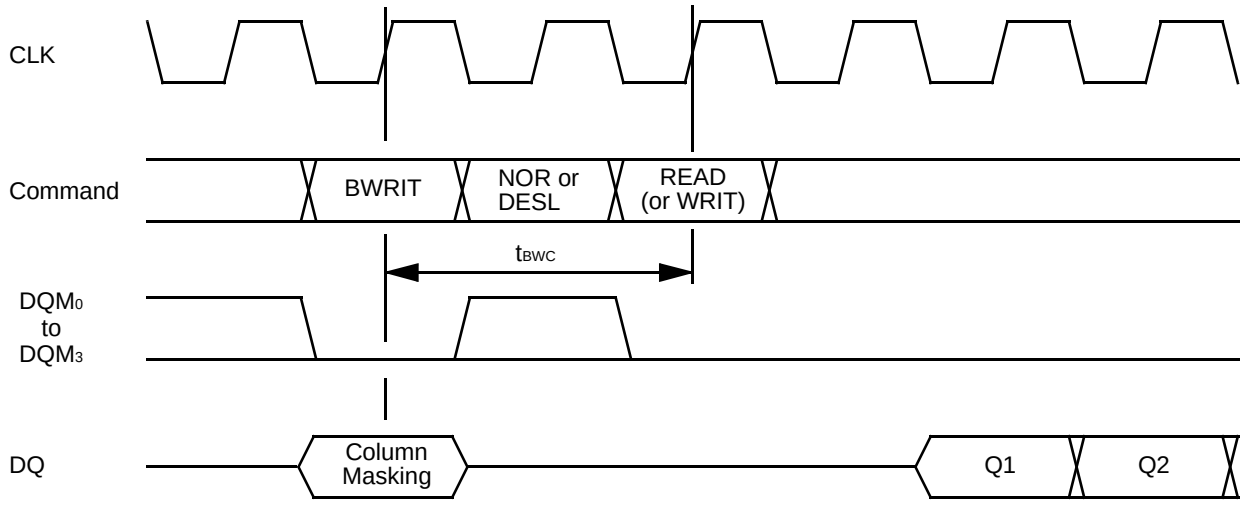
Note: DQ inputs are used for column masking. (DQ=H : Write Enable, DQ=L : Masked)
Write data is set by SMRS (Load Color Register) command.

TIMING DIAGRAM-14 : WRITE PER BIT TIMING



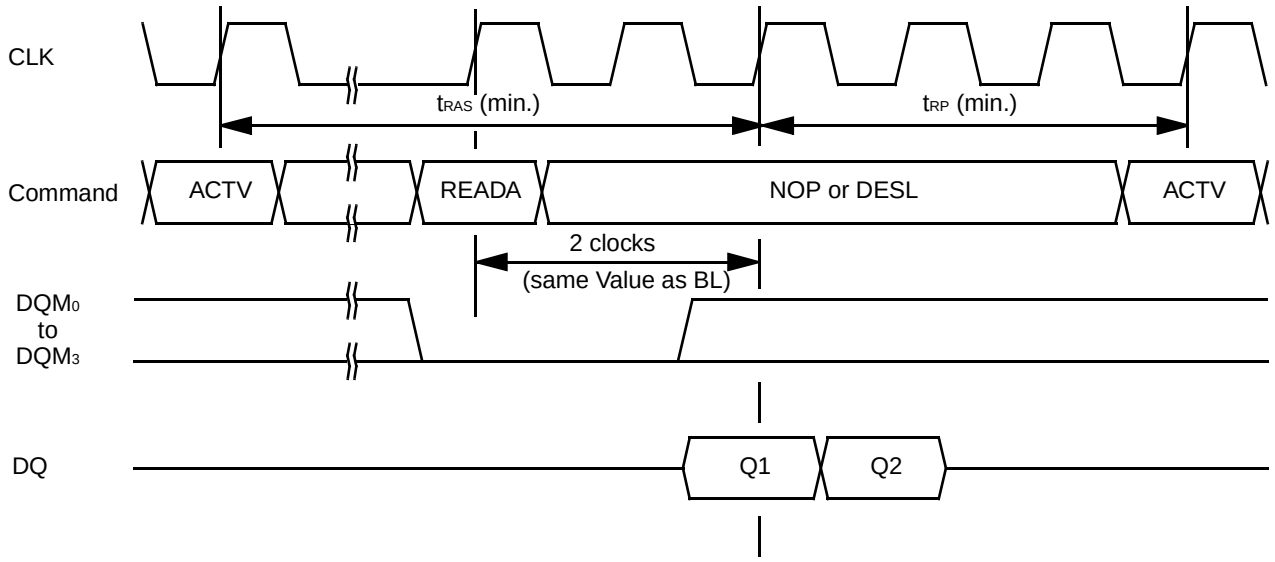
Note: WPB is available for the bank activated by ACTVM command.
Mask Data (Mask enable/disable) is set by SMRS (Load Mask Register) command.

TIMING DIAGRAM-15 : BLOCK WRITE TO READ/WRITE TIMING (Example @ CL=2, BL≥2)



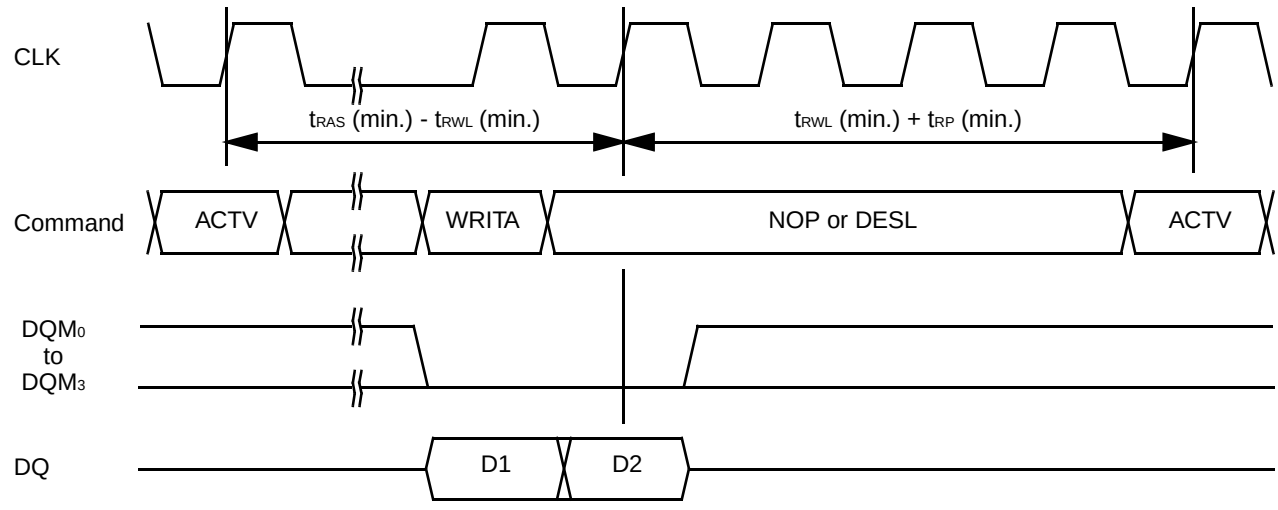
Note: Read/Write command can be asserted after t_{BWC} from block write command.

TIMING DIAGRAM-16 : READ WITH AUTO-PRECHARGE
(Example @ CL=2, BL=2 Applied to same bank)



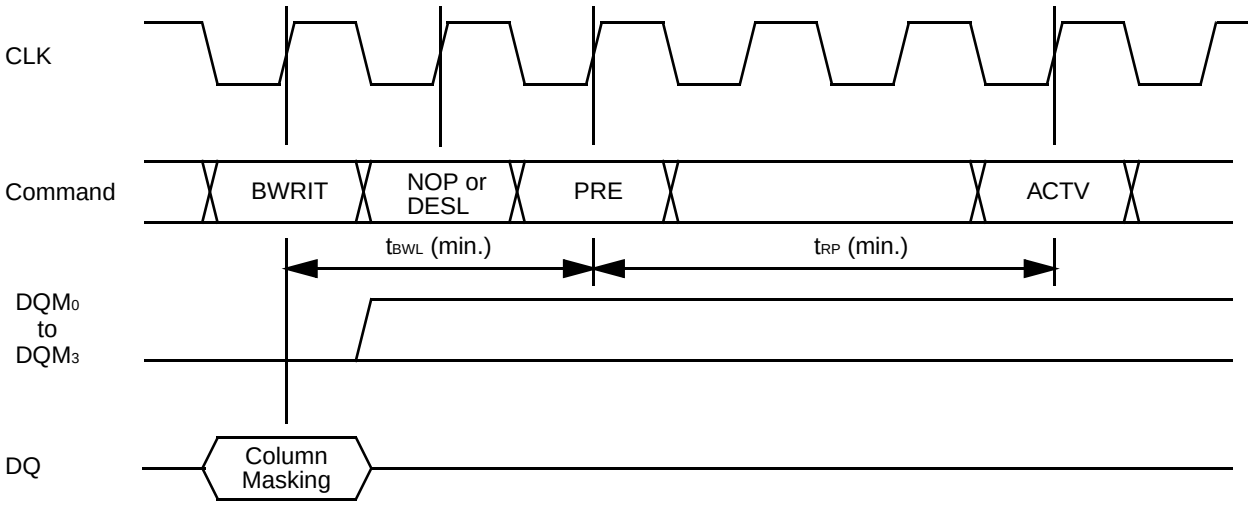
Note: Precharge at read with Auto-precharge command (READA) is started from number of clocks that is the same as Burst Length after READA command is asserted.

TIMING DIAGRAM-17 : WRITE WITH AUTO-PRECHARGE
(Example @ CL=2, BL=2 Applied to same bank)



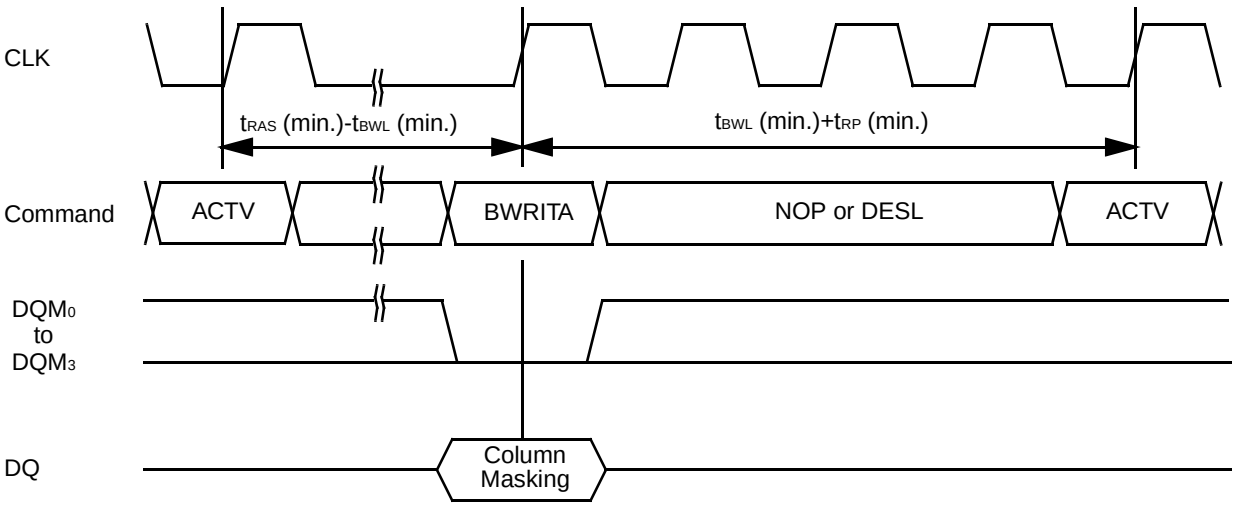
Note: Precharge at write with auto-precharge is started after the t_{RWL} from the end of burst.
Even if the final data is masked by DQM_{0-3}, the precharge does not start the clock of final data input.
Once auto precharge command is asserted, no new command within the same bank can be issued.
Auto-precharge command doesn't affect at full column burst operation except Burst Read & Single Write mode.

TIMING DIAGRAM-18 : BLOCK WRITE TO PRECHARGE TIMING



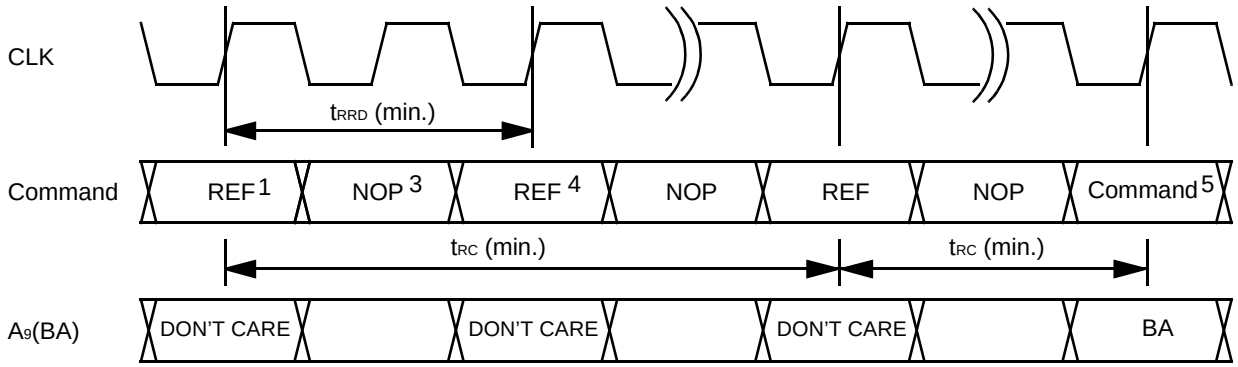
Note: The precharge command (PRE) should only be asserted after the t_{BWL} from last Block write command is satisfied.

TIMING DIAGRAM-19 : BLOCK WRITE WITH AUTO-PRECHARGE(Applied to same bank)



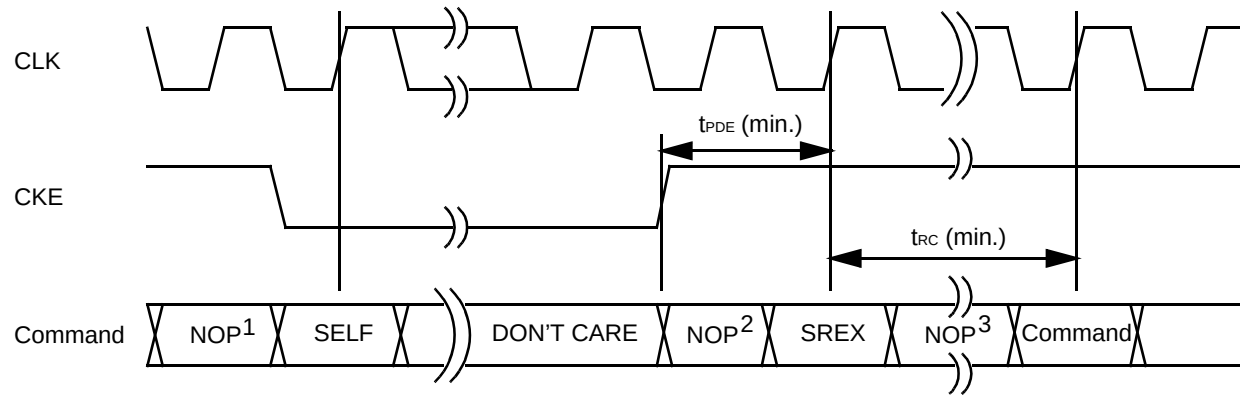
Note: Precharge at write with auto-precharge is started after the t_{BWL} from the BWRITA command.
Once auto precharge command is asserted, no new command within the same bank can be asserted.
Auto-precharge command doesn't affect at full column burst operation.

TIMING DIAGRAM-20 : AUTO-REFRESH TIMING



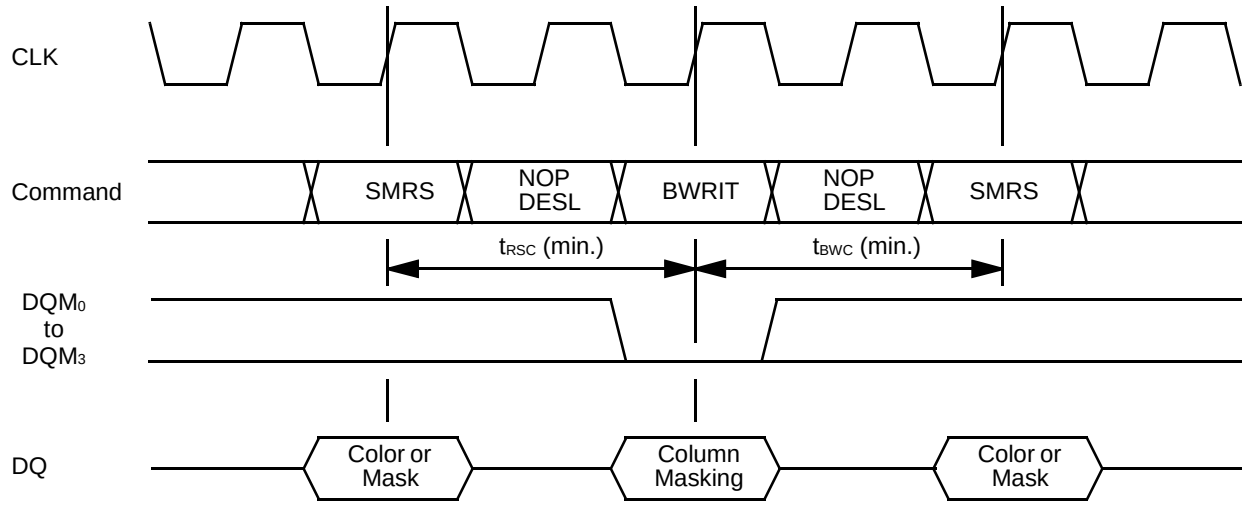
Notes: 1. All banks should be precharged prior to the first Auto-refresh command (REF).
2. Bank select is ignored at REF command. The refresh address and bank select are selected by internal refresh counter.
3. Either NOP or DESL command should be asserted during t_{RRD} and t_{RC} period while auto-refresh mode.
4. The second REF command can be asserted after t_{RRD} from the first REF command because the second REF command select the other bank.
5. Any activation command such as ACTV or MRS command other than REF command should be asserted after t_{RC} from the last REF command.

TIMING DIAGRAM-21 : SELF-REFRESH ENTRY AND EXIT TIMING



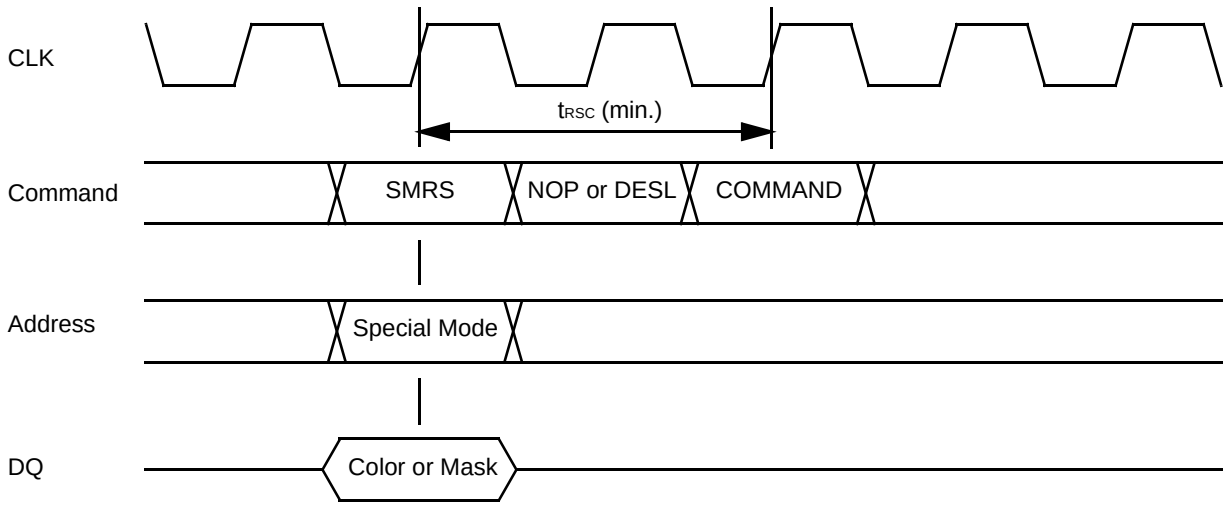
Notes: 1. Precharge command (PRE or PALL) should be asserted if any bank is active prior to Self-refresh Entry command (SELF).
2. The Self-refresh Exit command (SELFX) is latched after t_{PED} (min.). It is recommended to apply NOP command in conjunction with CKE. It is also recommended to apply minimum of 4 clocks to stabilize external clock prior to SELFX command.
3. Either NOP or DESL command can be used during t_{RC} period.

TIMING DIAGRAM-22 : BLOCK WRITE & SPECIAL MODE REGISTER SET TIMING



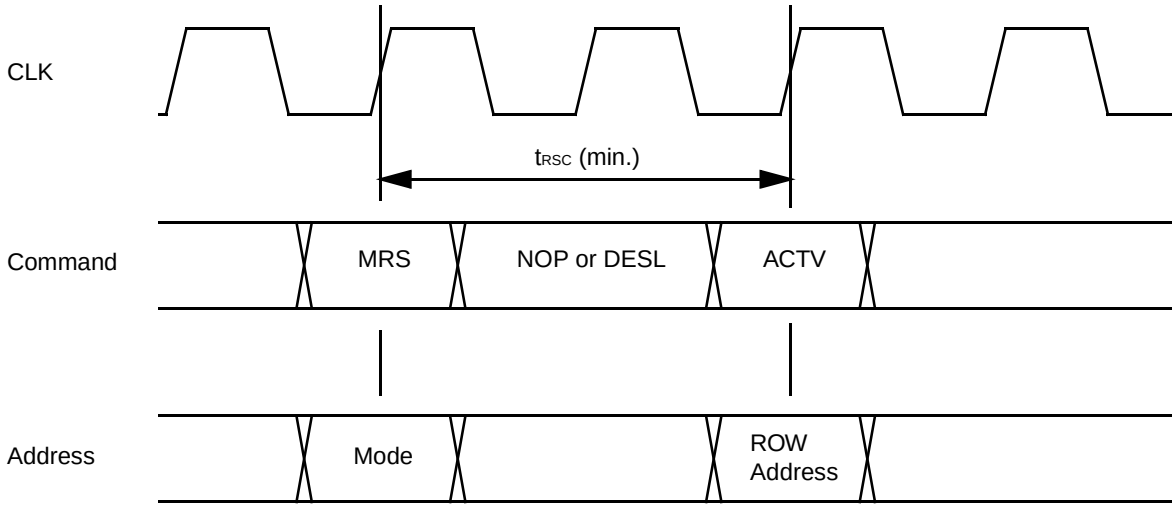
Notes: 1. Block Write command can be asserted after the t_{RSC} from special mode register set command is satisfied.
2. Special Mode Register Set command can be asserted after t_{BWC} from block write comand is satisfied.

TIMING DIAGRAM-23 : SPECIAL MODE REGISTER SET TIMING



Note: This command sets mask data or color data (depend on special mode address) for each I/O.
Mask data controls WPB operation (High : write enable, Low : Masked).
Color data is to be written by block write command.

TIMING DIAGRAM-24 : MODE REGISTER SET TIMING

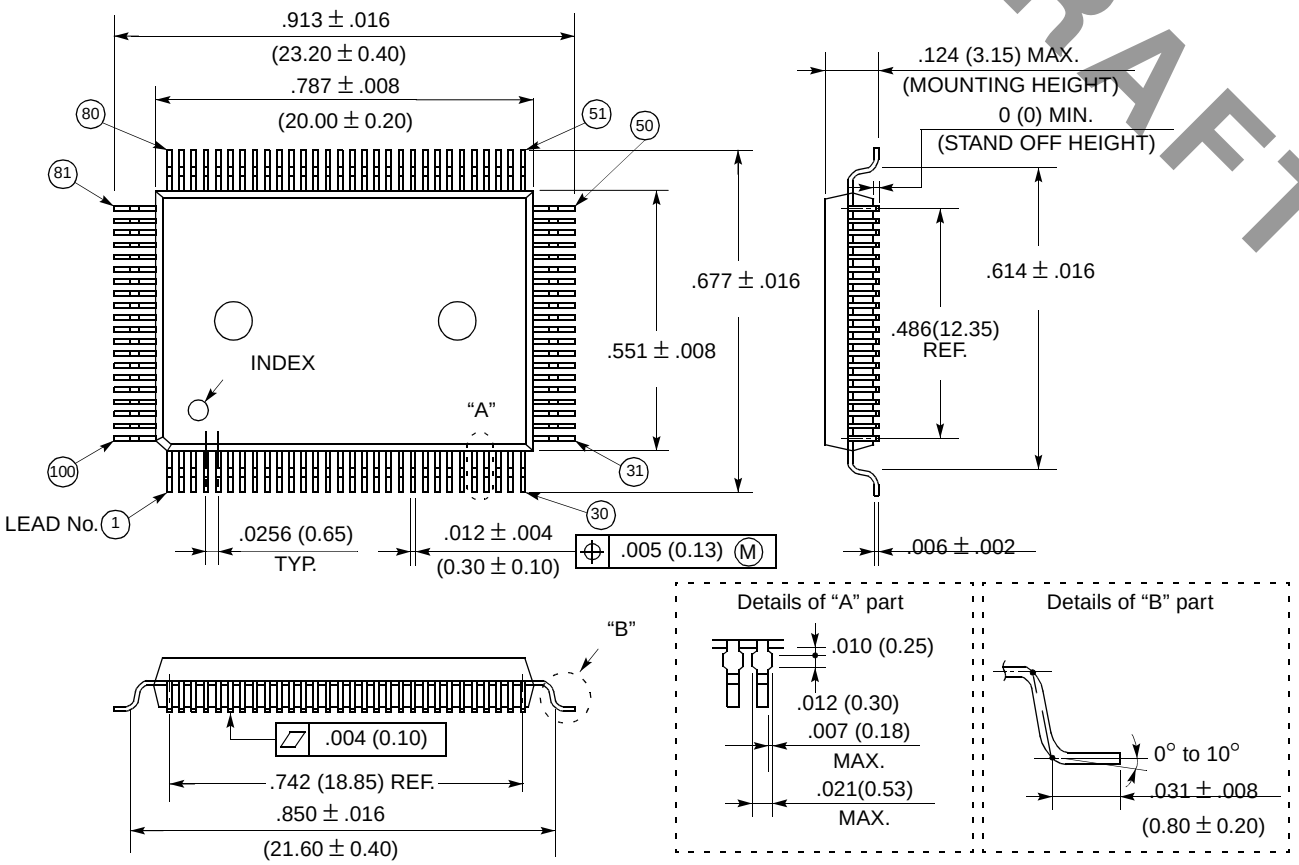


Note: The Mode Register Set command (MRS) should be only asserted after all banks have been precharged.

■ PACKAGE DIMENSIONS

(Suffix: -PQ)

100-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-100P-M15)



Dimensions in inches (millimeters)

* This dimension is being changed.

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