CIRRUS LOGIC®

CL-CD1284

Preliminary Product Bulletin

FEATURES

Parallel Port

High-speed, bidirectional, multi-protocol parallel port:

- **Hardware implementation of all modes of the IEEE STD 1284 specification:**
  - — EPP (Enhanced Parallel Port) mode
  - — ECP (Extended Capabilities Port) mode with run-length encoding/decoding
  - — Reverse Byte mode
  - — Reverse Nibble mode
  - — Centronics®-compatible mode
  - — Up to 2-Mbyte/sec. transfer rate in ECP and EPP modes
- **64-byte FIFO**
- **Supports peripheral-side operation**
- **Data and control input/output pads support IEEE 1284 level-2 interface specifications**

Two Serial UARTS

Serial channel asynchronous protocol support to 115.2 kbps. Register-set-compatible and functionally identical to CL-CD1400:

- **Twelve-byte FIFOs for each transmitter and receiver with programmable threshold for receive FIFO interrupt generation**
- **Improved interrupt schemes: Good Data™ interrupts eliminate the need for character status check**
- **User-programmable and automatic flow control for serial channels**
- **Special character recognition and generation**

(cont.)

IEEE 1284-Compatible Parallel Interface with Two CL-CD1400-Compatible Asynchronous Serial Ports

OVERVIEW

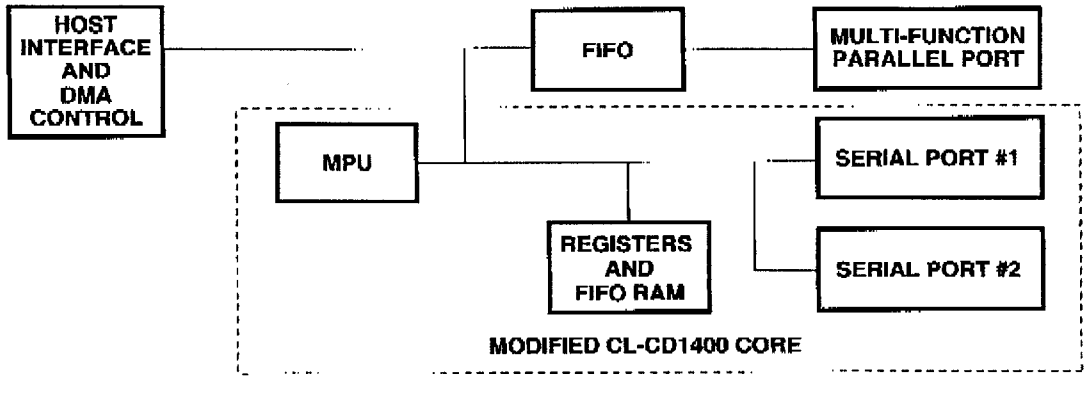
The CL-CD1284 is a multi-function interface controller ideal for printer/scanner applications that implements a high-speed, multi-protocol parallel port and two asynchronous serial ports. In addition, the CL-CD1284 has both programmed-I/O and DMA (direct memory access) operation (parallel port only), providing flexibility in host interface design and high-speed data transfers between the device and host memory.

The parallel port implements all modes of the IEEE STD 1284 standard signaling method for bidirectional parallel peripheral interface specification including: EPP, ECP, reverse byte, reverse nibble, and compatible. Data transfer rates of up to 2 Mbytes/second are achievable on the parallel port when the device is operated at its full rated clock of 25 MHz. This data rate is supported on the host side via a 64-byte FIFO and DMA interface. The parallel-port data and control signals implement the IEEE STD 1284-defined, level-2 interface in symmetrical drive type, current capability (±12 mA), slew rate (0.4 V/ns), and hysteresis (0.8V) (-2.0V to +7.0V protection is not implemented).

The two serial ports implement the standard asynchronous protocol. The serial ports are register-set compatible and functionally identical to the CL-CD1400.

(cont.)

Functional Block Diagram



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FEATURES (cont.)

- **Special character processing, particularly useful for UNIX® environments, optionally handled automatically by the serial channels**
- **Six modem control signals per channel (DTR, DSR, RTS, CTS, CD, and RI)**

General

- **Input clock frequencies at 16 to 25 MHz**
- **DMA handshake to/from parallel port enables fast host transfers (three clocks/per transfer)**
- **Eight general-purpose I/O pins (individual bidirectional programmable at bit level)**
- **DMA supports 16-bit data transfers to/from the parallel port FIFO**
- **Big/little endian architectures supported via the byte-swap input pin (DMA transfers only)**
- **Four separate service request lines — parallel, serial Rx, serial Tx, and serial modem signal change**
- **Advanced CMOS process, packaged in a 100-pin PQFP**

ADVANTAGES

Unique Features	Benefits
Parallel Port —	
■ Supports IEEE STD 1284 specification	❒ Multi-protocol bidirectional port for a wide range of applications. — Up to 2 Mbytes/sec. speed — Provides future connectivity with new host systems
■ 64-byte FIFO	❒ High throughput with reduced host load.
■ Parallel port pads provide level-2 drive characteristics	❒ Direct connection to printer cable, and reduced chip count.
■ DMA channel	❒ Reduced host interface overhead. High-speed data movement between memory and parallel port.
Serial —	
■ Two high-speed CL-CD1400-compatible ports	❒ Serial bit-rates to 115.2 kbps for state-of-the-art async modem requirements. Flexibility of printer interconnect.
■ 12-byte FIFO for transmit and receive	❒ High throughput with reduced host load.
General-Purpose I/O —	
■ Byte-wide, direction programmable port	❒ Added control and status provides flexible system design.

OVERVIEW (cont.)

Theory of Operation

The CL-CD1284 implements an efficient, high-performance communications controller with an on-chip RISC processor that off-loads much of the sending and receiving data tasks from the host processor. The RISC processor employs a high-performance proprietary architecture developed by Cirrus Logic specifically for data-communication applications. This internal CPU executes all instructions in one clock cycle, and uses a window architecture to ensure zero-overhead context switching for each type of internal interrupt. The processor is transparent to the user and does not require any programming. It provides all operations required for moving serial data between the host and the two serial channels, and a flexible host-interrupt interface for the parallel channel. The parallel channel, being separate and having intelligence, is able to provide a very high-speed data interface to the peripheral data port.

The serial channels each consists of separate 12-byte receive and transmit FIFOs, and the parallel channel has a single 64-byte FIFO to support higher speeds on parallel-data ports. The receive FIFOs have programmable thresholds to minimize interrupt latency requirements. The parallel-port FIFO also has a programmable threshold in the transmit direction. The deep FIFOs reduce both the number of interrupt requests made of the host and the time required to service them. The time required to service the requests is reduced by the ability to provide four unique vectors for internal interrupt conditions; thus the host sys-

OVERVIEW (cont.)

tem spends less time determining the source of the interrupt, whether it is a receive, transmit, or modem signal change. The receive interrupt service is further reduced by providing two types of receive vectors, one for Good Data™ and one for 'exception' data. If the receive vector signifies Good Data, the host removes the data from the FIFO without checking status. Exception data (framing error, overrun, break, etc.) will cause an interrupt with a vector that the host can immediately identify and check the status for only those characters.

The CL-CD1284 can also be daisy-chained with other CL-CD1284 or CL-CD1400 devices to implement larger, more complex systems. The Fair Share™ feature assures equal access for service requests across multiple devices.

The parallel channel within the CL-CD1284 implements all protocols defined for the peripheral by the IEEE STD 1284 *Standard Signaling Method for a Bidirectional Parallel Peripheral Interface for Personal Computers*. This specification defines four bidirectional protocols that allow a peripheral device to communicate with a host system (IBM®-PC type) via the parallel printer channel. The modes include Reverse Nibble, Reverse Byte (IBM-PS/2 style), ECP, and EPP (as implemented on the Intel® 80386SL processor). ECP and EPP modes operate at data rates as high as 2 Mbytes/second.

The IEEE 1284 port is implemented as two functional blocks: a data pipeline, which includes the 64-byte FIFO, and the DMA interface (a high-speed state-machine), which controls the parallel port and implements the IEEE 1284 protocols. The internal RISC processor assists the parallel channel by providing interrupt generation and acknowledgment functions, and the data interface to the parallel port registers.

While in ECP mode, the CL-CD1284 provides RLE (Run Length Encoded) data compression in both directions, as defined in the IEEE specification. This data compression is performed automatically if enabled, and is capable of compressing long strings (up to 128 bytes) of identical data into a 2-byte sequence (command/count and data). In printer applications, this greatly reduces data transmission time since bit patterns have large amounts of identical data.

The EPP mode defines a means of sending address and data (much like a processor address and data interface) over the parallel channel. This is used in LAN and SCSI interface adapters in laptop computers.

A possible CL-CD1284 configuration for a laser-printer application is shown below. This example provides a parallel and serial-data interface to a host system or server, and a serial channel for control communication with the printer console.

Configuration Example