Pin Descriptions

The Bt8920 pin locations are shown in Figure 1 and listed in Table 1. The functional pin assignments are listed in Table 2.

Figure 1. Bt8920 Pin Configuration

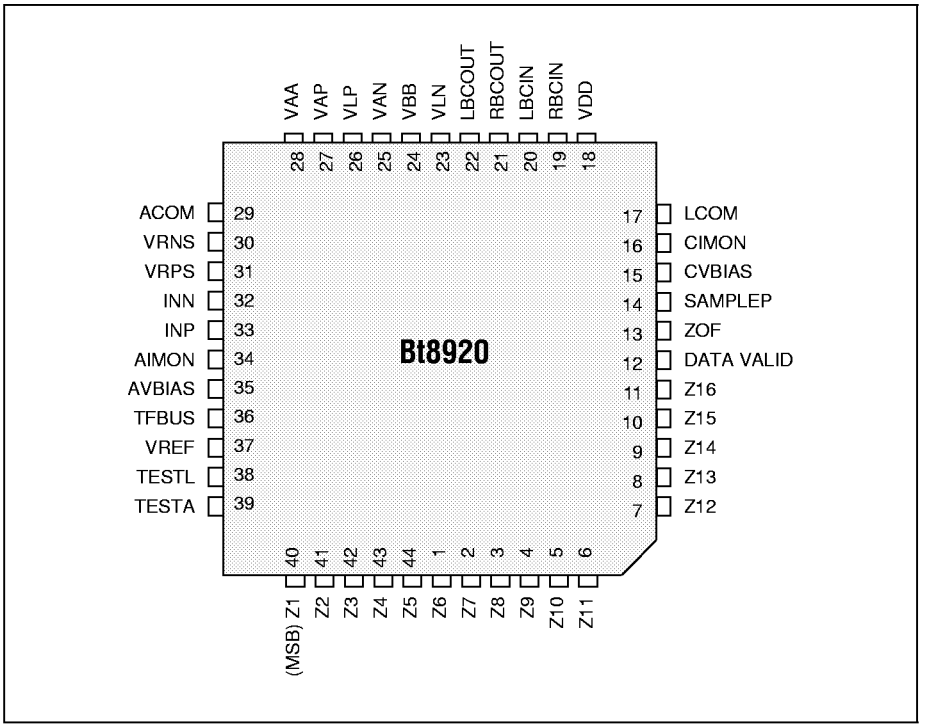


Table 1. Bt8920 Pin Assignments

Pin	Pin Label	I/O[1]	Pin	Pin Label	I/O[1]	Pin	Pin Label	I/O[1]
1	Z6	O	16	CIMON	A	31	VRPS	O
2	Z7	O	17	LCOM	P	32	INN	A
3	Z8	O	18	VDD	P	33	INP	A
4	Z9	O	19	RBCIN	A	34	AIMON	A
5	Z10	O	20	LBCIN	A	35	AVBIAS	A
6	Z11	O	21	RBCOUT	A	36	TFBUS	O
7	Z12	O	22	LBCOUT	A	37	VREF	A
8	Z13	O	23	VLN	P	38	TESTL	I
9	Z14	O	24	VBB	P	39	TESTA	I
10	Z15	O	25	VAN	P	40	Z1 (MSB)	O
11	Z16	O	26	VLP	P	41	Z2	O
12	DATA VALID	O	27	VAP	P	42	Z3	O
13	ZOF	O	28	VAA	P	43	Z4	O
14	SAMPLEP	I	29	ACOM	P	44	Z5	O
15	CVBIAS	A	30	VRNS	O			

1. The coding used in the I/O column is A: analog function, O: output, I: input, and P: power or ground.

Table 2. Hardware Signal Definitions (1 of 2)

Pin Label	Signal Name	I/O[1]	Definition
Z1:16	Digital Output Data	O	16-bit data bus. Z1 = MSB.
ZOF	Digital Data Output	O	ADC overflow/underflow bit.
DATA VALID	Digital Data Output	O	End of conversion bit. Conversion ends on rising edge.
SAMPLEP	Digital Convert Clock	I	ADC clock signal. Conversion starts on falling edge.
VDD	Digital Supply	P	Logic power supply.
LCOM	Digital Ground	P	Logic ground.
RBCIN	Charge Pump	A	A 2.2 µF capacitor should be connected between the RBCIN and RBCOUT pins.
LBCIN	Charge Pump	A	A 2.2 µF capacitor should be connected between the LBCIN and LBCOUT pins.
RBCOUT	Charge Pump	A	A 2.2 µF capacitor should be connected between the RBCIN and RBCOUT pins.
LBCOUT	Charge Pump	A	A 2.2 µF capacitor should be connected between the LBCIN and LBCOUT pins.
VLN	Digital Bypass Low	P	Negative logic supply bypass. A 6.8 µF capacitor in parallel with a 0.1 µF capacitor to LCOM should be used to decouple this pin.

1. The coding used in the I/O column is A: analog function, O: output, I: input, and P: power or ground.

Table 2. Hardware Signal Definitions *(2 of 2)*

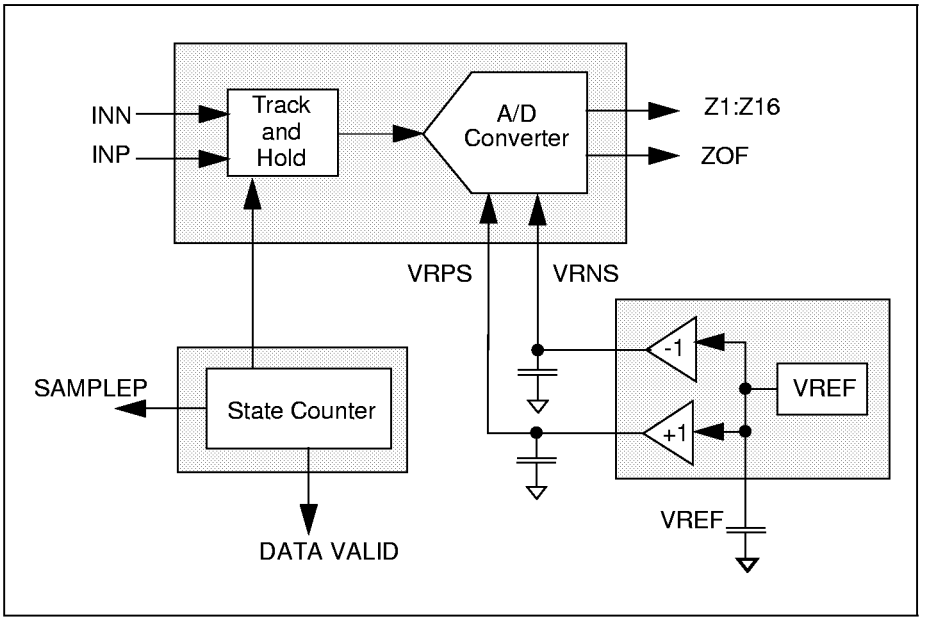
Pin Label	Signal Name	I/O[1]	Definition
VBB	Substrate	P	This pin should be connected to VAN.
VAN	Analog Bypass Low	P	Negative analog supply bypass. A 6.8 µF capacitor in parallel with a 0.1 µF capacitor to ACOM should be used to decouple this pin. This pin should be isolated from VLN by a 5 Ω resistor.
VLP	Digital Bypass High	P	Positive logic supply bypass. A 6.8 µF capacitor in parallel with a 0.1 µF capacitor to LCOM should be used to decouple this pin.
VAP	Analog Bypass High	P	Positive analog supply bypass. A 6.8 µF capacitor in parallel with a 0.1 µF capacitor to ACOM should be used to decouple this pin. This pin should be isolated from VLP by a 5 Ω resistor.
VAA	Analog Supply	P	A 6.8 µF capacitor in parallel with a 0.1 µF capacitor to ACOM should be used to decouple this pin. This pin should be isolated from VDD by a 5 Ω resistor.
ACOM	Analog ground	P	Analog ground.
VRNS	Negative Reference Bypass	O	Flash bypass. A 6.8 µF capacitor in parallel with a 0.1 µF capacitor to ACOM should be used to decouple the end of the flash resistor.
VRPS	Positive Reference Bypass	O	Flash bypass. A 6.8 µF capacitor in parallel with a 0.1 µF capacitor to ACOM should be used to decouple the end of the flash resistor.
INN	Analog Signal Negative	A	Analog input. INN is the input ground reference.
INP	Analog Signal Positive	A	Analog input. INP is the analog data signal input.
AIMON	Amplifier Current Resistor	A	Current monitor resistor. AIMON = 47 kΩ connected to ACOM.
CIMON	Convert Timing Resistor	A	Current monitor resistor. CIMON = 98 kΩ for E1, 120 KΩ for T1, connected to ACOM
AVBIAS	Analog Bias Decoupling	A	Bias decoupling. A 0.1 µF capacitor should be connected from this pin to ACOM.
CVBIAS	Convert Timing Bias Decoupling	A	Bias decoupling. A 0.1 µF capacitor should be connected from this pin to ACOM.
TFBUS	Factory Test Pin	O	Test pin. This pin should be left unconnected.
VREF	Voltage Reference	A	Voltage reference decoupling. This is a low current pin not intended to drive external circuits.
TESTA	Factory Test Pin	I	This pin should be connected LCOM.
TESTL	Factory Test Pin	I	This pin should be connected LCOM.

1. The coding used in the I/O column is A: analog function, O: output, I: input, and P: power or ground.

Functional Description

A block diagram for the Bt8920 is shown in Figure 2.

Figure 2. Bt8920 Block Diagram



The SAMPLEP pin initializes the ADC and starts the conversion cycle. The analog input is fed to an on-chip track and hold (T/H) which holds the analog signal on the falling edge of SAMPLEP. DATA VALID goes low at the commencement of the conversion cycle, and goes high when the conversion is complete. The digital data is then output. The T/H goes into the track mode as soon as DATA VALID goes high. The output of the ADC is offset binary (see Table 3 below). All internal supplies and references are derived from an externally supplied +5V and GND.

Table 3. Bt8920 Digital Output Code

Analog Input	Digital Code
+VRPS	1111 1111 1111 1111
VCEN	1000 0000 0000 0000
–VRNS	0000 0000 0000 0000

Applications

The Bt8920 is primarily intended for use in communications. Figure 3 shows a typical configuration for use with the Bt8952 and Bt8953 in an HDSL application.

Some important layout considerations are required to obtain the maximum performance from the Bt8920 (see Figure 4). Due to the high resolution of the part, and the combination of on-board power supply and reference generation, adequate power supply decoupling is essential. It is recommended that all the power pins be decoupled by a 6.8 µF tantalum capacitor in parallel with a 0.1 µF ceramic capacitor. The on-board analog power supplies, VAP and VAN, should be isolated from their digital counterparts, VLP and VLN, by a small series resistor of nominally 5 Ω. Also the analog power supply VAA should be isolated from VDD by a 5 Ω resistor. To minimize digital cross talk to the analog signal, it is recommended that separate ground planes be used for ACOM and LCOM. A short connection between the two ground planes should be made under the Bt8920 connecting the ACOM pin directly to the LCOM pin, thus ensuring there are no DC offsets between the two grounds.

Figure 3. Typical HDSL Two-Pair System

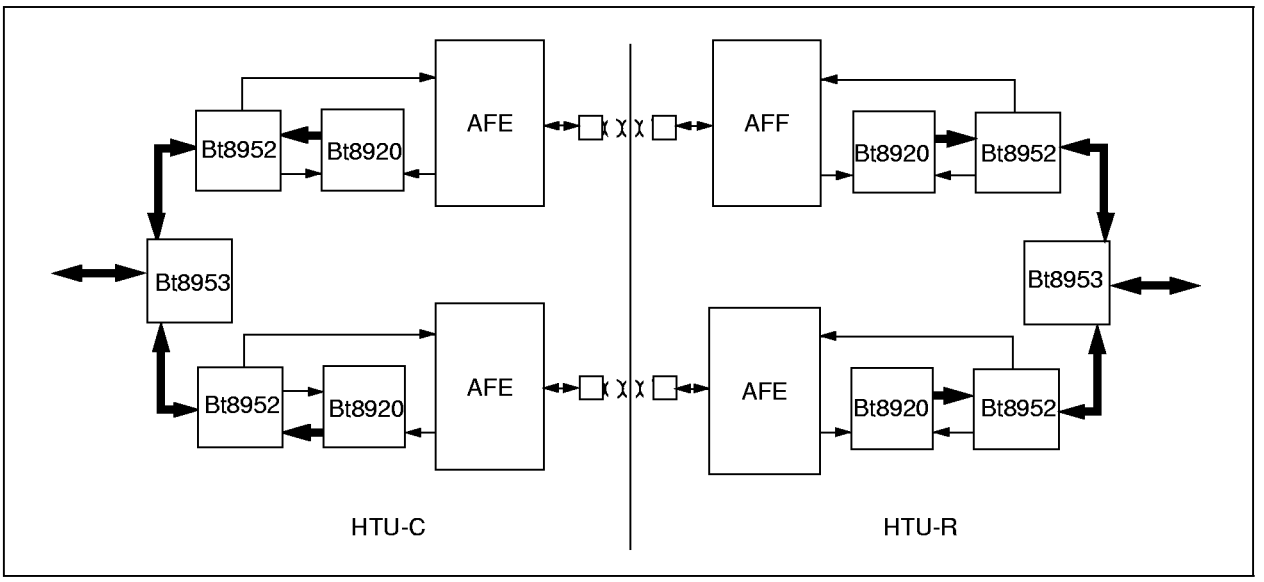
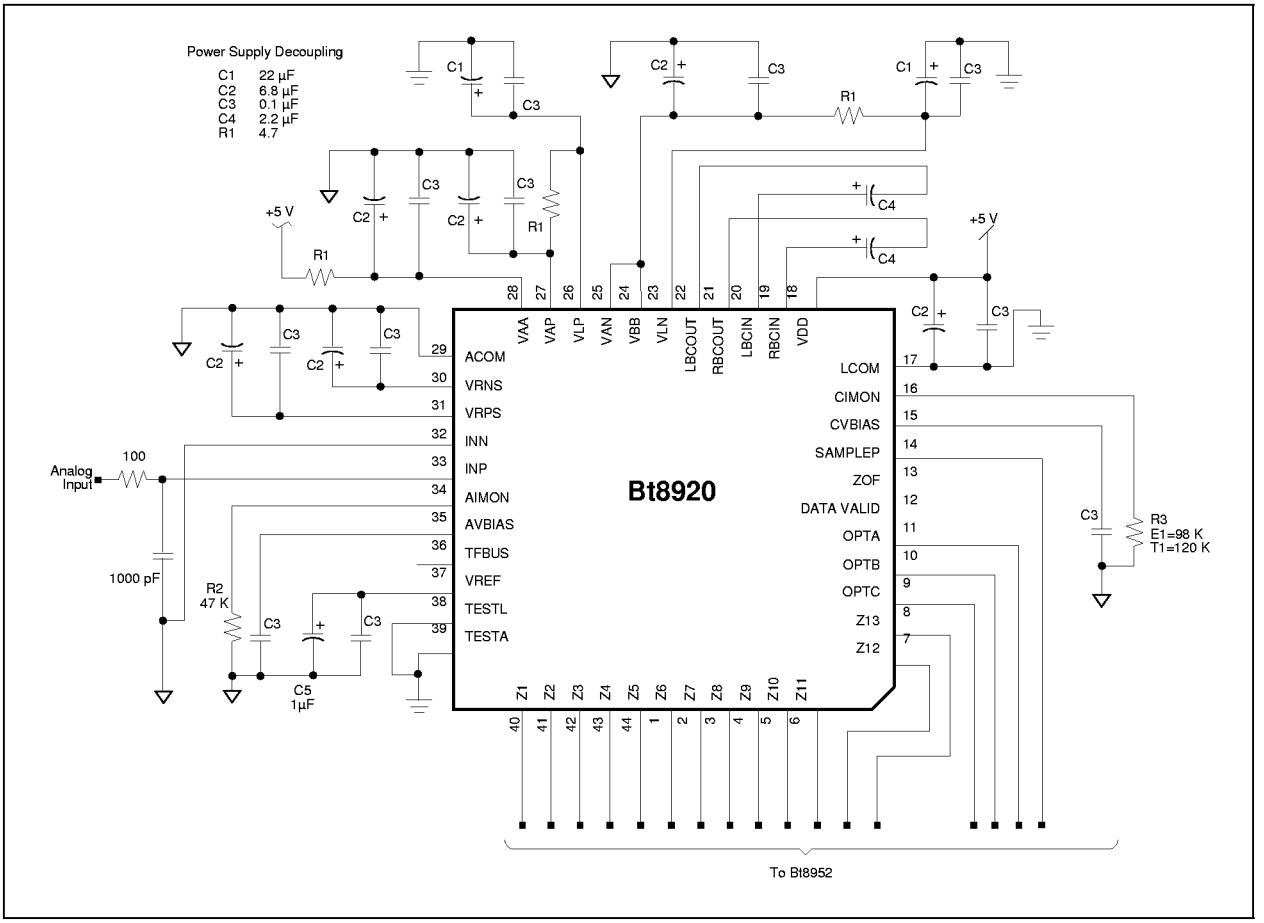


Figure 4. Bt8920 Decoupling



The output of the reference generator, VREF, has minimal drive capability and should not be used without buffering as a reference for any external circuits. A 1 µF tantalum capacitor in parallel with a 0.1 µF ceramic capacitor should be used to decouple this pin.

Due to the nature of the analog input, it is desirable to isolate it from the preceding analog stage. This can be accomplished with a simple RC filter of 100 Ω and 1000 pF in series with the analog input.

The current control resistor, CIMON, controls the speed of conversion. To obtain optimum performance this resistor should be set to the recommended value (121 kΩ for 400 ksps, 97.6 kΩ for 600 ksps).

Electrical and Mechanical Specifications

Absolute Maximum Ratings

Table 4. Bt8920 Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage	V_{AA}/V_{DD}	–0.3 to +7.0	V
Digital Input Voltage	V_{IH}/V_{IL}	–0.5 to VDD +0.5	V
Analog Input Voltage		±3.0	V
Operating Temperature	T_A	–40 to +85	°C
Storage Temperature	T_{STG}	–55 to +150	°C
Vapor Phase Soldering	T_{VSOL}	220	°C
Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.			

Recommended Operating Conditions

Table 5. Bt8920 Recommended Operating Ratings

Parameter	Symbol	Min	Typ	Max	Symbol
Power Supply	V_{AA}/V_{DD}	4.75	5	5.25	V
Analog Signal Input	INP INN	V_{RNS} –10	 0	V_{RPS} +10	V mV
Ambient Operating Temperature	T_A	–40		+85	°C

DC Characteristics

Table 6. Bt8920 DC Specification

Parameter	Symbol	Min	Typ	Max	Units
A/D Resolution		16			Bits
A/D Accuracy					
Integral Linearity	IL			±1.0	LSB@ 13 bits
Differential Linearity	DL			±0.8	LSB@ 13 bits
Gain Error				tbd	dB
Analog Input					
DC Input Impedance	R_{IN}		100		MΩ
Input Capacitance	C_{IN}		80		pF
Voltage Reference Outputs					
Reference Voltage	V_{REF}	1.65	1.75	1.90	V
Positive Reference Bypass	V_{RPS}	1.65		1.90	V
Negative Reference Bypass	V_{RNS}	–1.90		–1.65	V
Mid Range Voltage	V_{CEN}	tbd	0	tbd	V
Analog Bypass High	V_{AP}		2.9		V
Analog Bypass Low	V_{AN}		–2.9		V
Digital Bypass High	V_{LP}		2.9		V
Digital Bypass Low	V_{LN}		–2.9		V
Substrate Bypass	V_{BB}		–2.9		V
Digital Input					
Input High Voltage	V_{IH}	$0.8xV_{DD}$			V
Input Low Voltage	V_{IL}			$0.2xV_{DD}$	V
Input High Leakage	I_{IH}		1.0		µA
Input Low Leakage	I_{IL}		–1.0		µA
Input Capacitance	C_{IN}		3		pF
Digital Outputs					
Output High Voltage (IOH = –400 µA)	V_{OH}	V_{DD}–0.8			V
Output Low Voltage IOL = 400 µA)	V_{OL}			0.4	V
Power Supply Current	I			60	mA
Power Dissipation			250		mW

AC Characteristics

Table 7. Bt8920 AC Specifications

		Bt8920EPJ (400 ksps)			Bt8920EPJ600 (600 ksps)			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Peak Harmonic or Spurious Content F_{in} = 1 kHz –10 dB[1] F_{in} = Fs/2 kHz –10 dB[1]				 –75 –58			 –75 –58	 dB dB
Total Harmonic Distortion F_{in} = 1 kHz –10 dB[1]	THD			0.02			0.02	%
Signal to Noise plus Distortion F_{in} = 1 kHz, –10 dB[1] F_{in} = 1 kHz, –40 dB[1]	 SINAD SINAD	 70 40			 70 38			 dB dB
1. Referenced to full scale and tested at Max sample rate.								

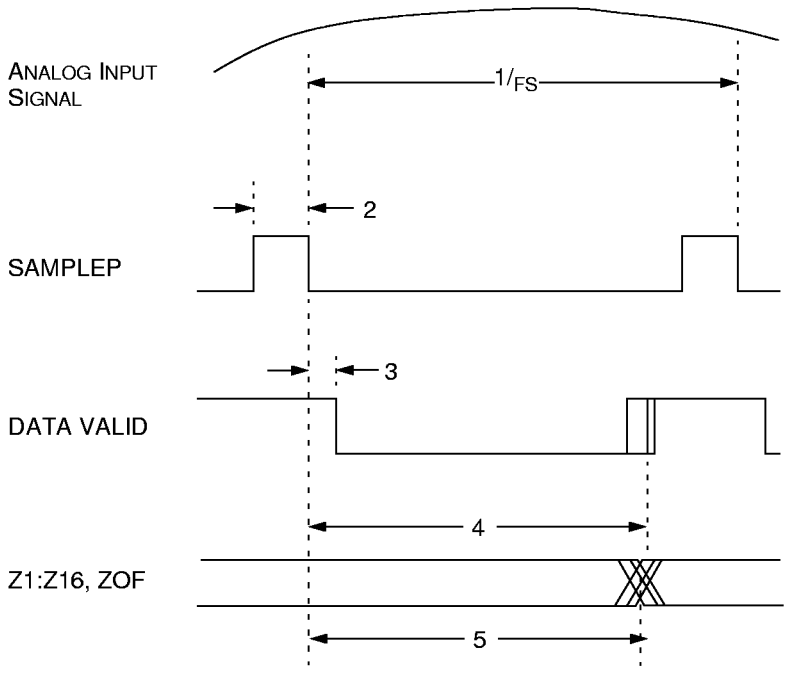
Switching Characteristics

Table 8. ADC Timing Specifications

			Bt8920EPJ (400 ksps)[1]			Bt8920EPJ600 (600 ksps)[1]			
%	Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Units
1	Conversion Rate	Fs			392			584	ksps
2	SAMPLEP Pulse Width High	$tpw(H)_{SP}$	100		200	100		160	ns
3	SAMPLEP Low to Data Valid Low	t_P		60			60		ns
4	Convert Time	t_C	1.0		2.3	1.0		1.6	µs
5	SAMPLEP Low to Data Out	t_D	1.0		2.2	1.0		1.5	µs
	Aperture Jitter	t_{AJ}		10			10		ps

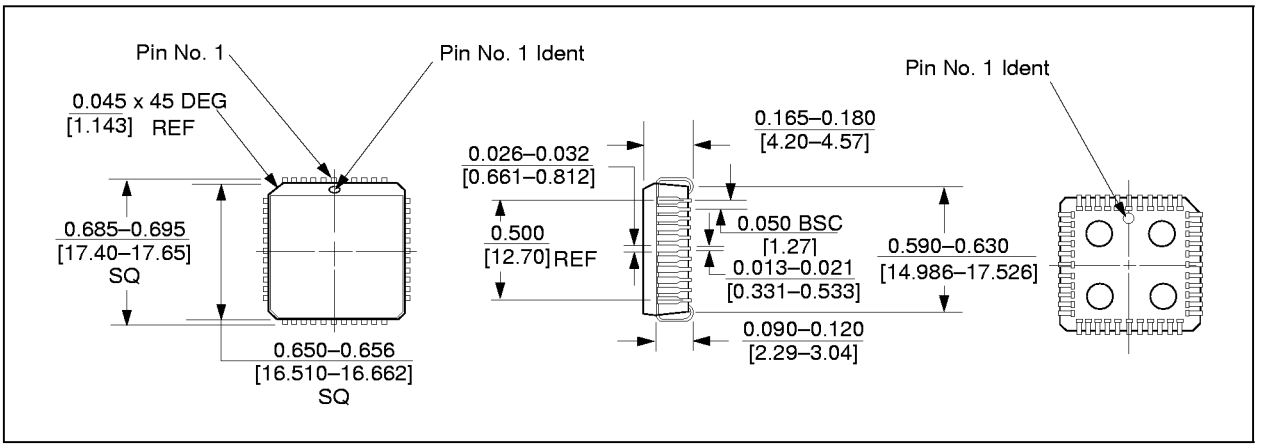
1. For 400 ksps timing AIMON = 47 kΩ, CIMON = 121 kΩ (1%)
   For 600 ksps timing AIMON = 47 kΩ, CIMON = 97.6 kΩ (1%)

Figure 5. ADC Timing



Package Drawing

Figure 6. 44-Pin Plastic J-Lead (PLCC)



Notes—Unless otherwise specified:

1. Dimensions are in inches [milimeters]
2. Controlled dimensions are in inches