# Electrical Specifications

## 65548 ABSOLUTE MAXIMUM CONDITIONS

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $P_D$ | Power Dissipation | – | – | 1.8 | W |
| $V_{CC}$ | Supply Voltage | –0.5 | – | 7.0 | V |
| $V_I$ | InputVoltage | –0.5 | – | $V_{CC}$+0.5 | V |
| $V_O$ | OutputVoltage | –0.5 | – | $V_{CC}$+0.5 | V |
| $T_{STG}$ | StorageTemperature | –40 | – | 125 | ° C |

**Note:** Permanent device damage may occur if Absolute Maximum Ratings are exceeded.
Functional operation should be restricted to the conditions described under Normal Operating Conditions.

## 65548 NORMAL OPERATING CONDITIONS

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage**(for5Voperation)** | 4.5 | 5 | 5.5 | V |
| $V_{CC}$ | Supply Voltage**(for3.3Voperation)** | 3.1 | 3.3 | 3.6 | V |
| $T_A$ | AmbientTemperature | 0 | – | 70 | ° C |

## 65548 DAC CHARACTERISTICS

(Under Normal Operating Conditions Unless Noted Otherwise)

| Symbol | Parameter | Notes | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_O$ | OutputVoltage | Io ≤ 10 mA | 1.5 | – | – | V |
| $I_O$ | Output Current | Vo ≤ 1V @ 37.5Ω Load | 21 | – | – | mA |
| | Full Scale Error | | – | – | ± 5 | % |
| | DAC to DAC Correlation | | – | 1.27 | – | % |
| | DACLinearity | | ± 2 | – | – | LSB |
| | Full Scale Settling Time | | – | – | 28 | nS |
| | Rise Time | 10% to 90% | – | – | 6 | nS |
| | Glitch Energy | | – | – | 200 | pVsec |
| | ComparatorSensitivity | | – | 50 | – | mV |

**Note:** Unless otherwise specified, specifications above apply to both 5V & 3.3V operation & memory clock is assumed to be 75MHz.
Electrical specifications contained herein are preliminary and subject to change without notice.

## 65548 DC CHARACTERISTICS

(Under Normal Operating Conditions Unless Noted Otherwise)

| Symbol | Parameter | Notes | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{CCE5}$ | Power Supply Current | 0° C, **5.5V**, MCLK=75 MHz, DAC on †† | – | TBD | TBD | mA |
| $I_{CCO5}$ | Power Supply Current | 0° C, **5.5V**, MCLK=75 MHz, DAC off †† | – | TBD | TBD | mA |
| $I_{CCE3}$ | Power Supply Current | 0° C, **3.3V**, MCLK=75 MHz, DAC on †† | – | TBD | TBD | mA |
| $I_{CCO3}$ | Power Supply Current | 0° C, **3.3V**, MCLK=75 MHz, DAC off †† | – | TBD | TBD | mA |
| $I_{CCSD}$ | Power Supply Current | 0° C, **3.3V**, Standby, SelfRefresh DRAMs† | – | TBD | TBD | µA |
| $I_{CCSS}$ | Power Supply Current | 0° C, **3.3V**, Standby, SlowRfsh 32KHZ in | – | TBD | TBD | µA |
| $I_{CCSR}$ | Power Supply Current | 0° C, **3.3V**, Standby, SlowRfsh XTALI in | – | TBD | TBD | µA |
| $I_{IL}$ | Input Leakage Current | | –100 | – | +100 | uA |
| $I_{OZ}$ | Output Leakage Current | High Impedance | –100 | – | +100 | uA |
| $V_{IL}$ | Input Low Voltage | All input pins | –0.5 | – | 0.8 | V |
| $V_{IH}$ | Input High Voltage | All input pins | 2.0 | – | $V_{CC}$+0.5 | V |
| $V_{THR}$ | Input Switch Point | All inputs except RESET# & STNDBY# | – | 1.4 | – | V |
| $V_{HYS}$ | Input Hysteresis | RESET# and STNDBY# | – | ± 0.15 | – | V |
| $V_{OL5}$ | Output Low Voltage | Under max load per table below **(5V)** | – | – | 0.5 | V |
| $V_{OL3}$ | Output Low Voltage | Under max load per table below **(3.3V)** | – | – | 0.5 | V |
| $V_{OH5}$ | Output High Voltage | Under max load per table below **(5V)** | 2.4 | – | – | V |
| $V_{OH3}$ | Output High Voltage | Under max load per table below **(3.3V)** | 0.7 x Vcc | – | – | V |

## 65548 DC DRIVE CHARACTERISTICS

(Under Normal Operating Conditions Unless Noted Otherwise)

| Symbol | Parameter | Output Pins | DC Test Conditions | Min | Units |
|---|---|---|---|---|---|
| $I_{OL}$ | Output Low Drive | H/VSYNC, LDEV#, LRDY#, ROMCS# | $V_{OUT}=V_{OL}$, see note††† | 12 | mA |
| | | FLM, LP, M, P0-15, SHFCLK, D0-31 | $V_{OUT}=V_{OL}$, see note††† | 8 | mA |
| | | ENAVEE, ENAVDD, ENABKL, ACTI | $V_{OUT}=V_{OL}$, see note††† | 8 | mA |
| | | RASA#, CASAH/L#, WEA#, PAR, BLANK# | $V_{OUT}=V_{OL}$, see note††† | 4 | mA |
| | | RASB#, CASBH/L#, WEB#, OEAB#, AA0-9 | $V_{OUT}=V_{OL}$, see note††† | 4 | mA |
| | | RASC#, CASCH/L#, WEC#, OEC#, CA0-8 | $V_{OUT}=V_{OL}$, see note††† | 4 | mA |
| | | All other outputs | $V_{OUT}=V_{OL}$, see note††† | 2 | mA |
| $I_{OH}$ | Output High Drive | H/VSYNC, LDEV#, LRDY#, ROMCS# | $V_{OUT}=V_{OH}$, see note††† | 12 | mA |
| | | FLM, LP, M, P0-15, SHFCLK, D0-31 | $V_{OUT}=V_{OH}$, see note††† | 8 | mA |
| | | ENAVEE, ENAVDD, ENABKL, ACTI | $V_{OUT}=V_{OH}$, see note††† | 8 | mA |
| | | RASA#, CASAH/L#, WEA#, PAR, BLANK# | $V_{OUT}=V_{OH}$, see note††† | 4 | mA |
| | | RASB#, CASBH/L#, WEB#, OEAB#, AA0-9 | $V_{OUT}=V_{OH}$, see note††† | 4 | mA |
| | | RASC#, CASCH/L#, WEC#, OEC#, CA0-8 | $V_{OUT}=V_{OH}$, see note††† | 4 | mA |
| | | All other outputs | $V_{OUT}=V_{OH}$, see note††† | 2 | mA |

**Note:** †Measured with all chip inputs driven to inactive levels and outputs not connected (or connected to typical external loads).

**Note:** ††640x480x8bpp, TFT panel (for power data for other configurations, contact Chips and Technologies in San Jose, California)

**Note:** †††IOL & IOH drive listed above indicates 5V low drive (Vcc=4.5V) and 3.3V high drive (Vcc=3V), as programmed via XR6C bits 2-5.

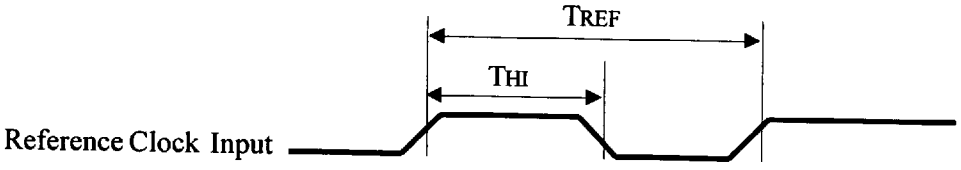
**Note:** Unless otherwise specified, specifications above apply to both 5V & 3.3V operation & memory clock is assumed to be 75MHz. Electrical specifications contained herein are preliminary and subject to change without notice.

## 65548 OUTPUT DRIVE CAPACITY

**Note:** Please refer to Pin List section for the drive capacity and maximum output load of individual pins. See pages 27-31.

## 65548 AC TIMING CHARACTERISTICS - REFERENCE CLOCK

| Symbol | Parameter | Notes | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $T_{REF}$ | Reference Frequency | (±100 ppm) | – | 14.31818 | – | MHz |
| $T_{REF}$ | Reference Clock Period | $1/F_{REF}$ | – | 69.84128 | – | nS |
| $T_{HI}/T_{REF}$ | Reference Clock Duty Cycle | | 25 | – | 75 | % |

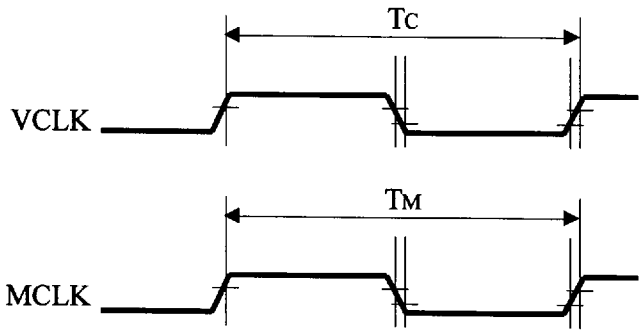



**Reference Clock Timing**

**Note:** Unless otherwise specified, specifications above apply to both 5V & 3.3V operation & memory clock is assumed to be 75MHz. Electrical specifications contained herein are preliminary and subject to change without notice.

## 65548 AC TIMING CHARACTERISTICS - CLOCK GENERATOR

| Symbol | Parameter | Notes | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $T_C$ | VCLK Period **(5V)** | 80 MHz | 12.5 | – | – | nS |
| $T_C$ | VCLK Period **(3.3V)** | 80 MHz | 12.5 | – | – | nS |
| $T_M$ | MCLK Period **(5V)** | 75 MHz | 13.33 | – | – | nS |
| $T_M$ | MCLK Period **(3.3V)** | 75 MHz | 13.33 | – | – | nS |




**Clock Timing**

**Note:** Unless otherwise specified, specifications above apply to both 5V & 3.3V operation & memory clock is assumed to be 75MHz. Electrical specifications contained herein are preliminary and subject to change without notice.

## 65548 AC TIMING CHARACTERISTICS - RESET

| Symbol | Parameter | Notes | Min | Max | Units |
|---|---|---|---|---|---|
| $T_{IPR}$ | Reset Active Time from Power Stable | See Note 1 | 5 | – | mS |
| $T_{ORS}$ | Reset Active Time from Ext. Osc. Stable | See Note 2 | – | – | – |
| $T_{RES}$ | Reset Active Time with Power Stable | See Note 3 | 2 | – | mS |
| $T_{STR}$ | Reset Active Time from Standby | See Note 4 | 2 | – | mS |
| $T_{RSR}$ | Reset Rise Time | Reset fall time is non-critical | – | 20 | nS |
| $T_{RSO}$ | Reset Active to Output Float Delay | | – | 40 | nS |
| $T_{CSU}$ | Configuration Setup Time | See Note 5 | 20 | – | nS |
| $T_{CHD}$ | Configuration Hold Time | | 5 | – | nS |

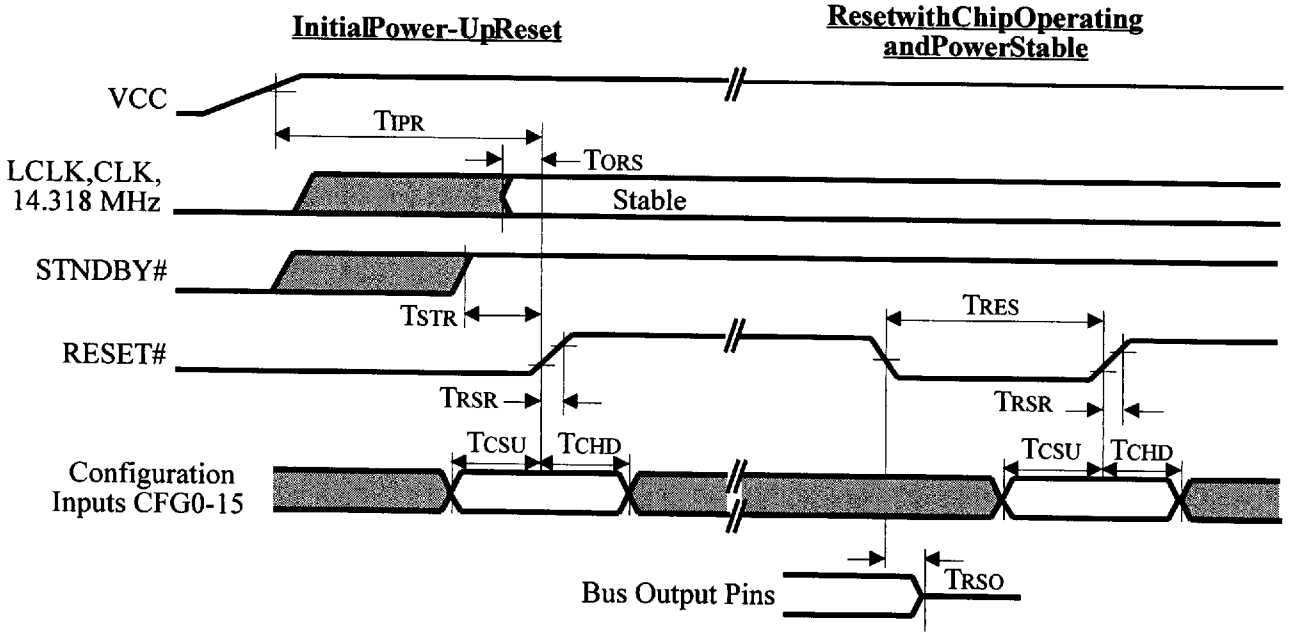
Note 1: This parameter includes time for internal voltage stabilization of all sections of the chip, startup and stabilization of the internal clock synthesizer, and setting of all internal logic to a known state.

Note 2: The external oscillator input is required. LCLK in Local Bus and CLK in PCI Bus modes should have the normal operating frequency during reset. The 65548 should see a minimum of 10 clocks before the inactive edge of Reset#.

Note 3: This parameter includes time for the internal clock synthesizer to reset to its default frequency and time to set all internal logic to a known state. It assumes power is stable and the internal clock synthesizer is already operating at some stable frequency.

Note 4: STNDBY# pin must be high when RESET occurs to properly reset the chip. On the other hand, RESET# can be pulled low during Standby mode without affecting Standby mode.

Note 5: Setup time to latch the state of the configuration bits reliably into XR01, XR6C, and XR74 is specified by this parameter. Changes in some configuration bits may take longer to stabilize inside the chip (such as internal clock synthesizer-related bits 4 and 5). It is therefore recommended that configuration bit setup time be TRES (2mS) to insure that the chip is in a completely stable state when Reset goes inactive.




**Reset Timing**

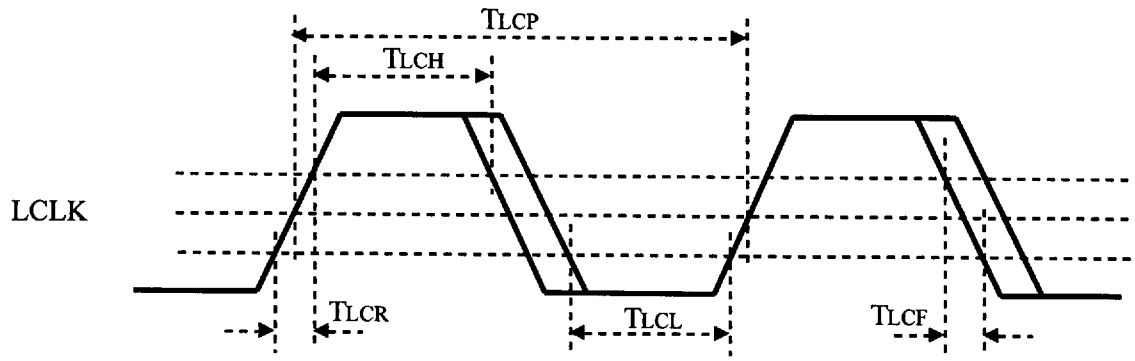
**Note:** Unless otherwise specified, specifications above apply to both 5V & 3.3V operation & memory clock is assumed to be 75MHz. Electrical specifications contained herein are preliminary and subject to change without notice.

## 65548 AC TIMING CHARACTERISTICS - LOCAL BUS CLOCK (40 MHz)

| Symbol | Parameter | Notes | Min | Max | Units |
|---|---|---|---|---|---|
| $T_{LCP}$ | Local Bus Clock Period **(40MHz)†** | 0.1% stability at 2.0V / 0.8V | 25 | 25 | nS |
| $T_{LCH}$ | Local Bus Clock High Time | | 8 | – | nS |
| $T_{LCL}$ | Local Bus Clock Low Time | | 8 | – | nS |
| $T_{LCR}$ | Local Bus Clock Rise Time | | – | 2 | nS |
| $T_{LCF}$ | Local Bus Clock Fall Time | | – | 2 | nS |
| — | Local Bus Clock Slew Rate | | 1 | 4 | **V / nS** |
| $T_{CRS}$ | CPU Reset Setup Time to Local Bus Clock | For 2x Clock Sync | 2 | – | nS |
| $T_{CRH}$ | CPU Reset Hold Time from Local Bus Clock | For 2x Clock Sync | 5 | – | nS |

**Note:** † VL-Bus timing is compatible with VL-Bus Specification 2.0. 50 MHz VL-Bus operation assumes BVCC and IVCC both at 5V. VL-Bus operation at 3.3V is limited to 40 MHz (refer to the VL-Bus 2.0 specification for 33 MHz timing details).

**Note:** The typical input capacitance on LCLK is 10pF.

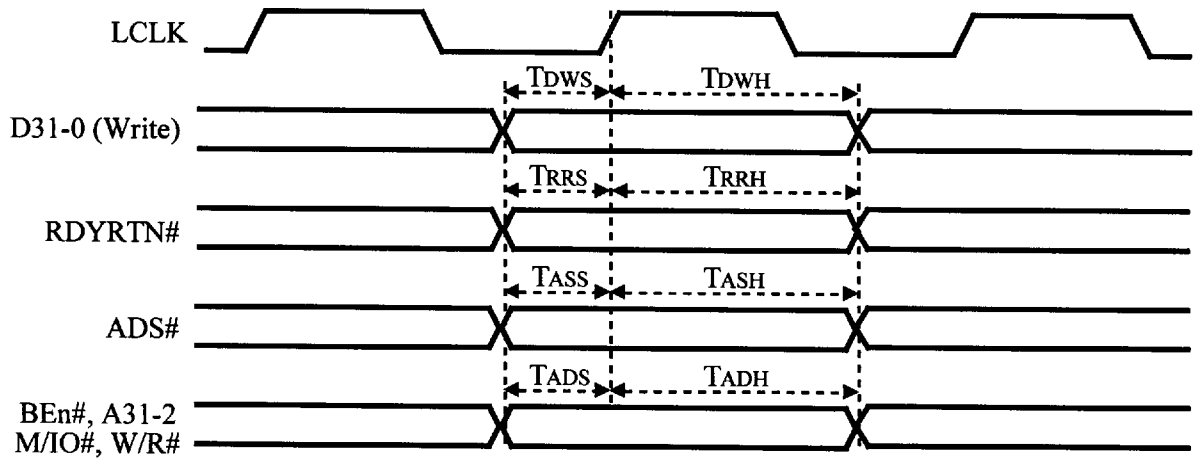



**Local Bus Clock Timing**

**Note:** Unless otherwise specified, specifications above apply to both 5V & 3.3V operation & memory clock is assumed to be 75MHz. Electrical specifications contained herein are preliminary and subject to change without notice.

## 65548 AC TIMING CHARACTERISTICS - LOCAL BUS INPUT SETUP & HOLD (40 MHz)

| Symbol | Parameter | Notes | Min | Max | Units |
|---|---|---|---|---|---|
| $T_{ADS}$ | Setup Time - A2-31,BEn#,M/IO#,W/R# | | 6 | – | nS |
| $T_{ASS}$ | Setup Time - ADS# | | 6 | – | nS |
| $T_{DWS}$ | Setup Time - D0-31 (Write) | | 6 | – | nS |
| $T_{RRS}$ | Setup Time - RDYRTN# | | 5 | – | nS |
| $T_{ADH}$ | Hold Time - A2-31,BEn#,M/IO#,W/R# | | 2 | – | nS |
| $T_{ASH}$ | Hold Time - ADS# | | 2 | – | nS |
| $T_{DWH}$ | Hold Time - D0-31 (Write) | | 2 | – | nS |
| $T_{RRH}$ | Hold Time - RDYRTN# | | 2 | – | nS |

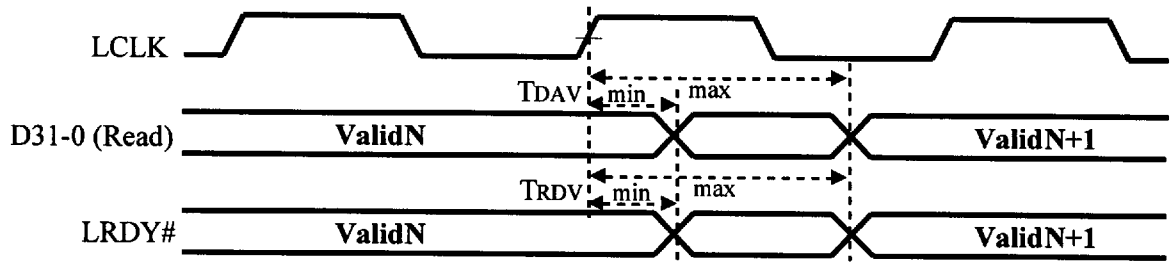



**Local Bus Input Setup & Hold Timing**

**Note:** Unless otherwise specified, specifications above apply to both 5V & 3.3V operation & memory clock is assumed to be 75MHz. Electrical specifications contained herein are preliminary and subject to change without notice.

## 65548 AC TIMING CHARACTERISTICS - LOCAL BUS OUTPUT VALID (40 MHz)

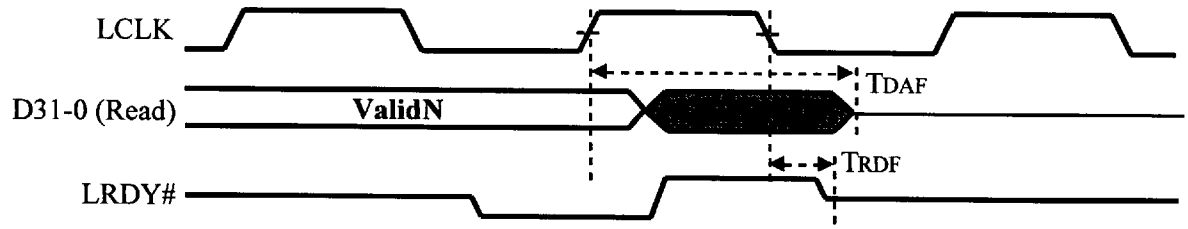
| Symbol | Parameter | Notes | Min | Max | Units |
|---|---|---|---|---|---|
| $T_{DAV}$ | Bus Clock to Output Valid - D0-31 (Read) | | 3 | 14 | nS |
| $T_{RDV}$ | Bus Clock to Output Valid - LRDY# | | 3 | 13 | nS |




**Local Bus Output Valid Timing**

## 65548 AC TIMING CHARACTERISTICS - LOCAL BUS FLOAT DELAY (40 MHz)

| Symbol | Parameter | Notes | Min | Max | Units |
|---|---|---|---|---|---|
| $T_{DAF}$ | Float Delay - D0-31 (Read) | | – | 18 | nS |
| $T_{RDF}$ | Float Delay - LRDY# | Driven high before floating | – | 15 | nS |

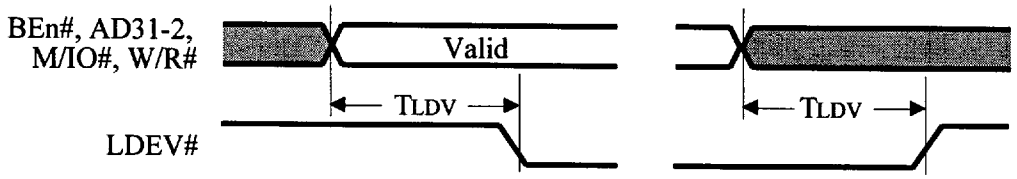



**Local Bus Output Float Delay Timing**

**Note:** Unless otherwise specified, specifications above apply to both 5V & 3.3V operation & memory clock is assumed to be 75MHz. Electrical specifications contained herein are preliminary and subject to change without notice.

## 65548 AC TIMING CHARACTERISTICS - VL BUS LDEV# (40 MHz)

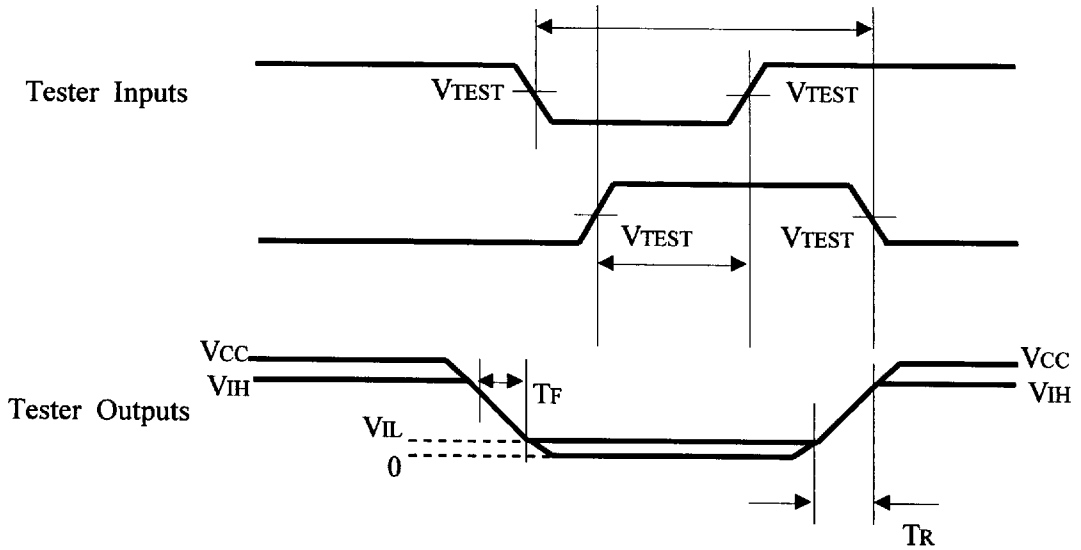
| Symbol | Parameter | Notes | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $T_{LDV}$ | Address to LDEV# change | | 3 | – | 20 | nS |




**VL-Bus LDEV# Timing**

## 65548 AC TEST CONDITIONS

| Symbol | Notes | 3.3 Volt Signaling | 5 Volt Signaling | Units |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 3.1 | 5.5 | V |
| $V_{TEST}$ | All AC parameters | 0.4 $V_{CC}$ | 1.5 | V |
| $V_{IL}$ | Input low voltage (10% of Vcc) | 0.1 $V_{CC}$ (Min) | – | V |
| $V_{IH}$ | Input high voltage (90% of Vcc) | – | 0.9 $V_{CC}$ (Max) | V |
| $T_R$ | Maximum input rise time (3/5.5V) | 3 | 3 | nS |
| $T_F$ | Maximum input fall time (3/5.5V) | 2 | 2 | nS |



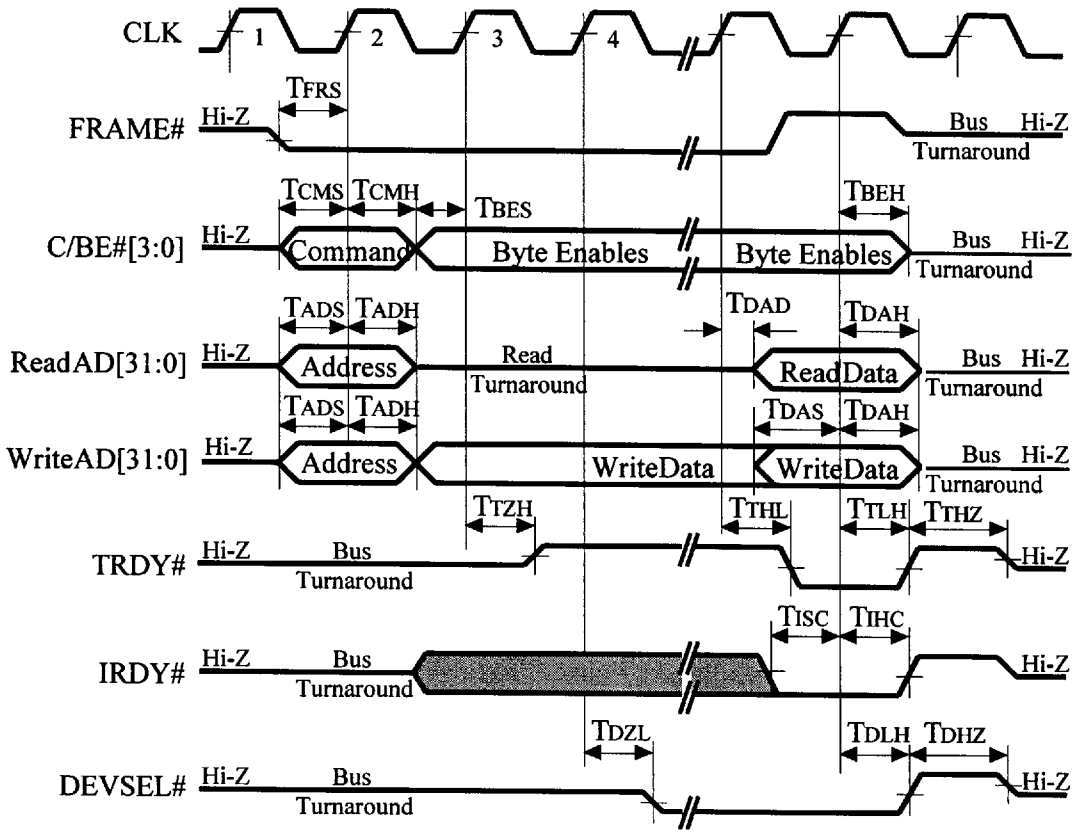

**AC Test Timing**

**Note:** Unless otherwise specified, specifications above apply to both 5V & 3.3V operation & memory clock is assumed to be 75MHz. Electrical specifications contained herein are preliminary and subject to change without notice.

## 65548 AC TIMING CHARACTERISTICS - PCI BUS FRAME (33 MHz)

| Symbol | Parameter | Notes | Min | Max | Units |
|---|---|---|---|---|---|
| $T_{FRS}$ | FRAME# Setup to CLK | | 7 | – | nS |
| $T_{CMS}$ | C/BE#[3:0] (Bus CMD) Setup to CLK | | 7 | – | nS |
| $T_{CMH}$ | C/BE#[31:0] (Bus CMD) Hold from CLK | | 2 | – | nS |
| $T_{BES}$ | C/BE#[3:0] (Byte Enable) Setup to CLK | | 7 | – | nS |
| $T_{BEH}$ | C/BE#[3:0] (Byte Enable) Hold from CLK | | 2 | – | nS |
| $T_{ADS}$ | AD[31:0] (Address) Setup to CLK | | 7 | – | nS |
| $T_{ADH}$ | AD[31:0] (Address) Hold from CLK | | 2 | – | nS |
| $T_{DAS}$ | AD[31:0] (Data) Setup to CLK | | 7 | – | nS |
| $T_{DAH}$ | AD[31:0] (Data) Hold from CLK | | 2 | – | nS |
| $T_{DAD}$ | AD[31:0] (Data) Valid from CLK | | – | 11 | nS |
| $T_{TZH}$ | TRDY# High Z to High from CLK | | – | 11 | nS |
| $T_{THL}$ | TRDY# Active from CLK | | – | 11 | nS |
| $T_{TLH}$ | TRDY# Inactive from CLK | | 2 | 11 | nS |
| $T_{THZ}$ | TRDY# High before High Z | | 1 | 1 | **CLK** |
| $T_{DZL}$ | DEVSEL# Active from CLK | | – | 11 | nS |
| $T_{DLH}$ | DEVSEL# Inactive from CLK | | 2 | 11 | nS |
| $T_{DHZ}$ | DEVSEL# High before High Z | | 1 | 1 | **CLK** |
| $T_{ISC}$ | IRDY# Setup to CLK | | 7 | – | nS |
| $T_{IHC}$ | IRDY# Hold from CLK | | 2 | – | nS |

**Note:** Unless otherwise specified, specifications above apply to both 5V & 3.3V operation & memory clock is assumed to be 75MHz. Electrical specifications contained herein are preliminary and subject to change without notice.




**PCI Bus Frame Timing**

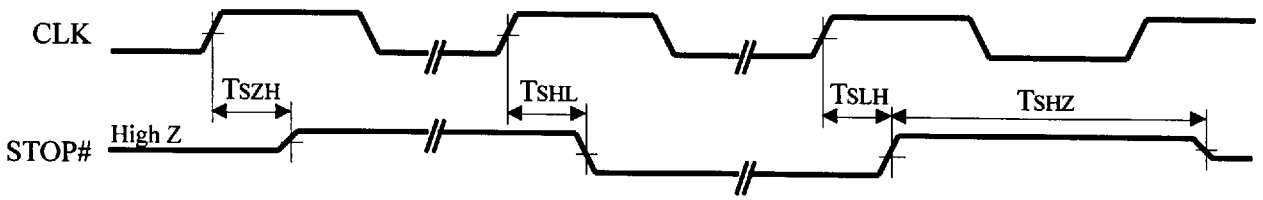
**Note:** The above diagram shows a typical PCI bus cycle. PCI bus read cycles require a bus turn-around cycle between address output and data input on AD31:0. PCI bus write cycles do not require this bus turnaround cycle so the write data is available from the bus master immediately after address output (in clock cycle 2 instead of clock cycle 3).

**Note:** Only consecutive active byte enables [BE(3:0)] are supported for both memory and I/O accesses.

**Note:** Unless otherwise specified, specifications above apply to both 5V & 3.3V operation & memory clock is assumed to be 75MHz. Electrical specifications contained herein are preliminary and subject to change without notice.

## 65548 AC TIMING CHARACTERISTICS - PCI BUS STOP (33 MHz)

| Symbol | Parameter | Notes | Min | Max | Units |
|---|---|---|---|---|---|
| $T_{SZH}$ | STOP# High Z to High from CLK | | – | 11 | nS |
| $T_{SHL}$ | STOP# Active from CLK | | – | 11 | nS |
| $T_{SLH}$ | STOP# Inactive from CLK | | – | 11 | nS |
| $T_{SHZ}$ | STOP# High before High Z | | 1 | 1 | CLK |

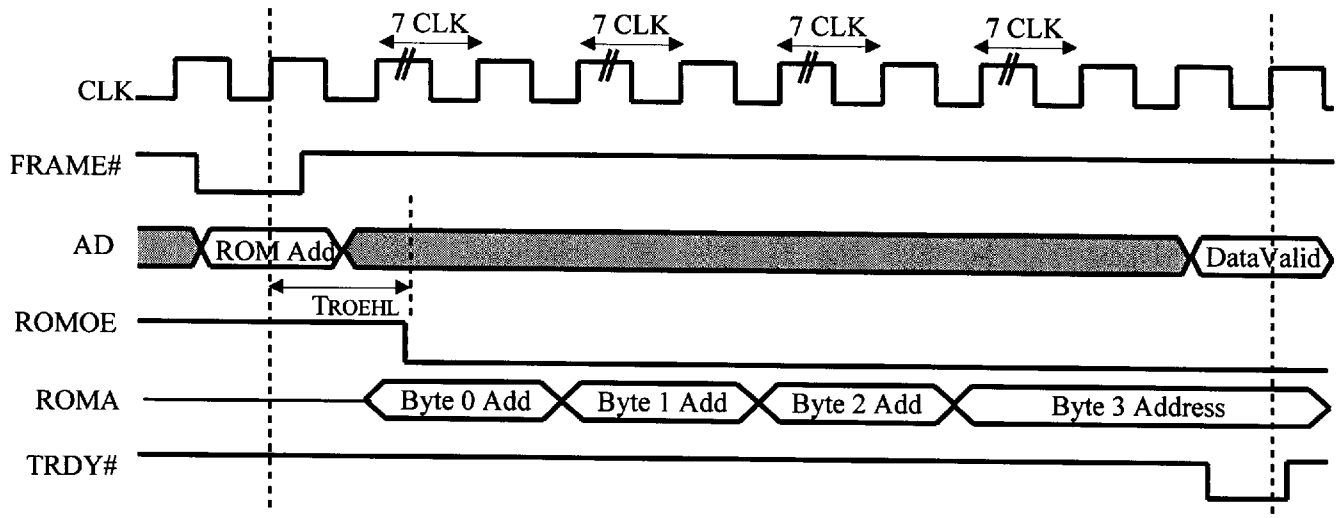



**PCI Bus Stop Timing**

## 65548 AC TIMING CHARACTERISTICS - PCI BIOS ROM

| Symbol | Parameter | Notes | Min | Max | Units |
|---|---|---|---|---|---|
| $T_{ROE}$ | ROMOE# Active from CLK | | – | 40 | nS |

**Note:** PCI BIOS ROM timing is derived from the PCI bus clock. Timing sequences are fixed assuming the use of widely-available, low-cost, typical industry-standard EPROMs. Timing specifications and performance of BIOS ROM memory accesses are non-critical since PCI BIOS ROM data is always shadowed into high-speed system memory prior to execution of BIOS code.



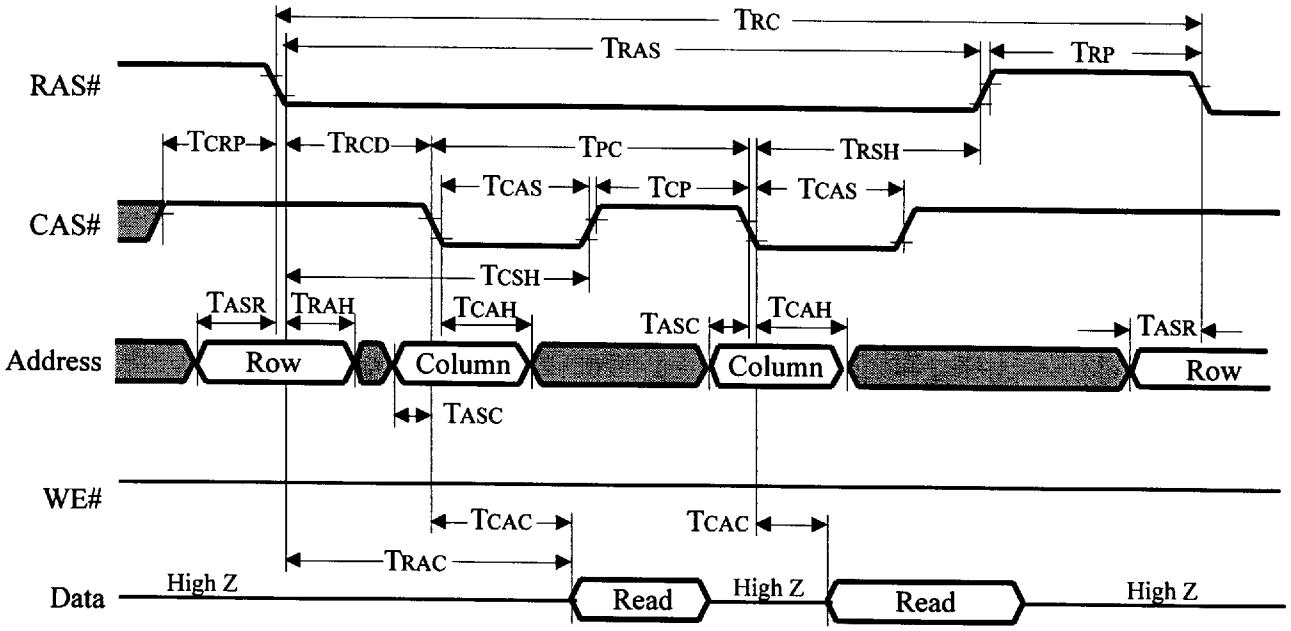

**PCI BIOS ROM Timing**

**Note:** Unless otherwise specified, specifications above apply to both 5V & 3.3V operation & memory clock is assumed to be 75MHz. Electrical specifications contained herein are preliminary and subject to change without notice.

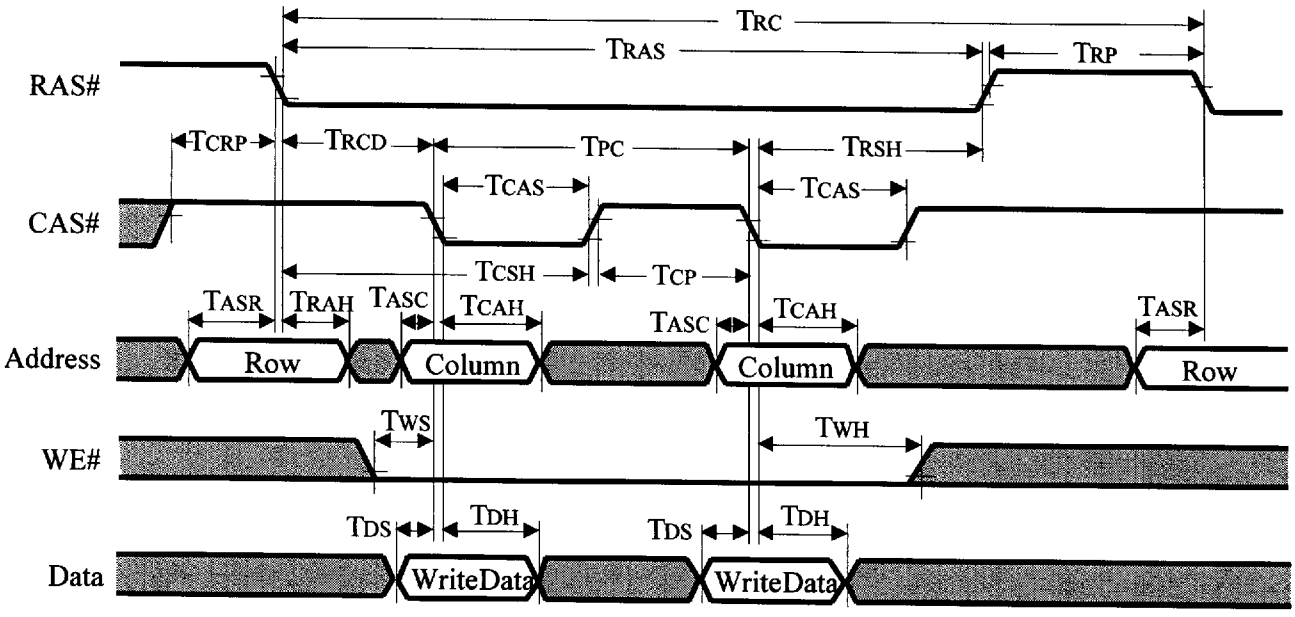
## 65548 AC TIMING CHARACTERISTICS - DRAM READ/WRITE

| Symbol | Parameter | Notes | Min | Max | Units |
|---|---|---|---|---|---|
| $T_{RC}$ | Read/WriteCycleTime | $T_{RCD}$=3, $T_{RP}$=3 (Reset) | 11Tm – 2 | – | nS |
| | | $T_{RCD}$=3, $T_{RP}$=4 (Normal) | 12Tm – 2 | – | nS |
| | | $T_{RCD}$=4, $T_{RP}$=3 | 12Tm – 2 | – | nS |
| | | $T_{RCD}$=4, $T_{RP}$=4 | 13Tm – 2 | – | nS |
| $T_{RAS}$ | RAS# Pulse Width | XR05[3]=0 ($T_{RCD}$=3 Clks) (Default) | 8Tm – 2 | – | nS |
| | | XR05[3]=1 ($T_{RCD}$=4 Clks) | 9Tm – 2 | – | nS |
| $T_{RP}$ | RAS# Precharge | XR04[4]=0 ($T_{RP}$=3 Clks) | 3Tm – 3 | – | nS |
| | | XR04[4]=1 ($T_{RP}$=4 Clks) (Default) | 4Tm – 3 | – | nS |
| $T_{CRP}$ | CAS# to RAS# Precharge | XR04[4]=1 ($T_{RP}$=4 Clks) (Default) | 4Tm – 5 | – | nS |
| | | XR04[4]=0 ($T_{RP}$=3 Clks) | 3Tm – 5 | – | nS |
| $T_{CSH}$ | CAS# Hold from RAS# | XR05[3]=0 ($T_{RCD}$=3 Clks) (Default) | 5Tm – 2 | – | nS |
| | | XR05[3]=1 ($T_{RCD}$=4 Clks),(4Clk CAS) | 6Tm – 2 | – | nS |
| $T_{RCD}$ | RAS# to CAS# Delay | XR05[3]=0 ($T_{RCD}$=3 Clks) (Default) | 3Tm – 5 | – | nS |
| | | XR05[3]=1 ($T_{RCD}$=4 Clks) | 4Tm – 5 | – | nS |
| $T_{RSH}$ | RAS# Hold from CAS# | | 2Tm – 5 | – | nS |
| $T_{CP}$ | CAS# Precharge | | Tm – 2 | – | nS |
| $T_{CAS}$ | CAS# Pulse Width | | 2Tm – 5 | – | nS |
| $T_{ASR}$ | Row Address Setup to RAS# | | Tm – 8 | – | nS |
| $T_{ASC}$ | Column Address Setup to CAS# | | 2Tm – 9 | – | nS |
| $T_{RAH}$ | Row Address Hold from RAS# | | Tm – 2 | – | nS |
| $T_{CAH}$ | Column Address Hold from CAS# | | Tm – 2 | – | nS |
| $T_{CAC}$ | Data Access Time from CAS# | XR05[2-1]=0 (3Clk CAS) Std | – | 2Tm – 5 | nS |
| | | XR05[2-1]=0 (3Clk CAS) EDO | – | 2.5Tm – 5 | nS |
| | | XR05[2-1]=1 (4Clk CAS) Std | – | 3Tm – 5 | nS |
| | | XR05[2-1]=1 (4Clk CAS) EDO | – | 3.5Tm – 5 | nS |
| $T_{RAC}$ | Data Access Time from RAS# | XR05[2-1]=0 ($T_{RCD}$=3 Clks) Std | – | 5Tm – 2 | nS |
| | | XR05[2-1]=0 ($T_{RCD}$=3 Clks) EDO | – | 5.5Tm – 2 | nS |
| | | XR05[2-1]=1 ($T_{RCD}$=3 Clks) Std | – | 6Tm – 2 | nS |
| | | XR05[2-1]=1 ($T_{RCD}$=3 Clks) EDO | – | 6.5Tm – 2 | nS |
| | | XR05[2-1]=0 ($T_{RCD}$=4 Clks) Std | – | 6Tm – 2 | nS |
| | | XR05[2-1]=0 ($T_{RCD}$=4 Clks) EDO | – | 6.5Tm – 2 | nS |
| | | XR05[2-1]=1 ($T_{RCD}$=4 Clks) Std | – | 7Tm – 2 | nS |
| | | XR05[2-1]=1 ($T_{RCD}$=4 Clks) EDO | – | 7.5Tm – 2 | nS |
| $T_{DS}$ | Write Data Setup to CAS# | XR05[3]=0 ($T_{RCD}$=3 Clks) (Default) | Tm – 9 | – | nS |
| | | XR05[3]=1 ($T_{RCD}$=4 Clks) | 2Tm – 9 | – | nS |
| $T_{DH}$ | Write Data Hold from CAS# | | Tm – 2 | – | nS |
| $T_{PC}$ | CAS Cycle Time | | 3Tm – 1 | – | nS |
| $T_{WS}$ | WE# Setup to CAS# | XR05[3]=0 ($T_{RCD}$=3 Clks) (Default) | Tm – 5 | – | nS |
| | | XR05[3]=1 ($T_{RCD}$=4 Clks) | 2Tm – 5 | – | nS |
| $T_{WP}$ | WE# Hold from CAS# | | 2Tm – 5 | – | nS |

**Note:** The minimum $T_{RAS}$ is 8 clocks for a 2 CAS page mode cycle. Without page mode it is 5 clocks.




**DRAM Page Mode Read Cycle Timing**



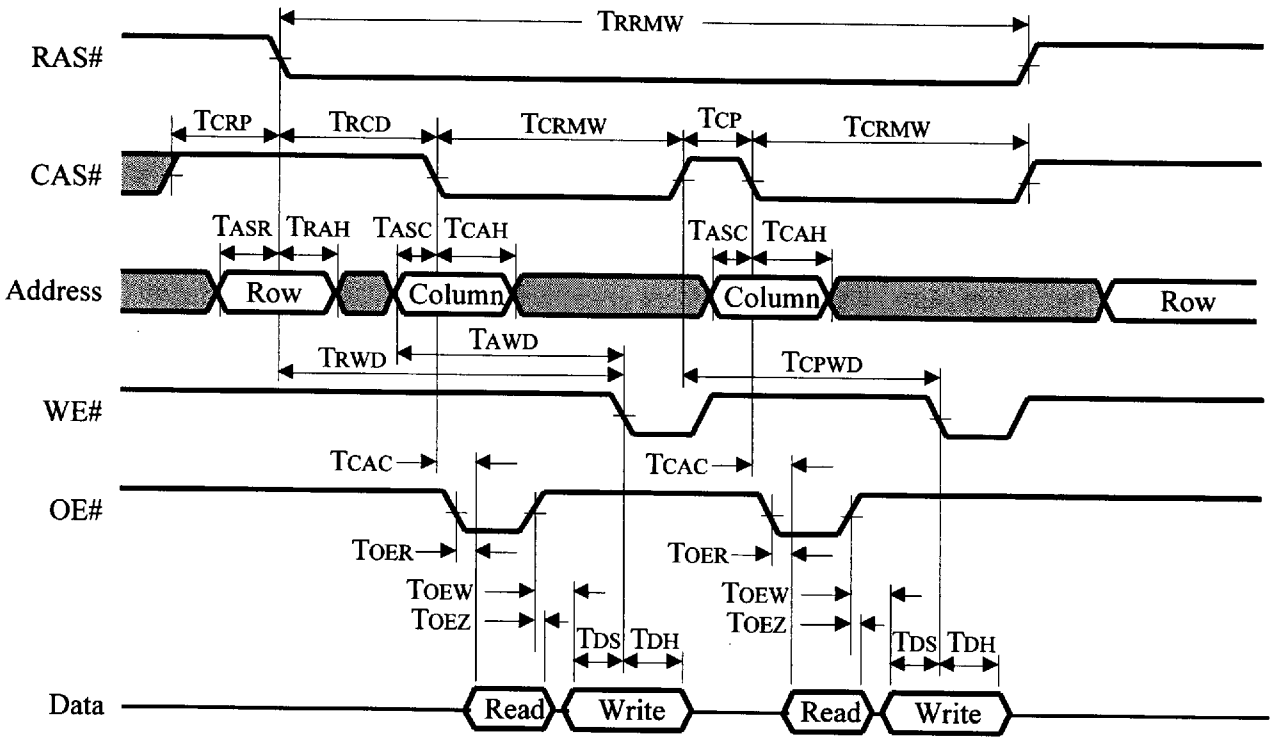

**DRAM Page Mode Write Cycle Timing**

**Note:** The above diagrams represent typical page mode cycles. The number of actual CAS cycles may vary.

**Note:** Unless otherwise specified, specifications above apply to both 5V & 3.3V operation & memory clock is assumed to be 75MHz. Electrical specifications contained herein are preliminary and subject to change without notice.

## 65548 AC TIMING CHARACTERISTICS - DRAM READ/MODIFY/WRITE

| Symbol | Parameter | Notes | Min | Max | Units |
|---|---|---|---|---|---|
| $T_{RRMW}$ | RAS# Pulse Width | XR05[3]=0 ($T_{RCD}$=3 Clks) (Default) | 16Tm – 5 | – | nS |
| | | XR05[3]=1 ($T_{RCD}$=4 Clks) | 17Tm – 5 | – | nS |
| $T_{CRMW}$ | CAS# Pulse Width | | 6Tm – 5 | – | nS |
| $T_{AWD}$ | Col Address to WE# Delay | XR05[3]=0 ($T_{RCD}$=3 Clks) (Default) | 6Tm – 8 | – | nS |
| | | XR05[3]=1 ($T_{RCD}$=4 Clks) | 7Tm – 8 | – | nS |
| $T_{RWD}$ | RAS# to WE# Delay | XR05[3]=0 ($T_{RCD}$=3 Clks) (Default) | 7Tm – 5 | – | nS |
| | | XR05[3]=1 ($T_{RCD}$=4 Clks) | 8Tm – 5 | – | nS |
| $T_{CPWD}$ | CAS# Precharge to WE# Delay | | 5Tm – 5 | – | nS |
| $T_{OEZ}$ | Output Turnoff Delay from OE# | | – | Tm | nS |
| $T_{OEW}$ | OE# Write Data Delay | | Tm + 3 | – | nS |
| $T_{OER}$ | OE# Read Data Delay | XR05[7]=0 (Std DRAMS) | – | 2Tm – 5 | nS |
| | | XR05[7]=1 (EDO DRAMs) | – | 3Tm – 5 | nS |
| | | XR05[1]=1 (4 Clk CAS) | – | 3Tm – 5 | nS |



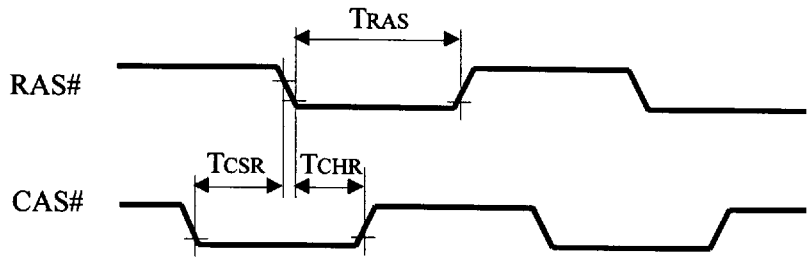

**DRAM Page Mode Read Modify Write Cycle Timing**

**Note:** The above diagrams represent typical page mode cycles. The number of actual CAS cycles may vary.

**Note:** Unless otherwise specified, specifications above apply to both 5V & 3.3V operation & memory clock is assumed to be 75MHz. Electrical specifications contained herein are preliminary and subject to change without notice.

## 65548 AC TIMING CHARACTERISTICS - CBR REFRESH

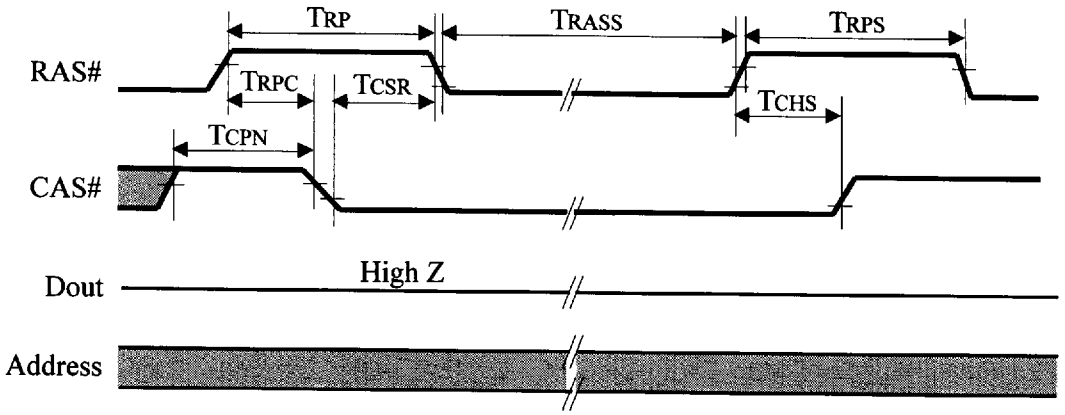
| Symbol | Parameter | Notes | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $T_{CHR}$ | RAS# to CAS# Delay | | 5Tm – 5 | – | – | nS |
| $T_{CSR}$ | CAS# to RAS# Delay | NormalOperation | Tm – 2 | – | – | nS |
| | | Standby Mode | 2Tm – 5 | – | – | nS |
| $T_{RAS}$ | RAS# Pulse Width | | 5Tm – 5 | – | – | nS |




**CAS-Before-RAS (CBR) DRAM Refresh Cycle Timing**

## 65548 AC TIMING CHARACTERISTICS - SELF REFRESH

| Symbol | Parameter | Notes | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $T_{RASS}$ | RAS# Pulse Width for Self-Refresh | | 100 | – | – | µS |
| $T_{RP}$ | RAS# Precharge | XR04[4]=0 ($T_{RP}$=3 Clks) | 3Tm – 3 | | – | nS |
| | | XR04[4]=1 ($T_{RP}$=4 Clks) (Default) | 4Tm – 3 | | – | nS |
| $T_{RPS}$ | RAS# Precharge for Self-Refresh | | 10Tm | – | – | nS |
| $T_{RPC}$ | RAS# to CAS# Delay | | 3Tm – 5 | – | – | nS |
| $T_{CSR}$ | CAS# to RAS# Delay | NormalOperation | Tm – 2 | – | – | nS |
| | | Standby Mode | 2Tm – 5 | – | – | nS |
| $T_{CHS}$ | CAS# Hold Time | | 0 | – | – | nS |
| $T_{CPN}$ | CAS# Precharge | | Tm – 5 | – | – | nS |

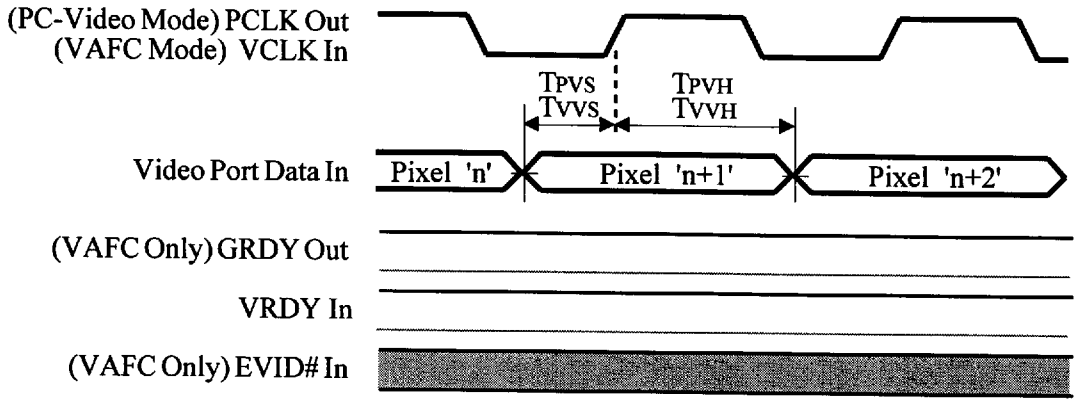



**'Self-Refresh DRAM' Refresh Cycle Timing**

**Note: Upon exiting self-refresh mode, the 65548 will perform a complete set of CBR refresh cycles before resuming normal DRAM activity. The duration of the burst refresh will equal the panel power sequencing delay, programmed in XR5B bits 7-4.**

## 65548 AC TIMING CHARACTERISTICS - VIDEO INPUT PORT TIMING

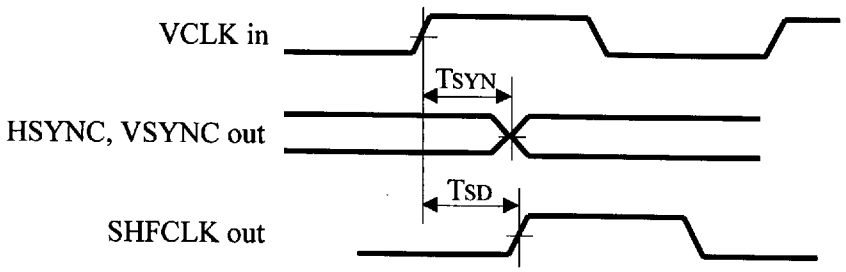
| Symbol | Parameter | Notes | Min | Max | Units |
|---|---|---|---|---|---|
| $T_{PVS}$ | Video Port Input Data Setup to PCLK out | PC-Video Mode | 12 | – | nS |
| $T_{PVH}$ | Video Port Input Data Hold from PCLK out | PC-Video Mode | 0 | – | nS |
| $T_{VVS}$ | Video Port Input Data Setup to VCLK in | VAFC Mode | 10 | – | nS |
| $T_{PVH}$ | Video Port Input Data Hold from VCLK in | VAFC Mode | 2 | – | nS |
| $T_{VCK}$ | VCLK Input Frequency | VAFC 1.0 Specification | – | 37.5 | MHz |
| $T_{VCH}$ | VCLK Input Clock High Time | VAFC 1.0 Specification | 10 | – | nS |
| $T_{VCL}$ | VCLK Input Clock Low Time | VAFC 1.0 Specification | 10 | – | nS |




**Video Input Port Timing**

## 65548 AC TIMING CHARACTERISTICS - CRT OUTPUT TIMING

| Symbol | Parameter | Notes | Min | Max | Units |
|---|---|---|---|---|---|
| $T_{SYN}$ | HSYNC, VSYNC delay from VCLK in | | – | 50 | nS |
| $T_{SYN}$ | HSYNC, VSYNC delay from VCLK in **(3.3V)** | | – | 80 | nS |
| $T_{SD}$ | VCLK in to SHFCLK delay | | – | 30 | nS |
| $T_{SD}$ | VCLK in to SHFCLK delay **(3.3V)** | | – | 50 | nS |



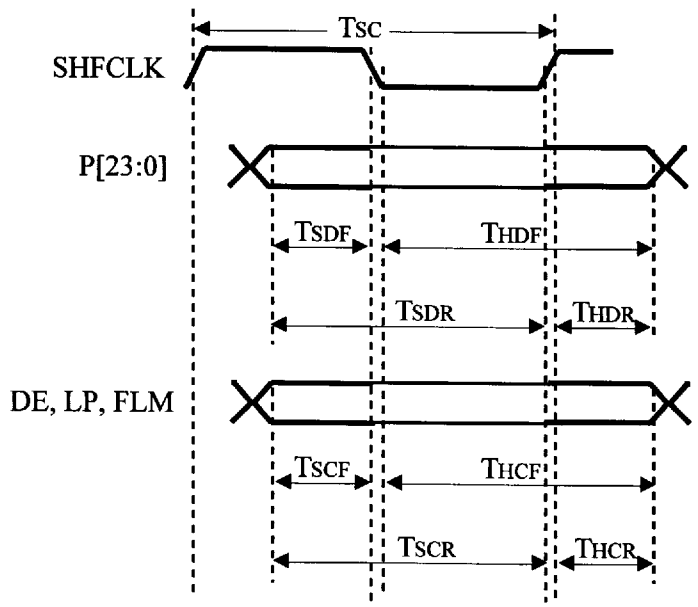

**CRT Output Timing**

**Note:** Unless otherwise specified, specifications above apply to both 5V & 3.3V operation & memory clock is assumed to be 75MHz. Electrical specifications contained herein are preliminary and subject to change without notice.

## 65548 AC TIMING CHARACTERISTICS - PANEL OUTPUT TIMING

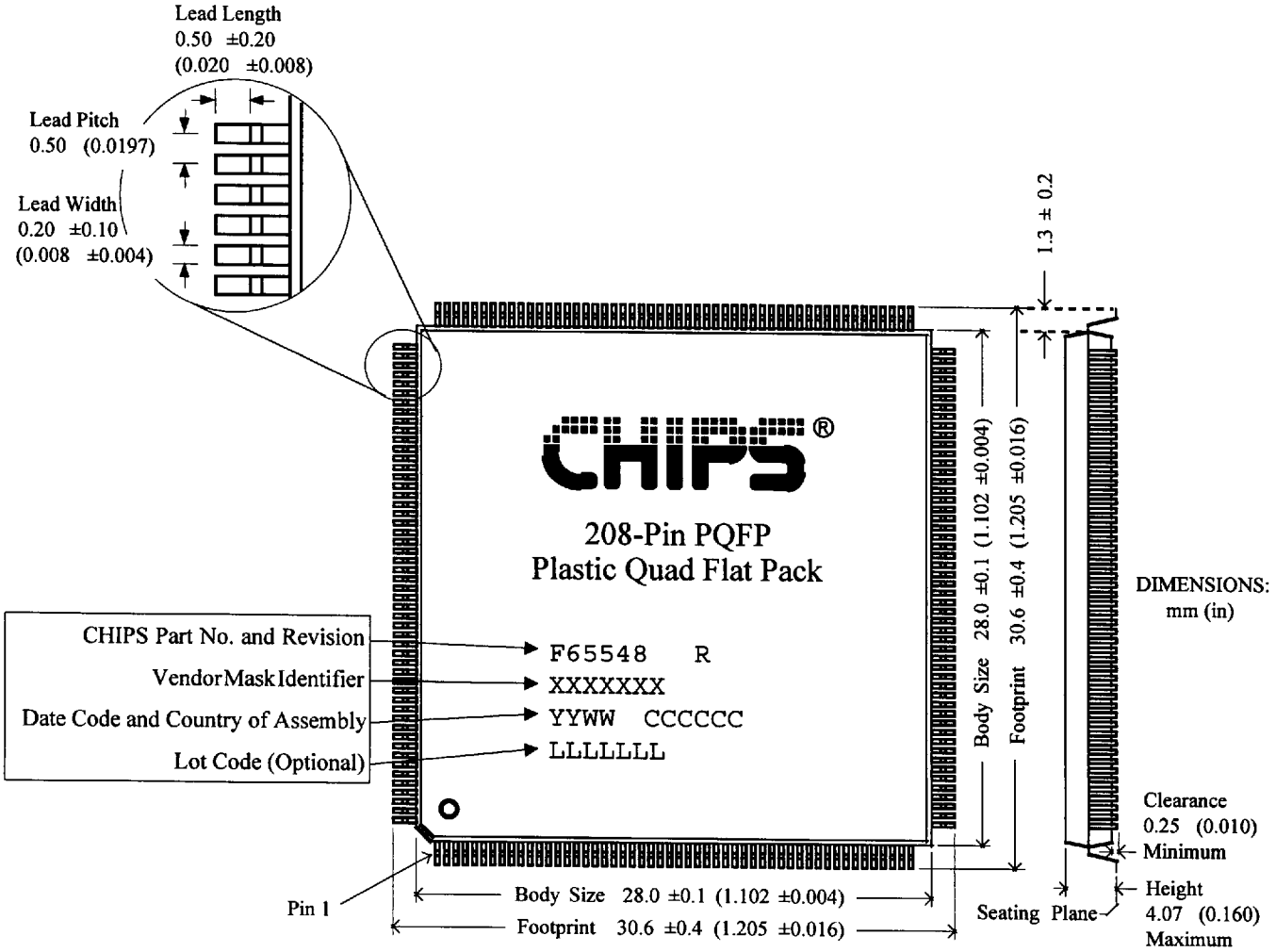
| Symbol | Parameter | Notes | Min | Max | Units |
|---|---|---|---|---|---|
| $T_{SC}$ | SHFCLK cycle time | Data latched on SHFCLK fall | 25 | – | nS |
| | | Data latched on SHFCLK rise | 15 | – | nS |
| $T_{SDF}$ | Panel data setup to SHFCLK fall | | 1/2 Tsc-5 | – | nS |
| $T_{HDF}$ | Panel data hold to SHFCLK fall | | 1/2 Tsc-3 | – | nS |
| $T_{SDR}$ | Panel data setup to SHFCLK rise | | Tsc-10 | – | nS |
| $T_{HDR}$ | Panel data hold to SHFCLK rise | | 0 | – | nS |
| $T_{SCF}$ | Panel control setup to SHFCLK fall | | 1/2 Tsc-5 | – | nS |
| $T_{HCF}$ | Panel control hold to SHFCLK fall | | 1/2 Tsc-3 | – | nS |
| $T_{SCR}$ | Panel control setup to SHFCLK rise | | Tsc-10 | – | nS |
| $T_{HCR}$ | Panel control hold to SHFCLK rise | | -3 | – | nS |

**Note:** AC Timing is valid when: DVCC=5V, XR6C[2]=X, max output loading=50pF or when: DVCC=3.3V, XR6C[2]=1, max output loading=25pF.




**Panel Output Timing**

# Mechanical Specifications
# Plastic Quad Flat Pack (PQFP)




DS176.2
Rev 1.1
2/28/96