

QL12X16B pASIC[®] 1 Family Very-High-Speed CMOS FPGA

Rev C

pASIC HIGHLIGHTS

...2,000 usable ASIC gates, 88 I/O pins

> QL12x16B Block Diagram

192 Logic Cells



- High Usable Density A 12-by-16 array of 192 logic cells provides 2,000 usable ASIC gates (4,000 PLD gates) in 68-pin and 84-pin PLCC, 84-pin CPGA and 100-pin TQFP packages.
- Low-Power, High-Output Drive Standby current typically 2 mA. A 16-bit counter operating at 100 MHz consumes less than 50 mA. Minimum IOL of 12 mA and IOH of 8 mA
- Low-Cost, Easy-to-Use Design Tools Designs entered and simulated using QuickLogic's new Quick*Works*[®] development environment, or with third-party CAE tools including Viewlogic, Synopsys, Mentor, Cadence and Veribest. Fast, fully automatic place and route on PC and workstation platforms using QuickLogic software.

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Up to 80 prog. I/O cells, 6 Input high-drive cells, 2 Input/Clk (high-drive) cells

QL12x1	6B
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X	QL12x16B
PRODUCT SUMMARY	The QL12x16B is a member of the pASIC 1 Family of very-high-speed CMOS user-programmable ASIC devices. The 192 logic cell field-programmable gate array (FPGA) offers 2,000 usable ASIC gates (4,000 usable PLD gates) of high-performance general-purpose logic in a wide variety of package configurations.
	Low-impedance, metal-to-metal, ViaLink interconnect technology provides nonvolatile custom logic capable of operating above 150 MHz. Logic cell delays under 2 ns, combined with input delays of under 1.5 ns and output delays under 3 ns, permit high-density programmable devices to be used with today's fastest microprocessors and DSPs.
	Designs can be entered using QuickLogic's Quick <i>Works</i> Toolkit or most populart third-party CAE tools. Quick <i>Works</i> combines Verilog/VHDL design entry and simulation tools with device-specific place & route and programming software. Ample on-chip routing channels allow fast, fully automatic place and route of designs using up to 100% of the logic and I/O cells, while maintaining fixed pin-outs.
FEATURES	Total of 88 I/O pins
	 80 Bidirectional Input/Output pins
	 6 Dedicated Input/High-Drive pins
	 2 Clock/Dedicated input pins with fanout-independent, low-skew clock networks Input + logic cell + output delays under 6 ns
	Chip-to-chip operating frequencies up to 110 MHz
	Internal state machine frequencies up to 150 MHz
	Clock skew < 0.5 ns
	Input hysteresis provides high noise immunity
	Built-in scan path permits 100% factory testing of logic and I/O cells and functional testing with Automatic Test Vector Generation (ATVG) software after programming
	Available in 68-pin and 84-pin PLCC, 84-pin CPGA and 100-pin TQFP packages
	✓ 68-pin PLCC compatible with QL8x12B
	84-pin PLCC compatible with QL16x24B
	■ 100-pin TQFP compatible with QL8x12B and QL16x24B
	■ 0.65µ CMOS process with ViaLink programming technology



Pins identified I/SCLK, SM, SO and SI are used during scan path testing operation.

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QL12x16B



Pinout Diagram 84-pin CPGA



BOTTOM VIEW						
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CPGA 84 Function/Connector Pin Table

PIN	FUNC	PIN	FUNC	PIN	FUNC	PIN	FUNC
B10	Ю	B2	10	K2	IO	K10	IO
B9	Ю	C2	10	K3	IO	J10	IO
A10	IO	B1	10	L2	IO	K11	IO
A9	ю	C1	10	L3	IO	J11	IO
B8	IO	D2	10	K4	IO	H10	IO
A8	ю	D1	10	L4	IO	H11	IO
A7	IO	E1	10	L5	IO	G11	IO
C7	GND	E3	GND	J5	GND	G9	GND
A6	IO	E2	10	L6	IO	G10	IO
B7	I/(SCLK)	F1	10	K5	I/(SI)	F11	IO
C6	I/CLK/(SM)	F2	10	J6	I/CLK	F10	IO
B6	I(P)	F3	10	K6	I	F9	IO
B5	I	G1	10	K7	I/(SO)	E11	IO
C5	VCC	G3	VCC	J7	VCC	E9	VCC
A5	IO	G2	10	L7	IO	E10	IO
A4	IO	H1	10	L8	IO	D11	IO
B4	IO	H2	10	K8	IO	D10	IO
A3	IO	J1	10	L9	IO	C11	IO
A2	10	K1	10	L10	10	B11	IO
B3	10	J2	10	K9	IO	C10	IO
A1	10	L1	10	L11	IO	A11	10

QL12x16B





ABSOLUTE MAXIMUM RATINGS

Supply Voltage	0.5 to 7.0V
Input Voltage	$-0.5\ to\ VCC\ +0.5\ V$
ESD Pad Protection	±2000V
DC Input Current	±20 mA
Latch-up Immunity	±200 mA

Storage Temperature	$65^{\circ}C \text{ to } + 1$	50°C
Lead Temperature	,	300°C

OPERATING RANGE

Symbol	Parameter		Military		Industrial		Commercial		Unit
			Min	Max	Min	Max	Min	Max	
VCC	Supply Voltage		4.5	5.5	4.5	5.5	4.75	5.25	V
TA	Ambient Temperature		-55		-40	85	0	70	°C
TC	Case Temperature			125					°C
		-X Speed Grade			0.4	2.75	0.46	2.55	
K	Delay Factor	-0 Speed Grade	0.39	1.82	0.4	1.67	0.46	1.55	
		-1 Speed Grade	0.39	1.56	0.4	1.43	0.46	1.33	
		-2 Speed Grade			0.4	1.35	0.46	1.25	

DC CHARACTERISTICS over operating range

Symbol	Parameter	Conditions	Min	Max	Unit
VIH	Input HIGH Voltage		2.0		V
VIL	Input LOW Voltage			0.8	V
		IOH = -4 mA	3.7		V
VOH	Output HIGH Voltage	IOH = -8 mA	2.4		V
		IOH = -10 μA	VCC-0.1		V
VOL	Output LOW Voltage	IOL = 12 mA*		0.4	V
		IOL = 10 μA		0.1	V
П	Input Leakage Current	VI = VCC or GND	-10	10	μA
IOZ	3-State Output Leakage Current	VI = VCC or GND	-10	10	μA
CI	Input Capacitance [1]			10	pF
IOS	Output Short Circuit Current [2]	VO = GND	-10	-80	mA
		VO = VCC	30	140	mA
ICC	D.C. Supply Current [3]	VI, VIO = VCC or GND		10	mA

*IOL = 12 mA for commercial range only. IOL = 8 mA for the industrial and military ranges.

Notes:

- [1] Capacitance is sample tested only. CI = 20 pF max on I/(SI).
- [2] Only one output at a time. Duration should not exceed 30 seconds.
- [3] Commercial temperature grade only. Maximum Icc for industrial grade is 15mA and for military grade is 20 mA. For AC conditions use the formula described in the Section 9 Power vs Operating Frequency.
- [4] Stated timing for worst case Propagation Delay over process variation at VCC = 5.0V and TA = 25°C. Multiply by the appropriate Delay Factor, K, for speed grade, voltage and temperature settings as specified in the Operating Range.
- [5] These limits are derived from a representative selection of the slowest paths through the pASIC logic cell *including net delays*. Worst case delay values for specific paths should be determined from timing analysis of your particular design.



AC CHARACTERISTICS at VCC = 5V, TA = 25° C (K = 1.00)

Logic Cell

		Propagation Delays (ns)					
Symbol	Parameter	Fanout					
		1	2	3	4	8	
tPD	Combinatorial Delay [5]	1.7	2.2	2.6	3.2	5.2	
tSU	Setup Time [5]	2.1	2.1	2.1	2.1	2.1	
tH	Hold Time	0.0	0.0	0.0	0.0	0.0	
tCLK	Clock to Q Delay	1.0	1.5	1.9	2.5	4.6	
tCWHI	Clock High Time	2.0	2.0	2.0	2.0	2.0	
tCWLO	Clock Low Time	2.0	2.0	2.0	2.0	2.0	
tSET	Set Delay	1.7	2.1	2.6	3.2	5.2	
tRESET	Reset Delay	1.5	1.9	2.2	2.7	4.3	
tSW	Set Width	1.9	1.9	1.9	1.9	1.9	
tRW	Reset Width	1.8	1.8	1.8	1.8	1.8	

Input Cells

Symbol	Parameter	Propagation Delays (ns) [4]						
			2	3	4	6	8	
tIN	High Drive Input Delay [6]	2.4	2.5	2.6	2.7	3.0	3.3	
tINI	High Drive Input, Inverting Delay [6]	2.5	2.6	2.7	2.8	3.1	3.4	
tIO	Input Delay (bidirectional pad)	1.4	1.9	2.2	2.8	3.7	4.6	
tGCK	Clock Buffer Delay [7]	2.7	2.8	2.8	2.9	2.9	3.0	
tGCKHI	Clock Buffer Min High [7]	2.0	2.0	2.0	2.0	2.0	2.0	
tGCKLO	Clock Buffer Min Low [7]	2.0	2.0	2.0	2.0	2.0	2.0	

Output Cell

		Propagation Delays (ns) [4]						
Symbol	Parameter	r Output Load Capacitar				F)		
-		30	50	75	100	150		
tOUTLH	Output Delay Low to High	2.7	3.4	4.2	5.0	6.7		
tOUTHL	Output Delay High to Low	2.8	3.7	4.7	5.6	7.6		
tPZH	Output Delay Tri-state to High	4.0	4.9	6.1	7.3	9.7		
tPZL	Output Delay Tri-state to Low	3.6	4.2	5.0	5.8	7.3		
tPHZ	Output Delay High to Tri-state [8]	2.9						
tPLZ	Output Delay Low to Tri-state [8]	3.3						

Notes:

[6] See High Drive Buffer Table for more information.

[7] Clock buffer fanout refers to the maximum number of flip flops per half column. The number of half columns used does not affect clock buffer delay.

[8] The following loads are used for tPXZ:



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High Drive Buffer

		Clock Drivers	Propagation Delays (ns) [4] Fanout					
Symbol	Parameter	Wired Together						
		-	12	24	48	72	96	
		1	4.5	5.4				
tIN	tIN High Drive Input Delay	2		3.9	5.6			
		3			4.5	5.3	6.3	
		4				4.6	5.3	
		1	4.7	5.6				
tINI	High Drive Input,	2		4.0	5.8			
	Inverting Delay	3			4.6	5.5	6.4	
		4				4.8	5.5	

AC Performance

Propagation delays depend on routing, fanout, load capacitance, supply voltage, junction temperature, and process variation. The AC Characteristics are a design guide to provide initial timing estimates at nominal conditions. Worst case estimates are obtained when nominal propagation delays are multiplied by the appropriate Delay Factor, K, as specified in the Delay Factor table (Operating Range). The effects of voltage and temperature variation are illustrated in the graphs on page 4-47, K Factor versus Voltage and Temperature. The pASIC Development Tools incorporate data sheet AC Characteristics into the QDIF database for pre-place-and-route timing analysis. The SpDE Delay Modeler extracts specific timing parameters for precise path analysis or simulation results following place and route.

