



**A416316**

**64K X 16 CMOS DYNAMIC RAM WITH FAST PAGE MODE**

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**Document Title**

**64K X 16 CMOS DYNAMIC RAM WITH FAST PAGE MODE**

**Revision History**

<b><u>Rev. No.</u></b>	<b><u>History</u></b>	<b><u>Issue Date</u></b>	<b><u>Remark</u></b>
0.0	Initial issue	March 06, 1998	Preliminary
0.1	Modify 40/44L TSOP type II package outline drawing and dimensions notes	June 17, 1998	
0.2	Remove timing waveform of $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh counter test cycle	August 21, 1998	
0.3	Final spec release	September 8, 1998	Final
0.4	Erase $t_{\text{CP}}$ parameter Modify SOJ 40L outline dimensions Modify TSOP 40/44L (type II) outline dimensions	October 23, 1998	



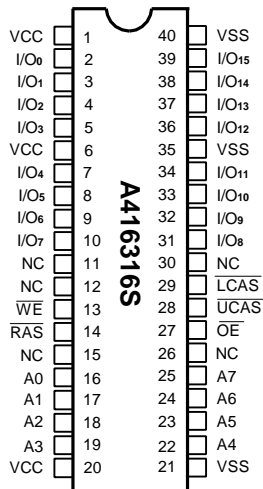
**64K X 16 CMOS DYNAMIC RAM WITH FAST PAGE MODE**

**Features**

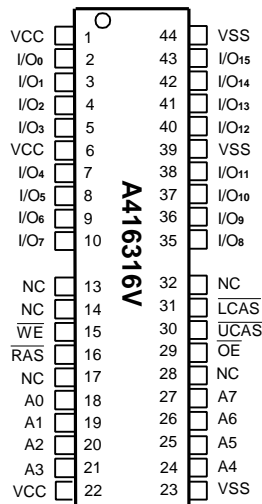
- Organization: 65,536 words X 16 bits
- High speed
  - 40/50/60 ns  $\overline{\text{RAS}}$  access time
  - 20/25/30 ns column address access time
  - 12/13/15 ns  $\overline{\text{CAS}}$  access time
- Low power consumption
  - Operating: 160mA (-40 max)
  - Standby: 3 mA (TTL)
- 256 refresh cycles, 4 ms refresh interval
- Read-modify-write,  $\overline{\text{RAS}}$ -only,  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ , Hidden refresh capability
- TTL-compatible, three-state I/O
- JEDEC standard packages
  - 400mil, 40-pin SOJ
  - 400mil, 40/44 TSOP type II package
- Single 5V power supply/built-in VBB generator

**Pin Configuration**

■ SOJ



■ TSOP



**Pin Descriptions**

Symbol	Description
A0 – A7	Address Inputs
I/O <sub>0</sub> - I/O <sub>15</sub>	Data Input/Output
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{UCAS}}$	Column Address Strobe/Upper Byte Control
$\overline{\text{LCAS}}$	Column Address Strobe/Lower Byte Control
$\overline{\text{WE}}$	Write Enable
$\overline{\text{OE}}$	Output Enable
VCC	+5V Power Supply
VSS	Ground
NC	No Connection

**Selection Guide**

Symbol	Description	-40	-50	-60	Unit
t <sub>RAC</sub>	Maximum $\overline{\text{RAS}}$ Access Time	40	50	60	ns
t <sub>AA</sub>	Maximum Column Address Access Time	20	25	35	ns
t <sub>CAC</sub>	Maximum $\overline{\text{CAS}}$ Access Time	12	13	15	ns
t <sub>OE</sub>	Maximum Output Enable ( $\overline{\text{OE}}$ ) Access Time	12	13	15	ns
t <sub>RC</sub>	Minimum Read or Write Cycle Time	75	90	110	ns
t <sub>PC</sub>	Minimum Fast Page Mode Cycle Time	22	31	40	ns
I <sub>CC1</sub>	Maximum Operating Current	160	140	120	mA
I <sub>CC6</sub>	Maximum CMOS Standby Current	2.0	2.0	2.0	mA

**Functional Description**

The A416316 is a high performance CMOS Dynamic Random Access Memory organized as 65,536 words X 16 bits. The A416316 is fabricated with advanced CMOS technology and designed with innovative design techniques resulting in high speed, extremely low power and wide operating margins at component and system levels.

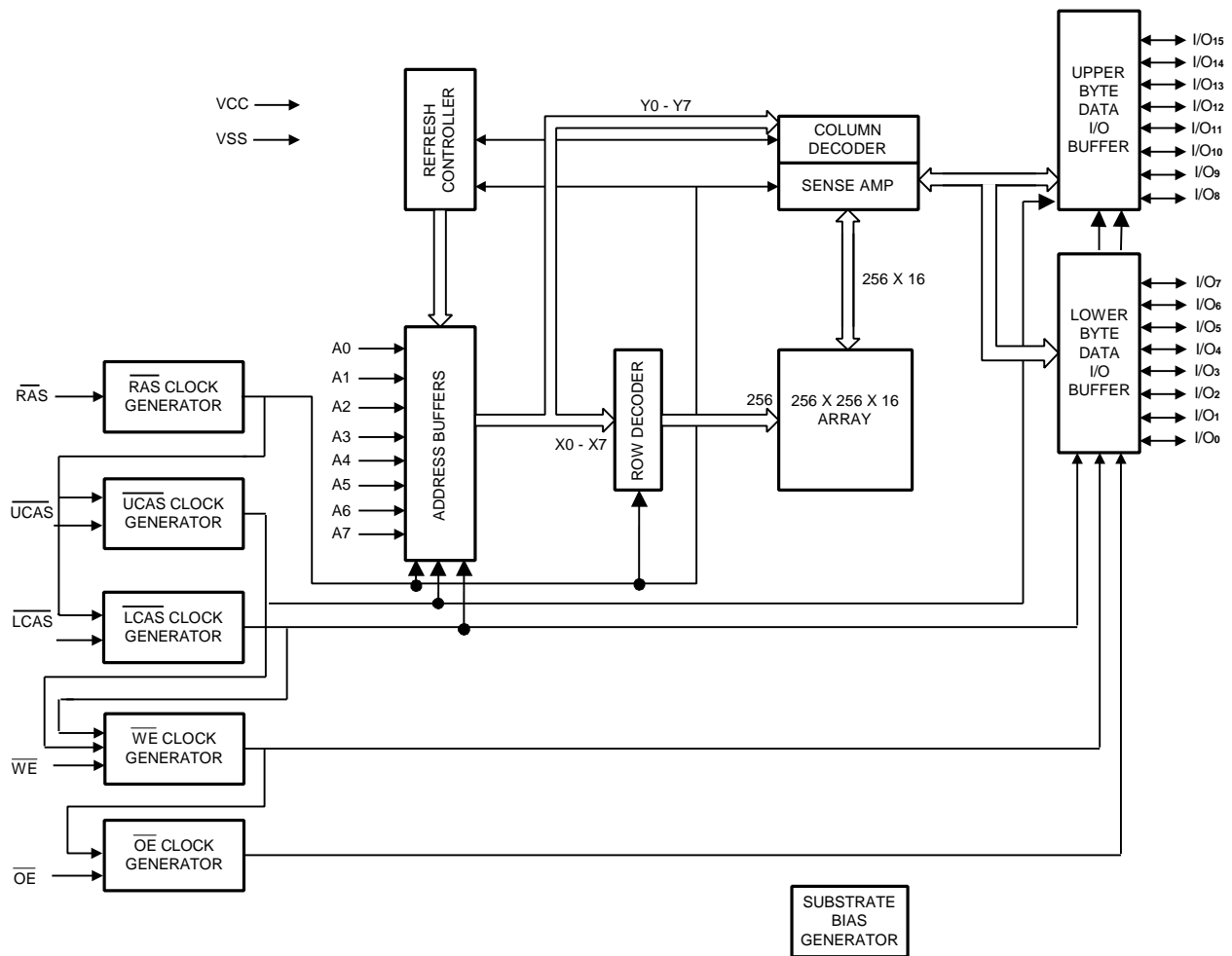
The A416316 features a high speed page mode operation in which high speed read, write and read-write are performed on any of the bits defined by the column address. The asynchronous column address uses an extremely short row address capture time to ease the system level timing constraints associated with multiplexed addressing. Output is tri-stated by a column

address strobe ( $\overline{\text{UCAS}}$  and  $\overline{\text{LCAS}}$ ) which acts as an output enable independent of  $\overline{\text{RAS}}$ . Very fast  $\overline{\text{UCAS}}$  and  $\overline{\text{LCAS}}$  to output access time eases system design.

All inputs are TTL compatible. Fast Page Mode operation allows random access up to 256 X 16 bits within a page, with cycle time as short as 22/31/40 ns.

The A416316 is best suited for graphics, digital signal processing and high performance peripherals.

The A416316 is available in JEDEC standard 40-pin plastic SOJ package and 40/44 TSOP type II package.

**Block Diagram**

**Recommended Operating Conditions** (T<sub>a</sub> = 0°C to +70°C)

Symbol	Description	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
VSS		0.0	0.0	0.0	V
V <sub>IH</sub>	Input Voltage	2.4	-	VCC + 1	V
V <sub>IL</sub>		-1.0	-	0.8	V

**Absolute Maximum Ratings\***

Input Voltage (V <sub>in</sub> )	-1.0V to +7.0V
Output Voltage (V <sub>out</sub> )	-1.0V to +7.0V
Power Supply Voltage (V <sub>CC</sub> )	-1.0V to +7.0V
Operating Temperature (T <sub>OPR</sub> )	0°C to +70°C
Storage Temperature (T <sub>STG</sub> )	-55°C to +150°C
Soldering Temperature X Time (T <sub>SLDER</sub> )	260°C X 10sec
Power Dissipation (P <sub>b</sub> )	1W
Short Circuit Output Current (I <sub>out</sub> )	50mA
Latch-up Current	200mA

**\*Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of these specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

**DC Electrical Characteristics (V<sub>CC</sub> = 5V ± 10%, V<sub>SS</sub> = 0V, T<sub>a</sub> = 0°C to +70°C)**

Symbol	Parameter	-40		-50		-60		Unit	Test Conditions	Notes
		Min.	Max.	Min.	Max.	Min.	Max.			
I <sub>IL</sub>	Input Leakage Current	-10	+10	-10	+10	-10	+10	μA	0V ≤ V <sub>in</sub> ≤ +5.5V Pins not under Test = 0V	
I <sub>OL</sub>	Output Leakage Current	-10	+10	-10	+10	-10	+10	μA	DOUT disabled, 0V ≤ V <sub>out</sub> ≤ +5.5V	
I <sub>CC1</sub>	Operating Power Supply Current	-	160	-	140	-	120	mA	$\overline{\text{RAS}}, \overline{\text{UCAS}}, \overline{\text{LCAS}}$ Address cycling; t <sub>rc</sub> = min.	1, 2
I <sub>CC2</sub>	TTL Standby Power Supply Current	-	3.0	-	3.0	-	3.0	mA	$\overline{\text{RAS}} = \overline{\text{UCAS}} = \overline{\text{LCAS}} = V_{IH}$	
I <sub>CC3</sub>	Average Power Supply Current, RAS Refresh Mode	-	160	-	140	-	120	mA	$\overline{\text{RAS}}$ cycling, $\overline{\text{UCAS}} = \overline{\text{LCAS}} = V_{IH}$ , t <sub>rc</sub> = min.	1
I <sub>CC4</sub>	Fast Page Mode Average Power Supply Current	-	160	-	140	-	120	mA	$\overline{\text{RAS}} = V_{IL}$ , $\overline{\text{UCAS}}, \overline{\text{LCAS}}$ Address cycling; t <sub>rc</sub> = min.	1, 2
I <sub>CC5</sub>	$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Power Supply Current	-	160	-	140	-	120	mA	$\overline{\text{RAS}}, \overline{\text{UCAS}}, \overline{\text{LCAS}}$ cycling; t <sub>rc</sub> = min.	1
I <sub>CC6</sub>	CMOS Standby Power Supply Current	-	2.0	-	2.0	-	2.0	mA	$\overline{\text{RAS}} = \overline{\text{UCAS}} = \overline{\text{LCAS}} = V_{CC} - 0.2V$	
V <sub>OH</sub>	Output Voltage	2.4	-	2.4	-	2.4	-	V	I <sub>out</sub> = -5.0mA	
V <sub>OL</sub>		-	0.4	-	0.4	-	0.4	V	I <sub>out</sub> = 4.2mA	

**AC Characteristics** ( $V_{CC} = 5V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $T_a = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ )

#	JEDEC Symbol	Std Symbol	Parameter	-40		-50		-60		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
1	tRL2RL2	trc	Random Read or Write Cycle Time	75	-	90	-	110	-	ns	
2	tRH2RL2	trp	$\overline{\text{RAS}}$ Precharge Time	25	-	25	-	25	-	ns	
3	tRL1RH1	trAS	$\overline{\text{RAS}}$ Pulse Width	40	75K	50	75K	60	75K	ns	
4	tCL1CH1	tCAS	$\overline{\text{CAS}}$ Pulse Width	12	-	12	-	12	-	ns	
5	tRL1CL1	trCD	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	16	30	18	37	20	45	ns	6
6	tRL1AV	trAD	$\overline{\text{RAS}}$ to Column Address Delay Time	11	22	13	25	15	30	ns	7
7	tCL1RH1	trSH(R)	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Hold Time (Read)	12	-	12	-	12	-	ns	
8	tRL1CH1	tCSH	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Hold Time	40	-	50	-	60	-	ns	
9	tCH2RL2	tCRP	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	5	-	5	-	5	-	ns	
10	tAVRL2	tASR	Row Address Setup Time	0	-	0	-	0	-	ns	
11	tRL1AX	trAH	Row Address Hold Time	6	-	8	-	10	-	ns	
	tT	tT	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	4, 5
	trVRV	tREF	Refresh Period	-	4	-	4	-	4	ms	3
12	tCL1QX	tCLZ	$\overline{\text{CAS}}$ to Output in Low Z	0	-	0	-	0	-	ns	8

**Read Cycle** ( $V_{CC} = 5V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $T_a = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ )

#	JEDEC Symbol	Std Symbol	Parameter	-40		-50		-60		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
13	tRL1QV	tRAC	Access Time from $\overline{\text{RAS}}$	-	40	-	50	-	60	ns	6
14	tCL1QV	tCAC	Access Time from $\overline{\text{CAS}}$	-	12	-	13	-	15	ns	6, 13
15	tAVQV	tAA	Access Time from Address	-	20	-	25	-	30	ns	7, 13
16	tRL1AZ	tAR(R)	Column Add Hold from $\overline{\text{RAS}}$	30	-	40	-	45	-	ns	
17	tWH2CL2	tRCS	Read Command Setup Time	0	-	0	-	0	-	ns	
18	tCH2WX	tRCH	Read Command Hold Time to $\overline{\text{CAS}}$	0	-	0	-	0	-	ns	9
19	tRH2WX	tRRH	Read Command Hold Time to $\overline{\text{RAS}}$	0	-	0	-	0	-	ns	9
20	tAVRH1	tRAL	Column Address to $\overline{\text{RAS}}$ Lead Time	20	-	25	-	30	-	ns	
21	tCH2CL2	tCRP	$\overline{\text{CAS}}$ Precharge Time	5	-	5	-	5	-	ns	
22	tRH2OL1	tODS	Output Disable Setup Time	0	-	0	-	0	-	ns	
23	tCH2QZ	tOFF	Output Buffer Turn-Off Time	0	8	0	10	0	12	ns	8, 10

**Write Cycle** ( $V_{CC} = 5V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $T_a = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ )

#	JEDEC Symbol	Std Symbol	Parameter	-40		-50		-60		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
24	tAVWL2	tASC	Column Address Setup Time	0	-	0	-	0	-	ns	
25	t1CL1AX	tCAH	Column Address Hold Time	6	-	8	-	10	-	ns	
26	tRL1AX	tAWR	Column Address Hold Time to $\overline{\text{RAS}}$	30	-	40	-	45	-	ns	
27	tWL1CL2	twCS	Write Command Setup Time	0	-	0	-	0	-	ns	11
28	tCH2WH1	twCH	Write Command Hold Time	6	-	7	-	10	-	ns	11
29	tRL1WH1	twCR	Write Command Hold Time to $\overline{\text{RAS}}$	30	-	40	-	45	-	ns	
30	tWL1WH1	tWP	Write Command Pulse Width	6	-	7	-	10	-	ns	
31	tWL1RH1	trWL	Write Command to $\overline{\text{RAS}}$ Lead Time	12	-	13	-	15	-	ns	
32	tWL1CH1	tcWL	Write Command to $\overline{\text{CAS}}$ Lead Time	12	-	13	-	15	-	ns	
33	tdVWL2	tdS	Data-in setup Time	0	-	0	-	0	-	ns	12
34	tWL1DX tCL1DX	tdH	Data-in Hold Time	6	-	7	-	10	-	ns	12
35	tRL1DX	tdHR	Data-in Hold Time to $\overline{\text{RAS}}$	33	-	40	-	45	-	ns	

**Read-Modify-Write Cycle** ( $V_{CC} = 5V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $T_a = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ )

#	JEDEC Symbol	Std Symbol	Parameter	-40		-50		-60		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
36	tRL2RL2	trWC	Read-Modify-Write Cycle Time	120	-	130	-	140	-	ns	
37	tRL1WL2	trWD	$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	63	-	75	-	85	-	ns	11
38	tCL1WL2	tcWD	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	30	-	33	-	38	-	ns	11
39	tAVWL2	tAWD	Column Address to $\overline{\text{WE}}$ Delay Time	38	-	43	-	53	-	ns	11
40	tCL1RH1	trSH(W)	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Hold Time (Write)	12	-	12	-	12	-	ns	
41	tCL1CH1	tcAS(W)	$\overline{\text{CAS}}$ Pulse Width (Write)	12	-	12	-	12	-	ns	



**Fast Page Mode Cycle** ( $V_{CC} = 5V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $T_a = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ )

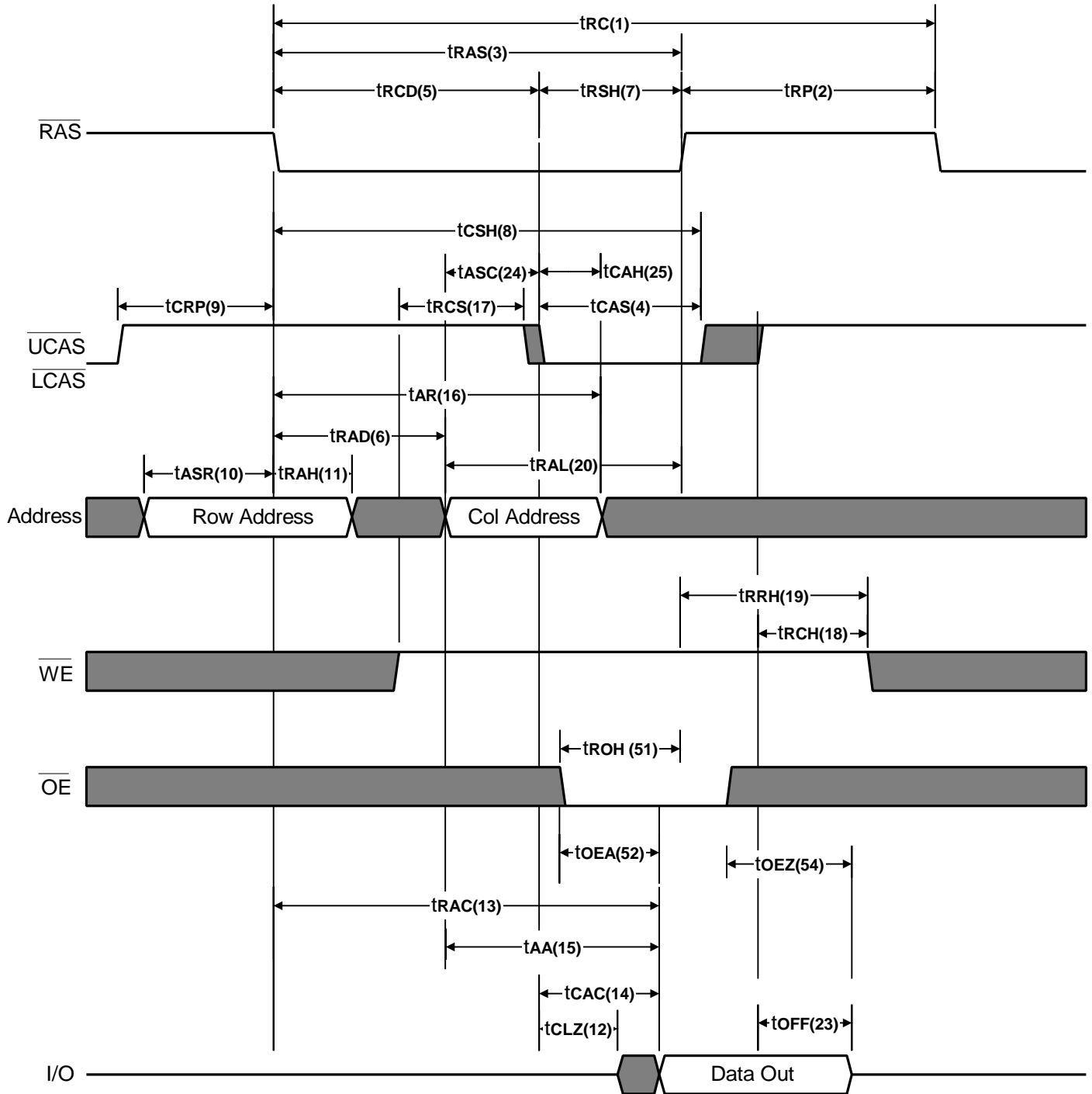
#	JEDEC Symbol	Std Symbol	Parameter	-40		-50		-60		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
42	tAVAV tWL2WL2	tPC	Read-Write Cycle Time (Fast Page)	22	-	31	-	40	-	ns	14
43	tCH2CQV	tCPA	Access Time from $\overline{\text{CAS}}$ Precharge	-	25	-	30	-	35	ns	13
44	tCH2CL2	tCP	$\overline{\text{CAS}}$ Precharge Time (Fast Page)	7	-	8	-	10	-	ns	
45	tCL2CL2	tPCM	FAST PAGE Mode RMW Cycle	55	-	63	-	85	-	ns	
46	tCL2CH2	tCRW	Page Mode $\overline{\text{CAS}}$ Pulse Width (RMW)	45	-	49	-	60	-	ns	
47	tRLRH1	tRASP	$\overline{\text{RAS}}$ Pulse Width	40	125K	50	125K	60	125K	ns	

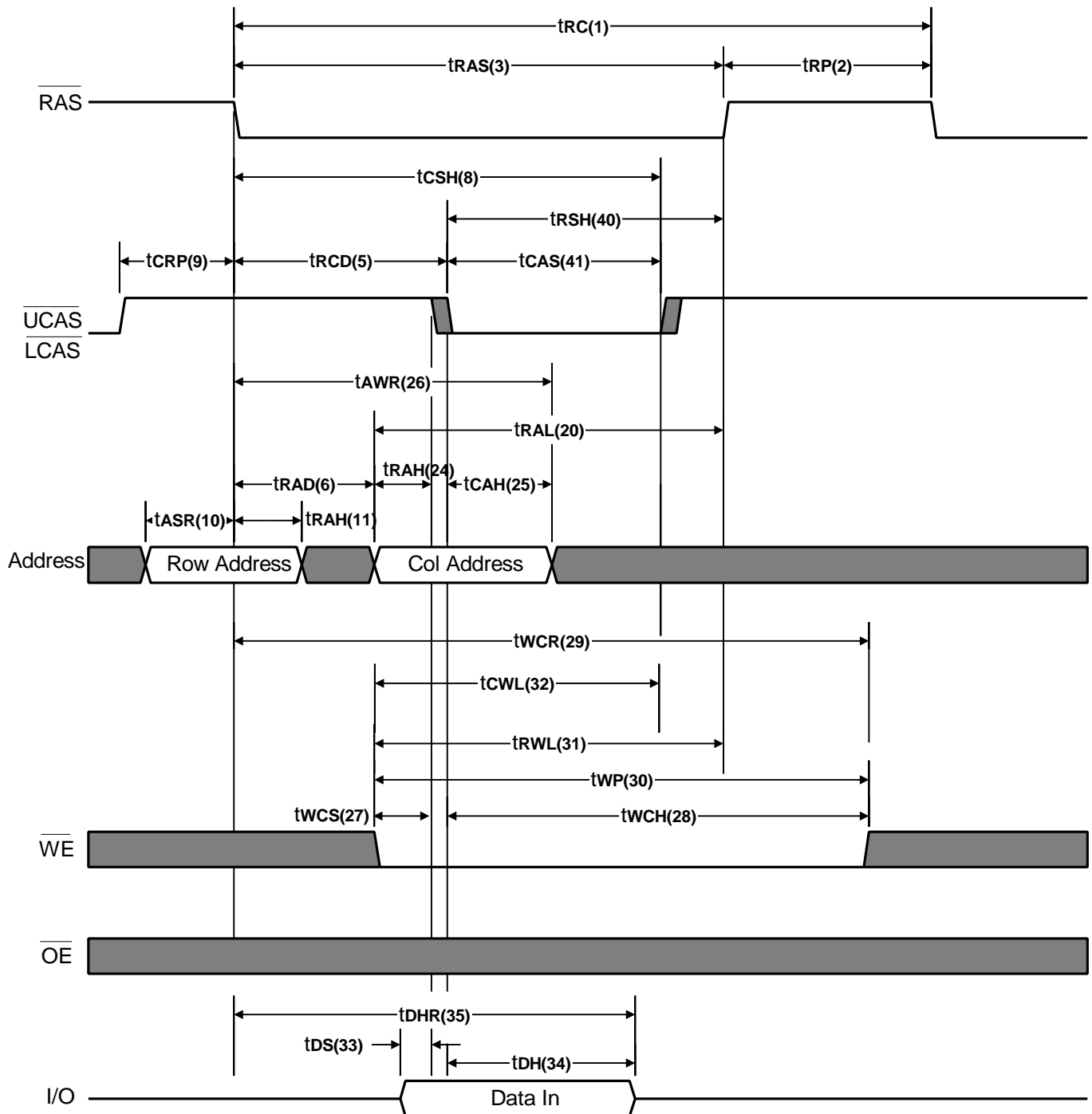
**Refresh Cycle** ( $V_{CC} = 5V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $T_a = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ )

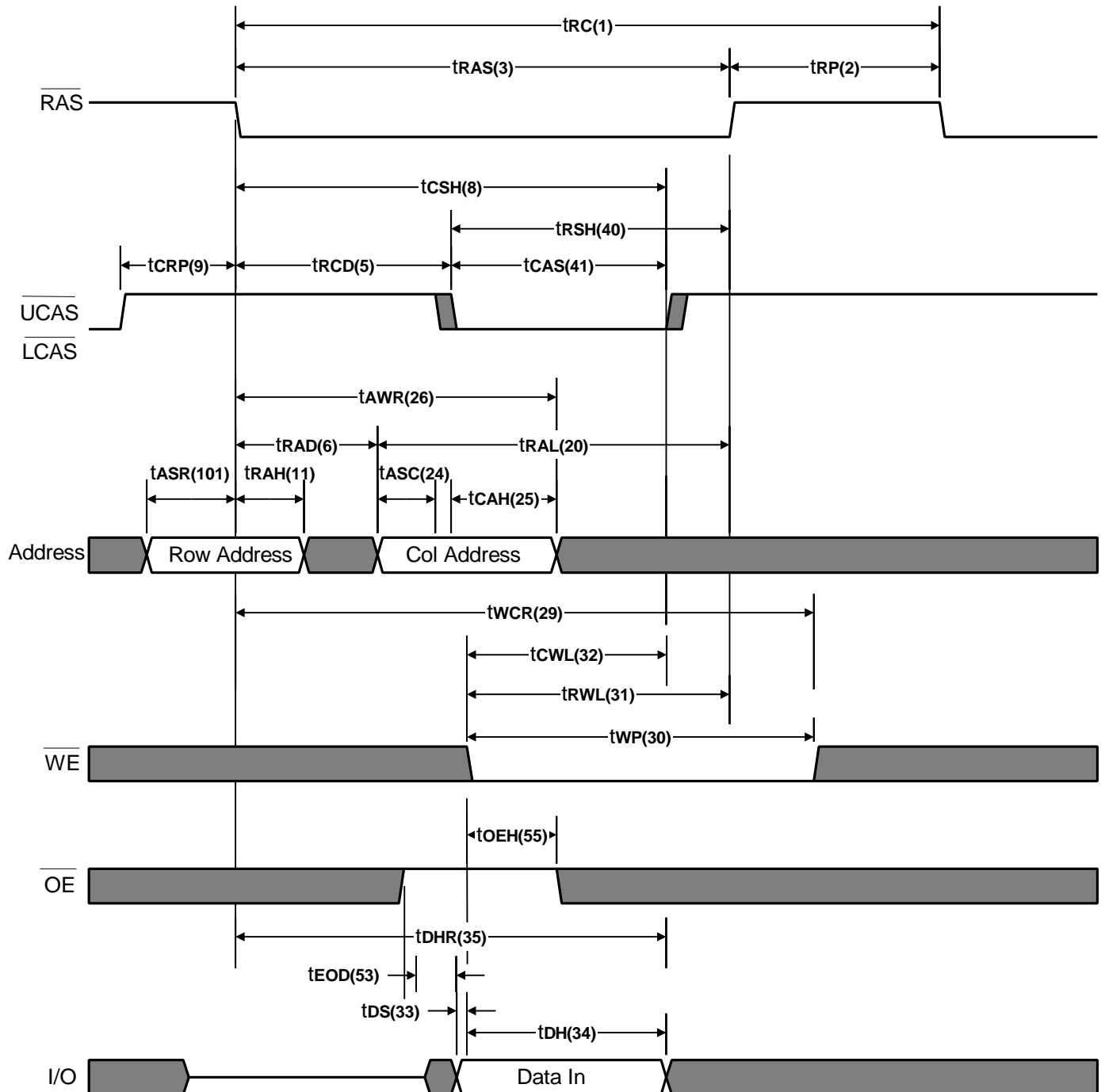
#	JEDEC Symbol	Std Symbol	Parameter	-40		-50		-60		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
48	tCL1RL2	tCSR	$\overline{\text{CAS}}$ Setup Time ( $\overline{\text{CAS}}$ - before- $\overline{\text{RAS}}$ )	5	-	5	-	5	-	ns	3
49	tRL1CH1	tCHR	$\overline{\text{CAS}}$ Hold Time ( $\overline{\text{CAS}}$ - before- $\overline{\text{RAS}}$ )	10	-	10	-	10	-	ns	3
50	tRH2CL2	tRPC	$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Hold Time	5	-	5	-	5	-	ns	
51	tOL1RH1	tROH	$\overline{\text{RAS}}$ Hold Time Reference to $\overline{\text{OE}}$	5	-	5	-	5	-	ns	
52	tOL1QV	tOEA	$\overline{\text{OE}}$ Access Time	-	12	-	13	-	15	ns	
53	tOH2QX	tOED	$\overline{\text{OE}}$ to Data Delay	8	-	10	-	13	-	ns	
54	tOH2QZ	tOEZ	Output Buffer Turn-off Delay from $\overline{\text{OE}}$	0	8	0	10	0	13	ns	8
55	tWL1OL2	tOEH	$\overline{\text{OE}}$ Command Hold Time	0	-	0	-	0	-	ns	

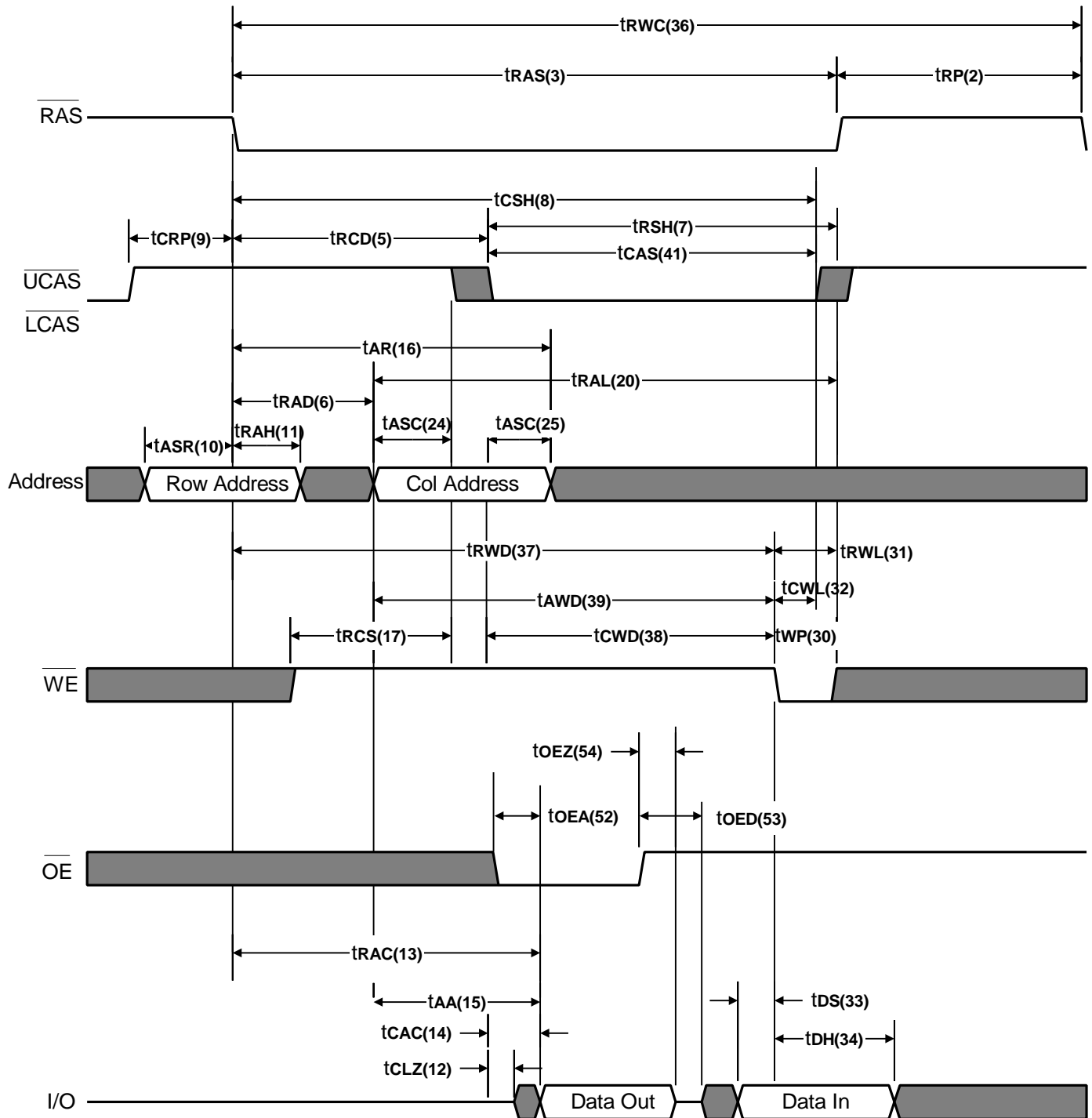
## Notes:

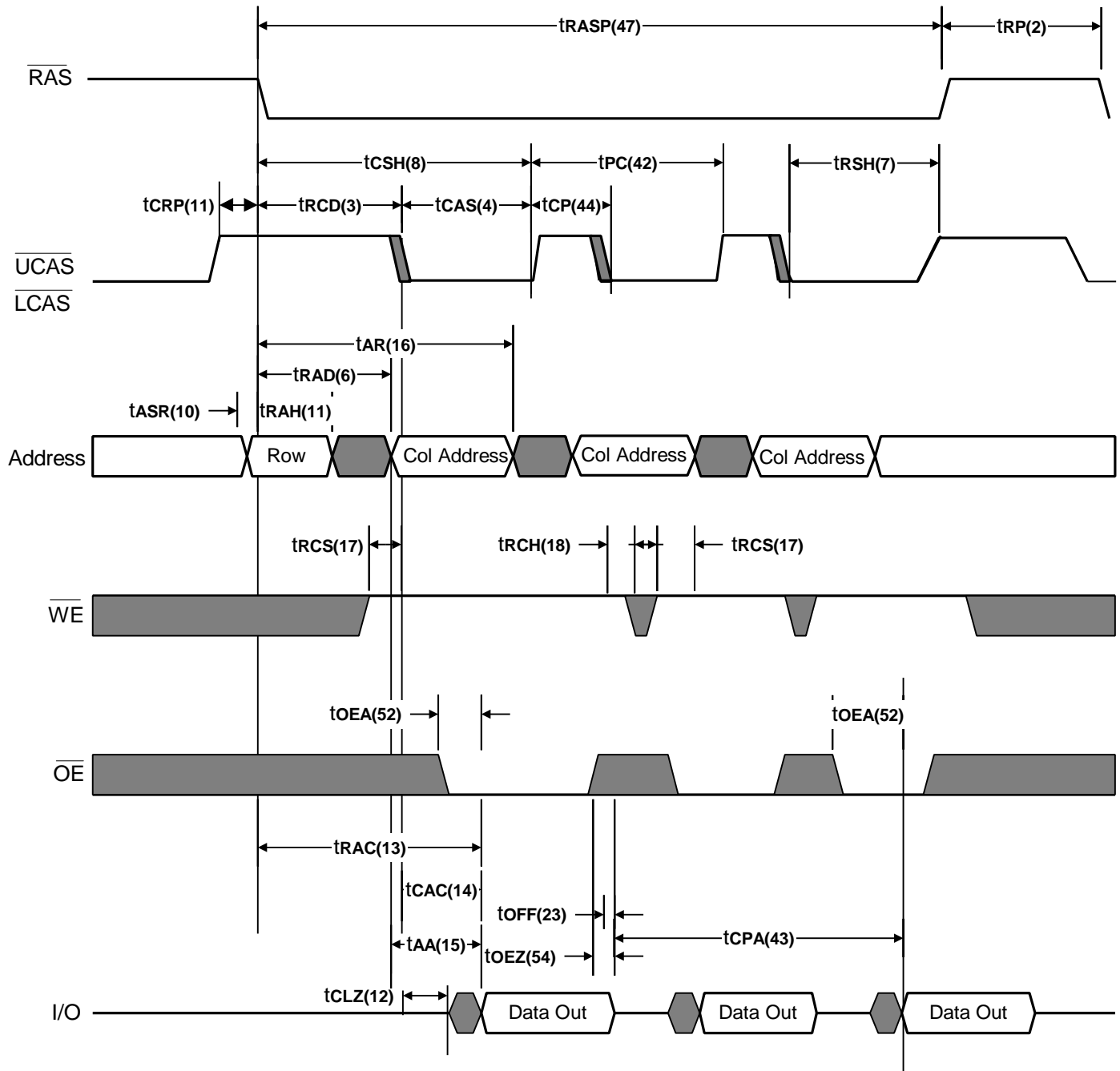
1.  $I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$ , and  $I_{CC6}$  depend on cycle rate.
2.  $I_{CC1}$  and  $I_{CC4}$  depend on output loading. Specified values are obtained with the output open.
3. An initial pause of 200 $\mu$ s is required after power-up followed by any 8  $\overline{\text{RAS}}$  cycles before proper device operation is achieved. In the case of an internal refresh counter, a minimum of 8  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  initialization cycles instead of 8  $\overline{\text{RAS}}$  cycles are required. 8 initialization cycles are required after extended periods of bias without clocks (greater than 8ms).
4. AC Characteristics assume  $t_r = 5\text{ns}$ . All AC parameters are measured with a load equivalent to two TTL loads and 100pF,  $V_{IL}(\text{min.}) \geq \text{GND}$  and  $V_{IH}(\text{max.}) \leq \text{VCC}$ .
5.  $V_{IH}(\text{min.})$  and  $V_{IL}(\text{max.})$  are reference levels for measuring timing of input signals. Transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
6. Operation within the  $t_{RC\overline{D}}$  (max.) limit insures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RC\overline{D}}$  (max.) is specified as a reference point only. If  $t_{RC\overline{D}}$  is greater than the specified  $t_{RC\overline{D}}$  (max.) limit, then access time is controlled exclusively by  $t_{CAC}$ .
7. Operation within the  $t_{RC\overline{D}}$  (max.) limit insures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RAD}(\text{max.})$  is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD}(\text{max.})$  limit, then access time is controlled exclusively by  $t_{AA}$ .
8. Assumes three state test load (5pF and a 380 $\Omega$  Thevenin equivalent).
9. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
10.  $t_{OFF}(\text{max.})$  defines the time at which the output achieves the open circuit condition; it is not referenced to output nvoltage levels.
11.  $t_{WCS}$ ,  $t_{WCH}$ ,  $t_{RWD}$ ,  $t_{CWD}$  and  $t_{AWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}(\text{min.})$  and  $t_{WCH} \geq t_{WCH}(\text{min.})$ , the cycle is an early write cycle and data out pins will remain open circuit, high impedance, throughout the cycle. If  $t_{RWD} \geq t_{RWD}(\text{min.})$ ,  $t_{CWD} \geq t_{CWD}(\text{min.})$  and  $t_{AWD} \geq t_{AWD}(\text{min.})$ , the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is satisfied, the condition of the data out at access time is indeterminate.
12. These parameters are referenced to  $\overline{\text{UCAS}}$  and  $\overline{\text{LCAS}}$  leading edge in early write cycles and to  $\overline{\text{WE}}$  leading edge in read-write cycles.
13. Access time is determined by the longest of  $t_{AA}$  or  $t_{CAC}$  or  $t_{CAP}$ .
14.  $t_{ASC} \geq t_{CP}$  to achieve  $t_{PC}(\text{min.})$  and  $t_{CAP}(\text{max.})$  values.
15. These parameters are sampled and not 100% tested.

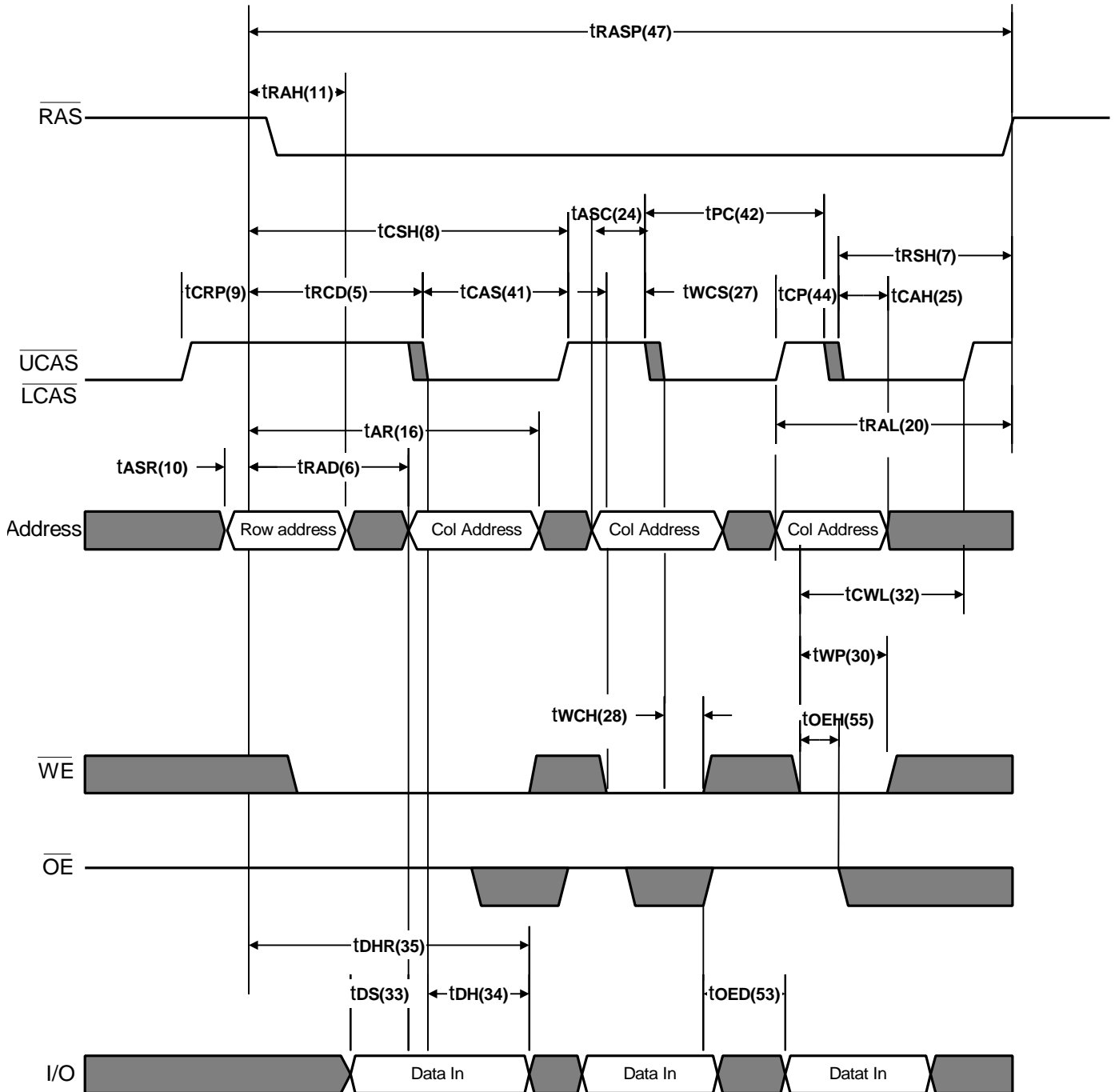
**Timing Waveform of Read Cycle**


**Timing Waveform of Early Write Cycle**


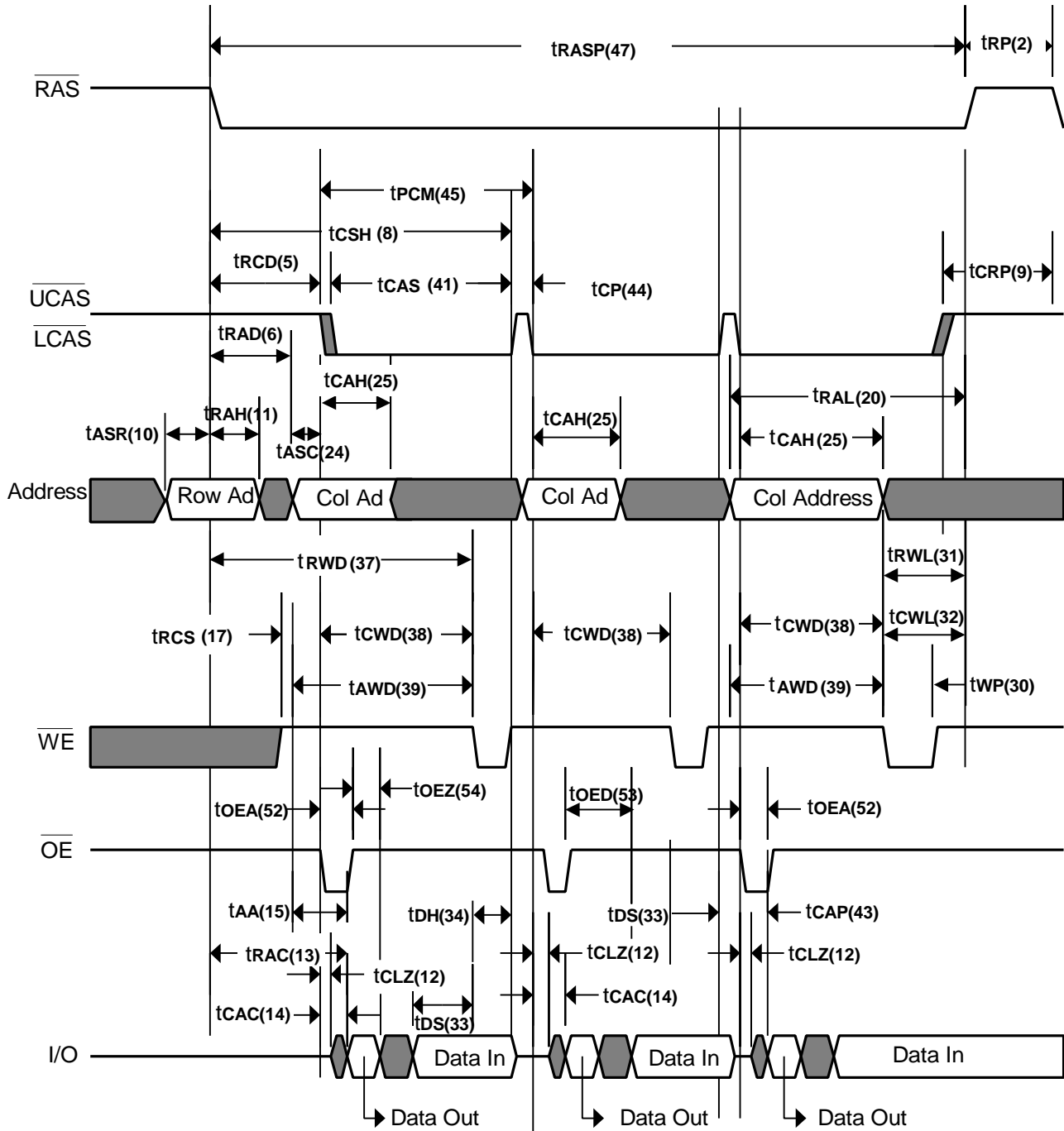
**Timing Waveform of Late Write Cycle**


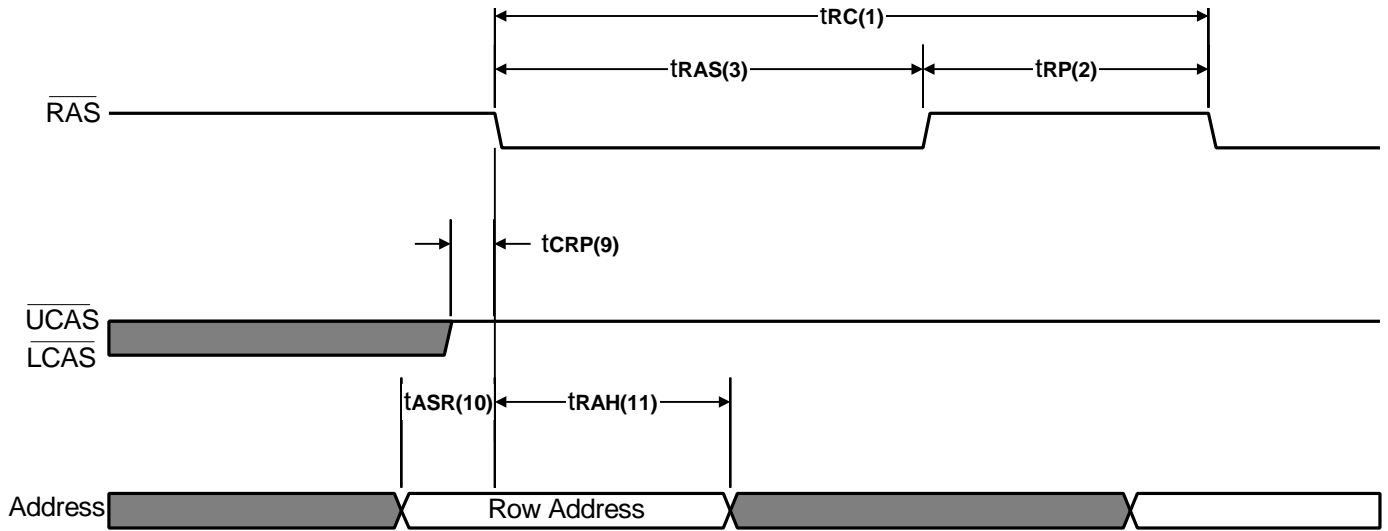
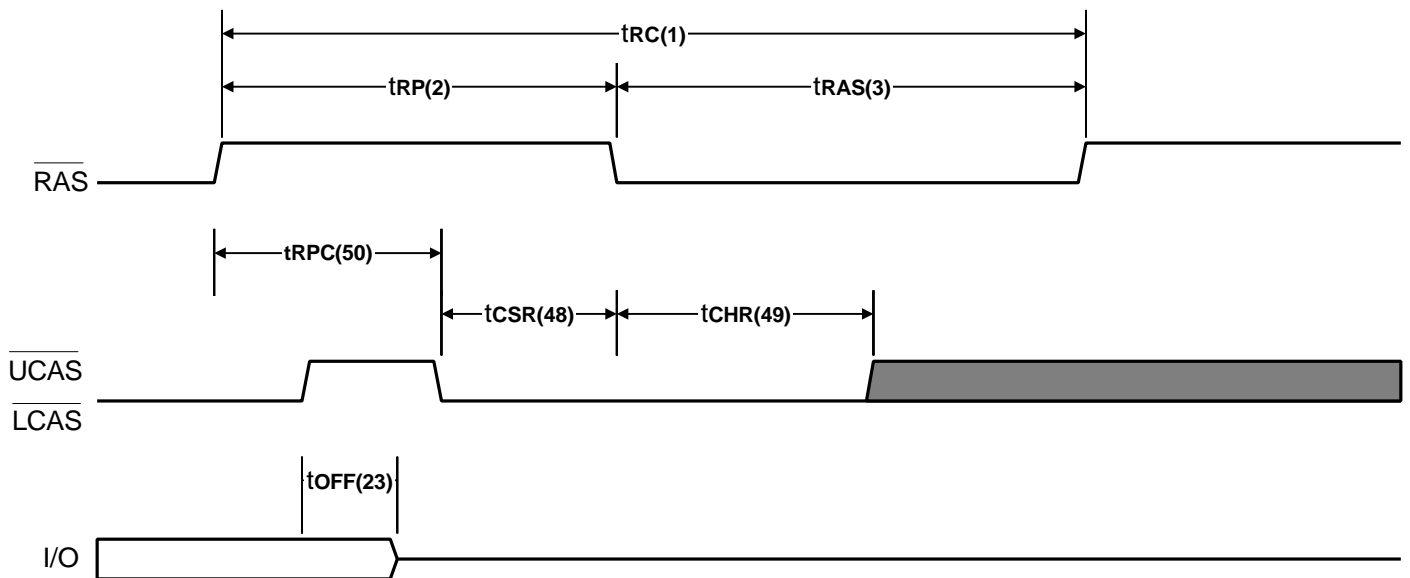
**Timing Waveform of Read-Modify-Write Cycle**


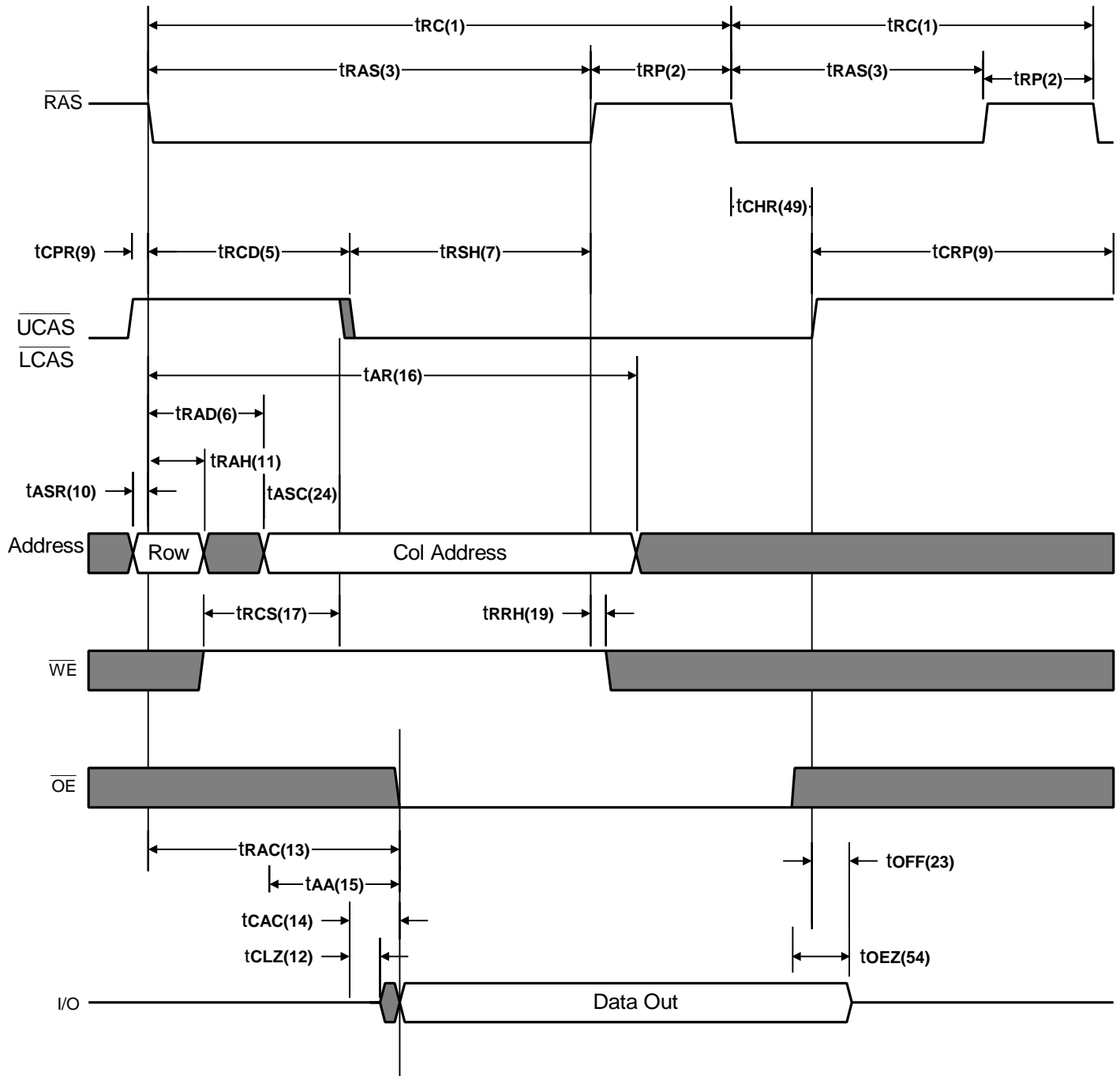
**Timing Waveform of Fast Page Mode Read Cycle**


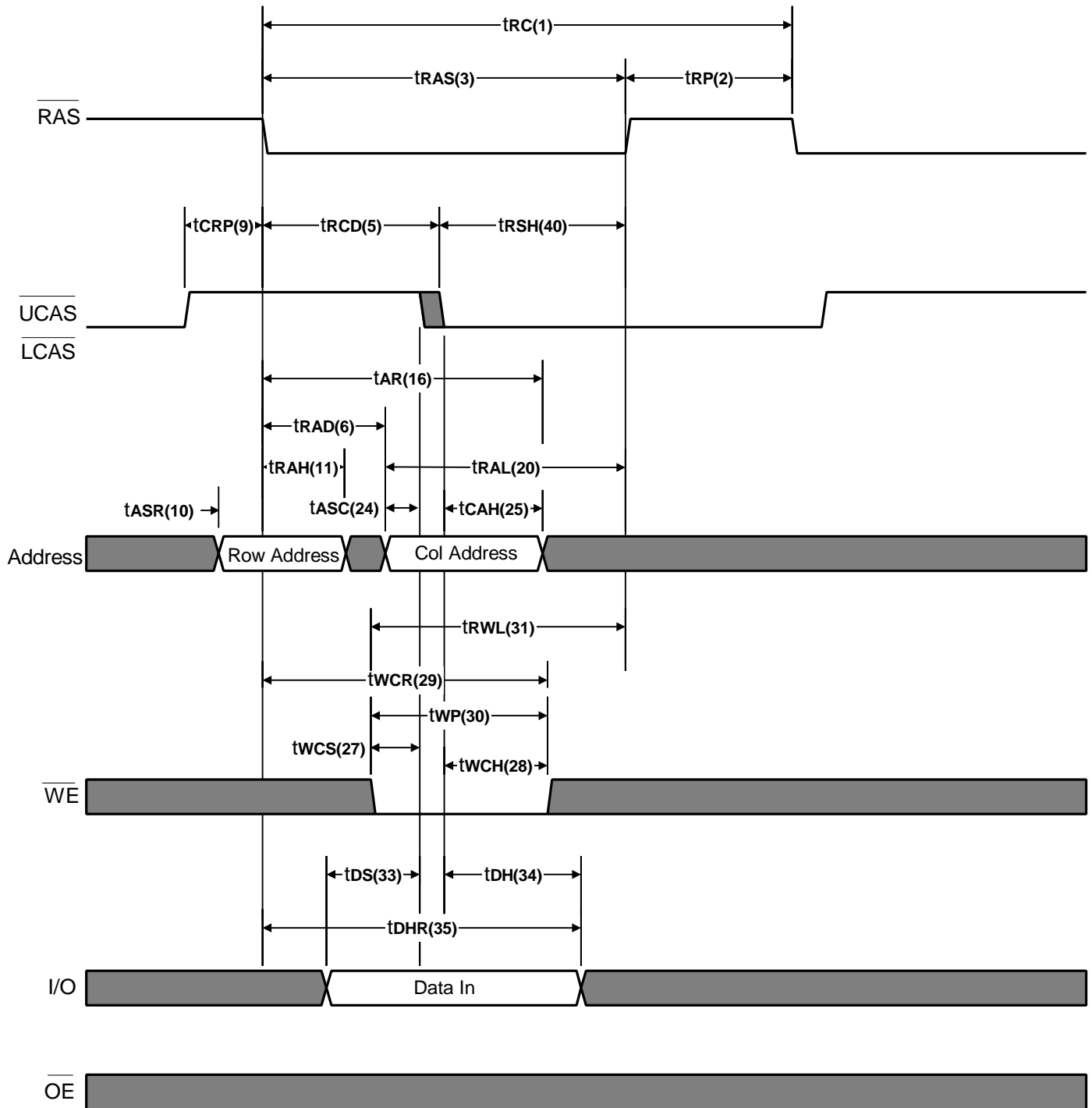
**Timing Waveform of Fast Page Mode Early Write Cycle**




**Timing Waveform of Fast Page Mode Read-Modify-Write Cycle**


**Timing Waveform of  $\overline{\text{RAS}}$  Only Refresh Cycle**

**Timing Waveform of CAS-before-RAS Refresh Cycle**


**Timing Waveform of Hidden Refresh Cycle (Read)**


**Timing Waveform of Hidden Refresh Cycle (Write)**


**Capacitance**<sup>15</sup> (f = 1MHz, Ta = Room Temperature, VCC = 5V ± 10%)

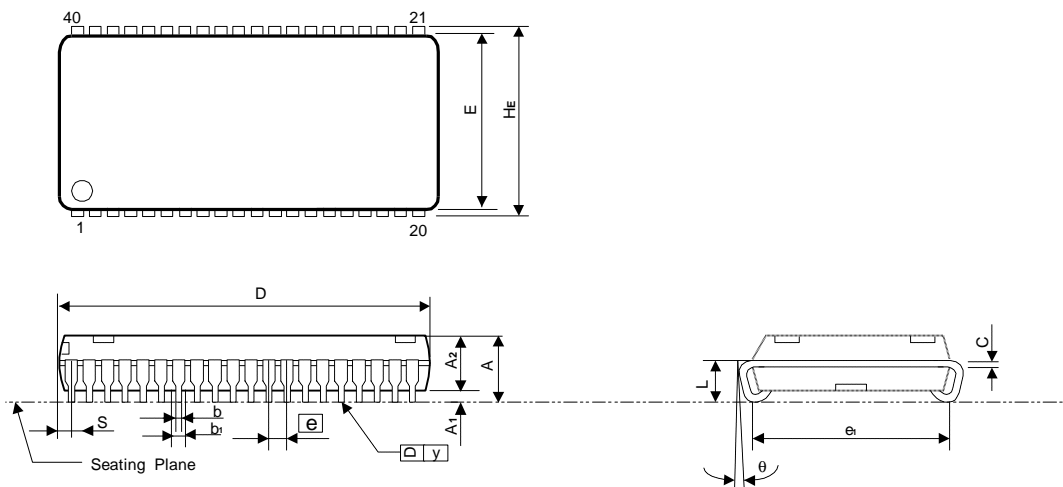
Symbol	Signals	Parameter	Max.	Unit	Test Conditions
C <sub>IN1</sub>	A0 – A7	Input Capacitance	5	pF	V <sub>in</sub> = 0V
C <sub>IN2</sub>	$\overline{\text{RAS}}$ , $\overline{\text{UCAS}}$ , $\overline{\text{LCAS}}$ , $\overline{\text{WE}}$ , $\overline{\text{OE}}$		7	pF	V <sub>in</sub> = 0V
C <sub>I/O</sub>	I/O <sub>1</sub> - I/O <sub>16</sub>	I/O Capacitance	7	pF	V <sub>in</sub> = V <sub>out</sub> = 0V

**Ordering Codes**

Package \ $\overline{\text{RAS}}$ Access Time	40ns	50ns	60ns
40L SOJ (400 mil)	A416316S-40	A416316S-50	A416316S-60
40/44L TSOP type II (400mil)	A416316V-40	A416316V-50	A416316V-60

**Package Information**
**SOJ 40L Outline Dimensions**

unit: inches/mm



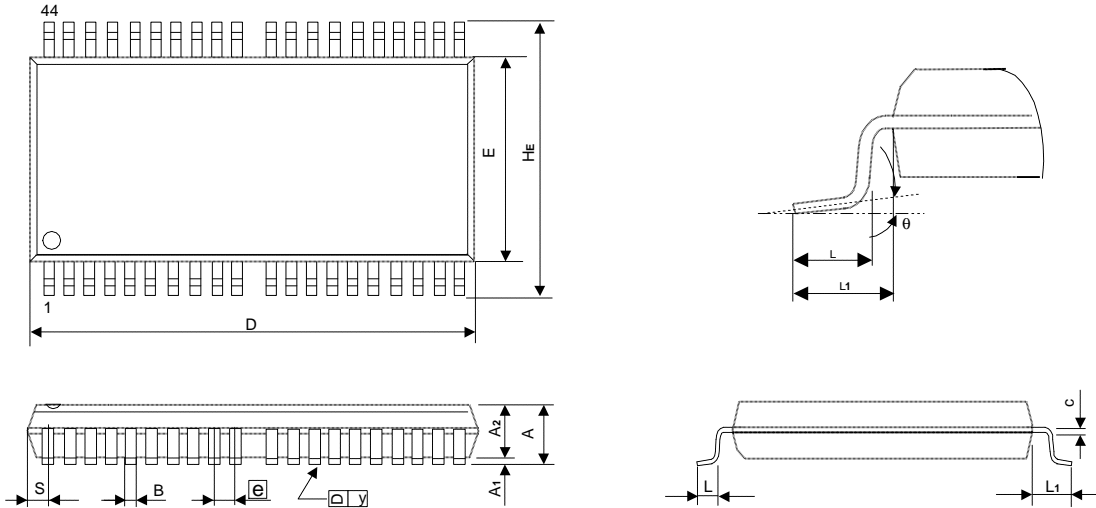
Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.144	-	-	3.66
A1	0.025	-	-	0.64	-	-
A2	0.105	0.110	0.115	2.67	2.79	2.92
b1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.022	0.41	0.46	0.56
C	0.008	0.010	0.014	0.20	0.25	0.36
D	1.020	1.025	1.030	25.91	26.04	26.16
E	0.395	0.400	0.405	10.03	10.16	10.29
e1	0.044	0.050	0.056	1.12	1.27	1.42
e1	0.355	0.366	0.376	9.114	9.383	9.652
HE	0.430	0.440	0.450	10.92	11.18	11.43
L	0.081	0.093	0.105	2.083	2.39	2.70
S	-	-	0.050	-	-	1.27
y	-	-	0.004	-	-	0.10
theta	0°	-	10°	0°	-	10°

**Notes:**

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension e1 is for PC Board surface mount pad pitch design reference only.
4. Dimension S includes end flash.

**Package Information**
**TSOP 40/44L (Type II) Outline Dimensions**

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.047	-	-	1.20
A1	0.002	-	0.006	0.05	-	0.15
A2	0.037	0.039	0.041	0.95	1.00	1.05
B	0.013	0.015	0.017	0.32	0.37	0.42
c	0.003	0.005	0.009	0.08	0.13	0.23
D	0.720	0.725	0.730	18.28	18.41	18.54
E	0.395	0.400	0.405	10.03	10.16	10.29
e	0.031 BSC			0.80 BSC		
HE	0.455	0.463	0.471	11.56	11.76	11.96
L	0.016	0.020	0.024	0.40	0.50	0.60
L1	-	0.031	-	-	0.80	-
S	-	-	0.035	-	-	0.90
y	-	-	0.004	-	-	0.10
θ	1°	3°	5°	1°	3°	5°

**Notes:**

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension S includes end flash.