CHIPS

PRELIMINARY

T-52-33-05

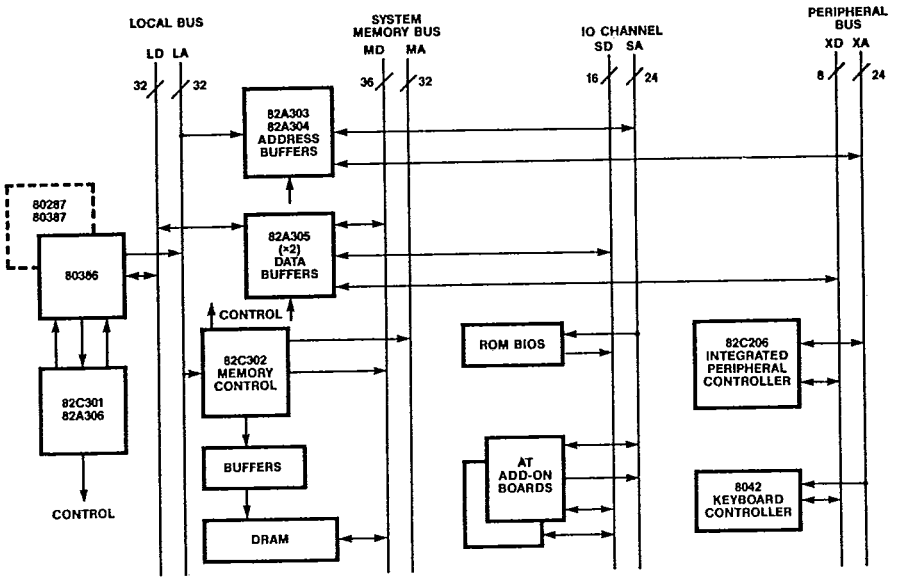
82C301, 82C302, 82A303, 82A304, 82A305, 82A306
CS8230: AT/386 CHIPSet™

- 100% IBM™ PC AT compatible
- Flexible architecture allows usage in any iAPX 386™ design
- Operates in Page mode with Interleave memory subsystem
- 16 MHz zero wait operation using 100ns DRAMs
- Independent clock to support correct AT bus timing
- 1MB to 16MB of DRAM memory support
- A complete PC AT requires only 40 IC's plus memory

The CS8230 AT/386 CHIPSet™ is a seven chip VLSI implementation of most of the system logic to control an iAPX 386 based system. The CHIPSet is designed to offer a 100% PC AT compatible integrated solution. The flexible architecture of the CHIPSet allows it to be used in any iAPX386 based system design, such as CAD/CAE workstations, office systems, industrial and financial transaction systems.

CS8230 CHIPSet combined with CHIPs 82C206, Integrated Peripherals Controller, provides a complete PC AT compatible system using only 40 components plus memory devices.

The CS8230 CHIPSet™ consists of one 82C301 Bus Controller, one 82C302 Page/Interleave Memory Controller, one each of 82A303 and 82A304 Address Bus Interfaces, two 82A305



AT/386 System Block Diagram

Data Bus Interfaces, and a 82A306 Control Signal Buffer. An all CMOS CS8232-16 CHIPSet allow OEM's to reduce the form factor, size and weight of their portable, laptop machines due to the reduced power requirements, the reduced cooling requirements and the reduced buffering requirements of the CHIPSet. In particular, the all CMOS CS8232-16 CHIPSet will reduce a system's power consumption requirement by at least half that of an NMOS/BIPOLAR/CMOS based system.

The only difference between the CS8232-16 CHIPSet and the CS8230-16 CHIPSet is that the bipolar parts (82A303, 82A304, 82A305, 82A306) in the CS8230 CHIPSet have been replaced with CMOS parts (82C303, 82C304, 82C305, 82C306). The difference between the new CMOS parts is that the drive capability is 12 mamps as opposed 24 mamps in the bipolar parts. Additionally I_{CC} is 20 amps (worst case) with no loading (infinite impedance) and steady state current is 100μA for the new CMOS device.

The CHIPSet supports a local CPU bus, a 32-bit system memory bus, and AT buses as shown in the system diagram below. The 82C301 and 82A306/82C306 provide the generation and synchronization of control signals for all buses. The 82C301 also supports an independent AT bus clock, and allows for dynamic selection of the processor clock between the 16 MHz clock and the AT bus clock. The 82A306 provides buffers for bus control signal in addition to other miscellaneous logic functions.

The 82C302 Page/Interleave Memory Controller provides an interleaved memory subsystem design with page mode operation. It supports 1 MB to 16 MB of DRAMs with combinations of 256Kbit and 1Mbit DRAMs. The processor can operate at 16 MHz with zero wait state memory accesses by using 100 nsec DRAMs, or at 20 MHz with zero wait state memory access using 85ns static column DRAMs (t_{CAC} = 35ns) or using 75ns page mode DRAMs (t_{CAC} = 35ns).

The 82A303/82C303 and 82A304/82C304 interface between all address buses and the addresses needed for proper data path conversion. Two 82A305/82C305 are used to interface between the local, system memory, and AT data buses. In addition to having high current drive, they also perform the conversion necessary between the different sized data paths.

System Overview

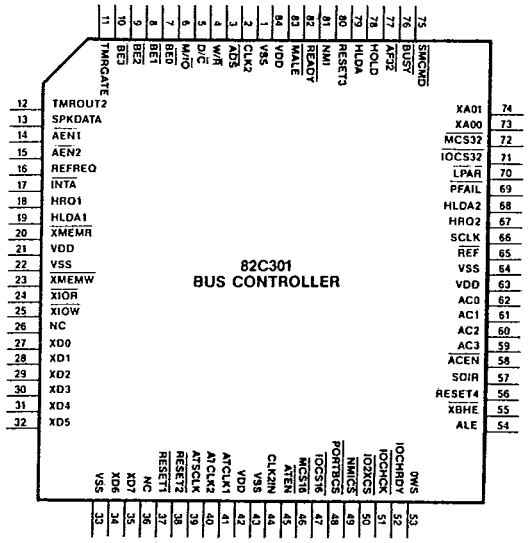
The CS 8230 is designed for use in 80386-based systems and provides complete support for the IBM PC AT bus. There are four buses supported by the CS 8230 as shown in the AT/386 system block diagram: the CPU local bus (A and D), the system memory bus (MA and MD), the IO Channel bus (SA and SD), and the X bus (XA and XD). The system memory bus is used to interface to DRAM's controlled by the 82C302. The IO channel bus refers to the bus supporting the AT bus adapters which could be either a 8 bit devices or 16 bit devices. The X bus refers to the peripheral bus to which the DMA controllers and timers are attached in an IBM PC AT. The X bus has only an 8-bit data path. The term "AT bus" is used to refer to the IO channel bus and X bus. Provisions are also made for user extension of the IO channel to a 32 bit bus.

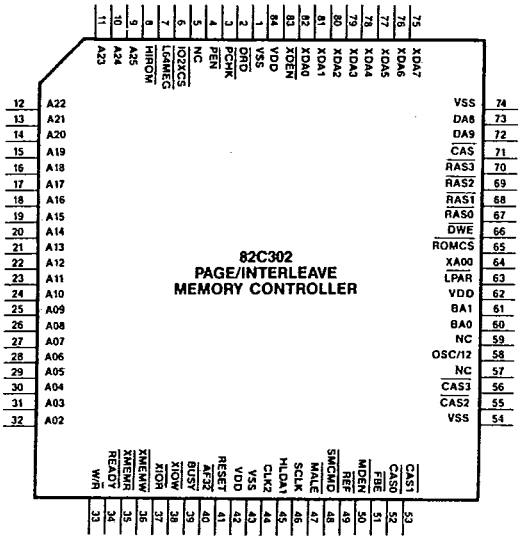
Notations and Glossary

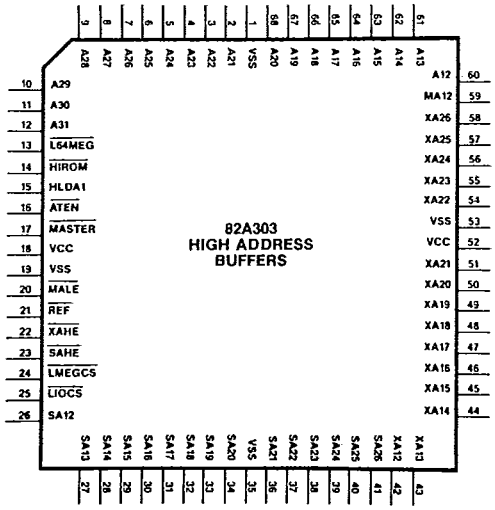
The following notations are used to refer to the configuration and diagnostic registers internal to the 82C301 and 82C302.

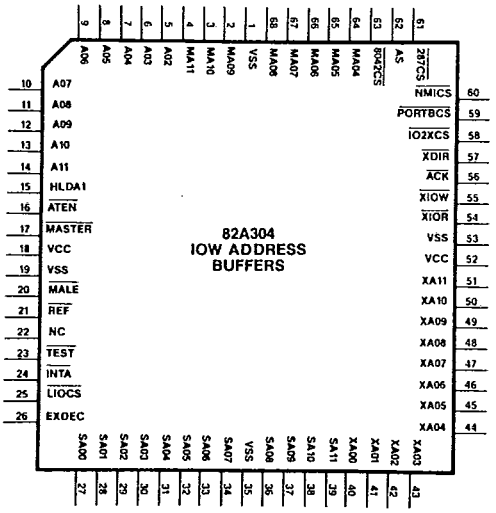
REGnH denotes the internal register with the index n in hexadecimal notation.

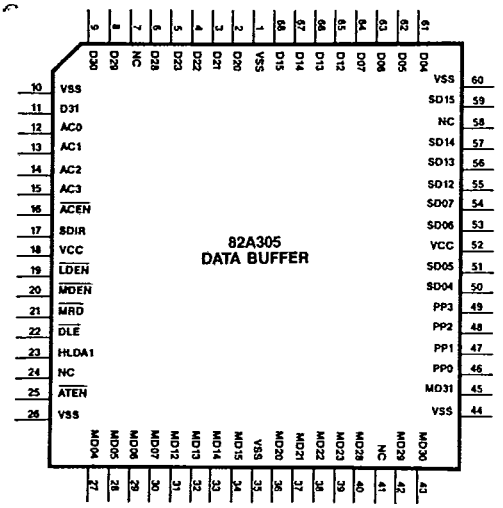
REGnH<x:y> denotes the bit field from bits y to x of the internal register with the index n in hexadecimal notation.

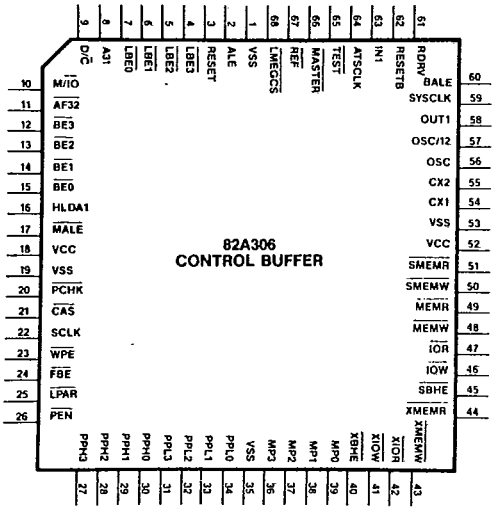

82C301
BUS CONTROLLER
TMRGATE 11
BE3 10
BE2 9
BE1 8
BE0 7
D/C 6
M/IO 5
W/R 4
ADS 3
CLK2 2
VSS 1
VDD 84
MALE 83
READY 82
NMI 81
RESET3 80
HLDA 79
HOLD 78
AF/32 77
BUSY 76
SMCMD 75
TMROUT2 12
SPKDATA 13
AEN1 14
AEN2 15
REFREQ 16
INTA 17
HRQ1 18
HLDA1 19
XMEMR 20
VDD 21
VSS 22
XMEMW 23
XIOR 24
XIOW 25
NC 26
XD0 27
XD1 28
XD2 29
XD3 30
XD4 31
XD5 32
VSS 33
XD6 34
XD7 35
NC 36
RESET1 37
RESET2 38
ATSCLK 39
ATCLK2 40
ATCLK1 41
VDD 42
VSS 43
CLK2IN 44
ATEN 45
MCS16 46
IOCS16 47
PORTBCS 48
NMICS 49
IO2XCS 50
IOCHCK 51
IOCHRDY 52
0WS 53
ALE 54
XBHE 55
RESET4 56
SDIR 57
ACEN 58
AC3 59
AC2 60
AC1 61
AC0 62
VDD 63
VSS 64
REF 65
SCLK 66
HRQ2 67
HLDA2 68
PFAIL 69
LPAR 70
IOCS32 71
MCS32 72
XA00 73
XA01 74


82C302
PAGE/INTERLEAVE
MEMORY CONTROLLER
A23 11
A24 10
A25 9
HIROM 8
LGAMECG 7
IO2XCS 6
NC 5
PEN 4
PCHK 3
DRD 2
XDEN 1
VDD 84
XDA0 83
XDA1 82
XDA2 81
XDA3 80
XDA4 79
XDA5 78
XDA6 77
XDA7 76
A22 12
A21 13
A20 14
A19 15
A18 16
A17 17
A16 18
A15 19
A14 20
A13 21
A12 22
A11 23
A10 24
A09 25
A08 26
A07 27
A06 28
A05 29
A04 30
A03 31
A02 32
WR 33
READY 34
XMEMR 35
XMEMW 36
XIOR 37
XIOW 38
BUSY 39
AF/32 40
RESET 41
VDD 42
VSS 43
CLK2 44
HLDA1 45
SCLK 46
MALE 47
SMCMD 48
REF 49
MDEN 50
FBE 51
CAS0 52
CAS1 53
VSS 54
CAS2 55
CAS3 56
NC 57
OSC/12 58
NC 59
BA0 60
BA1 61
VDD 62
LPAR 63
XA00 64
ROMCS 65
DWE 66
RAS0 67
RAS1 68
RAS2 69
RAS3 70
CAS 71
DA9 72
DA8 73
VSS 74


82A303
HIGH ADDRESS
BUFFERS


82A304
IOW ADDRESS
BUFFERS


82A305
DATA BUFFER


82A306
CONTROL BUFFER

82C301 Pin Description

Pin No.	Symbol	Pin Type	Description
Clocks			
44	CLK2IN	I	CLOCK 2 INPUT from a packaged TTL crystal oscillator having twice the rated frequency of the processor.
2	CLK2	O	CLK2 output to the Clock 2 input of 80386 and the memory controller. This clock output is derived from 82C302 CLK2IN and has a 50% duty cycle. The clock can also be programmed to be the same as the BCLK.
66	SCLK	O	SCLK is CLK2 divided by two and is an output generated as a reference to verify the phase relationship of the internal clock and CLK2.
41	ATCLK1	I	BUS CLOCK INPUT source from Crystal or Oscillator. This clock input is used for the AT Bus operation and is required only if the AT bus state machine clock (BCLK) will not be derived from the CLK2 input. This signal should be tied low if not used. Its frequency should be lower than CLK2IN.
40	ATCLK2	O	BUS CLOCK CRYSTAL OUTPUT is connected to the crystal oscillator circuit if a packaged oscillator is not used. A series resistor of 10Ω should be used to reduce the amplitude of the resonant circuit. It should be left unconnected if a packaged TTL oscillator is used.
39	ATSCLK	O	AT SYSTEM CLOCK is buffered to drive the clock signal SYSCLK on the AT bus I/O channel. It is half the frequency of BCLK and should have a nominal value in the range of 6 to 8 MHz for maintaining correct AT I/O bus timing with IBM PC AT.
Control			
37	$\overline{\text{RESET1}}$	I	$\overline{\text{RESET1}}$ is an active low input generated by the POWER GOOD signal of the power supply. When low, it activates RESET3 and RESET4. $\overline{\text{RESET1}}$ is latched internally.
38	$\overline{\text{RESET2}}$	I	Active low. $\overline{\text{RESET2}}$ (8042RC) is an active low signal generated from the keyboard controller 8042 for a "warm reset" not requiring the system power to be shut off. It forces a CPU reset by activating the RESET3 signal.
56	RESET4	O	RESET4 is an active high output used to reset the AT Bus, the 82C206 IPC, the 8042 keyboard controller and the 82C302 or 82C312 memory controller. RESET4 is synchronized with the processor clock.

82C301 Pin Description (Continued)

Pin No.	Symbol	Pin Type	Description
CPU Interface			
80	RESET3	O	RESET3 is an active high output to the 80386 and the 80387 when either RESET1 or RESET2 is active. It is also activated when a shutdown condition in the CPU is detected. RESET3 will stay active for at least 78 CLK2 cycles.
82	READY	I/O	READY is an output during AT bus cycles (AF32 high), and is driven low to terminate the current CPU cycle after detecting IOCHRDY high and 0WS high or if a "time out" condition is detected. It is an open collector output requiring an external pull-up resistor of 1 KOhm. During all other cycles (AF32 low), it is an input (from the 82C302 and any other 32 bit memory controller), and has to be driven low to terminate the current CPU access. It is connected to the READY input of the 80386 processor.
3	ADS	I	Active low. ADDRESS STROBE input connected to the 80386 ADS pin. A 10KΩ pullup resistor is recommended.
4	W/R	I/O	READ/WRITE STATUS input from the 80386 W/R signal. It indicates a write bus cycle if it is high and a read cycle if it is low. A 10KΩ pull-up resistor is recommended.
5	D/C	I	DATA/CONTROL STATUS input from the 80386 D/C signal. A 10KΩ pull-up resistor is recommended.
6	M/IO	I	MEMORY/IO STATUS input from the 80386 M/IO signal. A 10KΩ pull-up resistor is recommended.
78	HOLD	O	Active high. HOLD REQUEST output to the 80386 HOLD input pin. This signal is used to request the CPU to relinquish the bus to another requesting master on HRQ1, HRQ2 or REFREQ.
79	HLDA	I	Active high. HOLD ACKNOWLEDGE input connected to processor HLDA signal. When the signal is HIGH it indicates that the processor has relinquished the system bus in response to the HOLD request. When active, it forces all commands (IOR, IOW, MEMR, MEMW, INTA) to be tri-stated.
10-7	BE<3:0>	I/O	Active low. BYTE ENABLE signals input from the 80386 BE<3:0> during a CPU cycle. BE3 controls the most significant byte while BE0 controls the least significant byte. BE<3:0> are generated by 82C301 during DMA cycles based on the status signals XA0, XA1 and XBHE
81	NMI	O	Active HI. NON-MASKABLE INTERRUPT connects to the 80386 NMI pin and is generated by 82C301 to cause an NMI.

82C301 Pin Description (Continued)

Pin No.	Symbol	Pin Type	Description
Decodes			
48	$\overline{\text{PORTBCS}}$	I	Active low. PORT B CHIP SELECT is the address decode input from the 82A304 as enable for the Port B register at address 061H.
49	$\overline{\text{NMICS}}$	I	Active low. NMI CHIP SELECT is the address decode input from the 82A304 as enable for the NMI enable bit at address 070H.
50	$\overline{\text{IO2XCS}}$	I	Active low. IO2X CHIP SELECT is the address decode input from the 82A304 as chip select for the IO registers at 022H and 023H used to access the 82C301 internal configuration registers.
IO Channel Interface			
53	$\overline{\text{0WS}}$	I	ZERO WAIT STATE (0WS) is an active low input from the AT bus, causing termination of the AT bus cycle. 16-bit Memory/I/O cards residing on the AT expansion bus use this line to speed up accesses. It requires a 330Ω pull-up resistor.
52	IOCHRDY	I	Active high. IO CHANNEL READY input from the AT bus. When lowW it indicates a 'not ready' condition and forces the insertion of wait states in I/O or memory accesses. When HIGH it will allow the completion of the current memory or I/O access.
51	$\overline{\text{IOCHCK}}$	I	Active low. IO CHANNEL CHECK input from the AT bus which causes an NMI to be generated if enabled. It is used to signal an Error condition from a device residing on the AT bus. A 10KΩ pull-up resistor is recommended.
70	$\overline{\text{LPAR}}$	I	Active low. PARITY ERROR input from local memory system which causes an NMI to be generated if enabled.
69	$\overline{\text{PFAIL}}$	I	Active low. POWER FAIL WARNING signal input from the power supply.
54	ALE	O	Active high. ADDRESS LATCH ENABLE to AT bus. This signal controls the address latches used to hold the address during a bus cycle. The signal should be buffered to drive the AT bus.
DMA Interface			
19	HLDA1	O	Active high. HOLD ACKNOWLEDGE 1 is active when a bus cycle is granted in response to HRQ1.
68	HLDA2	O	Active high. HOLD ACKNOWLEDGE 2 is active when a bus cycle is granted in response to HRQ2.

82C301 Pin Description (Continued)

Pin No.	Symbol	Pin Type	Description
18	HRQ1	I	Active high. HOLD REQUEST 1 is active when a DMA/ Master is requesting a bus cycle. For an AT compatible architecture it should be connected to the HOLD REQUEST signal from DHA1 and DMA2.
67	HRQ2	I	Active high. HOLD REQUEST 2 is active when a DMA/ Master is requesting a bus cycle. This should be grounded if not used.
14	$\overline{\text{AEN1}}$	I	ADDRESS ENABLE 1 is an active low input from one of the two DMA controllers enabling the address latches for 8 bit DMA transfers.
15	$\overline{\text{AEN2}}$	I	ADDRESS ENABLE 2 is an active low input from one of the two DMA controllers enabling the address latches for 16 bit DMA transfers.
Control Strobes			
46	$\overline{\text{MCS16}}$	I	Active low. $\overline{\text{MCS16}}$ When active causes 16 bit memory accesses on IO channel. If $\overline{\text{MEMCS32}}$ and $\overline{\text{MEMCS16}}$ are both high it implies a 8 bit memory transfer. A pull-up resistor of 330Ω is recommended.
72	$\overline{\text{MCS32}}$	I	Active low. $\overline{\text{MCS32}}$ when active causes 32 bit memory accesses on IO channel.
47	$\overline{\text{IOCS16}}$	I	Active low. $\overline{\text{IOCS16}}$ when active causes 16 bit IO accesses on IO channel. If $\overline{\text{IOCS32}}$ and $\overline{\text{IOCS16}}$ are both high, it implies a 8 bit I/O transfer. A pull-up resistor of 330Ω is recommended.
71	$\overline{\text{IOCS32}}$	I	Active low. $\overline{\text{IOCS32}}$ when active causes 32 bit IO accesses on IO channel.
75	$\overline{\text{SMCMD}}$	O	Active low. SYSTEM MEMORY COMMAND when active indicates the current access cycle is a memory cycle.
Refresh			
16	REFREQ	I	Active high. REFresh REQuest when active initiates a DRAM refresh sequence. It is generated by the 8254 compatible timer controller #1 of the 82C206 IPC in a PC/AT implementation.
65	$\overline{\text{REF}}$	I/O	Active low. REFresh is open drain signal. It initiates a refresh cycle for the DRAMs. As an input it can be used to force a refresh cycle from an I/O device. An external pull up of 620Ω is required.

82C301 Pin Description (Continued)

Pin No.	Symbol	Pin Type	Description
X Bus Interface			
20	$\overline{\text{XMEMR}}$	I/O	X BUS MEMORY READ is an active low control strobe directing memory to place valid data on the data bus. It is an output if the CPU is controlling the bus. It is an input if a DMA controller is in control of the bus.
23	$\overline{\text{XMEMW}}$	I/O	X BUS MEMORY WRITE is an active low control strobe directing memory to accept data from the data bus. It is an output if the CPU is controlling the bus and is an input if a DMA controller is in control of the bus.
24	$\overline{\text{XIOR}}$	I/O	X BUS I/O READ is an active low strobe directing an I/O device to place data on the data bus. It is an output if the CPU is controlling the bus or an input if a DMA controller is in control of the bus.
25	$\overline{\text{XIOW}}$	I/O	X BUS I/O WRITE is an active low strobe directing an I/O device to accept data from the data bus. It is an output if the CPU is controlling the bus or an input if a DMA controller is in control of the bus.
55	$\overline{\text{XBHE}}$	I/O	X BYTE HIGH ENABLE is an active low signal indicating the high byte has valid data on the bus. It is an output if the CPU is controlling the bus and is an input if a DMA controller is in control of the bus.
35-34	XD<7:6>	I/O	EXPANSION DATA BUS bits <7:6>
32-27	XD<5:0>	I/O	EXPANSION DATA BUS bits <5:0>
57	SDIR	O	SYSTEM BUS DIRECTION controls the direction of data transfer between the IO channel and the local bus. When low it enables data transfer from the IO channel to local bus.
58	$\overline{\text{ACEN}}$	O	Active low. ACTION CODE ENABLE when active validates the action code signals AC<3:0>.
59-62	AC<3:0>	O	ACTION CODE is a four bit encoded command for bus size control and byte assembly operations performed by the 82A305s.
Memory Control			
77	$\overline{\text{AF32}}$	I	$\overline{\text{AF32}}$ is an active low input indicating that the current cycle is a local 32-bit cycle not requiring data size conversion. A high indicates an AT bus cycle. A 10KΩ pull-up resistor is recommended.
76	$\overline{\text{BUSY}}$	I	Active low. BUSY from memory controller.
83	$\overline{\text{MALE}}$	O	Active low. Address Latch Enable for accesses to on board memory/IO. It also indicates start of a new CPU cycle.

82C301 Pin Description (Continued)

Pin No.	Symbol	Pin Type	Description
11	TMRGATE	O	Active high. TIMER GATE signal enables the timer on 8254 Timer to generate the tone signal for the speaker.
12	TMROUT2	I	Active high. TIMER OUT 2 is the output from the timer 8254. It can be read from port B.
13	SPKDATA	O	Active high. SPEAKER DATA is used to gate the 8254 tone signal to the speaker.
17	$\overline{\text{INTA}}$	O	Active low. Interrupt acknowledge output to the interrupt controller. It is also used to direct data from the X to the S bus during an interrupt acknowledge cycle.
45	$\overline{\text{ATEN}}$	O	Active low. AT ENABLE when active indicates the current CPU access is an AT bus cycle.
73	XA00	I/O	Address bit 0. It is sourced from the 82C301 when 80386 or DMA (16 bit) is a bus master.
74	XA01	I/O	Address bit 1. It is sourced from the 82C301 when 80386 is a bus master.
26,36	NC		Reserved
21,42 63,84	VDD VDD		Power
1 22,33 43,64	VSS VSS VSS		Ground

82C302 Pin Description

Pin No.	Symbol	Pin Type	Description
Clocks and Control			
44	CLK2	I	Processor Clock input from 82C301.
46	SCLK	O	Generated CLK2/2 for reference.
41	RESET	I	RESET4 is the active high reset input from the 82C301. It resets the configuration registers to their default values. When active, RAS<0:3> and CAS <0:3> remain high, and OSC and OSC/12 remain inactive.
49	$\overline{REF}$	I	REFRESH is an active low input for DRAM refresh control from the 82C301. It initiates a refresh cycle for the DRAMs.
47	$\overline{MALE}$	I	Active low. Address Latch Enable
33	W/$\overline{R}$	I	System WRITE/$\overline{READ}$ status input
48	$\overline{SMCMD}$	I	Active low. System Memory Command. Indicates that the current command is for memory.
37	$\overline{XIOR}$	I	Active low. I/O READ command used to qualify $\overline{IO2XCS}$.
38	$\overline{XIOW}$	I	Active low. I/O WRITE command used to qualify $\overline{IO2XCS}$.
36	$\overline{XMEMR}$	I	Active low. X Bus memory READ command.
35	$\overline{XMEMW}$	I	Active low. X Bus memory WRITE command.
45	HLDA1	I	Active high. HOLD ACKNOWLEDGE 1 input from 82C301. It is used to generate RAS and CAS signals for the DMA cycles, in response to a HOLD request.
63	$\overline{LPAR}$	I	Active low. Parity error indication during a DRAM read. The failing address will be latched inside the chip for diagnostic purposes.
8	$\overline{HIROM}$	I	Active low. High ROM address chip select asserted when the highest 16 MBytes of memory is addressed (A<31:A24>=FFH). Unlatched. This is used in conjunction with the remaining address bits to generate the $\overline{ROMCS}$ signal.
7	$\overline{L64MEG}$	I	Active low. Low 64M address that is asserted when A<31:26>=00H. Unlatched. This is an active low input, normally sourced from the 82A303 high order address buffer. This input is asserted when A<31:26> = 00H. It is not latched internally. This input can optionally be de-activated by external logic to prevent the 82C302 from activating either $\overline{AF32}$ or memory control signals.
65	$\overline{ROMCS}$	O	Active low. Chip select for the BIOS EPROMs that is qualified with W/$\overline{R}$ and $\overline{SMCMD}$.

82C302 Pin Description (Continued)

Pin No.	Symbol	Pin Type	Description
6	$\overline{\text{IO2XCS}}$	I	Active low. IO address 22H and 23H chip selects. I/O port 22H is the index register for the configuration register set and and I/O 23H is accessed as the 8 bit configuration register selected by the index written to I/O port 22H.
09-32	A<25:02>	I	Address from the CPU local bus.
64	XA00	I	Address from the X Bus
34	$\overline{\text{READY}}$	I/O	$\overline{\text{READY}}$ is the system ready signal to the CPU. It is an active low output, activated when the requested memory data transfer is being completed. It is an input when the current bus cycle is an AT bus cycle ($\overline{\text{AF32}}$ = 1) and an output during local 32 bit memory cycle ($\overline{\text{AF32}}$ = 0).
39	$\overline{\text{BUSY}}$		Active low. Indicates that the memory controller is still servicing a previous request. This should be connected to IOCHRDY through an open collector buffer. This signal should not be confused with the BUSY of 80386.
40	$\overline{\text{AF32}}$	O	Active low, open drain. If asserted indicates that the current address is for local 32-bit memory on the system board (DRAM or possibly EPROM). Otherwise the current address is assumed to be on the AT IO channel.
Memory Expansion			
61-60	BA<1:0>	O	No connect.
2	$\overline{\text{DRD}}$	O	Active low. DRAM Read controls the direction of data transfer between the DRAM and local bus. When low, it enables data transfer from the memory bus <MD BUS> to the local data bus. When high, the data transfer is from the local data bus to the memory data bus.
DRAM Interface			
70-67	$\overline{\text{RAS}}$<3:0>	O	Row Address Strobes <3:0> are active low outputs. There is one RAS for each bank. RAS0 selects the lowest bank and RAS3 selects the highest bank. These lines should be buffered and line terminated with 33Ω resistor before driving the DRAM RAS lines.
71	$\overline{\text{CAS}}$	O	Active low. Column Address Strobe. Used to latch data in the 82A305 data buffer.

82C302 Pin Description (Continued)

Pin No.	Symbol	Pin Type	Description
56-55 53-52	$\overline{CAS<3:2>}$ $\overline{CAS<1:0>}$	O	Active low. Column Address Strobe. A strobe per bank that must be externally gated with byte enables for each byte of DRAM chips. These signals should be buffered and line terminated with 33Ω resistors before driving the DRAM CAS lines.
58	OSC/12	I	1.19MHz Clock input used for RAS low time out. This input can optionally be strapped high to disable RAS time out.
66	$\overline{DWE}$	O	Active low. DRAM Write Enable.
62	$\overline{FBK}$	O	Active low. Force Bank. Will always be inactive.
51	$\overline{FBE}$	O	This is an active low signal. It is activated during local memory read cycles. When active, all the byte enables are forced low, independent of $\overline{MALE}$ or the BE<3:0>, thereby resulting in 32-bit memory read operation. This signal is connected to the FBE input on the 82A306.
72-73	DA<9:8>	O	DRAM address lines DA9 and DA8. These lines should be buffered and line terminated with 75Ω resistors before driving the DRAM array.
75-82	XDA<7:0>	I/O	These are multiplexed bi-directional pins. During accesses to the internal registers, these lines provide the index value and configuration information. During DRAM cycles, DA<7:0> generate the lower address bits for the DRAM array. A 74LS245 is required to isolate DRAM addresses during a memory access. These lines should be buffered and line terminated with 75Ω resistors before driving the DRAM array.
83	$\overline{XDEN}$	O	Active low. XD bus buffer Enable. $\overline{XDEN}$ is asserted during IO access cycles to 022H and 023H if 022H access is for an internal register of 82C302. XDEN is used to control the chip enable for the buffer between the XD and XDA buses.
3	$\overline{PCHK}$	O	Active low. Parity Check.
4	$\overline{PEN}$	O	Active low. Overall Parity Enable.
50	$\overline{MDEN}$	O	Active low. MEMORY DATA BUFFER ENABLE. This signal is by default always low and is connected to $\overline{MDEN}$ of 82A305.
Miscellaneous			
5,57,59			Reserved. No Connect.
42,84	VDD		Power
1,43 54,74	VSS VSS		Ground

82A303 Pin Description

Pin No.	Symbol	Pin Type	Description
Control			
17	$\overline{\text{MASTER}}$	I	Active low. Bus MASTER is generated by a device that is active on the expansion bus. After $\overline{\text{MASTER}}$ is forced low by an I/O device, the I/O CPU must wait for one system clock period before forcing the address and data lines. $\overline{\text{MASTER}}$ must not be held low for more than 15 microseconds, or else data in the system memory may be lost due to lack of a refresh cycle.
15	HLDA1	I	Hold Acknowledge is an active high input from the 82C301 used for address and data direction control during DMA cycles.
20	$\overline{\text{MALE}}$	I	Active low. MEMORY ADDRESS LATCH ENABLE clocks addresses into the address registers on the rising edge.
21	$\overline{\text{REF}}$	I	REFRESH is an active low input. This signal controls the address buffer direction. When REF is active, the contents of the refresh address counter on the 82A304 is gated to the SA address bus.
16	$\overline{\text{ATEN}}$	I	Active low. AT BUS ENABLE is active when the CPU makes an AT bus access.
25	$\overline{\text{LIOCS}}$	O	Active low. LOW IO ADDRESS CHIP SELECT is asserted when A<15:12> = 0.
24	$\overline{\text{LMEGCS}}$	O	LOW MEG CHIP SELECT is an unlatched active low output asserted when the low Meg memory address space (0 to 1024Kbytes) is accessed or during refresh cycles.
13	$\overline{\text{L64MEG}}$	O	Active low. LOW 64 MB SELECT is active when the access address decodes to the low 64MB address space: A<31:26> = 0.
14	$\overline{\text{HIROM}}$	O	Active low. HI ROM SELECT is active when A<31:26> = 3FH.
Processor/Bus Interface			
12-2 68-60	A<31:21> A<20:12>	I/O I/O	Local Address Bus
58-54 51-42	XA<26:22> XA<21:12>	I/O I/O	X Address Bus
22	$\overline{\text{XAHE}}$	I	Active low XBUS Address High Enable. Enable bits 26:24 from the XA bus. A pullup is provided so that the input can be left open if only 24 bits are sourced externally.

82A303 Pin Description (Continued)

Pin No.	Symbol	Pin Type	Description
41-36 34-26	SA<26:21> SA<20:12>	I/O I/O	System Address Bus. These outputs have 24mA drive.
23	$\overline{\text{SAHE}}$	I	Active low SBUS Address High Enable. Enable bits 26:24 from the SA bus. A pullup is provided so that the input can be left open if only 24 bits are sourced externally.
59	MA12	O	Memory Address Bus Latched on the trailing edge of $\overline{\text{MALE}}$.
Miscellaneous			
18,52	VCC		Power
1,19 35,53	VSS VSS		Ground

82A304 Pin Description

Pin No.	Symbol	Pin Type	Description
Control			
17	$\overline{\text{MASTER}}$	I	Active low. BUS MASTER is generated by a device active on the expansion bus.
15	HLDA1	I	Hold Acknowledge is an active high input from the 82C301 used for address and data direction control during DMA cycles.
20	$\overline{\text{MALE}}$	I	Active low. MEMORY ADDRESS LATCH ENABLE clocks addresses into the address registers on the rising (trailing) edge.
21	$\overline{\text{REF}}$	I	REFRESH is an active low input. This signal controls the address buffer direction. When REF is active, the contents of the refresh address counter on the 82A304 is gated to the SA address bus.
16	$\overline{\text{ATEN}}$	I	Active low. AT BUS ENABLE is active when the CPU makes an AT bus access.
25	$\overline{\text{LIOCS}}$	I	Active low. LOW IO ADDRESS CHIP SELECT.
54	$\overline{\text{XIOR}}$	I	Active low. X BUS IO Read.
55	$\overline{\text{XIOW}}$	I	Active low. X BUS IO Write
57	$\overline{\text{XDIR}}$	O	X BUS DIRECTION is used to control the drivers between the X bus and S bus. The drivers should be used such that S bus signals are driven toward X bus when $\overline{\text{XDIR}}$ is low and in the other direction when high.
26	EXDEC	I	Active high. EXTENDED IO DECODE. A strapping option that when low ignores A<11:10> and $\overline{\text{LIOCS}}$ (which is decoded based on A<15:12>) for decoding the system board IO ports. An internal pullup is provided.
58	$\overline{\text{IO2XCS}}$	O	Active low. IO 2x SELECT is decode of IO address 022H or 023H.
63	$\overline{\text{8042CS}}$	O	Active low. 8042 SELECT is decode of 8042 address at 060H or 064H.
59	$\overline{\text{PORTBCS}}$	O	Active low. PORTB SELECT is decode of Port B address at 061H
60	$\overline{\text{NMICS}}$	O	Active low. NMI SELECT is decode of NMI address at 070H.
61	$\overline{\text{287CS}}$	O	Active low. 80287 SELECT is decode of 287 address at 0E0-0FFH.
56	$\overline{\text{ACK}}$	O	Active low. ACKNOWLEDGE indicates that AEN1 or AEN2 has been asserted. This signal is used to generate the AEN signal on the AT I/O channel.

82A304 Pin Description (Continued)

Pin No.	Symbol	Pin Type	Description
62	AS	O	Active high. Address Strobe for the RTC. IO address 7xH is conditioned with $\overline{XIOW}$.
24	$\overline{INTA}$	I	Active low. INTERRUPT ACKNOWLEDGE bus cycle indication.
Processor/Bus Interface			
14-5	A<11:02>	I/O	Local address
51-40	XA<11:00>	I/O	X bus address
39-36 34-27	SA<11:08> SA<07:00>	I/O I/O	System address. These outputs have 24mA drive.
4-2 68-64	MA<11:09> MA<08:04>	O O	Memory address
23	$\overline{TEST}$	I	Active low. TEST when active resets the refresh counter to zero. A pullup is provided.
22	NC		Reserved
Miscellaneous			
18,52	VCC		Power
1,19 35,53	VSS VSS		Ground

82A305 Pin Description

Pin No.	Symbol	Pin Type	Description
Control			
15-12	AC<3:0>	I	ACTION CODES input from the 82C301 are used for data bus sizing and byte assembly operations.
16	$\overline{\text{ACEN}}$	I	Active low. Action Code Enable when active validates the action codes.
17	SDIR	I	System bus DIRection. A low enables data transfers from the System to Local bus and in the other direction when high.
25	$\overline{\text{ATEN}}$	I	Active low. AT bus ENable
23	HLDA1	I	Active high. HoLD Acknowledge.
20	$\overline{\text{MDEN}}$	I	Active low. MEMORY DATA BUFFER ENABLE. When low enables the memory data buffers for transfer between the processor and memory subsystem. When high disables these bus buffers. Should be connected to $\overline{\text{MDEN}}$ on the 82C302.
19	$\overline{\text{LDEN}}$	I	Active low. Selects LD as a source for the SD bus during MASTER or DMA reads. When HI selects MD. Asserting $\overline{\text{MRD}}$ overrides $\overline{\text{LDEN}}$ and gates MD to the SD bus. A pullup is provided.
21	$\overline{\text{MRD}}$	I	Active low. Memory Bus DIRection. When low enables data movement for a processor read from the memory to local bus. $\overline{\text{MRD}}$ when Hi enables drivers from local to memory bus.
22	$\overline{\text{DLE}}$	I	DATA LATCH ENABLE is an active low signal used to latch the data in the 82A305 data buffers. This is normally connected to the CAS output (pin 71) of the 82C302.
11, 9	D<31:30>	I/O	Local Data Bus
8, 6	D<29:28>	I/O	
5-2	D<23:20>	I/O	
68-65	D<15:12>	I/O	
64-61	D<07:04>	I/O	
45,43	MD<31:30>	I/O	Memory Data Bus
42,40	MD<29:28>	I/O	
39-36	MD<23:20>	I/O	
34-31	MD<15:12>	I/O	
30-27	MD<07:04>	I/O	
49-46	PP<03:00>	O	Memory Partial Parity

82A305 Pin Description (Continued)

Pin No.	Symbol	Pin Type	Description
59,57	SD<15:14>	I/O	IO Channel Data Bus
56,55	SD<13:12>	I/O	
54-53	SD<07:06>	I/O	
51-50	SD<05:04>	I/O	
7,24	NC		Reserved.
41,58	NC		
Power Supplies			
18,52	VCC		Power
1,10	VSS		Ground
26,35	VSS		
44,60	VSS		

82A306 Pin Description

Pin No.	Symbol	Pin Type	Description
64	ATSCLK	I	AT IO channel SYSCLK input.
59	SYSCLK	O	Buffered 24mA SYSCLK to AT IO channel. Nominally one half of the bus state machine clock frequency.
Control			
54	CX1	I	14.318MHz oscillator input from crystal.
55	CX2	O	14.318MHz oscillator output to crystal.
56	OSC	O	System 14.318MHz output. This output has 24mA drive capability.
57	OSC/12	O	14.318MHz/12 = 1.19MHz output. This output has 24mA drive capability.
17	$\overline{\text{MALE}}$	I	Active low. Address Latch Enable for on board access.
12-15	$\overline{\text{BE<3:0>}}$	I	Active low. BYTE ENABLES.
4-7	$\overline{\text{LBE<3:0>}}$	O	Active low. LATCHED BYTE ENABLE on the trailing edge of $\overline{\text{MALE}}$.
24	$\overline{\text{FBE}}$	I	Active low. FORCE BYTE ENABLE Forces all byte enables LBE active independent of $\overline{\text{MALE}}$ and the $\overline{\text{BE<3:0>}}$ inputs.
67	$\overline{\text{REF}}$	I	Active low. REFRESH.
8	A<31>	I	Local Address Bus bit 31.
10	M/$\overline{\text{IO}}$	I	80386 Status used to generate $\overline{\text{AF32}}$ for the 80387 and other 32 bit IO devices.
9	D/$\overline{\text{C}}$	I	80386 Status used to generate $\overline{\text{AF32}}$ for the 80387 and other 32 bit IO devices.
68	$\overline{\text{LMEGCS}}$	I	LOW MEG CHIP SELECT is an unlatched active low output asserted when the low Meg memory address space (0 to 1024Kbytes) is accessed or during refresh cycles.
11	$\overline{\text{AF32}}$	T	Active low. Tri-state output $\overline{\text{AF32}}$ when active indicates a 32 bit local bus memory or an I/O access cycle on the system board. It is generated from M/$\overline{\text{IO}}$, D/$\overline{\text{C}}$, <31>, and HLDA1.

82A306 Pin Description (Continued)

Pin No.	Symbol	Pin Type	Description
66	$\overline{\text{MASTER}}$	I	Active low. Bus MASTER input from the AT IO channel.
3	RESET	I	Active high. RESET input. Should be connected to RESET4 of 82C301.
62	RESETB	O	Active high. Buffered RESET to X bus.
61	RDRV	O	Active high. RESET to AT bus. 24mA drive capability.
2	ALE	I	Active high. ALE for AT bus.
40	$\overline{\text{XBHE}}$	I/O	Active low. X Bus BHE.
44	$\overline{\text{XMEMR}}$	I/O	Active low. X Bus Memory Read.
43	$\overline{\text{XMEMW}}$	I/O	Active low. X Bus Memory Write.
42	$\overline{\text{XIOR}}$	I/O	Active low. X Bus IO Read.
41	$\overline{\text{XIOW}}$	I/O	Active low. X Bus IO Write.
60	BALE	O	Active high. Buffered ALE to AT bus. 24mA drive capability.
45	$\overline{\text{SBHE}}$	I/O	Active low. System bus BHE. 24mA drive capability.
51	$\overline{\text{SMEMR}}$	O	Active low. System bus MEMory Read. 24mA drive capability.
50	$\overline{\text{SMEMW}}$	O	Active low. System bus MEMory Write. 24mA drive capability.
49	$\overline{\text{MEMR}}$	I/O	Active low. Memory Read. 24mA drive capability.
48	$\overline{\text{MEMW}}$	I/O	Active low. Memory Write. 24mA drive capability.
47	$\overline{\text{IOR}}$	I/O	Active low. IO Read. 24mA drive capability.
46	$\overline{\text{IOW}}$	I/O	Active low. IO Write. 24mA drive capability.
16	HLDA1	I	Active high. HOLD ACKNOWLEDGE from 82C301.
22	SCLK	I	CLK2/2 clock input. Should be connected to SCLK output of 82C302.
27-30	PPH<3:0>	I	PARTIAL PARITY HIGH computed by 82A305 for the high nibble data bits.
31-34	PPL<3:0>	I	PARTIAL PARITY lowW computed by 82A305 for the low nibble data bits.
36-39	MP<3:0>	I/O	Data Parity bits for the DRAMs.
21	$\overline{\text{CAS}}$	I	Active low. Read Parity latch enable.
20	$\overline{\text{PCHK}}$	I	Active low. PARITY CHECK STROBE for generating $\overline{\text{LPAR}}$ from the partial parity and data parity bits.
26	$\overline{\text{PEN}}$	I	Active low. Overall PARITY CHECK ENABLE.

82A306 Pin Description (Continued)

Pin No.	Symbol	Pin Type	Description
23	$\overline{WPE}$	I	Active low. WRITE PARITY ENABLE. Enables the sourcing of write parity onto the MP bus. A pullup is provided.
25	$\overline{LPAR}$	O	Active low. LATCHED PARITY ERROR signal.
65	$\overline{TEST}$	I	Active low. Enables testing of the OSC/12 counter. A pullup is provided.
63	IN1	I	Input to an uncommitted 24mA non-inverting buffer.
58	OUT1	O	Output of the IN1 buffer. 24mA drive capability.
Power Supply			
18,52	VCC		Power
1,19 35,53	VSS VSS		Ground

82C301 Bus Controller

- Optional Independent AT Bus Clock
- Processor Clock Selection
- AT Bus Timing Configuration
- CPU Interface and Bus Control
- Port B Register

Overview

The 82C301 provides a clock generation circuitry to solve two basic problems. One is to provide system designers the choice of a particular AT bus clock most adequate for their applications. The other is to allow the processor to run at the full speed and optionally at a speed to match timing dependent application software. Because many AT adapter boards are designed with built in timing assumptions, independent programmable controls are provided for AT bus command timing and wait state generation for IO accesses and for 8, 16, and 32 bit memory accesses.

The 82C301 interfaces directly with the 80386 and implements the state machines required for controlling all bus accesses. It also features a status register known as Port B register used in a standard IBM PC AT.

Functional Description

The 82C301 has the following function blocks as illustrated in figure 1-1:

- Clock generation and reset control
- CPU bus access state machine
- AT bus access state machine
- Port B register and NMI logic
- Bus Arbitration and refresh logic

Clock Generation and Selection Logic

The 82C302 provides a flexible clock selection scheme as shown in Figure 1.2. It has two inputs; CLK2IN and ATCLK1. CLK2IN is driven from a packaged crystal oscillator circuit, running at twice the processor rated CPU frequency (32 MHz for a 16 MHz 80386). An oscillator circuit is provided for the ATCLK1 signal, so that it can be connected to either a packaged oscillator or a crystal. Typically, the ATCLK1 should be of a lower frequency than CLK2IN.

The 82C301 generates processor clock, CLK2, for driving the 80386 CLK2 input as well as the CPU state machine. SCLK is CLK2/2 and is in phase with the internal states of the 80386. BCLK (internal) is the AT bus state machine clock and is used for the AT bus interface. SYSCLK is the AT bus system clock and is always BCLK/2.

CLK2 can be derived from CLK2IN or from the ATCLK1. In the synchronous mode, both CLK2 and BCLK are derived from CLK2IN, so that the processor state machine and the AT state machine run synchronously. In the asynchronous mode, BCLK is generated from the ATCLK1 and CLK2 is generated from CLK2IN or the ATCLK1. In this case, the processor state machine and the AT state machine run asynchronous to each other. The following clock selections are possible:

Synchronous mode

1. CLK2 = CLK2IN
   BCLK = CLK2IN/2
   SYSCLK = BCLK/2 = CLK2IN/4
2. CLK2 = CLK2IN
   BCLK = CLK2IN/3
   SYSCLK = BCLK/2 = CLK2IN/6
3. CLK2 = BCLK = CLK2IN/2
   SYSCLK = BCLK/2 = CLK2IN/4

Asynchronous mode

1. CLK2 = CLK2IN
   BCLK = ATCLK1
   SYSCLK = BCLK/2 = ATCLK1/4

Under normal operation, CLK2IN should be selected as the processor clock (CLK2) to allow the processor to operate at the rated maximum speed. BCLK can either be a subdivision of CLK2IN or be derived from the ATCLK1. ATCLK may be selected to generate the CLK2 only when it is desired to slow

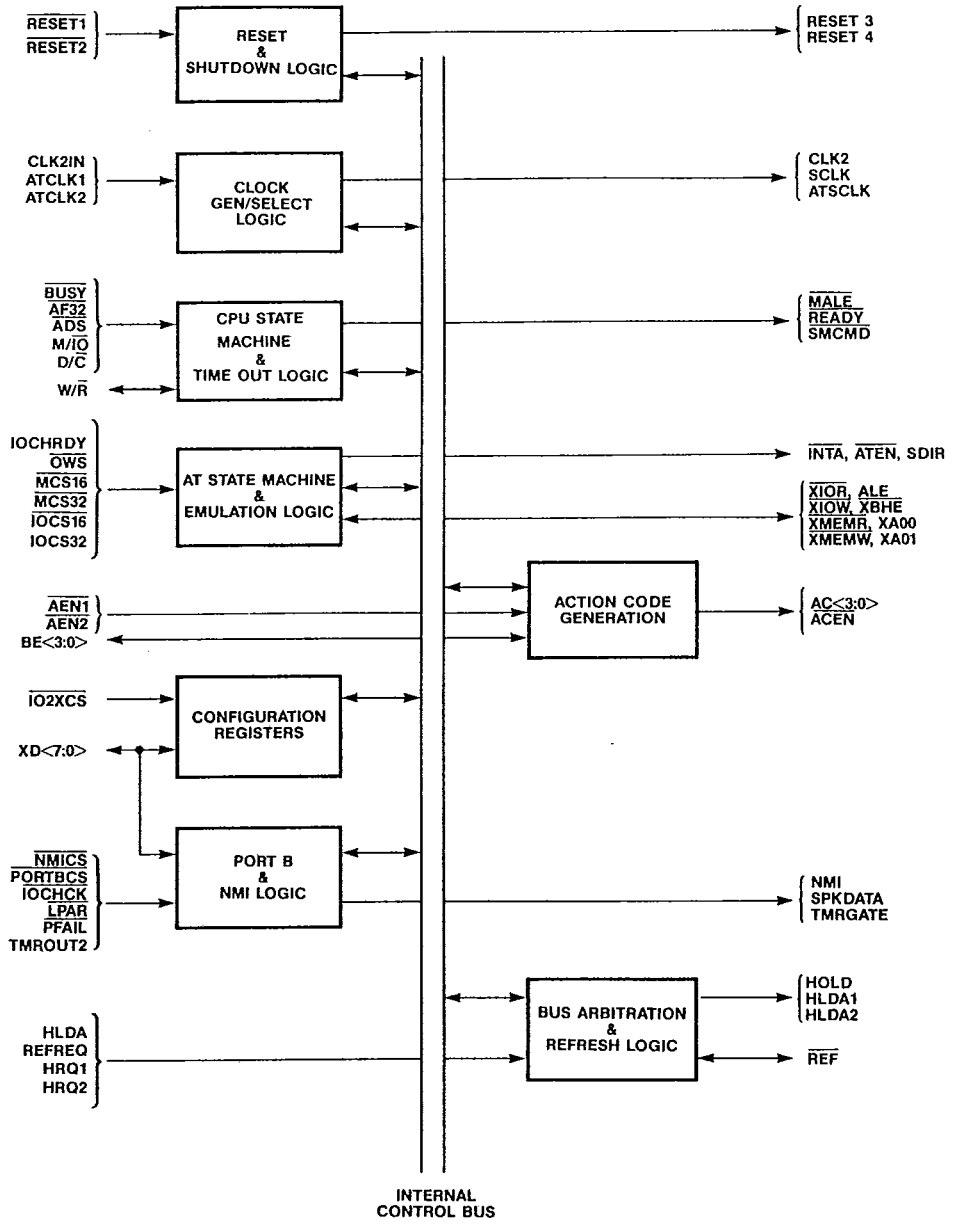


Figure 1-1. 82C301 Functional Block Diagram

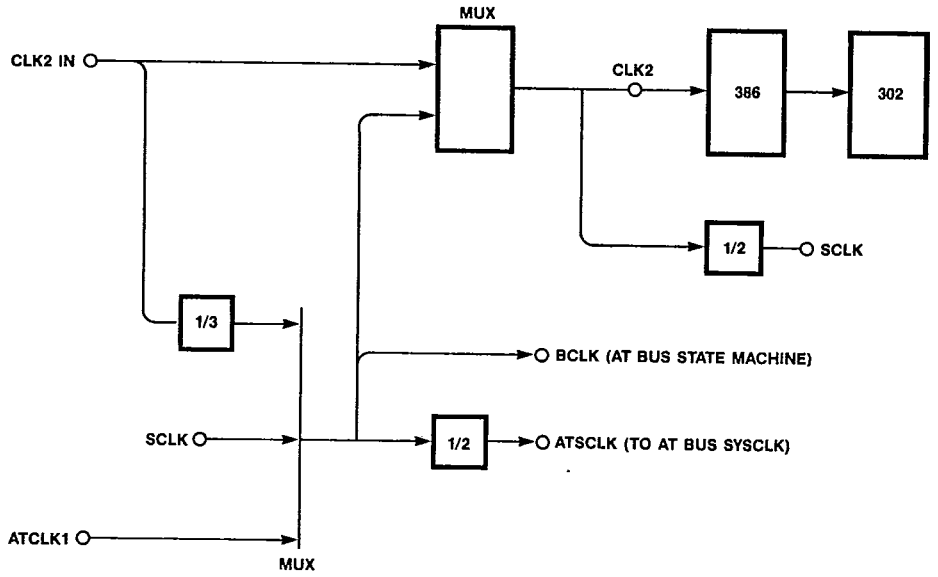


Figure 1-2. CLK2 and ATSCLK Clock Selection

down the processor for timing dependent code execution. Once the options for clock selections are set, the clock switching occurs with clean transition in the synchronous or the asynchronous mode. During clock switching, no phases of CLK2 are less than the minimum value or greater than the maximum value specified for the 80386 CPU. The clock source selection is made by writing to REG 4H<4> and REG 6H<1:0>, which defaults to:

CLK2 = CLK2IN
SYSCLK = CLK2IN/6

CLK2IN	SCLK	Ratio	BCLK	SYSCLK
24	12	/2	12	6
32	16	/2	16	8
32	16/3	10.7	5.4	

Table 1-1. Examples of BCLK and SYSCLK derived from CLK2

Reset and Shutdown Logic

Two reset inputs $\overline{\text{RESET1}}$ and $\overline{\text{RESET2}}$ are provided on the 82C301 bus controller. $\overline{\text{RESET1}}$ is the Power Good signal from the power supply. When $\overline{\text{RESET1}}$ is active, the 82C301 asserts RESET3 and RESET4 for a system reset. $\overline{\text{RESET2}}$ is generated from the 8042 (or 8742) keyboard controller when a "warm reset" is required. The warm reset activates RESET3 to reset the 80386 CPU. RESET3 is also activated by the 82C301 when a shutdown condition is detected.

RESET3 is asserted for at least 85 CLK2 cycles during power on reset and for during warm reset. RESET4 is used to reset the AT bus, 82C206 IPC, 8042 keyboard controller and the 82C302 page interleaved memory controller. It is synchronized with respect to CLK2 and is asserted as long as the power good signal is held low. After a shut down condition is detected, RESET3 is asserted and is held high for at least 85 CLK2 cycles

and then deasserted. RESET3 resulting from a shut down condition is synchronous with respect to CLK2, ensuring proper CPU operation. Both RESET3 and RESET4 meet the setup and hold time requirements of the 80386 CPU.

Bus Arbitration

The 82C301 controls all bus activity and provides arbitration between CPU, DMA/Master devices, and DRAM refresh logic. It handles HRQ1, HRQ2 and REFREQ by generating a hold request to the CPU and arbitrating among these requests in a non-preemptive manner. The CPU relinquishes the bus by issuing HLDA. The 82C302 responds by issuing HLDA1, HLDA2 or REF depending on the requesting device. During refresh cycles, the refresh logic has control of the bus until REF goes inactive. XMEMR is asserted low during a refresh cycle and the refresh addresses are provided on the MA0-MA9 address lines by the refresh address counter on the 82C302. During a DMA cycle, the DMA controller has control of the bus until HRQ goes inactive. During the HLDA cycle, the 82C301 generates both SMCMD and action code AC<3:0> to control the buffer enable and directions for the address and data buffers. Bus size conversions are not supported by the 82C301 for these bus cycles and if necessary, should be performed by the requesting device.

Action Code Generation Logic

The AT state machine performs the data conversions for CPU accesses to devices not on the local CPU or memory bus. The AT bus conversions are performed for 32, 16 or 8 bit read or write operations. 32 bit transfers are broken down into smaller 8 bit or 16 bit AT bus reads or writes. The action codes are generated as shown in table 5.2 to control the data bus buffers on the 82A305 data buffers. The action codes are in response to IOCS32, MEMCS32, IOCS16 and MEMCS16 inputs.

CPU and AT Bus State Machines

In order to extract maximum performance out of the 80386 on the system board, it is desirable to operate the processor at the maximum rated CPU frequency. This frequency may be too fast for the AT bus. In order to overcome this problem, the 82C301 supports two state machines: the CPU state machine which typically runs off CLK2 and the AT bus state machine which runs off the BCLK.

The CPU state machine and AT state machine control CPU accesses to the devices on the local bus and non-local buses respectively. The CPU state machine supports only 32 bit transfers between the 80386 and system memory (or memory mapped IO) and no bus size conversions are done. Thus the BS16 input on the 80386 is not used in a CS8230 system and should be connected to a HI level. The AT state machine responsible for all non-local bus CPU accesses controls the AT bus and supports bus size matching.

All CPU access cycles are started by 82C301 asserting MALE. The CPU state machine then samples AF32 one SCLK clock cycle later. If AF32 is active, it is assumed to be a local bus cycle and the CPU state machine terminates this cycle when it detects READY signal active. In response to an MALE, if the AF32 is detected inactive the control is passed to AT state machine. At the end of the bus access cycle, the AT state machine generates READY to terminate the processor access cycle as well as the CPU state machine cycle.

CPU State Machine

The interface to the 80386 requires interpretation of the status lines upon assertion of ADS and synchronization and generation of a READY response to the CPU upon completion of the requested operation. By interpreting the CPU status lines and ADS, the 82C301 generates control signals MALE and SMCMD. In response to each ADS generated by the CPU, an MALE is generated by the 82C301 to indicate the start of a new CPU access cycle. In a non-pipelined CPU cycle, MALE is generated in response to ADS being asserted by the 80386. In a pipelined cycle, MALE is generated when the assertion of READY is detected for the previous CPU cycle. If AF32 is not active one cycle after MALE is asserted, control is passed to the AT bus state machine. The CPU state machine then waits for READY

becoming active to terminate the access cycle. In the CS 8230 CHIPset, the READY can be generated by 82C302 which controls the system memory access.

SMCMD indicates a memory cycle for both CPU and non-CPU accesses. During CPU cycles it is generated for all memory cycles by decoding M/IO, D/C and W/R signals. During non-CPU cycles it is active when XMEMR or XMEMW is active.

NA Pipeline Control

The 82C301 supports both pipelined and non-pipelined cycles of the 80386. The NA (Next Address) input on the 80386 can be always asserted in a CS8230 system for higher performance.

Bus Timeout

An optional feature allows generation of an NMI if an internal memory cycle does not complete within a certain timeout period. This occurs if AF32 is asserted in response to MALE and READY is not returned to the 82C301 within 128 CLK2 cycles. A control bit in the 82C301 configuration registers enables this feature.

AT Bus State Machine

The AT state machine gains the control of the buses when AF32 is detected inactive by the CPU state machine. It uses BCLK having a frequency twice that of the IO channel clock SYSCLK. When ATCLK1 is selected as the source for BCLK, it also performs the necessary synchronization of control and status signals between the AT bus and the processor. The 82C301 supports 8, 16 or 32 bit transfers between the processor and 8, 16 or 32 bit memory or IO devices located on the IO channel.

An AT bus cycle is initiated by asserting ALE decoded from the CPU status signals and is terminated by asserting READY. On the falling (or trailing) edge of the ALE, MCS16, IOCS16, MCS32, IOCS32 are sampled to determine the bus size conversion required. It then enters the command cycle. The AT bus state machine provides the sequencing and timing controls for status and command phases of different AT bus cycles. These controls provide for timing emulation of lower speed IO channels to maintain compatibility with AT or PC/XT IO adapters and memory cards. The command cycle is terminated by detecting 0WS or IOCHRDY active.

IO Channel Speed Control

The AT state machine can be programmed to insert wait states in units of ATSCLK and to delay the generation of XIOR, XIOW, XMEMR, and XMEMW commands in one half units of ATSCLK (BCLK) within the selected wait states. The command phase delay can be selectively defined for IO cycles and for 8, 16, and 32 bit wide memory cycles by setting the corresponding fields in REG05H. REG06H controls the IO Channel wait state generation for 8, 16, and 32 bit accesses.

The bus clock BCLK is selected by setting REG06H<1:0>. It should be noted that the processor clock source should be set to CLK2IN whenever the BCLK is selected to be SCLK.

Data Conversion

The AT bus access state machine performs data conversion for CPU accesses to devices not on the local bus when AF32 is not asserted. AT bus data conversions are performed for the following types of transfers:

— 32 bit to 8/16 bit,
— 24 bit to 8/16 bit,
— 16 bit to 8/16 bit.

Larger transfers are broken into smaller AT bus reads or writes and the action code AC<3:0> to the 82A305/82B305/82C305 is generated. Byte addresses XA<01:00> are generated to drive the lower two bits of the AT address bus.

The 82C301 responds to IOCS16, MCS16, IOCS32, and MCS32 in determining what size of data the IO channel needs. If none of the above signals are asserted, 8 bit transfers are assumed and the request is converted into 2, 3 or 4 IO channel cycles based on BE<3:0>. For either MCS16 or IOCS16, the AT bus

state machine converts a 32-bit access into two 16 bit AT bus accesses.

The bus state machine also supports 32-bit transfer between the processor and memory and IO devices on the IO channel. IOCS32 and MCS32 inputs allow a device to request a 32-bits transfer. It is assumed that the necessary extensions to the AT bus are made to utilize this feature. IOCS32 and MCS32 override IOCS16 and MCS16.

In performing these data conversions, a 4-bit action code AC<3:0> is generated to control the buffers in 82A305 for the alignment of data path, and direction control between D, MD, and SD data buses. The definition for the action codes is given in the functional description of 82A305.

Port B Register

The 82C301 provides access to Port B defined for a PC AT as shown in figure 1-3. PORTBCS enables the access to Port B register and is provided as an output from 82A304. Table 1-2 gives the Port B register bit definition.

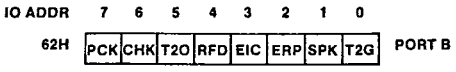


Figure 1-3 Port B register definition

The NMI sub-module performs the latching and enabling of I/O and parity error conditions, which will generate a non-maskable interrupt to the CPU if NMI is enabled. Reading Port B will indicate the source of the error condition (IOCK and PCHK). Enabling and disabling of NMI is accomplished by writing to the I/O address 070H. On the rising edge of XIOW, NMI will be enabled if data bit 7 (XD7) is equal to 1 and will be disabled if XD7 is equal to 0.

CS 8230 Internal Register Access Ports

The CS 8230 have internal registers used for system configuration and for diagnostics. These are accessed through IO ports 22H and 23H normally found in the interrupt controller. An indexing scheme is used to reduce the number of IO addresses required to access all registers needed to configure and control CS 8230 chips. Each access (either read or write) to an internal register is done by first writing its index into port 22H. This index then controls the multiplexers gating the appropriate register data accessible as port 23H. Every access to port 23H must be pre-

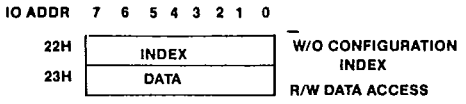


Figure 1-4. Configuration Register Access Ports

Addr	Bits	Function	
61H		Port B Register	
	7	Read only.	PCK - System memory parity check.
	6	Read only.	CHK - IO channel check.
	5	Read only.	T2O - Timer 2 out
	4	Read only.	RFD - Refresh Detect.
	3	Read/write.	EIC - Enable IO channel check.
	2	Read/write.	ERP - Enable system memory parity check.
	1	Read/write.	SPK - Speaker Data
	0	Read/write.	T2G - Timer 2 Gate Speaker

Table 1-2 Port B register definition

ceded by writing the index value to port 22H even if the same data port is being accessed again.

Configuration Registers

There are 3 bytes of configuration and diagnostic registers in 82C301 as shown in figure 1-5. The definitions for these registers are given in table 1-3.

INDEX	7	6	5	4	3	2	1	0	
04H	VERS		—	PC	FE	TE	PF	TO	VERSION/PROCESSOR CLOCK/NMI SOURCES
05H	M32		M15		M8		IO		COMMAND DELAY
06H	32 WS		16 WS		8 WS		B CLK		WAIT STATE/BUS CLOCK

Figure 1-5. 82C301 Internal Configuration Registers

Index	Bits	Function
04H		Version/Processor clock select/NMI source
	7:6	Read only. Version
		0 Initial version
	5	Reserved
	4	Processor Clock Select. If SCLK is selected as the source for BCLK, CLK2 source must not be selected as BCLK.
		0 Use processor oscillator input. Default. 1 Use AT bus state machine clock (SYSCLKx2).
	3	Power Fail Warning Enable
		0 Power Fail NMI not enabled. Default. 1 Power Fail NMI enabled
	2	Local Bus READY timeout NMI Enable
		0 READY timeout NMI not enabled. Default. 1 READY timeout NMI enabled
	1	Read only. Power Fail warning active during last NMI arbitration.
		0 Power Fail warning pin not active. Default. 1 Power Fail warning pin was active.
	0	Read only. Local bus READY timeout
		0 READY timeout has not occurred. Default. 1 READY timeout has occurred

Table 1-3 82C301 Configuration Register Definitions

Index	Bits	Function
05H		Command delay The value for each one of the command delay field is defined as: 0 0 cycle delay 1 1 cycle delay 2 2 cycle delay 3 3 cycle delay
	7:6	AT Bus 32 bit memory command delay. Specifies between 0 and 3 BCLK cycles for command delay during an AT bus 32 bit memory cycle. Default is 0.
	5:4	AT Bus 16 bit memory command delay. Specifies between 0 and 3 BCLK cycles for command delay during an AT bus 16 bit memory cycle. Default is 0.
	3:2	AT Bus 8 bit memory command delay. Specifies between 0 and 3 BCLK cycles for command delay during an AT bus 8 bit memory cycle. Default is 1.
	1:0	AT Bus I/O Cycle command delay. Specifies between 0 and 3 BCLK cycles for command delay during an AT bus IO cycle. Default is 1.
06H		Wait State/Bus Clock Source
	7:6	32 bit AT Bus wait state selects 0-3 wait states per 32 bit transfer on the AT bus. Each wait state is 2 BCLK cycles. Default is 3. 0 3 cycle delay 1 2 cycle delay 2 1 cycle delay 3 0 cycle delay
	5:4	16 bit AT Bus wait state selects 0-3 wait states per 16 bit transfer on the AT bus. Each wait state is 2 BCLK cycles. Default is 3. 0 3 cycle delay 1 2 cycle delay 2 1 cycle delay 3 0 cycle delay
	3:2	8 bit AT Bus wait state selects 2-5 wait states per 8 bit transfer on the AT bus. Each wait state is 2 BCLK cycles. Default is 5. 0 5 cycle delay 1 4 cycle delay 2 3 cycle delay 3 2 cycle delay
	1:0	Bus Clock Source Select 0 Use Proc Clock/3 for AT bus state machine. Default. 1 Use Proc Clock/2 for AT bus state machine. 2 Reserved. 3 Use ATCLK input pin for the AT bus state machine.

Table 1-3 82C301 Configuration Register Definitions (Continued)

82C301 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	—	7.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{op}	-25	85	C
Storage Temperature	T_{stg}	-40	125	C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82C301 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	C

82C301 DC Characterisitcs

Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.0		V
Output Low Voltage I_{OL}=8mA (Note 1)	V_{OL}		0.45	V
Output High Voltage I_{OH}=-200 μA	V_{OH}	2.4		V
Input Current $0 < V_{IN} < V_{CC}$	I_{IL}		±10	μA
Output Short Circuit Current V_O=0V	I_{OS}	TBD	TBD	mA
Input Clamp Voltage	V_{IC}		TBD	V
Power Supply Current @ 16 MHz Clock	I_{CC}		40	mA
Output HI-Z Leak Current $0.45 < V_{OUT} < V_{CC}$	I_{OZ1}		±10	μA
CLK2 Output Low Voltage @ I_{OL} = 5 mA	V_{OLC}		0.45	V
CLK2 Output High Voltage @ I_{OH} = -1 mA	V_{OHC}	4.0		V

NOTE:
1. $\overline{\text{REF}}$ has I_{OL} = 16mA. CLK2, $\overline{\text{MALE}}$ have I_{OL} = 8mA. All other outputs and I/O pins have I_{OL} = 4mA. In all cases all $I_{OL} = I_{OH}$ for the pin.

82C301 AC Characteristics

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Sym	Description	82C301-16 Min	Typ	Max	82C301-20 Min	Typ	Max	Unit	Notes
t101	CLK period	31			25			ns	
t102	CLK2 low time	10			9			ns	at 2V
t103	CLK2 high time	10			9			ns	at 2V
t104	CLK2 rise time			5			4	ns	
t105	CLK2 fall time			5			4	ns	
t106	SCLK delay from CLK2	6			6			ns	
t181	RESET1, RESET2 input set-up time	28			28			ns	at 2V
t182	RESET1, RESET2 input hold time	10			10			ns	at 2V
t183	RESET1, RESET2 minimum pulse width	250			250			ns	
t107	RESET3, RESET4 active delay	11	15		11	15		ns	
t108	RESET3, RESET4 inactive delay	8	15		8	15		ns	
t109	$\overline{\text{SMCMD}}$ delay from $\overline{\text{MALE}}$ active		7	10		7	10	ns	
t110	$\overline{\text{AF32}}$ setup time to CLK2	15			11			ns	
t111	$\overline{\text{AF32}}$ hold time to CLK2	0			0			ns	
t112	HOLD delay from CLK2			25			25	ns	
t113	$\overline{\text{READY}}$ input set-up time from CLK2	13			10			ns	
t114	$\overline{\text{READY}}$ input hold time from CLK2	5			5			ns	
t115	$\overline{\text{ATEN}}$ active delay from CLK2			20			20	ns	
t116	$\overline{\text{ATEN}}$ inactive delay from CLK2			20			20	ns	
t117	$\overline{\text{MALE}}$ active delay from CLK2			15			15	ns	
t118	$\overline{\text{MALE}}$ inactive delay from CLK2			15			15	ns	
t119	$\overline{\text{READY}}$ output active delay from CLK2			20			20	ns	
t120	$\overline{\text{READY}}$ output inactive delay from CLK2			20			20	ns	
t121	ATSCLK period	100			100			ns	
t122	ATSCLK low time	45			45			ns	at 2V
t123	ATSCLK high time	45			45			ns	at 0.8V
t124	ATSCLK rise time			8			8	ns	

Test Load = 65pF unless otherwise specified.

82C301 AC Characteristics (Continued)
(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Sym	Description	82C301-16 Min	Typ	Max	82C301-20 Min	Typ	Max	Unit	Notes
t125	ATSCLK fall time			8			8	ns	
t126	ALE delay from ATSCLK (or)			10			10	ns	
t127	$\overline{XIOR}$, $\overline{XMEMR}$, $\overline{INTA}$ active delay from ATSCLK (or)			15			15	ns	
t128	$\overline{XIOR}$, $\overline{XMEMR}$, $\overline{INTA}$ inactive delay from ATSCLK			15			15	ns	
t129	IOCHRDY set-up time to ATSCLK	17			17			ns	
t130	IOCHRDY hold time to ATSCLK	0			0			ns	
t131	$\overline{MCS16}$, $\overline{IOCS16}$ set-up time to ATS CLK	35			35			ns	
t132	$\overline{MCS16}$, $\overline{IOCS16}$ hold time from ATSCLK		25			25		ns	
t133	$\overline{MCS32}$, $\overline{IOCS32}$ set-up time to ATSCLK	35			35			ns	
t134	$\overline{MCS32}$, $\overline{IOCS32}$ hold time from ATSCLK		25			25		ns	
t135	XA0, XA1, $\overline{SBHE}$ active delay from ATSCLK			20			20	ns	
t136	XA0, XA1, $\overline{SBHE}$ inactive delay from ATSCLK			15			15	ns	
t137	$\overline{ACEN}$ active delay (read) from ATSCLK	12			12			ns	
t138	$\overline{ACEN}$ inactive delay (read) from ATSCLK		10			10		ns	
t139	AC<3:0> active delay from ATSCLK	15			15			ns	
t140	AC<3:0> inactive delay from ATSCLK			10			10	ns	
t145	$\overline{XMEMR}$, $\overline{XMEMW}$ active delay from ATSCLK (with zero command delay)	15			15			ns	
t146	$\overline{ACEN}$ active delay (write) from ATSCLK	10			10			ns	
t147	$\overline{ACEN}$ inactive delay (write) from ATSCLK	0			0			ns	
t148	$\overline{0WS}$ set-up time to ATSCLK		17			17		ns	

Test Load = 65pF unless otherwise specified.

82C301 AC Characteristics (Continued)
(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Sym	Description	82C301-16 Min	82C301-16 Typ	82C301-16 Max	82C301-20 Min	82C301-20 Typ	82C301-20 Max	Unit	Notes
t149	$\overline{0WS}$ hold time from ATSCLK	0			0			ns	
t151	$\overline{NMICS}$ setup time to $\overline{XIOW}$ active	20			20			ns	
t152	$\overline{NMICS}$ hold time from $\overline{XIOW}$ inactive	20			20			ns	
t153	Data (XD7) set-up time to $\overline{XIOW}$ inactive	30			30			ns	
t154	Data (XD7) hold time from $\overline{XIOW}$ inactive	20			20			ns	
t155	NMI delay from $\overline{XIOW}$ inactive		25			25		ns	
t156	$\overline{PORTBCS}$ set-up to $\overline{XIOR}$, $\overline{XIOW}$ active	20			20			ns	
t157	$\overline{PORTBCS}$ hold time from $\overline{XIOR}$, $\overline{XIOW}$ inactive	20			20			ns	
t158	Data (XD<7:0>) valid delay from $\overline{XIOR}$ active	15			15			ns	
t159	Data (XD<7:0>) hold time from $\overline{XIOR}$ inactive	15			15			ns	
t160	$\overline{IO2XCS}$ set-up time to $\overline{XIOR}$, $\overline{XIOW}$ active		10			10		ns	
t161	$\overline{IO2XCS}$ hold time from $\overline{XIOR}$, $\overline{XIOW}$ inactive		15			15		ns	
t162	$\overline{LPAR}$, $\overline{IOCHK}$, $\overline{PFAIL}$ pulse width		15			15		ns	
t165	REFREQ pulse width	15			15			ns	
t166	$\overline{REF}$ set-up time to ATSCLK		10			10		ns	
t167	$\overline{XMEMR}$ active delay (refresh cycle) from ATSCLK		15			15		ns	
t168	$\overline{XMEMR}$ inactive delay (refresh cycle) from ATSCLK		15			15		ns	
t169	IOCHRDY set-up time (refresh cycle) from ATSCLK	25			25			ns	
t170	IOCHRDY hold time (refresh cycle) from ATSCLK	0			0			ns	
t171	$\overline{BE<3:0>}$ active delay from XA0, XA1, $\overline{XBHE}$ valid		15			15		ns	
t172	$\overline{BE<3:0>}$ inactive delay		15			15		ns	

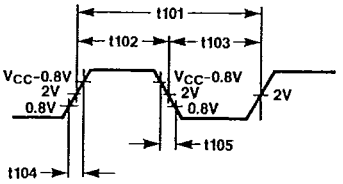
Test Load = 65pF unless otherwise specified.

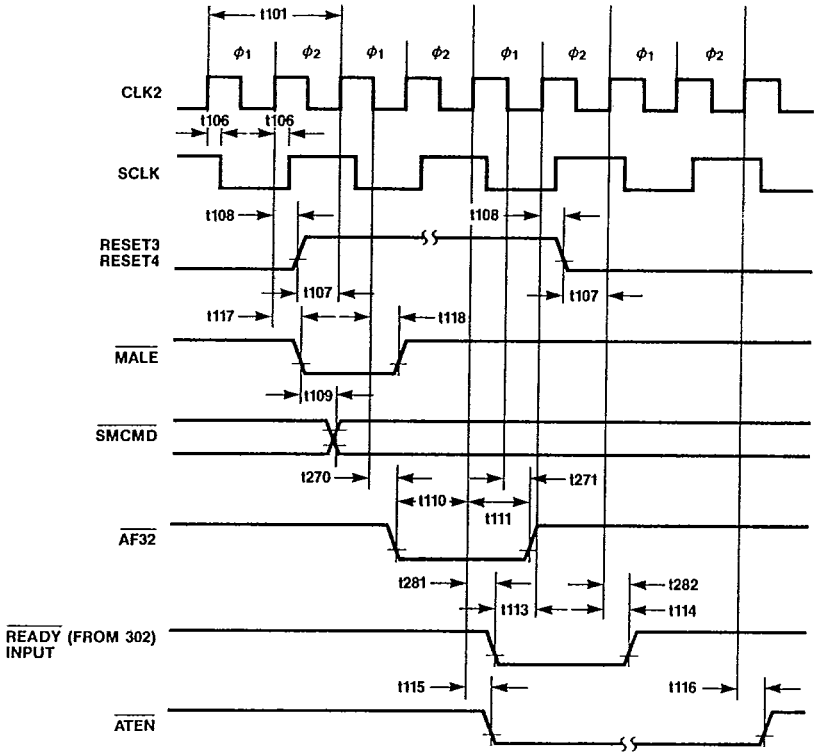
82C301 AC Characteristics (Continued)
(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Sym	Description	82C301-16 Min	82C301-16 Typ	82C301-16 Max	82C301-20 Min	82C301-20 Typ	82C301-20 Max	Unit	Notes
t173	$\overline{\text{SMCMD}}$ active delay from $\overline{\text{XMEMR}}$, $\overline{\text{XMEMW}}$ active		20			20		ns	
t174	$\overline{\text{SMCMD}}$ inactive delay from $\overline{\text{XMEMR}}$, $\overline{\text{XMEMW}}$ inactive		20			20		ns	
t175	$\overline{\text{ACEN}}$ active delay from HLDA1 active		20			20		ns	
t176	$\overline{\text{ACEN}}$ inactive delay from HLDA1 inactive		20			20		ns	
t177	AC<0:3> active delay from XA0, XA1, $\overline{\text{XBHE}}$ not valid	25			25			ns	
t178	AC<0:3> inactive delay from XA0, XA1, $\overline{\text{XBHE}}$ valid	25			25			ns	
t179	AC<0:3> active delay from $\overline{\text{XMEMR}}$ active	25			25			ns	
t180	AC<0:3> inactive delay from $\overline{\text{XMEMR}}$ inactive	25			25			ns	

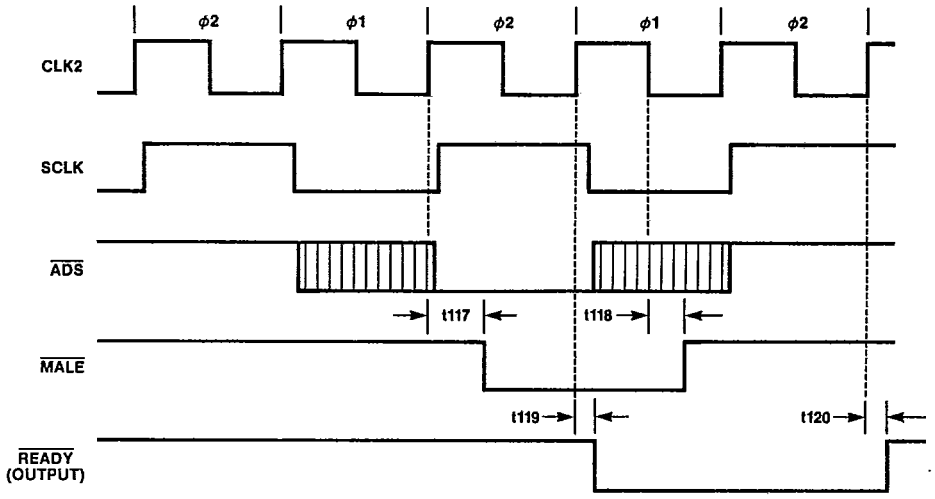
Test Load = 65pF unless specified.

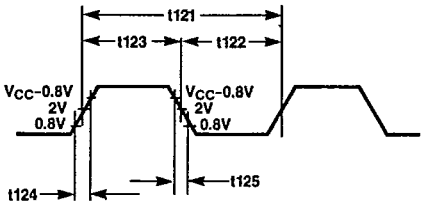
82C301 TIMING DIAGRAMS





82C301 TIMING DIAGRAMS





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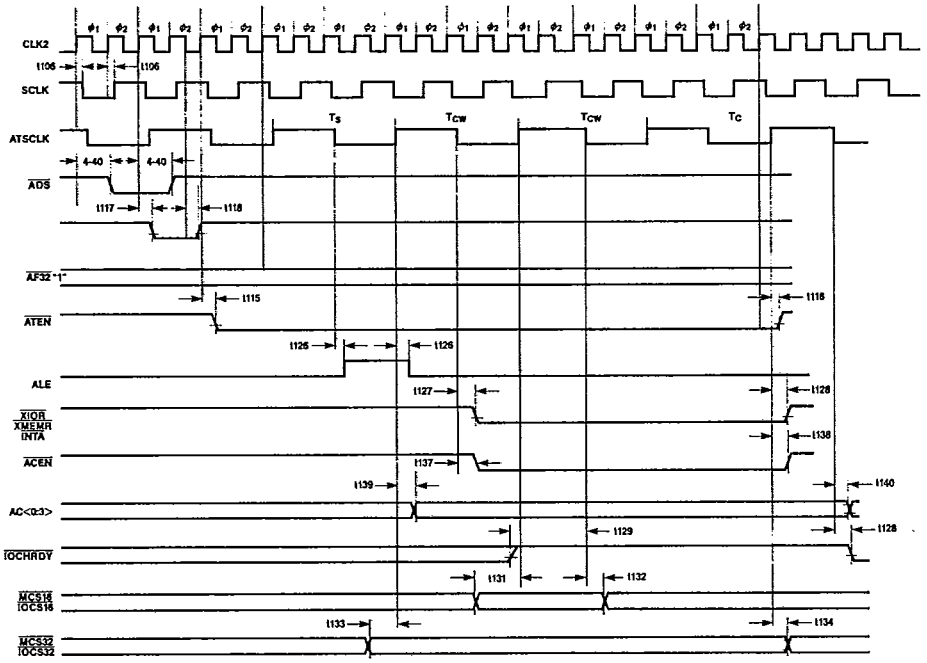

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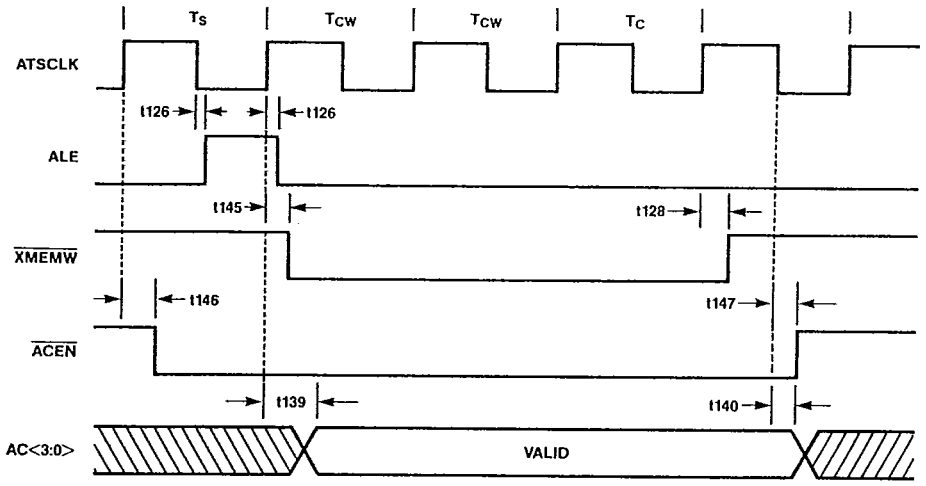
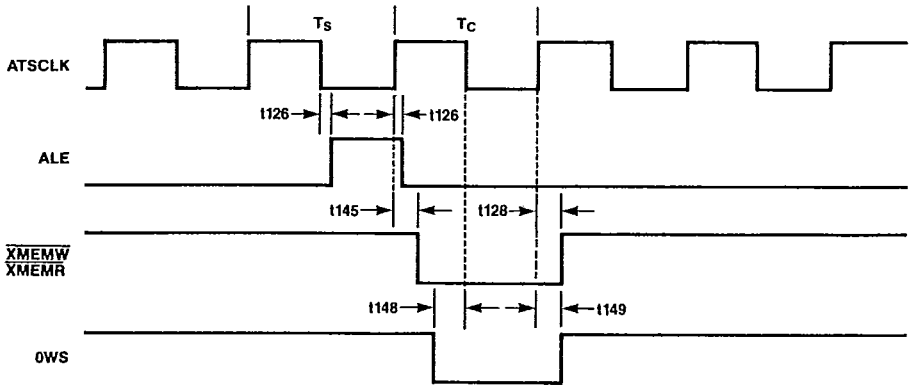
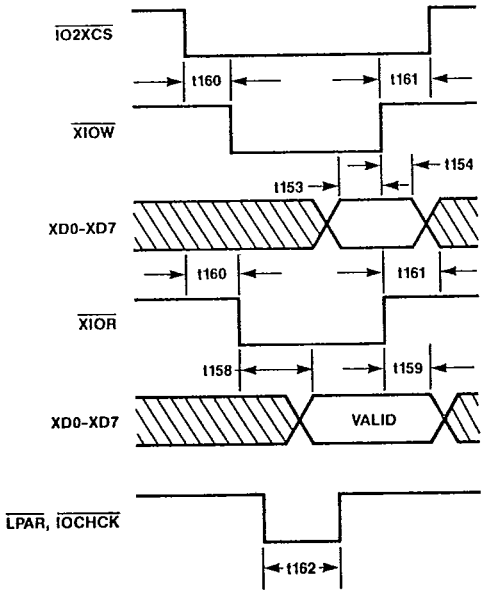
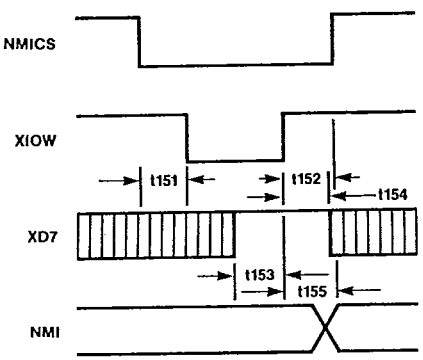
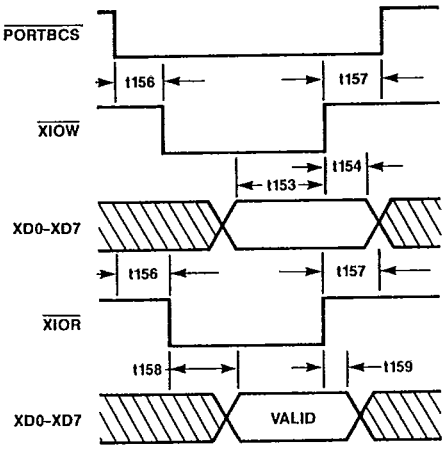




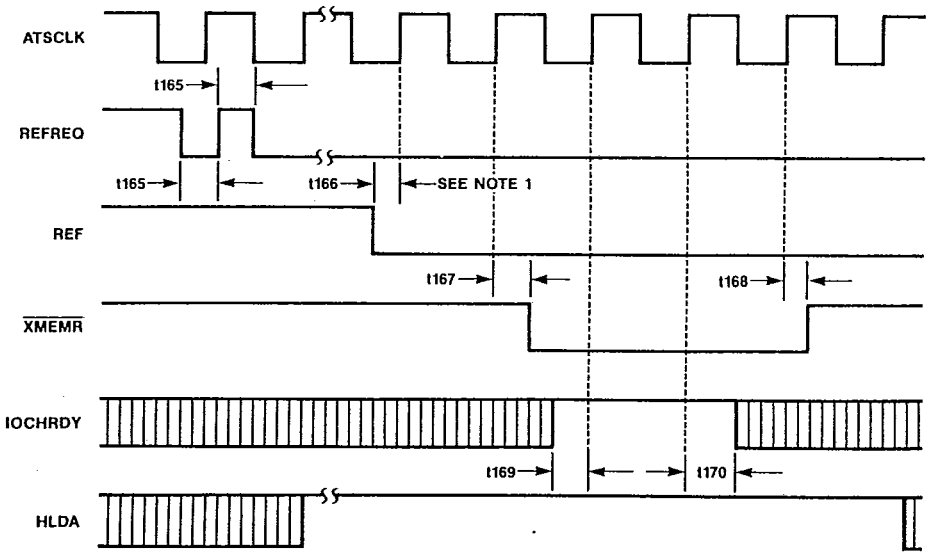
82C301 TIMING DIAGRAMS





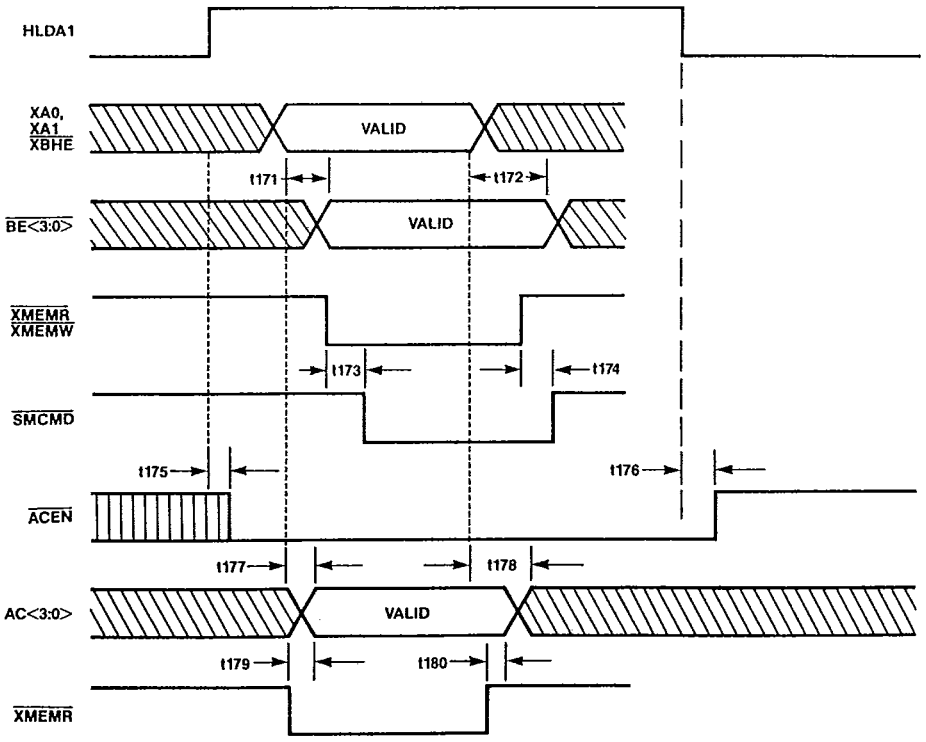


82C301 TIMING DIAGRAMS



NOTE
REF is an asynchronous signal and the setup time is specified only to guarantee starting a refresh cycle on that clock cycle instead of next one.

82C301 TIMING DIAGRAMS



82C302 Page/Interleave Memory Controller

- Page mode access with interleaved memory banks achieves higher performance than conventional DRAM arrays.
- Zero wait state access at 16MHz using 100ns DRAMs.
- Minimum configuration of 1 bank of 36 bits, 1MB using 256K x 1 or 4MB using 1M × 1 DRAMs.
- Maximum configuration of 4 banks of 36 bits, 4MB using 256K × 1 or 16MB using 1M × 1 DRAMs.
- Memory configurations of 1, 2 and 4 banks.
- Shadow RAM feature for efficient BIOS execution
- Staggered refresh to reduce power supply noise.

Overview

The 82C302 performs the memory control functions in a 80386-based systems that utilize page mode access DRAMs. The memory configurations can be one bank (non-interleaved) or multiple banks (2 or 4) interleaved on 2KB-page basis.

Array Configuration

The 82C302 organizes memory as banks of 36 bits consisting of 32 bits of data and 4 bits of parity. A common design may use either 36 by-1 DRAMs or 8 by-4 and 4 by-1 DRAMs. The minimum configuration can be a single bank operating in non-interleaved mode or can be one to two pairs of banks operating in two-way page interleaved mode at higher performance.

The memory controller is designed such that the memory can be up-graded from one to two banks by making it a two-way interleaved organization. Because of the interleaved page operation, the third and fourth banks must be added as a pair. Furthermore, the DRAM types must be identical in each bank of a pair due to the interleaved configuration. However, each pair of banks can use different DRAM types. with one or two banks of smaller DRAM types and later upgraded with additional pairs of banks of larger DRAMs.

Page Interleaved Operation

The 82C302 uses a page interleaved design that is different from most interleaved memory designs. Normal two-way interleaving uses two banks of DRAMs with even (double word) addresses stored in one bank and odd addresses in the other. If accesses are sequential (or at least to alternating even and odd addresses) the RAS precharge time of one set can be overlapped with the access time of the second set. Typically the hit rate (fraction of times that the required bank is available) is 50%. This is especially true since operand accesses (which tend to be more random) can be interspersed with (most likely sequential) instruction fetches.

Page mode operation available with most DRAMs operates because the access to the row address of the internal DRAM array makes available a large number of bits (512 bits in a 256K × 1) that are subsequently selected using the column address. Once a row access has been made higher speed random access can be made to any bit (1 of 512) within the row. The page mode access and cycle times are typically half that of the normal access and cycle times respectively. If 36 256K × 1 DRAMs are used to implement a bank, a page would have 512 × 4 bytes = 2KB. Thus memory could be interleaved on a 2KB page rather than 4 byte basis. Any access to the currently active RAS page would occur in the page access rather than the normal access time and any subsequent access could be to anywhere in the same 2KB without incurring any penalty due to RAS precharge.

When memory is configured to take advantage of this DRAM organization, significantly better performance can be achieved over normal interleaving. There are two reasons for this:

— The page mode access is faster than the normal access time. This permits more relaxed timing in order to achieve the same 0 wait-state "hit" access.

— The frequency of the next access being fast (same or alternate page vs. alternate address in interleaved mode) is significantly higher. This is because of the principle of locality of reference, instructions and data tend to be clustered together.

However, the complexity is somewhat higher in the page mode controller, making VLSI an ideal implementation vehicle.

Functional Description

The 82C302 performs four major functions as shown in figure 2-1:

- DRAM memory access arbitration
- DRAM memory access cycle control
- DRAM refresh
- Memory mapping

Memory Access State Machines and Arbitration

The 82C302 controls the DRAM memory access from three sources: CPU, DMA, and refresh requests. These accesses are arbitrated based on the inputs HLDA1 and REF and are handled by three state machines controlling each type of accesses. The CPU cycle state machine controls the memory operation for CPU accesses, the DMA cycle state machine for DMA accesses, and the refresh cycle state machine controls the DRAM refresh operation.

The refresh state machine is in control whenever REF is active. When HLDA1 is active the DMA state machine is in control. In all other cases, the CPU state machine is in control for valid DRAM memory accesses as defined by the memory map in the configuration registers. The arbitration is not preemptive in that the current active state machine always runs to completion before relinquishing the control. Therefore, it is possible for the HLDA1 with active IOR or XMEMR to prevent refresh cycles to take place.

CPU Access State Machine

The CPU initiated accesses are decoded according to the memory map defined in the configuration registers. These are the only accesses that use the page mode operation of the DRAMs. The 82C302 maintains four page registers storing the page addresses of the most recently accessed DRAM pages of the two-way page-interleaved banks. These four registers are called active page registers. Accesses to the active pages are called "hits" and are faster because the DRAM is operated in the page mode with the RAS staying asserted.

The 82C302 supports memory configurations with either one, two, or four banks. Since one active register is provided for each bank, the number of active pages varies with the amount of memory installed. In a non-interleaved minimum memory configuration only one active page register is in use. For each active page register in use, the corresponding RAS stays asserted after the previous access. If an access does not hit any active pages, a "miss" cycle, normal DRAM access cycle is entered by first de-asserting the RAS associated with the bank accessed. Refer to the timing diagram for the timing sequence for each of these cases.

RAS and CAS Generation

The 82C302 is based on 2K byte page-interleaved organization. To maintain this organization, the following table shows the address lines used for the different organizations:

For non-interleaved operation (one bank only):

	Row	Column
256K DRAM's	A<19:11>	A<10:2>
1M DRAM's	A<21:12>	A<11:2>

For interleaved memory (two or four banks):

	Row	Column
256K DRAM's	A<20:12>	A<10:2>
1M DRAM's	A<21:12>	A<22>, A<10:2>

Table 2-1. Row and Column Address Definition

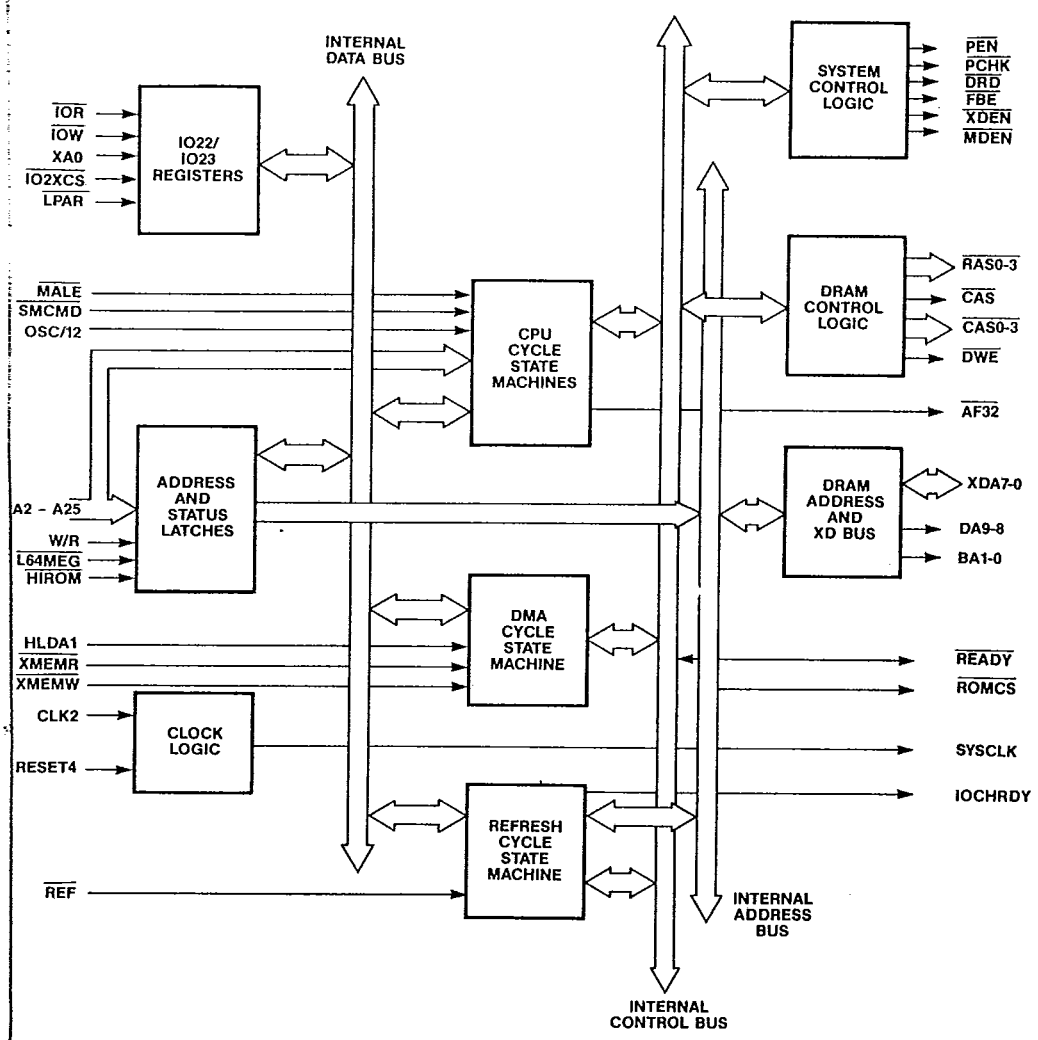


Figure 2-1. 82C302 Functional Block Diagram

In interleaved memory cases bit A<11> determines which one of the even page banks or odd page banks is accessed in the two-way interleaved organization. For 4 bank memory configurations, populated with 256K DRAMs, A<21> is used to select either RAS0 and RAS1 (A21 = 0) or RAS2 and RAS3 (A21 = 1). A<11> determines if the even bank (A11 = 0), Bank 0 or Bank 2) or the odd bank (A11 = 1, Bank1, Bank3) is accessed in a two way interleaved organization.

For 4 bank memory configurations, populated with 1 Megabit DRAMs, A<23> is used to select either RAS0 and RAS1 (A23 = 0) or RAS2 and RAS3 (A23 = 1). A<11> determines if the even or the odd bank is currently being accessed.

When 256K and 1 MBit DRAMs are used, it is required that 1 MBit DRAMs occupy the first two banks and the 256K DRAMs occupy the second two banks. This constraint is there to ensure that there will not be a hole in the address space without actual DRAMs. Figure 2.2 shows the memory addressing scheme for the allowable memory configurations.

RAS Timeout

When using DRAM page mode, the maximum RAS pulse width must be observed. For most DRAMs this is 10 microseconds (although some have 30 or 100 microsecond limits). Timers are maintained for each bank to assure data integrity using the OSC/12 (1.19MHz = 840nS) clock available on the system board. RAS is de-asserted for each bank when its counter times out at about 10 microseconds intervals. The RAS time out feature can be disabled by disconnecting the OSC/12 input.

CPU Access Cycles Sequences

There are many basic CPU memory access patterns: memory read-hit access, memory write-hit access, memory read-miss access, and memory write-miss access, and CPU IO access to 82C301 configuration registers. These basic access sequences and timing for the critical signals are shown in the timing charts. In addition to these basic patterns, the configuration register REG13H<6> may be programmed to have one wait state inserted for supporting slow DRAM's. Note that the default setting after the system reset is for one wait state insertion.

DMA Access State Machine

DMA accesses are initiated by asserting HLDA1. The XMEMR an IOR determines if it is a read or a write memory access. The bytes accessed are controlled externally with the BE<3:0> signals generated by the 82C301 Bus Controller. The DMA state machine makes one memory access per DMA bus cycle and does not attempt to pack or unpack data transfers to make full 32-bit transfers. Refer to the timing charts for a DMA access cycle sequence and timing.

EPROM and DRAM Control Logic

The EPROM and DRAM control logic in the 82C302 is responsible for the generation of RAS, CAS and DWE signals for DRAM accesses and the generation of ROMCS for EPROM accesses. This module also generates READY to the CPU upon completion of the local 32-bit DRAM access. The 82C301 generates the READY for the ROM access. CPU, DMA and refresh addresses use DA<9:8>, XDA<0:7> and BA<1:0> (Note that in the current version of the 82C302, the signals BA<1:0> default to zero). The system control logic provides MDEN to control the buffer chips. MDEN enables the data buffers on the 82A305 for the MD bus for non-refresh DRAM cycles.

System Control Logic

This module of the 82C302 generates the MDEN, MDRD, CAS (DLE), XDEN and AF32 for system control. XDEN is issued for I/O accesses to the internal configuration registers on the 82C302. It is used to enable the XD<7:0> onto the XDA<7:0> address lines from an external buffer, for accessing the internal registers. MDEN and MDRD are generated for enabling and controlling the data buffers between the MD data bus and the CPU data bus. AF32 is issued by the 82C302 CPU state machine. It is activated for local 32 bit memory cycles and satisfies the setup and hold requirement with respect to CLK2 of the 82C301 bus controller.

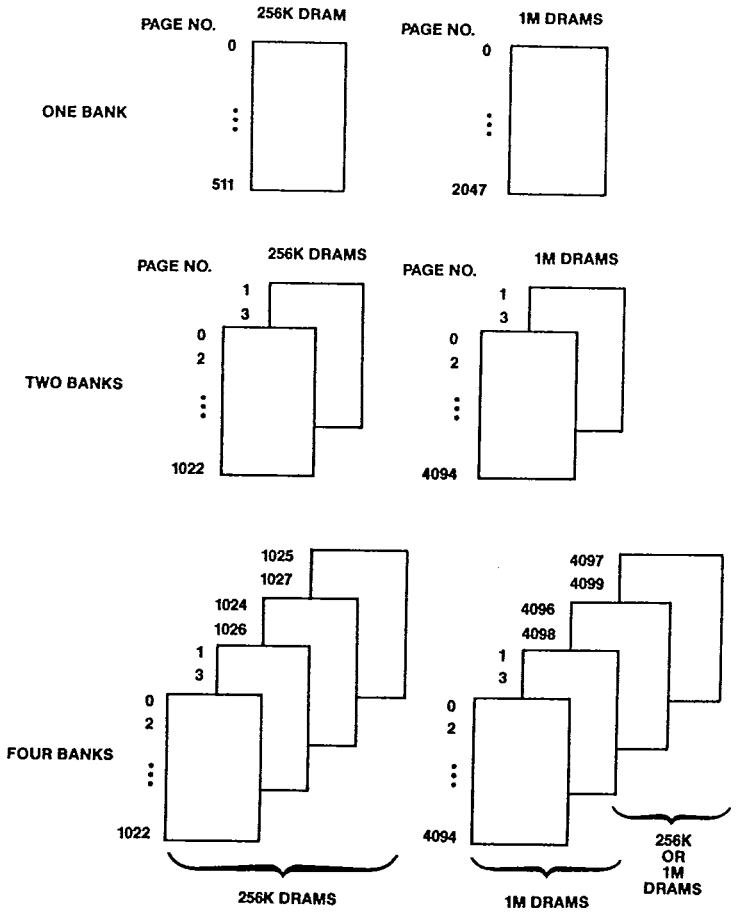


Figure 2-2. Memory Addressing

Refresh Cycles

To reduce power supply noise generation due to the surges caused during RAS transitions, RAS pulses to each bank are staggered by one CLK2 cycle, as shown in Figure 2-3. Because all RAS's could be active for page mode operation, a refresh cycle requires that all RAS's be first de-asserted for the RAS pre-charge period. IOCHRDY is activated low, to extend the cycle. Following the RAS pre-charge period, RAS0 is asserted, followed by RAS1 after a CLK2 cycle delay. RAS3 and RAS4 are also staggered by one CLK2 cycle. IOCHRDY is deasserted in the middle of RAS3 low time, to terminate the refresh cycle.

Memory Mapping Logic

The configuration registers REG08H to REG13H define what is a valid local memory access, and what is a ROM memory access according to the local bus addresses. REG08H and REG09H determines how ROM areas (as defined by an IBM PC AT) between the 768K to 1M address range are accessed.

For valid local memory accesses it asserts the AF32 to indicate that it has control of the local bus and also asserts the READY signal at the end of the access cycle. If an access is a ROM access, it asserts LDAC to provide controls for the ROM's or PROM's; in this case, the READY signal must be provided to the CPU and 82C302 by another source (82C301 will provide this signal in a chip set solution).

Shadow RAM Feature

For efficient BIOS execution, it is preferable to execute BIOS from the fast RAM rather than from the slower EPROM devices. The 82C302 supports the shadow RAM feature, which if invoked, allows the BIOS code to be executed from the system RAM resident at the same physical address as the BIOS EPROM. It is the responsibility of the system software to transfer the code stored in BIOS EPROMs to system RAM before enabling the shadow RAM feature. Shadowing EPROMs into RAM significantly improves performance in BIOS call intensive applications. Performance improve-

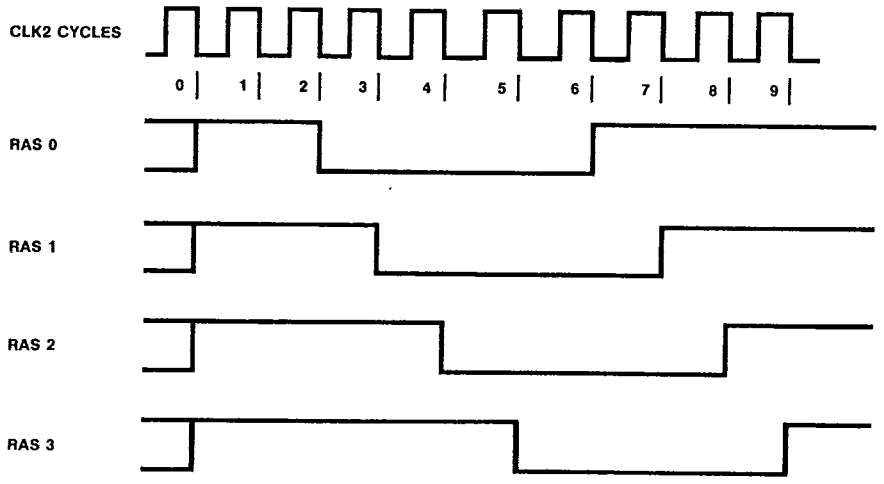


Figure 2-3. Staggered RAS pulses during refresh

ments as high as 300 to 400% have been observed in bench mark tests on shadow RAM. The shadow RAM feature is invoked by enabling the corresponding bits in the ROM enable register and the RAM mapping registers.

Clock, Reset and Other Miscellaneous Logic

The RESET4 input causes all internal registers to be reset to their default values. Configuration registers not specified with a default value are not reinitialized and may not retain its old value. The system control logic generates the RESETand MEMRsignals to be used for enabling parity error checking.

Configuration/Diagnostic Registers

There are 14 bytes of configuration and diagnostic registers in the 82C302. These are accessed through IO ports 22H and 23H normally found in the interrupt controller. Accesses to these configuration and diagnostic registers are done first by writing the index of the desired register into port 22H and then followed by an access (either read or write) to 23H for the data. XDEN is asserted for these accesses to control the buffer connecting the XD and XDA buses.

Memory Configuration Registers

The configuration registers REG08H to REG0FH are used to control how the CPU memory accesses are defined. They define all address as ROM accesses, system memory accesses (or DRAM accesses for short), other local CPU bus accesses, or as IO channel accesses . These provisions are made because the low one megabyte is both occupied by DRAM's, ROM's and also devices on the AT bus. For ROM accesses it generates the LDAC to control the PROM access; for system memory accesses it generates the necessary DRAM controls to the system memory under its control; it generates AF32 for all other local CPU bus accesses; and it does not control the IO channel accesses.

The 82C302 provides three 256KB areas where the ROM's can be located. The low ROM space is located just below the 1MB address, the middle ROM space is located below 16MB address, and the high ROM space is below 4GB address. The low ROM is used for 8086 compatible operation, the middle ROM is for 80286, and the high ROM is for 80386. Upon system reset, the default configuration register setting causes accesses to these three ROM areas to generate LDAC. With the exception of the high ROM area which is always recognized as ROM accesses, the other two ROM areas can be mapped to be either ROM or RAM accesses.

After reset, REG08<4:3> may be programmed to make the entire middle ROM area mapped to DRAM and with write protection if desired. REG08H<2> determines if the 82C301 recognizes the addresses generated beyond 16 MB as local CPU bus cycles. REG08H<1> is used to enable REG0AH to REG0FH which controls the "Low Meg DRAM" (40000H to FFFFFH) address mapping for 256KB to 1MB addresses in 16 KB blocks. This bit defaults upon reset so that only the 0 to 256KB areas are accessible. Accesses to the low megabyte DRAM can be made by enabling the mapping after the necessary configuration registers are correctly programmed. REG08H<0> defaults to single bank memory configuration upon reset and must be programmed to enable page/ interleaved operation.

The REG09H control the address mapping and write protection for the low ROM area (from C0000H to FFFFFH) in 64KB blocks. REG0AH to REG0FH define for each 16 KB address range if it is a DRAM block in the system memory or on the IO channel.

INDEX	7	6	5	4	3	2	1	0	
08H	0	VERS		MW	MR	HM	SM	NI	IDENTIFICATION
09H	R3	R2	R1	R0	D3	D2	D1	D0	ROM CONFIGURATION
0AH	368K						256K		MEMORY ENABLE (16KB RESOLUTION)
0BH	496K						384K		•
0CH	624K						512K		•
0DH	752K						640K		•
0EH	880K						768K		•
0FH	1008K						896K		MEMORY ENABLE (16KB RESOLUTION)

Figure 2-5 Control and Address Space Map Register Summary

Index	Bits	Function
08H		Identification
	7	Controller Type Part type
		0 Interleaved Memory Controller (82C302)
	6:5	Version
		0 Initial
	4	MW - Middle Boot Space Write Protect. This bit is used in conjunction with bit 3 allowing the BIOS code to be copied into RAM and write protected at this location as well as below 1MB. It should only be used if there is RAM present at this address (16MB installed). Executing out of RAM will result in better performance than out of narrower (usually 8 or 16 bits) EPROMs.
		0 Read/Write of 256KB RAM at 16128K 00FC0000H. Default. 1 Read-Only of 256KB RAM at 16128K 00FC0000H
	3	MR - Middle Boot ROM disable
		0 The boot/BIOS ROM located just below 16MB is enabled. This is necessary for 286 compatibility. Default. 1 The boot/BIOS ROM located just below 16MB is disabled.
	2	HM - 16MB IO Channel Memory Limit
		0 $\overline{AF32}$ will not be asserted for addresses ≥ 16MB. This should only be used if external logic can recognize addresses above 16MB. Default. 1 $\overline{AF32}$ is asserted for addresses ≥ 16MB (01000000H). Since IO channel memory cannot normally be configured above 16MB, accessing above 16MB will cause a READY timeout if that feature is enabled. This is necessary during setup because memory address above 16MB that are not enabled for local memory could wrap into a valid IO channel memory location.
	1	SM - Minimum memory configuration after reset. Used during initialization.
		0 256K only enabled. Default. Ignore memory address configuration registers 0AH to 0FH. 1 Normal configuration controlled by registers 0AH to 0FH.
	0	NI - Single bank/interleave select 0 Disable interleave (single bank). Default. 1 Enable interleave

Table 2-2 Memory Configuration Register Definition

Index	Bits	Function
09H		RAM/ROM Configuration in boot area.
	7	RAM at 768K C0000-CFFFFH (EGA)
	6	RAM at 832K D0000-DFFFFH
	5	RAM at 896K E0000-EFFFFH
	4	RAM at 960K F0000-FFFFFH (BIOS)
		Bits 7:4 disable writing to RAM located in the BIOS area in 64KB blocks. BIOS data.
		0 Read/Write. Default. 1 Read-Only
	3	ROM at 768K C0000-CFFFFH (EGA)
	2	ROM at 832K D0000-DFFFFH
	1	ROM at 896K E0000-EFFFFH
	0	ROM at 960K F0000-FFFFFH (BIOS)
		Bits 3:0 enable substitution of the BIOS ROM located below 1MB with RAM at the same location in 64KB blocks. This should be done after the BIOS code is copied from the ROM and the RAM locations have been write protected using bits 7:4.
		0 Disabled 1 Enabled. Default.
0AH		Address Map 256K 040000-05FFFFH (16K Resolution)
0BH		Address Map 384K 060000-07FFFFH
0CH		Address Map 512K 080000-09FFFFH
0DH		Address Map 640K 0A0000-0BFFFFH
0EH		Address Map 768K 0C0000-0DFFFFH
0FH		Address Map 896K 0E0000-0FFFFFH
		0 Address is on or controlled by the system board 1 Address is on the IO Channel.
		This permits 16K blocks of memory to be disabled allowing ROMs, memory expansion mechanisms (EMS or XMA) or memory mapped IO devices to reside within the lower 1MB address space.

Table 2-2. Memory Configuration Register Definition

DRAM Array Configuration and Timing

The configuration registers REG10H to REG13H provides the DRAM type definition and starting address for each pair of banks, banks 0 and 1, and banks 2 and 3. The REG10H<7:6> and REG12H<7:6> defines if the DRAM's are enabled, uses 256K DRAM's, or uses 1M DRAM's. These bits defaults to 256K DRAM's upon reset. The REG10H<6:0> and REG12H<6:0> defines the address bits <25:20> of the starting address of the pairs of banks. Some of these bits may not be valid because the memory banks must start at some predefined boundaries. For 256K DRAM's, all bits <25:20> are valid if only single bank is enabled -it can be on any 1MB boundary; otherwise only bits <25:21> are valid starting address bits on 2MB boundaries. For 1M DRAM's, only bits <25:23> are valid forcing it on 8 MB boundaries. The REG11H<7> and REG13H<7> define the RAS precharge time required when a page miss occurs so that DRAM's of different speeds can be supported for each pair of banks. The REG11H<6> and REG13H<6> define the wait state to be inserted to meet the DRAM speed. These parameters default to the slower timing upon reset so that the system can be powered up with minimal assumptions on the DRAM speed and the memory configuration. Refer to Table 2-3 for details of the bit definitions.

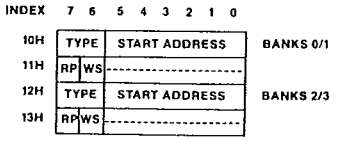


Figure 2.6. DRAM Configuration/Timing Register Summary

Index	Bits	Function
10H		bank 0/1 Type/Start Address
12H		bank 2/3 Type/Start Address
	7:6	DRAM Type
		0 none (bank disabled)
		1 256K words, default value for REG10H and REG12H
		2 1M words
		3 Reserved
	5:0	Starting Address 25:20 The DRAM type determines which address bits are valid in the address recognition process. This field of REG10H defaults to zero after reset.
		25:20 256K DRAM's. 1MB boundary 1MB per bank, single bank only. Valid for the first register only.
		25:21 256K DRAM's. 2MB boundary 1MB per bank, two banks required for interleaved operation.
		25:23 1M DRAM's. 8MB boundary 4MB per bank, two banks required for interleaved operation.

Table 2-3 DRAM Configuration and Timing Register Definition

Index	Bits	Function
11H		banks 0/1 Timing
13H		banks 2/3 Timing
	7	DRAM RAS precharge. Specifies the amount of time for RAS precharge when a page miss occurs. 0 3 CLK2 times (93 nS at 16MHz) 1 5 CLK2 times (155nS at 16MHz). Default.
	6	Access wait states Specifies the number of wait states in SCLK units to allow the use of slower DRAMs. 0 0 wait-state 1 1 wait-state. Default.
	5:0	Reserved

Table 2-3 DRAM Configuration and Timing Register Definition (Continued)

Diagnostic Access Register

REG28H<7> controls the parity check enable and defaults to "disable" after reset. This bit generates the $\overline{PEN}$ signal for enabling the parity check by 82A306. When parity errors occur REG28H<1:0> and REG29H<7:0> will latch the error address <25:16>.

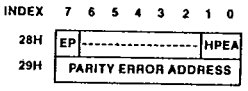


Figure 2.7. Diagnostic Access Register Summary

Index	Bits	Function
28H		Error Source/Address (MSBs)
	7	Parity check disable 0 Enabled 1 Disabled (default)
	6:2	Not used, returns unpredictable value.
	1:0	High Parity Error Address bits <25:24>
29H		Parity Error Address (LSBs)
	7:0	Error address bits <23:16>

Table 2-4. Diagnostic Access Registers Definition

82C302 AC Characteristics

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Sym	Description	82C302-16 Min	Typ	Max	82C302-20 Min	Typ	Max	Unit	Notes
t200	CLK2 input cycle time (t0 used as refer)	31			25			ns	
t201	CLK2 fall time	2		5	2		5	ns	
t202	CLK2 rise time	2		5	2		5	ns	
t203	CLK2 low time	10			9			ns	at 2V
t204	CLK2 high time	10			9			ns	at 2V
t205	RESET hold time	6			6			ns	
t206	RESET set-up time	5			5			ns	
t207	SCLK delay time	6	12	22	6	12	22	ns	
DMA Sequence									
t210	$\overline{RAS}i$ de-assertion time from HLDA1	13			13			ns	
t211	$\overline{RAS}i$ active delay from commands active	17		25	17		25	ns	
t212	Address set-up time to commands active	35			35			ns	
t213	Address hold time from commands inactive	0			0			ns	
t214	$\overline{AF32}$ active time from commands active	22	26		22	26		ns	
t215	$\overline{DRD}$ active time from commands active	10		25	10		25	ns	
t216	Row address set-up time to $\overline{RAS}$ active	10			10			ns	
t217	Row address hold time from $\overline{RAS}$ active	15			15			ns	
t218	$\overline{CAS}i$ active delay from $\overline{RAS}$ active for DMA memory read cycle	1.0 to			1.0 to			ns	
t219	$\overline{CAS}i$ active delay from $\overline{RAS}$ active for DMA memory write cycle	1.5 to			1.5 to			ns	
t220	$\overline{DWE}$ active delay from $\overline{RAS}$ active	0.5 to			0.5 to			ns	
t221	$\overline{READY}$ active delay from $\overline{RAS}$ active	1.5 to			1.5 to			ns	
t222	$\overline{RAS}i$ de-assertion time from commands inactive			15			15	ns	

Test Load = 65pF unless otherwise specified.

82C302 AC Characteristics (Continued)
(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Sym	Description	82C302-16 Min	82C302-16 Typ	82C302-16 Max	82C302-20 Min	82C302-20 Typ	82C302-20 Max	Unit	Notes
DMA Sequence									
t223	Column address hold time from commands active	16			16			ns	
t224	$\overline{CASi}$ de-assertion from commands inactive		22	28		22	28	ns	
t225	$\overline{AF32}$ tri-state delay from commands inactive		21	25		21	25	ns	
t226	$\overline{DWE}$ de-assertion time from commands inactive		11	15		11	15	ns	
t227	READY de-assertion time from commands inactive		16			16		ns	
t228	$\overline{DRD}$ de-assertion time from commands inactive		12			12		ns	
ROMCS Sequence									
t235	$\overline{ROMCS}$ active delay from CLK2			27			27	ns	
t236	$\overline{ROMCS}$ inactive delay from CLK2			22			22	ns	
t237	$\overline{READY}$ input set-up time to CLK2	8			8			ns	
t238	$\overline{READY}$ input hold time from CLK2	0			0			ns	
REFRESH Sequence									
t240	IOCHRDY going low from $\overline{REF}$ active		14	18		14	18	ns	
t241	IOCHRDY float delay from CLK2		18	25		18	25	ns	
t242	$\overline{RAS0}$ precharge time		3 to			3 to		ns	
t243	$\overline{RASi}$ (0 to 3) pulse width		4 to			4 to		ns	
t244	$\overline{RAS(i+1)}$ active delay from $\overline{RASi}$ active		1 to			1 to		ns	
t245	Refresh address set-up time to $\overline{RASi}$		3 to			3 to		ns	
t246	Refresh address hold time from $\overline{RASi}$		2 to			2 to		ns	
t247	$\overline{RASi}$ inactive delay from CLK2		14	18		14	18	ns	
t248	$\overline{RASi}$ active delay from CLK2		15	18		15	18	ns	

Test Load = 65pF unless otherwise specified.

82C302 AC Characteristics (Continued)
(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Sym	Description	82C302-16 Min	Typ	Max	82C302-20 Min	Typ	Max	Unit	Notes
IO Read/Write Sequence									
t250	$\overline{IO2XCS}$ set-up time to $\overline{XIOR}$ or $\overline{XIOW}$	10			10			ns	
t251	XA0 set-up time to $\overline{XIOR}$ or $\overline{XIOW}$	10			10			ns	
t252	$\overline{IOCS16}$ hold time from $\overline{XIOR}$ or $\overline{XIOW}$	15			15			ns	
t253	XA0 hold time from $\overline{XIOR}$ or $\overline{XIOW}$	15			15			ns	
t254	$\overline{XDEN}$ active delay from $\overline{XIOR}$ or $\overline{XIOW}$	15		19	15		19	ns	
t255	$\overline{XDEN}$ inactive delay from $\overline{XIOR}$ or $\overline{XIOW}$	12			12			ns	
t256	XDA<7:0> input set-up time to $\overline{XIOW}$	10			10			ns	
t257	XDA<0:7> input hold time to $\overline{XIOW}$	8			8			ns	
t258	XDA<7:0> output valid delay from $\overline{XIOR}$			37			37	ns	
t259	XDA<7:0> hold time from $\overline{XIOR}$			15			15	ns	
CPU to Memory Sequence									
t260	$\overline{MALE}$ active setup time to CLK2	5			5			ns	
t261	$\overline{MALE}$ inactive delay from CLK2	10			10			ns	
t262	Address/Status set-up time to CLK2	10			10			ns	
t263	Address/Status hold time from $\overline{MALE}$	10			10			ns	
t264	$\overline{L64MEG}$, $\overline{HIROM}$ set-up time to CLK2	10			10			ns	
t265	$\overline{L64MEG}$, $\overline{HIROM}$ hold time to $\overline{MALE}$	10			10			ns	
t266	$\overline{SMCMD}$ active delay from $\overline{MALE}$	10			10			ns	

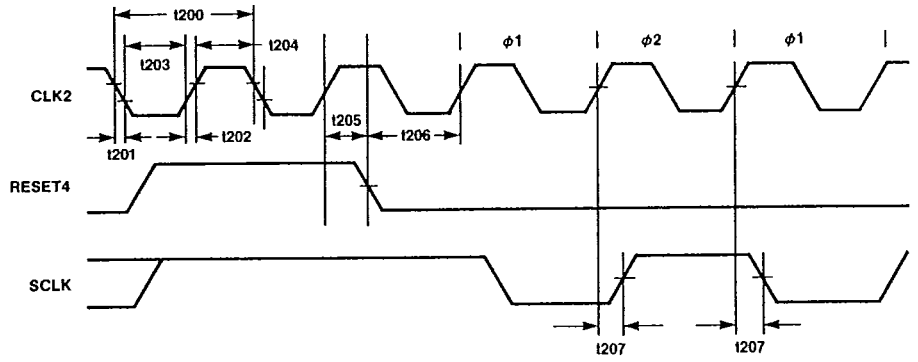
Test Load = 65pF unless otherwise specified.

82C302 AC Characteristics (Continued)
(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

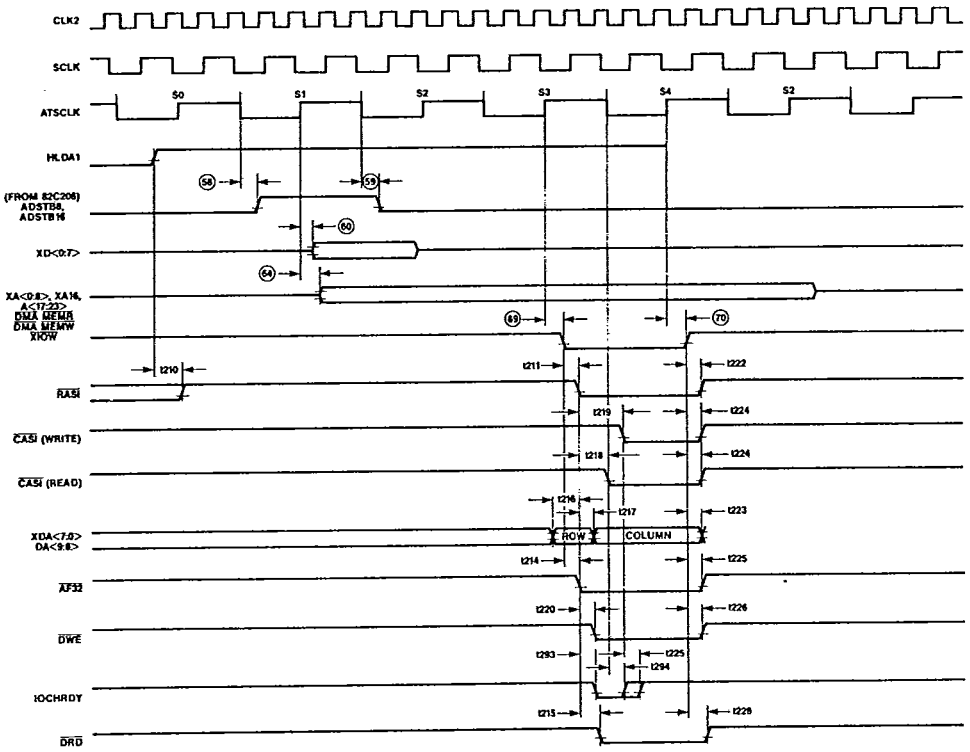
Sym	Description	82C302-16 Min	Typ	Max	82C302-20 Min	Typ	Max	Unit	Notes
CPU Cycle Timing									
t270	$\overline{AF32}$ active delay from CLK2			26			23	ns	C_L=35pF
t271	$\overline{AF32}$ inactive delay from CLK2		17	20		14	18	ns	
t272	$\overline{CASi}$ active delay from CLK2 for read hit cycles			13			11	ns	C_L=35pF
t272	$\overline{CASi}$ inactive delay from CLK2	12		17	12		17	ns	
t274	$\overline{CAS}$ active delay from CLK2 for read hit cycles	13		18	13		18	ns	
t275	$\overline{CAS}$ inactive delay from CLK2	18			18			ns	
t276	Column address stable from $\overline{MALE}$			25			25	ns	
t277	$\overline{DRD}$ active delay from CLK2		21	30		21	30	ns	
t278	$\overline{DRD}$ inactive delay from CLK2		17	22		17	22	ns	
t279	$\overline{FBE}$ active delay from CLK2		23	25		23	25	ns	
t280	$\overline{FBE}$ inactive delay from CLK2			20			20	ns	
t281	$\overline{READY}$ active delay from CLK2			18			15	ns	
t282	$\overline{READY}$ inactive delay from CLK2			18			18	ns	
t283	$\overline{RASi}$ active delay from CLK2	10	15	18	10	13	16	ns	C_L=35pF
t284	Row address set-up time to $\overline{RASi}$	10			10			ns	
t285	Row address hold time from CLK2	15			15			ns	
t286	$\overline{CASi}$ active delay from CLK2			18			18	ns	
t287	$\overline{CAS}$ active delay from CLK2			22			22	ns	
t288	$\overline{RASi}$ inactive delay from CLK2			18			18	ns	
t289	$\overline{RASi}$ precharge time		3 to			3 to		ns	
t290	$\overline{CASi}$ precharge time		1.5 to			1.5 to		ns	
t291	$\overline{DWE}$ active delay from CLK2			18			18	ns	
t292	$\overline{DWE}$ inactive delay from CLK2			19			19	ns	

Test Load = 65pF unless otherwise specified.

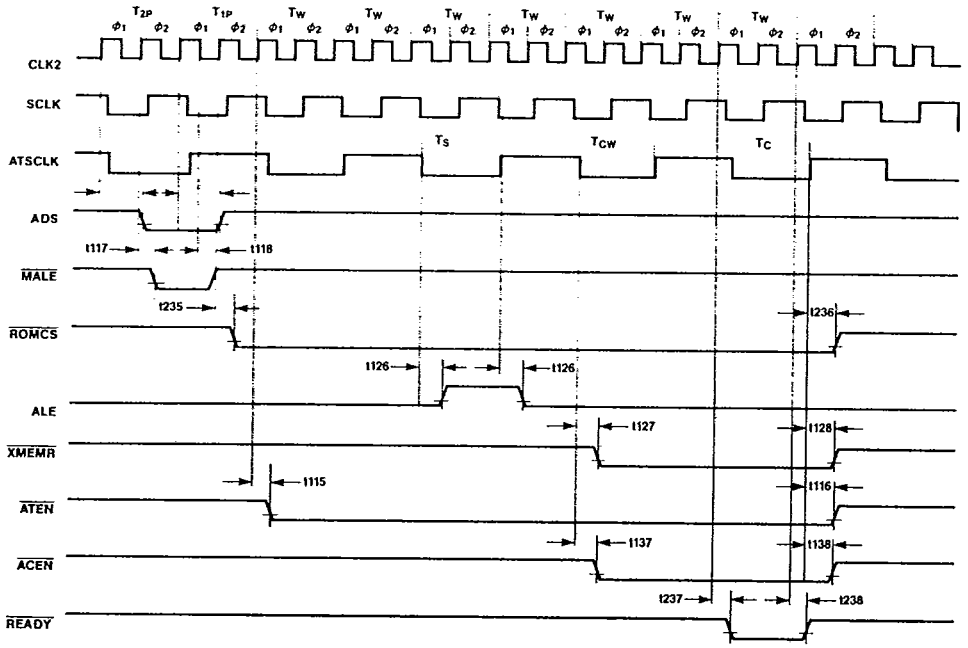
82C302 TIMING DIAGRAM (RESET SEQUENCE)



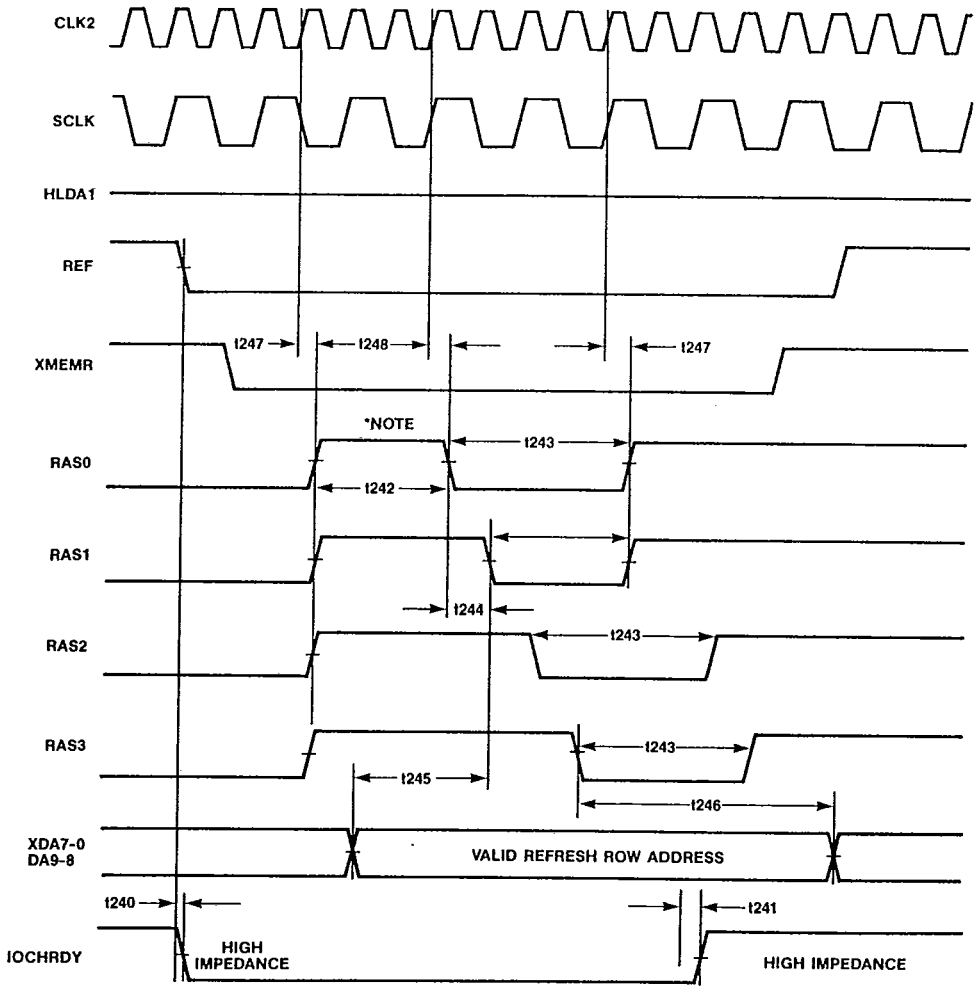
82C302 DMA Cycle



82C302 ROM Read Cycle

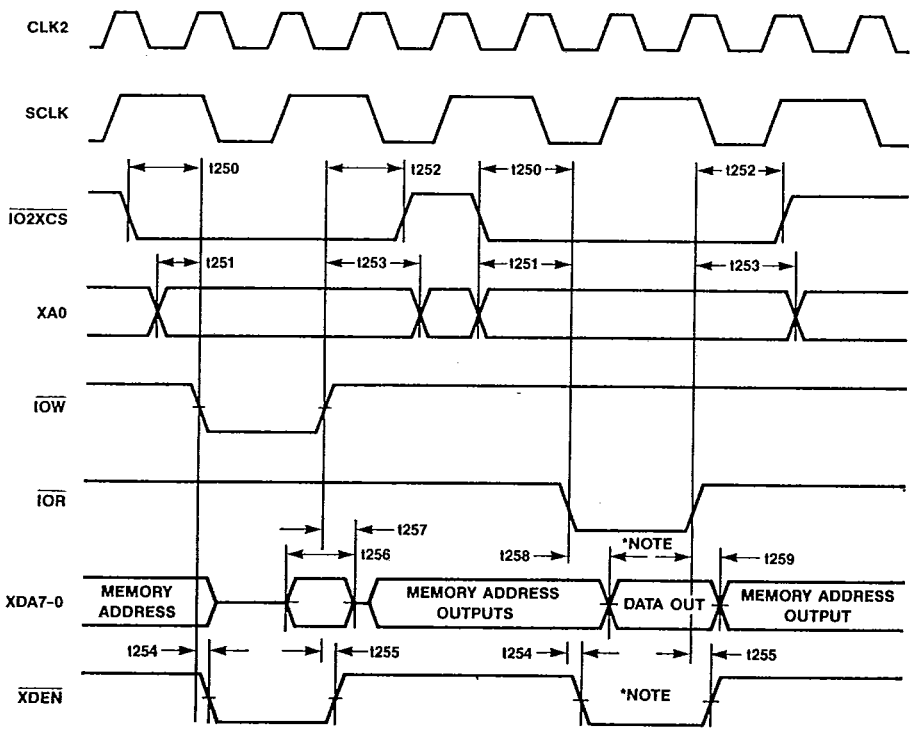


82C302 REFRESH CYCLE WAVEFORM



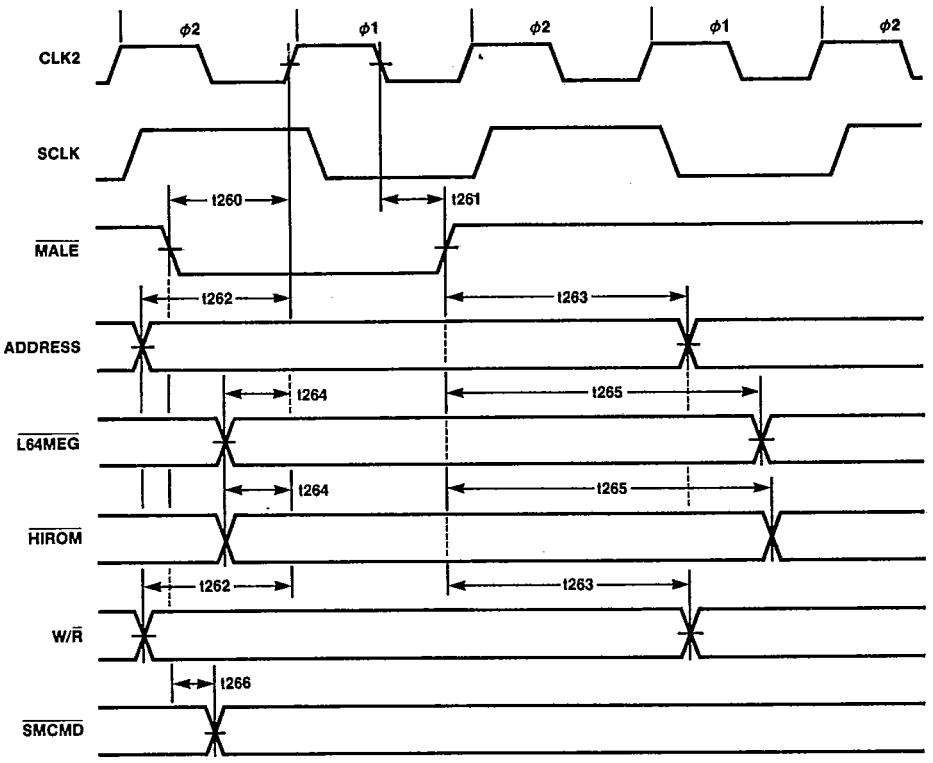
***NOTE:** Add 2 more clock cycles if either Bit 7 of register 11 is 1 or Bit 7 of register 13 is 1.

82C302 TIMING DIAGRAM (IO READ/WRITE)

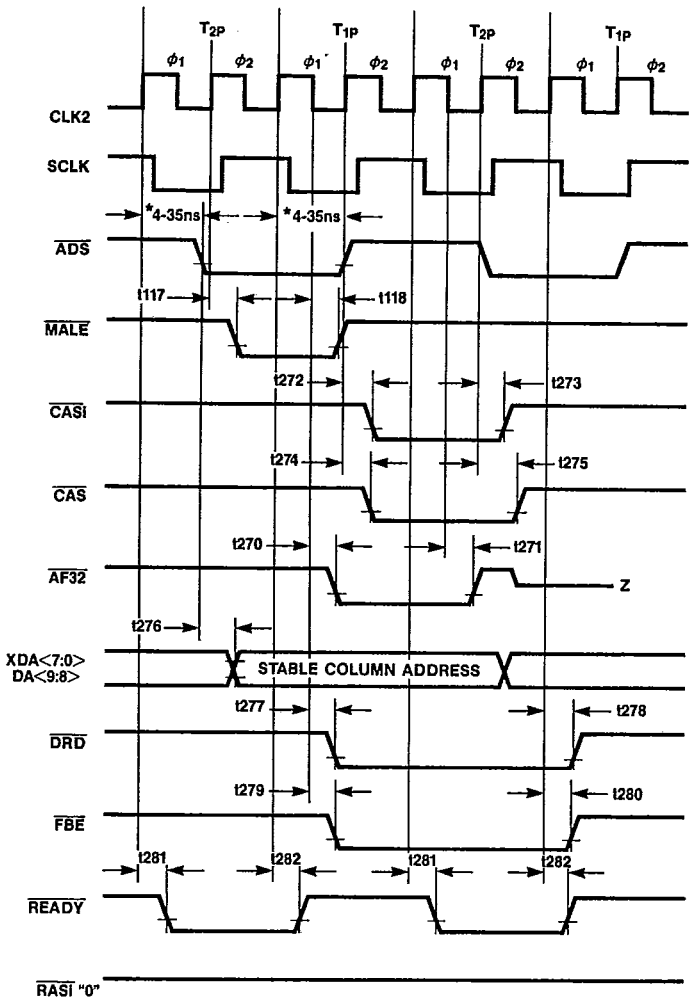


***NOTE:** No data output and XDEN is inactive if the index set up by the previous IO22 Write doesn't point to a valid IO23 register of 82C302.
Valid registers of IO23: 08H-0FH, 10H-13H, 28H-29H.

82C302 TIMING DIAGRAM (INPUT SETUP/HOLD TIME FOR CPU CYCLES)

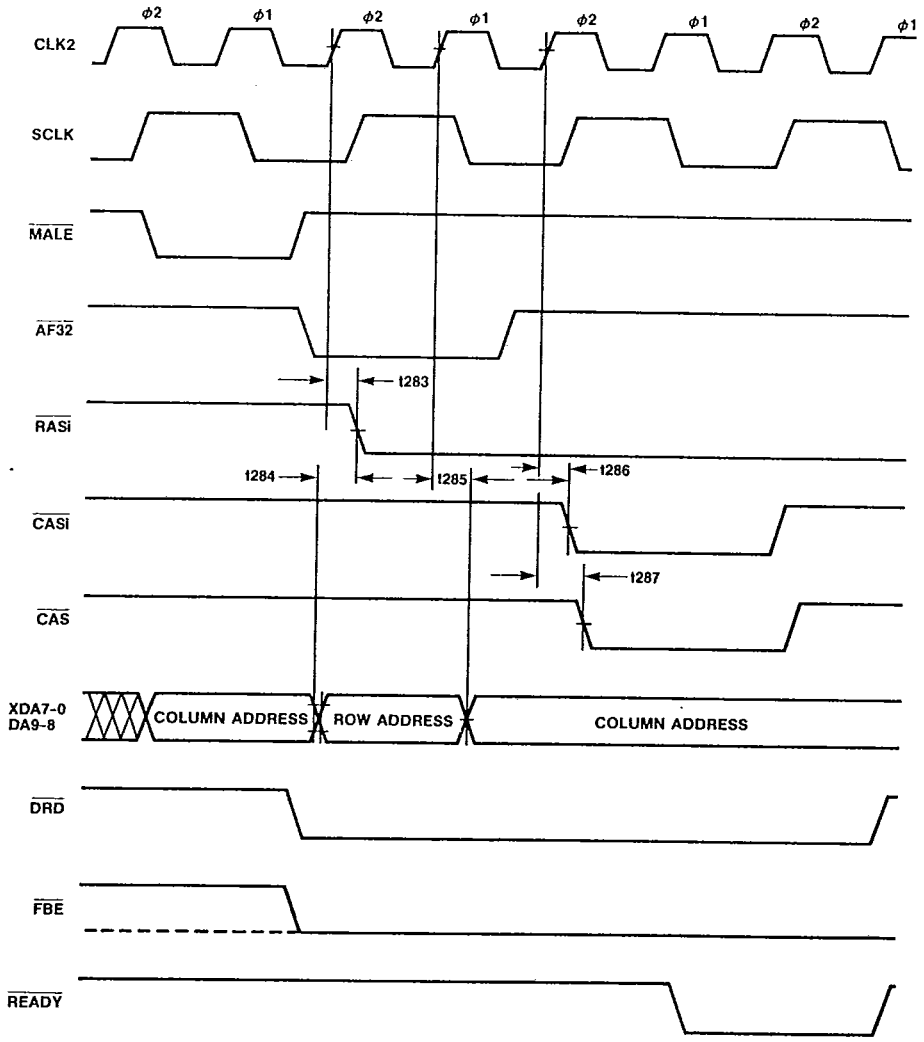


82C302 Timing Diagram (CPU to Local Memory Cycle) Read Hit 0WS

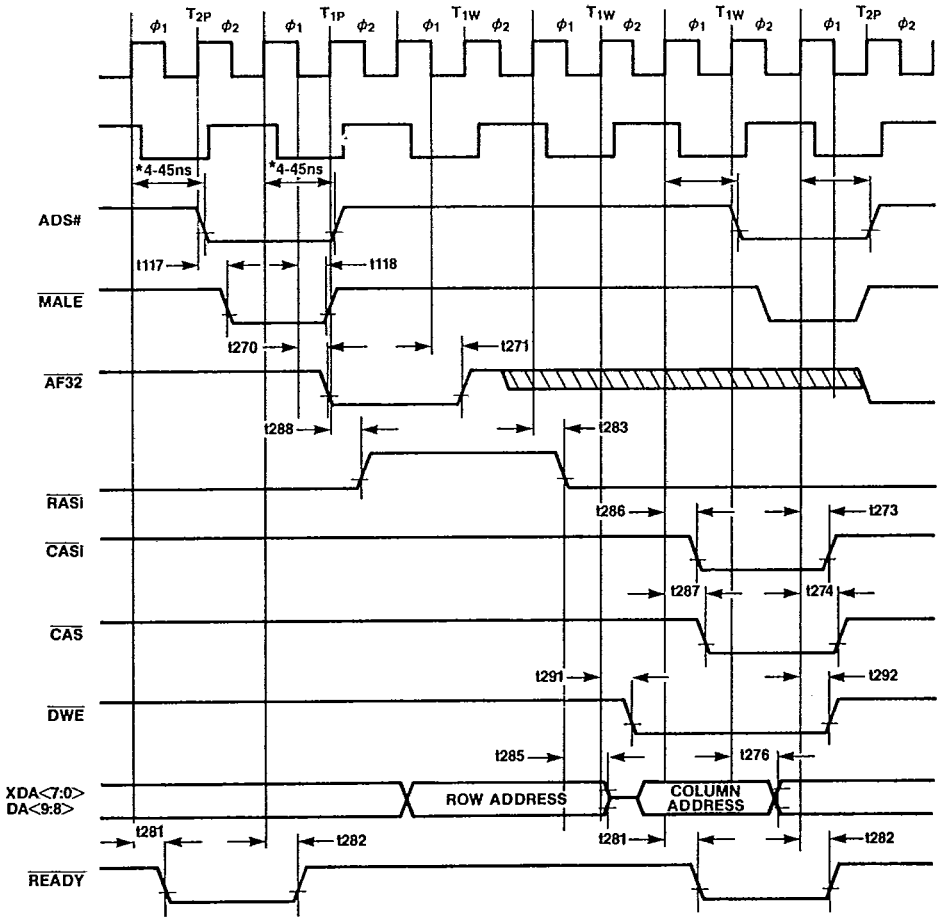


*INTEL 80386 DATA SHEET, A.C. TIMING SPECIFICATIONS.

82C302 TIMING DIAGRAM (CPU TO LOCAL MEMORY) READ CYCLE WITH RAS BEING INACTIVE

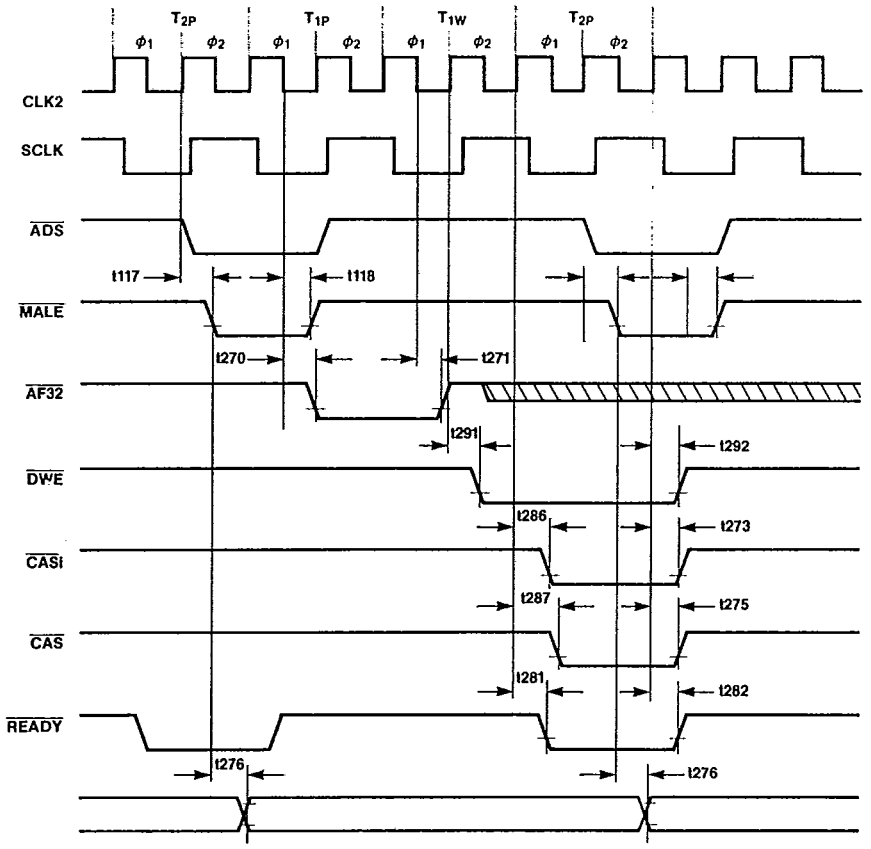


82C302 Write Miss Cycle with RAS Low

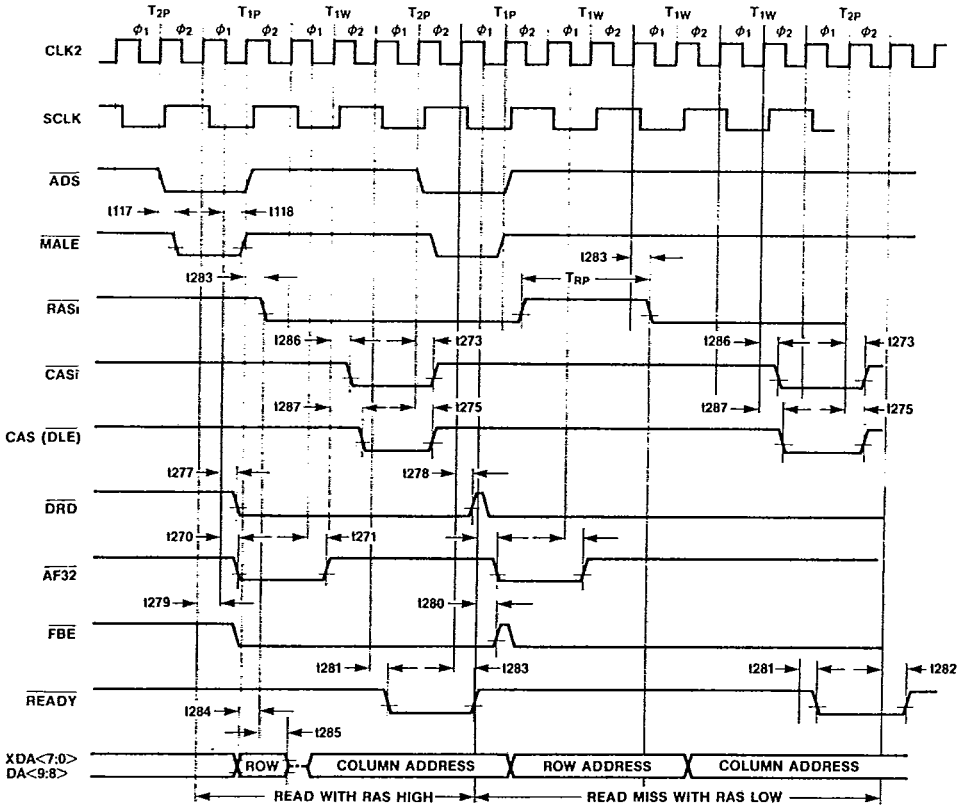


*INTEL 80386 DATA SHEET, A.C. TIMING PARAMETERS.

82C302 DRAM Write Hit Cycles



Read Cycle with RAS Being High



82A303/82C303
High Address Buffers

- Buffer for bits 31:12 of the Local, X and System address buses.
- X and S address bus can be extended to 27 bits (128MB).
- Direct interface to AT Bus
- Advanced Schottky TTL technology

Functional Description

The 82A303 as shown in figure 3-1 provides two functions:

- Generation of address decoding signals required by other chips.
- Interface between the local, X and System address bus.

Address Decode

The address decoding circuit provides as outputs LIOCS, LMEGCS, L64MEG, and HIROM. These signals are active if the address accesses satisfy the conditions defined in table 3-1. The signal decodes for LIOCS and LMEGCS are controlled by HLDA1 and latched on the trailing edge of MALE. The L64MEG and HIROM are simply decoded from the address signals.

Signal	Decode Condition
LIOCS	A<15:12> = 00H
LMEGCS	A<31:20> = 00H
L64MEG	A<31:26> = 00H
HIROM	A<31:26> = 3FH

Table 3-1. High Address Decodes Definition

Address Bus Interfaces

The 82A303 interconnects the local, X and system address buses with bidirectional drivers connecting each bus and the internal buses. These drivers have 24mA current drives for direct connection to the system address bus. The table 3-2 shows how the drivers are configured between the buses for each type of active bus requests. Note that the default configuration is set up so that the CPU address bus drives the memory address bus for local memory CPU access cycles.

For all CPU sourced accesses, the addresses are latched on the trailing edge of MALE.

27 Bit Address Extensions

The standard AT implementation supports only 24-bit addresses. The CS 8230 allows for address extension on the SA and XA buses to 27 bits (128MB). This is done by grounding the enable pin XBHE for XA bus and SBHE for SA bus. Internal pullups are provided so that if the enable pins are left unconnected bits 24 to 27 of the respective bus are forced low.

HLDA	ATEN	REF	MASTER	Cycle Type	A Bus Source	A Bus Output	S Bus Source	S Bus Output	X Bus Source	X Bus Output
0	1	1	1	CPU, non-AT	—	Disable	—	Disable	—	Disable
0	0	1	1	CPU AT bus cycle	—	Disable	A Bus	Enable	A Bus	Enable
0	1	0	1	CPU Refresh	—	Disable	X Bus	Enable	—	Disable
1	1	1	0	Master	S Bus	Enable	—	Disable	S Bus	Enable
1	1	0	0	Master Refresh	—	Disable	—	Enable	—	Disable
1	1	1	1	DMA	X Bus	Enable	X Bus	Enable	—	Disable

Table 3-2. High Address Bus Control

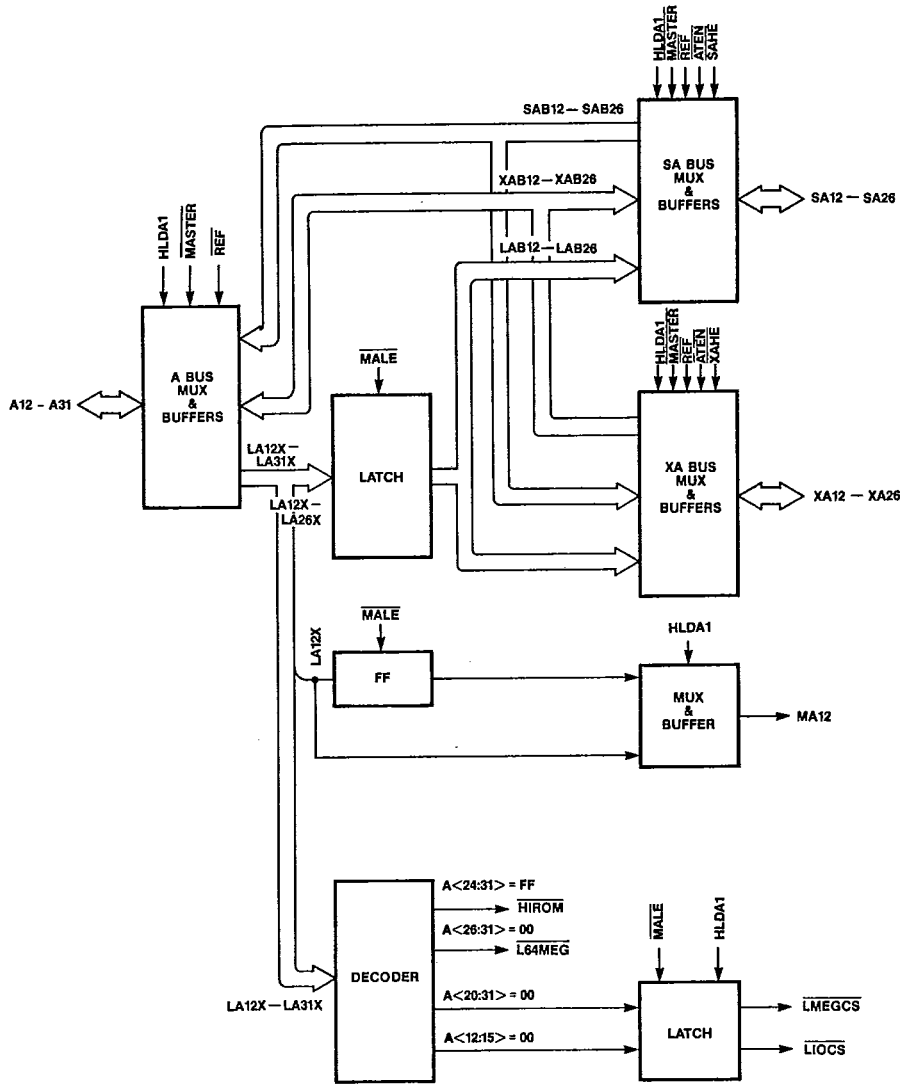
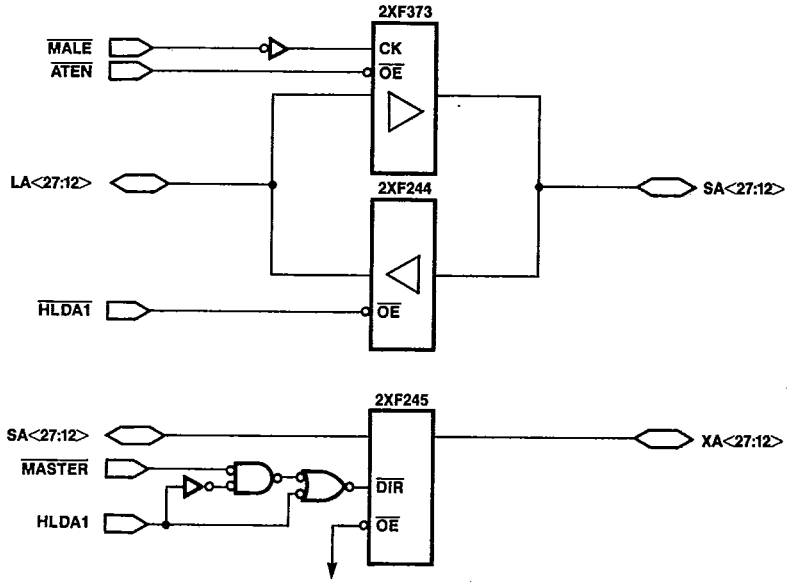
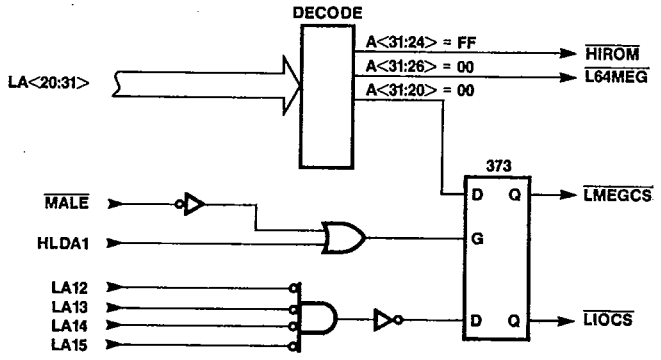


Figure 3-1. 82A303 Functional Block Diagram



82A303 SA to XA TTL Equivalent Address Buffer Architecture



82A303 TTL Equivalent Address Decode Logic

82A303 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	—	7.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{op}	-25	85	C
Storage Temperature	T_{stg}	-40	125	C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82A303 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	C

82A303 DC Characterisitcs

Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.0		V
Output Low Voltage I_{OL}=10mA (Note 1)	V_{OL1}		0.5	V
Output Low Voltage I_{OL}=24mA (Note 2)	V_{OL2}		0.5	V
Output High Voltage I_{OH}-3.3mA (Note 3)	V_{OH}	2.4		V
Input Low Current V_I = 0.5V, V_{CC} = 5.25V	I_{IL}		-200	μA
Input High Current V_I = 2.4V, V_{CC} = 5.25V	I_{IH}		20	μA
Input High Current V_I = 5.5V, V_{CC} = 5.25V	I_I		200	μA
Output Short Circuit Current V_O=0V	I_{OS}	-15	-100	mA
Input Clamp Voltage I_I = -18mA, V_{CC} = 4.75V	V_{IC}		-1.5	V
Power Supply Current	I_{CC}		200	mA
Output HI-Z Leak Current 3-State Output Pins	I_{OZ1}	-100	100	μA
Output HI-Z Leak Current Bidirectional Pins	I_{OZ2}	-300	120	μA

NOTES
1. All bus outputs other than SA<20:12> and XA<26:21>.
2. All SA<20:12> and XA<26:21> have I_{OL} = 24mA.
3. All outputs and bidirectional pins.

82C303 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	-0.5	6.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{op}	-25	85	C
Storage Temperature	T_{stg}	-40	125	C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82C303 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	C

82C303 DC Characteristics

Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.0		V
Output Low Voltage I_{OL}=3.2mA (Note 1)	V_{OL1}	V_{SS}	0.4	V
Output Low Voltage I_{OL}=12mA (Note 2)	V_{OL2}	V_{SS}	0.4	V
Output High Voltage I_{OH}=-0.2mA	V_{OH1}	4.2	V_{CC}	V
Output High Voltage I_{OH}=-0.4mA	V_{OH2}	4.2	V_{CC}	V
Input Low Current V_I = 0.5V, V_{CC} = 5.25V	I_{IL}		-200	μA
Input High Current V_I = 2.4V, V_{CC} = 5.25V	I_{IH}		20	μA
Input High Current V_I = 5.5V, V_{CC} = 5.25V	I_I		200	μA
Output Short Circuit Current V_O=0V	I_{OS}	-15	-100	mA
Input Clamp Voltage I_I = -18mA, V_{CC} = 4.75V	V_{IC}		-1.5	V
Power Supply Current	I_{CC}		100	mA
Output HI-Z Leak Current 3-State Output Pins	I_{OZ1}	-100	100	μA
Output HI-Z Leak Current Bidirectional Pins	I_{OZ2}	-300	120	μA

NOTES
1. All bus outputs other than SA<20:12> and XA<26:21>.
2. All SA<20:12> and XA<26:21> have I_{OL} = 12mA.
3. All outputs and bidirectional pins.

82A303 AC Characteristics

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Sym	Description	82A303 82C303 Min	Typ	Max	Unit	Notes
t301	A to MA input set-up time to $\overline{MALE}$↓	5			ns	
t302	A to MA input hold time from $\overline{MALE}$↓	10			ns	
t303	MA output valid delay from $\overline{MALE}$↓	5		27	ns	
t304	A to SA, XA input set-up time to $\overline{MALE}$↓	5			ns	
t305	A to SA,XA input hold time from $\overline{MALE}$↓	5			ns	
t306	SA output valid delay from $\overline{ATEN}$ active	8		28	ns	
t307	SA tri-state delay from $\overline{ATEN}$ inactive	6		25	ns	
t308	XA output valid delay from $\overline{ATEN}$ active	11		35	ns	
t309	XA tri-state delay from $\overline{ATEN}$ inactive	9		35	ns	
t310	$\overline{HIROM}$ decode active from A<32:26> valid	4		15	ns	
t311	$\overline{HIROM}$ decode inactive from A<32:26> invalid	2		16	ns	
t312	$\overline{L64MEG}$ decode active from A<32:26> valid	4		19	ns	
t313	$\overline{L64MEG}$ decode inactive from A<32:26> invalid	2		15	ns	
t314	$\overline{LIOCS}$ decode active from $\overline{MALE}$ active	6		26	ns	
t315	$\overline{LIOCS}$ decode inactive from $\overline{MALE}$ active	4		23	ns	
t316	$\overline{LMEGCS}$ decode active from $\overline{MALE}$ active	6		26	ns	
t317	$\overline{LMEGCS}$ decode inactive from $\overline{MALE}$ active	4		23	ns	
t318	A data valid delay from SA data valid	4		23	ns	
t319	XA data valid delay from SA data valid	7		30	ns	
t320	MA data valid delay from SA data valid	9		40	ns	
t321	$\overline{LIOCS}$ decode active from SA data valid	13		50	ns	
t322	$\overline{LIOCS}$ decode inactive from SA data invalid	10		39	ns	
t323	$\overline{L64MEG}$ decode active from SA data valid	12		47	ns	
t324	$\overline{L64MEG}$ decode inactive from SA data invalid	9		35	ns	
t325	$\overline{LMEGCS}$ decode active from SA data valid	14		53	ns	
t326	$\overline{LMEGCS}$ decode active from SA data invalid	10		40	ns	
t327	A data valid delay from XA data valid	4		27	ns	
t328	SA data valid delay from XA data valid	6		30	ns	

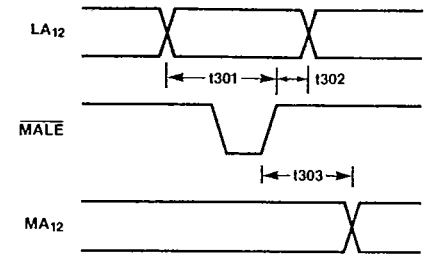
Test Load = 65pF unless otherwise specified.

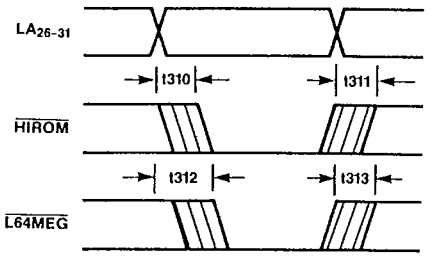
82A303 AC Characteristics (Continued)
(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

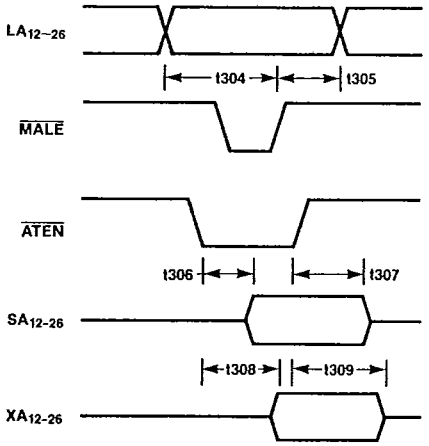
Sym	Description	82A303 82C303 Min	Typ	Max	Unit	Notes
t329	MA data valid delay from XA data valid	9		40	ns	
t330	$\overline{\text{LIOCS}}$ decode active from XA data valid	13		50	ns	
t331	$\overline{\text{LIOCS}}$ decode inactive from XA data valid	9		38	ns	
t332	$\overline{\text{L64MEG}}$ decode active from XA data valid	12		47	ns	
t333	$\overline{\text{L64MEG}}$ decode inactive from XA data valid	9		35	ns	
t334	$\overline{\text{LMEGCS}}$ decode active from XA data valid	14		53	ns	
t335	$\overline{\text{LMEGCS}}$ decode inactive from XA data valid	10		40	ns	
t336	SA valid delay from $\overline{\text{REF}}$ active	18		64	ns	
t337	SA tri-state delay from $\overline{\text{REF}}$ inactive	8		33	ns	

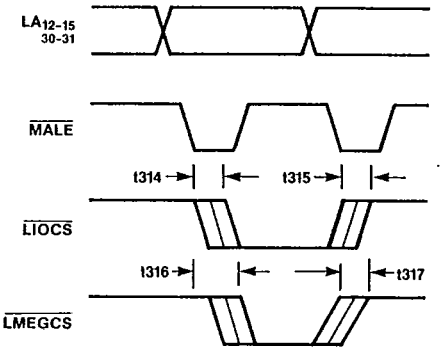
Test Load = 65pF unless otherwise specified.

82A303 TIMING DIAGRAMS

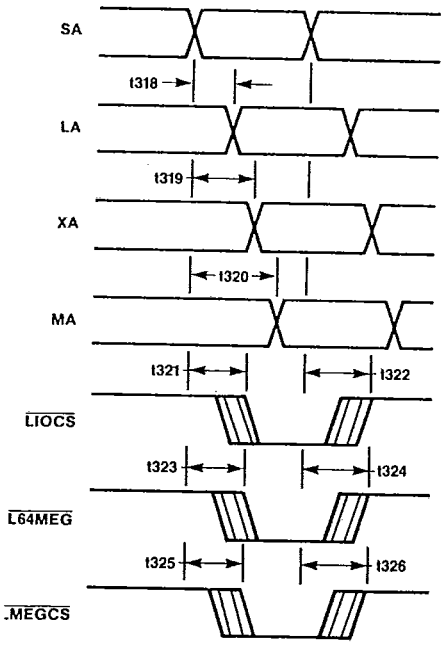


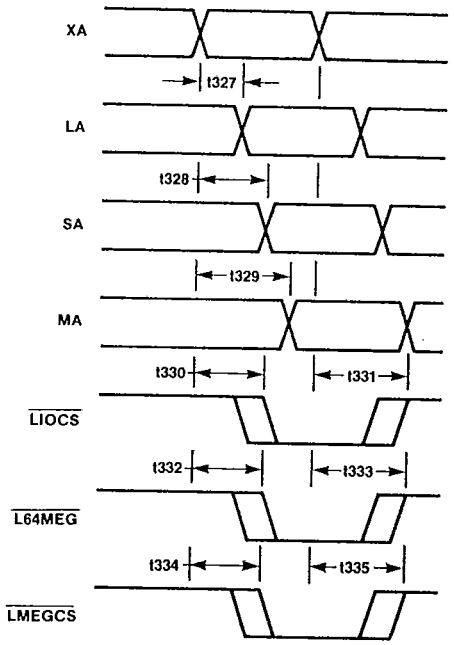


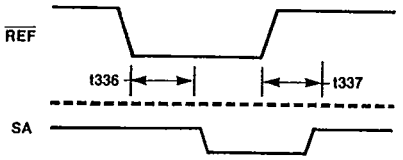




82A303 TIMING DIAGRAMS







82A304/82C304
Low Address Buffers

- Buffer for bits 11:00 of the Local, X and System address buses.
- Peripheral device decode
- Direct interface to AT Bus
- Refresh Address Generation
- Advanced Schottky TTL technology

Functional Description

Address Decode

The signals IO2XCS, 8042CS, PORTBCS, NMICS, 287CS, and AS provides the lower address decodes for the corresponding devices after being qualified by the LIOCS generated by the high address buffer decoder. The resulting decode is as defined by the IBM PC AT IO addresses and is as shown in table 4-1. For applications where these devices are required to be relocated, the EXDEC can be tied LOW to ignore the LIOCS qualification and the MA<11:10> address bits.

Signal	Addresses Decoded
IO2XCS	022H, 023H
8042CS	060H, 064H
PORTBCS	061H
NMICS	070H
287CS	0E0H to 0FFH

Table 4-1. Low Address Decode Definition

Address Bus Interfaces

The 82A304 interfaces between the bits 00 to 11 of A, SA, XA, and MA address buses. The buffers and multiplexers are controlled by the HLDA1, MASTER, REF, and ATEN to drive the signals from the source to the target buses as defined by table 4-2 for each signal when active. When REF is asserted, the refresh counter is gated to the SA bus as refresh row address and is incremented. When none of the listed signals are active, the default buffer configuration is that the A bus drives the MA bus for memory accesses by CPU.

The SA<11:00> are 24mA address buffers for direct interface to the AT bus.

HLDA1	ATEN	REF	MASTER	Cycle Type	A Bus Source	A Bus Output	S Bus Source	S Bus Output	X Bus Source	X Bus Output
0	1	1	1	CPU, non-AT	—	Disable	—	Disable	—	Disable
0	0	1	1	CPU AT	—	Disable	A Bus	Enable	A Bus	Enable
0	1	0	1	CPU Refresh	—	Disable	REFCTR	Enable	—	Disable
1	1	1	0	Master	S Bus	Enable	—	Disable	S Bus	Enable
1	1	0	0	Master Refresh	X Bus	Enable	X Bus	Enable	—	Disable

Table 4-2. Bus Control Definition

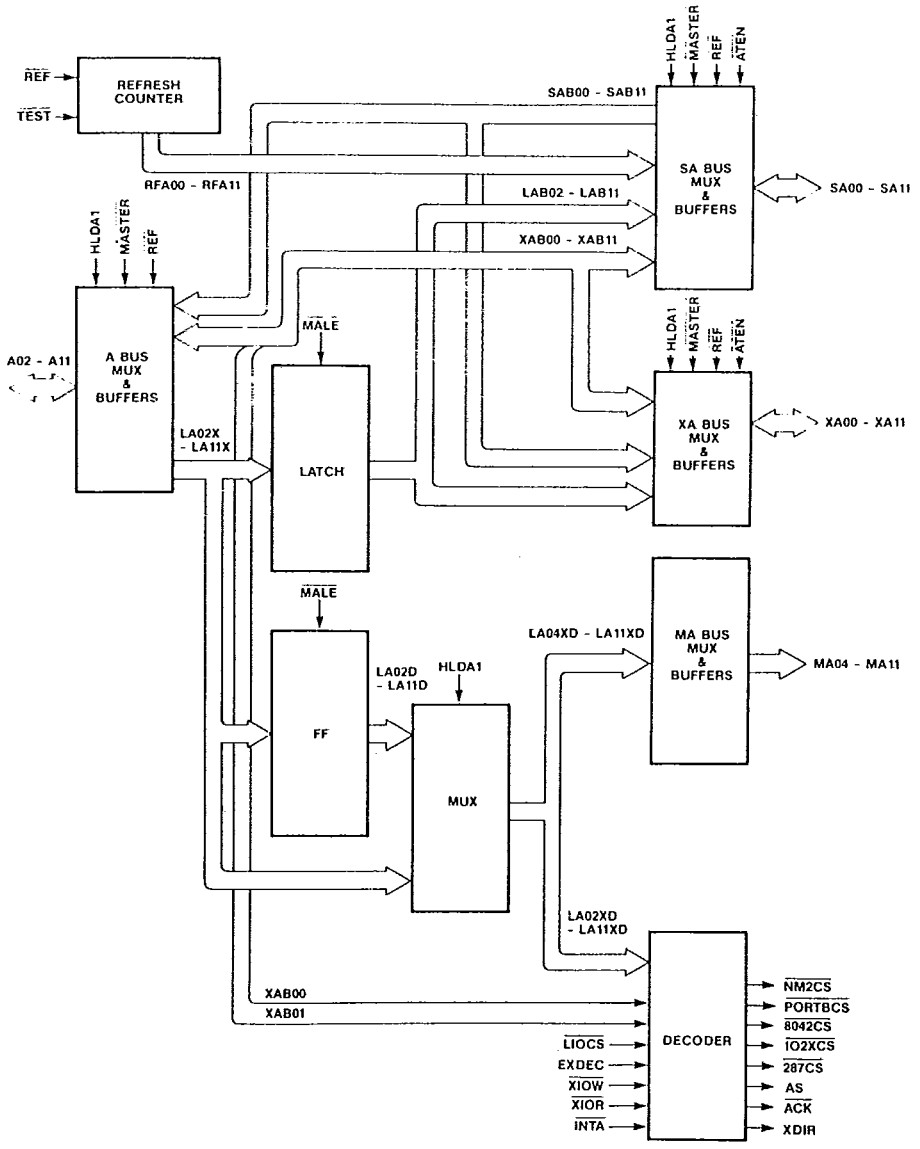
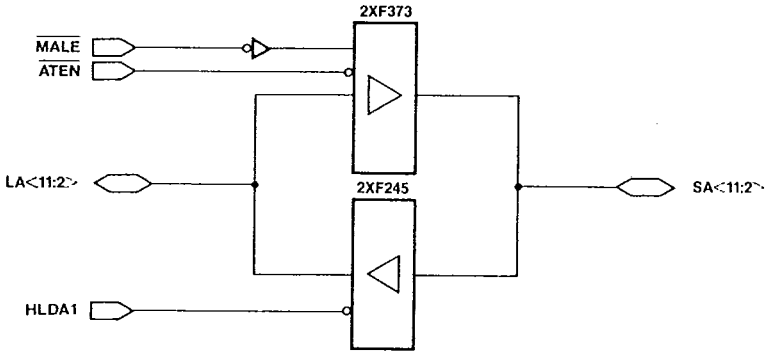
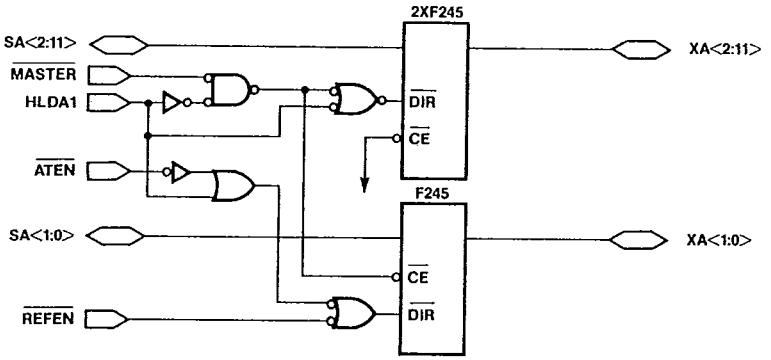


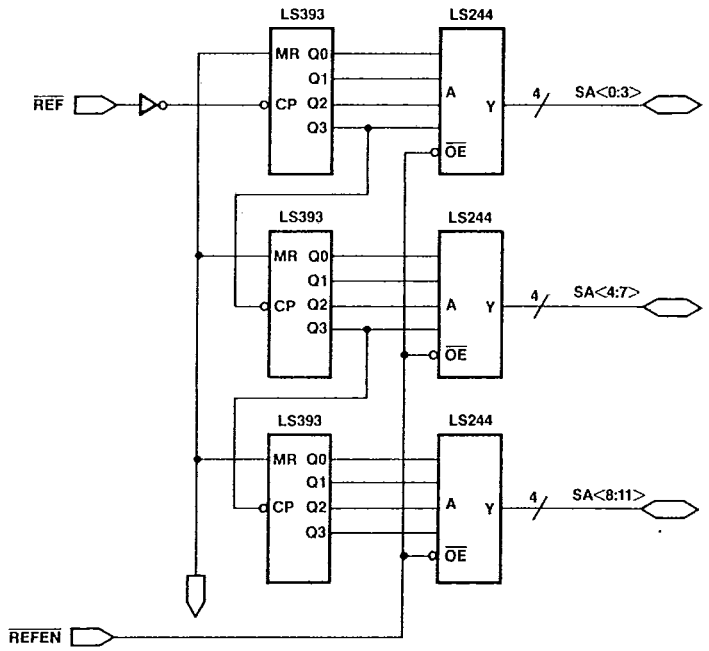
Figure 4-1. 82A304 Functional Block Diagram



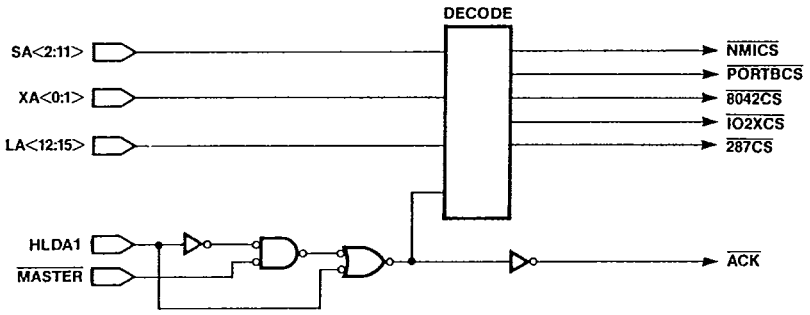
82A304 LA to SA TTL Equivalent Address Buffer Architecture



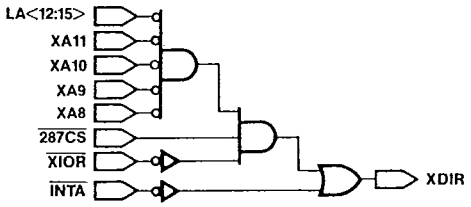
82A304 SA to XA TTL Equivalent Address Buffer Architecture



82A304 TTL Equivalent XDIR Generation Logic



82A304 AT Bus Refresh Address Generation Circuitry



82A304 TTL Equivalent Chip Select Generation Circuitry

82A304 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	—	7.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{op}	-25	85	C
Storage Temperature	T_{stg}	-40	125	C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82A304 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	C

82A304 DC Characteristics

Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.0		V
Output Low Voltage I_{OL}=10mA (Note 1)	V_{OL1}		0.5	V
Output Low Voltage I_{OL}=24mA (Note 2)	V_{OL2}		0.5	V
Output High Voltage I_{OH}-3.3mA (Note 3)	V_{OH}	2.4		V
Input Low Current V_I = 0.5V, V_{CC} = 5.25V	I_{IL}		-200	μA
Input High Current V_I = 2.4V, V_{CC} = 5.25V	I_{IH}		20	μA
Input High Current V_I = 5.5V, V_{CC} = 5.25V	I_I		200	μA
Output Short Circuit Current V_O=0V	I_{OS}	-15	-100	mA
Input Clamp Voltage I_I = -18mA, V_{CC} = 4.75V	V_{IC}		-1.5	V
Power Supply Current	I_{CC}	140	230	mA
Output HI-Z Leak Current 3-State Output Pins	I_{OZ1}	-100	100	μA
Output HI-Z Leak Current Bidirectional Pins	I_{OZ2}	-300	120	μA

NOTES
1. All bus outputs other than SA<20:12>.
2. All SA<20:12> have I_{OL} = 24mA.
3. All outputs and bidirectional pins.

82C304 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	-0.5	6.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{op}	-25	85	C
Storage Temperature	T_{stg}	-40	125	C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82C304 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	C

82C304 DC Characteristics

Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.0		V
Output Low Voltage I_{OL}=3.2mA (Note 1)	V_{OL1}	V_{SS}	0.4	V
Output Low Voltage I_{OL}=12mA (Note 2)	V_{OL2}	V_{SS}	0.4	V
Output High Voltage I_{OH}=-0.2mA (Note 3)	V_{OH1}	4.2	V_{CC}	V
Output High Voltage I_{OH}=-0.4mA	V_{OH2}	4.2	V_{CC}	V
Input Low Current V_I = 0.5V, V_{CC} = 5.25V	I_{IL}		-200	μA
Input High Current V_I = 2.4V, V_{CC} = 5.25V	I_{IH}		20	μA
Input High Current V_I = 5.5V, V_{CC} = 5.25V	I_I		200	μA
Output Short Circuit Current V_O=0V	I_{OS}	-15	-100	mA
Input Clamp Voltage I_I = -18mA, V_{CC} = 4.75V	V_{IC}		-1.5	V
Power Supply Current	I_{CC}		1000	μA
Output HI-Z Leak Current 3-State Output Pins	I_{OZ1}	-100	100	μA
Output HI-Z Leak Current Bidirectional Pins	I_{OZ2}	-300	120	μA

NOTES
1. All bus outputs other than SA<11:00>.
2. All SA<11:00> have I_{OL} = 12mA.
3. All outputs and bidirectional pins.

82A304 AC Characteristics

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Sym	Description	82C304 82A304 Min	Typ	Max	Unit	Notes
t401	A to MA input set-up time to $\overline{MALE}$↑	5			ns	
t402	A to MA input hold time from $\overline{MALE}$↑	5			ns	
t403	MA output valid delay from $\overline{MALE}$↑	5		30	ns	
t404	A to SA, XA input set-up time to $\overline{MALE}$↑	5			ns	
t405	A to SA, XA input hold time from $\overline{MALE}$↑	5			ns	
t406	SA output valid delay from $\overline{ATEN}$ active	8		30	ns	
t407	SA tri-state delay from $\overline{ATEN}$ inactive	6		24	ns	
t408	XA output valid delay from $\overline{ATEN}$ active	10		37	ns	
t409	XA tri-state delay from $\overline{ATEN}$ inactive	9		33	ns	
t410	$\overline{NMICS}$ decode active from $\overline{MALE}$↑	11		44	ns	
t411	$\overline{NMICS}$ decode inactive from $\overline{MALE}$↑	10		40	ns	
t412	$\overline{PORTBCS}$ decode active from $\overline{MALE}$↑	11		44	ns	
t413	$\overline{PORTBCS}$ decode inactive from $\overline{MALE}$↑	10		40	ns	
t414	$\overline{8042CS}$ decode active from $\overline{MALE}$↑	11		44	ns	
t415	$\overline{8042CS}$ decode inactive from $\overline{MALE}$↑	10		40	ns	
t416	$\overline{IO2XCS}$ decode active from $\overline{MALE}$↑	11		44	ns	
t417	$\overline{IO2XCS}$ decode inactive from $\overline{MALE}$↑	10		40	ns	
t418	$\overline{287CS}$ decode active from $\overline{MALE}$↑	11		44	ns	
t419	$\overline{287CS}$ decode inactive from $\overline{MALE}$↑	10		40	ns	
t420	A data valid delay from SA data valid	4		26	ns	
t421	XA data valid delay from SA data valid	3		27	ns	
t422	MA data valid delay from SA data valid	9		37	ns	
t423	$\overline{NMICS}$ decode active from SA data valid	14		58	ns	
t424	$\overline{NMICS}$ decode inactive delay from SA data invalid	11		46	ns	
t425	$\overline{PORTBCS}$ decode active from SA data valid	15		59	ns	
t426	$\overline{PORTBCS}$ decode inactive from SA data	11		46	ns	
t427	$\overline{8042CS}$ decode active from SA data valid	15		59	ns	
t428	$\overline{8042CS}$ decode inactive from SA data invalid	11		46	ns	
t429	$\overline{IO2XCS}$ decode active from SA data valid	12		59	ns	

Test Load = 65pF unless otherwise specified.

82A304 AC Characteristics (Continued)
(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Sym	Description	82C304 82A304 Min	Typ	Max	Unit	Notes
t430	$\overline{IO2XCS}$ decode inactive from SA data invalid	12		46	ns	
t431	$\overline{287CS}$ decode active from SA data valid	16		59	ns	
t432	$\overline{287CS}$ decode inactive from SA data invalid	13		46	ns	
t433	$\overline{XDIR}$ decode active from SA data valid	15		59	ns	
t434	$\overline{XDIR}$ decode inactive from SA data invalid	15		60	ns	
t435	A data valid delay from XA data valid	4		23	ns	
t436	SA data valid delay from XA data valid	7		30	ns	
t437	MA data valid delay from XA data valid	9		43	ns	
t438	$\overline{NMICS}$ decode active from XA data valid	14		58	ns	
t439	$\overline{NMICS}$ decode inactive from XA data invalid	11		46	ns	
t440	$\overline{PORTBCS}$ decode active from XA data valid	15		59	ns	
t441	$\overline{PORTBCS}$ decode inactive from XA data invalid	11		46	ns	
t442	$\overline{8042CS}$ decode active delay from XA data valid	15		50	ns	
t443	$\overline{8042CS}$ decode inactive delay from XA data invalid	11		46	ns	
t444	$\overline{IO2XCS}$ decode active from XA data valid	12		59	ns	
t445	$\overline{IO2XCS}$ decode inactive from XA data invalid	12		46	ns	
t446	$\overline{287CS}$ decode active from XA data valid	16		59	ns	
t447	$\overline{287CS}$ decode inactive from XA data invalid	13		46	ns	
t448	$\overline{XDIR}$ decode active from XA data valid	15		55	ns	
t449	$\overline{XDIR}$ decode inactive from XA data invalid	15		55	ns	
t450	$\overline{NMICS}$ decode active from $\overline{LIOCS}$ active	7		31	ns	
t451	$\overline{NMICS}$ decode inactive from $\overline{LIOCS}$ inactive	5		24	ns	
t452	$\overline{PORTBCS}$ decode active from $\overline{LIOCS}$ active	7		31	ns	
t453	$\overline{PORTBCS}$ decode inactive from $\overline{LIOCS}$ inactive	5		24	ns	
t454	$\overline{8042CS}$ decode active from $\overline{LIOCS}$ active	7		30	ns	
t455	$\overline{8042CS}$ decode inactive from $\overline{LIOCS}$ inactive	5		24	ns	
t456	$\overline{IO2XCS}$ decode active from $\overline{LIOCS}$ active	7		30	ns	

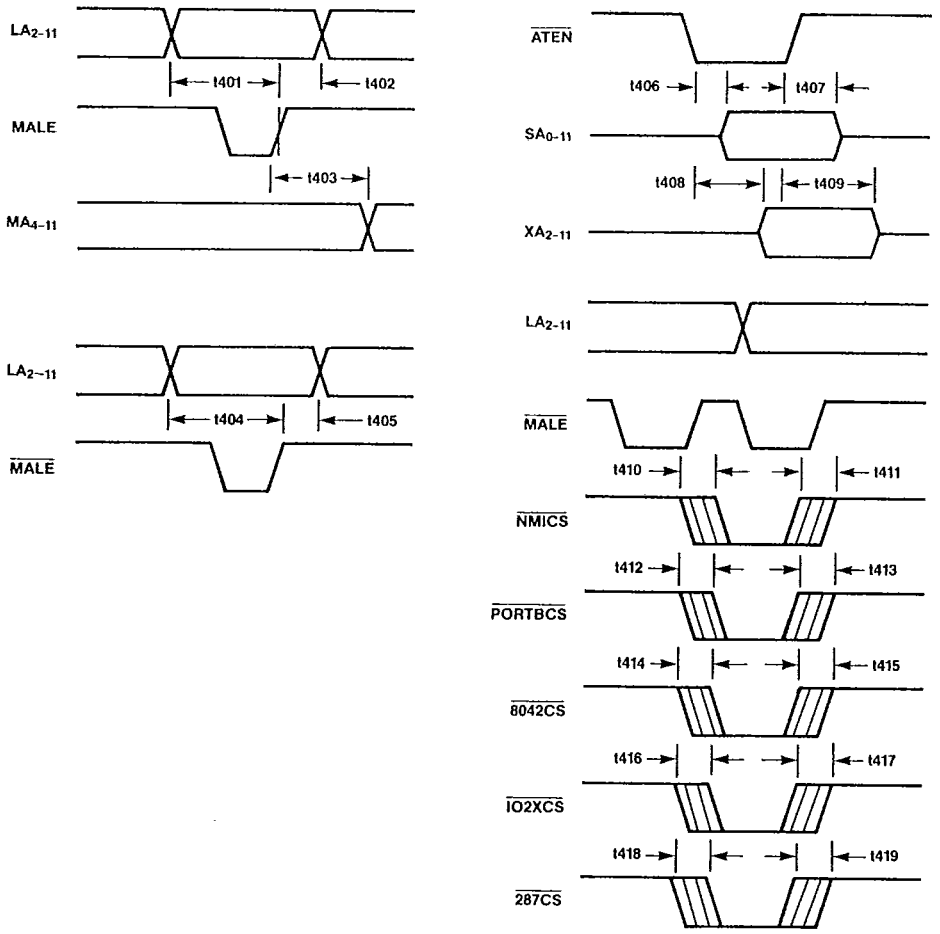
Test Load = 65pF unless otherwise specified.

82A304 AC Characteristics (Continued)
(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

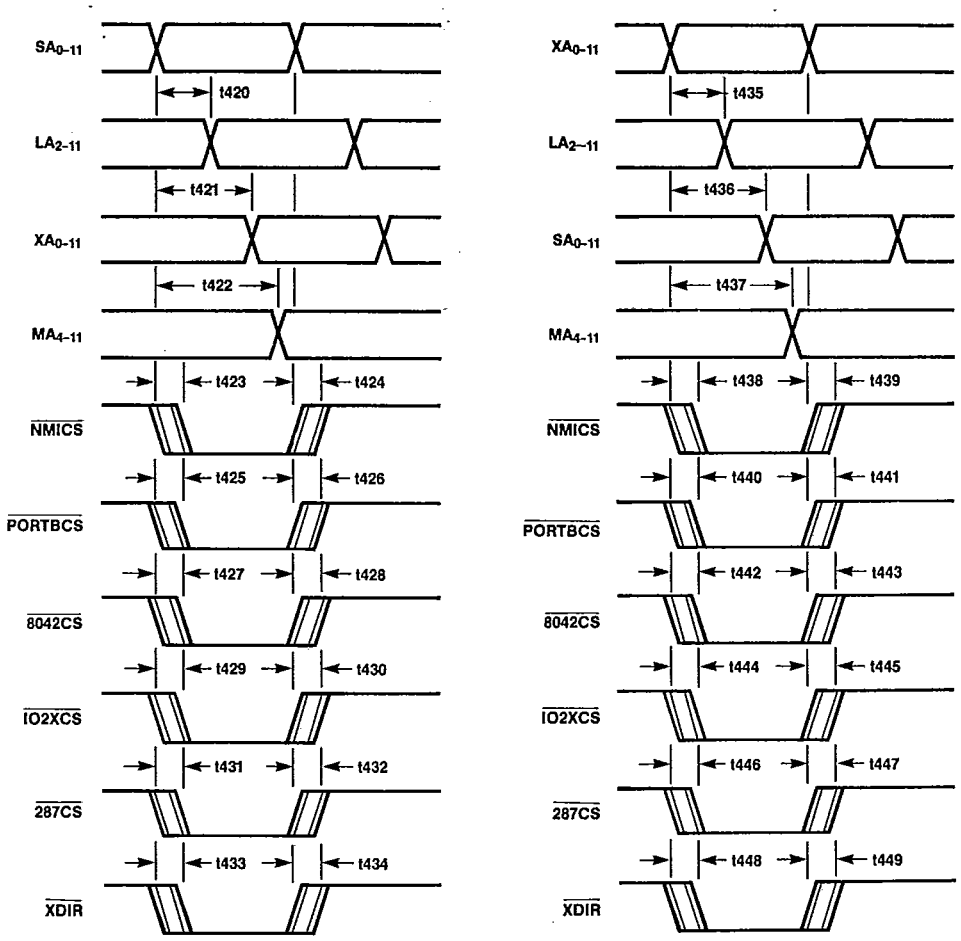
Sym	Description	82C304 82A304 Min	Typ	Max	Unit	Notes
t457	$\overline{IO2XCS}$ decode inactive from $\overline{LIOCS}$ inactive	5		24	ns	
t458	$\overline{287CS}$ decode active from $\overline{LIOCS}$ active	7		30	ns	
t459	$\overline{287CS}$ decode inactive from $\overline{LIOCS}$ inactive	5		24	ns	
t460	$\overline{XDIR}$ decode active from $\overline{LIOCS}$ active	8		32	ns	
t461	$\overline{XDIR}$ decode inactive from $\overline{LIOCS}$ inactive	5		26	ns	
t462	$\overline{XDIR}$ decode active from $\overline{INTA}$ active	4		23	ns	
t463	$\overline{XDIR}$ decode inactive from $\overline{INTA}$ inactive	2		17	ns	
t464	$\overline{XDIR}$ decode active from $\overline{XIOR}$ active	6		27	ns	
t465	$\overline{XDIR}$ decode inactive from $\overline{XIOR}$ inactive	4		20	ns	
t466	$\overline{ACK}$ decode active from HLDA1 active	9		37	ns	
t467	$\overline{ACK}$ decode inactive from HLDA1 inactive	7		32	ns	
t468	$\overline{ACK}$ decode active from $\overline{MASTER}$ active	8		33	ns	
t469	$\overline{ACK}$ decode inactive from $\overline{MASTER}$ inactive	6		26	ns	
t470	SA data valid delay from $\overline{REF}$ active	18		64	ns	
t471	SA tri-state delay from $\overline{REF}$	8		33	ns	

Test Load = 65pF unless otherwise specified.

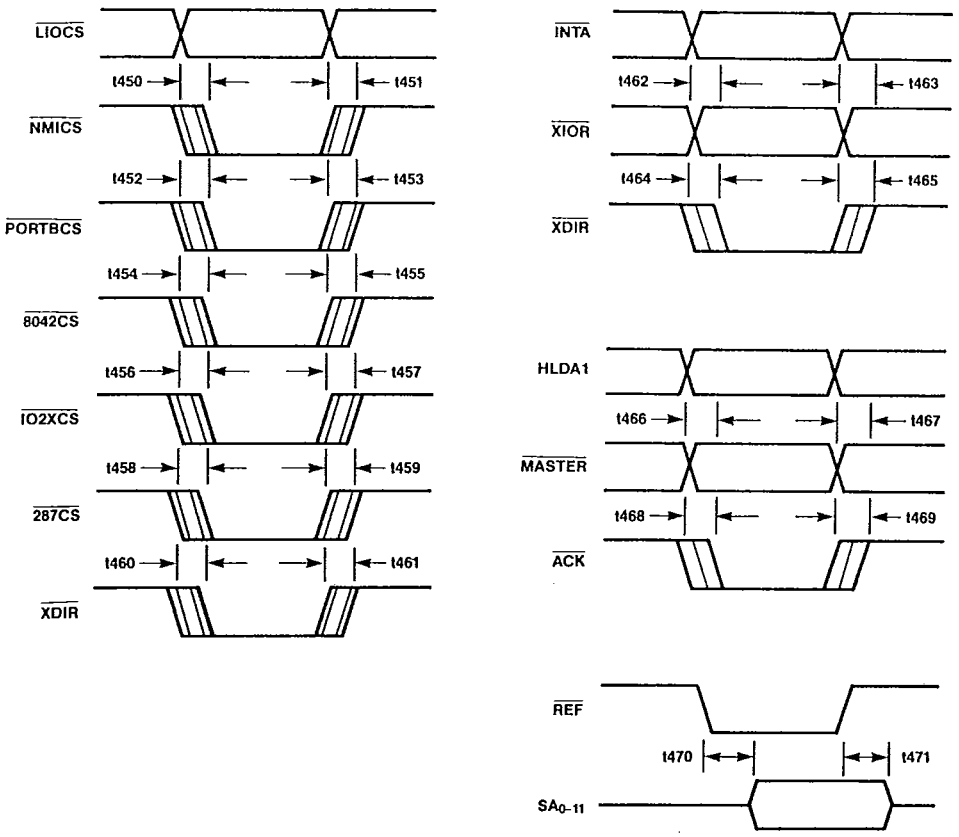
82A304 TIMING DIAGRAMS



82A304 TIMING DIAGRAMS



82A304 TIMING DIAGRAMS



82A305/82B305/82C305 Data Buffer

- Nibble Slice of Memory and AT Data Bus Interface
- Data Size Conversion
- Advanced Schottky technology

Functional Description

The 82A305 interfaces between the Local, Memory and System (AT IO channel) data busses and provides data alignment and size conversion for AT IO channel operations. It is designed as a nibble slice to reduce pin count and simplify system design. Two parts are used to interface all data buses.

Bus Controls

The 82A305 controls the bus buffers according to the signals HLDA1, $\overline{ATEN}$, $\overline{CS}$, $\overline{LDEN}$, SDIR, $\overline{MRD}$, and AC<3:0>. The first group of signals HLDA1, $\overline{ATEN}$, $\overline{CS}$, and $\overline{LDEN}$ determines which buses are connected, and the second group of signals SDIR, $\overline{MRD}$, and AC<3:0> determines the direction of the buffers drivers. Table 5-1 shows the bus connections for different bus cycles.

All drivers are active for the active buses, and external bus controls are required if selective data bits need to be controlled. For the DRAM interface, the $\overline{LBE}$<3:0> must be used to ensure that only the valid data bytes are written into the DRAM's during a write cycle.

Data Conversion

The 82A305 provides the data bus connections so that data conversions are done correctly for CPU accesses to the AT bus. The action codes AC<3:0> are used to control how bus bits are connected between the IO channel SD bus and the CPU local bus D or the system memory MD bus. The action codes are provided by the 82C301 bus controller for CPU to AT bus access cycles and is qualified by the ACEN. The meaning of the action codes are:

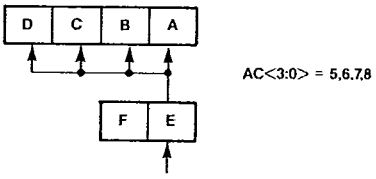
AC<3:0>	FROM	TO
0	AB	EF
1	B	EF
2	CD	EF
3	D	EF
4	ABCD	EFGH
5	E	A
6	E	B
7	E	C
8	E	D
9	EF	AB
A	EF	CD
B	—	—
C	EFGH	ABCD
D	—	—
E	—	—
F	—	—

Table 5-2. Action Code Definition

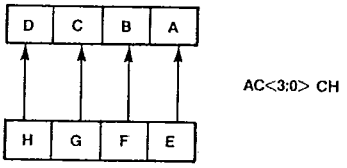
HLDA	ATEN	SDIR	$\overline{MDEN}$	$\overline{MRD}$	$\overline{LDEN}$	Cycle Type	D Bus Source	D Bus Output	S Bus Source	S Bus Output	M Bus Source	M Bus Output
0	1	X	0	0	X	CPU, non-AT Read	M Bus	Enable	—	Disable	—	Disable
0	1	X	0	1	X	CPU non-AT Write	—	Disable	—	Disable	D Bus	Enable
0	0	0	X	X	X	CPU AT Read	S Bus	Enable	—	Disable	—	Disable
0	0	1	X	X	X	CPU AT Write	—	Disable	D Bus	Enable	—	Disable
1	1	1	X	0	X	MASTER/DMA MemRd	—	Disable	M Bus	Enable	—	Disable
1	1	1	X	1	0	MASTER/DMA locRd	—	Disable	D Bus	Enable	—	Disable
1	1	0	X	1	X	MASTER/DMA locWR	S Bus	Enable	—	Disable	S Bus	Enable

Table 5-1. Bus Control Definitions

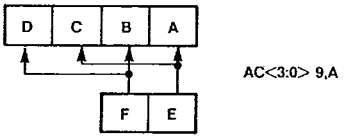
CPU Read from 8-Bit Devices



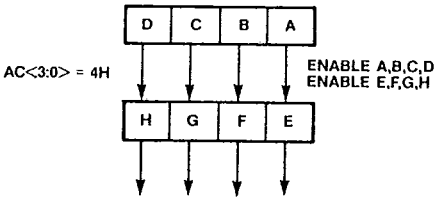
CPU Read from 32-Bit Device



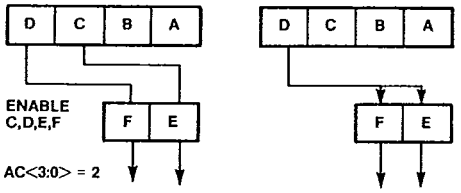
CPU Read from 16-Bit Devices

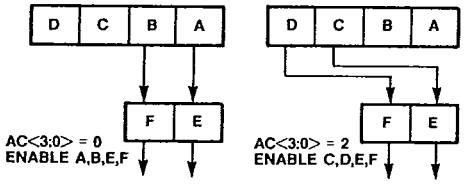


Write to 32-Bit Device

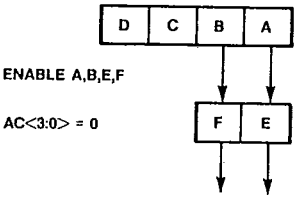


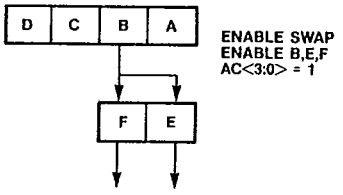
Write to 8-Bit Device





Write to 16-Bit Device





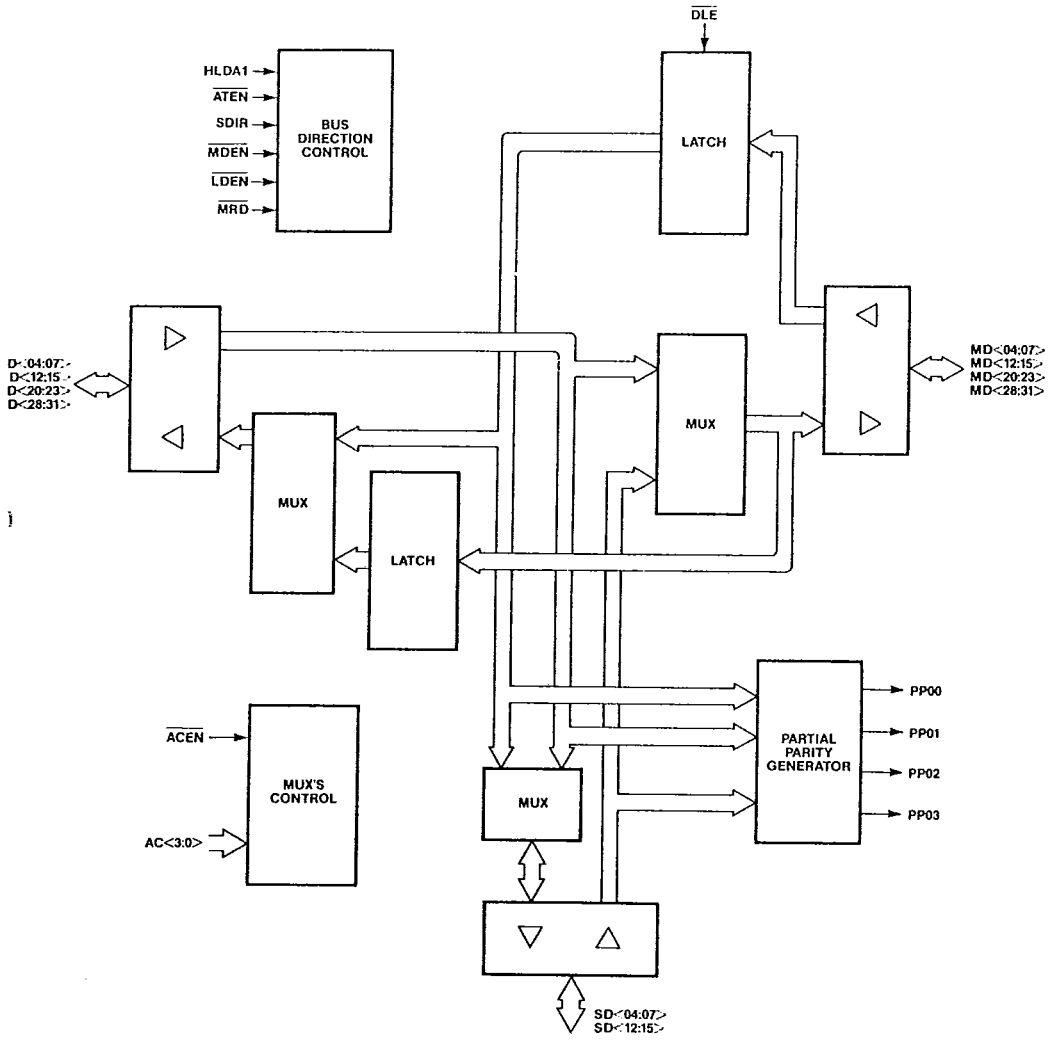
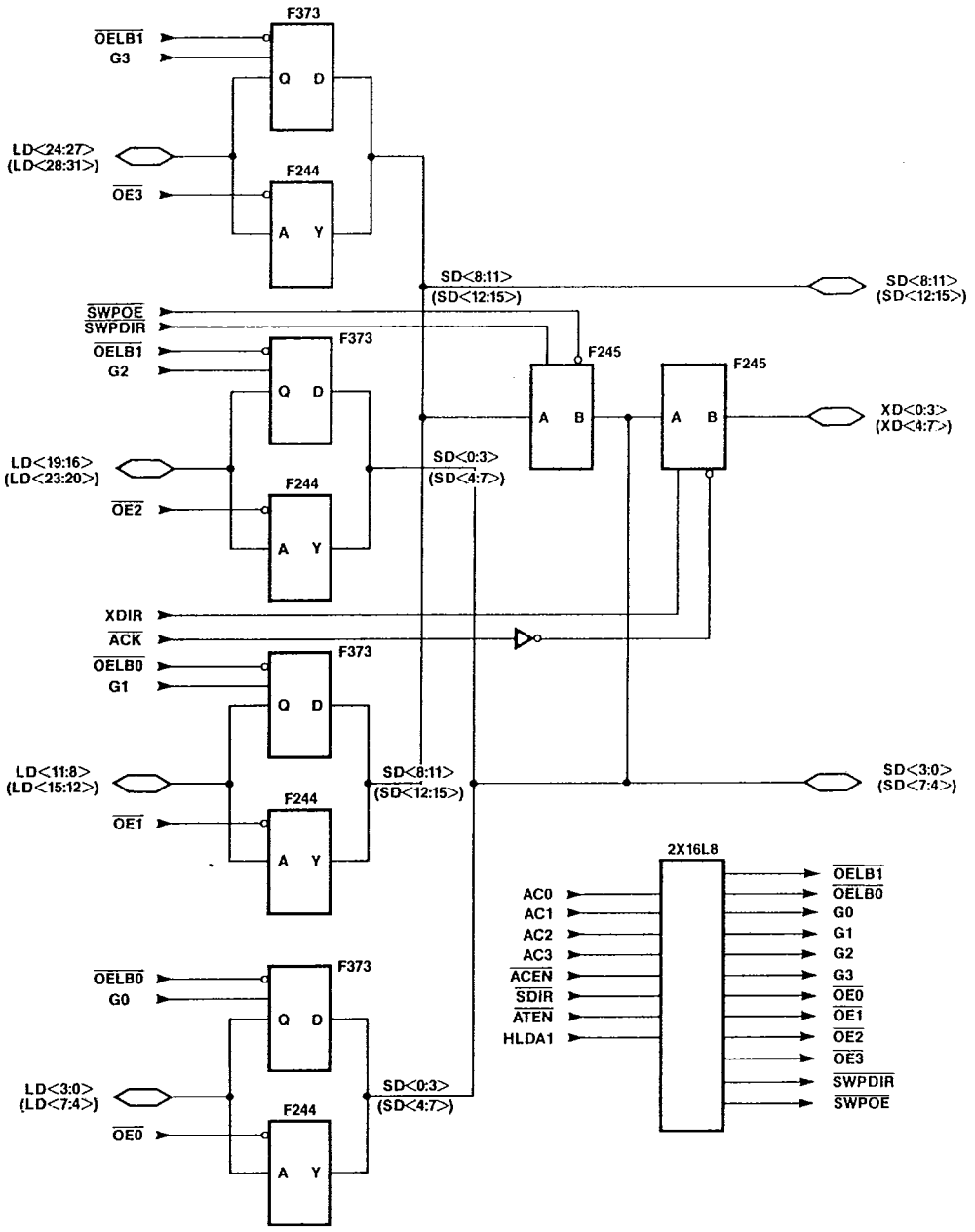
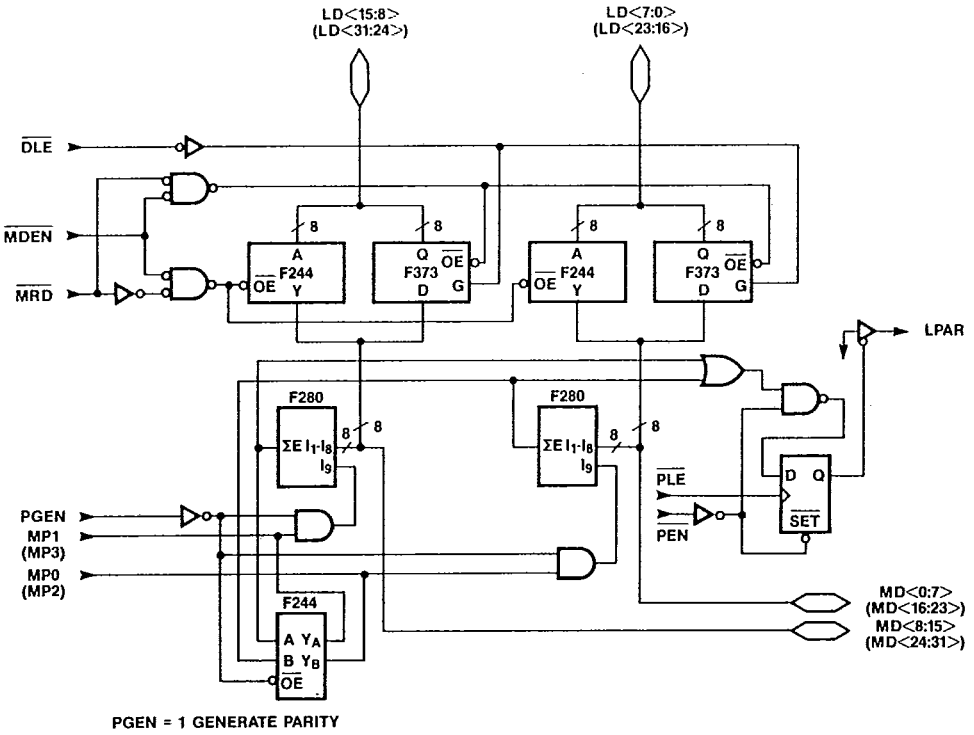


Figure 5-1. 82A305 Functional Block Diagram



82A305 TTL Equivalent Data Buffer Architecture



82A305 TTL Equivalent Data Buffer Architecture

82A305 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	—	7.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{op}	-25	85	C
Storage Temperature	T_{stg}	-40	125	C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82A305 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	C

82A305 DC Characteristics

Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.0		V
Output Low Voltage I_{OL}=10mA (Note 1)	V_{OL1}		0.5	V
Output Low Voltage I_{OL}=24mA (Note 2)	V_{OL2}		0.5	V
Output High Voltage I_{OH}-3.3mA (Note 3)	V_{OH}	2.4		V
Input Low Current V_I = 0.5V, V_{CC} = 5.25V	I_{IL}		-200	μA
Input High Current V_I = 2.4V, V_{CC} = 5.25V	I_{IH}		20	μA
Input High Current V_I = 5.5V, V_{CC} = 5.25V	I_I		200	μA
Output Short Circuit Current V_O=0V	I_{OS}	-15	-100	mA
Input Clamp Voltage I_I = -18mA, V_{CC} = 4.75V	V_{IC}		-1.5	V
Power Supply Current	I_{CC}	140	230	mA
Output HI-Z Leak Current 3-State Output Pins	I_{OZ1}	-100	100	μA
Output HI-Z Leak Current Bidirectional Pins	I_{OZ2}	-300	120	μA

NOTES
1. All bus outputs and PP<3:0> have I_{OL} = 10mA.
2. All outputs and bidirectional pins.

82C305 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	-0.5	6.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{op}	-25	85	C
Storage Temperature	T_{stg}	-40	125	C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82C305 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	C

82C305 DC Characteristics

Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.0		V
Output Low Voltage I_{OL}=3.2mA (Note 1)	V_{OL1}	V_{SS}	0.4	V
Output Low Voltage I_{OL}=12mA	V_{OL2}	V_{SS}	0.4	V
Output High Voltage I_{OH}=-0.2mA (Note 2)	V_{OH1}	4.2		V
Output High Voltage I_{OH}=-0.4mA	V_{OH2}	4.2		V
Input Low Current V_I = 0.5V, V_{CC} = 5.25V	I_{IL}		-200	μA
Input High Current V_I = 2.4V, V_{CC} = 5.25V	I_{IH}		20	μA
Input High Current V_I = 5.5V, V_{CC} = 5.25V	I_I		200	μA
Output Short Circuit Current V_O=0V	I_{OS}	-15	-100	mA
Input Clamp Voltage I_I = -18mA, V_{CC} = 4.75V	V_{IC}		-1.5	V
Power Supply Current	I_{CC}		100	μA
Output HI-Z Leak Current 3-State Output Pins	I_{OZ1}	-100	100	μA
Output HI-Z Leak Current Bidirectional Pins	I_{OZ2}	-300	120	μA

NOTES
1. All bus outputs and PP<3:> have I_{OL} = 3.2mA.
2. All outputs and bidirectional pins.

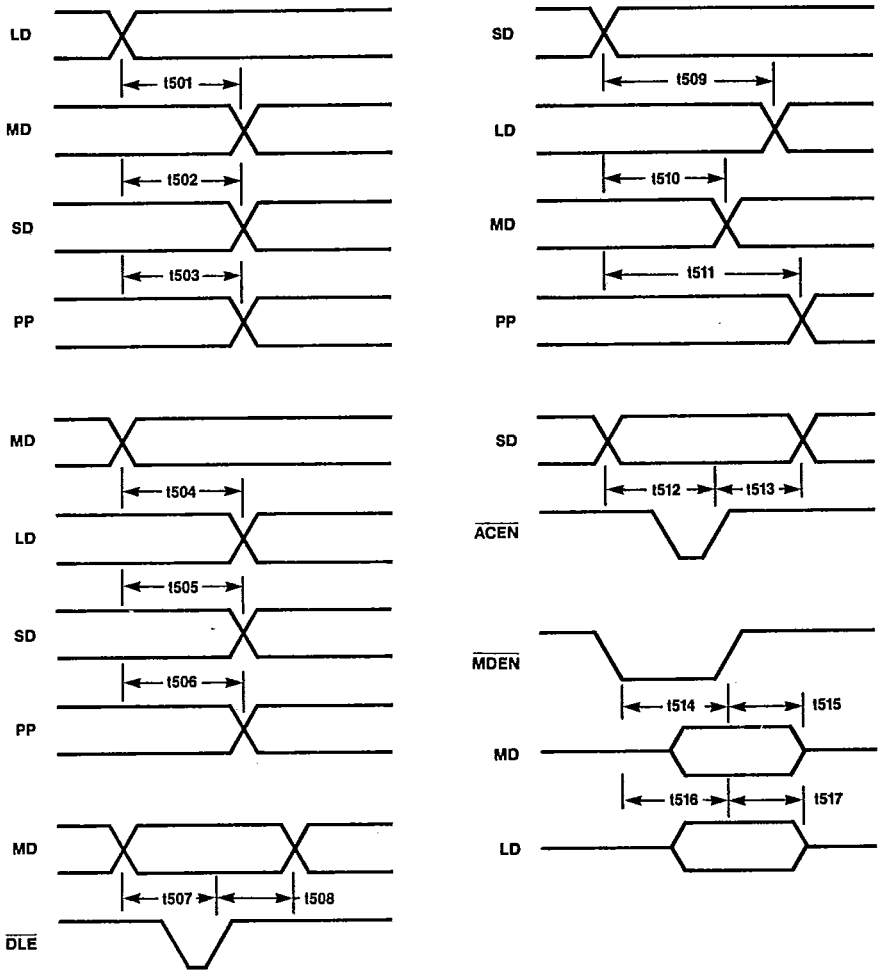
82A305 AC Characteristics

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Sym	Description	82A305-16 82C305-16 Min	Typ	Max	82B305-20 Min	Typ	Max	Unit	Notes
t501	MD data valid from LD data valid	4		15	4		13	ns	C_L=35pF
t502	SD data valid delay from LD data valid	4		27	4		23	ns	
t503	PP data valid delay from LD data valid	5		29	5		25	ns	
t504	LD data valid delay from MD data valid	4	17	15	4	13	13	ns	C_L=35pF
t505	SD data valid delay from MD data valid	4		28	4		25	ns	
t506	PP data valid delay from MD data valid	5		30	5		25	ns	
t507	MD data set-up time to $\overline{DLE}$	4			1			ns	
t508	MD data hold time from $\overline{DLE}$	5			5			ns	
t509	LD data valid delay from SD data valid	8		38	8		36	ns	
t510	MD data valid delay from SD data valid	4		27	4		25	ns	
t511	PP data valid delay from SD data valid	5		33	5		30	ns	
t512	SD data set-up time to $\overline{ACEN}$	10			10			ns	
t513	SD data hold time from $\overline{ACEN}$	5			5			ns	
t514	MD data valid delay from $\overline{MDEN}$	7		29	7		25	ns	
t515	MD tri-state delay from $\overline{MDEN}$	5		23	5		23	ns	
t516	LD data valid delay from $\overline{MDEN}$	7		30	7		30	ns	
t517	LD tri-state delay from $\overline{MDEN}$	5		23	5		23	ns	

Test Load = 65pF unless otherwise specified.

82A305 TIMING DIAGRAMS



82A306/82C306 Control Buffer

- 14.318MHz oscillator and divide by 12 counter
- Byte enable latch
- Parity Checking
- Direct interface to AT Bus
- Advanced Schottky TTL technology

Functional Description

14MHz Oscillator and Divider

The color reference oscillator is provided eliminating the 8224 normally used in AT compatible systems. A divide by 12 counter is also included to generate the OSC/12 (1.19MHz) signal used on the system board.

$\overline{AF32}$ Generation

The $\overline{AF32}$ is used in the CS 8230 system to indicate that the current bus cycle is a CPU local bus cycle.

Byte Enable Latch

The register that holds the byte enables valid during a memory cycle is located on the 82A306. An additional input $\overline{FBE}$ is provided to force all byte enables active during certain memory operations. A pullup resistor is provided on the $\overline{FBE}$ input for implementations not requiring this feature.

Parity Checking and Generation

The 82A306 provides the necessary exclusive OR'ing to generate full (byte) write and read parity from the partial parity bits PPH<3:0> and PPL<3:0> generated on the two (nibble wide) data buffers 82A305.

For a memory read access, read parity PPH<3:0> and PPL<3:0> are checked against the parity bits MP<3:0> read from memory. These parity bits are latched by $\overline{CAS}$ and $\overline{PCHK}$ so that they are kept valid during parity checking. The results of the byte-wise comparison are further gated by byte enables to ignore errors for bytes which are not valid. The OR'ed byte-wise parity error is then latched as the output LPAR if $\overline{PEN}$ input is asserted.

During a memory write access, write parity for each byte is generated from PPH<3:0> and PPL<3:0> and can be gated onto the memory parity bus MP<3:0> if enabled by $\overline{WPE}$ controlling the tri-state drivers. If an external parity generation circuit is used, an internal pullup resistor is provided for $\overline{WPE}$ to disable the write parity output buffers if left unconnected.

Bus Drivers

24mA drivers are provided for some of the control signals on the IO channel. These include SYSCLK, OSC, OSC/12, RDRV, $\overline{SBHE}$, $\overline{BALE}$, $\overline{IOR}$, $\overline{IOW}$, $\overline{MEMR}$, $\overline{MEMW}$, $\overline{SMEMR}$, $\overline{SMEMW}$ and $\overline{OUT1}$.

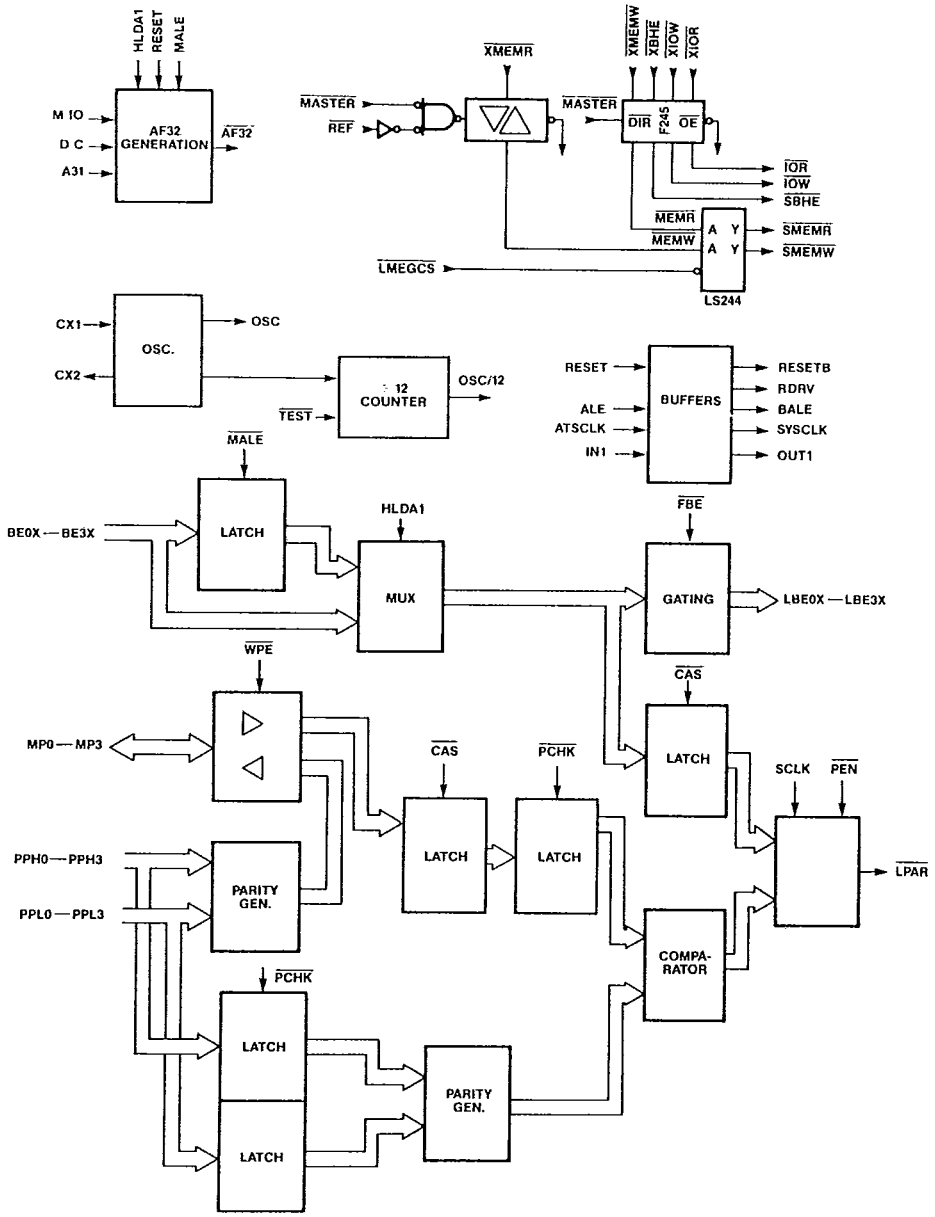


Figure 6-1. 82A306 Functional Block Diagram

82A306 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	—	7.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{op}	-25	85	C
Storage Temperature	T_{stg}	-40	125	C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82A306 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	C

82A306 DC Characteristics

Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.0		V
Output Low Voltage I_{OL}=10mA (Note 1)	V_{OL1}		0.5	V
Output Low Voltage I_{OL}=24mA (Note 2)	V_{OL2}		0.5	V
Output High Voltage I_{OH}-3.3mA (Note 3)	V_{OH}	2.4		V
Input Low Current V_I = 0.5V, V_{CC} = 5.25V	I_{IL}		-200	μA
Input High Current V_I = 2.4V, V_{CC} = 5.25V	I_{IH}		20	μA
Input High Current V_I = 5.5V, V_{CC} = 5.25V	I_I		200	μA
Output Short Circuit Current V_O=0V	I_{OS}	-15	-100	mA
Input Clamp Voltage I_I = -18mA, V_{CC} = 4.75V	V_{IC}		-1.5	V
Power Supply Current	I_{CC}	140	230	mA
Output HI-Z Leak Current 3-State Output Pins	I_{OZ1}	-100	100	μA
Output HI-Z Leak Current Bidirectional Pins	I_{OZ2}	-300	120	μA

NOTES
1. MP<3:0>, $\overline{\text{XIOW}}$, $\overline{\text{XIOR}}$, $\overline{\text{XBHE}}$, $\overline{\text{XMEMW}}$, $\overline{\text{XMEMR}}$, $\overline{\text{RESTEB}}$, $\overline{\text{LBE}}$<3:0> all have I_{OL} = 10mA.
2. $\overline{\text{SBHE}}$, $\overline{\text{IOW}}$, $\overline{\text{IOR}}$, $\overline{\text{MEMW}}$, $\overline{\text{MEMR}}$, $\overline{\text{SMEMW}}$, $\overline{\text{SMEMR}}$, OSC, OSC/12, OUT1, SYSCLK, BALE, RDRV all have I_{OL} = 24mA.
3. All outputs and bidirectional pins.

82C306 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	-0.5	6.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{op}	-25	85	C
Storage Temperature	T_{stg}	-40	125	C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82C306 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	C

82C306 DC Characteristics

Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.0		V
Output Low Voltage I_{OL}=3.2mA (Note 1)	V_{OL1}	V_{SS}	0.4	V
Output Low Voltage I_{OL}=12mA (Note 2)	V_{OL2}	V_{SS}	0.4	V
Output High Voltage I_{OH}=-0.2mA (Note 3)	V_{OH1}	4.2		V
Output High Voltage I_{OH}=-0.4mA	V_{OH2}	4.2		V
Input Low Current V_I = 0.5V, V_{CC} = 5.25V	I_{IL}		-200	μA
Input High Current V_I = 2.4V, V_{CC} = 5.25V	I_{IH}		20	μA
Input High Current V_I = 5.5V, V_{CC} = 5.25V	I_I		200	μA
Output Short Circuit Current V_O=0V	I_{OS}	-15	-100	mA
Input Clamp Voltage I_I = -18mA, V_{CC} = 4.75V	V_{IC}		-1.5	V
Power Supply Current	I_{CC}		100	mA
Output HI-Z Leak Current 3-State Output Pins	I_{OZ1}	-100	100	μA
Output HI-Z Leak Current Bidirectional Pins	I_{OZ2}	-300	120	μA

NOTES
1. MP<3:0>, $\overline{XIOW}$, $\overline{XIOR}$, $\overline{XBHE}$, $\overline{XMEMW}$, $\overline{XMEMR}$, RESETB, $\overline{LBE<3:0>}$ all have I_{OL} = 3.2mA.
2. SBHE, $\overline{IOW}$, $\overline{IOR}$, $\overline{MEMW}$, $\overline{MEMR}$, SMEMW, SMEMR, OSC, OSC/12, OUT1, SYSCLK, BALE, RDRV all have I_{OL} = 24mA.
3. All outputs and bidirectional pins.

82A306 AC Characteristics

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Sym	Description	82C306 82A306 Min	Typ	Max	Unit	Notes
t601	OSC delay from CX1↑	4		22	ns	
t602	OSC delay from CX1↓	5		26	ns	
t603	OSC/12 delay from CX1↑	9		35	ns	
t604	OSC/12 delay from CX1↓	9		37	ns	
t605	$\overline{BE}$<3:0> set-up time to $\overline{MALE}$↑	5			ns	
t606	$\overline{BE}$<3:0> hold time to $\overline{MALE}$↑	5			ns	
t607	$\overline{LBE}$<3:0> valid delay from $\overline{MALE}$↑	7		35	ns	
t608	$\overline{LBE}$<3:0> valid delay from $\overline{BE}$<3:0> valid	3		25	ns	
t609	$\overline{LBE}$<3:0> LO delay from $\overline{FBE}$↓	5		25	ns	
t610	$\overline{LBE}$<3:0> de-asserted from $\overline{FBE}$↑	3		19	ns	
t611	PPH<3:0>, PPL<3:0> set-up time to $\overline{PCHK}$↑	5			ns	
t612	PPH<3:0>, PPL<3:0> hold time to $\overline{PCHK}$↑	5			ns	
t613	MP<3:0> valid delay from corresponding PPH<3:0> and PPL<3:0>	2		21	ns	
t614	MP<3:0> set-up time from $\overline{CAS}$↑	5			ns	
t615	MP<3:0> hold time from $\overline{CAS}$↑	5			ns	
t616	$\overline{LPAR}$ delay from SCLK↑	4		23	ns	
t617	$\overline{LPAE}$ delay from SCLK↑	6		24	ns	
t618	$\overline{LPAR}$ delay from $\overline{PEN}$↑	1		13	ns	
t619	$\overline{LPAR}$ delay from $\overline{PEN}$↓	3		19	ns	
t620	$\overline{MEMW}$ (or $\overline{MEMR}$) delay from $\overline{XMEMW}$ (or $\overline{XMEMR}$)↓	3		19	ns	
t621	$\overline{MEMW}$ (or $\overline{MEMR}$) delay from $\overline{XMEMW}$ (or $\overline{XMEMR}$)	1		14	ns	
t622	$\overline{XMEMW}$ (or $\overline{XMEMR}$) delay from $\overline{MEMW}$ (or $\overline{MEMR}$)↓	4		21	ns	
t623	$\overline{XMEMW}$ (or $\overline{XMEMR}$) delay from $\overline{MEMW}$ (or $\overline{MEMR}$)	1		14	ns	
t624	$\overline{SMEMW}$ (or $\overline{SMEMR}$) delay from $\overline{XMEMW}$ (or $\overline{XMEMR}$)↓	5		23	ns	
t625	$\overline{SMEMW}$ (or $\overline{SMEMR}$) LO to HI-Z transition delay from LMEGCS↓	4		23	ns	

Test Load = 65pF unless otherwise specified.

82A306 AC Characteristics (Continued)
(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Sym	Description	82C306 82A306 Min	Typ	Max	Unit	Notes
t627	$\overline{SMEMW}$ (or $\overline{SMEMR}$) LO to HI-Z transition delay from $\overline{REF}$↓	6		28	ns	
t628	$\overline{SMEMW}$ (or $\overline{SMEMR}$) HI-Z to LO transition delay from $\overline{REF}$↑	8		32	ns	
t629	$\overline{SMEMW}$ (or $\overline{SMEMR}$) delay from XMEMW (or XMEMR)↑	3		19	ns	
t630	$\overline{SMEMW}$ (or $\overline{SMEMR}$) HI to HI-Z transition delay from $\overline{LMEGCS}$↓	4		23	ns	
t631	$\overline{SMEMW}$ (or $\overline{SMEMR}$) HI-Z to HI transition delay from $\overline{LMEGCS}$↑	6		28	ns	
t632	$\overline{SMEMW}$ (or $\overline{SMEMR}$) HI to HI-Z transition delay from $\overline{REF}$↓	6		28	ns	
t633	$\overline{SMEMW}$ (or $\overline{SMEMR}$) HI-Z to HI transition delay from $\overline{REF}$↑	8		32	ns	
t634	$\overline{SMEMW}$ (or $\overline{SMEMR}$) delay from $\overline{MEMW}$ (or $\overline{MEMR}$)↑	5		23	ns	
t635	$\overline{SMEMW}$ (or $\overline{SMEMR}$) delay from $\overline{MEMW}$ (or $\overline{MEMR}$)↑	3		19	ns	
t636	$\overline{IOW}$ (or $\overline{IOR}$) delay from $\overline{XIOW}$ (or $\overline{XIOR}$)↓	3		18	ns	
t637	$\overline{IOW}$ (or $\overline{IOR}$) delay from $\overline{XIOW}$ (or $\overline{XIOR}$)↑	1		14	ns	
t638	$\overline{XIOW}$ (or $\overline{XIOR}$) delay from $\overline{IOW}$ (or $\overline{IOR}$)↓	4		21	ns	
t639	$\overline{XIOW}$ (or $\overline{XIOR}$) delay from $\overline{IOW}$ (or $\overline{IOR}$)↑	1		14	ns	
t640	$\overline{SBHE}$ delay from $\overline{XBHE}$↓	3		18	ns	
t641	$\overline{SBHE}$ delay from $\overline{XBHE}$↑	1		14	ns	
t642	$\overline{XBHE}$ delay from $\overline{SBHE}$↓	4		21	ns	
t643	$\overline{XBHE}$ delay from $\overline{SBHE}$↑	1		14	ns	
t644	RESETB delay from RESET↓	3		20	ns	
t645	RESETB delay from RESET↑	1		14	ns	
t646	RDRV delay from RESET↓	3		18	ns	
t647	RDRV delay from RESET↑	1		14	ns	
t648	$\overline{BALE}$ delay from ALT↓ SYSCLK delay from ATSCLK↓ OUT1 delay from IN1↓	2		17	ns	

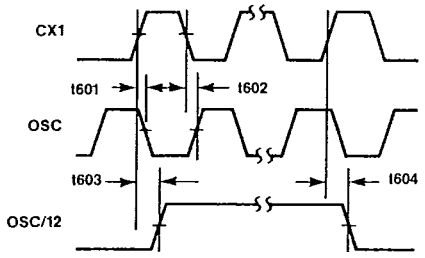
Test Load = 65pF unless otherwise specified.

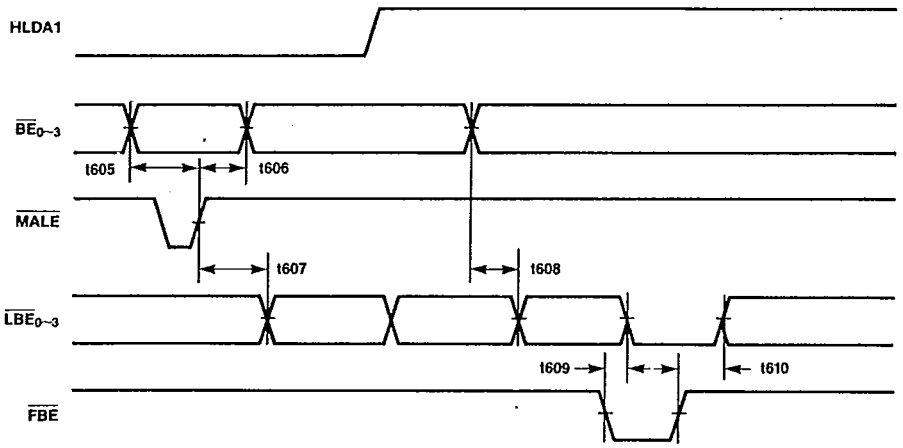
82A306 AC Characteristics (Continued)
(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Sym	Description	82C306 82A306 Min	Typ	Max	Unit	Notes
t649	$\overline{BALE}$ delay from ALT↑ SYSCLK delay from ATSCLK↑ OUT1 delay from IN1↑	1		13	ns	
t650	M/$\overline{IO}$, D/$\overline{C}$, A31 set-up time to $\overline{MALE}$↑	5			ns	
t651	M/$\overline{IO}$, D/$\overline{C}$, A31 hold time to $\overline{MALE}$↑	5			ns	
t652	$\overline{AF32}$ HI-Z to LO transition delay from $\overline{MALE}$↑	7		32	ns	
t653	$\overline{AF32}$ LO to HI-Z transition delay from $\overline{MALE}$↑	6		29	ns	
t654	$\overline{AF32}$ LO to HI-Z transition delay from RESET	6		28	ns	
t655	$\overline{AF32}$ HI-Z transition delay from HLDA1	6		29	ns	

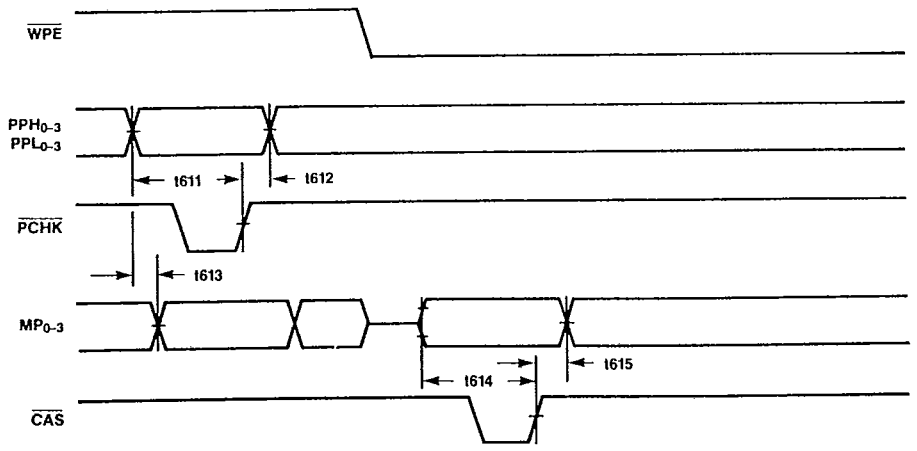
Test Load = 65pF unless otherwise specified.

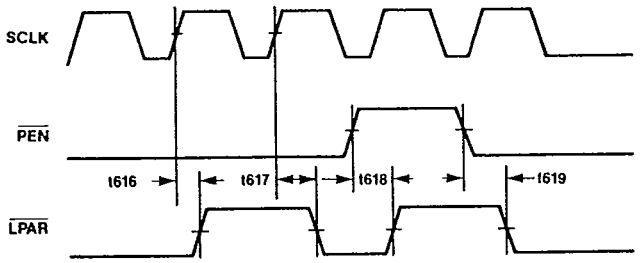
82A306 TIMING DIAGRAMS



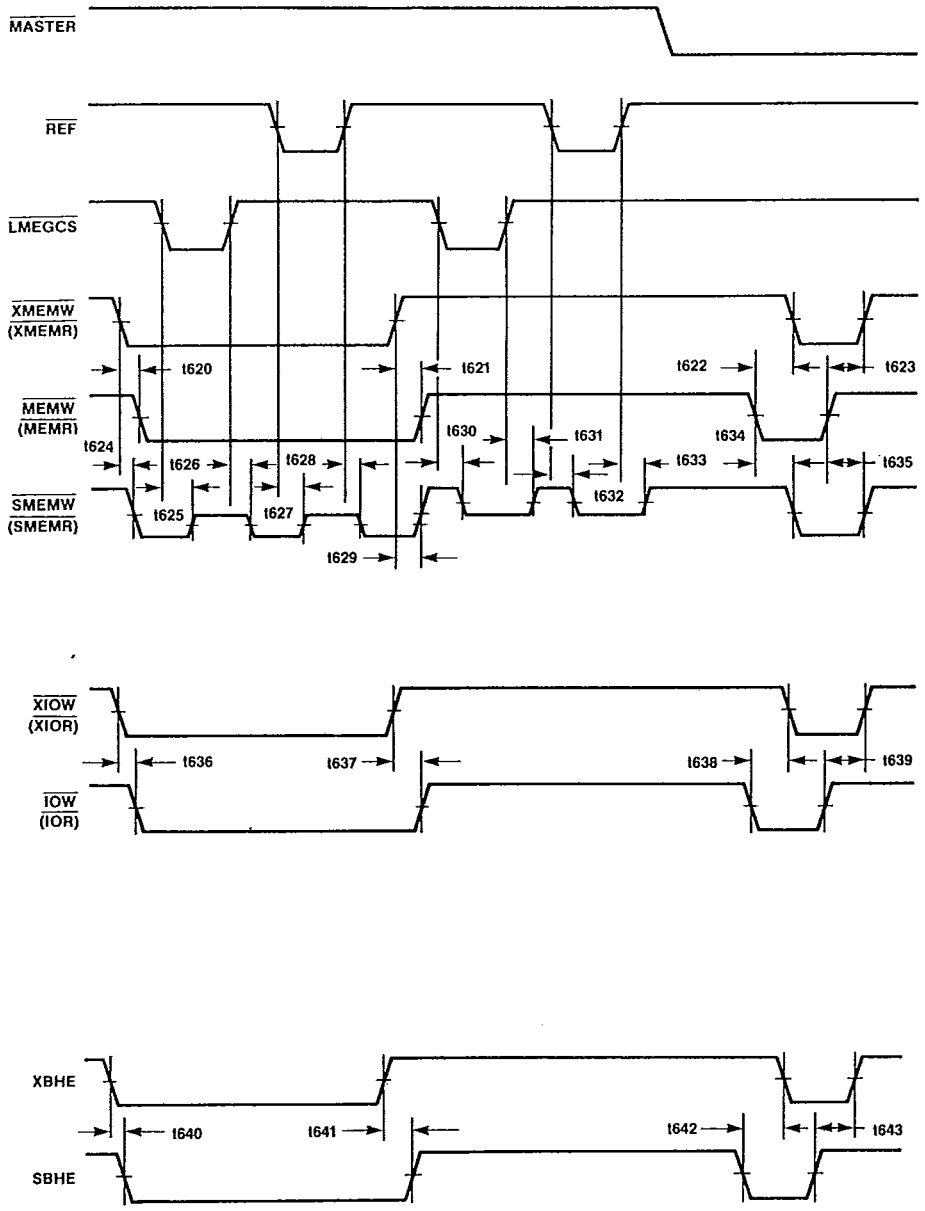


82A306 TIMING DIAGRAMS

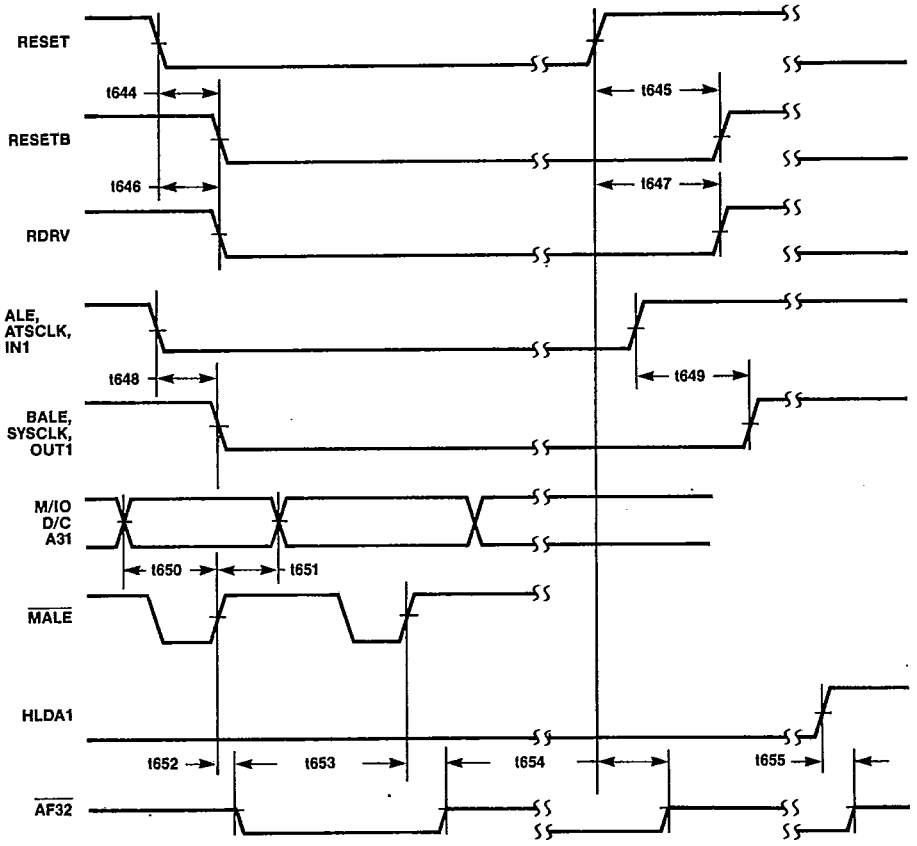




82A306 TIMING DIAGRAMS



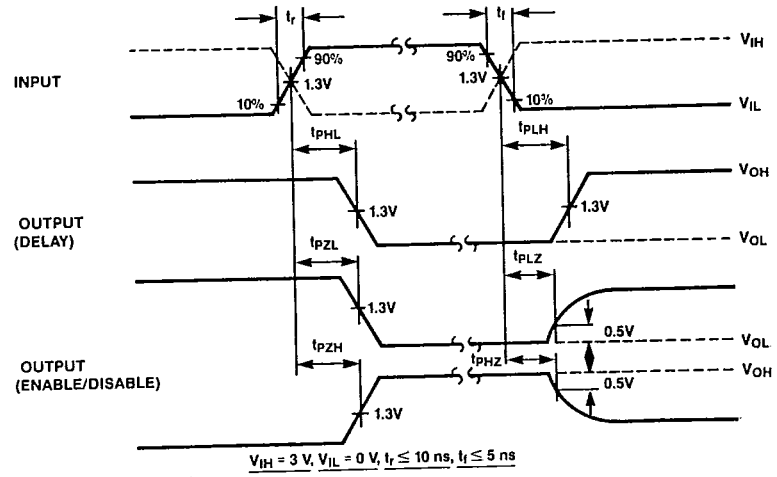
82A306 TIMING DIAGRAMS

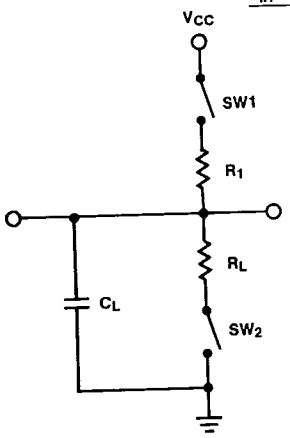


CHIPS

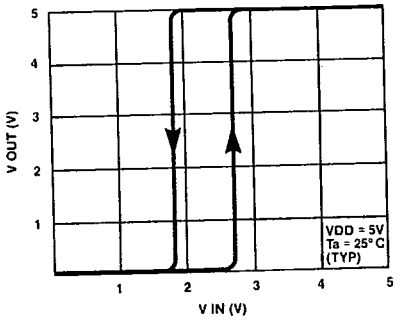
Load Circuit Measurement Conditions

Parameter	Output Type	Symbol	C_L(pF)	R_1 (Ω)	R_L (Ω)	SW_1	SW_2
Propagation Delay Time	Totem pole 3-state Bidirectional	t_{PLH} t_{PHL}	50	—	1.0K	OFF	ON
Propagation Delay Time	Open drain or Open Collector	t_{PLH} t_{PHL}	50	0.5K	—	ON	OFF
Disable Time	3-state Bidirectional	t_{PLZ} t_{PHZ}	5	0.5K	1.0K	ON OFF	ON
Enable Time	3-state Bidirectional	t_{PZL} t_{PZH}	50	0.5K	1.0K	ON OFF	ON ON



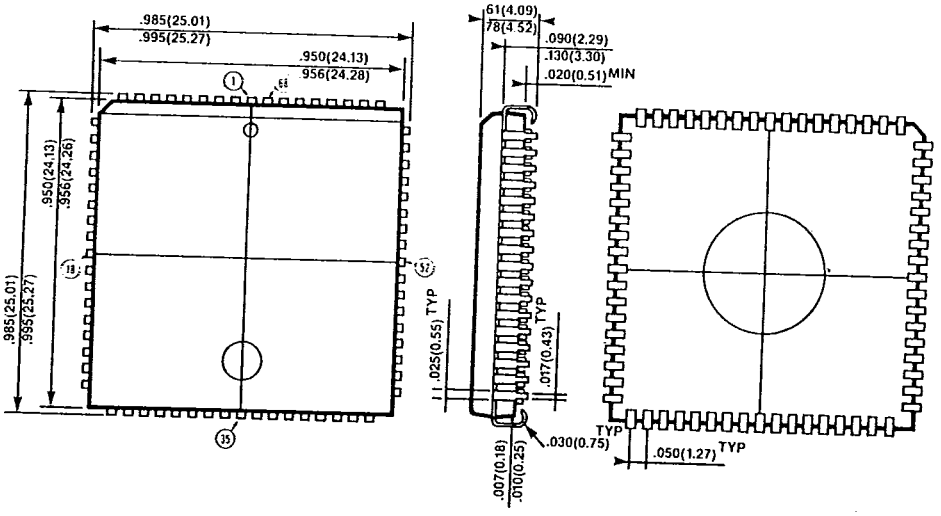


Reset 1 DC Characteristics



Load Circuit and AC Characteristics Measurement Waveform

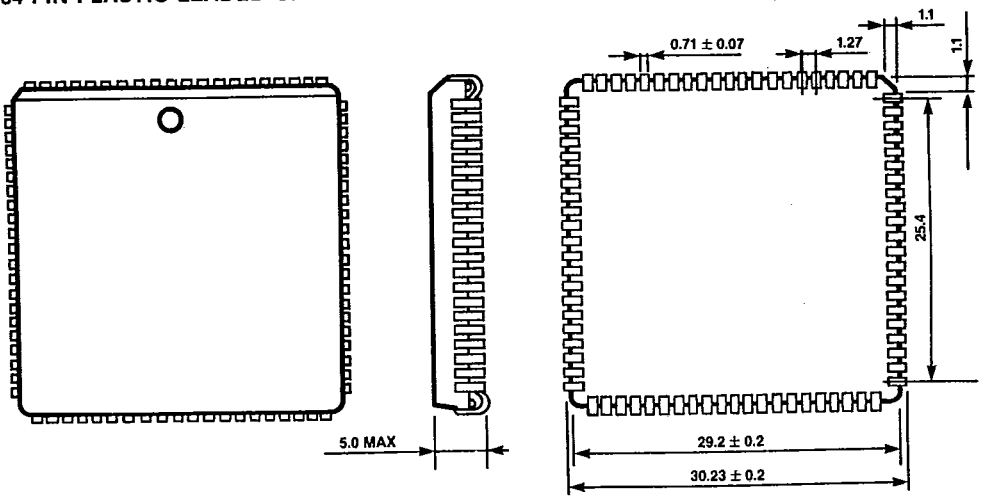
68-LEAD PLASTIC CHIP CARRIER



DIMENSIONS IN INCHES (MILLIMETERS) S = 3.6/1

84-PIN PLASTIC LEADED CHIP CARRIER

UNIT (mm)



82A303 Absolute Maximum Ratings

Order Number	Package Type Note 1	Remarks
P82C301	PLCC-84	C (Note 2)
P82C302	PLCC-84	C
P82A303	PLCC-68	C
P82A304	PLCC-68	C
P82A305	PLCC-68	C
P82A306	PLCC-68	C
CS8230	—	Standard CHIPSet (Note 3)

NOTES
1. PLCC = Plastic Leaded Chip Carrier 84 Pins
2. C = Commercial Range, 0° to 70°C, V_{DD} = 4.75 to 5.25 V
3. CS8230 consists of P82C301, P82C302, P82A303, P82A304, P82A305, P82A306.