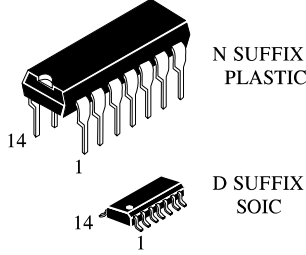


IW4069UB

Hex Inverter
High-Voltage Silicon-Gate CMOS

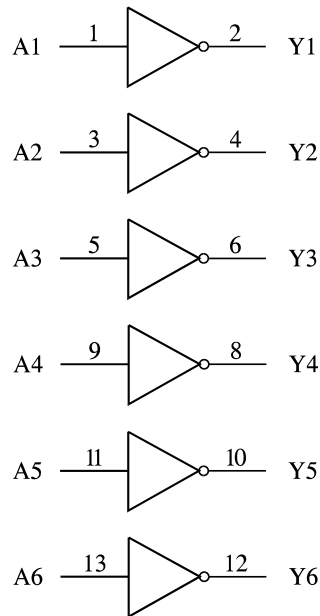
The IW4069UB types consist of six inverter circuits. These devices are intended for all general-purpose inverter applications where the medium-power TTL-drive and logic-level-conversion capabilities of circuits such as the IW4049UB Hex Inverter/Buffers are not required. Each of the six inverters is a single stage

- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1 μ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
 - 0.5 V min @ 5.0 V supply
 - 1.0 V min @ 10.0 V supply
 - 1.5 V min @ 15.0 V supply



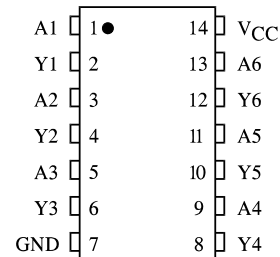
ORDERING INFORMATION
 IW4069UBN Plastic
 IW4069UBD SOIC
 IZ4069UB CHIP
 T_A = -55° to 125° C for all packages

LOGIC DIAGRAM



PIN 14 = V_{CC}
 PIN 7 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Inputs	Output
A	Y
L	H
H	L

L – LOW voltage level
 H – HIGH voltage level

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +20	V
V _{IN}	DC Input Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
I _{IN}	DC Input Current, per Pin	±10	mA
P _D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	500 500	mW
P _{tot}	Power Dissipation per Output Transistor	100	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 12 mW/°C from 100° to 125°C
SOIC Package: - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	3.0	18	V
V _{IN} , V _{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-55	+125	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				≥-55°C	25°C	≤125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} =0.5V	5.0	4.0	4.0	4.0	V
		V _{OUT} =1.0 V	10	8.0	8.0	8.0	
		V _{OUT} =1.5V	15	12.5	12.5	12.5	
V _{IL}	Maximum Low - Level Input Voltage	V _{OUT} = V _{CC} - 0.5 V	5.0	1.0	1.0	1.0	V
		V _{OUT} = V _{CC} - 1 V	10	2.0	2.0	2.0	
		V _{OUT} = V _{CC} - 1.5 V	15	2.5	2.5	2.5	
V _{OH}	Minimum High-Level Output Voltage	V _{IN} =GND	5.0	4.95	4.95	4.95	V
			10	9.95	9.95	9.95	
			15	14.95	14.95	14.95	
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} = V _{CC}	5.0	0.05	0.05	0.05	V
			10	0.05	0.05	0.05	
			15	0.05	0.05	0.05	
I _{IN}	Maximum Input Leakage Current	V _{IN} = GND or V _{CC}	18	±0.1	±0.1	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{IN} = GND or V _{CC}	5.0	0.25	0.25	7.5	μA
			10	0.5	0.5	15	
			15	1.0	1.0	30	
			20	5.0	5.0	150	
I _{OL}	Minimum Output Low (Sink) Current	V _{IN} = GND or V _{CC} U _{OL} =0.4 V U _{OL} =0.5 V U _{OL} =1.5 V	5.0	0.64	0.51	0.36	mA
			10	1.6	1.3	0.9	
			15	4.2	3.4	2.4	
I _{OH}	Minimum Output High (Source) Current	V _{IN} = GND or V _{CC} U _{OH} =2.5 V U _{OH} =4.6 V U _{OH} =9.5 V U _{OH} =13.5 V	5.0	-2.0	-1.6	-1.15	mA
			5.0	-0.64	-0.51	-0.36	
			10	-1.6	-1.3	-0.9	
			15	-4.2	-3.4	-2.4	

AC ELECTRICAL CHARACTERISTICS($C_L=50\text{pF}$, $R_L=200\text{k}\Omega$, Input $t_r=t_f=20\text{ ns}$)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			≥-55°C	25°C	≤125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A to Output Y (Figure 1)	5.0	110	110	110	ns
		10	60	60	80	
		15	50	50	80	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figure 1)	5.0	200	200	200	ns
		10	100	100	100	
		15	80	80	80	
C _{IN}	Maximum Input Capacitance	-		15		pF

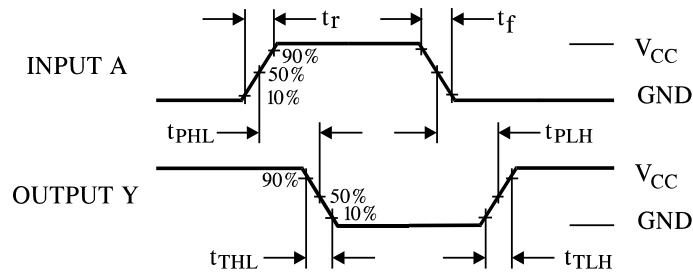
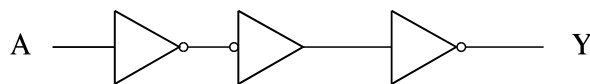
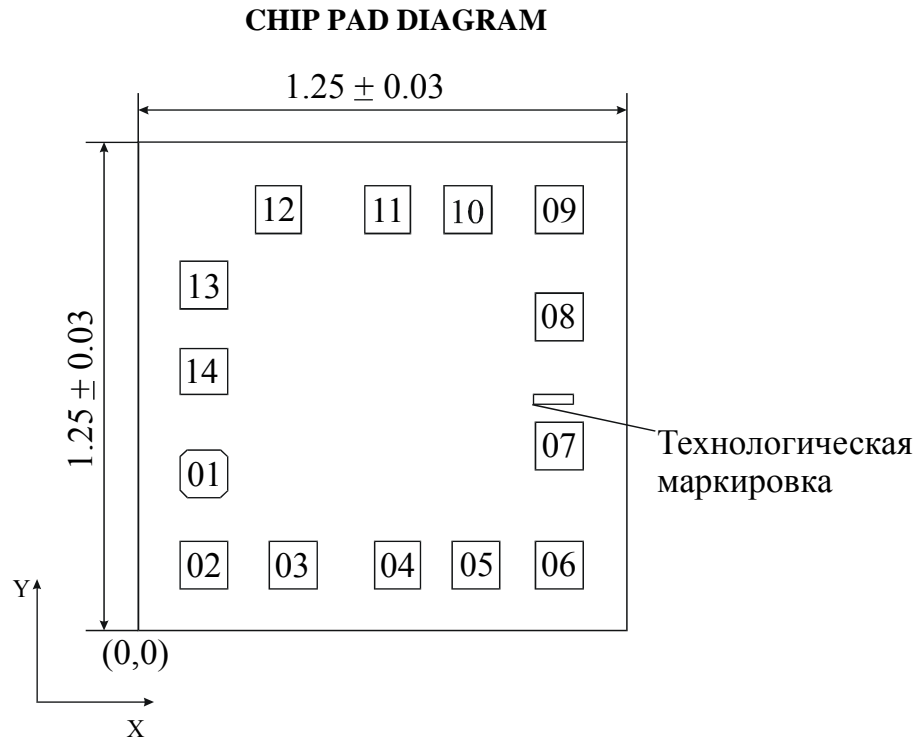


Figure 1. Switching Waveforms

**EXPANDED LOGIC DIAGRAM
(1/6 of the Device)**





Chip marking :406915

Location of marking (mm): left lower corner $x = 1.015$, $y = 0.580$

Chip thickness: 0.46 ± 0.02 mm

PAD LOCATION

Pad No	Symbol	Location (left lower corner), mm		Pad size, mm
		X	Y	
01	A1	0.114	0.348	0.120×0.120
02	Y1	0.114	0.112	0.120×0.120
03	A2	0.343	0.112	0.120×0.120
04	Y2	0.604	0.112	0.120×0.120
05	A3	0.804	0.112	0.120×0.120
06	Y3	1.019	0.112	0.120×0.120
07	GND	1.019	0.417	0.120×0.120
08	Y4	1.019	0.743	0.120×0.120
09	A4	1.019	1.019	0.120×0.120
10	Y5	0.784	1.019	0.120×0.120
11	A5	0.574	1.019	0.120×0.120
12	Y6	0.301	1.019	0.120×0.120
13	A6	0.114	0.826	0.120×0.120
14	V _{cc}	0.114	0.604	0.120×0.120

Note: Location is given as per passivation layer