

IW4066B

Quad Bilateral Switch
High-Voltage Silicon-Gate CMOS

The IW4066B is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. In addition, the on-state resistance is relatively constant over the full input-signal range.

The IW4066B consists of four independent bilateral switches. A single control signal is required per switch. Both the p and the n device in a given switch are biased on or off simultaneously by the control signal. (As show in Fig.1.) The well of the n-channel device on each switch is either tied to the input when the switch is on or to GND when the switch is off. This configuration eliminates the variation of the switch-transistor threshold voltage with input signal, and thus keeps the on-state resistance low over the full operating-signal range.

The advantages over single-channel switches include peak input-signal voltage swings equal to the full supply voltage and more constant on-state impedance over the input-signal range.

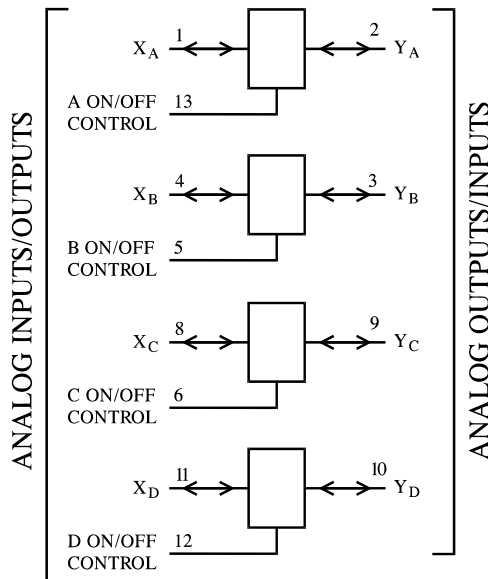
- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1 μ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
 - 1.0 V min @ 5.0 V supply
 - 2.0 V min @ 10.0 V supply
 - 2.5 V min @ 15.0 V supply

ORDERING INFORMATION

IW4066BN Plastic DIP
IW4066BD SOIC
IZ4066B chip

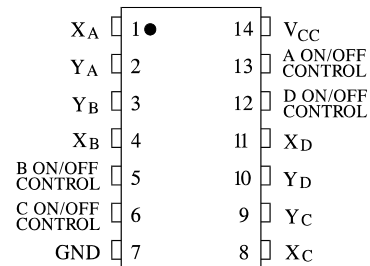
$T_A = -55^\circ$ to 125° C for all packages

LOGIC DIAGRAM



PIN 14 = V_{CC}
PIN 7 = GND

PIN ASSIGNMENT



FUNCTION TABLE

On/Off Control Input	State of Analog Switch
L	Off
H	On

H = high level
L = low level

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +20	V
V _{IN}	DC Input Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
I _{IN}	DC Input Current, per Pin	±10	mA
P _D	Power Dissipation in Still Air	500* ¹	mW
P _{tot}	Power Dissipation per Output Transistor	100	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SO Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

*¹ - for Plastic DIP from -55° to +100°C, for SO Package from -55° to +65°C.

+Derating - Plastic DIP: - 12 mW/°C from 100° to 125°C

SO Package: - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	3.0	18	V
V _{IN}	DC Input Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-55	+125	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$.

Unused digital pins must be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused Analog I/O pins may be left open or terminated.

DC ELECTRICAL CHARACTERISTICS Digital Section

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				≥ -55 °C	≤ 25 °C	≤ 125 °C	
V _{IHC}	Minimum High-Level Input Voltage, Channel-Select or Enable Inputs		5	3.5	3.5	3.5	V
			10	7	7	7	
			15	11	11	11	
V _{ILC}	Maximum Low -Level Input Voltage, Channel-Select or Enable Inputs		5.0	1	1	1	V
			10	2	2	2	
			15	2	2	2	
I _{IN}	Maximum Input Leakage Current, Channel-Select or Enable Inputs	V _{IN} =V _{CC} or GND	18	±0.1	±0.1	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)		5.0	0.25	0.25	7.5	μA
			10	0.5	0.5	15	
			15	1	1	30	
			20	5	5	150	

DC ELECTRICAL CHARACTERISTICS Analog Section

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				≥ -55 °C	≤ 25 °C	≤ 125 °C	
R _{ON}	Maximum "ON" Resistance	V _C = V _{CC} V _{IS} = GND to V _{CC}	5.0	800	1000	1150	Ω
			10	310	400	550	
			15	190	240	320	
ΔR _{ON}	Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	V _C = V _{CC} V _{IS} = GND to V _{CC}	5.0	-	15*	-	Ω
			10	-	10*	-	
			15	-	5*	-	
I _{OFF}	Maximum Off- Channel Leakage Current, Any One Channel	V _{IL} = 0 V, V _{IH} = 18 V	18	±0.1	±0.1	±1.0	μA
	Maximum Off- Channel Leakage Current, Common Channel	V _{IL} = 0 V, V _{IH} = 18 V	18	±0.1	±0.1	±1.0	

* - Typical Value

AC ELECTRICAL CHARACTERISTICS($C_L=50\text{pF}$, Input $t_r=t_f\leq 20\text{ ns}$)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit	
			≥-55°C	25°C	≤125°C		
t _{PHL} (t _{PLH})	Maximum Propagation Delay, Analog Input to Analog Output (Figure 2) R _L =200 kΩ	5.0	40	40	40	ns	
		10	20	20	20		
		15	15	15	15		
t _{PLZ} (t _{PHZ}), t _{PZL} (t _{PZH})	Maximum Propagation Delay, ON/OFF Control to Analog Output (Figure 3) R _L =1 kΩ	5.0	70	70	70	ns	
		10	40	40	40		
		15	30	30	30		
C _{IN}	Maximum Input Capacitance	5	-	7.5	-	pF	
C _{I/O}	Maximum Capacitance V _{CC} = GND = -5V					pF	
		Analog Input	5	-	8*		-
		Analog Output	5	-	6*		-
		Between Analog Input and Analog Output	5	-	0.5*		-

ADDITIONAL APPLICATION CHARACTERISTICS

Symbol	Parameter	Test Conditions	V _{CC} V	Limit 25°C	Unit
THD	Total Harmonic Distortion	V _C = V _{CC} , V _{IS} = 5 V R _L = 10 kΩ, f _{IS} = 1 kHz sine wave	5	0.4	%
B _w	Maximum On-Channel Bandwidth or Minimum Frequency Response	C _L = 50 pF, t _r , t _f ≤ 20 ns R _L = 1 kΩ	5	40	MHz
f ₁	Feedthrough Frequency	C _L = 50 pF, t _r , t _f ≤ 20 ns R _L = 1 kΩ	10	1	MHz
f ₂	Signal Crosstalk Frequency	C _L = 50 pF, t _r , t _f ≤ 20 ns R _L = 1 kΩ	5	8	MHz
V _{AO/I}	Cross talk (Control Input to Signal Output)	R _L = 10 kΩ, t _r , t _f ≤ 20 ns V _C = 10 V	10	50	mV
fs	Maximum Control Input Repetition Rate	C _L = 50 pF, t _r , t _f ≤ 20 ns R _L = 1 kΩ	5	6	MHz
			10	9	
			15	9.5	

V _{CC} (V)	V _{IS} (V)	Switch Input			Switch Output, V _{OS} (V)	
		I _{IS} (mA)			Min	Max
		-55 °C	+25 °C	+125 °C		
5	0	0.64	0.51	0.36	-	0.4
5	5	-0.64	-0.51	-0.36	4.6	-
10	0	1.6	1.3	0.9	-	0.5
10	10	-1.6	-1.3	-0.9	9.5	-
15	0	4.2	3.4	2.4	-	1.5
15	15	-4.2	-3.4	-2.4	13.5	-

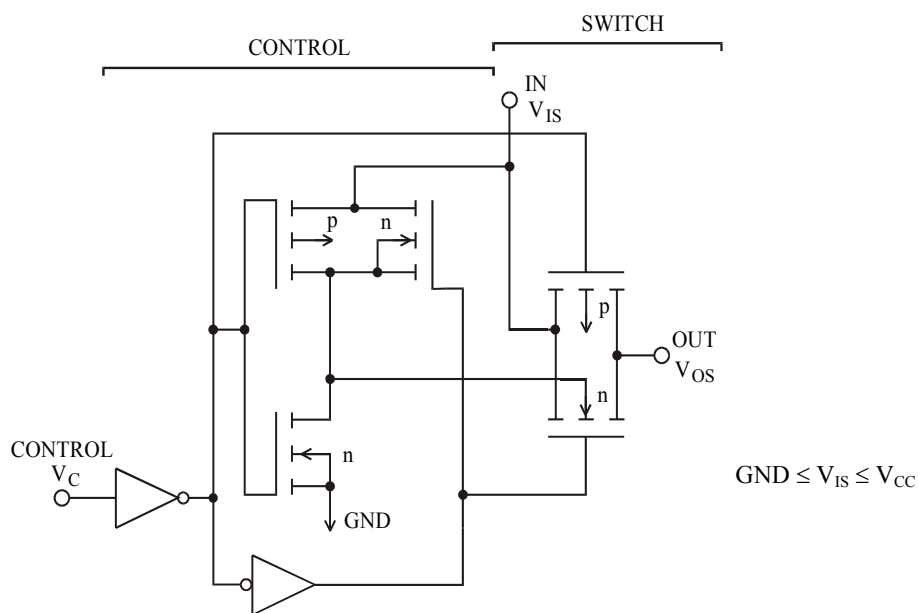


Figure 1. Schematic diagram of 1 of 4 identical switches and its associated control circuitry.

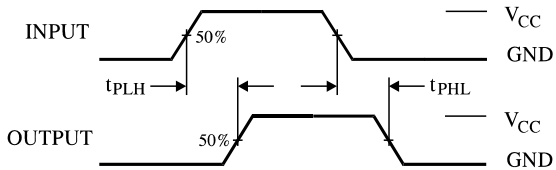


Figure 2. Switching Waveforms

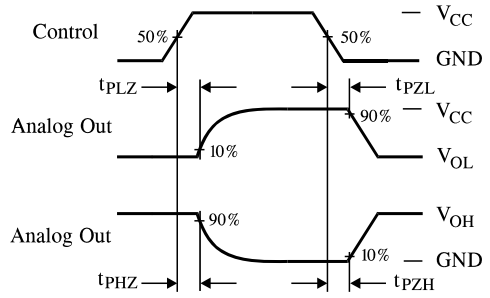
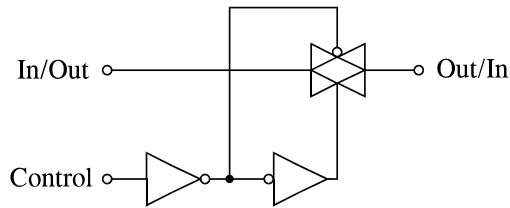


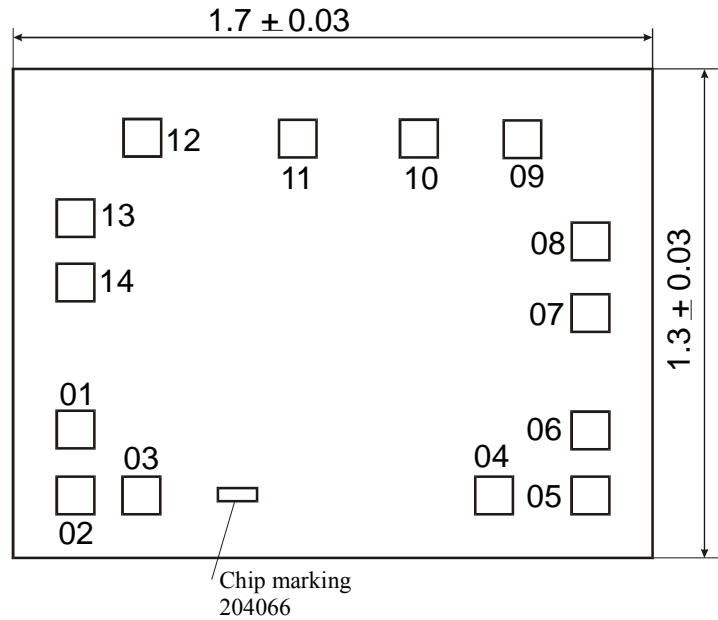
Figure 3. Switching Waveforms

**EXPANDED LOGIC DIAGRAM
(1/4 of the Device)**



Control	Switch
GND = L	OFF
V _{CC} = H	ON

CHIP PAD DIAGRAM



Location of marking (mm): left lower corner $x=0.740$, $y=0.147$, right higher corner $x=0.854$, $y=0.180$
Chip thickness: 0.46 ± 0.02 mm

PAD LOCATION

Pad No	Pin No	Location (left lower corner), mm		Pad size, mm
		X	Y	
01	01	0.116	0.289	0.110 x 0.110
02	02	0.116	0.116	0.110 x 0.110
03	03	0.291	0.116	0.110 x 0.110
04	04	1.229	0.116	0.110 x 0.110
05	05	1.485	0.116	0.110 x 0.110
06	06	1.485	0.291	0.110 x 0.110
07	07	1.485	0.601	0.110 x 0.110
08	08	1.485	0.792	0.110 x 0.110
09	09	1.304	1.063	0.110 x 0.110
10	10	1.029	1.063	0.110 x 0.110
11	11	0.707	1.063	0.110 x 0.110
12	12	0.291	1.063	0.110 x 0.110
13	13	0.116	0.853	0.110 x 0.110
14	14	0.116	0.681	0.110 x 0.110

Note: Pad location is given as per passivation layer