

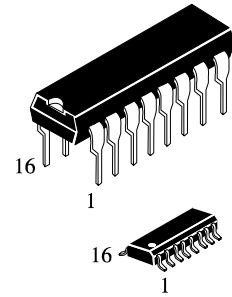
IN74ACT138

1-OF-8 DECODER/DEMULTIPLEXER High-Speed Silicon-Gate CMOS

The IN74ACT138 is identical in pinout to the LS/ALS138, HC/HCT138. The IN74ACT138 may be used as a level converter for interfacing TTL or NMOS outputs to High Speed CMOS inputs.

The IN74ACT138 decodes a three-bit Address to one-of-eight active-low outputs. This device features three Chip Select inputs, two active-low and one active-high to facilitate the demultiplexing, cascading, and chip-selecting functions. The demultiplexing function is accomplished by using the Address inputs to select the desired device output; one of the Chip Selects is used as a data input while the other Chip Selects are held in their active states.

- TTL/NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 μ A; 0.1 μ A @ 25°C
- Outputs Source/Sink 24 mA



N SUFFIX
PLASTIC

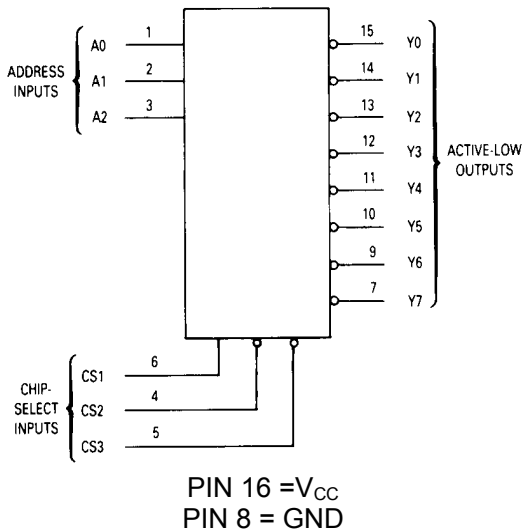
D SUFFIX
SOIC

ORDERING INFORMATION
IN74ACT138N Plastic
IN74ACT138D SOIC
 $T_A = -40^\circ$ to 85° C for all packages

PIN ASSIGNMENT

| | | | |
|-----|---|----|-----------------|
| A0 | 1 | 16 | V _{CC} |
| A1 | 2 | 15 | Y0 |
| A2 | 3 | 14 | Y1 |
| CS2 | 4 | 13 | Y2 |
| CS3 | 5 | 12 | Y3 |
| CS1 | 6 | 11 | Y4 |
| Y7 | 7 | 10 | Y5 |
| GND | 8 | 9 | Y6 |

LOGIC DIAGRAM



FUNCTION TABLE

| Inputs | | | | Outputs | | | | | | | |
|--------|-----|-----|----------|---------|----|----|----|----|----|----|----|
| CS1 | CS2 | CS3 | A2 A1 A0 | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| X | X | H | X X X | H | H | H | H | H | H | H | H |
| X | H | X | X X X | H | H | H | H | H | H | H | H |
| L | X | X | X X X | H | H | H | H | H | H | H | H |
| H | L | L | L L L | L | H | H | H | H | H | H | H |
| H | L | L | L L H | H | L | H | H | H | H | H | H |
| H | L | L | L H L | H | H | L | H | H | H | H | H |
| H | L | L | L H H | H | H | H | L | H | H | H | H |
| H | L | L | H L L | H | H | H | H | L | H | H | H |
| H | L | L | H L H | H | H | H | H | H | L | H | H |
| H | L | L | H H L | H | H | H | H | H | H | L | H |
| H | L | L | H H H | H | H | H | H | H | H | H | L |

H = high level (steady state)

L = low level (steady state)

X = don't care

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MAXIMUM RATINGS*

| Symbol | Parameter | Value | Unit |
|-----------|---|------------------------|--------------------|
| V_{CC} | DC Supply Voltage (Referenced to GND) | -0.5 to +7.0 | V |
| V_{IN} | DC Input Voltage (Referenced to GND) | -0.5 to $V_{CC} + 0.5$ | V |
| V_{OUT} | DC Output Voltage (Referenced to GND) | -0.5 to $V_{CC} + 0.5$ | V |
| I_{IN} | DC Input Current, per Pin | ± 20 | mA |
| I_{OUT} | DC Output Sink/Source Current, per Pin | ± 50 | mA |
| I_{CC} | DC Supply Current, V_{CC} and GND Pins | ± 50 | mA |
| P_D | Power Dissipation in Still Air, Plastic DIP+ SOIC Package+ | 750 500 | mW |
| Tstg | Storage Temperature | -65 to +150 | $^{\circ}\text{C}$ |
| T_L | Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) | 260 | $^{\circ}\text{C}$ |

Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/ $^{\circ}\text{C}$ from 65 $^{\circ}$ to 125 $^{\circ}\text{C}$

SOIC Package: : - 7 mW/ $^{\circ}\text{C}$ from 65 $^{\circ}$ to 125 $^{\circ}\text{C}$

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|-------------------|---|--|----------------|--------------------|
| V_{CC} | DC Supply Voltage (Referenced to GND) | 4.5 | 5.5 | V |
| V_{IN}, V_{OUT} | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | V_{CC} | V |
| T_J | Junction Temperature (PDIP) | | 140 | $^{\circ}\text{C}$ |
| T_A | Operating Temperature, All Package Types | -40 | +85 | $^{\circ}\text{C}$ |
| I_{OH} | Output Current - High | | -24 | mA |
| I_{OL} | Output Current - Low | | 24 | mA |
| t_r, t_f | Input Rise and Fall Time * (except Schmitt Inputs) | $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 5.5 \text{ V}$ | 0 10 8.0 | ns/V |

* V_{IN} from 0.8 V to 2.0 V

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $\text{GND} \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

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DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | V _{CC} V | Guaranteed Limits | | Unit |
|--------------------|--|--|----------------------|-------------------|---------------|------|
| | | | | 25 °C | -40°C to 85°C | |
| V _{IH} | Minimum High-Level Input Voltage | V _{OUT} =0.1 V or V _{CC} -0.1 V | 4.5 5.5 | 2.0 2.0 | 2.0 2.0 | V |
| V _{IL} | Maximum Low-Level Input Voltage | V _{OUT} =0.1 V or V _{CC} -0.1 V | 4.5 5.5 | 0.8 0.8 | 0.8 0.8 | V |
| V _{OH} | Minimum High-Level Output Voltage | I _{OUT} ≤ -50 μA | 4.5 5.5 | 4.4 5.4 | 4.4 5.4 | V |
| | | *V _{IN} =V _{IH} or V _{IL} I _{OH} =-24 mA I _{OH} =-24 mA | 4.5 5.5 | 3.86 4.86 | 3.76 4.76 | |
| V _{OL} | Maximum Low-Level Output Voltage | I _{OUT} ≤ 50 μA | 4.5 5.5 | 0.1 0.1 | 0.1 0.1 | V |
| | | *V _{IN} = V _{IH} or V _{IL} I _{OL} =24 mA I _{OL} =24 mA | 4.5 5.5 | 0.36 0.36 | 0.44 0.44 | |
| I _{IN} | Maximum Input Leakage Current | V _{IN} =V _{CC} or GND | 5.5 | ±0.1 | ±1.0 | μA |
| ΔI _{CCCT} | Additional Max. I _{CC} /Input | V _{IN} =V _{CC} - 2.1 V | 5.5 | | 1.5 | mA |
| I _{OLD} | +Minimum Dynamic Output Current | V _{OLD} =1.65 V Max | 5.5 | | 75 | mA |
| I _{OHD} | +Minimum Dynamic Output Current | V _{OHD} =3.85 V Min | 5.5 | | -75 | mA |
| I _{CC} | Maximum Quiescent Supply Current (per Package) | V _{IN} =V _{CC} or GND | 5.5 | 8.0 | 80 | μA |

* All outputs loaded; thresholds on input associated with output under test.
+Maximum test duration 2.0 ms, one output loaded at a time.

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AC ELECTRICAL CHARACTERISTICS ($V_{CC}=5.0\text{ V} \pm 10\%$, $C_L=50\text{ pF}$, Input $t_r=t_f=3.0\text{ ns}$)

| Symbol | Parameter | Guaranteed Limits | | | | Unit |
|-----------|--|--------------------------------------|------|---------------|------|------|
| | | 25 °C | | -40°C to 85°C | | |
| | | Min | Max | Min | Max | |
| t_{PLH} | Propagation Delay, Input A to Output Y (Figure 1) | 1.5 | 10.5 | 1.5 | 11.5 | ns |
| t_{PHL} | Propagation Delay, Input A to Output Y (Figure 1) | 1.5 | 10.5 | 1.5 | 11.5 | ns |
| t_{PLH} | Propagation Delay, CS2 or CS3 to Output Y (Figure 3) | 2.5 | 11.5 | 2.0 | 12.5 | ns |
| t_{PHL} | Propagation Delay, CS2 or CS3 to Output Y (Figure 3) | 2.0 | 11.5 | 2.0 | 12.5 | ns |
| t_{PLH} | Propagation Delay, CS1 to Output Y (Figure 2) | 2.5 | 12.0 | 2.0 | 13.0 | ns |
| t_{PHL} | Propagation Delay, CS1 to Output Y (Figure 2) | 2.0 | 10.5 | 1.5 | 11.5 | ns |
| C_{IN} | Maximum Input Capacitance | 4.5 | | 4.5 | | pF |
| C_{PD} | Power Dissipation Capacitance | Typical @25°C, $V_{CC}=5.0\text{ V}$ | | | | pF |
| | | 60 | | | | |

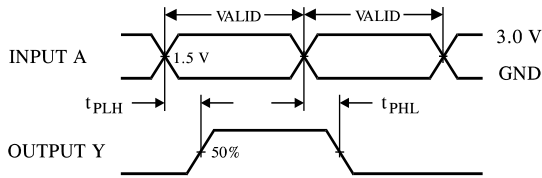


Figure 1. Switching Waveforms

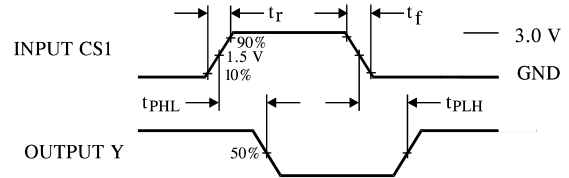


Figure 2. Switching Waveforms

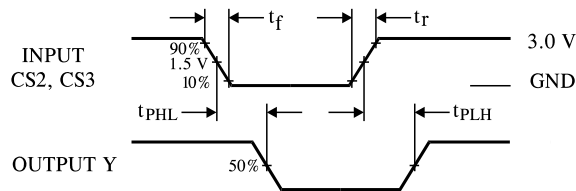


Figure 3. Switching Waveforms

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EXPANDED LOGIC DIAGRAM

