AmPAL16R8 Family

20-Pin IMOX™ Programmable Array Logic (PAL) Elements

Distinctive Characteristics

- AMD's superior IMOX technology
  - Guarantees t_{PD} = 15 ns Max. "B" Versions
- High-Speed, Half-Power ("AL") and Quarter-Power ("Q") versions
- Platinum-silicide fuses and added test words ensure programming yields > 98%
- Post Programming Functional Yields (PPFY) of 99.9%
- PRELOAD feature permits full logical verification
- Reliability assured through more than 70 billion fuse hours of life testing with no failures
- AC and DC parametric testing at the factory through on-board testing circuitry
- AMD's industry-leading quality guarantees

General Description

AMD PAL devices are high-speed, electrically programmable array logic elements. They utilize the familiar sum-of-products (AND-OR) structure allowing users to program custom logic functions to fit most applications precisely. Typically they are a replacement for low-power Schottky SSI/MSI logic circuits, reducing chip count by more than 5 to 1 and greatly simplifying prototyping and board layout.

Seven different devices are available, including both registered and combinatorial devices, in six different speed and power versions. The very High-Speed "B" versions (t_{PD} = 15 ns) run approximately 40% faster than the High-Speed "A" versions (t_{PD} = 25 ns). High-Speed, Half-Power "AL" versions (t_{PD} = 25 ns, I_{CC} = 90 mA) are available, as well as Standard-Speed, Half-Power "L" versions (t_{PD} = 35 ns, I_{CC}* = 80 mA). Quarter-Power "Q" versions (t_{PD} = 35 ns, I_{CC} = 45 mA) are also available.

Please see the following pages for Block Diagrams.

*Combinatorial functions

Product Selector Guide

AMD PAL Speed/Power Families

Family	t_{PD} (2) ns (Max.)		t_S (1) ns (Min.)		t_{CO} (1) ns (Max.)		I_{CC} mA (Max.)	I_{OL} mA (Min.)	
	C Devices	M Devices	C Devices	M Devices	C Devices	M Devices	C/M Devices	C Devices	M Devices
Very High-Speed ("B") Versions	15	20	13	18	12	15	180	24	12
High-Speed ("A") Versions	25	30	20	25	15	20	180(1)/ 155(2)	24	12
High-Speed, Half-Power ("AL") Versions	25	30	20	25	15	20	90	24	12
Standard Versions	35	40	30	35	25	25	180(1)/ 155(2)	24	12
Half-Power ("L") Versions	35	40	30	35	25	25	90(1)/ 80(2)	24	12
Quarter-Power ("Q") Versions	35	40	30	35	25	25	45	12	8

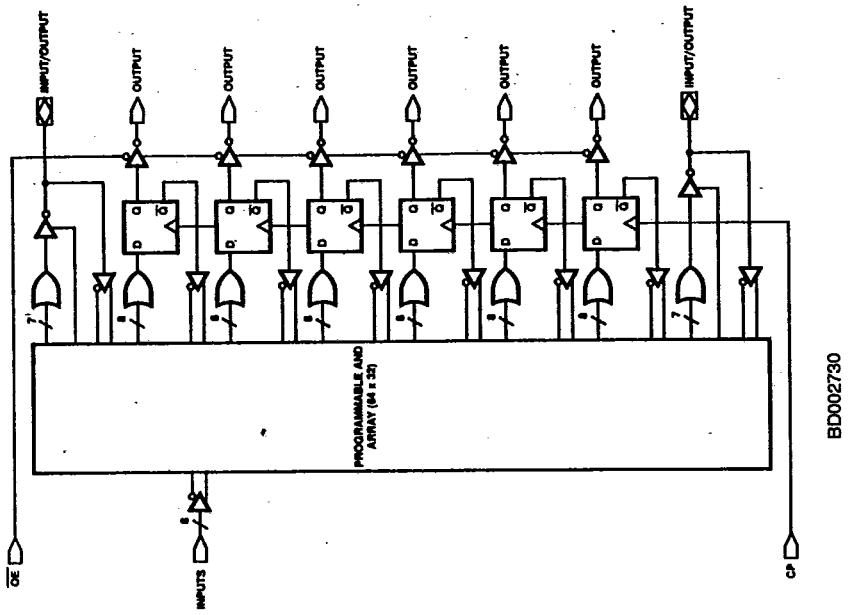
(1) Sequential functions
(2) Combinatorial functions

AMD PAL FUNCTIONS

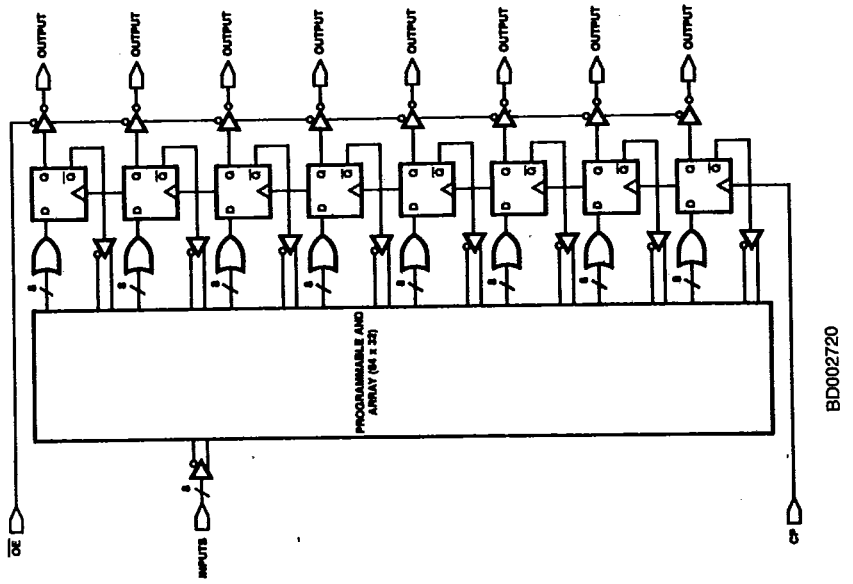
Part Number	Array Inputs	Logic	Output Enable	Outputs	Package Pins
16R8	Eight Dedicated, Eight Feedback	Eight 8-Wide AND-OR	Dedicated	Registered Inverting	20
16R6	Eight Dedicated, Six Feedback, Two Bidirectional	Six 8-Wide AND-OR	Dedicated	Registered Inverting	20
		Two 7-Wide AND-OR-INVERT	Programmable	Bidirectional	
16R4	Eight Dedicated, Four Feedback, Four Bidirectional	Four 8-wide AND-OR	Dedicated	Registered Inverting	20
		Four 7-Wide AND-OR-INVERT	Programmable	Bidirectional	
16L8	Ten Dedicated, Six Bidirectional	Eight 7-Wide AND-OR-INVERT	Programmable	Six Bidirectional Two Dedicated	20

Block Diagrams

AmPAL16R6



AmPAL16R8



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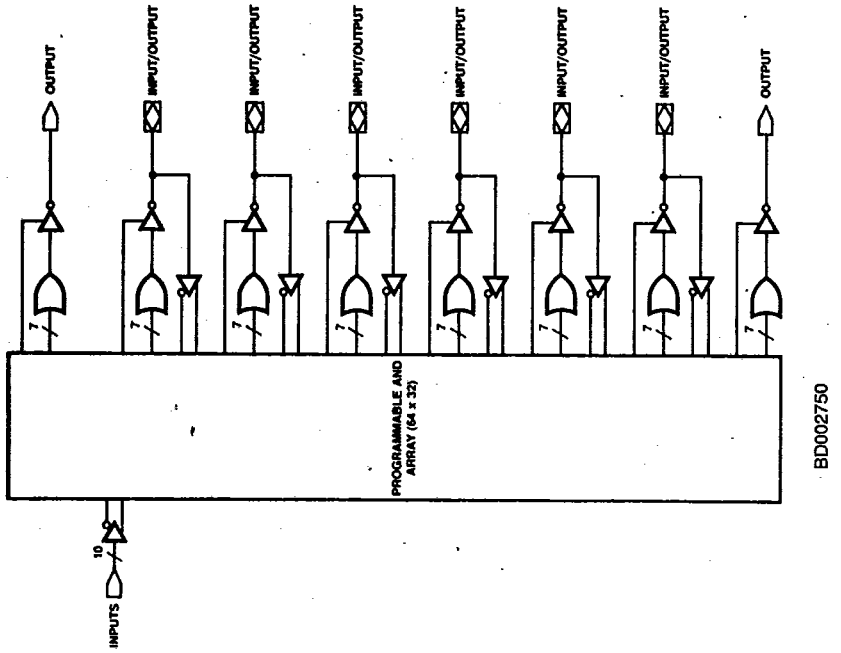
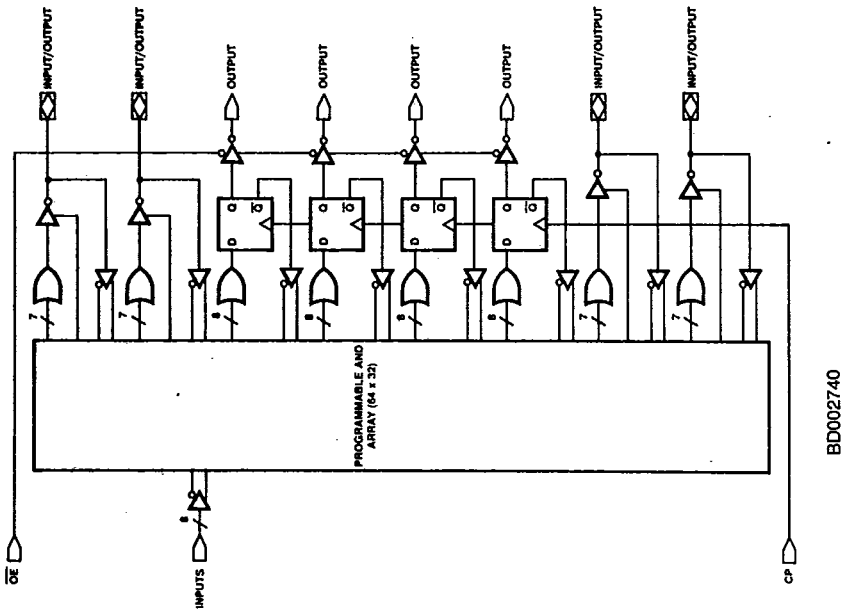
Block Diagrams (Cont'd.)

AmPAL16L8



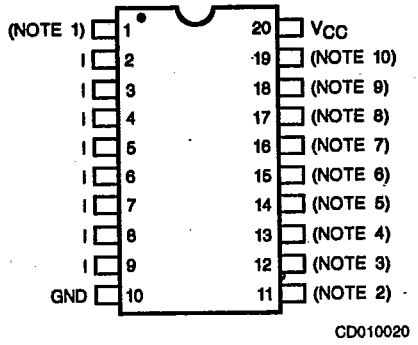
AmPAL16R4



Connection Diagrams

Top View

DIPs*



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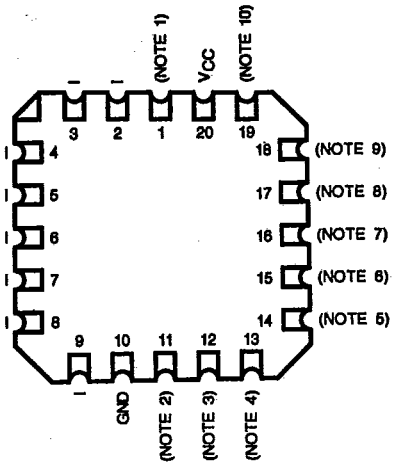
LCC**



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Note: Pin 1 is marked for orientation.

Notes:

	16L8	16R8	16R6	16R4
1	I	CLK	CLK	CLK
2	I	OE	OE	OE
3	O	O	I/O	I/O
4	I/O	O	O	I/O
5	I/O	O	O	O
6	I/O	O	O	O
7	I/O	O	O	O
8	I/O	O	O	O
9	I/O	O	O	I/O
10	O	O	I/O	I/O

*Also available in 20-Pin Ceramic Flatpack. Pinouts identical to DIPs.
**Also available in 20-Pin Plastic Leaded Chip Carrier. Pinouts identical to LCC.

Pin Designations

I = Input
I/O = Input/Output
O = Output
V_{CC} = Supply Voltage
GND = Ground
CLK = Clock
OE = Output Enable

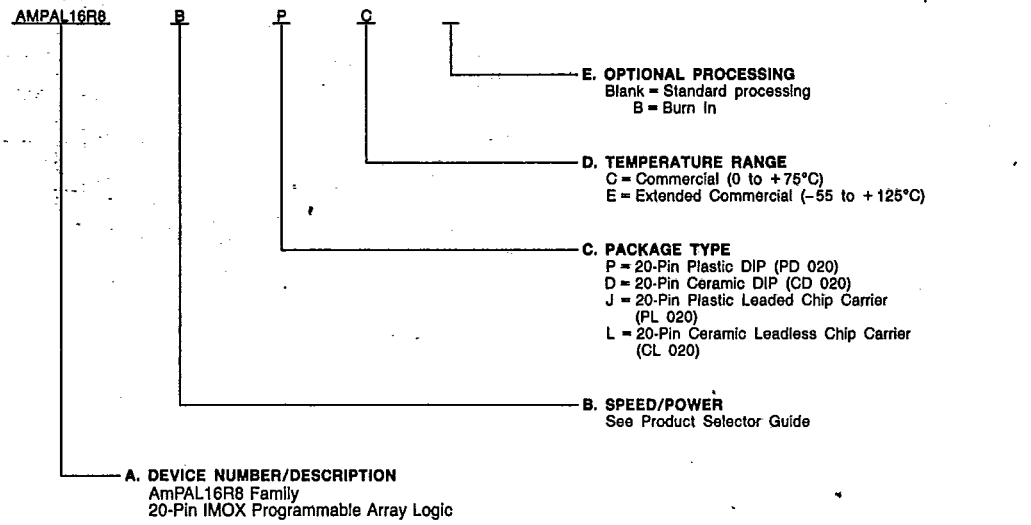
5

Ordering Information

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

A. Device Number
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AMPAL16R6/B/A/AL/L/Q	PC, DC, DCB, DE, JC, LC, LE
AMPAL16R6/B/A/AL/L/Q	
AMPAL16R4/B/A/AL/L/Q	
AMPAL16L8/B/A/AL/L/Q	

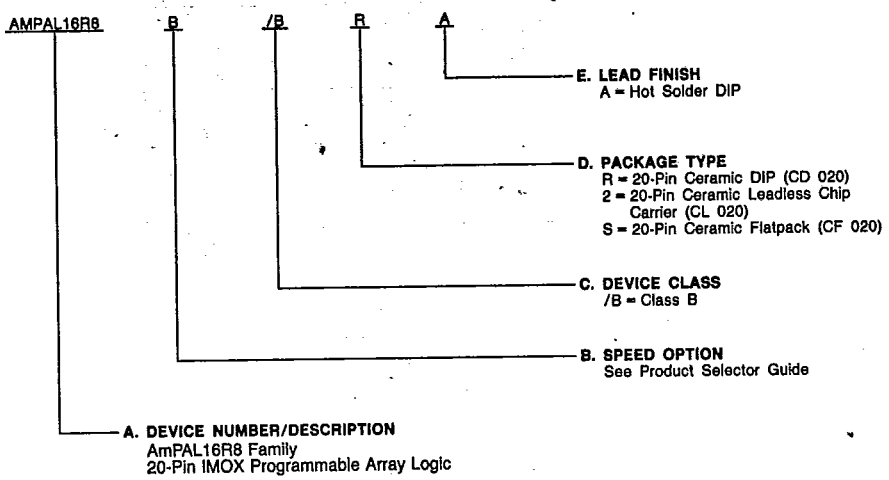
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Ordering Information (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AMPAL16R8/B/A/AL/L/Q	/BRA, /B2A, /BSA
AMPAL16R6/B/A/AL/L/Q	
AMPAL16R4/B/A/AL/L/Q	
AMPAL16L8/B/A/AL/L/Q	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 4, 9, 10, 11.

5

DESC Certified PAL Devices

Generic	AMD Part Number	DESC Numbers
16L8	AmPAL16L8A/BRA	8103607RX
	AmPAL16L8A/B2A	81036072X
	AmPAL16L8A/BSA	8103607SX
	AmPAL16L8L/BRA	8103611RX
	AmPAL16L8L/B2A	81036112X
	AmPAL16L8L/BSA	8103611SX
	AmPAL16L8/BRA	8103601RX
	AmPAL16L8/B2A	81036012X
16R8	AmPAL16R8A/BRA	8103608RX
	AmPAL16R8A/B2A	81036082X
	AmPAL16R8A/BSA	8103608SX
	AmPAL16R8L/BRA	8103612RX
	AmPAL16R8L/B2A	81036122X
	AmPAL16R8L/BSA	8103612SX
	AmPAL16R8/BRA	8103602RX
	AmPAL16R8/B2A	81036022X
16R6	AmPAL16R6A/BRA	8103609RX
	AmPAL16R6A/B2A	81036092X
	AmPAL16R6A/BSA	8103609SX
	AmPAL16R6L/BRA	8103613RX
	AmPAL16R6L/B2A	81036132X
	AmPAL16R6L/BSA	8103613SX
	AmPAL16R6/BRA	8103603RX
	AmPAL16R6/B2A	81036032X
16R4	AmPAL16R4A/BRA	8103610RX
	AmPAL16R4A/B2A	81036102X
	AmPAL16R4A/BSA	8103610SX
	AmPAL16R4L/BRA	8103614RX
	AmPAL16R4L/B2A	81036142X
	AmPAL16R4L/BSA	8103614SX
	AmPAL16R4/BRA	8103604RX
	AmPAL16R4/B2A	81036042X

Functional Description

AMD PAL Family Characteristics

All members of the AMD PAL Family have common electrical characteristics and programming procedures. All parts are produced with a fusible link at each input to the AND-gate array, and connections may be selectively removed by applying appropriate voltages to the circuit.

Initially the AND gates are connected, via fuses, to both the TRUE and complement of each input. By selective programming of fuses the AND gates may be "connected" to only the TRUE input (by blowing the complement fuse), to only the complement input (by blowing the TRUE fuse), or to neither type of input (by blowing both fuses) establishing a logical "don't care." When both the TRUE and complement fuses are left intact a logical FALSE results on the output of the AND gate, while all fuses blown results in a logical-TRUE state. The outputs of the AND gates are connected to fixed-OR gates. The only limitations imposed are the number of inputs to the AND gates (up to 16) and the number of AND gates per OR (up to 8).

All parts are fabricated with AMD's fast programming, highly reliable Platinum-Silicide Fuse technology. Utilizing an easily implemented programming algorithm, these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to ensure extremely high field programming yields (> 98%), and provide extra test paths to achieve excellent parametric correlation.

Power-Up RESET

The registered devices in the AMD PAL family have been designed to reset during system power-up. Following power-up, all registers will be initialized to zero, setting all the outputs to a logic 1. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization.

PRELOAD

AMD PAL devices are designed with unique PRELOAD circuitry that provides an easy method of testing registered devices for logical functionality. PRELOAD allows any arbitrary state value to be loaded into the registered output of an AMD PAL device.

A typical functional test sequence would be to verify all possible state transitions for the device being tested. This requires the ability to set the state registers into an arbitrary "present state" value and to set the device inputs to any arbitrary "present input" value. Once this is done, the state machine is clocked into a new state or "next state." The next state is then checked to validate the transition from the present state. In this way any state transition can be checked.

Security Fuse

An additional fuse is provided on each AMD PAL circuit to prevent unauthorized copying of AMD PAL device fuse patterns when design security is desired. Blowing the security fuse blocks entry to the fuse pattern verify mode.

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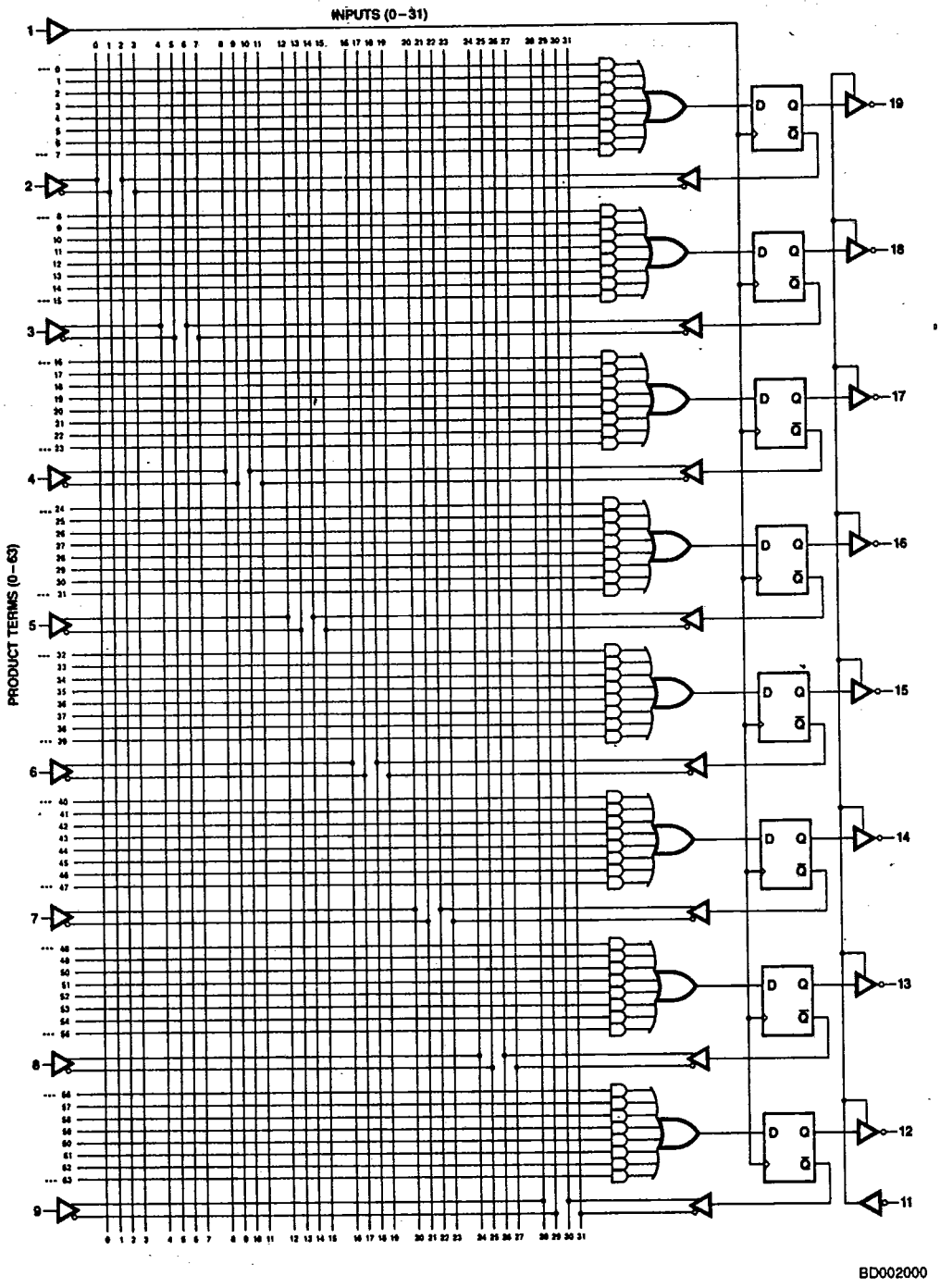


Figure 1. AmPAL16R8 Logic Diagram

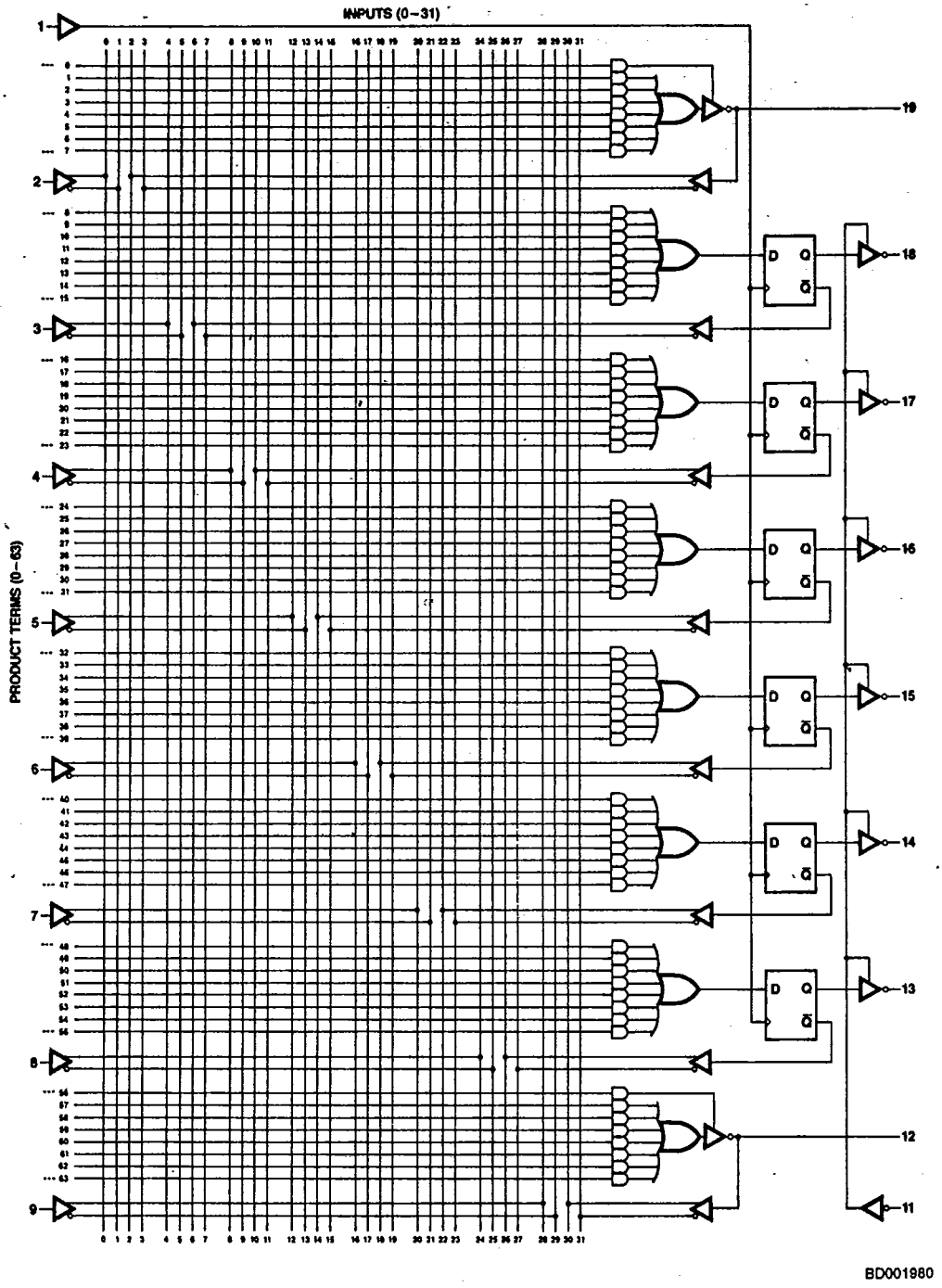


Figure 2. AmPAL16R6 Logic Diagram

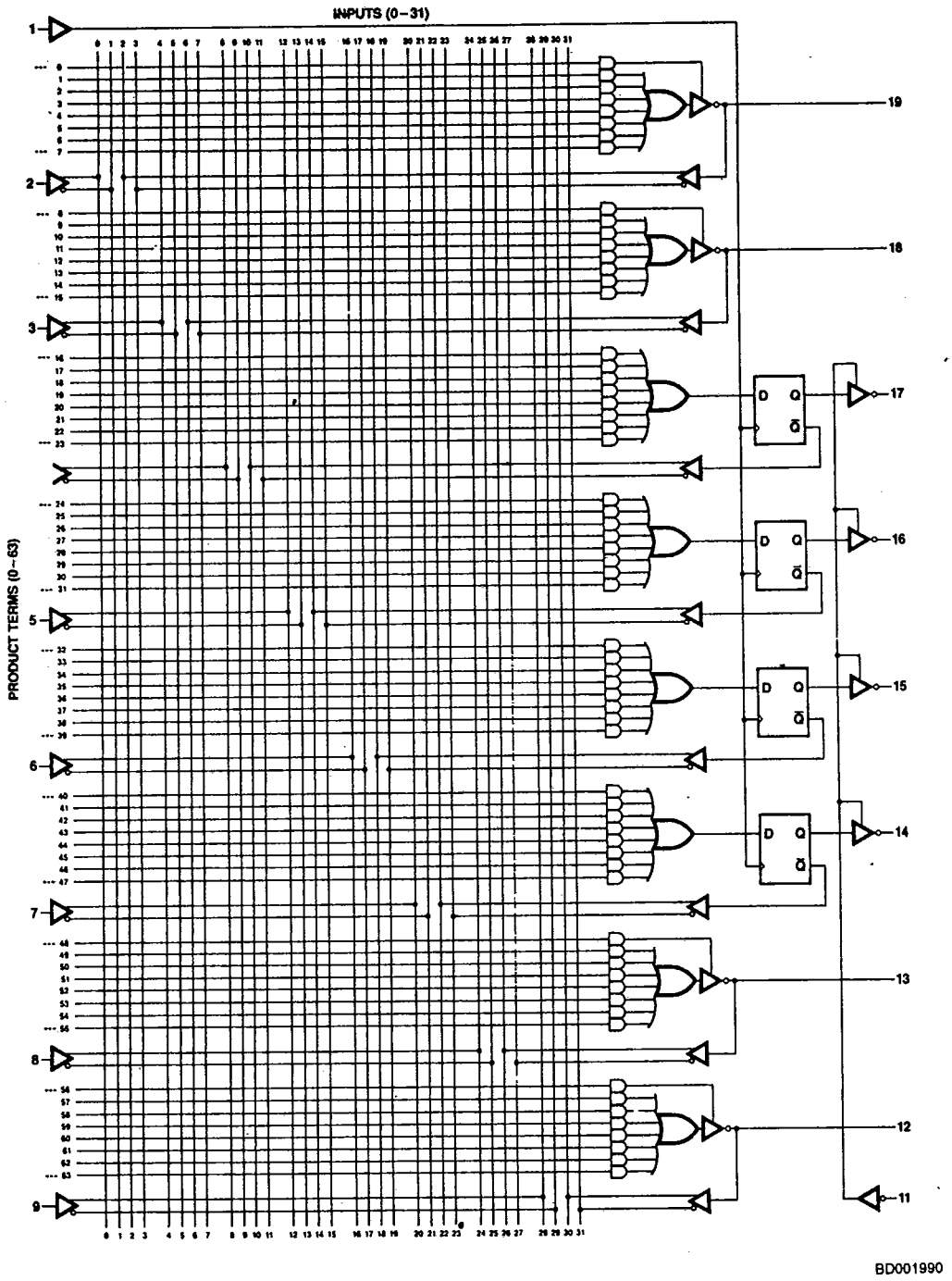


Figure 3. AmPAL16R4 Logic Diagram

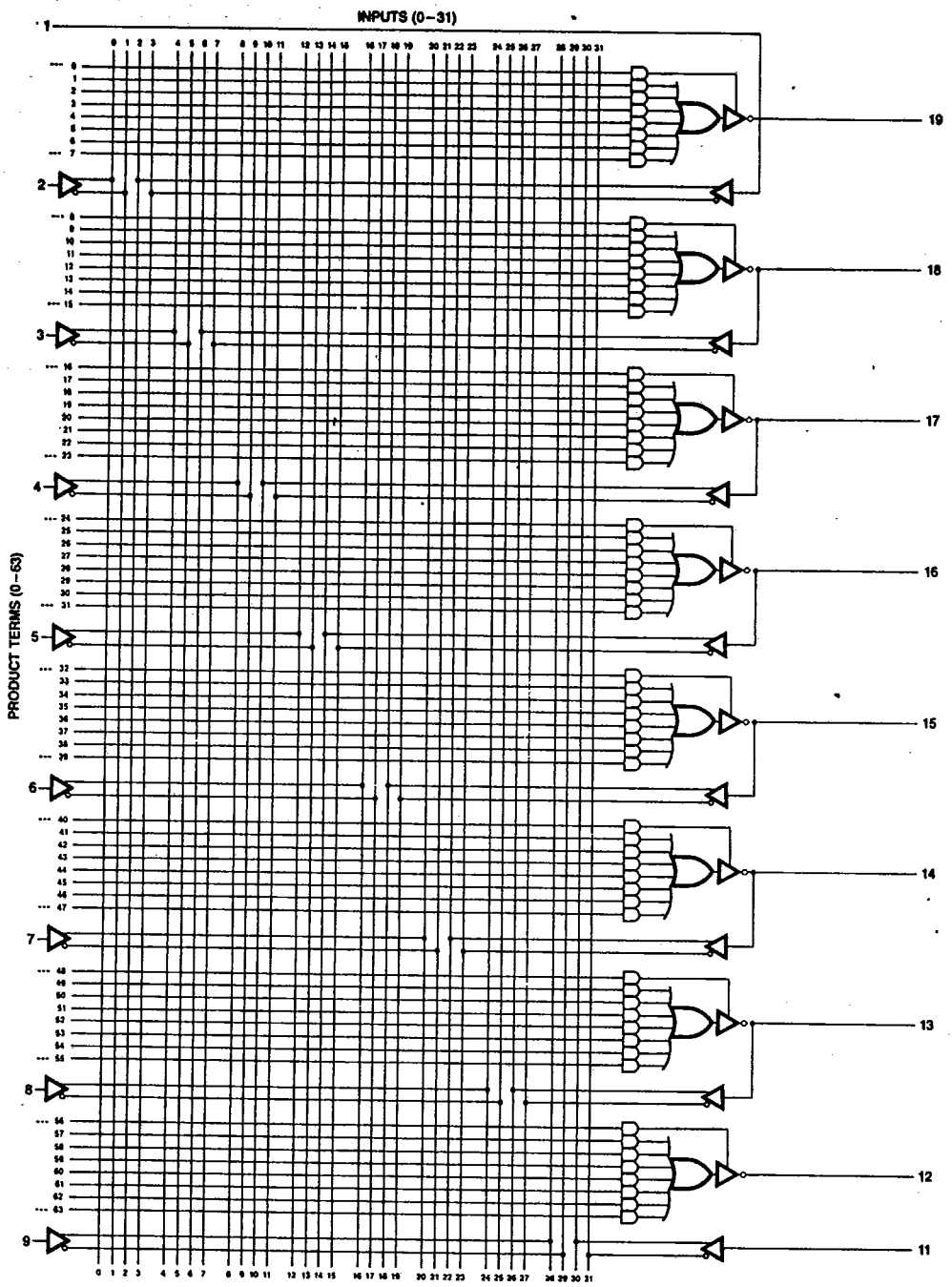


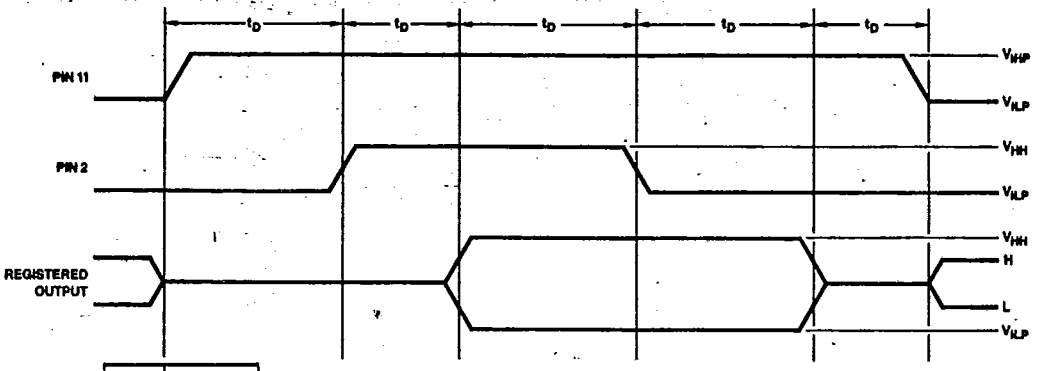
Figure 4. AmPAL16L8 Logic Diagram

Applications

PRELOAD of Registered Outputs

AMD PAL registered outputs are designed with extra circuitry to allow loading each register asynchronously to either a HIGH or LOW state. This feature simplifies testing since any initial state for the registers can be set to optimize test sequencing.

The pin levels and timing necessary to perform the PRELOAD function are detailed below:



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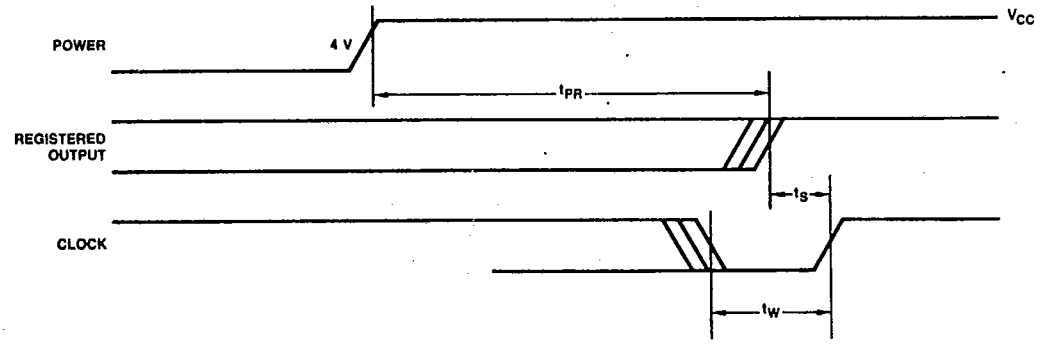
Par.	Min.	Max.
V_{HH}	10	12
V_{ILP}	0	0.5
V_{IHP}	2.4	5.5
V_{CCH}	5.4	6.0

Level forced on registered output pin during PRELOAD cycle	State of the output pin after cycle
V_{HH}	HIGH
0 V to V_{CCH} or OPEN	LOW

Power-Up Reset

The registered devices in the AMD PAL Family have been designed to reset during system power-up. Due to the asynchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from low to high until all applicable input and feedback setup times are met.



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Parameters	Description	Min.	Typ.	Max.	Units
t_{PR}	Power-Up Reset Time		600	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics			
t_W	Clock Width				

Absolute Maximum Ratings

Storage Temperature ..... −65 to +150°C
Supply Voltage to Ground Potential
(Pin 20 to Pin 10) Continuous ..... −0.5 to +7.0 V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5 V to +V_{CC} Max.
DC Voltage Applied to Outputs
During Programming ..... 21 V
Output Current Into Outputs During
Programming (Max Duration of 1 sec) ..... 200 mA
DC Input Voltage ..... −0.5 to +5.5 V
DC Input Current ..... −30 to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Operating Ranges

Commercial (C) Devices
Temperature (T_A) ..... 0 to +75°C
Supply Voltage (V_{CC}) ..... +4.75 to +5.25 V

Extended Commercial (E) Devices
Temperature (T_A) ..... −55°C Min.
Temperature (T_C) ..... +125°C Max.
Supply Voltage (V_{CC}) ..... +4.50 to +5.50 V

Military (M) Devices*
Temperature (T_A) ..... −55°C Min.
Temperature (T_C) ..... +125°C Max.
Supply Voltage (V_{CC}) ..... +4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military product 100% tested at T_C = +25°C, +125°C, and −55°C.

DC Characteristics

over operating range unless otherwise specified; included in Group A, Subgroup 1, 2, 3, 4 tests unless otherwise noted

Parameter Symbol	Parameter Description	Test Conditions				Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	"Q"	I_{OH} = −2 mA	COM'L	2.4	3.5		V
			All others	I_{OH} = −3.2 mA	COM'L				
				I_{OH} = −2 mA	MIL				
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	"B," "A," "Std." "AL," & "L"	I_{OL} = 24 mA	COM'L			0.5	V
				I_{OL} = 12 mA	MIL				
			"Q"	I_{OL} = 12 mA	COM'L				
				I_{OL} = 8 mA	MIL				
V_{IH} (Note 2)	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs				2.0		5.5	V
V_{IL} (Note 2)	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs						0.8	V
I_{IL}	Input LOW Current	V_{CC} = Max., I_{IN} = 0.40 V		"B," "AL," & "Q"			−20	−100	μA
				"A," "L," & "Std."			−20	−250	
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7 V						25	μA
I_I	Input HIGH Current	V_{CC} = Max., V_{IN} = 5.5 V						1.0	mA
I_{SC}	Output Short-Circuit Current	V_{CC} = Max., V_{OUT} = 0.5 V (Note 3)				−30	−60	−90	mA
I_{CC}	Power Supply Current	All Inputs = GND, V_{CC} = Max.		16L8A, 16L8,			110	155	mA
				16L8L,			55	80	
				16R8B, 16R6B, 16R4B, 16L8B, 16R8A, 16R6A, 16R4A, 16R8, 16R6, 16R4				180	
				16R8L, 16R6L, 16R4L, 16L8AL, 16R8AL, 16R6AL, 16R4AL			60	90	
				16L8Q, 16R8Q, 16R6Q, 16R4Q				45	
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA					−0.9	−1.2	V
I_{OZH}	Output Leakage Current (Note 4)	Vcc = Max., V_{IN} = V_{IL} or V_{IH}		V_O = 2.7 V				100	μA
I_{OZL}				V_O = 0.4 V				−100	
C_{IN}	Input Capacitance	V_{IN} = 2.0 V @ f = 1 MHz (Note 5)					6		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V @ f = 1 MHz (Note 5)					9		

Notes: 1. Typical limits are at V_{CC} = 5.0 V and T_A = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
4. I/O pin leakage is the worst case of I_{OZX} or I_{IX} (where X = H or L).
5. These parameters are not 100% tested, but are periodically sampled.

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Switching Characteristics

over operating range unless otherwise specified; included in Group A, Subgroup 9, 10, 11 tests unless otherwise noted

Commercial Range

No.	Parameter Symbol	Parameter Description	"B" Version			"A" & "AL" Version			"Std," "L" & "Q" Versions			Units
			Min.	Typ. (Note 1)	Max.	Min.	Typ. (Note 1)	Max.	Min.	Typ. (Note 1)	Max.	
1	t_{PD}	Input or Feedback to Non-Registered Output 16L8, 16R6, 16R4,		12	15		17	25		23	35	ns
2	t_{EA}	Input to Output Enable 16L8, 16R6, 16R4, 16H8		12	15		17	25		23	35	ns
3	t_{ER}	Input to Output Disable 16L8, 16R6, 16R4, 16H8		12	15		17	25		23	35	ns
4	t_{PZX}	Pin 11 to Output Enable 16R8, 16R6, 16R4		8	15		12	20		17	25	ns
5	t_{PXZ}	Pin 11 to Output Disable 16R8, 16R6, 16R4		8	15		12	20		17	25	ns
6	t_{CO}	Clock to Output 16R8, 16R6, 16R4		8	12		12	15		17	25	ns
7	t_S	Input or Feedback Setup Time 16R8, 16R6, 16R4	13	10		20	15		30	20		ns
8	t_H	Hold Time 16R8, 16R6, 16R4	0	−8		0	−10		0	−10		ns
9	t_P	Clock Period ($t_S + t_{CO}$)	25			35			55			ns
10	t_W	Clock Width	10			15			25			ns
11	$f_{MAX.}$	Maximum Frequency			40			28.5			18	MHz

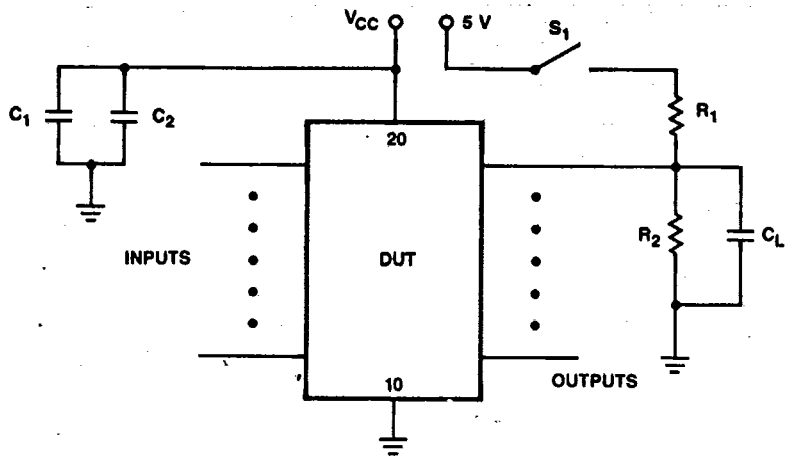
Notes: 1. Typical limits are at $V_{CC} = 5.0$ V and $T_A = 25°C$.
2. t_{PD} is tested with switch S_1 closed and $C_L = 50$ pF.
3. For three-state outputs, output enable times are tested with $C_L = 50$ pF to the 1.5 V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. Output disable times are tested with $C_L = 5$ pF. HIGH to high impedance tests are made to an output voltage of $V_{OH} - 0.5$ V with S_1 open; LOW to high impedance tests are made to the $V_{OL} + 0.5$ V level with S_1 closed.

Military Range

No.	Parameter Symbol	Parameter Description	"B" Version			"A" & "AL" Version			"Std," "L" & "Q" Versions			Units
			Min.	Typ. (Note 1)	Max.	Min.	Typ. (Note 1)	Max.	Min.	Typ. (Note 1)	Max.	
1	t_{PD}	Input or Feedback to Non-Registered Output 16L8, 16R6, 16R4,		12	20		17	30		23	40	ns
2	t_{EA}	Input to Output Enable 16L8, 16R6, 16R4, 16H8		12	20		17	30		23	40	ns
3	t_{ER}	Input to Output Disable 16L8, 16R6, 16R4, 16H8		12	20		17	30		23	40	ns
4	t_{PZX}	Pin 11 to Output Enable 16R8, 16R6, 16R4		8	20		12	25	STD L / Q	17	25 / 30	ns
5	t_{PXZ}	Pin 11 to Output Disable 16R8, 16R6, 16R4		8	20		12	25	STD L / Q	17	25 / 30	ns
6	t_{CO}	Clock to Output 16R8, 16R6, 16R4		8	15		12	20		17	25	ns
7	t_S	Input or Feedback Setup Time 16R8, 16R6, 16R4	18	10		25	15		35	20		ns
8	t_H	Hold Time 16R8, 16R6, 16R4	0	−8		0	−10		0	−10		ns
9	t_P	Clock Period ($t_S + t_{CO}$)	33			45			60			ns
10	t_W	Clock Width	12			20			25			ns
11	$f_{MAX.}$	Maximum Frequency			30			22			16.5	MHz

Notes: 1. Typical limits are at $V_{CC} = 5.0$ V and $T_A = 25°C$.
2. t_{PD} is tested with switch S_1 closed and $C_L = 50$ pF.
3. For three-state outputs, output enable times are tested with $C_L = 50$ pF to the 1.5 V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. Output disable times are tested with $C_L = 5$ pF. HIGH to high impedance tests are made to an output voltage of $V_{OH} - 0.5$ V with S_1 open; LOW to high impedance tests are made to the $V_{OL} + 0.5$ V level with S_1 closed.

Switching Test Circuit



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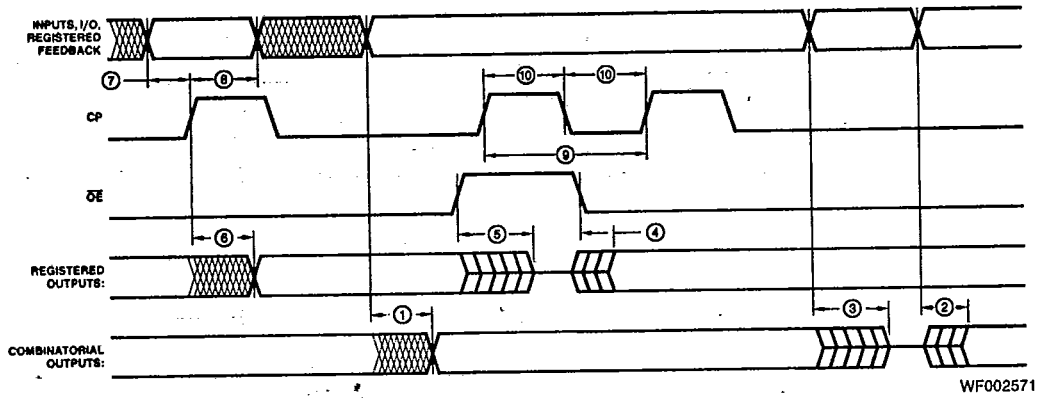
Note: C_1 and C_2 are to bypass V_{CC} to ground.

TEST OUTPUT LOADS				
	"Std," "B," "A," "AL" & "L"		"Q"	
Name	Commercial	Military	Commercial	Military
R_1	200 Ω	390 Ω	390 Ω	600 Ω
R_2	390 Ω	750 Ω	750 Ω	1200 Ω
C_1	1 μF	1 μF	1 μF	1 μF
C_2	0.1 μF	0.1 μF	0.1 μF	0.1 μF
C_L	50 pF	50 pF	50 pF	50 pF

5

Switching Waveforms



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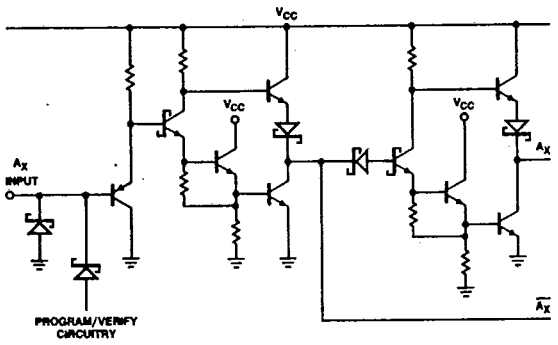
Key to Timing Diagram

WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
———		
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING, STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010

Input Circuitry



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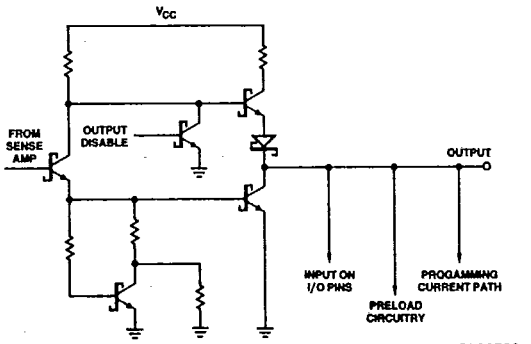
Output Circuitry



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Programmers/Development Systems

(refer to Programmer Reference Guide, page 3-81)