ESS Technology, Inc.

ES1869
*Audio*Drive® Solution
Data Sheet

DESCRIPTION

The ES1869 *Audio***Drive**® solution is a mixed-signal single chip that adds 16-bit stereo sound and FM music synthesis to personal computers. It is compliant with the Microsoft® PC 97 and PC 98 specification and WHQL audio requirements. The ES1869 possesses an embedded microcontroller, OPL3™ superset **ESFM**™ music synthesizer, 16-bit stereo wave ADC and DAC, 16-bit stereo music DAC, MPU-401 UART serial port, dual game port, full Plug and Play support, CD-ROM IDE interface, hardware master volume control, two serial port interfaces to external DSP and external wavetable music synthesizer, I²S Zoom Video interface, DMA control logic with FIFO, and ISA bus interface logic. There are three stereo inputs (typically line, CD audio, and auxiliary line) and a mono microphone input. All of this on a single chip that can be designed into a motherboard, add-on card, or integrated into other peripheral cards such as Fax/Modem, VGA, LAN, I/O, etc.

The ES1869 *Audio***Drive**® solution can record, compress, and play back voice, sound, and music with built-in mixer controls. It supports full-duplex operation for simultaneous record and playback using two DMA channels. The **ESFM**™ synthesizer has extended capabilities within native mode operation providing superior sound and power-down capabilities. It is a register compatible superset of the OPL3 FM synthesizer.

The ES1869 *Audio***Drive**® solution supports the full ISA Plug and Play standard. It provides Plug and Play configuration for logical devices: audio, **ESFM**™ synthesizer, game port, MPU-401, CD-ROM IDE, Modem, and an additional user-defined device.

The MPU-401 serial port is for interfacing to an external MIDI device.

The integrated 3-D audio effects processor uses technology from *Spatializer*® Audio Laboratories, Inc. and expands the sound field emitted by two speakers to create a resonant 3-D sound environment.

The speakerphone application can be implemented either by digital interface through the DSP serial port, or by analog interface through Mono-In and Mono-Out.

A DSP serial interface in the ES1869 allows an external DSP to take over ADC or DAC resources.

The ES1869 *Audio***Drive**® solution supports telegaming architecture with headsets and includes data paths for host-based Acoustic Echo Cancellation processing.

Advanced power management features include suspend/resume from disk or host-independent self-timed power-down and automatic wake-up. The ES1869 is compliant to the ACPI standard.

It is available in an industry-standard 100-pin Plastic Quad Flat Pack (PQFP) and Thin Quad Flat Pack (TQFP) packages.

FEATURES

- Single, high-performance, mixed-signal, 16-bit stereo VLSI chip
- High-quality, OPL3 superset **ESFM**™ music synthesizer
- IDE CD-ROM interface
- High-performance DMA supports Demand Transfer and F-type
- Integrated *Spatializer*® 3-D audio effects processor

Plug and Play Features

- On-chip Plug and Play support for audio, joystick port, FM, Modem, MPU-401, CD-ROM, and a user-defined I/O device
- Software address mapping with software chip select, plus 4 DMA and 6 IRQ selections for motherboard implementation
- Internal configuration data for audio Plug and Play support
- Serial interface for Plug and Play resource EEPROM

Record and Playback Features

- Record, compress, and play back voice, sound, and music
- 16-bit stereo ADC and DAC
- Programmable independent sample rates from 4 kHz to 48.0 kHz for record and playback
- Full-Duplex operation for simultaneous record and playback
- 2- and 3-button hardware volume control for up, down, and mute

Inputs and Outputs

- Stereo inputs for line-in, auxiliary A (CD audio), and auxiliary B, and a mono input for microphone
- MPU-401 (UART mode) interface for wavetable synthesizers and MIDI devices
- Integrated dual game port

- I²S Zoom Video port interface with a sample rate up to 48 kHz for MPEG audio
- Serial port interface to external DSP (e.g. AT&T, TI, API, and MWAVE)
- Separate mono input (MONO_IN) and mono output (MONO_OUT_) for telegaming

Mixer Features

- 7-channel mixer with stereo inputs for line, CD audio, auxiliary line, music synthesizer, digital audio (wave files), and mono inputs for microphone and speakerphone
- Programmable 6-bit logarithmic master volume control

Power

- Advanced power management with self-timed power-down, automatic wake-up, and suspend/resume to and from disk
- Supports 3.3 V or 5.0 V operation

Compatibility

- Supports PC games and applications for Sound Blaster™ and Sound Blaster™ Pro
- Supports Microsoft Windows™ Sound System®
- Meets PC 97 and PC 98 and WHQL specifications

Operating Systems

- Microsoft Windows®95 and Windows®98
- Microsoft Windows™ 3.1 and Windows for Workgroups™
- Windows Sound System
- Microsoft Windows NT™ 4.0
- IBM® OS/2® Warp™

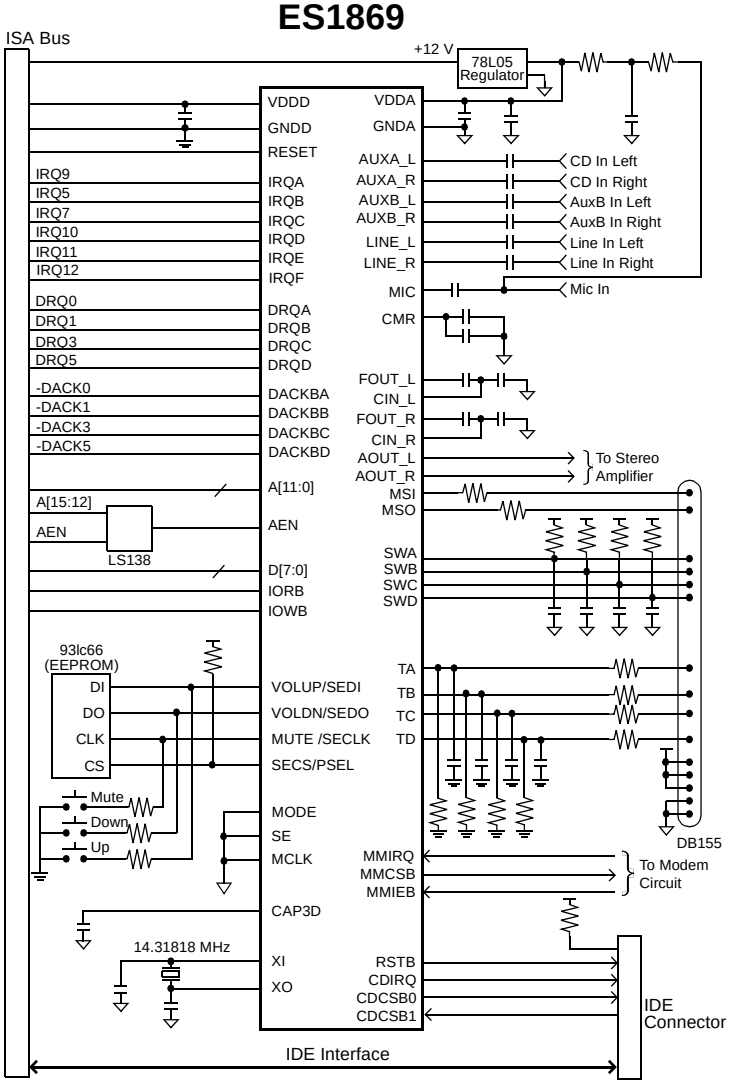

Figure 1 Typical Application

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FIGURES

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PINOUT

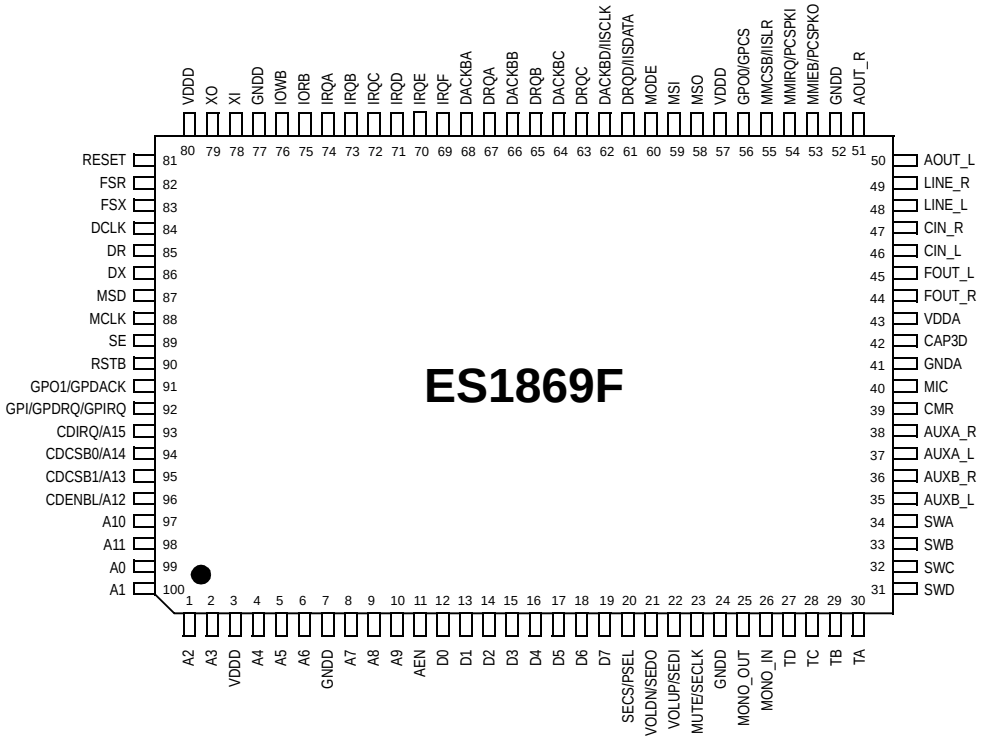


Figure 2 ES1869F Pinout (PQFP Package)

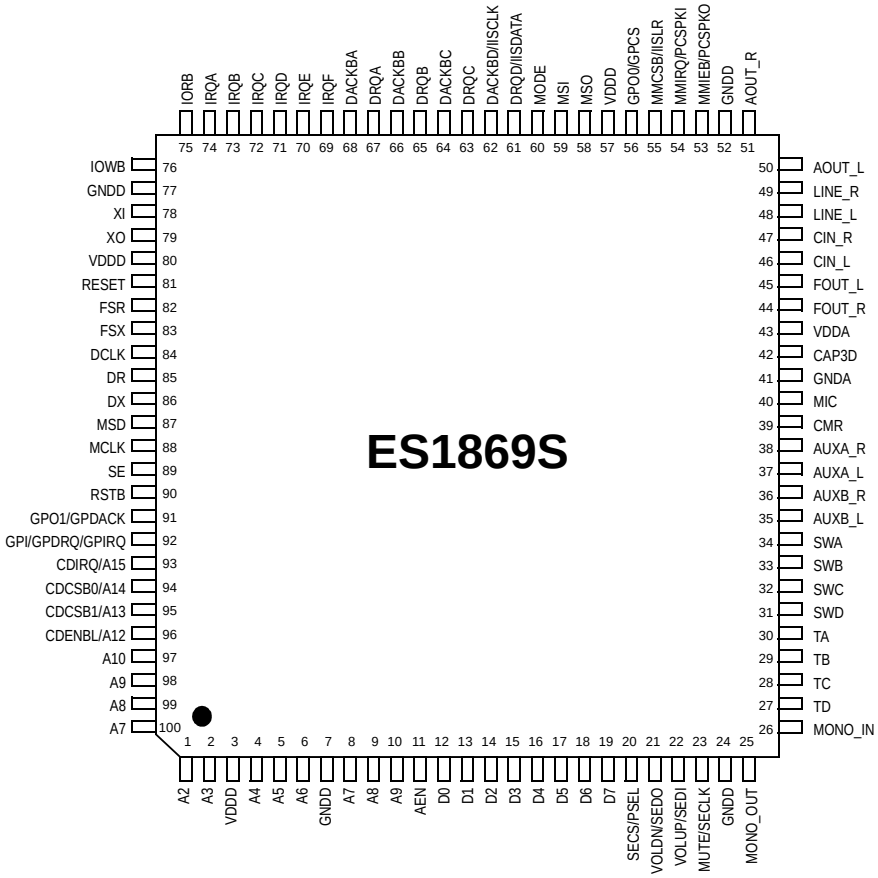


Figure 3 ES1869S Pinout (TQFP Package)

PIN DESCRIPTION

Name	Number	I/O	Description
A[11:0]	99,100,1,2,6:4, 10:8,97,98	I	Address inputs from the ISA bus.
VDDD	3,57,80	I	Digital supply voltage (4.5 to 5.5 V).
GNDD	7,24,52,77	I	Digital ground.
AEN	11	I	Active-low address enable from the ISA bus.
D[7:0]	19:12	I/O	ISA bidirectional data bus.
PSEL	20	I	Selects the PnP ROM device used: 0 Internal ROM 1 93LC66 – 512 x 8, 9 address bits
SECS		I/O	Serial EEPROM CS. This is an input pin during RESET.
SEDO	21	I	Input connected to the data output pin of the external PnP serial EEPROM.
VOLDN		I	Active-low volume decrease button input with internal pull-up (shared with the SEDO pin).
SEDI	22	O	Output connected to the data input pin of the external PnP serial EEPROM.
VOLUP		I	Active-low volume increase button input with internal pull-up (shared with the SEDI pin).
MUTE	23	I	Active-low mute toggle button input with internal pull-up (shared with the SECLK pin).
SECLK		O	External serial EEPROM clock output for PnP.
MONO_OUT	25	O	Mono output with source select and volume control (including mute). This pin can drive an external 5k ohm AC load.
MONO_IN	26	I	Mono input to mixer and ADC. This pin has an internal pull-up to CMR.
T(A-D)	27:30	I/O	Joystick timer pins. These pins connect to the X-Y positioning variable resistors for the two joysticks.
SW(A-D)	31:34	I	Active-low joystick switch setting inputs. These pins have an internal pull-up resistor. The joystick port is typically at address 201h.
AUXB_L	35	I	Auxiliary B input left. AUXB_L has an internal pull-up resistor to CMR. Normally intended for connection to an external music synthesizer or other line-level source.
AUXB_R	36	I	Auxiliary B input right. AUXB_R has an internal pull-up resistor to CMR. Normally intended for connection to an external music synthesizer or other line-level source.
AUXA_L	37	I	Auxiliary A input left. AUXA_L has an internal pull-up resistor to CMR. Normally intended for connection to an internal or external CD-ROM analog output.
AUXA_R	38	I	Auxiliary A input right. AUXA_R has an internal pull-up resistor to CMR. Normally intended for connection to an internal or external CD-ROM analog output.
CMR	39	O	Common mode buffered reference output (2.25 V ± 5%). This pin should be bypassed to analog ground with a 47 µF electrolytic capacitor with a 0.1 µF capacitor in parallel.
MIC	40	I	Microphone input. MIC has an internal pull-up resistor to CMR.
GNDA	41	I	Analog ground.
CAP3D	42	I	Bypass capacitor to analog ground for 3-D effect.
VDDA	43	I	Analog supply voltage (4.5 to 5.5 V). Must be greater than or equal to VDDD - 0.3 V.
FOUT_R	44	O	Filter output right. FOUT_R is AC-coupled externally to CIN_R to remove DC offsets. This output has an internal series resistor of about 5k ohms. A capacitor to analog ground on this pin can be used to create a low-pass filter pole that removes the switching noise introduced by the switched-capacitor filter.

Name	Number	I/O	Description
FOUT_L	45	O	Filter output left. FOUT_L is AC-coupled externally to CIN_L to remove DC offsets. This output has an internal series resistor of about 5k ohms. A capacitor to analog ground on this pin can be used to create a low-pass filter pole that removes the switching noise introduced by the switched-capacitor filter.
CIN_L	46	I	Capacitive coupled input left. CIN_L has an internal pull-up resistor to CMR of approximately 50k ohms.
CIN_R	47	I	Capacitive coupled input right. CIN_R has an internal pull-up resistor to CMR of approximately 50k ohms.
LINE_L	48	I	Line input left. LINE_L has an internal pull-up resistor to CMR.
LINE_R	49	I	Line input right. LINE_R has an internal pull-up resistor to CMR.
AOUT_L	50	O	Line-level stereo output left. AOUT_L can drive a 10k ohm load.
AOUT_R	51	O	Line-level stereo output right. AOUT_R can drive a 10k ohm load.
MMIEB [0]	52	I	Modem interrupt enable active-low input. Generated from the modem UART.
PCSKPO [1]		O	PC speaker analog output.
MMIRQ [0]	53	I	Modem interrupt request active-high input. IRQ input from the modem device gets mapped to an IRQ output on the ES1869 based on the PnP configuration.
PCSPKI [1]		I	Normally low digital PC speaker input. This signal is converted to an analog signal with volume control and appears on analog output PCSPKO.
IISLR [1]	55	I	Left/right strobe for I²S interface. This pin has a pull-down.
MMCSB [0]		O	Output from ES1869 for the modem CSB. The address space is determined by the PnP configuration.
GPCS	56	O	If selected by the PnP logic, GPCS is an active-high user-defined chip select for an external general-purpose device.
GPO0		O	Output that is set low by external reset and is thereafter controlled by bit 0 of port Audio_Base+7h. Available to system software for power management or other applications.
MSO	58	O	MIDI serial data output.
MSI	59	I	MIDI serial data input. Schmitt trigger input with internal pull-up resistor. Either MPU-401 or Sound Blaster formats.
MODE	60	I	Mode function pin. Connect to either GNDD or VDDD to select the function of the groups of multiple function pins (indicated by a superscript 0 or 1).
DRQD [0]	61	O	Tri-state output. Optional 16-bit DMA request for IDE interface.
IISDATA [1]		I	Serial data for I²S interface. This pin has a pull-down.
DACKBD [0]	62	I	Optional 16-bit DMA acknowledge for IDE interface.
IISCLK [1]		I	Serial shift clock for I²S interface. This pin has a pull-down.
DRQ(A-C)	75,65,63	O	Three (A,B,C) active-high DMA requests to the ISA bus. Unselected DRQ outputs are high impedance. When DMA is not active, the selected DRQ output has a pull-down device that holds the DRQ line inactive unless another device that shares the same DRQ line can source enough current to make the DRQ line active. DRQs are software configurable.
DACKB(A-C)	68,66,64	I	Three (A,B,C) active-low DMA acknowledge inputs.
IRQ(A-F)	69:74	O	Six (A,B,C,D,E,F) active-high interrupt requests to the ISA bus. Unselected IRQ outputs are high impedance. IRQs are software configurable.
IORB	75	I	Active-low read strobe from the ISA bus.
IOWB	76	I	Active-low write strobe from the ISA bus.
XI	78	I	Crystal oscillator/external clock input. Connect to external 14.318 MHz crystal or clock source with CMOS levels.

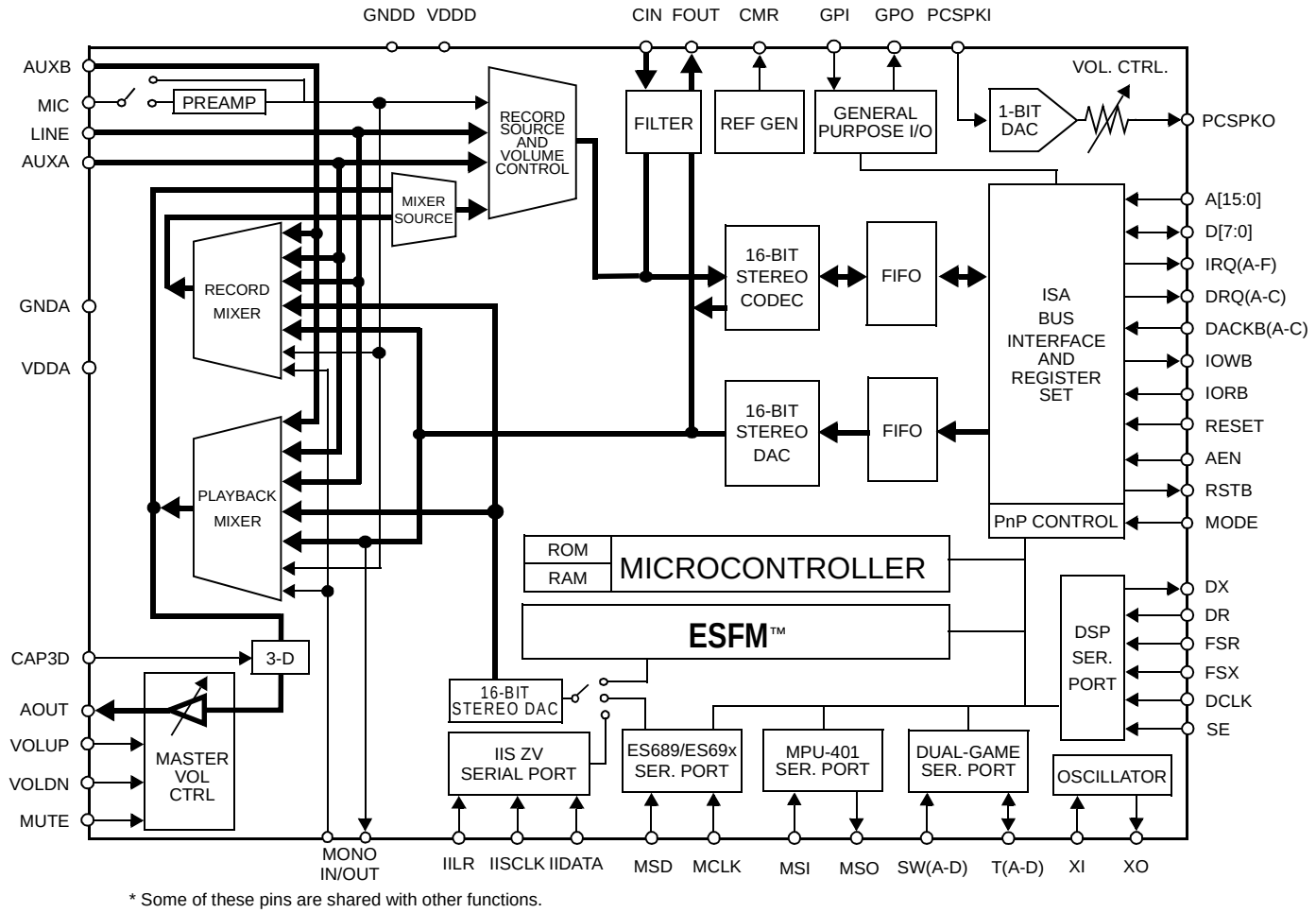
Name	Number	I/O	Description
XO	79	O	Crystal oscillator output. Connect to external 14.318 MHz crystal.
RESET	81	I	Active-high reset from the ISA bus.
FSR	82	I	Input with internal pull-down. Frame sync for receive data from external DSP. Programmable for active-high or active-low.
FSX	83	I	Input with internal pull-down. Frame sync for transmit request from external DSP. Programmable for active-high or active-low.
DCLK	84	I	Input with internal pull-down. Serial data clock from external DSP. Typically 2.048 MHz.
DR	85	I	Input with internal pull-down. Data receive pin from external DSP.
DX	86	O	Tri-state output. Data transmit to external DSP. High impedance when not transmitting.
MSD	87	I	Input with internal pull-down. Music serial data from external ES689/ES69x wavetable music synthesizer.
MCLK	88	I	Input with internal pull-down. Music serial clock from external ES689/ES69x wavetable music synthesizer.
SE	89	I	Input with internal pull-down. Active-high to enable serial mode, that is, it enables an external DSP to control analog resources of the ES1869 through the DSP serial interface. This pin is logically OR'd internally with bit 7 of mixer register 48h.
RSTB	90	O	Inverted RESET output.
GPDACK	91	O	Active-low DMA acknowledge output to general-purpose device that uses DMA.
GPO1		O	Output that is set high by external reset and thereafter controlled by bit 1 of port Audio_Base+7h. Available to system software for power management or other applications.
GPDRQ	92	I	DMA request output from general-purpose device based on the PnP configuration.
GPI		I	General-purpose input option.
GPIRQ		I	Interrupt request output from the general-purpose device based on the PnP configuration.
A15 [1]	93	I	Address input from the ISA bus.
CDIRQ [0]		I	Interrupt request input from the IDE interface.
A14 [1]	94	I	Address input from the ISA bus.
CDCSB0 [0]		O	Active-low IDE interface chip select #0.
A13 [1]	95	I	Address input from the ISA bus.
CDCSB1 [0]		O	Active-low IDE interface chip select #1.
A12 [1]	96	I	Address input from the ISA bus.
CDENBL [0]		O	Active-low IDE data bus transceiver enable.

0: Pins enabled by MODE = 0 (pin 60).
1: Pins enabled by MODE = 1 (pin 60).

FUNCTIONAL DESCRIPTION

This section shows the overall structure of the ES1869 and discusses its major functional subunits.

The major subunits of the ES1869 are shown in Figure 4 and described briefly in the following paragraphs.



* Some of these pins are shared with other functions.

Figure 4 ES1869 Block Diagram

Digital Subsystems

- **RISC microcontroller** – game-compatible audio functions are performed by an embedded microcontroller.
- **Oscillator** – circuitry to support an external crystal.
- **ROM and RAM** – firmware ROM and data RAM to the embedded microcontroller.
- **FIFO** – RAM for a 256-byte FIFO data buffer for use with the first audio channel and RAM for a 64-byte FIFO data buffer for use with the second audio channel.
- **ISA bus interface** – provides interface to ISA bus address, data, and control signals.
- **Dual game port** – integrated dual game port for two joysticks.
- **MPU-401 serial port** – asynchronous serial port for MIDI devices such as a wavetable synthesizer or a music keyboard input.
- **Wavetable serial port** – serial port connection from the output of an ES689 or ES69x that eliminates the requirements for an external DAC.
- **DSP serial port** – interface to an optional external DSP for control of the CODEC.
- **I²S Zoom Video interface** – supports sample rates up to 48 kHz for MPEG audio.
- **ESFM music synthesizer** – high-quality, OPL3 superset FM synthesizer with 20 voices.
- **Hardware volume control** – 3 pushbutton inputs with internal pull-up devices for up/down/mute that can be used to adjust the master volume control.

  A software-selectable option allows the mute input to be omitted. The mute input is defined as the state when both up and down inputs are low. By default, this feature is disabled.

Analog Subsystems

- **Record and Playback Mixers** – seven input stereo mixers. Each input has independent left and right 4-bit volume control:
  - Line In
  - Mic In
  - Aux A (CD-audio)
  - Aux B (or FDXI)
  - Digitized audio (wave files)
  - FM/ES689/ES69x/IIS ZV music DAC
  - MONO_IN/MONO_OUT
- **16-Bit stereo CODEC** – for audio record and playback of the first audio channel.
- **16-Bit stereo system DAC** – for audio playback of the second audio channel.
- **16-Bit stereo music DAC** – for **ESFM™**, external wavetable synthesizer, or IIS MPEG audio.
- **1-Bit DAC** – for PC speaker digital input.
- **3-D Processor** – 3-D audio effects processor.
- **Record source and input volume control** – input source and volume control for recording. The recording source can be selected from one of four choices:
  - Line In
  - Mic In
  - Aux A (CD-audio)
  - Mixer (playback or record)
- **Mixer source** – determines which mixer is used for the record source, either the playback or record mixer.
- **Output volume and mute control** – The master volume is controlled either by programmed I/O or by volume control switch inputs. The master volume supports 6 bits per channel plus mute.
- **Reference generator** – analog reference voltage generator.
- **PC speaker volume control** – The PC speaker is supported with a 1-bit DAC with volume control. The analog output pin PCSPKO is intended to be externally mixed at the external amplifier.
- **Filter** – switched capacitor low-pass filter.
- **General purpose I/O** – outputs available to system software for power management or other applications.
- **Pre-amp** – 26 dB microphone pre-amplifier.

MIXER SCHEMATIC BLOCK DIAGRAM

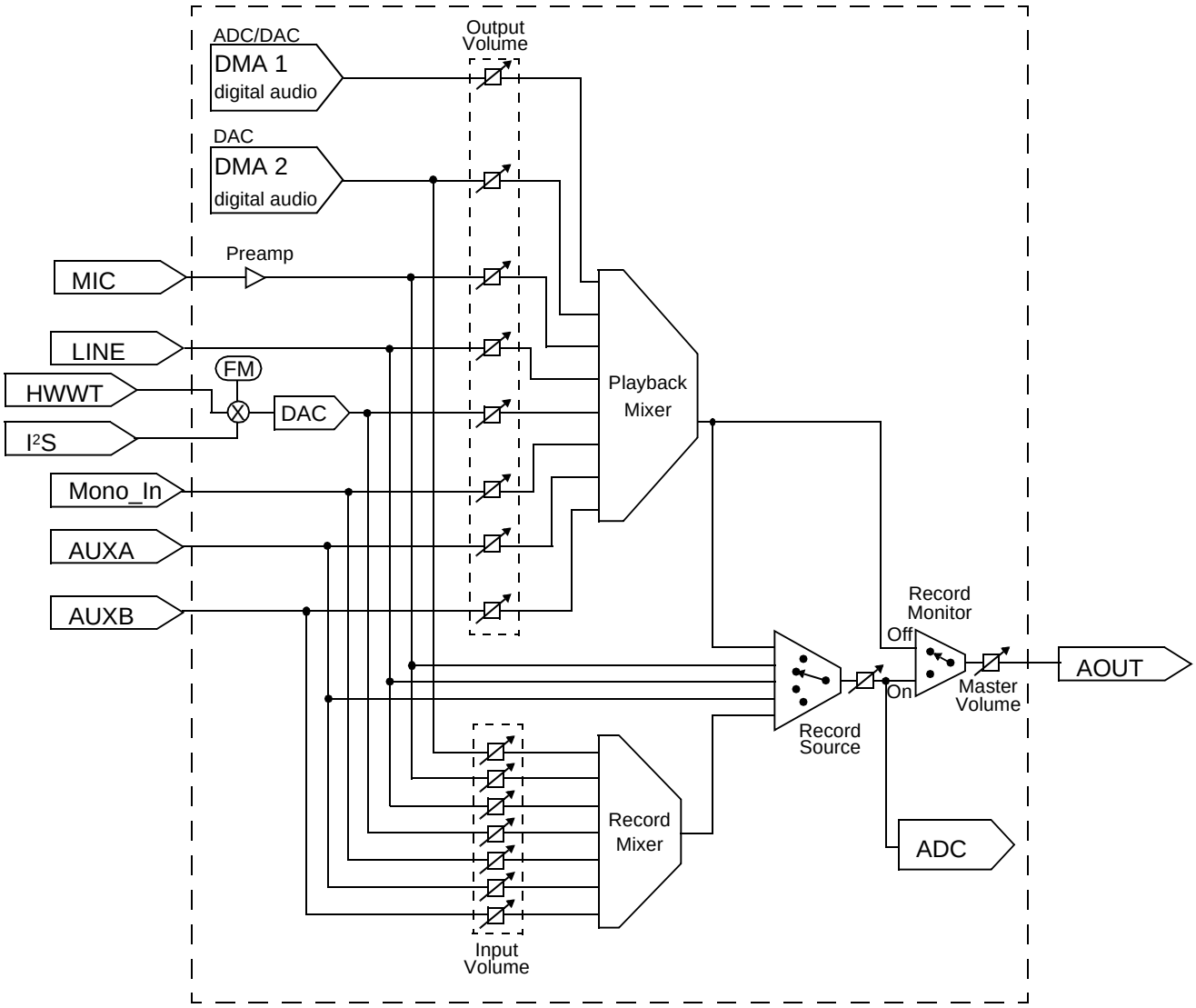


Figure 5 ES1869 Mixer Schematic Block Diagram

BUS INTERFACING

This section discusses interfacing to the PC bus, and items relating to configuration for the bus.

Table 1 shows the pins used to interface the ES1869 to the ISA bus.

Table 1 ISA Bus Interface Pins

Pins	Descriptions
A[15:12]	Dual-purpose pins. A[15:12] are ISA bus address inputs.
A[11:0]	ISA bus address inputs.
AEN	ISA active-low address enable.
D[7:0]	ISA bidirectional data bus.
DRQD	Dual-purpose pin. DRQD is a tri-state output. Optional 16-bit DMA request for IDE interface.
DACKBD	Dual-purpose pin. DACKBD is an optional 16-bit DMA acknowledge for IDE interface.
DRQ(A-C)	Three (A, B, C) active-high DMA requests to the ISA bus. Unselected DRQ outputs are high-impedance. When DMA is not active, the selected DRQ output has a pull-down device that holds the DRQ line inactive unless another device that shares the same DRQ line can source enough current to make the DRQ line active. DRQs are software configurable.
DACKB(A-C)	Three (A, B, C) active-low DMA acknowledge inputs.
IRQ(A-F)	Six (A, B, C, D, E, F) active-high interrupt requests to the ISA bus. Unselected IRQ outputs are high-impedance. IRQs are software configurable.
IORB	ISA active-low read strobe.
IOWB	ISA active-low write strobe.
RESET	Active-high. Reset from ISA bus.

DIGITAL AUDIO

The ES1869 incorporates two digital audio channels. There are three sources of DMA requests and three targets for DMA acknowledge:

Audio 1 The first audio channel. This channel is used for Sound Blaster Pro compatible DMA, Extended mode DMA, and programmed I/O. It can be used for either record or playback. Ideally, this channel should be assigned to ISA channel 1.

Audio 2 The second audio channel. This channel is used for audio playback in full-duplex mode. This channel can be mapped to any of the three 8-bit ISA DMA channels: 0,1, or 3.

External GPO1 can be assigned to be a DMA acknowledge output, GPI can be used as a DMA request input from an external device; either CD-ROM, Modem, or general-purpose device. This channel can be mapped to any of the four DRQ/DACK pairs.

The three DMA sources are mapped to the four DMA pin pairs by Plug and Play (PnP) registers. Also, the four DMA pin pairs are assigned ISA DMA channel numbers by Vendor-Defined Card-Level registers 23h and 24h. At least two of the four pin pairs must be assigned to 8-bit ISA DMA channels (0,1, or 3). The other one or two of the four pin pairs can be assigned to one of the 16-bit ISA DMA channels (5, 6, or 7) for use by the external DMA source.

In order for a DRQ output pin to be *driving* (as opposed to *high-impedance*), two conditions must be met:

- The PnP register for the DMA of a given device must match the ISA DMA channel number of the pin.
- The given device must be activated; that is, bit 0 of PnP register 30h must be high.

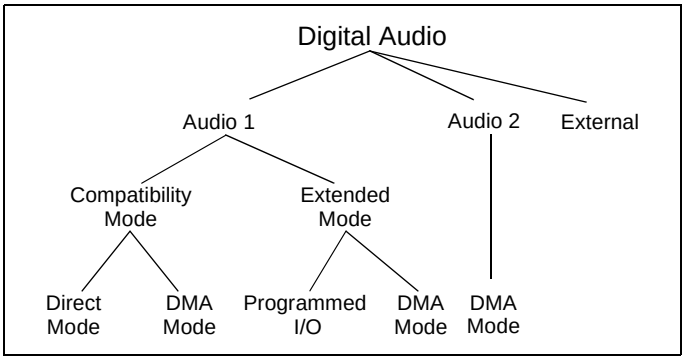


Figure 6 Data Transfer Modes

Programming DMA Transfers

Programming data transfers can be complicated with the ES1869. Both Compatibility and Extended modes offer a variety of modes for conducting transfers. The commands to enable the different transfers vary depending on which DMA channel and which mode (Compatibility or Extended) is used.

The biggest difference in available data transfer modes is between audio channel 1 and audio channel 2. This is illustrated in Figure 6. Audio 2 only allows for DMA mode. Audio 1 allows for Direct mode and DMA mode when using Compatibility mode, and for programmed I/O and DMA mode when using Extended mode.

Data Formats

See “Data Formats” on page 45.

DMA Transfers in Compatibility Mode

The first audio channel is programmed using standard Sound Blaster compatible commands. These commands are written to the chip through port Audio_Base+Ch.

When programming the first audio channel for transfers, one of the following modes can be used:

- Direct mode
- DMA modes
  - Normal
  - Auto-Initialize

In addition, both DMA Normal mode and DMA Auto-Initialize mode can use a special High-Speed mode.

Direct Mode

In Direct mode, timing for DMA transfers is handled by the application program. For example, the system timer can be reprogrammed to generate interrupts at the desired sample rate. At each system timer interrupt, the command 10h, 11h, 20h, or 21h is issued followed by the sample. Polling of the Write-Buffer-Available flag (Audio_Base+Ch [bit 7]) is required before writing the command and between writing the command and the data.

NOTE: The switched capacitor filter is initialized by reset for an intended sample rate of 8 kHz. In Direct mode, the application may wish to adjust this filter appropriate to the actual sample rate. Do this by programming the timer with command 40h just as if the application were using DMA mode.

DMA Modes

In DMA mode, the programmable timer in the ES1869 controls the rate at which samples are sent to the CODEC. The timer is programmed using command 40h, which also sets up the programmable filters inside the ES1869. The ES1869 firmware maintains an internal FIFO (32 levels for 16-bit transfers, 64 levels for 8-bit transfers) that is filled by DMA transfers and emptied by timed transfers to the DAC.

Before a DMA transfer, the application first programs the DMA controller for the desired transfer size and address, then programs the ES1869 with the same size information. At the end of the transfer, the ES1869 generates an interrupt request, indicating that the current block transfer is complete. The FIFO gives the application program sufficient time to respond to the interrupt and initiate the next block transfer.

The ES1869 supports both Normal DMA mode and Auto-Initialize DMA mode.

Normal DMA Mode

In Normal mode DMA transfers, the DMA controller must be initialized and the ES1869 commanded for every block that is transferred.

Auto-Initialize DMA Mode

In Auto-Initialize mode, the DMA transfer is continuous, in a circular buffer, and the ES1869 generates an interrupt for the transition between buffer halves. In this mode the DMA controller and ES1869 only need to be set up once.

High-Speed Mode

The ES1869 supports mono 8-bit DMA transfers at a rate up to 44 kHz. Mono 16-bit transfers are supported up to a rate of 22 kHz.

The special “High-Speed mode” allows 8-bit sampling up to 44 kHz for ADC, using commands 98h (auto-initialize) and 99h (normal). No automatic gain control (AGC) is performed. The input volume is controlled with command DDh.

DMA Transfers in Extended Mode

The first audio channel is programmed using the controller registers internal to the ES1869. The commands written to the controller registers are written to the chip through port Audio_Base+Ch.

When programming the first audio channel for transfers, one of the following modes can be used:

- Programmed I/O
- DMA modes
  - Normal (Single or Demand transfer)
  - Auto-Initialize (Single or Demand transfer)

In addition, both DMA normal mode and DMA auto-initialize mode use Single transfer or Demand transfer modes.

Programmed I/O

For some applications, DMA mode is not suitable or available for data transfer, and it is not possible to take exclusive control of the system for DAC and ADC transfers. In these situations, use I/O block transfers within an interrupt handler. The REP OUTSB instruction of the 80x86 family transfers data from memory to an I/O port specified by the DX register. The REP INSB instruction is the complementary function. Use ES1869 port Audio_Base+Fh for block transfers.

I/O transfers to FIFO are nearly identical to the DMA process, except that an I/O access to port Audio_Base+Fh replaces the DMA cycle. For details about programmed I/O operation see “Extended Mode Programmed I/O Operation” on page 52.

DMA Modes

Extended mode DMA supports both Normal and Auto-Initialize mode. In addition Normal mode and Auto-Initialize mode both support Single and Demand transfer modes.

Single Transfer

One byte is transferred per DMA request.

Demand Transfer

To reduce the number of DMA requests necessary to make a transfer, two or four bytes are transferred per DMA request (DRQ). Using Demand transfer enables multiple DMA acknowledges for each DMA request.

For a description of DMA mode including Normal DMA mode and Auto-Initialize DMA mode see “DMA Modes” on page 13.

Extended Mode Audio 1 Controller Registers

The following registers control operation of the first audio channel in Extended mode:

Table 2 Extended Mode Audio 1 Controller Registers

Address	Name
A1h	Audio 1 Sample Rate Generator register
A2h	Audio 1 Filter Clock Divider register
A4h	Audio 1 Transfer Count Reload register – low byte
A5h	Audio 1 Transfer Count Reload register – high byte
B1h	Legacy Audio Interrupt Control register
B2h	Audio 1 DRQ Control register
B4h	Input Volume Control register
B5h	Audio 1 DAC Direct Access register – low byte
B6h	Audio 1 DAC Direct Access register – high byte
B7h	Audio 1 Control 1 register
B8h	Audio 1 Control 2 register
B9h	Audio 1 Transfer Type register

Data Transfers Using the Second Audio Channel

The second audio channel is programmed using mixer registers 70h through 7Dh. The commands written to the mixer registers are written to the chip through ports Audio_Base+4h and Audio_Base+5h.

DMA mode is used when programming the second audio channel for transfers:

- DMA modes
  - Normal (Single or Demand transfer)
  - Auto-Initialize (Single or Demand transfer)

In addition, both DMA Normal mode and DMA Auto-Initialize mode use Single or Demand transfer modes.

DMA Modes

DMA under the second audio channel supports both Normal and Auto-Initialize mode. In addition, Normal mode and Auto-Initialize mode both support Single and Demand transfer modes.

For a description of DMA mode including Normal DMA mode and Auto-Initialize DMA mode, see “DMA Modes” on page 13.

For a description of Single and Demand transfer modes, see “DMA Modes” on page 14.

Audio 2 Related Mixer Registers

The following registers control DMA operations for the second audio channel:

Table 3 Audio 2 Related Mixer Registers

Address	Name
70h	Audio 2 Sample Rate register
71h	Audio 2 Mode register
72h	Audio 2 Filter Clock Rate register
74h	Audio 2 Transfer Count Reload register – low byte
76h	Audio 2 Transfer Count Reload register – high byte
78h	Audio 2 Control 1 register
7Ah	Audio 2 Control 2 register
7Ch	Audio 2 DAC Volume Control register

External DMA Sharing with Audio DMA

It is possible for an external DMA device to share a DMA channel with audio DMA if they do not operate at the same time, and if the respective Windows drivers can communicate with each other. In this case, the external DMA device does not request an audio channel in its resource data. Instead, the Windows driver writes to the PnP DMA register of the appropriate device to assign it to the same DMA channel as one of the two audio channels.

Bits 4:2 of Vendor-Defined Card-Level register 26h can be used to mask any of the three DMA sources (audio 1, audio 2, and external). Use masking when DMA channels are shared to be sure that only one device has access to a given DMA channel at one time.

DRQ Latch Feature

DRQ latching is enabled when bit 7 of PnP Vendor-Defined Card-Level register 25h is high.

If this feature is enabled, each of the four audio DRQs is latched high until one of the following occurs:

- A DACK low pulse occurs while DRQ is low or goes low due to a DACK pulse.
- A hardware reset occurs.
- 8-16 milliseconds elapse while DRQ is low.

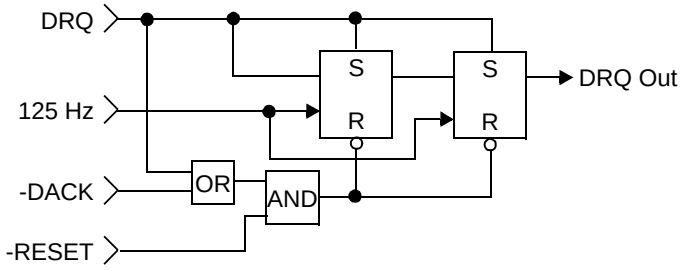


Figure 7 DRQ Latch

First DMA Channel CODEC

The CODEC of the first audio channel cannot perform stereo DAC and ADC simultaneously. It can either be a stereo DAC, a stereo ADC, or a mono CODEC. After reset, the CODEC is set up for DAC operations. Any ADC command causes a switch to the ADC “direction,” and any subsequent DAC command switches the converter back to the DAC “direction.”

The DAC output is filtered and sent to the mixer. After reset, input to the mixer from the first audio channel DAC is muted to prevent pops. The ES1869 maintains a status flag to determine if the input to the mixer from the first audio channel DAC is enabled or disabled. Command D8h returns the status of the flag (0h=disabled and FFh=enabled). Use command D1h to enable input to the mixer from the first audio channel DAC and command D3h to disable the input.

To play a new sound without resetting beforehand, when the status of the analog circuits is not clear, mute the input to the mixer with command D3h, then set up DAC direction and level using the direct-to-DAC command:

10h + 80h

Wait 25 milliseconds for the analog circuitry to settle before enabling the voice channel with command D1h.

Pop sounds may still occur if the DAC level was left at a value other than mid-level (code 80h on an 8-bit scale) by the previous play operation. To prevent this, always finish a DAC transfer with a command to set the DAC level to mid-range:

10h + 80h

INTERRUPTS

There are seven interrupt sources in the ES1869, shown in Table 4.

Table 4 ES1869 Interrupt Sources

Interrupt Source	Description
Audio 1	An interrupt used for the first DMA channel (Sound Blaster compatible DMA, Extended mode DMA, and Extended mode programmed I/O), as well as Sound Blaster-compatible MIDI receive. Controller register B1h controls use of this interrupt for Extended mode DMA and programmed I/O. This interrupt request is cleared by hardware or software reset, or an I/O read from port Audio_Base+0Eh. The interrupt request can be polled by reading from port Audio_Base+0Ch. The Audio 1 interrupt is assigned to an interrupt channel by PnP register 70h of LDN 1.
Audio 2	An optional interrupt for the second DMA channel. The ES1869 can operate in full-duplex mode using two DMA channels. However, since the second DMA channel must share the same sample rate as the first DMA channel, it is not necessary to use a separate interrupt for the second DMA channel. The Audio 2 interrupt is masked by bit 6 of mixer register 7Ah. It can be polled and cleared by reading or writing bit 7 of register 7Ah. This interrupt is assigned to an interrupt channel by PnP register 72h of LDN 1.
Hardware Volume	Hardware volume activity interrupt. This interrupt occurs when one of the three hardware volume controls changes state. Bit 1 of mixer register 64h is the mask bit for this interrupt. The interrupt request can be polled by reading bit 3 of register 64h. The interrupt request is cleared by writing any value to register 66h. The Hardware Volume interrupt is assigned to an interrupt channel by PnP register 27h. Typically this interrupt, if used, is shared with an audio interrupt.
MPU-401	The MPU-401 interrupt occurs when a MIDI byte is received. It goes low when a byte is read from the MIDI FIFO and goes high again quickly if there are additional bytes in the FIFO. The interrupt status is the same as the Read-Data-Available status flag in the MPU-401 status register. The MPU-401 interrupt is masked by bit 6 of mixer register 64h. This interrupt is assigned to an interrupt channel in one of two ways. If the MPU-401 is part of the audio device, then PnP register 28h is used to assign the MPU-401 interrupt. If the MPU-401 is its own logical device, it can also be assigned to an interrupt by PnP register 70h of LDN 3. Both these methods access the same physical register.
CD-ROM	The source of the CD-ROM interrupt is the input pin CDIRQ.
Modem	The source of the Modem interrupt is the input pin MMIRQ.
General-Purpose	The source of the General-Purpose interrupt is the input pin GPI. If GPI is used for a DMA request for the CD-ROM, Modem, or General-Purpose device, then this pin cannot be used as a general-purpose device interrupt.

Interrupt sources are mapped to one of the six interrupt output pins through the PnP registers. Zero, one, or more interrupts can map to any given pin. Each PnP pin is assigned to an ISA interrupt channel number by Vendor-Defined Card-Level PnP registers 20h, 21h, and 22h. These registers are automatically loaded from the 8-byte header in the PnP configuration data.

Each interrupt pin can be in either an active or high-impedance state.

If a given interrupt pin has one or more sources assigned to it, and one or more of those sources is activated (register 30h, bit 0), then the interrupt pin is active; that is, it always drives high or low. An exception is the Modem interrupt, which can be deactivated if input MMIEB is high or if the Modem device is not active. Each interrupt also has one or more mask bits that are AND'ed with the interrupt request.

Interrupt Status Register

Port Config_Base+6h of the configuration device can be read to quickly find out which ES1869 interrupt sources are active. The bits are:

Table 5 Interrupt Status Bits in Config_Base+6h

Bit	Description
0	Audio 1 interrupt request
1	Audio 2 interrupt request AND'ed with bit 6 of mixer register 7Ah
2	Hardware volume interrupt request AND'ed with bit 1 of mixer register 64h
3	MPU-401 receive interrupt request AND'ed with bit 6 of mixer register 64h
4	CDIRQ input pin
5	MMIRQ input pin AND'ed with inverse of MMIEB input
6	GPI input pin

Interrupt Mask Register

Port Config_Base+7h can be used to mask any of the seven interrupt sources.

The mask bits can be used to force the interrupt source to be zero, without putting the interrupt pin in a high-impedance state. Each bit is AND'ed with the corresponding interrupt source. This register is set to all ones by hardware reset.

The Interrupt Status register (ISR) is not affected by the state of the Interrupt Mask register (IMR). That is, the ISR reflects the status of the interrupt request lines before being masked by the IMR.

The IMR is useful when interrupts are shared. For example, assume that Audio 1, Audio 2, Hardware Volume, and MPU-401 all share the same interrupt in Windows. When returning from Windows to DOS, the Hardware Volume, MPU-401, and Audio 2 interrupts can be masked by setting the appropriate bits to 0.

A second use is within an interrupt handler. The first thing the interrupt handler can do is mask all the interrupt sources mapped to the interrupt handler. Then, the ISR can be polled to decide which sources to process. Just before exiting the interrupt handler, the IMR can be restored. If an unprocessed interrupt remains active, it generates an interrupt request because the interrupt pin was low during the masked period and then went high when the interrupt sources were unmasked. Also, while the interrupts are masked, the individual interrupt sources can change state any number of times without generating a false interrupt request.

Sharing Interrupts

Plug and Play does not allow sharing of interrupts in its resource assignment decision making. If a device wants to share an interrupt with another device that has been assigned an interrupt by PnP, the first device cannot request an interrupt for itself.

A logical device that supports interrupts can be assigned to an interrupt after the PnP sequence by the Windows driver. Refer to “Bypass Key” on page 28 for information on the PnP sequence. In this case, it would typically be forced to share an interrupt with the first audio interrupt. For all but two cases, this is done simply by programming the appropriate PnP register (70h or 72h) for the selected device. Below are the two exceptions:

- The hardware volume interrupt. This interrupt source can be assigned to an interrupt through Vendor-Defined Card-Level register 27h.
- The MPU-401 interrupt. This device is either part of the audio device or its own logical device. If it is part of the audio device, the interrupt can be assigned by writing to Vendor-Defined Card-Level register 28h. If this device is its own logical device, it is assigned an interrupt by either register 28h or register 70h of LDN 3.

PERIPHERAL INTERFACING

I²S Serial Interface

Three input pins, IISDATA, IISCLK, and IISLR, are used for a serial interface between an external device and a stereo DAC within the ES1869. These inputs can be left floating or connected to ground if the serial interface is not used.

Typical applications of the I²S serial interface are MPEG audio or digital CD audio.

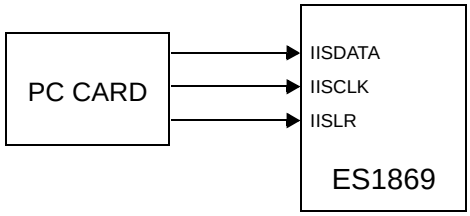


Figure 8 I²S Implementation in ES1869

Table 6 identifies the three pins in the I²S interface.

Table 6 I²S Interface Pins

Pin	Description
IISLR	Left/right strobe for I²S interface. Input with pull-down.
IISDATA	Serial data for I²S interface. Input with pull-down.
IISCLK	Serial shift clock for I²S interface. Input with pull-down.

I²S Serial Interface Timing

Within the ES1869, IISLR and IISDATA are sampled on the rising edge of IISCLK. See Figure 31 and Figure 32 for detailed I²S timing.

Wavetable Interface

The ES1869 contains a synchronous serial interface for connection to an ES689/ES69x wavetable music synthesizer. Table 7 identifies pins in the wavetable interface.

Table 7 Wavetable Interface Pins

Pin	Description
MCLK	Serial clock from external ES689/ES69x music synthesizer (2.75 MHz).
MSD	Serial data from external ES689/ES69x music synthesizer. When both MCLK and MSD are active, the stereo DACs that are normally used by the FM synthesizer are acquired for use by the external ES689/ES69x. The normal FM output is blocked.

DSP Interface

The ES1869 contains a synchronous serial interface for connection to a DSP serial interface. The typical application for this interface is a speakerphone.

Table 8 identifies pins in the DSP interface.

Table 8 DSP Interface Pins

Pin	Description
SE	Active-high signal from an external DSP to enable serial mode.
DCLK	Data clock. The rate can vary, but a typical value is 2.048 MHz (8 kHz x 256).
DX	Data transmit. Active output when data is being transmitted serially from the ES1869, otherwise high-impedance.
DR	Serial data input.
FSX	Frame sync transmit. FSX is either active-high or active-low based on bit 3 of mixer register 48h. The FSX pulse is a request from the external DSP to begin transmission of 8 or 16 bits of data out of pin DX.
FSR	Frame sync receive. FSR is either active-high or active-low, based on bit 3 of mixer register 48h. The FSR pulse signals the arrival of 8 or 16 bits of data to pin DR.

DSP Operating Modes

There are two DSP data transfer modes for the ES1869. The state of a single switch internal to the ES1869 determines which mode is enabled. This switch can route the first audio channel to the second audio channel DAC. When the first audio channel is routed to the second audio channel DAC, Telegaming mode is enabled. Otherwise the DSP is operating in its default mode.

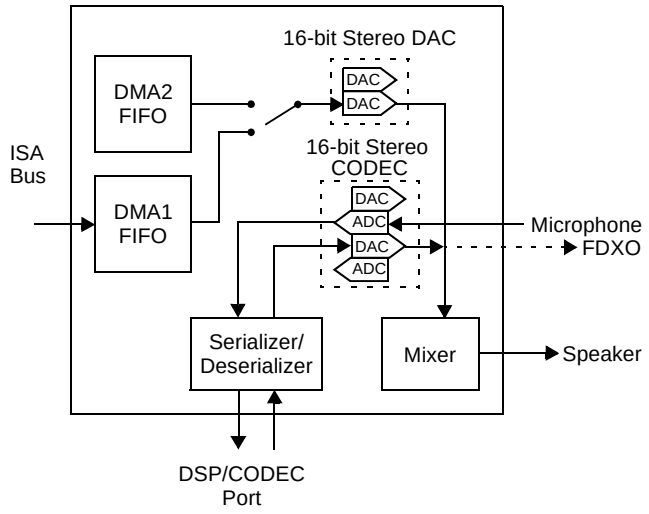


Figure 9 Telegaming Mode

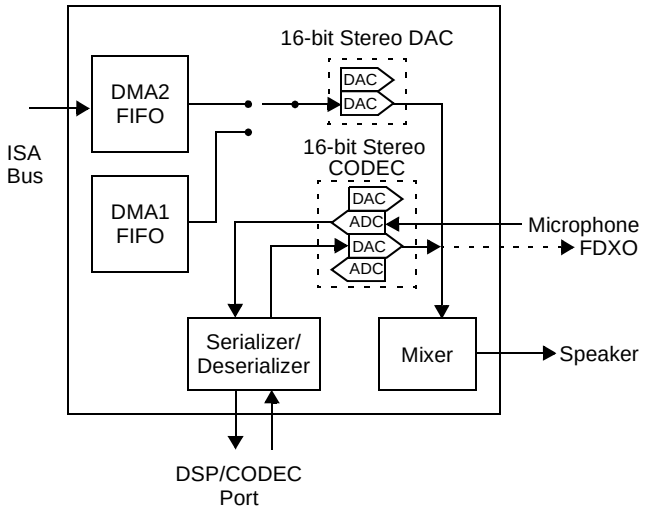


Figure 10 Default Mode

Telegaming Mode

This mode is enabled when two conditions are present:

1. The DSP serial port must be enabled (i.e., either bit 7 of mixer register 48h is high or the input pin SE is high).
2. Bit 1 of mixer register 48h is high. This bit enables Telegaming mode.

In previous chips, when the DSP serial port is enabled, the Audio 1 CODEC is unavailable for use by the first audio channel. This means digital audio for Sound Blaster Pro compatible games is muted. Sound Blaster can use only the first audio channel for digital audio. The Audio 1 CODEC is used by the DSP.

In Telegaming mode, the first audio channel can be switched over to the Audio 2 DAC. Internally, the first audio channel is routed to the second audio channel DAC and the second audio channel has no function. In addition, the second audio channel mixer volume control is slaved to the first channel mixer volume control.

Default Mode

The default mode operates just like Telegaming mode except that data from the first audio channel cannot be heard. Data sent through the second audio channel can be mixed as in Telegaming mode.

No Acoustic Echo Cancellation

The DSP cannot perform acoustic echo cancellation in either mode. Because the audio from the host does not pass directly through the DSP, there is no way for the DSP to compensate for acoustic echo. Therefore, using a headset for either the microphone or speakers or both is recommended.

DSP Digital Audio Playback

There are two choices for mixing the DSP digital audio playback data with other audio sources. The audio data can be mixed in the ES1869's internal playback mixer or externally to the ES1869.

Mixing Internal to the ES1869

The DSP digital audio playback can be mixed within the ES1869 playback mixer. To select this method, set the Output Signal Control bits of the mixer register 44h for mixer output. To do this, program bits 6:4 of mixer register 44h to 1, 0, and 0, respectively. The volume of the DSP digital audio playback is controlled by the Audio 1 Play Volume register (14h).

NOTE: In Telegaming mode, register 14h also controls the game-compatible first audio channel digital audio playback. If independent mixer volume control of the game-compatible and DSP digital audio data is necessary, use the second method.

Mixing External to the ES1869

The second method is to use the FDXO output pin and mix the DSP digital audio playback and the game-compatible digital audio playback in an external audio mixer. To select this method, set the Output Signal Control bits of mixer register 44h for mixer output except DAC playback. To do this, program bits 6:4 of register 44h to 1, 0, and 1,

respectively. In addition, set bit 1 of Mixer register 46h high to enable FDXO as an output when DSP serial mode is enabled.

The volume of the DSP digital audio playback is controlled within the DSP by scaling the data.

Serial Data Format

Figure 11 shows the format for serial data used with the DSP serial interface.

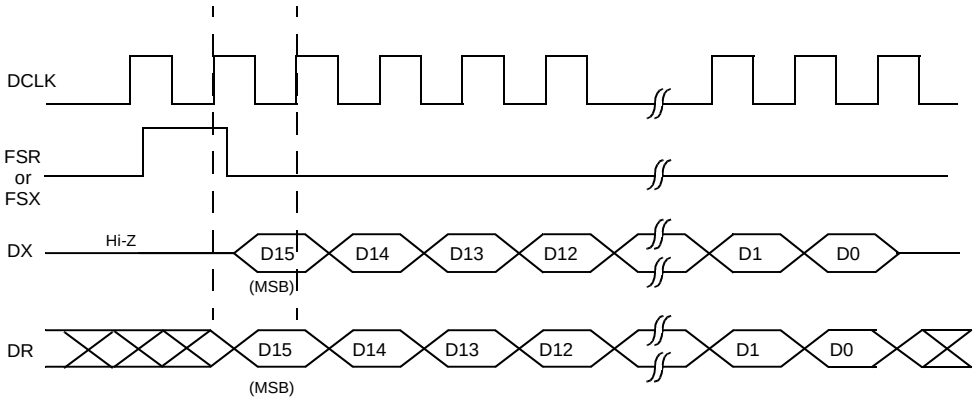


Figure 11 16-Bit Data, Positive Sync Pulse

Modem Interface

The ES1869 allows a direct interface to an external modem. There are four pins dedicated for an external modem. Table 9 identifies pins in the Modem interface.

Table 9 External Modem Interface Pins

Pin	Description
MMCSB	Output from the ES1869 to an external modem chip select, active-low. The address space is determined by the PnP configuration. The Modem device uses eight consecutive addresses, with the base address, typically one of the COM ports.
MMIRQ	Interrupt request from the Modem device. This signal is mapped to an IRQ output on the ES1869, based on the PnP configuration.
MMIEB	Modem interrupt enable input. Active-low when the Modem interrupt is enabled. High when the Modem interrupt request is disabled. Generated from the Modem UART.
GPCS	User-defined general-purpose chip select output. If selected by the PnP logic and based on the PnP configuration.

Modem Operating Modes

If the modem DSP also requires a DMA channel, the GPI/GPO1 pins can be used for DRQ/-DACK from the modem.

The modem can also connect to the ES1869 through the DSP serial interface. This allows the modem to set the sample rate for both chips and have access to the microphone and speaker for speakerphone or voice-over-data applications. DSP determines the sample rate of the serial link by generating FSR/FSX pulses.

Figure 12 shows a typical modem interface application, a speakerphone or modem with voice-over-data.

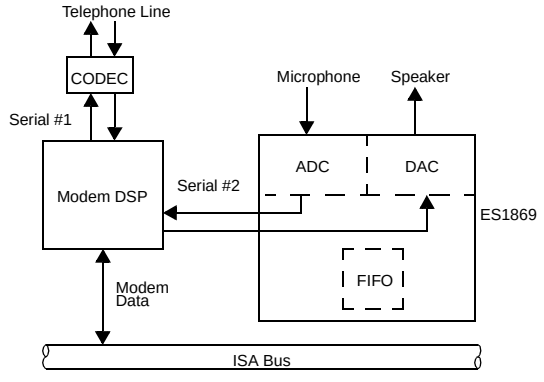


Figure 12 Speakerphone or Modem w/ Voice-Over-Data

IDE CD-ROM Interface

The ES1869 allows a direct interface to an IDE CD-ROM drive. There are four pins dedicated for an IDE CD-ROM interface. Table 10 identifies these pins.

Table 10 IDE CD-ROM Interface Pins

Pin	Description
CDIRQ	Interrupt request from CD-ROM. Internally routed to one of the six IRQ ISA outputs (A-F).
CDCSB0	Active-low decode output for eight command block registers. 24 mA driver.
CDCSB1	Active-low decode output for two control block registers. 24 mA driver.
CDENBL	Active-low decode output for external 74LS245 transceiver that buffers the least 8 bits of the ISA data bus. This pin is active-low when CDCSB0, CDCSB1, or CD DMA -DACK is active-low.

In most cases, the IDE interface does not use DMA. If it *must* use DMA, then the GPO1/GPI pair (pins 91 and 92) can be used for this purpose. In this case, these pins would not be available for other external devices such as a modem/audio processor. Also, typically only one of the 4 DRQ/DACK pairs of the ES1869 would be connected to a 16-bit DMA channel. This does not give the PnP system any choice about assigning the CD DMA channel.

It is not recommended to use DMA for the CD-ROM.

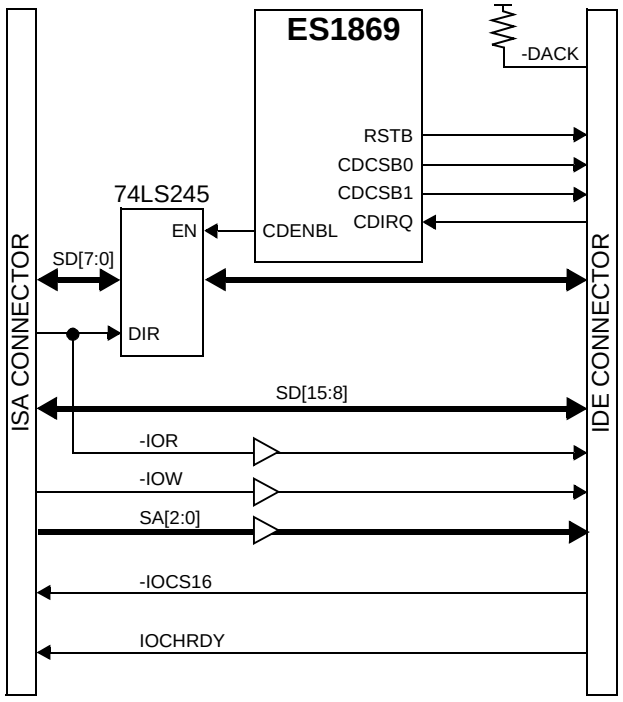


Figure 13 IDE Interface – Typical Application

General-Purpose I/O Device

In addition to modem and CD-ROM interfaces, the ES1869 Plug and Play logic supports one general-purpose I/O device. The GPO0 output can be configured to provide an active-high chip-select output when this device is accessed. The General-Purpose device can decode 1, 2, 4, 8, or 16 consecutive addresses.

It is also possible to use GPI/GPO1 as a DMA channel for the General-Purpose device if these pins are not used for the Modem or CD-ROM device.

The GPI pin can also be used as an interrupt source for the General-Purpose device if the pin is not otherwise used.

Joystick / MPU-401 Interface

MPU-401 UART Mode

There are two separate MIDI interfaces in the ES1869. The Sound Blaster compatible command set and a MPU-401 “UART mode” compatible serial port. MPU-401 is a superior method of MIDI serial I/O because it does not interfere with DAC or ADC Sound Blaster commands. Both methods of serial I/O share the same MSI and MSO pins. The MPU-401 interface consists of separate 8-byte FIFOs for receive and transmit.

By default after hardware reset, the MPU-401 interface is disabled. It must be configured using PnP register 30h of LDN3, which is described in “LDN 3: MPU-401 Device” on page 35.

MPU-401 requires an interrupt channel for MIDI receive. This interrupt should be selected using PnP register 70h of LDN3. It should be different than the interrupt selected for audio DMA interrupts.

If MPU-401 is enabled, a low-level signal on pin MSI prevents power-down and causes automatic wake-up if the ES1869 is powered down. Likewise, power-down is prevented if a byte is currently being received or transmitted.

Temporarily disabling MPU-401 using PnP register 30h of LDN3 (if MPU-401 is its own device) or PnP register 30h of LDN1 (if MPU-401 is part of the audio device) acts as a reset to the FIFOs.

Joystick / MIDI External Interface

The joystick portion of the ES1869 reference design is identical to that on a standard PC game control adaptor or game port. The PC compatible joystick can be connected to a 15-pin D-sub connector. It supports all standard PC joystick-compatible software. If the system already has a game card or port, either remove the game card or disable the joystick port in the reference design by removing the joystick enable jumper. Disabling the joystick port does not affect its use as a MIDI port.

If multiple joysticks are required, use a joystick conversion cable. This cable uses a 15-pin D-sub male connector on one end, and two 15-pin D-sub female connectors on the other end. All signals on this cable have direct pin-to-pin connection, except for pins 12 and 15. On the male connector, pins 12 and 15 should be left without connection. On the female connectors, pin 15 is internally connected to pin 8, and pin 12 is internally connected to pin 4. The dual joystick and MIDI port take up only one slot in the system, leaving room for other cards. Figure 14 shows the dual joystick/MIDI connector configuration.

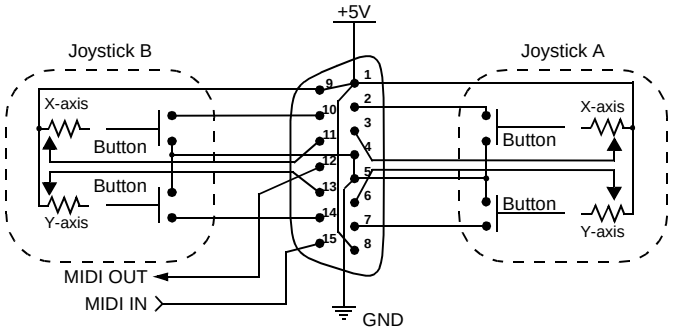


Figure 14 Dual Joystick/MIDI Connector

Figure 15 shows the MIDI serial interface adaptor from the joystick/MIDI connector.

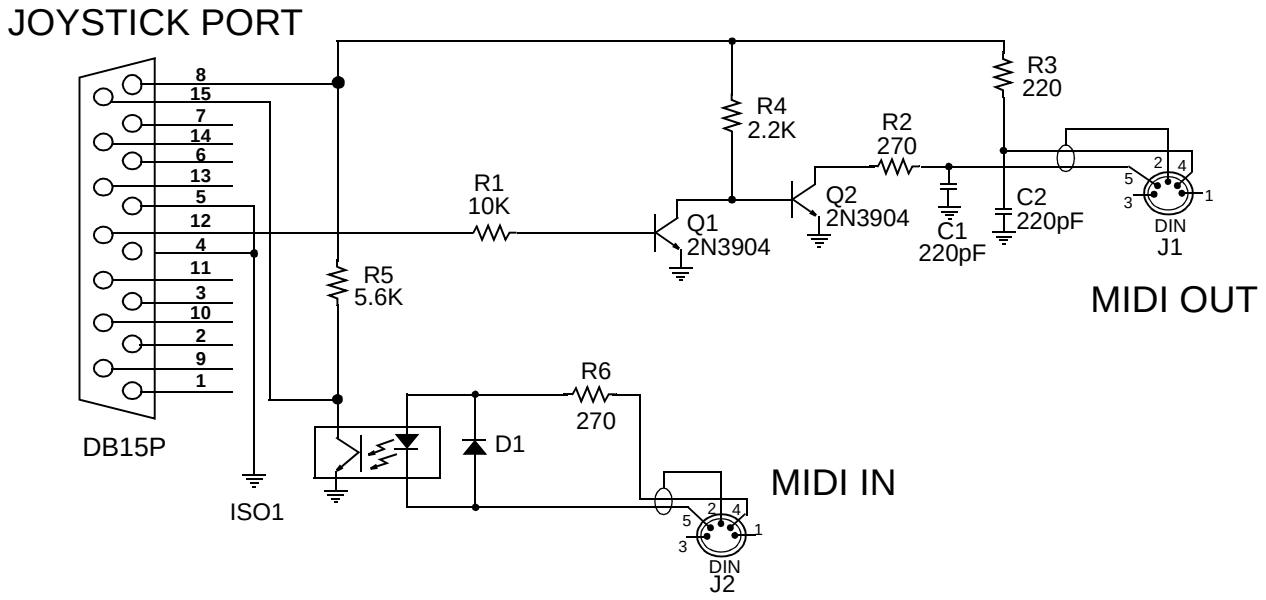


Figure 15 MIDI Serial Interface

Serial EEPROM Interface

The ES1869 gets Plug and Play configuration data from an internal masked ROM or an external EEPROM device. The external EEPROM device is 512K x 8-bit in size.

The EEPROM interface is shared with the hardware volume controls. When the EEPROM interface is active, the volume controls are deactivated. See Figure 16.

The host processor can read or write the EEPROM, allowing the EEPROM to be reprogrammed or initially programmed during production test.

Pin 20, when used as SECS, is an input during reset. If an EEPROM exists and needs to be used, pull this pin high externally. Otherwise, pull it low, to force the use of the internal ROM.

Depending on the value of pin 20 and the operating mode selected for this pin, either the internal mask-ROM or the external EEPROM device is used.

SECS/PSEL			
0	Internal ROM		
1	93LC66	512 x 8	9 address bits

EEPROM ROM Format

```
'A5'            Sync Byte
IRQB IRQA       Mapping for IRQB/A
IRQD IRQC       Mapping for IRQD/C
IRQF IRQE       Mapping for IRQF/E
DRQB DRQA       Mapping for DRQB/A
DRQD DRQC       Mapping for DRQD/C
PNP Reg 25h     Miscellaneous
PNP Reg 26h     Miscellaneous
```

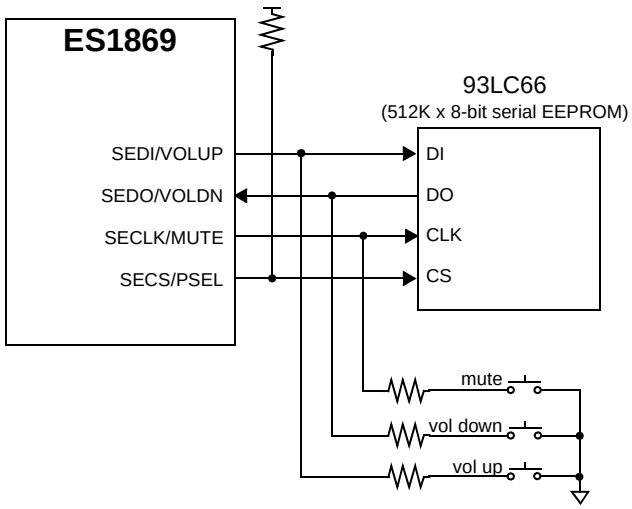


Figure 16 Serial EEPROM – Typical Application

MONO_IN and MONO_OUT

MONO_IN is a line-level analog input. It has an input pull-up resistor to CMR with a value of approximately 40 kohms. MONO_IN is an input to the playback mixer and the record mixer. The mixer volumes are controlled by mixer registers 6Dh (playback) and 6Fh (record).

Alternately, MONO_IN can be mixed with AOUT_L and AOUT_R after the mixer, Spatializer, and master volume stages. Bit 0 of mixer register 7Dh, when high, enables MONO_IN to be mixed directly (unity gain) with AOUT_L and AOUT_R.

A third use of MONO_IN is as an input to the left channel ADC in full-duplex DSP serial port mode. In this application, MONO_IN is typically a line-level microphone input (external preamp). MONO_IN can be selected as an input in serial port mode by setting bits 6 and 7 of mixer register 42h high. MONO_IN as an ADC input bypasses the recording source select and record volume stages. MONO_IN directly drives the left channel switched-capacitor filter. The output of the switched-capacitor filter is FOUT_L, which is AC-coupled externally to CIN_L, the left channel ADC input.

MONO_OUT is a line-level mono output that can drive an external 5 kohm load. During power-down or during opamp calibration, MONO_OUT is held at CMR (as are AOUT_L and AOUT_R) by an internal, high-impedance resistor divider. MONO_OUT can be selected from among four sources by bits 2 and 1 of mixer register 7Dh.

Mixer Register 7Dh		**MONO_OUT Source**
Bit 2	**Bit 1**	
0	0	Mute (CMR)
0	1	First channel filter output (actually CIN_R pin)
1	0	Second channel DAC, right channel
1	1	Mono mix of record level stage outputs

Normally bits 2:1 are both zero, so that MONO_OUT is muted.

When bit 2 is 0 and bit 1 is 1, MONO_OUT is a buffered version of input pin CIN_R. CIN_R is typically the right channel DAC output, filtered by the first channel switched-capacitor filter. If the right channel is used for ADC, CIN_R will be the right channel ADC input. MONO_OUT can be used in this application as digitized audio playback through the first channel DMA, right channel DAC, or, if the DSP serial interface is enabled, the right channel DAC output can be the digitized serial data received from the DSP.

When bit 2 is 1 and bit 1 is 0, MONO_OUT is a buffered version of the second channel, right channel DAC. In this case, the second channel DMA can play digitized audio through MONO_OUT.

When bit 2 is 1 and bit 1 is 1, MONO_OUT is a buffered version of a mono mix of the record level stage left and right outputs. This gives the utmost flexibility in the source or sources of MONO_OUT. The record source select and record levels can be programmed to generate any combination of sources and volumes for MONO_OUT.

Spatializer Audio Processor

The ES1869 contains an embedded Spatializer audio processor positioned between the output of the playback mixer and the master volume controls. The Spatializer produces a wider perceived stereo effect and also has a mode that generates a stereo effect given a mono input.

The amount of effect is controlled by directly programming Spatializer Level register 52h.

Hardware and Master Volume Control

Three external pins, VOLUP, VOLDN, and MUTE can be connected to external momentary switches to ground to implement hardware master volume controls. Pressing one of these buttons produces a low signal to one of the inputs and thereby changes the master volume.

In one mode the MUTE input can be replaced by the state where both VOLUP and VOLDN inputs are low.

The up and down buttons produce a single step change in volume when they are first pressed. If these buttons are held down, they enter a fast-scrolling mode. The single step change can be either one volume unit (.75 dB) or three volume units (2.25 dB). In scrolling mode, the step change is always one volume unit.

The three inputs have debounce circuitry within the ES1869. Hold each input low for 40 milliseconds or more for it to be recognized as a valid button press. Hold each input high for 40 milliseconds or more between button presses. A software option allows the debounce time to be reduced from 40 milliseconds to 10 microseconds.

Normally the hardware volume controls directly change the master volume registers and produce an interrupt at each change. However, the ES1869 can be programmed so that the hardware volume controls do not directly change the master volume registers. This is called “split mode”, in which the hardware volume control counters are split from the master volume registers. Pressing a hardware volume control button changes the hardware volume counters and produces an interrupt. The host

software can read the hardware volume counters and update the master volume registers as needed. Split mode is enabled by bit 7 of mixer register 64h.

For support of mixer master volume control, a write to mixer registers 22h or 32h translates automatically into writes to the master volume registers. Since register 22h only has 3-bit resolution per channel, and register 32h only has 4-bit resolution per channel, a translation circuit is included in the ES1869 that translates 3- or 4-bit volume values into the 6-bit volume + mute that is used in the master volume registers. Support of these mixer registers can be defeated under software control.

Reading master volume registers 22h or 32h also requires a translation circuit to translate 6-bit + mute master volumes into 3- or 4-bit master volume numbers for registers 22h or 32h.

PC Speaker

The PC Speaker is supported with a 1-bit DAC with volume control. The analog output pin PCSPKO is intended to be externally mixed at the external amplifier.

PC Speaker Volume Control

When the PCSPKI signal is high, a resistive path to analog ground is enabled. The value of the resistor is selected from among 7 choices to control the amplitude of the output signal.

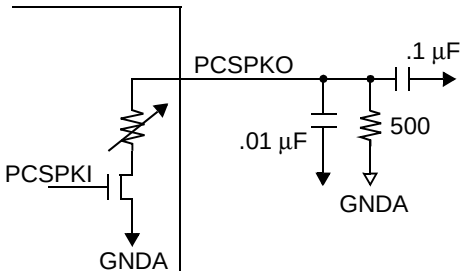


Figure 17 PC Speaker Volume Circuitry

With the external circuit shown in Figure 17, the amplitude of a square wave output on pin PCSPKO should be approximately VDDA/2 for maximum volume, i.e., the internal resistor is approximately 500 ohms (± 30%). The other levels are relative to this amplitude as follows:

off, -18dB, -15dB, -12dB, -9dB, -6dB, -3dB, +0dB

The purpose of the circuit, beyond volume control of the speaker, is to prevent digital noise from the PC speaker signal being mixed into the analog signal. This circuit provides a clean analog signal. The output can be either mixed with the AOUT_L and AOUT_R pins externally or it can be used to drive a simple transistor amplifier to drive an 8 ohm speaker dedicated to producing beeps.

ANALOG DESIGN CONSIDERATIONS

This section describes design considerations related to inputs and outputs of analog signals and related pins on the chip.

Game Port

The game port address 201h is decoded for timer pins TA, TB, TC, and TD, and switch pins SWA, SWB, SWC, and SWD. The MIDI serial input and output also come from the game port connector in most applications.

Reference Generator

Reference generator pin CMR is shown bypassed to analog ground.

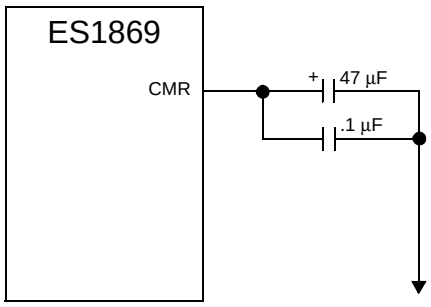


Figure 18 Reference Generator Pin Diagram

Switch-Capacitor Filter

The outputs of the FOUT_L and FOUT_R filters must be AC-coupled to the inputs CIN_L and CIN_R. This provides for DC blocking and an opportunity for low-pass filtering with capacitors to analog ground at these inputs.

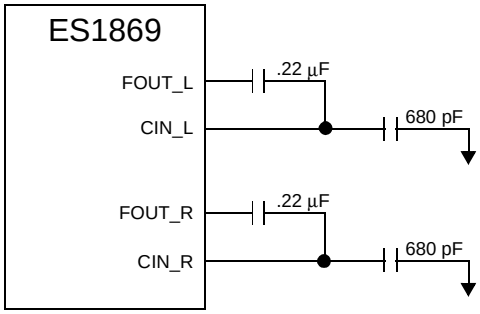


Figure 19 Switch-Capacitor Filter Pin Diagram

Audio Inputs and Outputs

Analog inputs MIC, LINE_L, LINE_R, AUXA_L, and AUXA_R should be capacitively coupled to their respective input signals. All have pull-up resistors to CMR.

ES1869 analog outputs AOUT_L and AOUT_R should be AC-coupled to an amplifier, volume control potentiometer, or line-level outputs.

PNP CONFIGURATION AND REGISTERS

Figure 20 shows the configuration register set that is discussed in the following pages. As shown below, the Card-Level registers supported by the ES1869 are the Card-Control Card-Level registers at addresses 00h-07h, and the Vendor-Defined Card-Level registers at addresses 20h-2Fh. The Card-Control Card-Level register at address 07h is a pointer to the Logical Device registers supported by the ES1869 (one set of registers for each logical device on the "card"). In the ES1869, there are six logical devices: the configuration device, the audio+FM+MPU-401 device, the joystick device, the CD-ROM device, the Modem device, and a user-defined General-Purpose device.

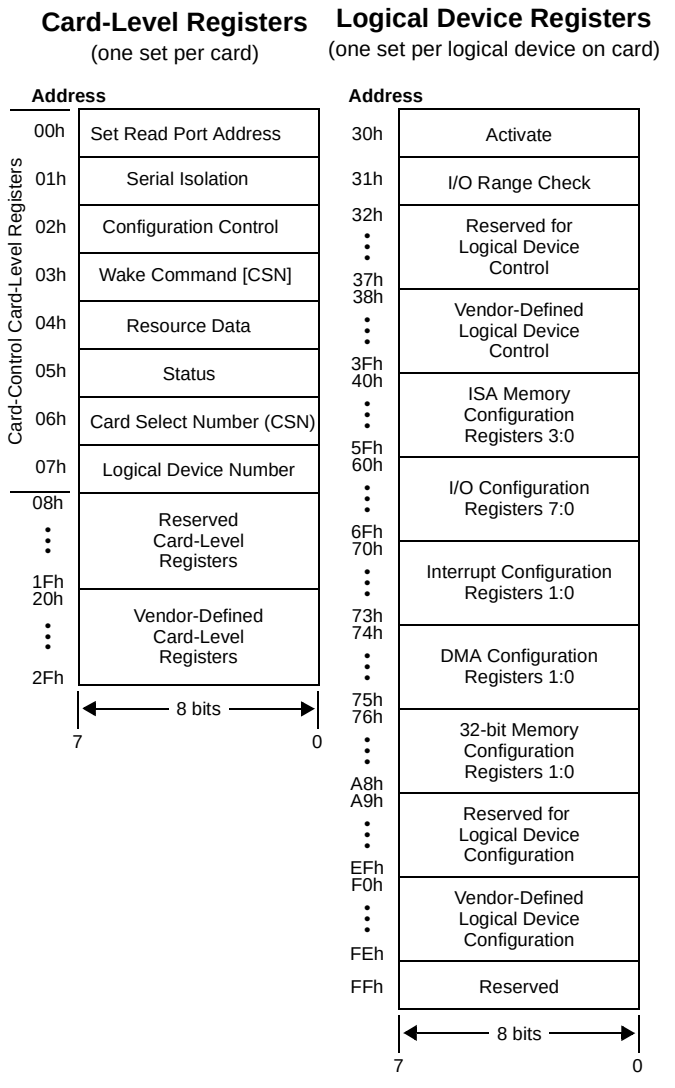


Figure 20 Configuration Register Set

Access to PnP Registers

Configuration Ports

To directly access the PnP registers, and bypass the PnP sequence, write a special key sequence to port 279h that depends on bits 6:5 of PnP register 25h, and conclude with two I/O writes to 279h to set the base address of the configuration ports. The key sequence also sets the activate bit for the configuration device.

Bypass Key

If PnP is not supported by the system, it is possible to bypass PnP by issuing a special "bypass key" to the ES1869 to force the configuration device to be enabled at a specific I/O address. The ES1869 must be in the "wait-for-key" Plug and Play state. The special key is 32 bytes long, written to the PnP address register (279h). Follow the bypass key immediately with two I/O writes to the PnP address register to set the low and high bytes of the address register of the configuration device. The bypass key also activates the configuration device. The address of the configuration device must be in the range 100h-FF8h, aligned on a multiple of 8. An "alias" of the audio device address can be used. For example, use E20h for the configuration device if the audio device address is at 220h.

The actual key sequence is determined by the state of bits 5 and 6 of Vendor-Defined Card-Level register 25h. These bits are both zero after reset, and are loaded from the seventh byte of the PnP ROM header (if the first byte of the header is 'A5'). The purpose of the bypass key is to handle the case where multiple instances of the ES1869 coexist in a single non-PnP system. It is recommended to try all four keys successively. The only difference between the four keys are the two least significant bits: XOR bits 1 and 0 of key #0 with bits 5 and 6 of register 25h to generate keys #1, #2, and #3.

NOTE: Perform the entire sequence with interrupts disabled to minimize the chance that an interrupt corrupt the sequence.

Register 25h, bits 6:5 = 0,0

```
66, a1, c2, f1, ea, e7, 71, aa
c7, 63, 33, 1b,  d, 96, db, 6d
a4, 50, 28, 16, 9b, 4d, b6, c9
f4, 78, 3e, 8d, d6, fb, 7f, 3d
<config_address_low>, <config_address_high>
```

Register 25h, bits 6:5 = 0,1

```
67, a0, c3, f0, eb, e6, 70, ab
c6, 62, 32, 1a,  c, 97, da, 6c
a5, 51, 29, 17, 9a, 4c, b7, c8
f5, 79, 3f, 8c, d7, fa, 7e, 3c
<config_address_low>, <config_address_high>
```

Register 25h, bits 6:5 = 1,0

```
64, a3, c0, f3, e8, e5, 73, a8
c5, 61, 31, 19,  f, 94, d9, 6f
a6, 52, 2a, 14, 99, 4f, b4, cb
f6, 7a, 3c, 8f, d4, f9, 7d, 3f
<config_address_low>, <config_address_high>
```

Register 25h, bits 6:5 = 1,1

```
65, a2, c1, f2, e9, e4, 72, a9
c4, 60, 30, 18,  e, 95, d8, 6e
a7, 53, 2b, 15, 98, 4e, b5, ca
f7, 7b, 3d, 8e, d5, f8, 7c, 3e
<config_address_low>, <config_address_high>
```

CAUTION: When using the bypass key method of address configuration, the address cannot be reliably relocated without reissuing the bypass key. Writing directly to Logical Device Number 0 register 60h to change the configuration address is unreliable. Use the bypass key to relocate the configuration address. Use this method for the initial address configuration as well as any subsequent change in the address configuration.

Card-Control Card-Level Registers (00h-07h)

Set RD_DATA Port (00h, R/W)

Bits 9:2 of the PnP RD_DATA port							
7	6	5	4	3	2	1	0

The PnP read port can be written only when the card is in Isolation mode. It is reset low by hardware reset. It can be read only from Configuration mode. Bits 1:0 of PnP read port are always one.

Serial Isolation (01h, R)

Data							
7	6	5	4	3	2	1	0

Read-only in isolation state. Used to read the serial identifier during card isolation process.

Config Control (02h, W)

					RESET_CSN	WFK	SWR
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
2	RESET_CSN	RESET_CSN command. 1 = Card's CSNs set to zero.
1	WFK	WAIT_FOR_KEY command. 1 = Enter wait-for-key state.
0	SWR	Software reset command. Does not work in wait-for-key state. 1 = Reset config registers to default.

Wake[CSN] (03h, W)

Data							
7	6	5	4	3	2	1	0

If data written is 00h and it:

- matches the CSN:
  this card goes from Sleep mode to Isolation mode.
- does not match the CSN:
  this card goes from Configuration mode to Sleep mode.

If the data written is non-zero, and it:

- matches the CSN:
  this card goes from Sleep mode to Configuration mode.
- does not match the CSN:
  this card goes from Isolation mode to Sleep mode.

Resource Data (04h, R)

Resource data							
7	6	5	4	3	2	1	0

Returns next byte of resource data, provided the status bit in register 05h has been polled before each byte read, indicating that data is ready. Only works in Configuration mode.

Status (05h, R)

Reserved							Status
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
0	Status	1 = Ready to read resource data in register 04h. Only works in Configuration mode. 0 = Resource data not available.

CSN (06h, R/W)

Card select number							
7	6	5	4	3	2	1	0

Read/write card select number. Write only works in Isolation mode. Causes transition to Configuration mode. Read only works in Configuration mode.

LDN (07h, R/W)

Logical device number							
7	6	5	4	3	2	1	0

Read/write logical device number. Only works in Configuration mode.

Vendor-Defined Card-Level Registers (20h-29h)

IRQB, IRQA (20h, R)

IRQB				IRQA			
7	6	5	4	3	2	1	0

Defines IRQ number assigned to B and A pins. Loaded from Configuration ROM Header after PnP reset. Unused IRQ pins should be assigned IRQ #1.

IRQD, IRQC (21h, R)

IRQD				IRQC			
7	6	5	4	3	2	1	0

Defines IRQ number assigned to D and C pins. Loaded from Configuration ROM Header after PnP reset. Unused IRQ pins should be assigned IRQ #1.

IRQF, IRQE (22h, R)

IRQF				IRQE			
7	6	5	4	3	2	1	0

Defines IRQ number assigned to F and E pins. Loaded from Configuration ROM Header after PnP reset. Unused IRQ pins should be assigned IRQ #1.

DRQB, DRQA (23h, R)

DRQB				DRQA			
7	6	5	4	3	2	1	0

Defines DRQ number assigned to B and A pins. Loaded from Configuration ROM header after PnP reset. Unused DRQ pins should be assigned DRQ #2.

DRQD, DRQC (24h, R)

DRQD				DRQC			
7	6	5	4	3	2	1	0

Defines DRQ number assigned to D and C pins. Loaded from Configuration ROM header after PnP reset. Unused DRQ pins should be assigned DRQ #2.

Configuration ROM Header 0 (25h, R)

DRQ latch	Motherboard/ card		GP		Modem	CD-ROM	MPU-401
7	6	5	4	3	2	1	0

Loaded from Configuration ROM header after PnP reset.

Bit Definitions:

Bits	Name	Description
7	DRQ latch	1 = DRQ latch feature enabled. 0 = DRQ latch feature disabled.
6:5	Mother-board/ card	Bit 6 Bit 5 0 0 motherboard 0 1 card 1 0 reserved 1 1 reserved
4:3	GP	Bit 4 Bit 3 0 0 GP is not present 0 1 GP is LDN 3,4,5,or 6; GP uses 4 addresses 1 0 GP uses 8 addresses 1 1 GP uses 16 addresses
2	Modem	1 = Modem is LDN 3, 4, or 5. 0 = Modem is not present.
1	CD-ROM	1 = CD-ROM is LDN 3 or 4. 0 = CD-ROM is not present.
0	MPU-401	1 = MPU-401 is LDN 3; interrupt is not shared with audio interrupt 1 or 2. 0 = MPU-401 is part of LDN 1; interrupt is shared with audio interrupt 1 or 2.

Configuration ROM Header 1 (26h, R)

Reserved			Ext DMA mask	Audio 2 DMA mask	Audio 1 DMA mask	GPO1	GPO0
7	6	5	4	3	2	1	0

Loaded from configuration ROM header after PnP reset.

Bit Definitions:

Bits	Name	Description
4	External DMA mask	1 = Enable external DMA mask. 0 = Disable.
3	Audio 2 DMA mask	1 = Enable audio 2 DMA mask. 0 = Disable.
2	Audio 1 DMA mask	1 = Enable audio 1 DMA mask. 0 = Disable.
1	GPO1	1 = GPO1 pin is external DACK, GPI is external DRQ. 0 = GPO1 pin is GPO1.
0	GPO0	1 = GPO0 pin is GPCS. 0 = GPO0 pin is GPO0.

Hardware Volume IRQ Number (27h, R)

Hardware volume IRQ number							
7	6	5	4	3	2	1	0

Hardware volume IRQ number (must be shared with audio 1 or audio 2). Reset to 0 by PnP reset.

MPU-401 IRQ Number (28h, R)

MPU-401 IRQ number							
7	6	5	4	3	2	1	0

MPU-401 IRQ number (alias address with register 70h of MPU-401 LDN 3).

PnP Enable (29h, R)

							PnP enable
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
0	PnP enable	1 = PnP enabled. 0 = PnP disabled. The ES1869 will not respond to any PnP commands. This bit is set high by hardware reset.

Logical Device Registers

Table 11 Logical Device Summary

LDN #	**Device**
LDN 0 (mandatory)	**Configuration device**
30h	Activate; bit 0 is activate bit.
31h	I/O Range Check.
60h	I/O base address, bits 11:8.If zero, this device is disabled. Eight locations.
61h	I/O base address, bits 7:3.
74h	DMA Channel Select 0 (default = 4).
75h	DMA Channel Select 1 (default = 4).
LDN 1 (mandatory)	**Audio device**
30h	Activate; bit 0 is activate bit.
31h	I/O Range Check.
60h	I/O base address of audio processor; bits 11:8. If zero, this device is not accessible. Sixteen locations.
61h	I/O base address of audio processor, bits 7:4.
62h	I/O base address of FM alias, bits 11:8. If zero, this device is not accessible. Four locations.
63h	I/O base address of FM alias, bits 7:2.
64h	I/O base address of MPU-401, bits 11:8. If zero, this device is not accessible. MPU-401 may also be accessible through LDN 3. Two locations.
65h	I/O base address of MPU-401, bits 7:2.
70h	Interrupt Request Channel 1 Select.
71h	Interrupt Request Type Select 1 (returns 2).
72h	Interrupt Request Channel 2 Select.
73h	Interrupt Request Type Select 2 (returns 2).
74h	DMA Channel 1 Select (default = 4).
75h	DMA Channel 2 Select (default = 4).
LDN 2 (mandatory)	**Joystick device**
30h	Activate; bit 0 is activate bit.
31h	I/O Range Check.
60h	I/O base address, bits 11:8. If zero, this device is disabled. One location.
61h	I/O base address, bits 7:0.
LDN 3 or LDN 1 I/O descriptor #2 (optional)	**MPU-401 device**
30h	Activate; bit 0 is activate bit.
31h	I/O Range Check.
60h	I/O base address, bits 11:8. If zero, this device is disabled. Two locations.
61h	I/O base address, bits 7:0.
70h	Interrupt Request MPU Select.
71h	Interrupt Request Type Select 0 (returns 2).
LDN 3 or 4 (optional)	**CD-ROM device**

Table 11 Logical Device Summary (Continued)

LDN #	Device
30h	Activate; bit 0 is activate bit.
31h	I/O Range Check.
60h	I/O base address of 1st address range, bits 11:8. If zero, this device is not accessible. Eight locations.
61h	I/O base address of 1st address range, bits 7:0.
62h	I/O base address of 2nd address range, bits 11:8. If zero, this device is not accessible. Two locations.
63h	I/O base address of 2nd address range, bits 7:0.
70h	Interrupt Request CD-ROM Select.
71h	Interrupt Request Type Select 0 (returns 2).
74h	DMA Channel Select for CD-ROM (default = 4).
LDN 3, 4, or 5 (optional)	**Modem device**
30h	Activate; bit 0 is activate bit.
31h	I/O Range Check.
60h	I/O base address, bits 11:8. If zero, this device is not accessible. Eight locations.
61h	I/O base address, bits 7:0.
70h	Interrupt Request Modem Select.
71h	Interrupt Request Type Select 0 (returns 2).
74h	DMA Channel Select for Modem (default = 4).
LDN 3, 4, 5, or 6 (optional)	**General-Purpose device**
30h	Activate; bit 0 is activate bit.
31h	I/O Range Check.
60h	I/O base address, bits 11:8. If zero, this device is not accessible. Four, eight, or sixteen locations.
61h	I/O base address, bits 7:0.
70h	Interrupt Request General-Purpose Device Select.
71h	Interrupt Request Type Select 0 (returns 2).
74h	DMA Channel Select for General-Purpose Device (default = 4).

LDN 0: Configuration Device

Activate **(30h, R/W)**

0	0	0	0	0	0	0	Activate
7	6	5	4	3	2	1	0

After reset or after a 1 is written to the reset bit in the card's configuration control bit, the default for this register is 0.

Bit Definitions:

Bits	Name	Description
0	Activate	1 = Activate. 0 = Deactivate (default).

I/O Range Check **(31h, R)**

0	0	0	0	0	0	Enable range check	Pattern select
7	6	5	4	3	2	1	0

This register verifies that the I/O range assigned to a logical device does not conflict with the I/O range used by another device.

Bit Definitions:

Bits	Name	Description
1	Enable range check	1 = Enable range check. 0 = Disable.
0	Pattern select	1 = 55h. 0 = AAh.

I/O Decoder 0 Base Address **(60h, R)**

0	0	0	0	A[11:8]			
7	6	5	4	3	2	1	0

This register is used to assign an I/O base address to I/O decoder 0 of the logical device. I/O base address, bits 11:8.

I/O Decoder 0 Base Address **(61h, R)**

A[7:3]					0	0	0
7	6	5	4	3	2	1	0

I/O base address, bits 7:3.

DMA Channel Select 0 **(74h, R)**

0	0	0	0	0	Data		
7	6	5	4	3	2	1	0

Returns 4 (no DMA channel selected).

Bit Definitions:

Bits	Name	Description
2:0	Data	Select which channel is in use for DMA 0.

DMA Channel Select 1 **(75h, R)**

0	0	0	0	0	Data		
7	6	5	4	3	2	1	0

Returns 4 (no DMA channel selected).

Bit Definitions:

Bits	Name	Description
2:0	Data	Select which channel is in use for DMA 1.

LDN 1: Audio Device

This device actually supports three functions: audio, FM, and MPU-401. Audio requires sixteen I/O locations, one interrupt which is shared with MPU-401, and two DMA channels. FM requires four I/O locations. MPU-401 requires two I/O locations.

Activate **(30h, R/W)**

0	0	0	0	0	0	0	Activate
7	6	5	4	3	2	1	0

After reset or after a 1 is written to the reset bit in the card's configuration control bit, the default for this register is 0.

Bit Definitions:

Bits	Name	Description
0	Activate	1 = Activate. 0 = Deactivate (default).

I/O Range Check **(31h, R)**

0	0	0	0	0	0	Enable range check	Pattern select
7	6	5	4	3	2	1	0

This register verifies that the I/O range assigned to a logical device does not conflict with the I/O range used by another device.

Bit Definitions:

Bits	Name	Description
1	Enable range check	1 = Enable range check. 0 = Disable.
0	Pattern select	1 = 55h. 0 = AAh.

Audio Processor I/O Base Address **(60h, R/W)**

0	0	0	0	A[11:8]			
7	6	5	4	3	2	1	0

I/O base address of audio processor, bits 11:8. Sixteen locations.

Audio Processor I/O Base Address **(61h, R/W)**

A[7:4]				0	0	0	0
7	6	5	4	3	2	1	0

I/O base address of audio processor, bits 7:4.

FM Alias I/O Base Address **(62h, R/W)**

0	0	0	0	A[11:8]			
7	6	5	4	3	2	1	0

I/O base address of FM alias, bits 11:8. Four locations.

FM Alias I/O Base Address **(63h, R/W)**

A[7:2]						0	0
7	6	5	4	3	2	1	0

I/O base address of FM alias, bits 7:2.

MPU-401 I/O Base Address **(64h, R/W)**

0	0	0	0	A[11:8]			
7	6	5	4	3	2	1	0

I/O base address of MPU-401, bits 11:8. (MPU-401 may also be accessible through LDN 3). Two locations.

MPU-401 I/O Base Address **(65h, R/W)**

A[7:2]						0	0
7	6	5	4	3	2	1	0

I/O base address of MPU-401, bits 7:2.

Interrupt Request Channel 1 Select **(70h, R/W)**

0	0	0	0	Data			
7	6	5	4	3	2	1	0

Interrupt request channel 1 select.

Bit Definitions:

Bits	Name	Description
3:0	Data	Select which interrupt used for channel 1 IRQ.

Interrupt Request Type Select 1 **(71h, R)**

0	0	0	0	0	0	1	0
7	6	5	4	3	2	1	0

Interrupt request type select 1. Returns 2 (low-to-high transition).

Interrupt Request Channel 2 Select (72h, R/W)

0	0	0	0	Data			
7	6	5	4	3	2	1	0

Interrupt request channel 2 select.

Bit Definitions:

Bits	Name	Description
3:0	Data	Select which interrupt used for channel 2 IRQ.

Interrupt Request Type Select 2 (73h, R)

0	0	0	0	0	0	1	0
7	6	5	4	3	2	1	0

Interrupt request type select 2. Returns 2 (low-to-high transition).

DMA Channel 1 Select (74h, R)

0	0	0	0	0	Data		
7	6	5	4	3	2	1	0

Returns 4 (no DMA channel selected).

Bit Definitions:

Bits	Name	Description
2:0	Data	Select which DMA channel is in use for channel 1 DRQ.

DMA Channel 2 Select (75h, R)

0	0	0	0	0	Data		
7	6	5	4	3	2	1	0

Returns 4 (no DMA channel selected).

Bit Definitions:

Bits	Name	Description
2:0	Data	Select which DMA channel is in use for channel 2 DRQ.

LDN 2: Joystick Device

Activate (30h, R/W)

0	0	0	0	0	0	0	Activate
7	6	5	4	3	2	1	0

After reset or after a 1 is written to the reset bit in the card's configuration control bit, the default for this register is 0.

Bit Definitions:

Bits	Name	Description
0	Activate	1 = Activate. 0 = Deactivate (default).

I/O Range Check (31h, R)

0	0	0	0	0	0	Enable range check	Pattern select
7	6	5	4	3	2	1	0

This register verifies that the I/O range assigned to a logical device does not conflict with the I/O range used by another device.

Bit Definitions:

Bits	Name	Description
1	Enable range check	1 = Enable range check. 0 = Disable.
0	Pattern select	1 = 55h. 0 = AAh.

I/O Decoder 0 Base Address (60h, R/W)

0	0	0	0	A[11:8]			
7	6	5	4	3	2	1	0

I/O base address, bits 11:8. One location.

I/O Decoder 0 Base Address (61h, R/W)

A[7:0]							
7	6	5	4	3	2	1	0

I/O base address, bits 7:0.

LDN 3: MPU-401 Device

The MPU-401, as an independent device, is optional; normally MPU-401 is part of the *Audio***Drive**® solution.

Activate **(30h, R/W)**

0	0	0	0	0	0	0	Activate
7	6	5	4	3	2	1	0

After reset or after a 1 is written to the reset bit in the card's configuration control bit, the default for this register is 0.

Bit Definitions:

Bits	Name	Description
0	Activate	1 = Activate. 0 = Deactivate (default).

I/O Range Check **(31h, R)**

0	0	0	0	0	0	Enable range check	Pattern select
7	6	5	4	3	2	1	0

This register verifies that the I/O range assigned to a logical device does not conflict with the I/O range used by another device.

Bit Definitions:

Bits	Name	Description
1	Enable range check	1 = Enable range check. 0 = Disable.
0	Pattern select	1 = 55h. 0 = AAh.

I/O Decoder 0 Base Address **(60h, R/W)**

0	0	0	0	A[11:8]			
7	6	5	4	3	2	1	0

I/O base address, bits 11:8. Two locations.

I/O Decoder 0 Base Address **(61h, R/W)**

A[7:0]							
7	6	5	4	3	2	1	0

I/O base address, bits 7:0.

Interrupt Request MPU Select **(70h, R/W)**

0	0	0	0	Data			
7	6	5	4	3	2	1	0

Interrupt request MPU select.

Bit Definitions:

Bits	Name	Description
3:0	Data	Select which interrupt used for MPU IRQ.

Interrupt Request Type Select 0 **(71h, R)**

0	0	0	0	0	0	1	0
7	6	5	4	3	2	1	0

Interrupt request type select 0. Returns 2 (low-to-high transition).

LDN 4: CD-ROM Device

The CD-ROM Device is optional. If present, it is LDN 3 or 4.

Activate **(30h, R/W)**

0	0	0	0	0	0	0	Activate
7	6	5	4	3	2	1	0

After reset or after a 1 is written to the reset bit in the card's configuration control bit, the default for this register is 0.

Bit Definitions:

Bits	Name	Description
0	Activate	1 = Activate. 0 = Deactivate (default).

I/O Range Check **(31h, R)**

0	0	0	0	0	0	Enable range check	Pattern select
7	6	5	4	3	2	1	0

This register verifies that the I/O range assigned to a logical device does not conflict with the I/O range used by another device.

Bit Definitions:

Bits	Name	Description
1	Enable range check	1 = Enable range check. 0 = Disable.
0	Pattern select	1 = 55h. 0 = AAh.

I/O Decoder 0 Base Address **(60h, R/W)**

0	0	0	0	A[11:8]			
7	6	5	4	3	2	1	0

I/O base address of first address range, bits 11:8. Eight locations.

I/O Decoder 0 Base Address **(61h, R/W)**

A[7:0]							
7	6	5	4	3	2	1	0

I/O base address of first address range, bits 7:0.

I/O Decoder 1 Base Address **(62h, R/W)**

0	0	0	0	A[11:8]			
7	6	5	4	3	2	1	0

I/O base address of second address range, bits 11:8. Two locations.

I/O Decoder 1 Base Address **(63h, R/W)**

A[7:0]							
7	6	5	4	3	2	1	0

I/O base address of second address range, bits 7:0.

Interrupt Request CD-ROM Select **(70h, R/W)**

0	0	0	0	Data			
7	6	5	4	3	2	1	0

Interrupt request CD-ROM select.

Bit Definitions:

Bits	Name	Description
3:0	Data	Select which interrupt used for CD-ROM IRQ.

Interrupt Request Type Select 0 **(71h, R)**

0	0	0	0	0	0	1	0
7	6	5	4	3	2	1	0

Interrupt request type select 0. Returns 2 (low-to-high transition).

DMA Channel Select for CD-ROM **(74h, R)**

0	0	0	0	0	Data		
7	6	5	4	3	2	1	0

Returns 4 (no DMA channel selected).

Bit Definitions:

Bits	Name	Description
2:0	Data	Select which DMA channel is in use for CD-ROM DRQ.

LDN 5: Modem Device

The Modem Device is optional. If present, it is LDN 3, 4, or 5.

Activate **(30h, R/W)**

0	0	0	0	0	0	0	Activate
7	6	5	4	3	2	1	0

After reset or after a 1 is written to the reset bit in the card's configuration control bit, the default for this register is 0.

Bit Definitions:

Bits	Name	Description
0	Activate	1 = Activate. 0 = Deactivate (default).

I/O Range Check **(31h, R)**

0	0	0	0	0	0	Enable range check	Pattern select
7	6	5	4	3	2	1	0

This register verifies that the I/O range assigned to a logical device does not conflict with the I/O range used by another device.

Bit Definitions:

Bits	Name	Description
1	Enable range check	1 = Enable range check. 0 = Disable.
0	Pattern select	1 = 55h. 0 = AAh.

I/O Decoder 0 Base Address **(60h, R/W)**

0	0	0	0	A[11:8]			
7	6	5	4	3	2	1	0

I/O base address of address range, bits 11:8.
Eight locations.

I/O Decoder 0 Base Address **(61h, R/W)**

A[7:0]							
7	6	5	4	3	2	1	0

I/O base address of address range, bits 7:0.

Interrupt Request Modem Select **(70h, R/W)**

0	0	0	0	Data			
7	6	5	4	3	2	1	0

Interrupt request modem select.

Bit Definitions:

Bits	Name	Description
3:0	Data	Select which interrupt used for modem IRQ.

Interrupt Request Type Select 0 **(71h, R)**

0	0	0	0	0	0	1	0
7	6	5	4	3	2	1	0

Interrupt request type select 0. Returns 2 (low-to-high transition).

DMA Channel Select for Modem **(74h, R)**

0	0	0	0	0	Data		
7	6	5	4	3	2	1	0

Returns 4 (no DMA channel selected).

Bit Definitions:

Bits	Name	Description
2:0	Data	Select which DMA channel is in use for Modem DRQ.

LDN 6: General-Purpose Device

The general-purpose I/O device is optional. If present, it is LDN 3, 4, 5, or 6.

Activate **(30h, R/W)**

0	0	0	0	0	0	0	Activate
7	6	5	4	3	2	1	0

After reset or after a 1 is written to the reset bit in the card's configuration control bit, the default for this register is 0.

Bit Definitions:

Bits	Name	Description
0	Activate	1 = Activate. 0 = Deactivate (default).

I/O Range Check **(31h, R)**

0	0	0	0	0	0	Enable range check	Pattern select
7	6	5	4	3	2	1	0

This register verifies that the I/O range assigned to a logical device does not conflict with the I/O range used by another device.

Bit Definitions:

Bits	Name	Description
1	Enable range check	1 = Enable range check. 0 = Disable.
0	Pattern select	1 = 55h. 0 = AAh.

I/O Decoder 0 Base Address **(60h, R/W)**

0	0	0	0	A[11:8]			
7	6	5	4	3	2	1	0

I/O base address of address range, bits 11:8. Four, eight, or sixteen locations.

I/O Decoder 0 Base Address **(61h, R/W)**

A[7:0]							
7	6	5	4	3	2	1	0

I/O base address of address range, bits 7:0.

Interrupt Request General-Purpose Device Select **(70h, R/W)**

0	0	0	0	Data			
7	6	5	4	3	2	1	0

Interrupt request general-purpose device select.

Bit Definitions:

Bits	Name	Description
3:0	Data	Select which interrupt used for general-purpose device IRQ.

Interrupt Request Type Select 0 **(71h, R)**

0	0	0	0	0	0	1	0
7	6	5	4	3	2	1	0

Interrupt request type select 0. Returns 2 (low-to-high transition).

DMA Channel Select for General-Purpose Device **(74h, R)**

0	0	0	0	0	Data		
7	6	5	4	3	2	1	0

Returns 4 (no DMA channel selected).

Bit Definitions:

Bits	Name	Description
2:0	Data	Select which DMA channel is in use for general-purpose device DRQ.

I/O PORTS

Port Summary

Table 12 I/O Ports for Configuration, Audio, FM, MPU-401, and Joystick Devices

Port	Read/Write	Function
Configuration Device		
Base+0h	Read/write	Configuration Register Address.
Base+1h	Read/write	Configuration Register Data.
Base+2h	Read/write	EEPROM Data register.
Base+3h	Read/write	EEPROM Command register.
Base+4h	Read/write	Reset EEPROM Address.
Base+5h	Read/write	Status register.
Base+6h	Read-only	Interrupt Status register.
Base+7h	Read/write	Interrupt Mask register.
Audio Device		
Base+0h - Base+3h	Read/write	20-voice FM synthesizer. Address and data registers.
Base+4h	Read/write	Mixer Address register (port for address of mixer controller registers).
Base+5h	Read/write	Mixer Data register (port for data to/from mixer controller registers).
Base+6h	Read/write	Audio reset and status flags.
Base+7h	Read/write	Power Management register. Suspend request and FM reset.
Base+8h - Base+9h	Read/write	11-voice FM synthesizer. Address and data registers.
Base+Ah	Read-only	Input data from read buffer for command/data I/O. Poll bit 7 of port Audio_Base+Eh to test whether the read buffer contents are valid.
Base+Ch	Read/write	Output data to write buffer for command/data I/O. Read embedded processor status.
Base+Eh	Read-only	Data available flag from embedded processor.
Base+Fh	Read/write	Address for I/O access to FIFO in Extended mode.
FM Device		
Base+0h - Base+3h	Read/write	20-voice FM synthesizer. Address and data registers.
MPU-401 Device		
Base+0h - Base+1h	Read/write	MPU-401 port (x=0,1,2, or 3) if enabled.
Joystick Device		
Base+0h	Read/write	Joystick.

Port Descriptions

Configuration Device

EEPROM Command Register (Config_Base+3h, R/W)

				EEPROM Command			
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description				
3:0	EEPROM Command	Bit 3	Bit 2	Bit 1	Bit 0	Function
		0	0	0	0	Write disable
		0	0	0	1	Write all
		0	0	1	0	Erase all
		0	0	1	1	Write enable
		0	1	0	0	Write
		1	0	0	0	Read
		1	1	0	0	Erase

Status Register (Config_Base+5h, R/W)

Reserved	EEPROM type	State	PNPOK	Rst seq busy
7 6	5 4	3 2	1	0

Bit Definitions:

Bits	Name	Description		
7:6	Reserved	Reserved.		
5:4	EEPROM type	Bit 5	Bit 4	Function
		0	0	Internal ROM
		0	1	128 x 8-bit
		1	0	256 x 8-bit
		1	1	512 x 8-bit
3:2	State	Bit 3	Bit 2	Function
		0	0	Wait-for-key
		0	1	Sleep
		1	0	Isolation
		1	1	Configure
1	PNPOK	PNPOK bit.		
0	Rst seq busy	Reset sequence busy bit.		

Interrupt Status Register (Config_Base+6h, R)

Reserved	GP	Modem	CD-ROM	MPU-401	H/W vol	Audio 2	Audio 1
7	6	5	4	3	2	1	0

Read this register to find out which ES1869 interrupt sources are active.

Bit Definitions:

Bits	Name	Description
7	Reserved	Reserved.
6	GP	General-Purpose. GPI input pin.
5	Modem	Modem. MMIRQ input pin AND'ed with inverse of MMIEB input.
4	CD-ROM	CD-ROM interface. CDIRQ input pin.
3	MPU-401	MPU-401. MPU-401 receive interrupt request AND'ed with bit 6 of mixer register 64h.
2	H/W vol	Hardware volume. Hardware volume interrupt request AND'ed with bit 1 of mixer register 64h.
1	Audio 2	Audio 2. Audio 2 interrupt request AND'ed with bit 6 of mixer register 7Ah.
0	Audio 1	Audio 1. Audio 1 interrupt request.

Interrupt Mask Register (Config_Base+7h, R/W)

Reserved	GP	Modem	CD-ROM	MPU-401	H/W vol	Audio 2	Audio 1
7	6	5	4	3	2	1	0

The mask bits of this register can be used to force the interrupt source to be zero without putting the interrupt pin in a high-impedance state. Each bit is AND'ed with the corresponding interrupt source. Set to all ones by hardware reset.

Bit Definitions:

Bits	Name	Description
7	Reserved	Reserved.
6	GP	General-Purpose interrupt mask bit.
5	Modem	Modem interrupt mask bit.
4	CD-ROM	CD-ROM interface interrupt mask bit.
3	MPU-401	MPU-401 interrupt mask bit.
2	H/W vol	Hardware volume interrupt mask bit.
1	Audio 2	Audio 2 interrupt mask bit.
0	Audio 1	Audio 1 interrupt mask bit.

Audio Device

Mixer Address Register (Audio_Base+4h, R/W)

X	X	A5	A4	A3	A2	A1	MXD
7	6	5	4	3	2	1	0

The ES1869 provides a means to read back the Mixer Address register. Reading back this register is useful for a "hot-key" application that needs to change the mixer while preserving the address register.

Mixer Data Register (Audio_Base+5h, R/W)

D7	D6	D5	D4	D3	D2	D1	D0
7	6	5	4	3	2	1	0

Reset and Status Flags (Audio_Base+6h, W)

0	0	0	0	0	0	FIFO reset	SW reset
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:2	–	Reserved. Always write 0.
1	FIFO reset	1 = Hold ES1869 FIFO in reset. 0 = Release ES1869 FIFO from reset. Bit 1 has no function for Compatibility mode.
0	SW reset	1 = Hold ES1869 in reset. 0 = Release ES1869 from reset.

Reset and Status Flags (Audio_Base+6h, R)

Act flag 2	Act flag 1	Act flag 0	Serial act flag	Digital power-down	MIDI modes	FIFO reset	SW reset
7	6	5	4	3	2	1	0

Bits 7:4 of port Audio_Base+6h can be used to monitor I/O activity to the ES1869.

Bits 7:5 are set high after any read from port Audio_Base+6h. Then specific I/O activity can set these bits low. When port Audio_Base+6h is read at a later time, these bits will indicate whether I/O activity has occurred between the reads from Audio_Base+6h.

In addition, bit 4 can be used to indicate if the DSP or ES689/ES69x serial interface is in use. Bit 4 is set high if bit 7 or bit 5 of mixer register 48h is high (software serial enable or serial reset). It is also set high if the ES689/ ES69x serial interface is active, which is a combination of bit 4 of mixer register 48h set high and MCLK (ES689/ ES69x serial bit clock) being high periodically.

Bit Definitions:

Bits	Name	Description
7	Act flag 2	Set low by I/O reads/writes to MPU-401 or FM ports.
6	Act flag1	Set low by I/O reads/writes to audio ports Audio_Base+Ch and Audio_Base+Eh.
5	Act flag 0	Set low by I/O writes to audio ports Audio_Base+2h, Base+3h, Base+6h, and Base+Ch. Set low by I/O reads from audio ports Audio_Base+2h, Base+3h, and Base+Ah. Also set low by DMA accesses to ES1869.
4	Serial act flag	1 = Serial activity flag. High if DSP serial mode is enabled (SE input pin is high or bits 7or 5 of register 48h is high) or if an external ES689/ ES69x is using MCLK/MSD to drive the FM DAC.
3	Digital power-down	0 = The ES1869 digital section is currently powered-down (power mode 0 and 1). Power to the analog section is controlled by bit 3 of Audio_Base+7h.
2	MIDI mode	1 = The ES1869 is processing a MIDI command 30h, 31h, 34h, or 35h. In this mode, the ES1869 is monitoring serial input. Powering-down may cause a loss of data. The ES1869 does not automatically wake up on serial input on the MSI pin.
1	FIFO reset	FIFO Reset bit.
0	SW reset	Software Reset bit.

Power Management Register (Audio_Base+7h, R/W)

Suspend request	GPI	FM synth reset	0	Analog power-down	Power-down request	GPO1	GPO0
7	6	5	4	3	2	1	0

Reading or writing port Audio_Base+7h does not automatically wake up the ES1869.

Bit Definitions:

Bits	Name	Description
7	Suspend request	Pulse high, then low to request suspend.
6	GPI	Read-only. Indicates the status of the GPI pin.
5	FM synth reset	1 = Hold FM synthesizer in reset. 0 = Release FM synthesizer from reset.
4	–	Reserved. Always write 0.
3	Analog power-down	1 = Set Analog_Stays_On 0 = Clear Analog_Stays_On
2	Power-down request	Pulse high, then low to request power-down.

Bits	Name	Description
1	GPO1	1 = Set GPO1 high (Hardware reset condition). 0 = Clear GPO1.
0	GPO0	1 = Set GPO0 high. 0 = Clear GPO0 (Hardware reset condition).

Read Data Register (Audio_Base+Ah, R)

D7	D6	D5	D4	D3	D2	D1	D0
7	6	5	4	3	2	1	0

Read data from embedded audio processor. Poll bit 7 of port Audio_Base+Eh to test whether the register contents are valid.

Write Data Register (Audio_Base+Ch, W)

D7	D6	D5	D4	D3	D2	D1	D0
7	6	5	4	3	2	1	0

Write data to embedded audio processor. Sets bit 7 of port Audio_Base+Ch high (write buffer not available) until data is processed by the ES1869.

Read Data Register (Audio_Base+Ch, R)

D7	D6	D5	D4	D3	D2	D1	D0
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7	BUSY flag	1 = write buffer not available or ES1869 busy. 0 = write buffer available or ES1869 not busy.
6		1 = Data available in read buffer. 0 = Data not available in read buffer. This flag is reset by a read from port Audio_Base+Ah.
5		1 = Extended mode FIFO Full (256 bytes loaded).
4		1 = Extended mode FIFO Empty (0 bytes loaded).
3		1 = FIFO Half Empty, Extended mode flag.
2		1 = ES1869 processor generated an interrupt request (e.g., from Compatibility mode DMA complete).
1		1 = Interrupt request generated by FIFO Half Empty flag change. Used by programmed I/O interface to FIFO in Extended mode.
0		1 = Interrupt request generated by DMA counter overflow in Extended mode.

Read Buffer Status Register (Audio_Base+Eh, R)

D7	D6	D5	D4	D3	D2	D1	D0
7	6	5	4	3	2	1	0

A read from port Audio_Base+Eh will reset any interrupt request.

Bit Definitions:

Bits	Name	Description
7		1 = Data available in read buffer. 0 = Data not available in read buffer. This flag is reset by a read from port Audio_Base+Ah.

Programmed I/O Access to FIFO Register (Audio_Base+Fh, R/W)

D7	D6	D5	D4	D3	D2	D1	D0
7	6	5	4	3	2	1	0

This port can be used to replace Extended mode DMA with programmed I/O.

FM Device

The FM synthesizer operates in two different modes: Emulation mode and Native mode. In Emulation mode the FM synthesizer is fully compatible with the OPL3 FM synthesizer. In Native mode the FM synthesizer has increased capabilities and performance for more realistic music. The following register descriptions are for Emulation mode only.

FM Status (FM_Base+0h, R)

IRQ	FT1	FT2	0	0	0	0	0
7	6	5	4	3	2	1	0

Reading this register returns the overflow flags for timers 1 and 2 and the “interrupt request” from these timers (this is not a real interrupt request but is supported as a status flag for backward compatibility with the OPL3 FM synthesizer).

FM Low Bank Address (FM_Base+0h, W)

A7	A6	A5	A4	A3	A2	A1	A0
7	6	5	4	3	2	1	0

Low bank register address.

NOTE: Any write to this register will also put the FM synthesizer in Emulation mode if it is currently in Native mode.

FM Data Write **(FM_Base+1h, W)**

D7	D6	D5	D4	D3	D2	D1	D0
7	6	5	4	3	2	1	0

FM register write. The data written to FM_Base+1h is written to the current address FM register. Note that register writes must follow the timing requirements of the OPL3 FM synthesizer.

FM High Bank Address **(FM_Base+2h, W)**

A7	A6	A5	A4	A3	A2	A1	A0
7	6	5	4	3	2	1	0

High bank register address.

FM Data Write **(FM_Base+3h, W)**

D7	D6	D5	D4	D3	D2	D1	D0
7	6	5	4	3	2	1	0

FM register write. Writing to this register in Emulation mode is the same as writing to register FM_Base+1h.

MPU-401 Device

MPU-401 Data **(MPU_Base+0h, R/W)**

D7	D6	D5	D4	D3	D2	D1	D0
7	6	5	4	3	2	1	0

This register is used to read data from the MPU-401 receive FIFO or a command acknowledge byte (0FEh). This register is also used to write data to the MPU-401 transmit FIFO.

MPU-401 Command **(MPU_Base+1h, W)**

D7	D6	D5	D4	D3	D2	D1	D0
7	6	5	4	3	2	1	0

The MPU-401 device accepts only two commands:

FFh	Reset/return to Smart mode. This command generates an acknowledge byte if received when already in Smart mode.
3Fh	Go to UART mode. This command generates an acknowledge byte if received while in Smart mode. It is ignored if the device is already in UART mode.

MPU-401 Status **(MPU_Base+1h, R)**

-RR	-TR	X	X	X	X	X	X
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7		0 = read data available in the receive FIFO, or pending acknowledge byte to be read (0FEh).
6		0 = there is room in the transmit FIFO to accept another byte.

Joystick Device

The joystick device uses only a single I/O port. The device can function in one of two modes: Analog mode or Digital mode. The use of this I/O port is different depending on the mode. This section describes Analog mode. Digital mode is described in “Joystick / MIDI External Interface” on page 23.

Joystick_Base+0h **(W)**

X	X	X	X	X	X	X	X
7	6	5	4	3	2	1	0

Any value written to the Joystick_Base+0h port will restart the timing sequence. This should be done before reading the timer status flags.

Joystick_Base+0h **(R)**

SWD	SWC	SWB	SWA	TD	TC	TB	TA
7	6	5	4	3	2	1	0

SW(A-D) return the current state of the joystick switch inputs. T(A-D) return the current state of the four one-shot timers connected to the X and Y resistors of the dual joysticks.

PROGRAMMING THE ES1869

Identifying the ES1869

The ES1869 may be identified by reading mixer register 40h successively. It returns the following values on four successive reads:

18h, 69h, A[11:0], A[7:0]

where 18h and 69h are data reads indicating the part number (1869), and A[11:0] is the base address of the configuration device.

Resetting the ES1869 by Software

The chip can be reset in either of two ways: hardware and software reset. The hardware reset signal comes from the ISA bus. Software reset is controlled by bit 0 of port Audio_Base+6h.

To reset the ES1869 by software:

1. Write 1h to port Audio_Base+6h.
2. Delay a short period, for example, by reading back Audio_Base+6h.
3. Write 0h to port Audio_Base+6h.
4. In a loop that lasts at least 1 millisecond, poll port Audio_Base+Eh bit 7 for Read-Data-Available.

   If bit 7 is high, read the byte from port Audio_Base+Ah. Exit the loop if the content is 0AAh; otherwise, continue polling.

Both hardware and software reset:

- Disable Extended mode.
- Reset the timer divider and filter registers for 8 kHz sampling.
- Stop any DMA transaction in progress.
- Clear any active interrupt request.
- Disable voice input of mixer (see the D1h/ D3h commands).
- Reset Compatibility mode and Extended mode DMA counters to 2048 bytes.
- Set analog direction to be DAC, with the DAC value set to mid-level.
- Set input volume for 8-bit recording with Automatic Gain Control (AGC) to maximum.
- Set input volume for 16-bit recording to mid-range

In addition to performing actions on the above list, a hardware reset resets all mixer registers to default values.

Modes of Operation

The ES1869 can operate the first audio channel in one of two modes: Compatibility mode or Extended mode.

In both modes, a set of mixer and controller registers enables application software to control the analog mixer, record source, and output volume. Programming the ES1869 Enhanced Mixer is described later in this document. See “Programming the ES1869 Mixer” on page 54.

Compatibility Mode Description

The first mode, Compatibility mode, is compatible to the Sound Blaster Pro. This is the default mode after reset. In this mode, the ES1869 microcontroller is an intermediary in all functions between the ISA bus and the CODEC. The ES1869 microcontroller performs limited FIFO functions using 64 bytes of internal memory.

Extended Mode Description

The ES1869 also supports an Extended mode of operation. In this case, a 256-byte FIFO is used as an intermediary between the ISA bus and the ADC and DAC Control registers, and various Extended mode controller registers are used for control. The ES1869 microcontroller is mostly idle in this mode. DMA control is handled by dedicated logic. Programming for Extended mode operation requires accessing various control registers with ES1869 commands. Some of these commands are also useful for Compatibility mode, such as those that configure DMA and IRQ channels.

Table 13 Comparison of Operation Modes

	Compatibility Mode (Sound Blaster Pro)	**Extended Mode**
Sound Blaster Pro compatible	Yes	No
FIFO Size	64 bytes (firmware managed)	256 bytes (hardware managed)
Mono 8-bit ADC, DAC	Yes, to 44 kHz	Yes, to 44 kHz
Mono 16-bit ADC, DAC	Yes, to 22 kHz	Yes, to 44 kHz
Stereo 8-bit DAC	Yes, to 22 kHz	Yes, to 44 kHz
Stereo 8-bit ADC	Yes, to 22 kHz	Yes, to 44 kHz
Stereo 16-bit DAC	Yes, to 11 kHz	Yes, to 44 kHz
Stereo 16-bit ADC	No	Yes, to 44 kHz
Signed/Unsigned Control	No	Yes
Automatic Gain Control during recording	Firmware controlled, to 22 kHz, mono only	No
Programmed I/O block transfer for ADC and DAC	No	Yes
FIFO status flags	No	Yes
Auto reload DMA	Yes	Yes
Time base for programmable timer	1 MHz or 1.5 MHz	800 kHz or 400 kHz
ADC and DAC jitter	± 2 microseconds	None

Mixing Modes Not Recommended

Avoid mixing Extended mode commands with Compatibility mode commands. The Audio 1 DAC Enable/ Disable commands D1h and D3h are safe to use when using Extended mode to process ADC or DAC. However, other Compatibility mode commands can cause problems. The Extended mode commands may be used to set up the DMA or IRQ channels before entering Compatibility mode.

Data Formats

This section briefly describes the different audio data formats used by the ES1869.

Compressed Data Formats

The ES1869 supports two types of compressed sound DAC operations: **ESPCM**®, which uses a variety of proprietary compression techniques developed by ESS Technology, and ADPCM, which is supported by many other sound cards but is of a lower quality.

Both ADPCM and **ESPCM**® are only transferred using DMA transfer. The first block of a multiple-block transfer uses a different command than subsequent blocks. The first byte of the first block is called the reference byte.

Use Compatibility mode when transferring compressed data.

Sound Blaster Pro Compatible Data Formats

There are four formats available from the combination of the following two options:

- 8-bit or 16-bit
- Mono or stereo

The 8-bit samples are unsigned, ranging from 0h to 0FFh, with the DC-levels around 80h.

16-bit samples are unsigned, ranging from 0000h to 0FFFFh, with the DC-levels around 8000h.

Stereo DMA Transfers in Compatibility Mode

Stereo DMA transfers are only available using DMA rather than Direct mode commands.

To perform a stereo DMA transfer, first set bit 1 of mixer register 0Eh high. Then set the timer divider to twice the per-channel sample rate.

The maximum stereo transfer rate for 8-bit data is 22 kHz per channel, so for this case program the timer divider as if it were for 44 kHz mono. The maximum stereo transfer rate for 16-bit data is 11 kHz per channel. Stereo ADC transfers for 16-bit data are not allowed in Compatibility mode.

For 8-bit data, the ES1869 expects the first byte transferred to be for the right channel, and subsequent bytes to alternate left, right etc.

For 16-bit data, the ES1869 expects DMA transfers to be a multiple of 4, with repeating groups in the order:

1. left low byte
2. left high byte
3. right low byte
4. right high byte

ES1869 Data Formats (Extended Mode and Audio 2)

There are eight formats available from the combination of the following three options:

- Mono or stereo
- 8-bit or 16-bit
- Signed or unsigned

For stereo data, the data stream always alternates channels in successive samples: first left, then right. For 16-bit data, the low byte always precedes the high byte.

Sending Commands During DMA Operations

It is useful to understand the detailed operation of sending a command during DMA.

The ES1869 uses the Audio 1 FIFO for DMA transfers to/from the CODEC. When the FIFO is full (in the case of DAC) or empty (in the case of ADC), DMA requests are temporarily suspended and the Busy flag (bit 7 of port Audio_Base+Ch) is cleared. This opens a window of opportunity to send a command to the ES1869. Commands such as D1h and D3h which control the Audio 1 DAC mixer input enable/disable status, and command D0h, which suspends or pauses DMA, are acceptable to send during this window.

The ES1869 chip sets the Busy flag when the command window is no longer open. Application software must send a command within 13 microseconds after the Busy flag goes high or the command will be confused with DMA data. Sending a command within the command window is easy if polling is done with interrupts disabled.

As an example of sending a command during DMA, consider the case where the application wants to send command D0h in the middle of a DMA transfer. The application disables interrupts and polls the Busy flag. Because of the FIFO and the rules used for determining the command window, it is possible for the current DMA transfer to complete while waiting for the Busy flag to clear. In this event, the D0h command has no function, and a pending interrupt request from the DMA completion is generated.

The interrupt request can be cleared by reading port Audio_Base+Eh before enabling interrupts or having a way of signaling the interrupt handler that DMA is inactive so that it does not try to start a new DMA transfer.

Figure 21 shows timing considerations for sending a command.

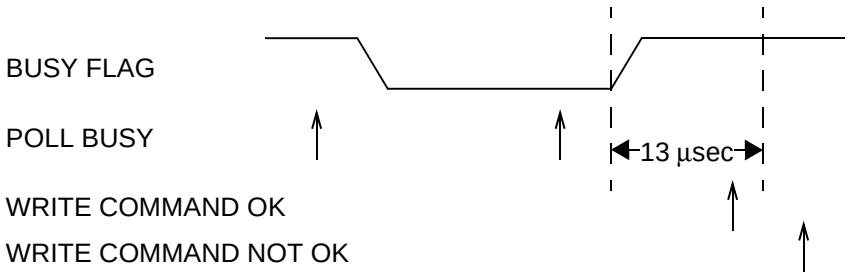


Figure 21 Command Transfer Timing

Compatibility Mode Programming

This section describes Compatibility mode programming.

Compatibility Mode DAC Operation

1. Reset

   Write 1h to port Audio_Base+6h.

   To play a new sound without resetting the ES1869 beforehand, when the status of the analog circuits is not clear, mute the input to the mixer with command D3h to prevent pops.

2. Enable stereo mode (optional).

   Set bit 1 of mixer register 0Eh high. Use only DMA mode. Clear bit 1 of mixer register 0Eh after the DAC transfer.

3. Set sample rate and filter clock.

   Use commands 40h or 41h to set the sample rate and filter clock divider. To set the filter clock to be independent from the sample rate, use command 42h in addition to 40h or 41h.

For stereo transfers, set the timer divider to twice the per-channel sample rate. The maximum stereo transfer rate for 8-bit data is 22 kHz per channel; so for this case, program the first timer divider as if you were transferring data at 44 kHz mono. The maximum stereo transfer rate for 16-bit data is 11 kHz per channel.

4. Set the block size. Only use this command (48h) with High-Speed DMA transfer modes (commands 90h and 91h).
5. Configure the system interrupt controller and system DMA controller.
6. Start DMA.

   Start the DMA transfer by sending the command for the desired transfer type and data length. The uncompressed modes are shown in Table 14. See Table 26 for a description of the commands in addition to the commands for DMA transfers of compressed data.

Table 14 Uncompressed DAC Transfer Modes

DAC DMA Transfer Mode	Data Length	Command
Direct	8-bit	10h
	16-bit	11h
DMA mode Normal	8-bit	14h
	16-bit	15h
High-Speed	8-bit	91h
DMA mode Auto-Initialize	8-bit	1Ch
	16-bit	1Dh
High-Speed	8-bit	90h

7. Delay approximately 100 milliseconds to allow the analog circuits to settle, then enable the Audio 1 DAC input to mixer with command D1h.
8. During DMA.

   For Auto-Initialize mode, it is not necessary to send any commands to the ES1869 at interrupt time, except to read Audio_Base+Eh to clear the interrupt request.

   For Normal mode, initialize the system DMA controller with the address and count of the next block size if it changes. Use command 48h. To start the next transfer, use command D4h.

   To stop DMA after the current auto-initialize block is finished, use command D0h.

   Commands such as D1h and D3h, which control the Audio 1 DAC mixer input enable/disable status, and command D0h, which suspends DMA, are acceptable to send during DMA transfers. These commands can only be sent during certain windows of opportunity. See “Stereo DMA Transfers in Compatibility Mode” on page 45.
9. After DMA is finished, restore the system interrupt controller and DMA controller to their idle state. Monitor the FIFO Empty status flag in port Audio_Base+Ch to be sure that data transfer is completed. Delay 25 milliseconds to let the filter outputs settle to DC-levels, then disable the Audio 1 DAC input to the mixer with command D3h.
10. Issue another software reset to the ES1869 to initialize the appropriate registers.

Compatibility Mode ADC Operation

ES1869 analog circuitry is switched from the DAC direction to the ADC direction by the first direct or DMA mode ADC command (2xh). Discard the first 25 to 100 milliseconds of samples because pops might occur in the data due to the change from the DAC to ADC direction. In the ADC direction the voice input to the mixer is automatically muted.

1. Reset

   Write 1h to port Audio_Base+6h.

   To play a new sound without resetting the ES1869 beforehand, when the status of the analog circuits is not clear, mute the input to the mixer with command D3h to prevent pops.
2. Select the input source using register 0Ch

   Sound Blaster Pro has three recording sources: microphone, line, and auxiliary A (CD). Microphone input is the default source after any reset.

   The ES1869 has four recording sources: microphone, line, auxiliary A (CD), and mixer. Use mixer register 1Ch to choose the additional source.
3. Program the input volume.

   The selected source passes through an input volume stage that can be programmed with 16 levels of gain from 0 to +22.5 dB in steps of 1.5 dB. In 8-bit recordings (other than High-Speed mode), the volume stage is controlled by the ES1869 firmware for the purposes of automatic gain control (AGC). In 16-bit recordings as well as High-Speed mode 8-bit recordings, the input volume stage is controllable from application software. Use command DDh to change the input volume level from 0 to 15. The reset default is mid-range, 8.
4. Enable stereo mode (optional).

   Set bit 1 of mixer register 0Eh high. Use only DMA mode. Clear bit 1 of mixer register 0Eh after the ADC transfer.

5. Set sample rate and filter clock.

   Use commands 40h or 41h to set the sample rate and filter clock divider. If you want to set the filter clock to be independent from the sample rate, use command 42h in addition to 40h or 41h.

   For stereo transfers, set the timer divider to twice the per-channel sample rate. The maximum stereo transfer rate for 8-bit data is 22 kHz per channel; so for this case, program the first timer divider as if you were transferring data at 44 kHz mono. The maximum stereo transfer rate for 16-bit data is 11 kHz per channel.

6. Set the block size. Only use this command (48h) with High-Speed DMA transfer modes (commands 98h and 99h).
7. Configure the system interrupt controller and system DMA controller.
8. Start DMA.

   Start the DMA transfer by sending the command for the desired transfer type and data length. The uncompressed modes are shown in Table 15. See Table 26 for a description of the commands in addition to the commands for DMA transfers of compressed data.

Table 15 Uncompressed ADC Transfer Modes

ADC DMA Transfer Mode	Data Length	Command
Direct	8-bit	20h
	16-bit	21h
DMA mode Normal	8-bit	24h
	16-bit	25h
High-Speed	8-bit	99h
DMA mode Auto-Initialize	8-bit	2Ch
	16-bit	2Dh
High-Speed	8-bit	98h

9. Delay approximately 100 milliseconds to allow the analog circuits to settle, then enable the Audio 1 DAC input to mixer with command D1h.
10. During DMA.

    For Auto-Initialize mode, it is not necessary to send any commands to the ES1869 at interrupt time, except to read Audio_Base+Eh to clear the interrupt request.

    For Normal mode, initialize the system DMA controller with the address and count of the next block size if it changes. Use command 48h. To start the next transfer, use command D4h.

    To stop DMA after the current auto-initialize block is finished, use command D0h.

    Commands such as D0h, which suspends DMA, are acceptable to send during DMA transfers. These commands can only be sent during certain windows of opportunity. See “Writing Commands to ES1869 Controller Registers” on page 48.

11. After DMA is finished, restore the system interrupt controller and DMA controller to their idle state. Monitor the FIFO Empty status flag in port Audio_Base+Ch to be sure that data transfer is completed.
12. Issue another software reset to the ES1869 to initialize the appropriate registers.

The maximum sample rate for Direct mode ADC is 22 kHz.

The maximum sample rate for DMA ADC for both 8-bit and 16-bit is 22 kHz, using commands 24h, 25h, 2Ch, or 2Dh.

There is a special High-Speed mode for ADC that allows 8-bit sampling up to 44 kHz. This mode uses commands 98h (auto-initialize) and 99h (normal). No AGC is performed as the input volume is controlled with command DDh.

Extended Mode Programming

This section describes Extended mode programming.

Commanding ES1869 Controller Registers

Controller registers are written to and read from using commands sent to ports Audio_Base+Ch and Audio_Base+Ah.

Commands of the format Axh, Bxh, and Cxh, where x is a numeric value, are used for Extended mode programming of the first audio channel.

Commands of the format Ax and Bx are used to access the ES1869 controller registers. For convenience, the registers are named after the commands used to access them. For example “register A4h,” the Audio 1 Transfer Count Reload (low-byte) register, is written to by “command A4h.”

Enabling Extended Mode Commands

After any reset, and before using any Extended mode commands first send command C6h to enable Extended mode commands.

ES1869 Command/Data Handshaking Protocol

This section describes how to write commands to and read data from the ES1869 controller registers.

Writing Commands to ES1869 Controller Registers

Commands written to the ES1869 enter a write buffer. Before writing the command, make sure the buffer is not busy.

Bit 7 of port Audio_Base+Ch is the ES1869 Busy flag. It is set when the write buffer is full or when the ES1869 is otherwise busy (for example, during initialization after reset or during Compatibility mode DMA requests).

To write a command or data byte to the ES1869 microcontroller:

1. Poll bit 7 of port Audio_Base+Ch until it is clear.
2. Write the command/data byte to port Audio_Base+Ch.

The following is an example of writing to ES1869 controller registers. To set up the Audio 1 Transfer Count Reload register to F800h, send the following command/data bytes:

```
A4h, 00h; register A4h = 0h
A5h, F8h; register A5h = F8h
```

NOTE: The port Audio_Base+Ch write buffer is shared with Compatibility mode DMA write operations. When DMA is active, the Busy flag is cleared during windows of time when a command can be received. Normally, the only commands that should be sent during DMA operations are Dxh commands such as DMA pause/continue and Audio 1 DAC enable/disable. In this situation it is recommended to disable interrupts between the time that the Busy bit is polled and the command is written. Also, minimize the time between these instructions. See “Sending Commands During DMA Operations” on page 46 for more information.

Reading the Read Data Buffer of the ES1869

Command C0h is used to read the ES1869 controller registers used for Extended mode. Send command C0h followed by the register number, Axh or Bxh. For example, to read register A4h, send the following command bytes:

```
C0h, A4h
```

Then poll the Read-Data-Buffer-Status bit, bit 7 of port Audio_Base+Eh, before reading the register contents from port Audio_Base+Ah.

The Read-Data-Buffer-Status flag can be polled by reading bit 7 of port Audio_Base+Eh. When a byte is available, the bit is set high.

NOTE: Any read of port Audio_Base+Eh also clears any active interrupt request from the ES1869. An alternate way of polling the Read-Data-Buffer-Status bit is through bit 6 of port Audio_Base+Ch, which is the same flag. The Read-Data-Buffer-Status flag is cleared automatically by reading the byte from port Audio_Base+Ah.

Extended Mode Audio 1 DAC Operation

Follow the steps below to program the first audio channel for Extended mode DAC operation:

1. Reset

   Write 3h to port Audio_Base+6h, instead of 1h as in Compatibility mode. Bit 1 high specifically clears the FIFO. The remainder of the software reset is identical to Compatibility mode. Reset disables the Audio 1 DAC input to the mixer. This is intended to mask any pops created during the setup of the DMA transfer.

2. After the reset, send command C6h to enable Extended mode commands.
3. Program direction and type: registers B8h, A8h, and B9h:

   Register B8h: set bit 2 low for Normal DMA mode, high for Auto-Initialize DMA mode. Leave bit 3 low for the CODEC to run in the DAC direction.

   Register A8h: read this register to preserve the bits and then modify only bits 1 and 0:

   Bits 1:0 10: Mono

   Bits 1:0 01: Stereo

   Set register B9h:

   Bits 1:0 00: Single transfer DMA.

   Bits 1:0 01: Demand Transfer DMA:
   2 bytes per DMA request.

   Bits 1:0 11: Demand transfer DMA:
   4 bytes per DMA request.

4. Clocks and counters: registers A1h, A2h, A4h and A5h:

   Register A1h: Sample Rate Clock Divider
   Register A2h: Filter Clock Divider
   Registers A4h/A5h: Audio 1 Transfer Count Reload register low/high byte, two's complement

5. Initialize and configure DACs: registers B6h and B7h: See Table 16.

   Register B6h: 80h for signed data and 00h for unsigned data. This also initializes the CODEC for DAC transfer.

   Register B7h: programs the FIFO (16-bit/8-bit, signed/unsigned, stereo/mono).

Table 16 Command Sequences for DMA Playback

Mono	Stereo	8-bits	16-bits	Unsigned	Signed	Sequence
X		X		X		Reg B6h = 80h, Reg B7h = 51h, Reg B7h = D0h
X		X			X	Reg B6h = 00h, Reg B7h = 71h, Reg B7h = F0h
X			X	X		Reg B6h = 80h, Reg B7h = 51h, Reg B7h = D4h
X			X		X	Reg B6h = 00h, Reg B7h = 71h, Reg B7h = F4h
	X	X		X		Reg B6h = 80h, Reg B7h = 51h, Reg B7h = 98h
	X	X			X	Reg B6h = 00h, Reg B7h = 71h, Reg B7h = B8h
	X		X	X		Reg B6h = 80h, Reg B7h = 51h, Reg B7h = 9Ch
	X		X		X	Reg B6h = 00h, Reg B7h = 71h, Reg B7h = BCh

6. Enable/select DMA channel and IRQ channel, registers B1h and B2h:

   Register B1h: Interrupt Configuration register.
   Make sure bits 4 and 6 are high. Clear bits 7 and 5.

   Register B2h: DRQ Configuration register.
   Make sure bits 4 and 6 are high. Clear bits 7 and 5.

7. Configure system interrupt controller and DMA controller.
8. To start DMA:

   Set bit 0 of register B8h high while preserving all other bits.

9. Delay approximately 100 milliseconds to allow analog circuits to settle, then enable the Audio 1 DAC input to mixer with command D1h.
10. During DMA

    For Auto-Initialize transfers, read Audio_Base+Eh to clear the interrupt request. Do not send any other commands to the ES1869 at interrupt time.

    For Normal mode, initialize the system DMA controller with the address and count of the next block to transfer. Update the ES1869 Transfer Count registers if the count is changed. To start the next transfer, clear bit 0 of register B8h, then set it high again.

    To stop a DMA transaction in progress, clear bit 0 of register B8h. To stop a DMA transaction after the current auto-initialize block is finished, clear bit 2 of register B8h, wait for the interrupt, and then clear bit 0 of register B8h.

11. After DMA is finished:

    Restore the system interrupt controller and DMA controller to their idle state. Monitor the FIFO Empty status flag in port Audio_Base+Ch to be sure data transfer is completed. A delay of 25 milliseconds is required to let the filter outputs settle to DC-levels, then disable the first DMA DAC input to the mixer with command D3h.

12. Finally:

    Issue another software reset to the ES1869 to initialize the appropriate registers.

Extended Mode Audio 1 ADC Operation

Follow the steps below to program the first audio channel for Extended mode ADC operation:

NOTE: In Extended mode, there is no Automatic Gain Control (AGC) performed while recording. If AGC is necessary, use 16-bit recordings and perform AGC in system software.

1. Reset

   Write 3h to port Audio_Base+6h instead of 1h as in Compatibility mode. Bit 1 high specifically clears the FIFO. The remainder of the software reset is identical to Compatibility mode. Reset disables the Audio 1 DAC input to the mixer. This is intended to mask any pops created during the setup of the DMA transfer.

2. Send command C6h to enable Extended mode commands.
3. Select the input source:

   The ES1869 has four recording sources: microphone, line, auxiliary A, and mixer. The mixer source can be the playback mixer or the record mixer. Bits 4:3 of mixer register 7Ah selects the mixer source. The record mixer is the default. Microphone input is the default after any reset. Select the source using the mixer control register 1Ch.

4. Program input volume register B4h.
5. Program direction and type: registers B8h, and A8h:

Register B8h: set bit 3 high to program the CODEC for the ADC direction. Set bit 2 low for Normal DMA mode, high for Auto-Initialize DMA mode.

At this point the direction of the analog circuits is ADC rather than DAC. Unless the recording monitor is enabled, there will be no output from AOUT_L or AOUT_R until the direction is restored to DAC.

Register A8h: read this register first to preserve the bits and modify only bits 3, 1, and 0:

Bits 1:0 10: Mono

Bits 1:0 01: Stereo

Bit 3 0: Disable Record Monitor for now

Register B9h:

Bits 1:0 00: Single Transfer DMA

Bits 1:0 01: Demand Transfer:
2 bytes per DMA request

Bits 1:0 11: Demand Transfer:
4 bytes per DMA request

6. Clocks and counters: registers A1h, A2h, A4h and A5h:

   Register A1h: Sample Rate Clock Divider. Set bit 7 high for sample rates greater than 22 kHz.

   Register A2h: Filter Clock Divider.

   Registers A4h/A5h: Audio 1 Transfer Count Reload register low/high, two's complement

7. Delay 100 milliseconds to allow analog circuits to settle.
8. Enable Record Monitor if desired:

   Register A8h bit 3 = 1: Enable Record Monitor (optional).

9. Initialize and configure ADC: register B7h. See Table 17. The first command sent to register B7h initializes the DAC and prevents pops.

   Register B7h: programs the FIFO (16-bit/8-bit, signed/ unsigned, stereo/mono).

Table 17 Command Sequence for DMA Record

Mono	Stereo	8-bits	16-bits	Unsigned	Signed	Sequence
X		X		X		Reg B7h = 51h, Reg B7h = D0h
X		X			X	Reg B7h = 71h, Reg B7h = F0h
X			X	X		Reg B7h = 51h, Reg B7h = D4h
X			X		X	Reg B7h = 71h, Reg B7h = F4h
	X	X		X		Reg B7h = 51h, Reg B7h = 98h
	X	X			X	Reg B7h = 71h, Reg B7h = B8h
	X		X	X		Reg B7h = 51h, Reg B7h = 9Ch
	X		X		X	Reg B7h = 71h, Reg B7h = BCh

10. Enable/select DMA channel and IRQ channel, registers B1h and B2h:

    Register B1h: Interrupt Configuration register.
    Verify that bits 4 and 6 are high. Clear bits 7 and 5.

    Register B2h: DRQ Configuration register:
    Verify that bits 4 and 6 are high. Clear bits 7 and 5.

11. Configure system interrupt controller and DMA controller.
12. To start DMA:

    Set bit 0 of register B8h high. Leave other bits unchanged.

13. During DMA

    For Auto-Initialize transfers, do not send any commands to the ES1869 at interrupt time, except for reading Audio_Base+Eh to clear the interrupt request.

    For Normal mode, initialize the system DMA controller with the address and count of the next block to transfer. Update the ES1869 Transfer Count registers if the count is changed. To start the next transfer, clear bit 0 of register B8h, then set it high again.

    To stop a DMA transaction in progress, clear bit 0 of register B8h. To stop a DMA transaction after the current auto-initialize block is finished, clear bit 2 of register B8h, wait for the interrupt, and then clear bit 0 of register B8h.

14. After DMA is finished:

    Restore the system interrupt controller and DMA controller to their idle state.

15. Finally:

    Issue another software reset to the ES1869 to initialize the appropriate registers. This returns the ES1869 to the DAC direction and turns off the record monitor.

Extended Mode Programmed I/O Operation

The REP OUTSB instruction of the 80x86 family transfers data from memory to an I/O port specified by the DX register. The REP INSB instruction is the complementary function. Use ES1869 port Audio_Base+Fh for block transfers.

I/O transfers to FIFO are nearly identical to the DMA process, except that an I/O access to port Audio_Base+Fh replaces the DMA cycle. Some differences are described here.

To program in this mode it is useful to understand how the FIFO Half-Empty flag generates an interrupt request. An interrupt request is generated on the rising edge of the FIFO Half-Empty flag. This flag can be polled by reading port Audio_Base+Ch. The meaning of this flag depends on the direction of the transfer:

DAC FIFOHE flag is set high if 0-127 bytes in FIFO

ADC FIFOHE flag is set high if 128-256 bytes in FIFO

Therefore, for DAC operations, an interrupt request is generated when the number of bytes in the FIFO changes from >= 128 to < 128. This indicates to the system processor that 128 bytes can be safely transferred without over-filling the FIFO. Before the first interrupt can be generated, the FIFO needs to be primed, or filled, with more than 128 bytes. Keep in mind that data may be taken out of the FIFO while it is being filled by the system processor. If that is the case, there may never be >= 128 bytes in the FIFO unless somewhat more than 128 bytes is transferred. Polling the ES1869 FIFOHE flag to be sure it goes low in the interrupt handler (or when priming the FIFO) and perhaps sending a second block of 128 bytes is a solution to this problem.

For ADC, the interrupt request is generated when the number of bytes in the FIFO changes from < 128 to >= 128, indicating that the system processor can safely read 128 bytes from the FIFO. Before the first interrupt can be generated, the FIFO should be emptied (or mostly so) by reading from Audio_Base+Fh and polling the FIFOHE flag. It is not safe to use FIFO reset bit 1 of port Audio_Base+6h indiscriminately to clear the FIFO, because it may get ADC data out-of-sync.

As in DMA mode, bit 0 of register B8h enables transfers between the system and the FIFO inside the ES1869.

NOTE: The ES1869 is designed for I/O block transfer up to a ISA bus speed of 8.33 MHz.

Programmed I/O DAC Operation

Programmed I/O DAC operation is done just as explained under “Extended Mode Audio 1 DAC Operation” on page 49 with the following exceptions:

- In step 3, programming register B9h is unnecessary.
- In step 6, leave bits 7:5 of register B2h low. Set bit 5 of register B1h high to enable an interrupt on FIFO half-empty transitions. Keep bit 6 of register B1h low.
- In step 8, in addition to setting bit 0 of register B8h high, send the REP OUTSB command.

Programmed I/O ADC Operation

Programmed I/O ADC operation is done just as explained under “Extended Mode Audio 1 ADC Operation” on page 50 with the following exceptions:

- In step 3, programming register B9h is unnecessary.
- In step 6, leave bits 7:5 of register B2h low. Set bit 5 of register B1h high to enable an interrupt on FIFO half-empty transitions. Keep bit 6 of register B1h low.
- In step 8, in addition to setting bit 0 of register B8h high, send the REP OUTSB command.

Second Audio Channel DAC Operation

Follow the steps below to program the second audio channel for DAC operation.

1. Reset

   Write 3h to port Audio_Base+6h, instead of 1h as in Compatibility mode. Bit 1 high specifically clears the FIFO. The remainder of the software reset is identical to Compatibility mode. On reset the playback mixer volume for the second audio channel is set to zero, register 7Ch. This masks any pops that might occur during the setup process.

2. Program transfer type: register 78h:

   Register 78h: set bit 4 low for Normal DMA mode, high for Auto-Initialize DMA mode.

   Bits 7:6 00: Single Transfer DMA

   Bits 7:6 01: Demand Transfer DMA:
   2 bytes per DMA request.

   Bits 7:6 10: Demand transfer DMA:
   4 bytes per DMA request.

   Bits 7:6 11: Demand transfer DMA:
   8 bytes per DMA request.

3. Clocks and counters: registers 70h, 72h, 74h and 76h:

   Register 70h: Sample Rate Generator
   Register 72h: Filter Clock Divider
   Registers 74h/76h: Audio 2 Transfer Count Reload register low/high, two's complement

4. Initialize and configure DAC: register 7Ah.

   Register 7Ah:

   Bit 2: set high for signed data, low for unsigned.

   Bit 1: set high for stereo, low for mono.

   Bit 0: set high for 16-bit samples, low for 8-bit.

5. Enable IRQ channel, register 7Ah:

   Register 7Ah: Audio 2 Control 2 register.
   Bit 6 unmasks channel 2 IRQ.

6. Configure system interrupt controller and DMA controller.

7. To start DMA:

   Set bits 1:0 of register 78h high.

8. Delay approximately 100 milliseconds to allow analog circuits to settle, then enable the Audio 2 DAC playback volume, register 7Ch.

9. During DMA

   For Auto-Initialize transfers, read Audio_Base+Eh to clear the interrupt request. Do not send any other commands to the ES1869 at interrupt time.

   For Normal mode, initialize the system DMA controller with the address and count of the next block to transfer. Update the ES1869 Transfer Count registers if the count is changed. To start the next transfer, clear bits 1:0 of register 78h, then set the bits high again.

   To stop a DMA transaction in progress, clear bit 0 of register B8h. To stop a DMA transaction after the current auto-initialize block is finished, clear bit 4 of register 78h, wait for the interrupt, and then clear bits 1:0 of register 78h.

10. After DMA is finished:

    Restore the system interrupt controller and DMA controller to their idle state. Monitor the FIFO Empty status flag in port Audio_Base+Ch to be sure data transfer is completed. A delay of 25 milliseconds is required to let the filter outputs settle to DC-levels, then disable the Audio 2 DAC input to the mixer.

11. Finally:

    Issue another software reset to the ES1869 to initialize the appropriate registers.

Full-Duplex DMA Mode (No DSP Serial Port)

The ES1869 supports stereo full-duplex DMA. In full-duplex (FD) mode, a second audio channel has been added to the ES1869. The second audio channel is programmed through mixer registers.

1. Program the first audio channel as in “Extended Mode Audio 1 ADC Operation” on page 50. Extended mode registers A1h and A2h define the sample rate and filter frequency for both record and playback. In other words, the record and playback must be at the same sample rate (synchronous).
2. Program the second audio channel. Mixer registers 74h and 76h are set to the two's complement DMA transfer count. The second audio channel supports both Auto-Initialize and Normal modes. The playback buffer in system memory does not have to be the same size as the record buffer. When the DMA transfer count rolls over to zero, it can generate an interrupt that is independent of the interrupt generated by the first audio channel.

If the record and playback buffers are the same size, then a single interrupt can be used. Program the DMA Transfer Count Reload registers (A4h, A5h, 74h, and 76h) are programmed with the same value for both channels. Enable the second audio channel before enabling the record channel. For example, assume there are two half-buffers in a circular buffer. When the record channel completes filling the first half, it generates an interrupt. To ensure that the playback channel is not accessing the first half at the time of the interrupt, start the playback channel first. It has a 32-word FIFO that fills quickly through DMA.

The recommended method is as follows:

Program both DMA controllers for Auto-Initialize DMA within separate circular buffers of the same size, N.

To exit full-duplex mode, clear bits 0 and 1 of mixer register 78h.

1. Reset

   Write 3h to port Audio_Base+6h, instead of 1h as in Compatibility mode. Bit 1 high specifically clears the FIFO. The remainder of the software reset is identical to Compatibility mode. Reset disables the Audio 1 DAC input to the mixer. This masks any pops created during the setup of the DMA transfer.

2. After the reset, send command C6h to enable Extended mode commands.
3. Program direction and type: registers B8h, A8h, and B9h:

   Register B8h: set bit 2 high for Auto-Initialize DMA mode. Leave bit 3 low to program the CODEC for the DAC direction.

Register A8h: read this register first to preserve the bits and modify only bits 3, 1, and 0:

Bits 1:0 10: Mono

Register B9h:

Bits 1:0 00: Single Transfer DMA

Bits 1:0 01: Demand Transfer DMA:
2 bytes per DMA request.

Bits 1:0 10: Demand transfer DMA:
4 bytes per DMA request.

4. Clocks and counters: registers A1h, A2h, A4h and A5h:

   Register A1h: Sample Rate Clock Divider
   Register A2h: Filter Clock Divider
   Registers A4h/A5h: DMA Counter Reload register low/high, two's complement

5. Initialize and configure DAC: registers B6h and B7h.

   Register B6h: 80h for signed data and 00h for unsigned data. This also initializes the CODEC for DAC transfer.

   Register B7h: set the data format for 16-bit mono. See Table 16, “Command Sequences for DMA Playback” on page 50.

6. Program transfer type: register 78h:

   Register 78h: set bit 4 high for Auto-Initialize DMA mode.

   Bits 7:6 00: Single Transfer DMA

   Bits 7:6 01: Demand Transfer DMA:
   2 bytes per DMA request.

   Bits 7:6 10: Demand transfer DMA:
   4 bytes per DMA request.

   Bits 7:6 11: Demand transfer DMA:
   8 bytes per DMA request.

7. Clocks and counters: registers 70h, 72h, 74h and 76h:

   Set the sample rate the same as in A1h. Set the Transfer Count Reload to 64 bytes.

   Register 70h: Sample Rate Generator
   Register 72h: Filter Clock Divider
   Registers 74h/76h: Second DMA Transfer Count Reload register low/high, two's complement

8. Initialize and configure DAC: register 7Ah.

   Register 7Ah:

   Bit 2: set high for signed data, low for unsigned.

   Bit 1: set low for mono.

   Bit 0: set high for 16-bit samples.

9. Enable IRQ channel, registers 7Ah and B2h:

   Register 7Ah: Audio 2 Control 2 register.
   Bit 6 unmasks channel 2 IRQ.

   Register B2h: DRQ Configuration register.
   Make sure bits 4 and 6 are high. Clear bits 7 and 5.

10. Set bit 0 of register 78h. Since the playback FIFO is presumably empty, the value zero is transferred to the playback DAC at each sample clock. A click or pop may be heard when full-duplex is enabled. To prevent this, use command D1h to enable the Audio 1 DAC input to the mixer after a suitable delay of 25 milliseconds.
11. Enable playback DMA by setting bit 1 of register 78h. After 64 bytes are transferred, bit 7 of 7Ah should go high. Poll this bit with a suitable time-out of 10 milliseconds.
12. After bit 7 of register 7Ah goes high, enable recording by setting bit 7 of register B7h and bit 0 of register B8h.
13. As usual, discard the first 50 to 100 milliseconds of recorded data until analog circuits have settled.

Programming the ES1869 Mixer

The ES1869 has a set of mixer registers that is backward compatible with the Sound Blaster Pro. However, some of the registers can be accessed in an “extended” or “alternate” way, providing for greater functionality.

Writing and Reading Data from the Mixer Registers

There are two I/O addresses used by the mixer: Audio_Base+4h is the address port; Audio_Base+5h is the data port. In the Sound Blaster Pro, Audio_Base+4h is write only, while Audio_Base+5h is read/write.

Writing Data to the ES1869 Mixer Registers

To set a mixer register, write its address to Audio_Base+4h, then write the data to Audio_Base+5h.

Reading Data from the ES1869 Mixer Registers

To read the register, write its address to Audio_Base+4h, then read the data from Audio_Base+5h.

Resetting the Mixer Registers

The mixer registers are not affected by software reset. To reset the registers to initial conditions, write any value to mixer register 00h:

1. Write 00h to Audio_Base+4h
   (select mixer register to 00h).
2. Write 00h to Audio_Base+5h
   (write 00h to the selected mixer register).

Extended Access to SB Pro Mixer Volume Controls

The Sound Blaster Pro Mixer Volume controls are mostly 3 bits per channel. See the Sound Blaster Compatibility register 04h in Table 23 for details. Bits 0 and 4 are always high when read. The ES1869 offers an alternate way to write each mixer register. Use the “extended access” registers for volume control of 4 bits per channel. If the Sound Blaster Pro compatible interface is used, bits 0 and 4 are cleared by a write and forced high on all reads. See Table 18 for a list of Sound Blaster Pro registers and the extended access counterparts.

Table 18 Sound Blaster Pro/Extended Access Registers

Register	Function	Extended Access Register for 4 bits/Channel
04h	Voice volume	14h
22h	Master volume	32h
26h	FM volume	36h
28h	CD (Aux) volume	38h
2Eh	Line volume	3Eh

For example, if you write 00h to Sound Blaster Pro register 04h, you will read back 11h because bits 0 and 4 are “stuck high” on reads. Inside the register, these bits are “stuck low,” so that writing 00h is the same as writing 11h.

A write or read to address 14h instead of 04h allows direct access to all 8 bits of this mixer register.

Extended Access to Mic Mix Volume

If Sound Blaster Compatibility mode register address 0Ah is used to control Mic Mix Volume, only bits 2 and 1 are significant. Bit 0 is stuck high on reads and stuck low on writes. Since this is a mono control, panning is not supported.

For extended access, use register address 1Ah instead. Register 1Ah offers 4 bits-per-channel for pan control of the mono microphone input to the mixer.

Mic Mix Volume (1Ah, R/W)

Mic mix volume left				Mic mix volume right			
7	6	5	4	3	2	1	0

Access to register 1Ah through address 0Ah is mapped as follows:

Write to 0Ah	D2=0, D1=0	Mic mix volume = 00h
	D2=0, D1=1	Mic mix volume = 55h
	D2=1, D1=0	Mic mix volume = AAh
	D2=1, D1=1	Mic mix volume = FFh
Read from 0Ah	D2 = Mic Mix Volume register bit 3	
	D1 = Mic Mix Volume register bit 2	
	D0 = 1	
	others are undefined.	

Extended Access to ADC Source Select

In Sound Blaster Compatibility mode in the Sound Blaster Pro mixer, there are three choices for recording source, set by bits 2 and 1 of mixer register 0Ch. Note that bit 0 is set to zero upon any write to 0Ch and set to one upon any read from 0Ch:

D2	D1	Source Selected
0	0	Microphone (default)
0	1	CD (Aux) input
1	0	Microphone
1	1	Line input

For extended access, use register address 1Ch to select recording from the mixer as follows:

D2	D1	D0	Source Selected
x	0	x	Microphone (default)
0	1	x	CD (Aux) input
1	1	0	Line input
1	1	1	Mixer * (Bits 4:3 of Mixer register 7Ah determine if the mixer input source is the playback or record mixer).

Sound Blaster Pro Volume Emulation

Sound Blaster Pro emulations for master volume means that the 6-bit volume counters can be written through the Sound Blaster Pro mixer register 22h (or 32h). Sound Blaster Pro emulation is enabled by default, and can be disabled by setting bit 0 of mixer register 64h.

The master volume registers 60h and 62h can always be read, regardless of whether Sound Blaster Pro volume emulation is enabled, using the Sound Blaster Pro mixer registers 22h (and 32h). The following 6-bit to 4-bit translation table is used.

Table 19 SB Pro Read Volume Emulation

Mute	Master Volume	Value Read at 32h	Value Read at 22h
1	xx	0	1
0	0-24	1	1
0	25-30	2	3
0	31-34	3	3
0	35-38	4	5
0	39-42	5	5
0	43-46	6	7
0	47-50	7	7
0	51-54	8	9
0	55	9	9
0	56-57	10	11
0	58	11	11
0	59-60	12	13
0	61	13	13
0	62	14	15
0	63	15	15

If Sound Blaster Pro volume emulation is enabled, then a mixer reset causes both left and right channels to be set to their power-on defaults, namely 54 (36h).

If Sound Blaster Pro volume emulation is enabled, then a write to mixer register 22h (or 32h) causes both left and right master volume registers to be changed as follows:

Table 20 SB Pro Write Volume Emulation

Value written to 22h or 32h	Mute	6-Bit Volume
0	1	24
1	0	24
2	0	30
3	0	34
4	0	38
5	0	42
6	0	46
7	0	50
8	0	54
9	0	55
10	0	56
11	0	58
12	0	59
13	0	61
14	0	62
15	0	63

Record and Playback Mixer

The ES1869 has stereo mixers for playback and record. Each stereo mixer has eight input sources, each with independent 4-bit left and right volume controls. For each 4-bit volume control, level 0 is mute and level 15 is maximum volume. The ES1869 mixers use a dual slope method for selecting volume. Each increase of one step in volume from settings 1 to 8 results in a +3 dB increase. Each increase of one step in volume from settings 8 to 15 results in a +1.5 dB increase.

Table 21 Extended Access Mixer Volume Values

4-Bit Value	Volume in Decibels (dB)			
	Audio 1[a] (Record)	Audio 2[b] (Playback)	Mic, Music DAC, I²S	AuxA, AuxB, Line, Mono-In
15	+1.5	0	+10.5	+3.0
14	0	-1.5	+9.0	+1.5
13	-1.5	-3.0	+7.5	0
12	-3.0	-4.5	+6.0	-1.5
11	-4.5	-6.0	+4.5	-3.0
10	-6.0	-7.5	+3.0	-4.5
9	-7.5	-9.0	+1.5	-6.0
8	-9.0	-10.5	0	-7.5
7	-12.0	-13.5	-3.0	-10.5
6	-15.0	-16.5	-6.0	-13.5
5	-18.0	-19.5	-9.0	-16.5
4	-21.0	-22.5	-12.0	-19.5
3	-24.0	-25.5	-15.0	-22.5
2	-27.0	-28.5	-18.0	-25.5
1	-30.0	-31.5	-21.0	-28.5
0	mute	mute	mute	mute

a. Audio 1 DAC mixer input is gated by the Sound Blaster "Speaker On" control. This control bit is toggled by the D1 (on) and D3 (off) Sound Blaster commands.

b. In Telegaming mode (enabled by bit 0 of mixer register 48h when in Serial mode), the audio 2 DAC mixer input volume is slaved to the audio 1 DAC mixer input volume.

Table 22 Mixer Input Volume Registers

Mixer Input	Playback Volume Register	Record Volume Register
Audio 1	14h	–
Audio 2	7Ch	69h
Microphone	1Ah	68h
Music DAC (FM/ ES689/ES69x/I²S)	36h	6Bh
AuxA (CD)	38h	6Ah
AuxB	3Ah	6Ch
Line	3Eh	6Eh
Mono In	6Dh	6Fh

REGISTERS

Register Types

Types of Register Access

There are two types of audio registers in the ES1869:

- Mixer registers.

  These registers are accessed through I/O ports Audio_Base+4h and Audio_Base+5h. Audio_Base+4h is written with the register address. Then the register can be read written through Audio_Base+5h. These registers control many functions other than the mixer.

- Controller registers.

  These registers are used to control Extended mode DMA playback and record through the first audio channel. Controller registers are accessed through an extension to the Sound Blaster common interface. This interface uses I/O ports Audio_Base+Ah, Audio_Base+Ch, and Audio_Base+Eh to transfer read data, write data/commands, and status respectively.

Mixer Registers

There are two types of mixer registers. Sound Blaster Pro Compatible mixer registers are fully compatible with the Sound Blaster Pro. ESS mixer registers are specific to ESS Technology, Inc. ES1869 *Audio***Drive**® chips, although many registers are shared throughout the *Audio***Drive**® family of chips.

Sound Blaster Pro Compatible Mixer Registers

This section provides a summary of Sound Blaster Pro compatible mixer registers in the ES1869 and some comments on the characteristics of these registers.

Table 23 Sound Blaster Compatibility Register Summary

Reg	D7	D6	D5	D4	D3	D2	D1	D0	Description
00h	Write: reset mixer								Mixer reset
04h	DAC play volume left			X	DAC play volume right			X	DAC playback volume
0Ah	X	X	X	X	X	Mic mix volume		X	Mic mix volume
0Ch	X	X	F1 *	X	F0 *	ADC source		X	See note for F0, F1.
0Eh	X	X	F2 *	X	X	X	Stereo	X	See note for F2.
22h	Master volume left			X	Master volume right			X	Master volume
26h	FM volume left			X	FM volume right			X	Music DAC volume
28h	AuxA (CD) volume left			X	AuxA (CD) volume right			X	AuxA (CD) volume
2Eh	Line volume left			X	Line volume right			X	Line volume

* Sound Blaster Filter Control bits F2, F1, and F0 have no equivalent function in the ES1869 and are ignored.

Filter Control Bits

The Sound Blaster Pro mixer has three bits that control input and output filters. They are labeled F0, F1, and F2 in Table 23 and Table 24. They have no equivalent function in the ES1869 and their values are ignored.

Mixer Stereo Control Bit

Bit 1 of register 0Eh is the Mixer Stereo Control bit. It is normally zero. Set this bit high to enable Sound Blaster Pro compatible stereo DAC functions. In this case, program the DAC sample rate to be twice the sample rate of each channel. For example, for 22 kHz stereo, program the “sample rate” to be 44 kHz using command 40h.

This bit enables stereo only for DMA transfer to the DAC in Compatibility mode. It should not be used in Extended mode.

Clear this bit after completing the stereo DMA transfer, because this bit is unaffected by software reset (only mixer reset).

See also “Stereo DMA Transfers in Compatibility Mode” on page 45.

ESS Mixer Registers

This section provides a summary of the ESS mixer registers followed by a detailed description of each register.

Table 24 ESS Mixer Registers Summary

Reg	D7	D6	D5	D4	D3	D2	D1	D0	Remark
00h	Write: reset mixer								Reset mixer
14h	Audio 1 play volume left				Audio 1 play volume right				Audio 1 play volume
1Ah	Mic mix volume left				Mic mix volume right				Mic mix volume
1Ch	x	x	F1	Mute	F0	Extended record source			
32h	Master volume left				Master volume right				Master volume
36h	FM volume left				FM volume right				FM volume
38h	AuxA (CD) volume left				AuxA (CD) volume right				AuxA (CD) volume
3Ah	AuxB volume left				AuxB volume right				AuxB volume
3Ch					PC speaker volume				PC speaker volume
3Eh	Line volume left				Line volume right				Line volume
40h	ES1869 identification value								Read-only
42h	Input override	Record Source Select			Record Level				Serial mode input control
44h	Master volume override	Serial mode output select			Master volume				Serial mode output control
46h	Analog control override	Music mixer test	Left ADC	Right ADC	Mono	x	FDXO enable	FDXI enable	Serial mode analog control
48h	SE	Two's comp	Serial reset	Enable ES689/ ES69x intfc	Active low sync	1: DSP test mode	Enable 1st DMA in SMODE	0	Serial mode control
4Ah	0	Two's complement divisor							FSX/FSR rate control (test)
4Ch	Filter over-ride	0	0	0	Two's complement filter divider				Serial mode filter divider
4Eh	TX SRC1	TX SRC0	TX 16/8	TX stereo/ mono	RX SRC1	RX SRC0	RX 16/8	RX stereo/ mono	Serial mode format/source/target
50h	0	0	0	0	1:Enable Spatializer	0:Reset	1:Mono mode	0	Spatializer enable and mode control
52h	0	0	Spatializer level						Spatializer level
5Ch	L/R state flag	Signal proc test mode	ADC test mode	1: Acc timing	Reserved				Spatializer test control
5Eh									Spatializer test data
60h	0	1:Mute	Left master volume						Left master volume and mute
61h	0	1:Mute	Left volume counter						Hardware volume control counter
62h	0	1:Mute	Right master volume						Right master volume and mute
63h	0	1:Mute	Right volume counter						Hardware volume control counter
64h	1:Split mode	MPU-401 int mask	1:Count by 3	Read-only HMV int request	Mode		HMV int mask	Disable SB Pro master vol control	Master volume control
65h								Opamp cal-ibration	Opamp calibration control
66h	Clear hardware volume interrupt request								Write-only
68h	Mic record volume left				Mic record volume right				Mic record volume
69h	Audio 2 record volume left				Audio 2 record volume right				Audio 2 record volume
6Ah	AuxA (CD) record volume left				AuxA (CD) record volume right				AuxA (CD) record volume
6Bh	Music DAC record volume left				Music DAC record volume right				Music DAC record volume

Table 24 ESS Mixer Registers Summary (Continued)

Reg	D7	D6	D5	D4	D3	D2	D1	D0	Remark
6Ch	AuxB record volume left				AuxB record volume right				AuxB record volume
6Dh	Left Mono_In play mix				Right Mono_In play mix				Mono_In play mix
6Eh	Line record volume left				Line record volume right				Line record volume
6Fh	Mono_In record volume left				Mono_In record volume right				Mono_In record volume
70h	Master clock	Two's complement rate divider							Audio 2 sample rate
71h	0	0	1:New reg A1h	1:4x mode	1:SCF2 bypass	1:SCF1 bypass	1:Async mode	1:FM mix	Audio 2 mode
72h	Two's complement filter rate divider								Audio 2 filter clock rate
74h	Two's complement transfer count – low byte								Audio 2 transfer count reload
76h	Two's complement transfer count – high byte								
78h	Single/demand transfer		0	1: Auto-initialize	0	0	Enable second channel DMA	Enable full-duplex mode	Audio 2 control 1
7Ah	2nd channel IRQ	IRQ mask	0	0	0	Data sign	Stereo /Mono	16-bit /8-bit	Audio 2 control 2
7Ch	Left channel volume				Right channel volume				Audio 2 DAC mixer volume
7Dh	0	0	0	0	Enable +26 dB mic amp	Mono_Out source select		Enable Mono_In mix w/ AOUTL/R	Mic preamp, Mono_In and Mono_Out
7Fh	Reserved			Music digital record	I²S data activity	I²S clock activity	MODE pin	Enable I²S connect to music DAC	I²S interface

Register Detailed Descriptions

Reset Mixer (00h, W)

Write: reset mixer							
7	6	5	4	3	2	1	0

Audio 1 Play Volume (14h, R/W)

Audio 1 play volume left				Audio 1 play volume right			
7	6	5	4	3	2	1	0

This register controls the playback volume of the first audio channel. On reset, this register assumes the value of 88h.

Mic Mix Volume (1Ah, R/W)

Mic mix volume left				Mic mix volume right			
7	6	5	4	3	2	1	0

This register controls the playback volume of the Mic input. On reset, this register assumes the value of 00h.

Extended Record Source (1Ch, R/W)

x	x	F1	Mute	F0	Extended record source		
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:6	–	No function.
5	F1	Sound Blaster Filter Control bit F1 has no equivalent function in the ES1869 and is ignored.
4	Mute	1 = Mutes the input to the filters for recording. This does not affect MONO_OUT.
3	F0	Sound Blaster Filter Control bit F0 has no equivalent function in the ES1869 and is ignored.

Bits	Name	Description			
2:0	Extended record source	Bit 2	Bit 1	Bit 0	Record Source
		0	0	0	Microphone
		0	1	0	AuxA (CD)
		1	0	0	Microphone
		1	1	0	Line
		0	0	1	Left channel: microphone Right channel: Master vol input (L+R)/2 *
		0	1	1	Left channel: AOUT_L Right channel: AOUT_R
		1	0	1	Record mixer
		1	1	1	Master volume inputs *

* The master volume inputs are the outputs of the Spatializer processor before master volume is applied. However, the design of the ES1869 causes some attenuation due to master volume in some conditions before the Spatializer. Unless the master volume is at one of the top 7 levels (0 dB, -.75 dB..-4.5 dB), there is -5.25 dB attenuation between the output of the playback mixer and the input to the Spatializer. If the master volume is at one of the top 7 levels, the attenuation according to the master volume level is determined prior to the input of the Spatializer.

Master Volume Register (32h, R/W)

Master volume left				Master volume right			
7	6	5	4	3	2	1	0

On reset, this register assumes the value of 88h.

This register provides backward-compatible access to master volume. New applications can also use registers 60h and 62h, which have more resolution.

FM Volume Register (36h, R/W)

FM volume left				FM volume right			
7	6	5	4	3	2	1	0

On reset, this register assumes the value of 88h.

AuxA (CD) Volume Register (38h, R/W)

AuxA (CD) volume left				AuxA (CD) volume right			
7	6	5	4	3	2	1	0

On reset, this register assumes the value of 00h.

AuxB Volume Register (3Ah, R/W)

AuxB volume left				AuxB volume right			
7	6	5	4	3	2	1	0

On reset, this register assumes the value of 00h.

PC Speaker Volume Register (3Ch, R/W)

Reserved					PC speaker volume		
7	6	5	4	3	2	1	0

On reset, this register assumes the value of 04h.

Line Volume Register (3Eh, R/W)

Line volume left				Line volume right			
7	6	5	4	3	2	1	0

On reset, this register assumes the value of 00h.

ES1869 Identification Value (40h, R)

ES1869 identification value							
7	6	5	4	3	2	1	0

To identify the ES1869, mixer register 40h returns the following values on four successive reads:

18h, 69h, A[11:8], A[7:0]

where 18h and 69h are data reads indicating the part number (1869) and A[11:0] is the base address of the configuration device.

Serial Mode Input Control (42h, R/W)

Input override	Record source select			Record level			
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description			
7	Input override	1 = The record source select and record level fields take effect and override settings in mixer registers 1Ch and B4h. Serial mode is enabled when input pin DCLK is clocking and either the external pin SE is high or bit 7 of mixer register 48h is high. 0 = no effect.			
6:4	Record source select	Bit 6	Bit 5	Bit 4	Signal
		0	0	0	Line
		0	0	1	AuxA (CD)
		0	1	0	Microphone
		0	1	1	Master volume inputs
		1	0	0	Left channel: microphone Right channel: master volume (L+R)/2
		1	0	1	AOUT_L/AOUT_R
		1	1	0	Record mixer
		1	1	1	Record source is disconnected from filters (muted)
		Record source is unchanged in Serial mode.			
3:0	Record level	For microphone source, specifies record gain from 0 to +22.5 dB in steps of 1.5 dB. For other sources, specifies record level from -6 dB to +16.5 dB in steps of 1.5 dB.			

Serial Mode Output Control (44h, R/W)

Master volume override	Serial mode output select			Master volume			
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7	Master volume override	1 = Master Volume during Serial mode is taken from this register rather than from the Master Volume registers.
6:4	Serial mode output select	Determines what signal is input to the master volume stage during Serial mode. Bit 6 Bit 5 Bit 4 Master Volume Input 0 0 0 Mute 0 0 1 No change from normal op 0 1 0 First audio channel DAC only – playback mixer bypassed * 0 1 1 No change from normal op 1 0 0 Playback mixer with 1st audio channel DAC set to 0 dB attenuation * 1 0 1 Playback mixer with 1st audio channel DAC muted * 1 1 0 ---- 1 1 1 ---- * Overrides record monitor and record mute features.
3:0	Master volume	Master Volume during Serial mode if bit 7 is high. 0 is mute and 15 is maximum (0 dB).

Serial Mode Analog Control (46h, R/W)

Analog control override	Music mixer test	Left ADC	Right ADC	Mono	x	FDXO enable	FDXI enable
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7	Analog control override	1 = bits 5:0 of this register take effect during Serial mode. 0 = bits 5:0 never take effect.
6	Music mixer test	Test feature. 1 = Music DAC mixer inputs are replaced with AUXB_L and AUXB_R inputs.
5	Left ADC	1 = Left channel combined ADC and DAC is in ADC mode. 0 = Left channel combined ADC and DAC is in DAC mode.
4	Right ADC	1 = Right channel combined ADC and DAC is in ADC mode. 0 = Right channel combined ADC and DAC is in DAC mode.
3	Mono	1 = Mono record, mono playback, or mono full-duplex modes. 0 = Stereo playback or stereo record.
2	–	No function.
1	FDXO enable	Provided for backward compatibility with ES1868. If Serial mode is enabled, bit 7 and bit 1 of this register (46h) are high, and bit 6 of register 48h is low (serial reset inactive), then the MONO_OUT pin is selected to be a buffered output of the right channel CIN_R pin (assumed to be used as a mono DAC output in Serial mode). This condition overrides the settings of mixer register 7Dh, bits 2:1, which normally select the MONO_OUT state.
0	FDXI enable	If Serial mode is enabled and bit 5 (left channel used for ADC) and bit 0 are high, then the left channel filter input is the MONO_IN pin rather than the normally selected record source.

Serial Mode Control (48h, R/W)

SE	Two's comp	Serial reset	Enable ES689/ES69x intfc	Active-low sync	DSP test mode	Enable 1st DMA in SMODE	0
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7	SW SE	1 = Enable DSP serial port. This signal is synchronized with DCLK input rising edge. If DCLK is not running, changing SE has no effect.
6	Two's comp	1 = Data format is signed, two's complement format. 0 = Data format is unsigned (offset binary) format.
5	Serial reset	1 = DSP serial interface reset. Resets left/right flags for stereo modes. 0 = Release from reset.
4	Enable ES689/ ES69x intfc	1 = Enable ES689/ES69x to use music DAC if MCLK is detected high at least once every 20 µsec. Mixer volume for this DAC is controlled by the FM mixer volume register. 0 = Disable ES689/ES69x serial interface.
3	Active-low sync	1 = Frame sync pulses (FSR,FSX) are active-low. 0 = Frame sync pulses are active-high.
2	DSP test mode	Test mode. DCLK, FSX, and FSR become outputs. DCLK is 1.5876 MHz. FSX and FSR are active-high frame syncs at a rate determined by mixer register 4Ah.
1	Enable 1st DMA in SMODE	1 = Game and Telephony mode enabled. In Serial mode, connect first channel DMA (game compatible DMA) to second channel DAC. The second channel DAC gets its filter clock and volume control from the first channel. 0 = Game and Telephony mode disabled. In Serial mode, the first channel DMA does not get played. The second channel DMA is connected to the second channel DAC as usual.
0	0	Reserved. Always write 0.

FSX/FSR Rate Control (Test) (4Ah, R/W)

0	Two's complement divisor						
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7	0	Reserved. Always write 0.
6:0	Two's comp divisor	Used in a test mode enabled by bit 2 of mixer register 48h. In this mode DCLK is a clock output of 1.5876 MHz. Bits 6:0 determine the rate of the active-high frame sync outputs FSX and FSR. Example: if bits 6:0 were programmed to be 5Ch (-36 decimal), then the frame rate is 44.1 kHz.

Serial Mode Filter Divider (4Ch, R/W)

Filter override	0	0	0	Two's complement filter divider			
7	6	5	4	3	2	1	0

This register controls the switched-capacitor filter during Serial mode.

Bit Definitions:

Bits	Name	Description
7	Filter override	1 = During Serial mode, the first channel DAC and ADC switched-capacitor filters are controlled by a clock derived from DCLK. 0 = This register has no effect.
6:4	0	Reserved. Always write 0.
3:0	Two's comp filter divider	Bits 3:0 are a two's complement value that divides down the DCLK input. The ratio of the filter -3 dB frequency to the filter clock is approximately 1:41. Examples: 02h (-14) External Serial Clock 2.048 MHz/14/41 = 3568 Hz for 8000 Hz Sample Rate. 0Eh (-2) Internal Serial Clock 1.591 MHz/2/41 = 19.4 kHz for 44,100 Sample Rate. Note that the sample rate divider is an integer multiple of the filter divide for 44,100, which gives maximum performance of DACs and ADCs.

Serial Mode Format/Source/Target (4Eh, R/W)

TX SRC1	TX SRC0	TX 16/8	TX stereo/ mono	RX SRC1	RX SRC0	RX 16/8	RX stereo/ mono
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:6	TX SRC1/ SRC0	Transmit Register Source. Bit 7 Bit 6 Source 0 0 None: transmit register held at zero. 0 1 1st channel DMA FIFO (1st channel in mono or stereo playback direction). 1 0 1st channel ADC (left channel ADC if mono). 1 1 ----
5	TX 16/8	1 = Transmit length is 16 bits. 0 = Transmit length is 8 bits.
4	TX stereo/ mono	1 = Transmit mode is stereo. Left and right channels alternate, with left channel data preceding right channel data. 0 = Transmit mode is mono.
3:2	RX SRC1/ SRC0	Receive Register Target. Bit 3 Bit 2 Target 0 0 None: receive register held at zero 0 1 1st channel DMA FIFO (1st channel in mono or stereo record direction). 1 0 1st channel DAC (right channel DAC if mono). 1 1 ----
1	RX 16/8	1 = Receive length is 16 bits. 0 = Receive length is 8 bits.
0	RX stereo/ mono	1 = Receive mode is stereo. Left and right channels alternate, with left channel data preceding right channel data. 0 = Receive mode is mono.

Spatializer Enable and Mode (50h, R/W)

0	0	0	0	Enable Spatializer	Reset	Mono mode	0
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:4	0	Reserved. Always write 0.
3	Enable Spatializer	1 = Enable Spatializer effect. 0 = Disable Spatializer effect (effect unit bypassed).
2	Reset	1 = Release from reset. 0 = Reset Spatializer.
1	Mono mode	1 = Mono-in stereo-out mode. 0 = Stereo-in stereo-out mode.
0	0	Reserved. Always write 0.

Spatializer Level (52h, R/W)

0	0	Spatializer level					
7	6	5	4	3	2	1	0

Reset to zero by hardware reset.

Bit Definitions:

Bits	Name	Description
7:6	0	Reserved. Always write 0.
5:0	Spatializer level	0 is minimum effect; 3Fh is maximum effect.

Spatializer Test Control (5Ch, R/W)

L/R state flag	Signal proc test mode	ADC test mode	Acc timing	Reserved			
7	6	5	4	3	2	1	0

Reset to zero by hardware reset.

Bit Definitions:

Bits	Name	Description
7	L/R state flag	Read-only. Left/right state flag.
6	Signal proc test mode	Allows the input to the signal processing logic to be written from the host for test purposes. Poll bit 7 of this register to synchronize. When it goes high, write to register 5Eh four times successively to write left low, left high, right low, right high.
5	ADC test mode	Poll bit 7 of this register to synchronize. then read register 5Eh four times successively to read left low, left high, right low, right high.
4	Acc timing	1 = Accelerated timing.
3:0	–	Reserved.

Spatializer Test Data (5Eh, R/W)

7	6	5	4	3	2	1	0

Except in ADC test mode, this register returns the current 8-bit gain setting. In ADC test mode, it is used to read back the ADC values. In signal processor test mode, it is used to write test pattern data.

In ADC test mode or signal processor test mode, four reads or writes are needed to access all four bytes in series. The sequence is controlled by an internal 2-bit counter. This counter is incremented after every I/O read or write to mixer register 5Eh. The counter is reset by an I/O read from mixer register 5Ch.

Left Master Volume and Mute (60h, R/W)

0	1:Mute	Left master volume					
7	6	5	4	3	2	1	0

Right Master Volume and Mute (62h, R/W)

0	1:Mute	Right master volume					
7	6	5	4	3	2	1	0

Registers 60h and 62h are the actual volume values presented to the analog hardware. These registers can be modified under five circumstances:

1. By hardware reset each register is loaded with 36h.
2. Direct write to mixer address 60h or 62h.
3. If bit 0 of mixer register 64h is low, then writing to mixer registers 22h or 32h updates 60h and 62h.
4. If bit 0 of mixer register 64h is low, then a mixer reset (writing to mixer register 0h) loads these registers with 36h.
5. If hardware volume controls are enabled and bit 7 of mixer register 64h is low, then the hardware volume controls can directly modify the contents of these registers.

Reading mixer registers 22h or 32h actually reads a value calculated from the current contents of 60h and 62h.

Left Hardware Volume Control Counter (61h, R/W)

0	1:Mute	Left volume counter					
7	6	5	4	3	2	1	0

See the explanation following the Right Hardware Volume Control Counter, mixer register 63h.

Right Hardware Volume Control Counter (63h, R/W)

0	1:Mute	Right volume counter					
7	6	5	4	3	2	1	0

These registers only exist if bit 7 of mixer register 64h is high. If bit 7 is low, these registers are combined with registers 60h and 62h and cannot be independently written or read.

If bit 7 of mixer register 64h is high, these registers have no connection with registers 60h or 62h. They are the hardware volume counters and mute. It is the responsibility of the host software to read these registers and update the master volume registers 60h and 62h.

Master Volume Control (64h, R/W)

Split mode	MPU-401 int mask	Count by 3	Read-only HMV int request	Mode		HMV int mask	Disable SB Pro master vol emulation
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7	Split mode	1 = Split counter registers from volume registers and access them independently. 0 = Slave counter and volume registers together.
6	MPU-401 int mask	This bit is AND'ed with the MPU-401 interrupt request. If it is low, the MPU-401 interrupt request stays low. This bit is cleared by hardware reset.
5	Count by 3	1 = Count up and down by 3 for each push of Up or Down buttons. 0 = Count up and down by 1 for each push of Up or Down buttons. This bit is cleared by hardware reset.
4	Read-only HMV int request	Read-only interrupt request from hardware volume event.
3:2	Mode	Selects operation mode: Bit 3 Bit 2 Operating Mode 0 0 Normal 3-wire mode (hardware reset default 0 1 2-wire mode: both Up and Down inputs being low together act the same as Mute input low. 1 0 Reduced debounce (10 µsec vs. 40 msec), 2-wire mode, auto-increment and decrement disabled. 1 1 Hardware volume control disabled
1	HMV int mask	This bit is AND'ed with the hardware volume interrupt request before being OR'd with the first channel audio interrupt request. If this bit is low, the hardware volume interrupt request does not get OR'd with the first channel audio interrupt request. This bit is cleared by hardware reset.
0	Disable SB Pro master vol emulation	When low, a write to Sound Blaster Pro master volume registers 22h or 32h is translated into a write to hardware master volume registers 60h and 62h. Also, if low, a mixer reset (writing to mixer register 0h) causes registers 60h and 62h to be reset to default value 36h. When high, the Sound Blaster Pro master volume registers are, in effect, read-only. This bit is cleared by hardware reset.

Opamp Calibration Control (65h, R/W)

							Opamp calibration
7	6	5	4	3	2	1	0

In the analog circuitry of the ES1869, operational amplifiers that require calibration go through a calibration procedure that takes about 200 milliseconds to perform. During this period the analog outputs of the chip (AOUT_L, AOUT_R, and MONO_OUT) are muted.

The calibration procedure occurs automatically after hardware reset and can be started at any time thereafter by writing 1 to mixer register 65h.

Bit Definitions:

Bits	Name	Description
0	Opamp calibration	Read: 1 = Opamp calibration is in progress. The calibration operation happens after hardware reset if a 1 is written to this bit. Calibration takes about 200 msec, during which the analog outputs of the chip (AOUT_L/R, MONO_OUT) are muted. Write: A 1 written to this register starts a calibration operation. A zero written to this register stops the calibration operation immediately (not recommended).

Clear Hardware Volume Interrupt Request (66h, R/W)

Clear Hardware Master Control							
7	6	5	4	3	2	1	0

Any write to this register resets the hardware volume interrupt request.

Mic Record (68h, R/W)

Left Mic record				Right Mic record			
7	6	5	4	3	2	1	0

Audio 2 Record (69h, R/W)

Left Audio 2 record				Right Audio 2 record			
7	6	5	4	3	2	1	0

AuxA (CD) Record (6Ah, R/W)

Left AuxA (CD) record				Right AuxA (CD) record			
7	6	5	4	3	2	1	0

Music DAC Record (6Bh, R/W)

Left music DAC record				Right music DAC record			
7	6	5	4	3	2	1	0

AuxB Record (6Ch, R/W)

Left AuxB record				Right AuxB record			
7	6	5	4	3	2	1	0

Mono_In Play Mix (6Dh, R/W)

Left Mono_In play mix				Right Mono_In play mix			
7	6	5	4	3	2	1	0

Line Record (6Eh, R/W)

Left Line record				Right Line record			
7	6	5	4	3	2	1	0

Mono_In Record (6Fh, R/W)

Left Mono_In record				Right Mono_In record			
7	6	5	4	3	2	1	0

Audio 2 Sample Rate (70h, R/W)

Master clock	Two's complement rate divider						
7	6	5	4	3	2	1	0

This register is reset to zero by hardware reset.

Bit Definitions:

Bits	Name	Description
7	Master clock	Selects the master clock for the sample rate generator: 1 = 768 kHz (used to generate 48 kHz, 32 kHz, 16 kHz, 8 kHz, and so on). 0 = 793.8 kHz (used to generate 44.1 kHz, 22.05 kHz, and so on).
6:0	Two's comp rate divider	Two's complement divisor of master clock to produce sample rate. Examples: Rate — Register 70h 8000 — A0h 48000 — F0h 44100 — 6Eh

Audio 2 Mode (71h, R/W)

0	0	New reg A1h	4x mode	SCF2 bypass	SCF1 bypass	Async mode	FM mix
7	6	5	4	3	2	1	0

This register is reset to zero by hardware reset.

Bit Definitions:

Bits	Name	Description
7:6	0	Reserved. Always write 0.
5	New reg A1h	1 = Register A1h behaves in the same manner as mixer register 70h, which gives more accurate sample rates that are divisors of 48 kHz. 0 = Enables register A1h to behave exactly as in previous ESS *Audio***Drive**® chips.
4	4x mode	1 = 2nd channel DAC is in 4x oversampling mode. 0 = 2nd channel DAC is not oversampling.
3	SCF2 bypass	1 = 2nd channel DAC switched capacitor filter is bypassed. 0 = 2nd channel DAC SCF is not bypassed. **NOTE:** the SCF is always bypassed in 4x oversampling mode.
2	SCF1 bypass	1 = 1st channel CODEC switched capacitor filter is bypassed. 0 = 1st channel CODEC SCF is not bypassed.
1	Async mode	1 = 2nd channel DAC is asynchronous to the sample rate of the 1st channel. 0 = 2nd channel DAC is slaved to the sample rate and filter rate of the 1st channel.
0	FM mix	1 = 2nd channel DMA is slaved to the FM synthesizer sample rate and the DMA data is digitally mixed to the FM synthesizer output.

Audio 2 Filter Clock Rate (72h, R/W)

Two's complement filter rate divider							
7	6	5	4	3	2	1	0

In Asynchronous mode, this register determines the filter clock rate of the second channel switched capacitor filter. If used, this register is programmed in the same manner as controller register A2h.

This register is reset to zero by hardware reset.

Audio 2 Transfer Count Reload (74h, R/W)

Two's complement transfer count – low byte							
7	6	5	4	3	2	1	0

Audio 2 Transfer Count Reload (76h, R/W)

Two's complement transfer count – high byte							
7	6	5	4	3	2	1	0

Audio 2 Control 1 (78h, R/W)

Single/demand transfer		0	Auto-initialize	0	0	Enable 2nd chan DMA	Enable FIFO to 2nd chan DAC
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:6	Single/demand transfer	Bit 7 / Bit 6 0 0 — Single transfer: 1 DACK per DRQ 0 1 — Demand transfer: 2 DACKs per DRQ 1 0 — Demand transfer: 4 DACKs per DRQ 1 1 — Demand transfer: 8 DACKs per DRQ
5	0	Reserved. Always write 0.
4	Auto-initialize	1 = Auto-initialize mode. After the transfer counter rolls over to 0, it is automatically reloaded and DMA continues. The second channel interrupt flag will be set high. 0 = Normal mode. After the transfer counter rolls over to 0, it is reloaded but DMA stops. Bit 1 of this register is cleared. The 2nd channel interrupt flag will be set high.
3:2	0	Reserved. Always write 0.

Bits	Name	Description
1	Enable 2nd chan DMA	1 = 2nd channel DMA enabled for data to be written into the 2nd channel FIFO (32 words deep). 0 = Second channel DMA not enabled. This bit is cleared when the transfer counter rolls over to zero, if not in Auto-initialize mode.
0	Enable FIFO to 2nd chan DAC	1 = Data transfer from the FIFO to the 2nd channel DAC is enabled (or, in special cases, from the FIFO to the DSP serial port or to be digitally mixed with the FM synthesizer output). 0 = Data transfer not enabled.

Audio 2 Control 2 (7Ah, R/W)

2nd chan IRQ	IRQ mask	0	0	0	Signed	stereo/ mono	16-bit/ 8-bit
7	6	5	4	3	2	1	0

This register is reset to zero by hardware or software reset.

Bit Definitions:

Bits	Name	Description
7	2nd chan-nel IRQ	This latch is set high when the DMA counter rolls over to zero, or when a 1 is written to this bit. The latch is cleared by writing a zero to this bit, or by hardware or software reset.
6	IRQ mask	This bit is AND'ed with bit 7 to produce the second DMA channel interrupt request.
5:3	0	Reserved. Always write 0.
2	Signed	1 = Data is in signed, two's complement format. 0 = Unsigned data.
1	Stereo/ mono	1 = Stereo data. This format is reserved for Interleave mode when using the DSP serial interface. 0 = Mono data.
0	16-bit/ 8-bit	1 = 16-bit samples. 0 = 8-bit samples.

Audio 2 DAC Mixer Volume (7Ch, R/W)

Left channel volume				Right channel volume			
7	6	5	4	3	2	1	0

This register is reset to zero by hardware reset.

Mic Preamp, MONO_IN and MONO_OUT (7Dh, R/W)

0	0	0	0	Enable +26 dB mic amp	MONO_OUT source select		Enable MONO_IN mix with AOUT_L/R
7	6	5	4	3	2	1	0

This register is reset to 08h by hardware reset.

Bit Definitions:

Bits	Name	Description
7:4	0	Reserved. Always write 0.
3	Enable +26 dB mic amp	1 = Enable +26 dB microphone preamp gain. 0 = Mic preamp is 0 dB.
2:1	MONO_OUT source select	Bit 2 Bit 1 0 0 Mute (CMR) 0 1 CIN_R pin (1st channel DAC, right channel playback, after filter stage). 1 0 2nd channel DAC, right channel output. 1 1 Mono mix of left and right record level stage outputs. MONO_OUT is controlled by record source select and record level registers.
0	Enable MONO_IN mix with AOUT_L/R	1 = MONO_IN is mixed with AOUT_L and AOUT_R after playback mixer, Spatializer, and master volume stages. Mix is unity gain.

I²S Interface (7Fh, R/W)

Reserved			Music digital record	I²S data activity	I²S clock activity	MODE pin	Enable I²S connect to music DAC
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:5	–	Reserved.
4	Music digital record	1 = Enable direct digital recording of Music DAC data (including FM, ES689/ES69x, or I²S). In this mode, the first DMA channel must be enabled for stereo recording. The sample rate is determined by the music DAC sample rate rather than by controller register A1h.
3	I²S data activity	This bit is set high if IISDATA has been high at least once since it was last cleared by software.
2	I²S clock activity	This bit is set high if both IISCLK and IISLR have been high at the same time at least once since the last time it was last cleared by software.
1	MODE pin	(Read-only) state of MODE input pin. This pin must be high for the I²S serial interface to be enabled.
0	Enable I²S con-nect to Music DAC	1 = Enable I²S serial interface to acquire control of music DAC. 0 = Allow FM synthesizer or ES689/ES69x serial interface to use DAC.

Controller Registers

This is a summary and description of the controller registers. These registers are written to and read from using commands of the format Axh or Bxh. To enable access to these registers send the command C6h.

Table 25 ESS Controller Registers Summary

Reg	D7	D6	D5	D4	D3	D2	D1	D0	Description
A1h	Clock source	Sample rate divider							
A2h	Filter clock divider								S/W reset, setup for 8 kHz sampling
A4h	DMA transfer counter reload – low byte								
A5h	DMA transfer counter reload – high byte								
A8h	0	0	0	1	Enable record monitor	0	Mono/stereo select		Analog control
B1h	Game compatible IRQ	Enable IRQ ovf Ext mode DMA cntr	Enable IRQ for FIFO1 HE status edge	x	Audio 1 interrupt				Legacy audio interrupt control
B2h	Game compatible DRQ	Enable DRQ for Ext mode DMA	Enable DRQ game compatible DMA	x	Audio 1 DRQ				Audio DRQ control
B4h	Left Channel Record Level				Right Channel Record Level				Record Level
B5h	DMA direct access holding – low byte								
B6h	DMA direct access holding – high byte								
B7h	Enable FIFO to/from CODEC	Reserved. Set opposite polarity of bit 3	Data type select	1	Stereo/ Mono mode select	16-bit/8-bit mode select	0	1	Audio 1 control 1
B8h	0	0	0	0	Codec mode	DMA mode	DMA read/ write	Trans-fer enable	Audio 1 control 2
B9h	0	0	0	0	0	0	Transfer type		Audio 1 transfer type
BAh	0		Disable time delay on analog wake-up	Sign	Adjust magnitude				Left channel ADC offset adjust
BBh	0			Sign	Adjust magnitude				Right channel ADC offset adjust

Controller Register Descriptions

Extended Mode Sample Rate Generator (A1h, R/W)

Clock source	Sample rate divider						
7	6	5	4	3	2	1	0

This register should be programmed for the sample rate for all DAC operations in Extended mode.

The clock source for the sample rate generator is 397.7 kHz if bit 7 is 0 and 795.5 kHz if bit 7 is 1.

The sample rate is determined by the two's complement divider in bits 7:0.

Sample_Rate = 397.7 kHz / (128-x) if bit 7 = 0.
= 795.5 kHz / (256-x) if bit 7 = 1.

where x = value in bits 7:0 of register A1h.

Bit Definitions:

Bits	Name	Description
7	Clock source	1 = clock source is 795.5 kHz for sample rates higher than 22 kHz. 0 = clock source is 397.7 kHz for sample rates lower than or equal to 22 kHz.
6:0	Sample rate divider	Signed sample rate divider.

Filter Divider (A2h, R/W)

Filter clock divider							
7	6	5	4	3	2	1	0

This register controls the low-pass frequency of the switch-capacitor filters inside the ES1869. Generally, the filter roll-off should be positioned at 80% - 90% of the Sample_Rate/2 frequency. The ratio of the roll-off frequency to the filter clock frequency is 1:82. In other words, first determine the desired roll-off frequency by taking 80% of the Sample_Rate divided by 2, then multiply by 82 to find the desired filter clock frequency. Use the formula below to determine the closest divider:

Filter_Clock_Frequency = 7.16 MHz / (256-Filter_Divider_Register)

DMA Transfer Count Reload (A4h, R/W)

DMA transfer count reload – low byte							
7	6	5	4	3	2	1	0

On reset, this register assumes the value of 00h.

DMA Transfer Count Reload (A5h, R/W)

DMA transfer count reload – high byte							
7	6	5	4	3	2	1	0

On reset, this register assumes the value of F8h.

The FIFO control logic of the ES1869 has a 16-bit counter for controlling transfers to and from the FIFO. These registers are the reload value for that counter which is the value that gets copied into the counter after each overflow (plus at the beginning of the initial DMA transfer). The counter is incremented after each successful byte is transferred by DMA. Since the counter counts up towards FFFFh and then overflows, the reload value is in two's complement form.

For Auto-Initialize mode DMA, the counter is used to generate interrupt requests to the system processor. In this mode, the ES1869 allows continuous DMA. In a typical application the counter is programmed to be one-half of the DMA buffer maintained by the system processor. In this application an interrupt is generated whenever DMA switches from one half of the circular buffer to the other.

For Normal mode DMA, DMA requests are halted at the time that the counter overflows, until a new DMA transfer is commanded by the system processor. Again, an interrupt request is generated to the system processor if bit 6 of register B1h is set high.

Analog Control (A8h, R/W)

0	0	0	1	Record monitor enable	0	Stereo/mono select	
7	6	5	4	3	2	1	0

When programming the FIFO for DMA playback modify only bits 1:0. When programming the FIFO for DMA record modify only bits 3, 1, and 0. Read this register first to preserve the remaining bits.

Bit Definitions:

Bits	Name	Description
7:5	0	Reserved. Always write 0.
4	1	Reserved. Always write 1.
3	Record monitor enable	1 = Enable record monitor. 0 = Disable record monitor.
2	0	Reserved. Always write 0.
1:0	Stereo/ mono select	Select operation mode of first DMA converters. Bit 1 Bit 0 Mode 0 0 Reserved 0 1 Stereo 1 0 Mono 1 1 Reserved

Legacy Audio Interrupt Control (B1h, R/W)

Game compatible IRQ	Enable IRQ ovf Ext mode DMA cntr	Enable IRQ for FIFO1 HE status edge	x	Audio 1 interrupt			
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7	Game compatible IRQ	Reserved for Compatibility mode. Leave zero for Extended mode.
6	Enable IRQ ovf Ext mode DMA cntr	Set high to receive interrupts for each overflow of the ES1869 DMA counter in Extended mode.
5	Enable IRQ for FIFO1 HE status edge	Set high to receive interrupts for FIFO Half-Empty transitions when doing block I/O to/ from the FIFO in Extended mode.
4	–	No function. The audio device activate bit serves the purpose of enabling the interrupt pin.
3:0	Audio 1 interrupt	Read-only. Decode the selected interrupt number for the first audio interrupt as follows: Bit 3 Bit 2 Bit 1 Bit 0 Audio 1 Interrupt 0 0 0 0 2, 9, all others 0 1 0 1 5 1 0 1 0 7 1 1 1 1 10

DRQ Control (B2h, R/W)

Game compatible DRQ	Enable DRQ for Extended mode DMA	Enable DRQ game compatible DMA	x	Audio 1 DRQ			
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7	Game compatible DRQ	Reserved for Compatibility mode. Leave zero for Extended mode.
6	Enable DRQ for Extended mode DMA	1 = Enable DRQ outputs and DACKB inputs for DMA transfers in Extended mode. 0 = Enable block I/O to/from the FIFO in Extended mode.
5	Enable DRQ game compatible DMA	Reserved for Compatibility mode. Leave zero for Extended mode.
4	–	No function. The DRQ lines always drive (there is no enable). If neither bit 5 nor bit 6 are set high, the first audio DRQ is always low.
3:0	Audio 1 DRQ	Read-only. The selected DMA channel number for the first audio DMA channel are decoded to set these bits as follows:

Bit 3	Bit 2	Bit 1	Bit 0	Audio 1 DRQ
0	1	0	1	0
1	0	1	0	1
1	1	1	1	3
0	0	0	0	all others

Record Level (B4h, R/W)

Left channel record level				Right channel record level			
7	6	5	4	3	2	1	0

Register B4h allows for independent left and right record level. Each channel has 16 levels (excluding mute). The amount of gain or attenuation for each level is different for microphone than for all other sources. The record levels are listed in the following table.

Record Level	Gain for Mic	Gain for Other Sources
0	+0 dB	-6.0 dB
1	+1.5 dB	-4.5 dB
2	+3.0 dB	-3.0 dB
3	+4.5 dB	-1.5 dB
4	+6.0 dB	0 dB
5	+7.5 dB	+1.5 dB
6	+9.0 dB	+3.0 dB
7	+10.5 dB	+4.5 dB
8	+12.0 dB	+6.0 dB
9	+13.5 dB	+7.5 dB
10	+15.0 dB	+9.0 dB
11	+16.5 dB	+10.5 dB
12	+18.0 dB	+12.0 dB
13	+19.5 dB	+13.5 dB
14	+21.0 dB	+15.0 dB
15	+22.5 dB	+16.5 dB

DAC Direct Access Holding (B5h, R/W)

DAC direct access holding – low byte							
7	6	5	4	3	2	1	0

Low byte of DAC direct access holding register. Because the bus between the ISA bus and the FIFO is only 8 bits wide, the ES1869 needs a location for storage of 16-bit data. Registers B5h and B6h serve this function.

DAC Direct Access Holding (B6h, R/W)

DAC direct access holding – high byte							
7	6	5	4	3	2	1	0

High byte of DAC direct access holding register. Because the bus between the ISA bus and the FIFO is only 8 bits wide, the ES1869 needs a location for storage of 16-bit data. Register B5h and B6h serve this function.

Audio 1 Control 1 (B7h, R/W)

Enable FIFO to/from CODEC	Set opposite bit 3	FIFO signed mode	1	FIFO stereo mode	FIFO 16-bit mode	0	Generate load signal
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7	Enable FIFO to/from CODEC	1 = Enable first DMA FIFO connection to DAC or ADC. This allows transfers to/from the FIFO and the analog circuitry. 0 = Disable first DMA FIFO connection to DAC or ADC.
6	Set opposite bit 3	Reserved function. This bit must be set to the opposite polarity of bit 3: high for mono and low for stereo.
5	FIFO signed mode	1 = First DMA FIFO two's complement mode (signed data). 0 = First DMA FIFO unsigned (offset 8000).
4	1	Reserved. Always write 1.
3	FIFO stereo mode	1 = First DMA FIFO stereo mode. 0 = First DMA FIFO mono mode. Bit 6 must be set at the opposite polarity of this bit: high for mono, low for stereo.
2	FIFO 16-bit mode	1 = First DMA FIFO 16-bit mode. 0 = First DMA FIFO 8-bit mode.
1	0	Reserved. Always write 0.
0	Generate load signal	Write 1. Generates a load signal that copies DAC Direct Access Holding register to DAC on the next sample rate clock edge (sample rate is determined by Extended mode register A1h). This bit is cleared after the holding register is copied to the DAC.

Audio 1 Control 2 (B8h, R/W)

0	0	0	0	CODEC mode	DMA mode	DMA read enable	DMA transfer enable
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:4	0	Reserved. Always write 0.
3	CODEC mode	1 = first DMA converter in ADC mode. 0 = first DMA converter in DAC mode.
2	DMA mode	1 = auto-initialize mode. 0 = normal DMA mode.
1	DMA read enable	1 = first DMA is read (e.g. for ADC operation). 0 = first DMA is write (e.g. for DAC operation).
0	DMA transfer enable	First DMA active-low reset. When high, first DMA is allowed to proceed.

Audio 1 Transfer Type (B9h, R/W)

0	0	0	0	0	0	DMA transfer type select	
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:2	0	Reserved. Always write 0.
1:0	DMA transfer type select	Selects the DMA transfer type for the first DMA:

Bit 1	Bit 0	Transfer Type	Bytes/DMA Request
0	0	Single	–
0	1	Demand	2
1	0	Demand	4
1	1	Reserved	–

Left Channel ADC Offset Adjust (BAh, R/W)

0	0	Disable time delay on analog wake-up	Sign	Adjust magnitude			
7	6	5	4	3	2	1	0

This register is reset to zero by hardware reset and is unaffected by software reset.

Bit Definitions:

Bits	Name	Description
7:6	0	Reserved. Always write 0.
5	Disable time delay on analog wake-up	Normally, the AOUT_L and AOUT_R pins are muted for 100 msec ± 20 msecs after hardware reset or after the analog sub-systems wake from power-down. Set high to disable delay. This bit is cleared by hardware reset.
4:0	Sign/Adjust magnitude	See the explanation for bits 4:0 following register BBh.

Right Channel ADC Offset Adjust (BBh, R/W)

0	0	0	Sign	Adjust magnitude			
7	6	5	4	3	2	1	0

This register is reset to zero by hardware reset and is unaffected by software reset.

Bit Definitions:

Bits	Name	Description
7:5	0	Reserved. Always write 0.
4:0	Sign/Adjust magnitude	See the following explanation for bits 4:0.

Bits 4 (sign) and 3:0 (adjust magnitude) of the ADC Offset Adjust registers cause a constant value to be added to the ADC converter output, as shown in the following:

Code	Offset	Code	Offset
00h	0	10h	-64
01h	+64	11h	-128
02h	+128	12h	-192
03h	+192	13h	-256
04h	+256	14h	-320
05h	+320	15h	-384
06h	+384	16h	-448
07h	+448	17h	-512
08h	+512	18h	-576
09h	+576	19h	-640
0Ah	+640	1Ah	-704
0Bh	+704	1Bh	-768
0Ch	+768	1Ch	-832
0Dh	+832	1Dh	-896
0Eh	+896	1Eh	-960
0Fh	+960	1Fh	-1024

Formula:

bit 4 = 0: offset = 64 * bits[3:0]

bit 4 = 1: offset = -64 * (bits[3:0] +1)

To calculate the offset adjust code, first measure the ADC offset for both right and left channels before adjustment by following these steps:

1. Program Extended mode registers BAh and BBh bits 4:0 to be zero (no digital offset).
2. Select a zero-amplitude (or low amplitude) recording source.
3. Set the recording volume to minimum by setting Extended mode register B4h to zero.
4. Make a stereo 16-bit two's complement recording at 11 kHz sample rate of 2048 stereo samples (2048 stereo samples = 4096 words = 8192 bytes, which is about 190 milliseconds).
5. Use the last 1024 stereo samples to calculate a long term average for both left and right channels.
6. With this average DC offset, calculate the best digital offset to bring the sum closest to zero, using the codes and offsets listed in the table above.

AUDIO MICROCONTROLLER COMMAND SUMMARY

Table 26 Command Summary

Command	Data Byte(s) Write/Read	Function
10h	1 write	Direct write 8-bit DAC. Data is 8-bit unsigned format.
11h	2 writes	Direct write 16-bit DAC. Data is 16-bit unsigned format, first low byte then high byte.
14h	2 writes	Start Normal mode DMA for 8-bit DAC transfer. Data is transfer count - 1, least byte first. Stereo DAC transfer if stereo flag is set in mixer register 0Eh. Maximum sample rate is 44 kHz mono, 22 kHz stereo.
15h	2 writes	Start Normal mode DMA for 16-bit DAC transfer. Data is transfer count - 1, least byte first. Stereo DAC transfer if stereo flag is set in mixer register 0EH. Maximum sample rate is 22 kHz mono, 11 kHz stereo.
1Ch		Start Auto-Initialize mode DMA for 8-bit DAC transfer. Block size must be previously set by command 48h. Stereo DAC transfer if stereo flag is set in mixer register 0Eh. Maximum sample rate is 44 kHz mono, 22 kHz stereo.
1Dh		Start Auto-Initialize mode DMA for 16-bit DAC transfer. Block size must be previously set by command 48h. Stereo DAC transfer if stereo flag is set in mixer register 0Eh. Maximum sample rate is 22 kHz mono, 11 kHz stereo.
20h	1 read	Direct mode 8-bit ADC. Data is 8-bit unsigned. Firmware controlled input volume for AGC.
21h	2 reads	Direct mode 16-bit ADC, returns least byte first. Data is 16-bit unsigned format. Input volume controlled by command DDh.
24h	2 writes	Start Normal mode DMA for 8-bit ADC transfer. Data is transfer count - 1, least byte first. Firmware controlled input volume for AGC. Maximum sample rate is 22 kHz: use command 99h for higher rates up to 44 kHz.
25h	2 writes	Start Normal mode DMA for 16-bit ADC transfer. Data is transfer count - 1, least byte first. Input volume controlled via command DDh. Maximum sample rate is 22 kHz.
2Ch		Start Auto-Initialize mode DMA for 8 bit ADC transfer. Block size must be previously set by command 48h. Firmware controlled input volume for AGC. Maximum sample rate is 22 kHz: use command 98h for higher rates up to 44 kHz.
2Dh		Start Auto-Initialize mode DMA for 16-bit ADC transfer. Block size must be previously set by command 48h. Input volume is controlled by command DDh. Maximum sample rate is 22 kHz.
30h/31h		MIDI input mode. Detects MIDI serial input data and transfers to data register, setting Data-Available flag in register Audio_Base+Eh. Command 31h will also generate an interrupt request for each byte received. Exit MIDI input mode by executing a write to port Audio_Base+Ch. The data written is ignored. A software reset will also exit this mode.
34h/35h		MIDI UART mode. Acts like commands 30h/31h, except that any data written to Audio_Base+Ch will be transmitted as MIDI serial output data. The only way to exit this mode is through software reset.
38h	1 write	MIDI output. Transmit one byte.
40h	1 write	Set time constant, X, for timer used for DMA mode DAC/ADC transfers: rate = 1 MHz / (256-X) X must be less than or equal to 233. For stereo DAC, program sample rate for twice the per-channel rate.
41h	1 write	Alternate set time constant, X: rate = 1.5 MHz / (256-X) This command provides more accurate timing for certain rates such as 22,050. X must be less than equal to 222. For stereo DAC, program sample rate for twice the per-channel rate.
42h	1 write	Set filter clock independently of timer rate. (note that the filter clock is automatically set by commands 40h/41h) Filter clock rate: rate = 7.16E6 / (256-X) The relationship between the low-pass filter -3 dB point and the filter clock rate is approximately 1:82.
48h	2 writes	Set block size-1 for high speed mode and auto-init mode transfer, least byte first.

Table 26 Command Summary (Continued)

Command	Data Byte(s) Write/Read	Function
64h	2 writes	Start **ESPCM**® 4.3-bit (low compression) format DMA transfer to DAC. Data is transfer count - 1, least byte first.
65h	2 writes	Same as command 64h, except with reference byte flag.
66h	2 writes	Start **ESPCM**® 3.4-bit (medium compression) format DMA transfer to DAC. Data is transfer count - 1, least byte first.
67h	2 writes	Same as command 66h, except with reference byte flag.
6Ah	2 writes	Start **ESPCM**® 2.5-bit (high compression) format DMA transfer to DAC. Data is transfer count - 1, least byte first.
6Bh	2 writes	Same as command 6Ah, except with reference byte flag.
6Eh	2 writes	Start **ESPCM**® 4.3-bit (low compression) format ADC, compression, and DMA transfer. Data is transfer count - 1, least byte first.
6Fh	2 writes	Same as command 6Eh, except with reference byte flag.
74h	2 writes	Start ADPCM 4-bit format DMA transfer to DAC. Data is transfer count - 1, least byte first.
75h	2 writes	Same as command 74h, except with reference byte flag.
76h	2 writes	Start ADPCM 2.6-bit format DMA transfer to DAC. Data is transfer count - 1, least byte first.
77h	2 writes	Same as command 76h, except with reference byte flag.
7Ah	2 writes	Start ADPCM 2-bit format DMA transfer to DAC. Data is transfer count - 1, least byte first.
7Bh	2 writes	Same as command 7Ah, except with reference byte flag.
80h	2 writes	Generate silence period. Data is number of samples - 1.
90h		Start Auto-Initialize DMA 8-bit transfer to DAC. Transfer count must be previously set by command 48h.
91h		Start DMA 8-bit transfer to DAC. Transfer count must be previously set by command 48h.
98h		Start High-Speed mode, Auto-Initialize, DMA 8-bit transfer from ADC. Transfer count must be previously set by command 48h. There is no AGC. Input volume is controlled with command DDh. Maximum sample rate is 44 kHz.
99h		Start High-Speed mode, DMA 8-bit transfer from ADC. Transfer count must be previously set by command 48h. There is no AGC. Input volume is controlled with command DDh. Maximum sample rate is 44 kHz.
Axh, Bxh, Cxh		(where x = 0 to Fh) ES1869 extension commands. Many of these commands are used to access the ES1869's controller registers. For information on these registers, see the register descriptions.
C1h		Resume after suspend.
C6h		Enable ES1869 Extension commands Axh, Bxh. Must be issued after every reset.
C7h		Disable ES1869 Extension commands Axh, Bxh.
CEh	1 read	Read GPO0/1 Power Management register
CFh	1 write	Write GPO/1 Power Management register
D0h		Pause DMA. Internal FIFO operations continue until the FIFO is empty (DAC transfer) or full (ADC transfer). It is not necessary to use this command to stop DMA if the transfer is completed normally and the end-of-DMA interrupt is generated.
D1h		Enable Audio 1 DAC input to mixer.
D3h		Disable Audio 1 DAC input to mixer.
D4h		Continue DMA after command D0h.
D8h	1 read	Return Audio 1 DAC enable status: 0=disabled FFh=enabled

Table 26 Command Summary (Continued)

Command	Data Byte(s) Write/Read	Function
DCh	1 read	Return current input gain, 0-15, (valid during 16-bit ADC and 8-bit “high speed mode” ADC).
DDh	1 write	Write current input gain, 0-15, (valid during 16-bit ADC and 8-bit “high speed mode” ADC).
E1h	2 reads	Return version number high (3), followed by version number low (1). This indicates Sound Blaster Pro compatibility.
E7h	2 reads	Returns bytes 68h 8xh, where x is the version code. The version code, x, is less than 8 for the ES688, and greater than or equal to 8 for a device such as the ES1869. Use mixer register 40h to properly identify the ES1869 (page 61).
F2h		Generate an interrupt for test purposes.
FDh		Forces power-down. Software or hardware reset. Required for wake-up.

POWER MANAGEMENT

Overview

The ES1869 supports three power states:

- full power-up
- partial power-down
- full power-down

The system processor decides whether to power down partially or fully. Activity flags monitored by the system processor are available to track I/O activity to and from the ES1869. After a predetermined idle period, the system processor can command the ES1869 to power down partially or fully.

If the oscillator clock is provided from an external circuit, automatic wake-up upon I/O activity is available. With the automatic wake-up feature, the act of reading or writing to an ES1869 I/O port causes the chip to immediately power up without losing context from partial or fully powered-down states.

If the oscillator clock is provided by a crystal, automatic wake-up from partial power-down is available because the oscillator continues to run as long as the ES1869 is not fully powered down. Once the chip is fully powered down, however, automatic wake-up is not available with a crystal oscillator due to the start-up requirements of the oscillator itself. System software must then provide for a start-up period for the oscillator before returning control to the application programs that may access the ES1869. There is no loss of context in either case.

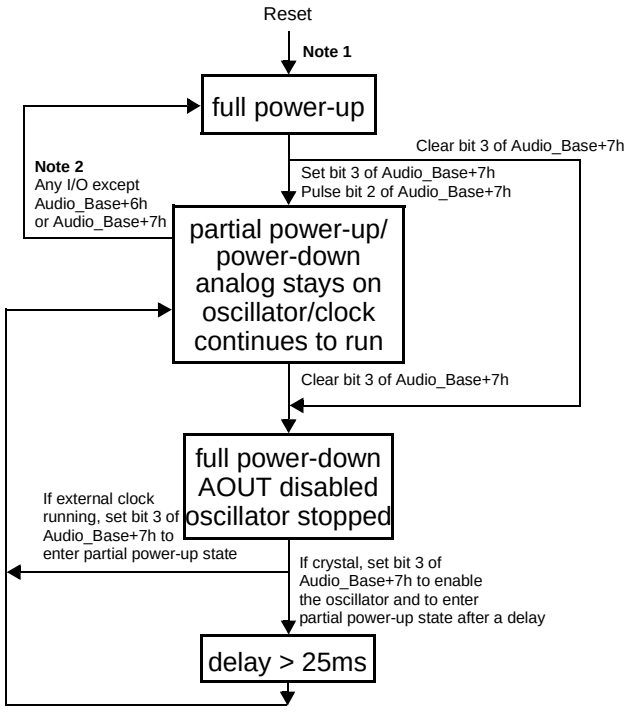


Figure 22 Summary of Power States in the ES1869

Note 1: After return to full power-up state from full power-down state, the AOUT_L and AOUT_R analog output pins are not enabled for 48 to 64 milliseconds. The chip should remain in the full power-up state for at least 64 milliseconds to be sure the AOUT_L and AOUT_R pins are enabled before changing to the partial power-down state. Otherwise the AOUT_L and AOUT_R pins may never get enabled. For this reason it is not possible to go directly from full power-down to partial power-down and have AOUT_L and AOUT_R enabled.

Note 2: A low input on any of the three hardware volume control pins (VOLUP, VOLDN, or MUTE) also acts as a wake-up event.

Mode	Description	Notes
0	Full power-down. Crystal oscillator disabled. AOUT_L and AOUT_R held at approximately CMR by high value resistors.	All inputs static at VDDD or GND.
1	Partial power-down. Joystick, MPU-401 are up. Audio, FM, ES689/ES69x interface, and DSP serial interface are down.	Digital standby.
2	Full power-up. This is the state after hardware reset.	Normal operating conditions.

Partial Power-Down

When the ES1869 is in the partial power-down state, the power supply remains connected to the chip during power-down and the chip's analog section remains active while the digital circuits are mostly inactive.

The total current used by the ES1869 can be reduced by a factor of two or more by putting the ES1869 in a partial power-down state. The crystal oscillator, if used, continues to operate. The analog circuitry remains powered up so that AUXA_L, AUXA_R, AUXB_L, AUXB_R, LINE_L, LINE_R, and MIC audio sources can continue to be heard. FM and DAC audio are automatically muted. No pops should occur when returning from partial power-down to full power-up state.

The following items are active during partial power-down operation:

- Oscillator is enabled.
- MPU-401 operates.
- PnP operates.
- Configuration device operates.
- H/W volume operates.
- Mixer operates.
- Analog operates.
- Joystick operates.
- Audio device is disabled, FM disabled.
- Automatic wake-up with any I/O activity to FM or audio registers except Audio_Base+4h, Audio_Base+5h, Audio_Base+6h, Audio_Base+7h.

Causing Partial Power-Down

To enter partial power-down mode, bit 3 of port Audio_Base+7h must be high and must remain high while pulsing bit 2 high, then low.

Example:

Powering down the ES1869 using system software timer interrupt:

In this example, it is assumed that the ES1869 is not using a crystal for its clock.

From a timer interrupt routine, read Audio_Base+6h to monitor activity. After one minute of I/O inactivity, you decide that you want the ES1869 to power down completely, then return from a timer interrupt. The ES1869 wakes up automatically upon any I/O access to the ES1869 by any application.

1. See if the ES1869 is already powered down (bit 3 of port Audio_Base+6h = 0). If so, there is nothing to do.
2. Check if the ES1869 is being held in reset by reading bit 0 of port Audio_Base+6h. If bit 0 is high, the reset must be released before power-down can occur: Clear bit 0 of port Audio_Base+6h, then delay 1 millisecond or more for the ES1869 processor to complete its initialization.
3. Check to see if the ES1869 is in MIDI serial interface mode by testing bit 2 of port address Audio_Base+6h. If so, it may not be prudent to power-down. While the ES1869 can power-down when in MIDI mode, it does not automatically wake up if serial data comes in to the MSI pin, and such data will be lost.
4. Send a power-down request to the chip by clearing bit 3 in port Audio_Base+7h, then pulsing bit 2 high, then low. The other bits of this register should be preserved. The ES1869 processor sees the rising edge of bit 2 of port Audio_Base+7h as an interrupt request to power-down.

Waking from Partial Power-Down

Any I/O activity, except Audio_Base+6h or Audio_Base+7h, automatically wakes the ES1869 from a partial power-down.

A low input on any of the three hardware volume control pins (VOLUP, VOLDN, or MUTE) also acts as a wake-up event.

Full Power-Down

Complete power-down reduces the operating current to less than 50 microamps.

The following items are indicators of full power-down operation:

- Nothing operates, except for some programmed I/O.
- The activity flags from a port Audio_Base+6h read are:

Bits	Name	Description
7	Act flag 2	Activity latch PnP, Joystick, MPU-401, Configuration, CD-ROM, Modem, or GPI/O or DMA activity.
6	Act flag 1	Activity latch: Audio_Base+4h, Audio_Base+5h I/O.
5	Act flag 0	Activity latch: Audio (except Audio_Base+4h, Audio_Base+5h, Audio_Base+6h read, Audio_Base+7h read/write), FM I/O or DMA.
4	Serial act	DSP and ES689/ES69x serial activity status.

Waking from Full Power-Down

There are three main ways to wake the chip up from full power-down:

- Hardware reset
- Software reset
- I/O activity

Hardware Reset

The chip is automatically restored to activity upon a hardware reset. Context is not preserved.

Software Reset

Refer to the section “Resetting the ES1869 by Software” on page 44 for information on the software reset sequence.

I/O Activity Causing Wake-Up

Wake-up is triggered by DMA accesses. However, this is unlikely if power-down is triggered by a period of I/O inactivity, which includes DMA accesses and the I/O operations required to set up the DMA transfer.

In the full power-down state the oscillator is stopped and the analog circuitry is powered down. The AOUT_L and AOUT_R pins are left at approximately the reference voltage by a high value resistor divider.

To wake the chip from a total power-down and enter the partial power-down state, set bit 3 of port Audio_Base+7h high for 25 milliseconds to allow the oscillator some time to stabilize. Any I/O activity, except Audio_Base+6h or Audio_Base+7h will automatically wake the ES1869 from a partial power-down.

Inputs and Outputs During Power-Down

When powered-down, digital inputs that do not have pull-up or pull-down devices should be driven high or low, and should not be left floating. Examples of such pins are A[11:0] and AEN.

Some input pins have circuitry that provides a pull-down device when the ES1869 digital circuits are powered up. During power-down, these inputs have a feedback device that latches the input state and prevents leakage current into the pin, effectively disabling the pull-down device. SE and DR are pins that have this feature.

The CE pin has a similar feature using a pull-up device rather than a pull-down device.

Output pins such as DRQx and IRQx are frozen in their state at power-down.

GPO0 and GPO1 can change state during full power-down if so programmed (see the section entitled “General-Purpose Outputs and Power-Down” on page 79).

The MSI pin has an internal pull-up device, so this pin can be left floating during power-down.

The internal inverter connected to pins XI and XO continues to operate when the digital portion of the ES1869 is powered-down as long as:

- SCLK is high
- The analog portion is powered-up

When the chip is fully powered-down, the inverter becomes high-impedance with a weak pull-up on the XO pin.

CMR is pulled low by an internal transistor during analog power-down.

The AOUT_L and AOUT_R pins are held at approximately the idle voltage level with a high-impedance resistor divider. After return to full power-up state from full power-down state, these pins are not enabled for 48-64 milliseconds. The chip remains in full power-up state for at least 64 milliseconds to assure that the AOUT_L and AOUT_R pins are enabled before changing to the partial power-down state. Otherwise they may never get enabled. For this reason it is not possible to go directly from full power-down to partial power-down and have AOUT_L and AOUT_R enabled.

Suspend/Resume

In suspend/resume, power is removed from the ES1869 during its suspended state. Before removing power, the entire context of the microcontroller and registers must be uploaded to the system processor and saved. After restoring power and generating a hardware reset, the opposite resume operation downloads the context.

The term “suspend” is used here to describe the process of uploading the context of the ES1869 and removing digital and analog power to the chip. The term “resume” describes the process of applying power to the ES1869 and downloading the context.

The ES1869 requires 782 (decimal) bytes to store its entire context.

It is possible to suspend the ES1869 regardless of its current state. This includes suspending in the middle of a DMA transfer.

To suspend operation of the ES1869, pulse bit 7 of port address Audio_Base+7h high, then low. This interrupts the ES1869 microcontroller and begins a sequence of upload operations.

To resume operation of the ES1869, a hardware reset is required before downloading the context. Downloading the context is initiated with command C1h. Before sending the download command, send the C6h command to enable access to the Extension commands.

Pop Prevention in the External Amplifier

Normally, to directly drive speakers in an ES1869 design, an external stereo amplifier chip is used. There are two power management problems associated with an external amplifier:

1. The amplifier itself draws current unless it can be powered down.
2. Suspend/resume causes pops because power is removed from the ES1869 and then re-applied.

Amplifiers such as the SGS/Thomson TDA7233 have a mute input which reduces current to 400 microamps and also reduces pops from the suspend/resume process. This part is a mono amplifier, so two are required. Connect GPO0 to the active-low MUTE input of the TDA7233. In this case the amplifier is muted after hardware reset. During start-up, program the ES1869 so that GPO0 is high when powered-up and low when fully powered-down. Program a delay of about 133 milliseconds between power-down and power-up states, before GPO0 returns high, to allow the ES1869 analog circuits to stabilize.

Power Management and the FM Synthesizer

The ES1869 FM synthesizer is a fully static design. This means that the clock can be stopped to power-down the circuitry without loss of the state. For suspend/resume applications, the entire context of the synthesizer can be read back.

Self-Timed Power-Down

The ES1869 microcontroller can be programmed to monitor I/O activity in place of the system processor, and after a programmable period of inactivity, enter either a partial or full power-down state.

In self-timed power-down, power is maintained as for partial or full power-down, except the decision to power-down is made by the ES1869 itself. The ES1869 microcontroller waits for a pre-programmed period of I/O inactivity between successive commands before entering partial or full power-down state.

The ES1869 requires use of the activity flags in register Audio_Base+6h. Therefore, if this feature is enabled, the system processor cannot monitor I/O activity.

Enabling Self-Timed Power-Down

1. Send command C6h to enable access to the controller registers.
2. Send command BDh.
3. Send the time out value N, where the time period is N x 8 seconds. If the value N is zero, self-timed power-down is disabled.
4. Send command C7h to disable access to the controller registers.

Whether the ES1869 enters partial or full power-down is determined by bit 3 of port Audio_Base+7h.

Even if self-timed power-down is enabled, the ES1869 can be commanded to power-down by bit 2 of port Audio_Base+7h.

There is one limitation to this feature. The timing of inactivity only occurs between commands sent to the ES1869. A program may leave the ES1869 in a state where timing will not happen, such as if it exits without completion of a DMA transfer. However, most programs will leave the ES1869 with appropriate registers defined.

General-Purpose Outputs and Power-Down

The ES1869 has the ability to have one or both of the general-purpose outputs GPO0 and GPO1 change state when the ES1869 is powered-down.

After hardware reset, this feature is disabled and the general-purpose outputs are not affected by power-down. A controller register in the ES1869 must be programmed to enable this feature. Specifically, the GPO Power-Down Control register is set by writing the command CFh to port Audio_Base+Ch followed by the data. To read the GPO Power-Down Control register write the command CEh to Audio_Base+Ch and read the data from port Audio_Base+Ah. This register should be set once by system software after system reset. This register is unaffected by soft resets. Using this register, one or both of the general-purpose outputs can be programmed to be inverted from their normal state during power-down. The normal state of each pin is set by the appropriate bits 1:0 of port Audio_Base+7h. A further feature allows the inverted outputs to return to their normal state immediately after power-up or after a programmed delay after power-up.

GPO Power-Down Register

Restore GPO1 timed	Invert GPO1 at PDN	Restore GPO0 timed	Invert GPO0 at PDN	0	T2	T1	T0
7	6	5	4	3	2	1	0

On reset, this register assumes the value of 00h. This means that GPO0 and GPO1 are unaffected by the power-down status; that is, they remain in the state programmed into port Audio_Base+7h.

NOTE: "Power-down" as used in this document refers to full power-down, i.e., when both the analog and digital parts of the ES1869 are powered-down.

Bits Definitions:

Bits	Name	Description
7	Delay GPO1 state return enable	1 = Delay GPO1's return to its normal state as determined by port Audio_Base+7h bit 1. The time delay is determined by bits 2:0, described below. 0 = Return GPO1 to its normal state immediately upon wake-up from full power-down.
6	GPO1 invert enable	1 = Invert bit 1 of Audio_Base+7h when entering the full power-down state.
5	Delay GPO0 state return enable	1 = Delay GPO0's return to its normal state as determined by port Audio_Base+7h bit 0. The time delay is determined by bits 2:0, described below. 0 = Return GPO0 to its normal state immediately upon wake-up from full power-down.
4	GPO1 invert enable	1 = Invert bit 0 of Audio_Base+7h when entering the full power-down state.
3	–	Reserved. Always write 0.
2:0	Time delay	The time period is determined by bits [2:0]: A 16 Hz counter starts at 0 and counts until it equals the 3-bit number "time delay". The maximum delay is (Time delay = 7) times (67 msec) or about 469 msec.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Ratings	Symbol	Value	Units
Analog supply voltage	VDDA	-0.3 to 7.0	V
Digital supply voltage	VDDD	-0.3 to 7.0	V
Input voltage	VIN	-0.3 to 7.0	V
Operating temperature range	TA	0 to 70	Deg C
Storage temperature range	TSTG	-50 to 125	Deg C

WARNING: Stressing the device beyond the “Absolute Maximum Ratings” may cause permanent damage. These are stress ratings only. Operation beyond the “Operating Conditions” is not recommended and extended exposure beyond the “Operating Conditions” may affect device reliability.

Thermal Characteristics

The ES1869 was designed to operate at temperatures between 0°C and +70°C.

Operating Conditions

The ES1869 digital and analog characteristics operate under the following conditions:

VDDD	4.5 V to 5.5 V (5 volts ± 10%)
VDDA	4.75 V to 5.25 V (5 volts ± 5%)
TA	25 °C

Operating Current

Operation	Digital	Analog
Full power-up	25 mA	61 mA
Idle (standby)	2.5 mA	61 mA
Full power-down	16 µA	8 µA

Table 27 Digital Characteristics

Parameter	Symbol	Min	Typ	Max	Unit (conditions)
Input high voltage: all inputs except VOLUP,VOLDN,MUTE,PSEL,SW(A-D)	VIH1	2.5 V			VDDD = min
Input high voltage: VOLUP,VOLDN,MUTE,PSEL,SW(A-D)	VIH2	4.0 V			VDDD = min
Input low voltage	VIL		0.8 V		VDDD = max
Output low voltage: all outputs except D[7:0], DRQx, IRQx	VOL1		0.4 V		IOL = 4 mA, VDDD = min
Output high voltage: all outputs except D[7:0], DRQx, IRQx	VOH1	2.5 V			IOH = -3 mA, VDDD = max
Output low voltage: D[7:0], DRQx, IRQx	VOL2		0.4 V		IOL = 16 mA, VDDD = min
Output high voltage: D[7:0], DRQx, IRQx	VOH2	2.5 V			IOH = -12 mA, VDDD = max

Table 28 Analog Characteristics

Parameter	Pins	Min	Typ	Max	Unit (conditions)
Reference voltage	CMR, VREF		2.25		volts
Input Impedance	LINE_L, LINE_R, AUXA_L, AUXA_R, AUXB_L, AUXB_R, MIC		125k		ohms
	CIN_L, CIN_R	35k	50k	65k	ohms
Output impedance	FOUT_L, FOUT_R	3.5k	5k	6.5k	ohms
	AOUT_L, AOUT_R max load for full-scale output		10k		ohms
Input voltage	MIC – preamp ON			125	mVp-p
	– preamp OFF			2.8	Vp-p
	LINE_L, LINE_R, AUXA_L, AUXA_R, AUXB_L, AUXB_R			3.4	Vp-p
Output voltage	AOUT_L, AOUT_R full-scale output range	0.5		VDDA-1.0	Vp-p
Mic preamp gain	MIC		26		decibels

TIMING DIAGRAMS

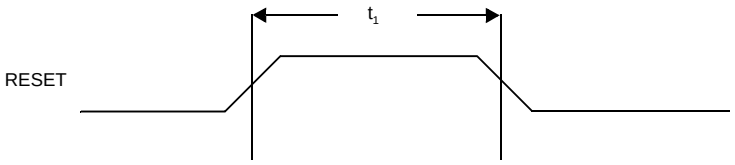


Figure 23 Reset Timing

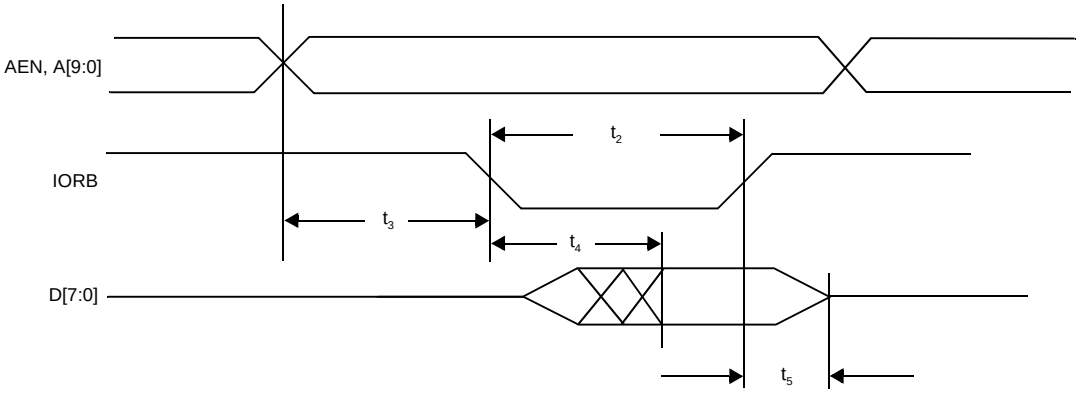


Figure 24 I/O Read Cycle

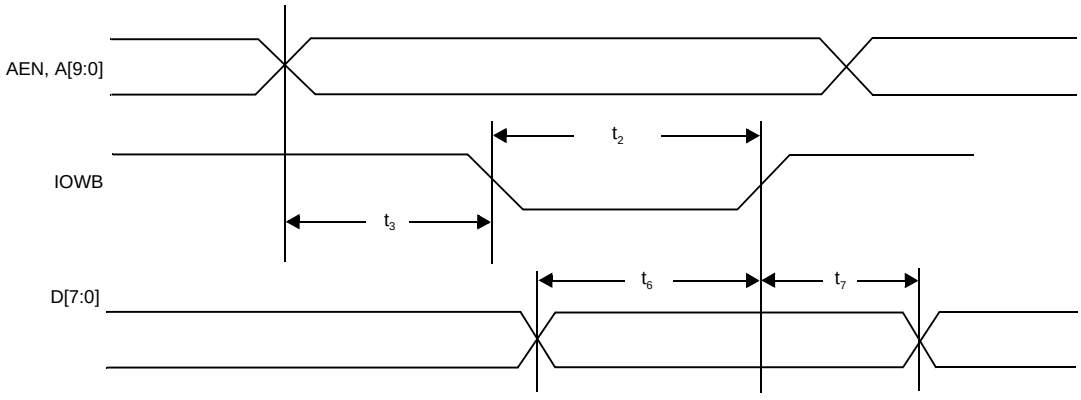


Figure 25 I/O Write Cycle

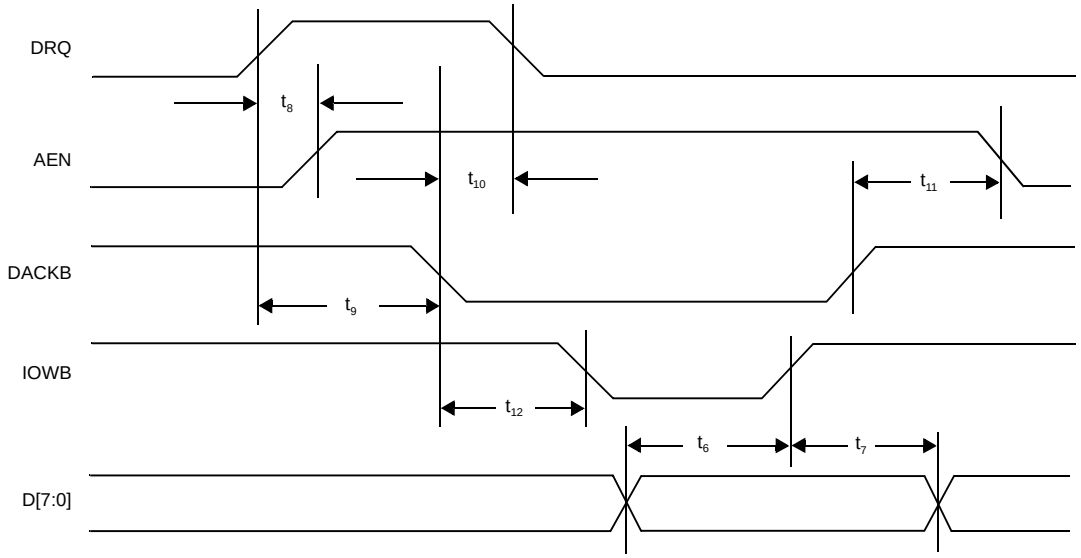


Figure 26 Compatibility Mode DMA Write Cycle

NOTE: In Compatibility mode DMA, the DMA request is reset by the acknowledge signal going low. In Extended mode DMA, the DMA request is reset when the acknowledge signal is low AND the correct command signal is low – either IORB (for DMA read from I/O device) or IOWB (for DMA writer to I/O device). For Extended mode DMA, the time t_{10} is relative to the later of the falling edge of the acknowledge signal, or the command signal.

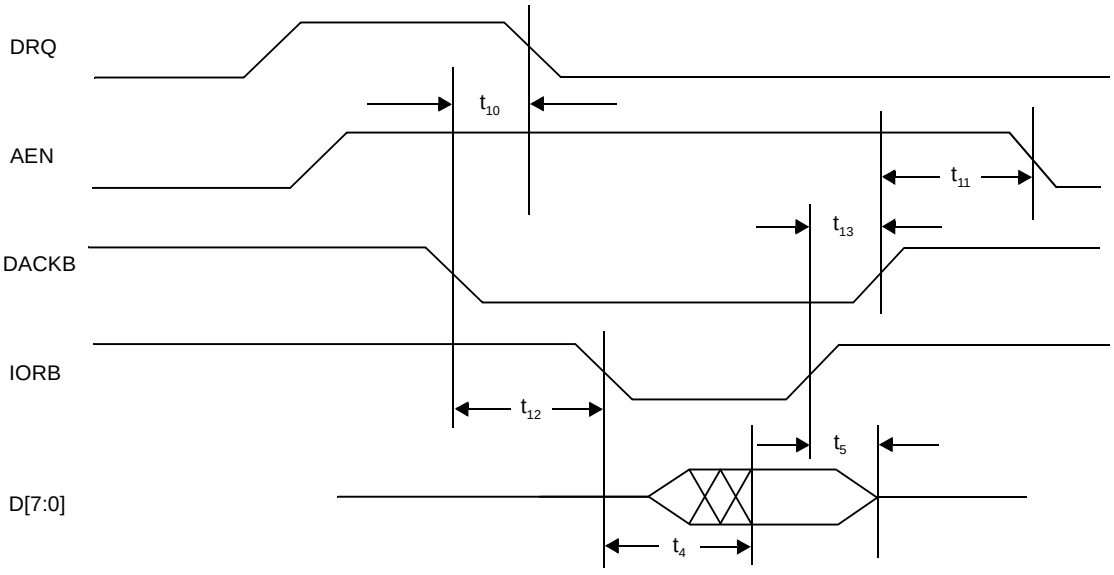


Figure 27 Compatibility Mode DMA Read Cycle

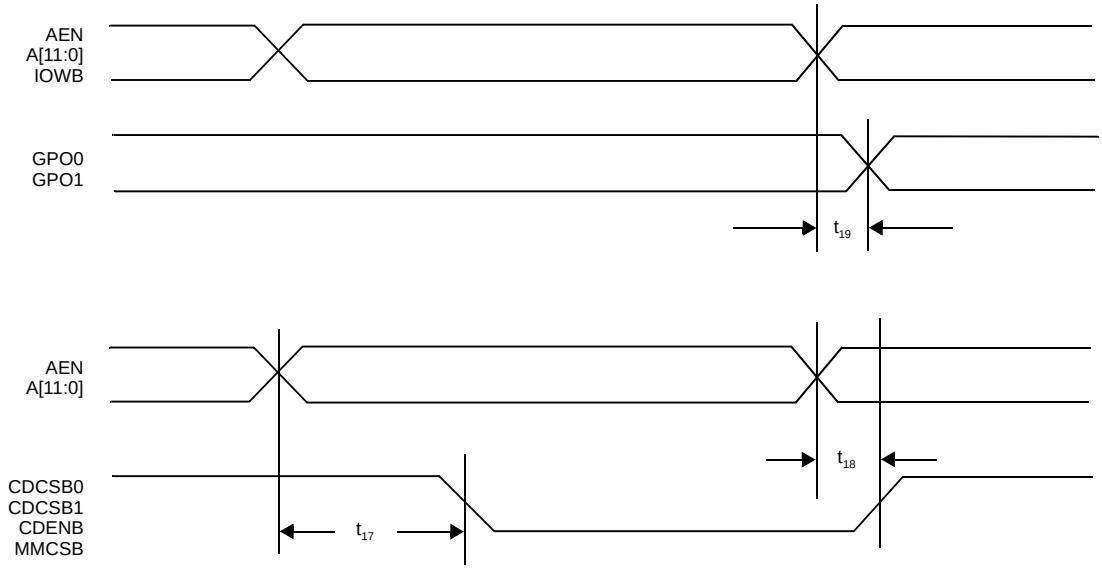


Figure 28 Miscellaneous Output Signals

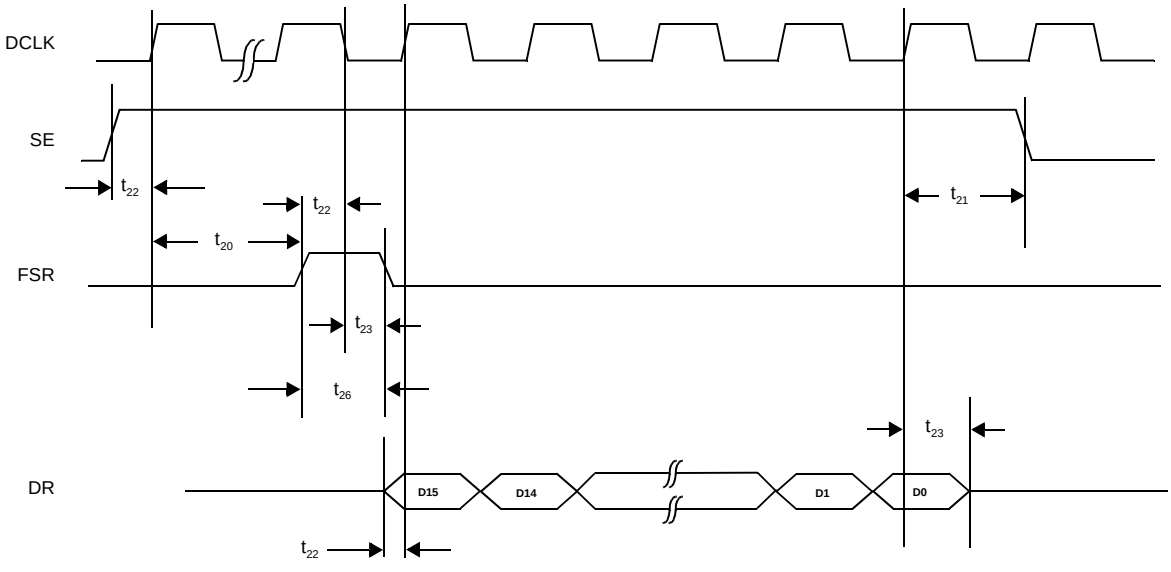


Figure 29 Serial Mode Receive Operation

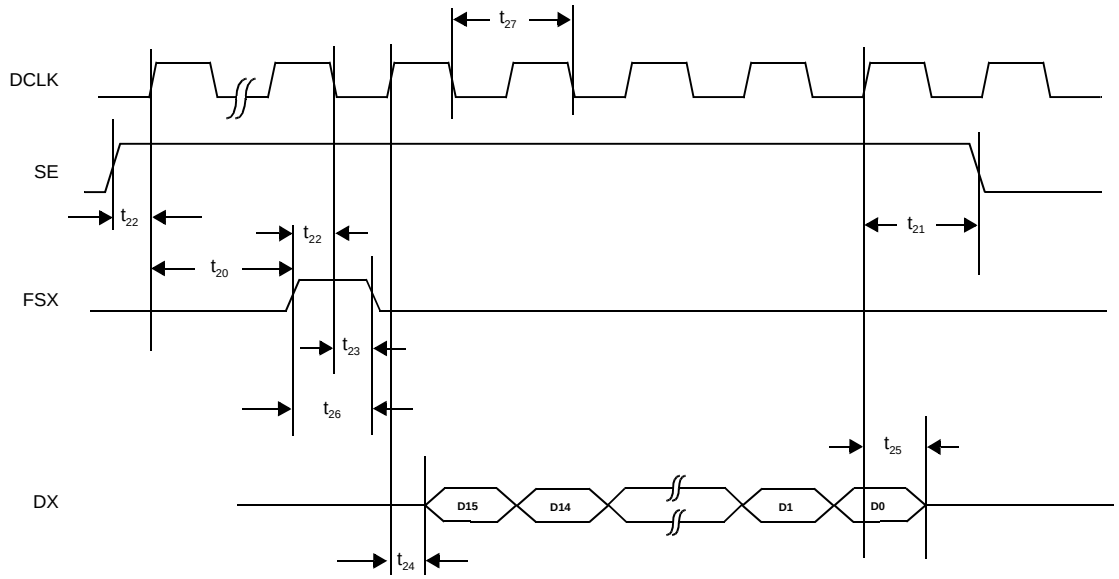


Figure 30 Serial Mode Transmit Operation

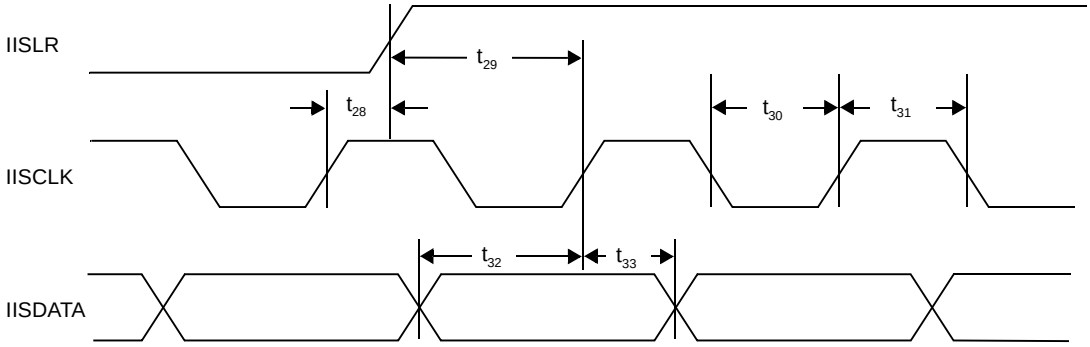
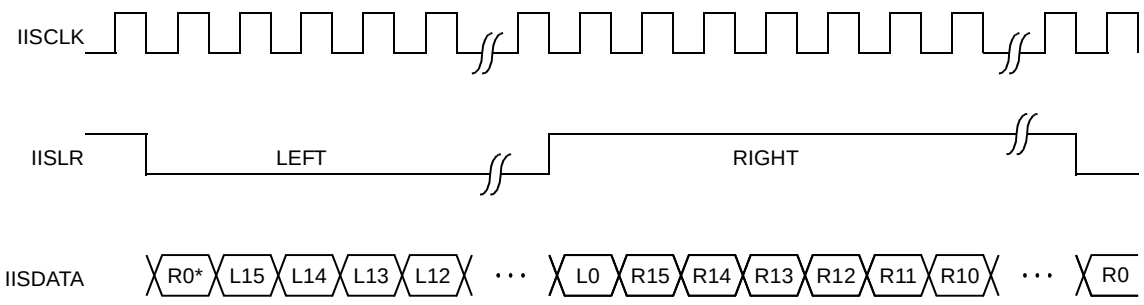


Figure 31 Serial Input Timing for I²S Interface



* Note: LSB of right channel, previous sample.

Figure 32 I²S Digital Input Format with 16 SCLK Periods

TIMING CHARACTERISTICS

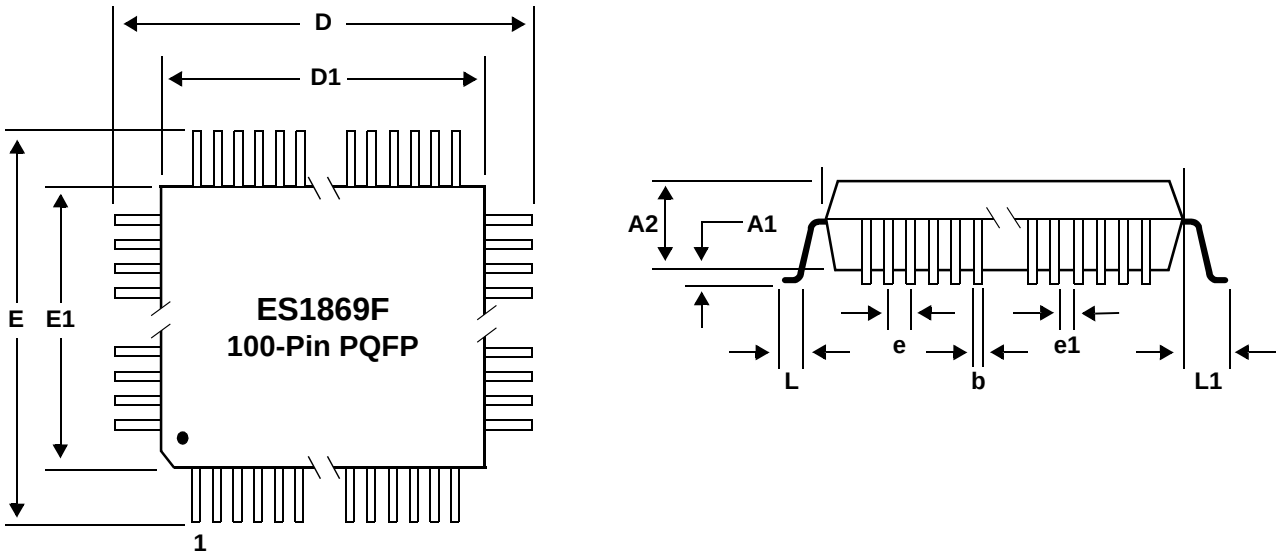
Table 29 Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_1	Reset pulse width	300			ns
t_2	IORB, IOWB pulse width	100			ns
t_3	Address setup time	10			ns
t_4	Read data access time			70	ns
t_5	Read data hold time			10	ns
t_6	Write data setup time	5			ns
t_7	Write data hold time	10			ns
t_8	DMA request to AEN high	0			ns
t_9	DMA request to DMA ACK	10			ns
t_{10}	DMA ACK to request release *			30	ns
t_{11}	DMA ACK high to AEN low	0			ns
t_{12}	DMA ACK to IOWB, IORB low	0			ns
t_{13}	IOWB, IORB to DMA ACK release	20			ns
t_{14}	Crystal frequency, XI/XO		14.318		MHz
t_{17}	AEN, A[11:0], CDCSB0, CDCSB1, MMCSB, CDENB low			20	ns
t_{18}	AEN, A[11:0], CDCSB0, CDCSB1, MMCSB, CDENB high			20	ns
t_{19}	AEN, A[11:0], IOWB, IORB to GPO0, GPO1 delays			20	ns
t_{20}	SE high to valid FSR, FSX edge	2			DCLK
t_{21}	SE release time to Last DX, DR data bit	1			DCLK
t_{22}	SE, FSX, FSR setup time to DCLK edge	15			ns
t_{23}	SE, FSX, FSR, DR hold time to DCLK edge	10			ns
t_{24}	DX delay time from DCLK edge			20	ns
t_{25}	DX hold time from DCLK edge	10			ns
t_{26}	FSR, FSX pulse width	60	500		ns
t_{27}	DCLK clock frequency		2.04		MHz
t_{28}	IISCLK delay	2			ns
t_{29}	IISCLK setup	32			ns
t_{30}	Bit clock low	22			ns
t_{31}	Bit clock high	22			ns
t_{32}	Data setup time	32			ns
t_{33}	Data hold time	2			ns

NOTE: * In Compatibility mode DMA, the DMA request is reset by the acknowledge signal going low. In Extended mode DMA, the DMA request is reset when the acknowledge signal is low AND the correct command signal is low – either IORB (for DMA read from I/O device) or IOWB (for DMA write to I/O device). For Extended mode DMA, the time t_{10} is relative to the later of the falling edge of the acknowledge signal or the command signal.

MECHANICAL DIMENSIONS

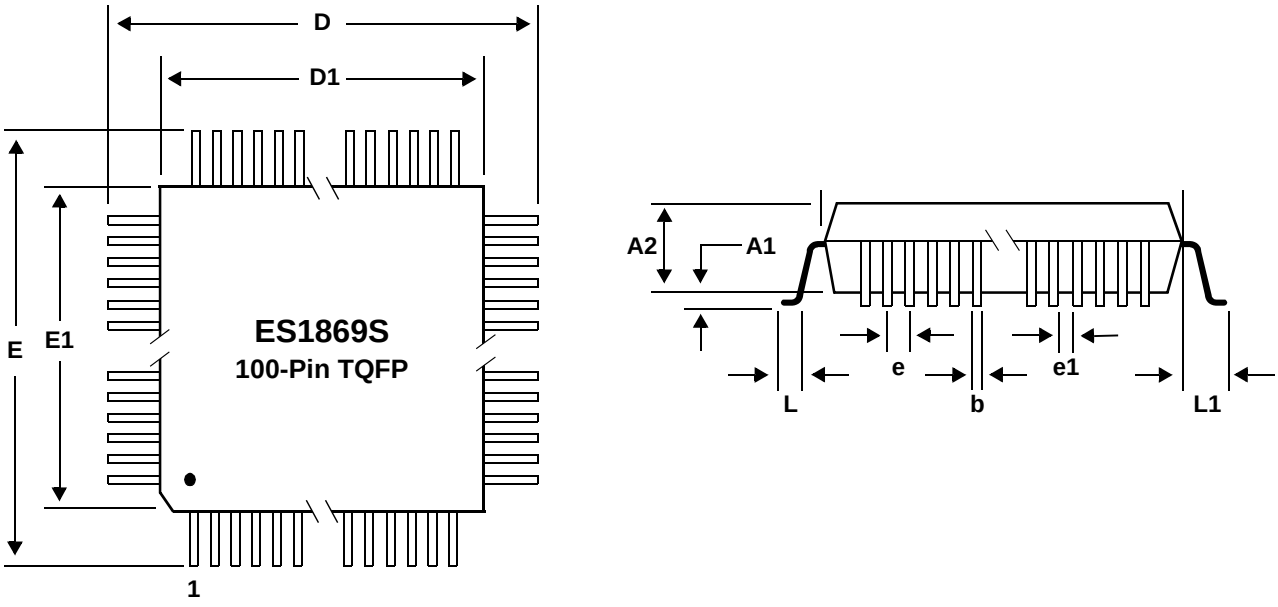
ES1869F PQFP Package



Symbol	Description	Millimeters		
		Min	Nom	Max
D	Lead to lead, X-axis	23.65	23.90	24.15
D1	Package's outside, X-axis	19.90	20.00	20.10
E	Lead to lead, Y-axis	17.65	17.90	18.15
E1	Package's outside, Y-axis	13.90	14.00	14.10
A1	Board standoff	0.10	0.25	0.36
A2	Package thickness	2.57	2.71	2.87
b	Lead width	0.20	0.30	0.40
e	Lead pitch	-	0.65	-
e1	Lead gap	0.24	-	-
L	Foot length	0.65	0.80	0.95
L1	Lead length	1.88	1.95	2.02
-	Foot angle	0°		7°
-	Coplanarity	-	-	0.102
-	Leads in X-axis	-	30	-
-	Leads in Y-axis	-	20	-
-	Total leads	-	100	-
-	Package type	-	PQFP	-

Figure 33 ES1869F PQFP Mechanical Dimensions

ES1869S TQFP Package



Symbol	Description	Millimeters		
		Min	Nom	Max
D	Lead to lead, X-axis	15.75	16.00	16.25
D1	Package's outside, X-axis	13.90	14.00	14.10
E	Lead to lead, Y-axis	15.75	16.00	16.25
E1	Package's outside, Y-axis	13.90	14.00	14.10
A1	Board standoff	0.05	0.10	0.15
A2	Package thickness	1.35	1.40	1.45
b	Lead width	0.17	0.22	0.27
e	Lead pitch	-	0.50	-
e1	Lead gap	0.24	-	-
L	Foot length	0.45	0.60	0.75
L1	Lead length	0.93	1.00	1.07
-	Foot angle	0°		7°
-	Coplanarity	-	-	0.102
-	Leads in X-axis	-	25	-
-	Leads in Y-axis	-	25	-
-	Total leads	-	100	-
-	Package type	-	TQFP	-

Figure 34 ES1869S TQFP Mechanical Dimensions

APPENDIX A: ES1869 PNP ROM DATA EXAMPLE

16-bit address decode used with external device decoding. A[15:12] and AEN should be all zero.

LDN #0 Control Interface

LDN #1 Audio (FM) MPU-401

LDN #2 Joystick

LDN #3 IDE CD-ROM

LDN #4 Modem (not used here)

NOTE: Contact your ESS sales representative or FAE for the most current EPROM data code for your hardware design.

```
; ******************************************************
;
; Start of ESS Proprietary Header (8 bytes)
;
; ******************************************************
0A5H                                    ; PNP OK byte
059H                                    ; IRQA = 9  IRQB = 5
0A7H                                    ; IRQC = 7  IRQD = 10
0CBH                                    ; IRQE = 11 IRQF = 12
010H                                    ; DRQA = 0  DRQB = 1
053H                                    ; DRQC = 3  DRQD = 5
002H                                    ; MPU-401 part of audio, CD, DRQ latching off
00CH                                    ; GPO1/GPI are not used by Modem DMA channel or g.p.


; ******************************************************
;
; Start of PNP Resource Header
;
; ******************************************************
016H, 073H, 018H, 069H                  ; "ESS1869A" product id for ES1869
0FFH, 0FFH, 0FFH, 0FFH                  ; serial number FFFFFFFF (not supported)
000H                                    ; header checksum
00AH, 010H, 010H                        ; PNP 1.0, ESS version 1.0
082H, 023H, 000H                        ; “ESS ES1869 Plug and Play AudioDrive”


; ******************************************************
;
; LOGICAL DEVICE 0  --  Configuration Ports
;  8 bytes at any I/O address that is a multiple of 8
;
; ******************************************************
015H, 016H, 073H, 000H, 000H, 000H              ; ESS0000
047H, 001H, 000H, 008H, 0F8H, 00FH, 008H, 008H  ; 800H-FF8H 8 bytes
```

```
; ******************************************************
;
; LOGICAL DEVICE 1 -- Audio Controller w/FM and MPU-401
;
; ******************************************************
015H, 016H, 073H, 018H, 069H, 000H; ESS1869A


;  Basic configuration 0000

031H, 000H
02AH, 002H, 008H                                ; DMA 0:   DRQ 1
02AH, 009H, 008H                                ; DMA 1:   DRQ 0 or 3
022H, 020H, 000H                                ; INT 0:   IRQ 5
047H, 001H, 020H, 002H, 020h, 002h, 000H, 010H  ; 220 16 bytes
047H, 001H, 088H, 003H, 088H, 003H, 000H, 004H  ; 388 4 bytes
047H, 001H, 030H, 003H, 030H, 003H, 000H, 002H  ; 330 2 bytes


;  Basic configuration 0001

031H, 001H
02AH, 002H, 008H                                ; DMA 0: DRQ 1
02AH, 009H, 008H                                ; DMA 1: DRQ 0 or 3
022H, 0A0H, 006H                                ; INT 0: IRQ 5, 7, 9, or 10
047H, 001H, 020H, 002H, 040H, 002H, 020H, 010H  ; 220 or 240 16 bytes
047H, 001H, 088H, 003H, 088H, 003H, 000H, 004H  ; 388 4 bytes
047H, 001H, 000H, 003H, 030H, 003H, 030H, 002H  ; 300 or 330 2 bytes


;  Basic configuration 0002

031H, 001H
02AH, 00BH, 008H                                ; DMA 0: DRQ 0, 1 or 3
02AH, 00BH, 008H                                ; DMA 1: DRQ 0, 1 or 3
022H, 0A0H, 01EH                                ; INT 0: IRQ 5, 7, 9, 10, 11, or 12
047H, 001H, 020H, 002H, 080H, 002H, 020H, 010H  ; 220, 240, 260, 280 16 bytes
047H, 001H, 088H, 003H, 088H, 003H, 000H, 004H  ; 388 4 bytes
047H, 001H, 000H, 003H, 030H, 003H, 030H, 002H  ; 330 or 330 2 bytes


;  Basic configuration 0003

031H, 001H
002H, 00BH, 008H                                ; DMA 0: DRQ 0, 1 or 3
02AH, 00BH, 008H                                ; DMA 1: DRQ 0, 1 or 3
022H, 0A0H, 01EH                                ; INT 0: IRQ 5, 7, 9, 10, 11, or 12
047H, 001H, 020H, 002H, 080H, 002H, 020H, 010H  ; 220, 240, 260, 280 16 bytes
047H, 001H, 088H, 003H, 088H, 003H, 000H, 004H  ; 388 4 bytes
047H, 001H, 000H, 008H, 0FEH, 00FH, 002H, 002H  ; 800/801-FFE/FFF 2 bytes


;  Basic configuration 0004

031H, 002H
02AH, 00BH, 008H                                ; DMA 0: DRQ 0, 1 or 3
02AH, 00BH, 008H                                ; DMA 1: DRQ 0, 1 or 3
022H, 0A0H, 01EH                                ; INT 0: IRQ 5, 7, 9, 10, 11, or 12
047H, 001H, 020H, 002H, 080H, 002H, 020H, 010H  ; 220, 240, 260, 280 16 bytes
047H, 001H, 000H, 008H, 0FCH, 00FH, 004H, 004H  ; 800/804-FFC/FFF 4 bytes
047H, 001H, 000H, 008H, 0FEH, 00FH, 002H, 002H  ; 800/801-FFE/FFF 2 bytes

038H                                            ; end configurations
```

```
; ******************************************************
;
; LOGICAL DEVICE 2 -- Joystick
; Only choice is one address at 201.
;
; ******************************************************
015H, 016H, 073H, 000H, 001H, 000H; ESS0001


;  Basic configuration 0000

031H, 000H
047H, 001H, 001H, 002H, 001H, 002H, 000H, 001H; 201 1 byte

;  Windows95 joystick driver will only allow 200-20F!!!


;  Basic configuration 0001

031H, 001H
047H, 001H, 000H, 002H, 00FH, 002H, 001H, 001H  ; 200/200-20F/20F 1 byte
038H                                            ; end dependent functions
01CH, 041H, 0D0H, 0B0H, 02FH                    ; Compatible ID: PNPB02F


; ******************************************************
;
; LOGICAL DEVICE 3 -- IDE CD-ROM
; needs an IRQ (10, 11, or 12) and two separate address ranges
;
; ******************************************************
015H, 016H, 073H, 000H, 002H, 000H; ESS0002


;  Basic configuration 0000

031H, 000H
022H, 000H, 00EH                                ; IRQ 9 10 11
047H, 001H, 068H, 001H, 068H, 001H, 000H, 008H  ; 168 8 bytes
047H, 001H, 06EH, 003H, 06EH, 003H, 000H, 002H  ; 36E 2 bytes


;  Basic configuration 0001

031H, 001H
022H, 000H, 00EH                                ; IRQ 9 10 11
047H, 001H, 0E8H, 001H, 0E8H, 001H, 000H, 008H  ; 1E8 8 bytes
047H, 001H, 0EEH, 003H, 0EEH, 003H, 000H, 002H  ; 3EE 2 bytes


;  Basic configuration 0002

031H, 001H
022H, 000H, 010H                                ; IRQ 12
047H, 001H, 068H, 001H, 068H, 001H, 000H, 008H  ; 168 8 bytes
047H, 001H, 06EH, 003H, 06EH, 003H, 000H, 002H  ; 36E 2 bytes


;  Basic configuration 0003

031H, 001H
022H, 000H, 010H                                ; IRQ 12
047H, 001H, 0E8H, 001H, 0E8H, 001H, 000H, 008H  ; 1E8 8 bytes
047H, 001H, 0EEH, 003H, 0EEH, 003H, 000H, 002H  ; 3EE 2 bytes
```

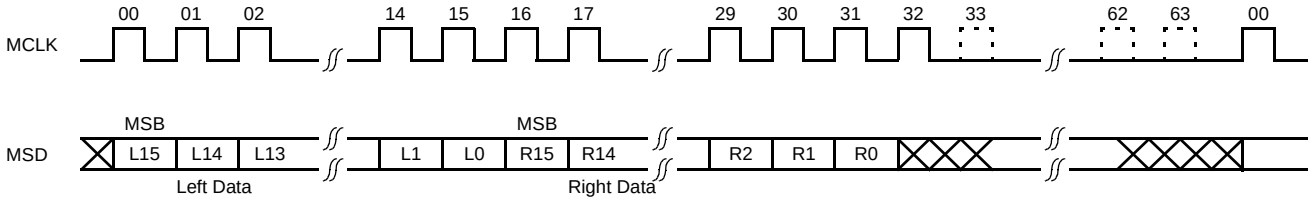
```
;  Basic configuration 0004

031H, 002H
022H, 000H, 01CH                                ; IRQ 9 10 11 12
047H, 001H, 000H, 001H, 0F8H, 001H, 008H, 008H  ; 100/1F8-107/1FF 8 bytes
047H, 001H, 000H, 003H, 0FEH, 003H, 002H, 002H  ; 300/301-3FE/3FF 2 bytes


038H                                            ; end dependent functions
01CH, 041H, 0D0H, 006H, 000H                    ; Compatible ID: PNP0600


079H, 000H                                      ; end tag + checksum
```

APPENDIX B: ES689/ES69x DIGITAL SERIAL INTERFACE

In order for the ES689/ES69x to acquire the FM DAC, bit 4 of mixer register 48h inside the ES1869 must be set high. When bit 4 is set high, activity on the MCLK signal causes the ES1869 to connect the FM DAC to the ES689/ ES69x. If MCLK stays low for more than a few sample periods, the ES1869 reconnects the FM DAC to the FM synthesizer.

After reset, the ES689/ES69x transmits samples continuously. In this mode, bit 4 of mixer register 48h must be set/cleared to assign the current owner of the FM DAC.

The ES689/ES69x can be programmed to enter Activity-Detect mode using system exclusive command 4. For more information on system exclusive commands, see the appropriate ES689/ES69x Data Sheet. In this mode, the ES689/ES69x blocks the serial port output (i.e., sets MSD and MCLK low) if no MIDI input is detected on the MSI pin for a period of 5 seconds. It resumes output of data on the serial port as soon as a MIDI input is detected on the MSI pin. This is the recommended mode of operation.



Bit Clock Rate (MCLK):	2.75 MHz
Sample Rate:	42,968.75 Hz
MCLK Clocks per Sample:	33 clocks (+ 31 missing clocks)
MSD Format:	16 bits, unsigned (offset 8000h), MSB first

MSD changes after rising edge of MCLK. Hold time relative to MCLK rising edge is 0-25 nanoseconds.

APPENDIX C: I²S ZV INTERFACE REFERENCE

(Excerpted from “PCMCIA Document Number 0135 – Release 010 1/15/96”)

Overview

The following diagram shows the system level concept of the ZV Port. The diagram demonstrates how TV in a window can be achieved in a portable computer with a low cost PC Card. An MPEG or teleconferencing card can also be plugged into the PC Card slot.

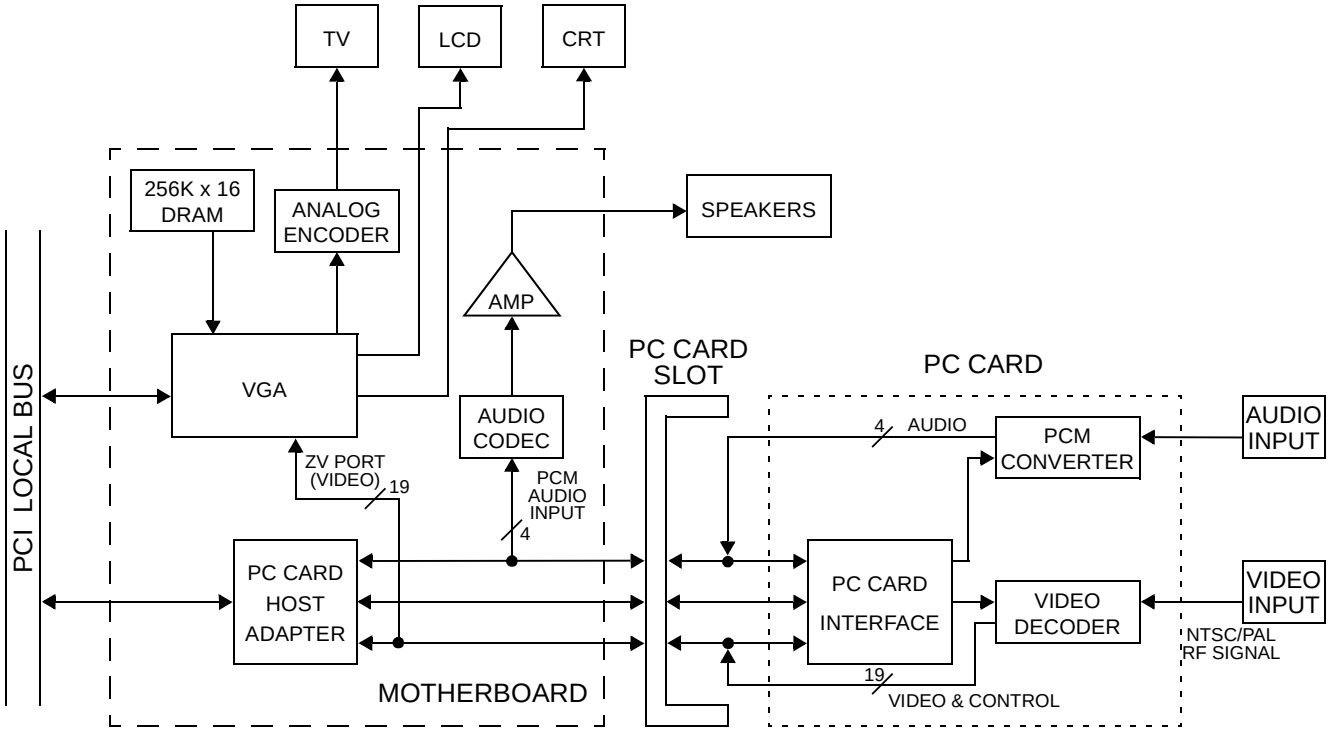


Figure 35 Example ZV Port Implementation

The Audio Interface

The ZV Port compliant PC Card sends audio data to the host computer using Pulse Code Modulation (PCM). Audio data is transferred using serial I²S format. The audio circuitry in the host system is primarily a PCM DAC.

The PCM audio DAC is a complete stereo digital-to-analog system including digital-interpolation, delta-sigma digital-to-analog conversion, digital de-emphasis and analog filtering. Only the normal power supply decoupling components and one resistor and capacitor per channel for analog signal reconstruction are required.

The DAC accepts data at standard audio frequencies including 48 kHz, 44.1 kHz, 32 kHz, and 22 kHz. Audio data is input via the serial data input pin, SDATA. The Left/ Right Clock (LRCLK) defines the channel and delineation of data. The Serial Clock (SCLK) clocks the audio data into the input data buffer. The Master Clock (MCLK) is used to operate the digital interpolation filter and the delta-sigma modulator.

NOTE: MCLK is not required in some I²S designs.

Table 30 Common Clock Frequencies

LRCLK (KHz)	MCLK(MHz)	
	256x	384x
22	5.632	8.448
32	8.192	12.2880
44.1	11.2896	16.9344
48	12.2880	18.4320

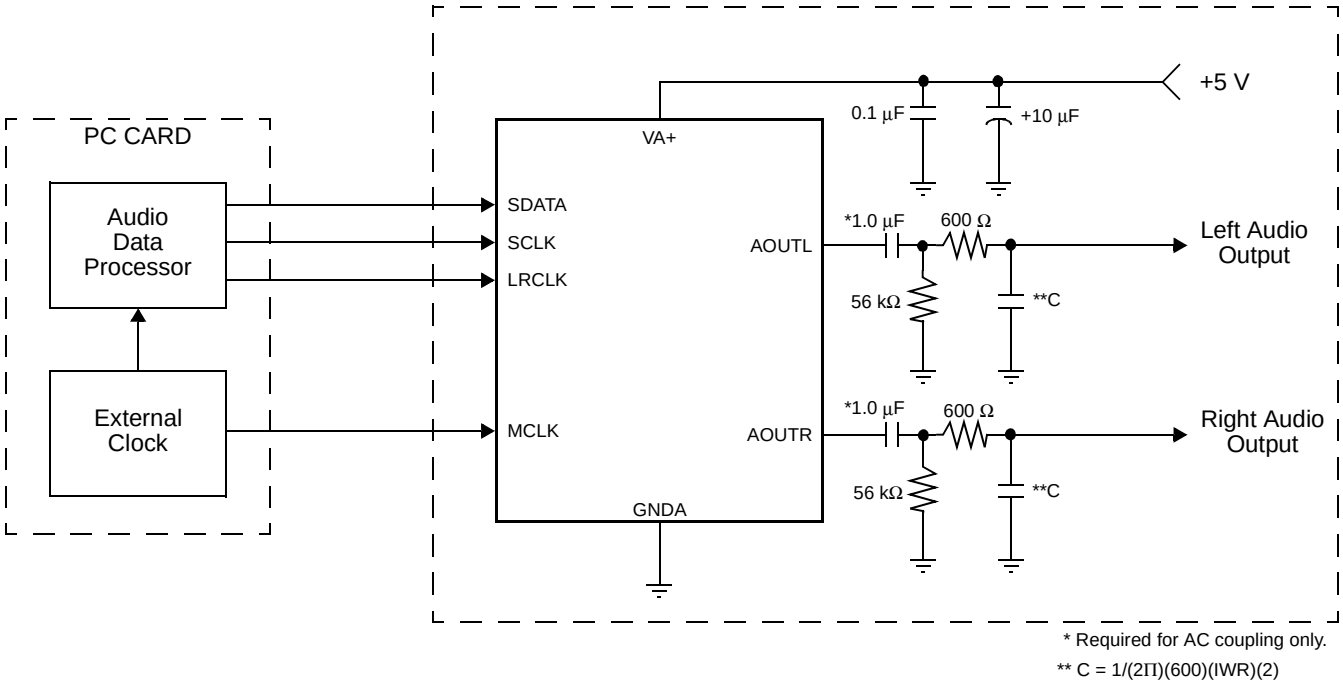


Figure 36 Typical ZV Port Audio Implementation

Audio Interface Timing

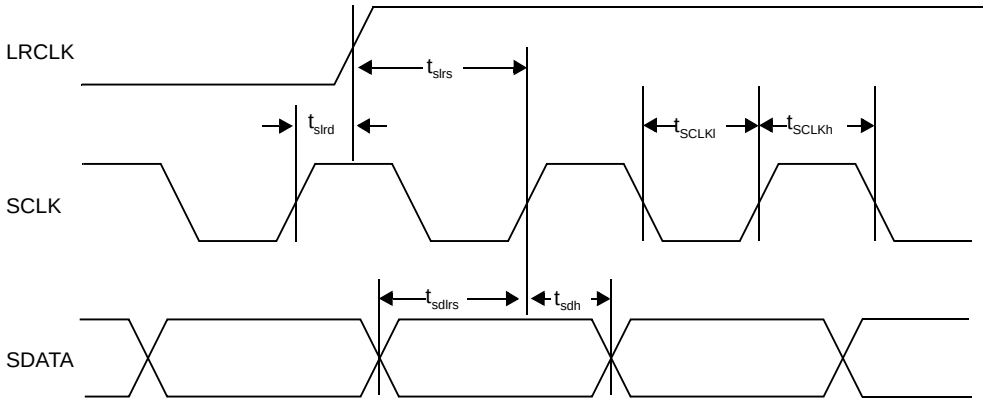


Figure 37 Audio Interface Timing

Table 31 AC Parameters for Audio Signals

Symbol	Parameter	Min
t_{slrd}	LRCLK delay	2 ns
t_{slrs}	LRCLK setup	32 ns
t_{SCLKl}	bit clock low	22 ns
t_{SCLKh}	bit clock high	22 ns
t_{sdlrs}	data setup	32 ns
t_{sdh}	data hold	2 ns

LRCLK

This signal determines which audio channel (left/right) is currently being input on the audio Serial Data input line. LRCLK is low to indicate the left channel and high to indicate the right channel. Typical frequency values for this signal are 48 kHz, 44.1 kHz, 32 kHz, and 22 kHz.

SCLK

This signal is the serial digital audio PCM clock.

SDATA

This signal is the digital PCM signal that carries audio information. Digital audio data is transferred using I²S format.

MCLK

This signal is the Master clock for the digital audio. MCLK is asynchronous to LRCLK, SDATA, and SCLK.

The MCLK must be either 256x or 384x the desired Input Word Rate (IWR). IWR is the frequency at which words for each channel are input to the DAC and is equal to the LRCLK frequency. The following table illustrates several standard audio word rates and the required MCLK and LRCLK frequencies. Typically, most devices operate with 384 Fs master clock.

The ZV Port audio DAC should support a MCLK frequency of 384 Fs. This results in the frequencies shown below.

LRCLK (kHz) Sample Frequency	SCLK (MHz) 32 x Fs	MCLK (MHz) 384x Fs
22	0.704	8.448
32	1.0240	12.2880
44.1	1.4112	16.9344
48	1.5360	18.4320

I²S Format

The I²S format is shown in Figure 38 below. The digital audio data is left-channel MSB-justified to the high-to-low going edge of the LRCLK plus one SCLK delay.

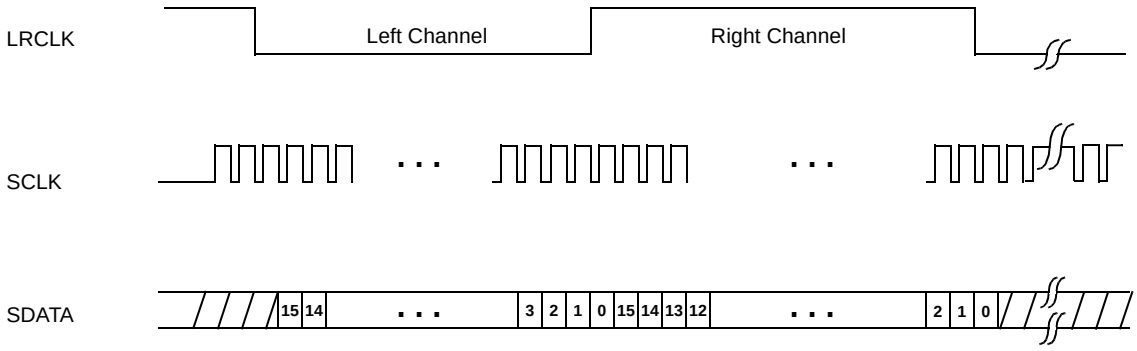


Figure 38 I²S Digital Input Format with 16 SCLK periods

ZV Port Pin Assignments

Table 32 shows the function of various PC Card signals when the ZV Port custom interface mode is set in the PC Card Host Adapter. PC Card signals not mentioned in the table below remain unchanged from the 16-bit PC Card I/O and Memory interface.

Table 32 ZV Port Interface Pin Assignments

PC Card Pin Number	I/O and Memory Interface Signal Name	I/O and Memory I/O[a]	ZV Port Interface Signal Name	ZV Port I/O[a]	Comments
8	A10	I	HREF	O	Horizontal Sync to ZV Port
10	A11	I	VSYNC	O	Vertical Sync to ZV Port
11	A9	I	Y0	O	Video Data to ZV Port YUV:4:2:2 format
12	A8	I	Y2	O	Video Data to ZV Port YUV:4:2:2 format
13	A13	I	Y4	O	Video Data to ZV Port YUV:4:2:2 format
14	A14	I	Y6	O	Video Data to ZV Port YUV:4:2:2 format
19	A16	I	UV2	O	Video Data to ZV Port YUV:4:2:2 format
20	A15	I	UV4	O	Video Data to ZV Port YUV:4:2:2 format
21	A12	I	UV6	O	Video Data to ZV Port YUV:4:2:2 format
22	A7	I	SCLK	O	Audio SCLK PCM Signal
23	A6	I	MCLK	O	Audio MCLK PCM Signal
24:25	A[5:4]	I	RESERVED	RFU	Put in three state by Host Adapter No connection in PC Card
26:29	A[3:0]	I	ADDRESS[3:0]	I	Used for accessing PC Card
33	IOIS16#	O	PCLK	O	Pixel Clock to ZV Port
46	A17	I	Y1	O	Video Data to ZV Port YUV:4:2:2 format
47	A18	I	Y3	O	Video Data to ZV Port YUV:4:2:2 format
48	A19	I	Y5	O	Video Data to ZV Port YUV:4:2:2 format
49	A20	I	Y7	O	Video Data to ZV Port YUV:4:2:2 format
50	A21	I	UV0	O	Video Data to ZV Port YUV:4:2:2 format
53	A22	I	UV1	O	Video Data to ZV Port YUV:4:2:2 format
54	A23	I	UV3	O	Video Data to ZV Port YUV:4:2:2 format
55	A24	I	UV5	O	Video Data to ZV Port YUV:4:2:2 format
56	A25	I	UV7	O	Video Data to ZV Port YUV:4:2:2 format
60	INPACK#	O	LRCLK	O	Audio LRCLK PCM Signal
62	SPKR#	O	SDATA	O	Audio PCM Data Signal

a. “I” indicates signal is input to PC Card, “O” indicates signal is output from PC Card

APPENDIX D: MOTHERBOARD SCHEMATICS

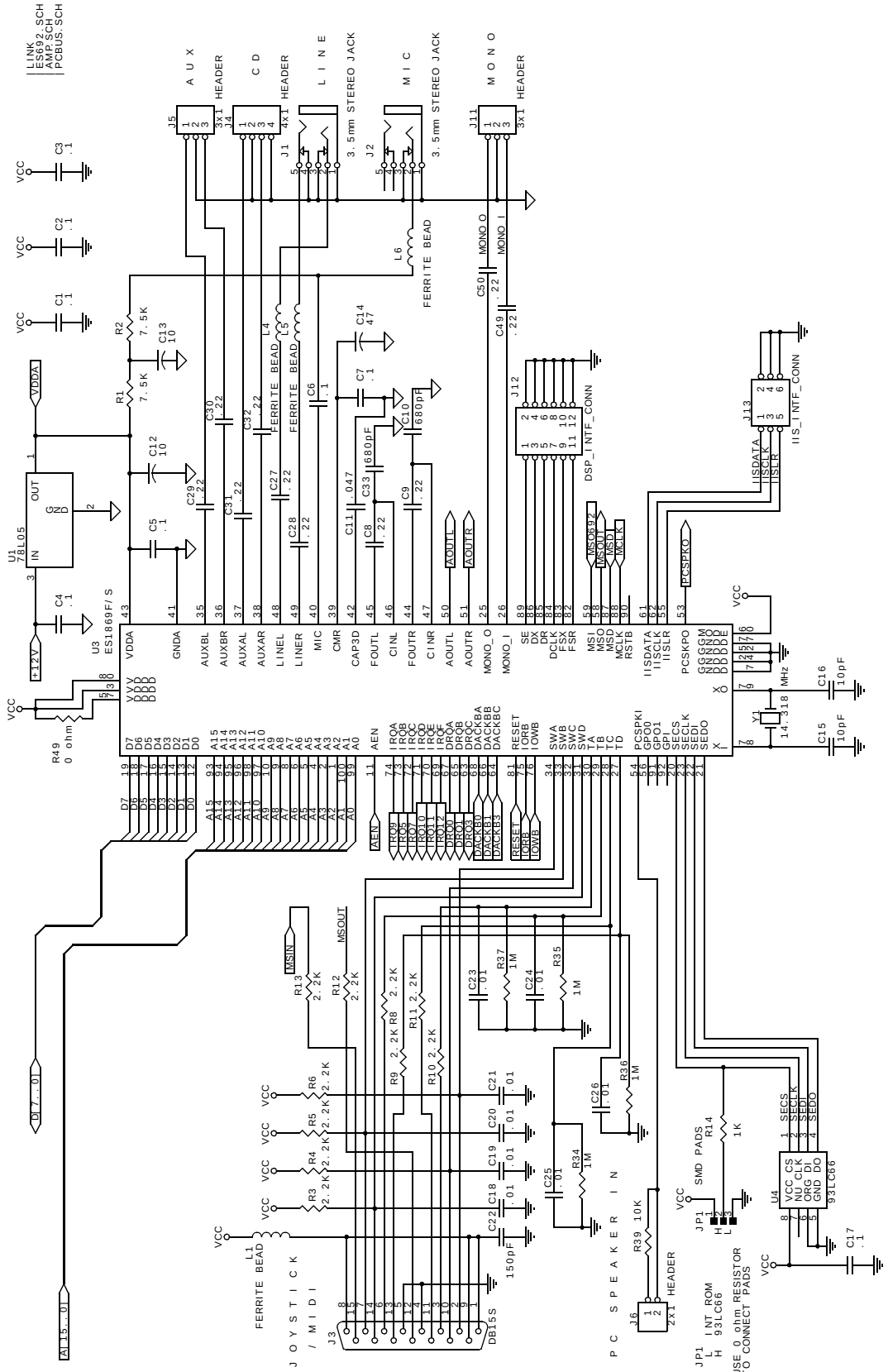


Figure 39 ES1869 – Motherboard Configuration

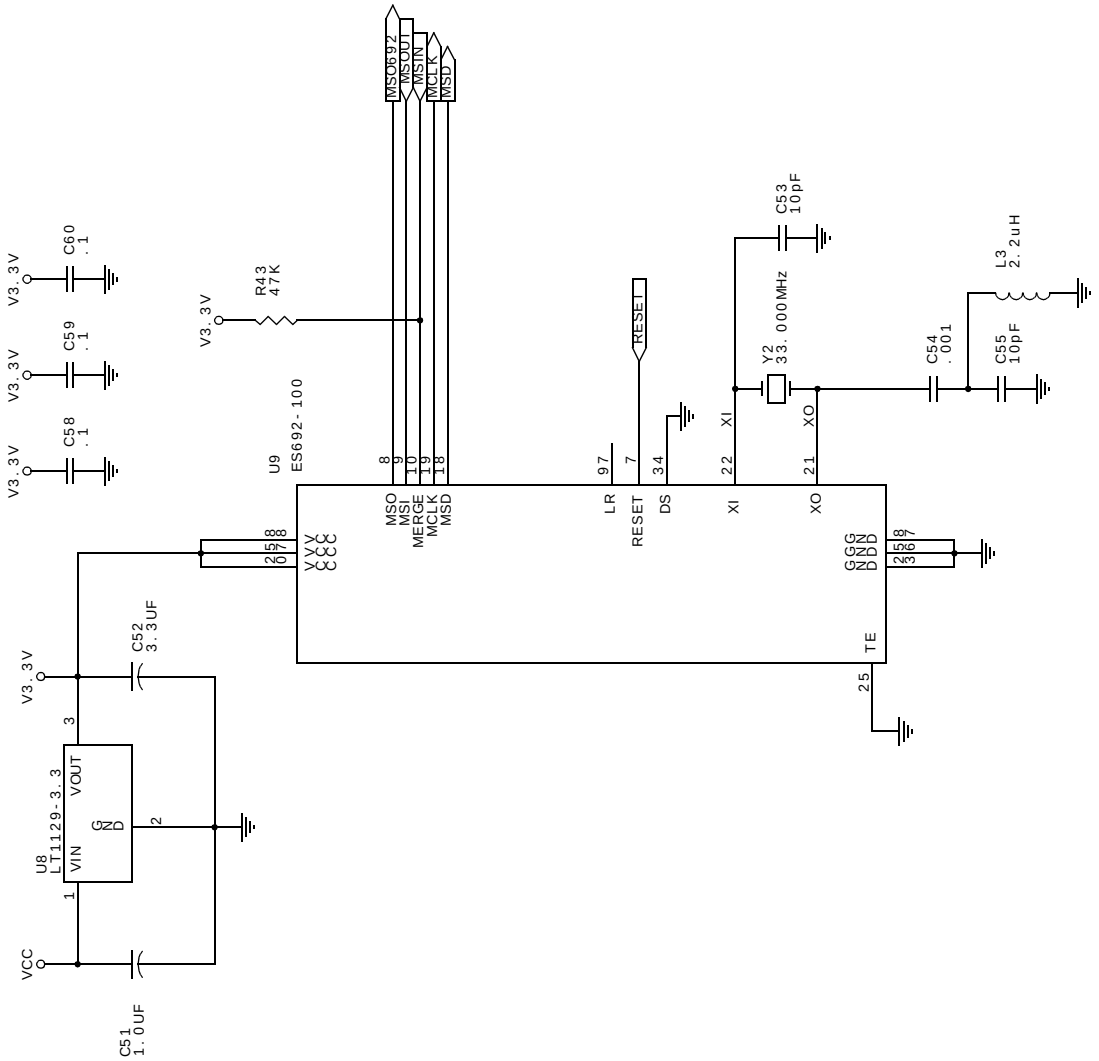


Figure 40 ES1869 and ES692 – Motherboard Configuration

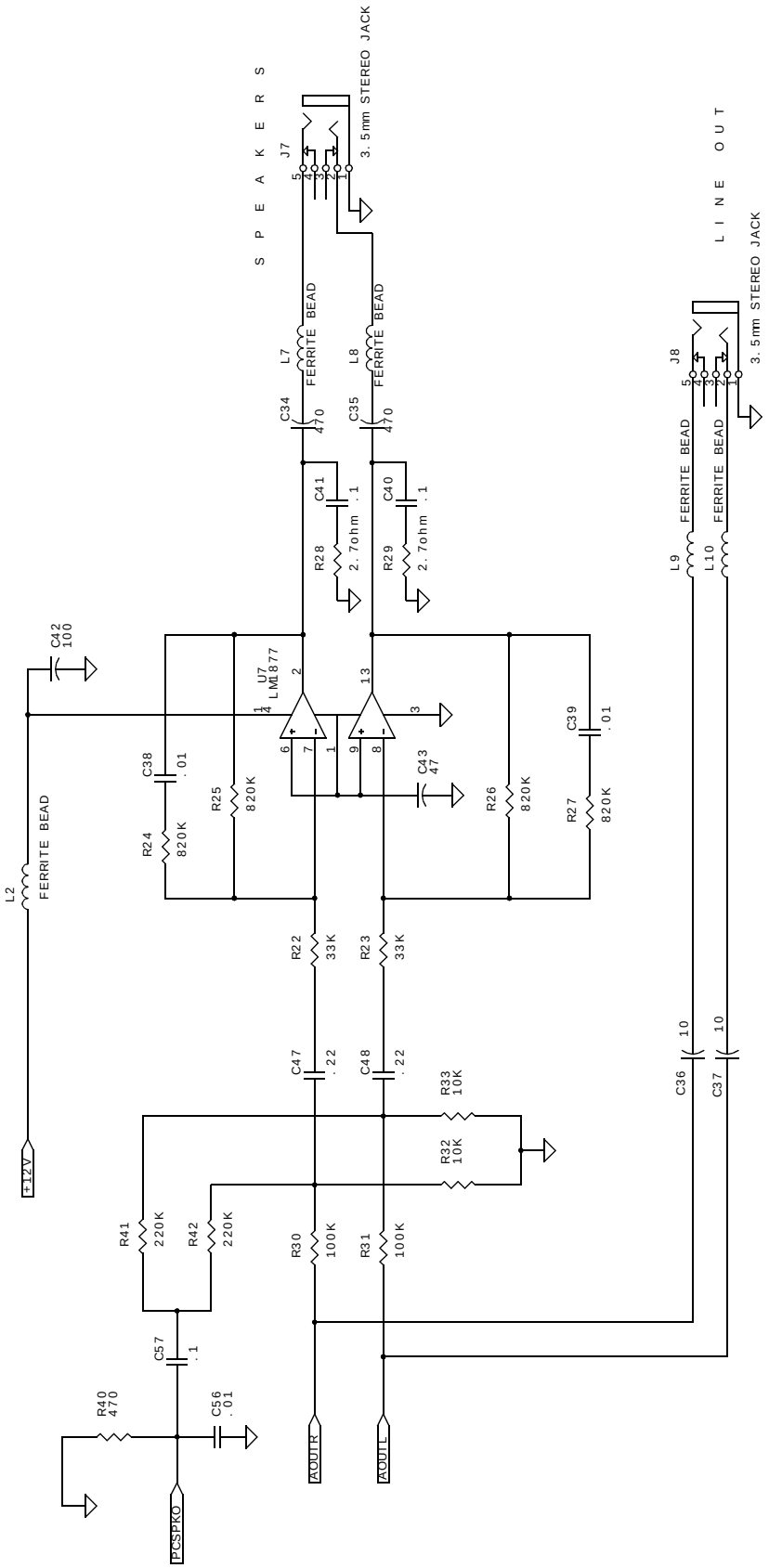


Figure 41 Amplifier – Motherboard Configuration

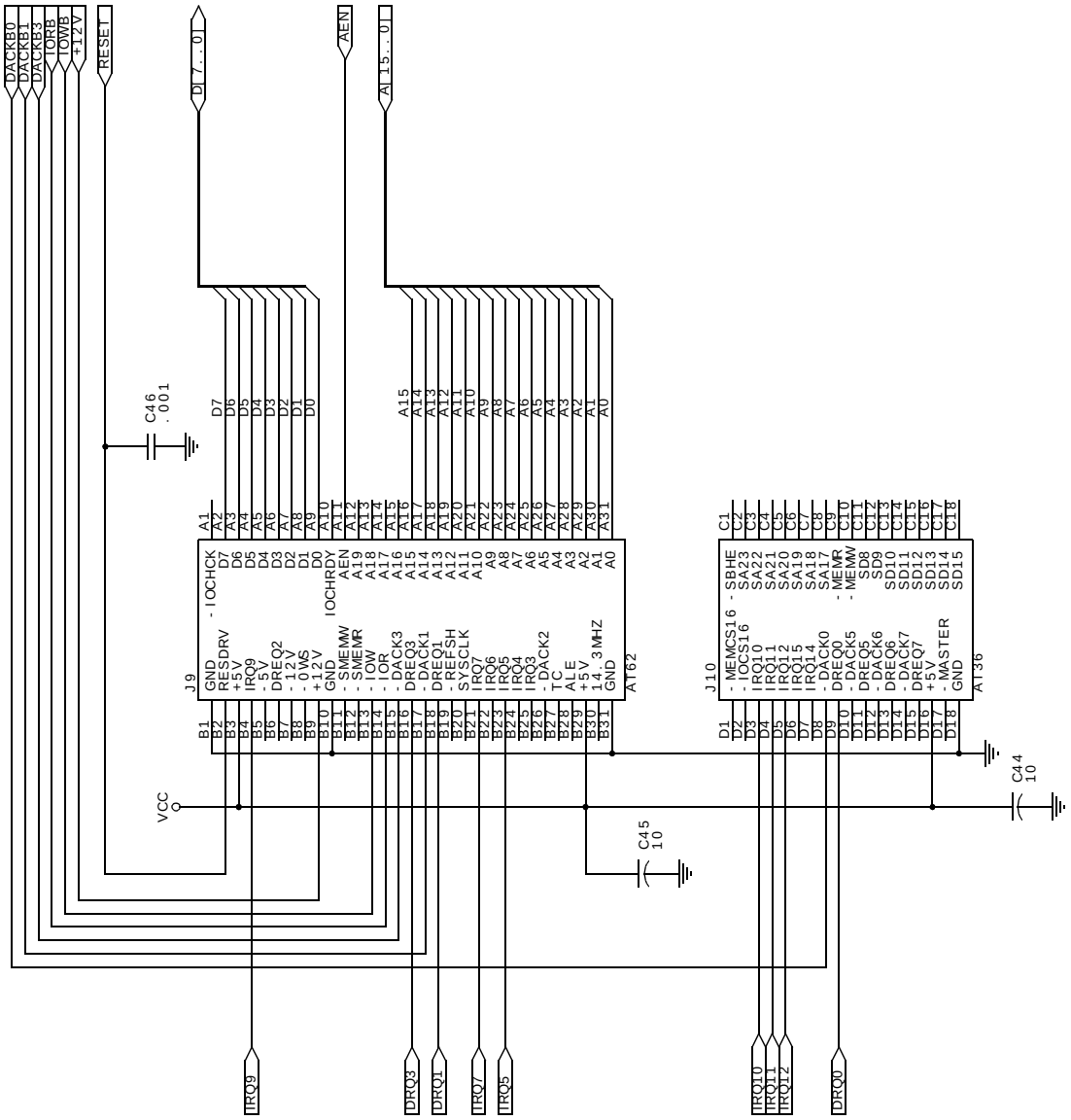


Figure 42 PC Interface – Motherboard Configuration

APPENDIX E: MOTHERBOARD BILL OF MATERIALS

Table 33 ES1869 Motherboard Bill of Materials (BOM)

Item	Quantity	Reference	Part
1	11	C1,C2,C3,C4,C5,C6,C7,C17,C40,C41,C57	.1 µF
2	12	C8,C9,C27,C28,C29,C30,C31,C32,C47,C48,C49,C50	.22 µF
3	1	C46	.001 µF
4	2	C10,C33	680 pF
5	1	C11	.047 µF
6	6	C2,C13,C36,C37,C44,C45	10 µF
7	2	C14,C43	47 µF
8	2	C15,C16	10 pF
9	11	C18,C19,C20,C21,C23,C24,C25,C26,C38,C39,C56	.01 µF
10	1	C22	150 pF
11	2	C34,C35	470 µF
12	1	C42	100 µF
13	2	JP1 (1-2), JP2 (2-3)	0 ohm
14	4	J1,J2,J7,J8	3.5 mm Stereo Jack
15	1	J3	DB15S
16	1	J4	4x1 Header
17	1	J5	13x2 Header optional wavetable connector
18	1	J6	2x1 Header
19	1	J11	3x1 Header
20	1	J12	6x2 Header
21	1	J13	3x2 Header
22	9	L1,L2,L4,L5,L6,L7,L8,L9,L10	Ferrite Bead
23	2	R1,R2	7.5K
24	10	R3,R4,R5,R6,R8,R9,R10,R11,R12,R13	2.2K
25	4	R14,R15,R16,R17	1K
26	1	R40	470 ohm
27	1	R18	22K
28	2	R22,R23	33K
29	4	R24,R25,R26,R27	820K
30	2	R28,R29	2.7 ohm
31	2	R30,R31	100K
32	3	R32,R33,R39	10K
33	4	R34,R35,R36,R37	1M
34	1	R49	0 ohm
35	2	R41,R42	220K
36	3	S1,S2,S3	Pushbutton
37	1	U1	78L05
38	1	U3	ES1869F/ES1869S
39	1	U4	93LC66
40	1	U7	LM1877

Table 33 ES1869 Motherboard Bill of Materials (BOM) (Continued)

Item	Quantity	Reference	Part
41	1	Y1	14.318 MHz
WITH OPTIONAL ES692 WAVETABLE MUSIC SYNTHESIZER:			
42	1	U9	ES692-TQFP100
43	1	U8	LT1129-3.3
44	1	Y2	33.000 MHz
45	1	C51	1.0 µF
46	1	C52	3.3 µF
47	2	C53,C55	10 pF
48	1	C54	.001 µF
49	3	C58,C59,C60	.1 µF
50	1	R43	47K
51	1	L3	2.2 µH

APPENDIX F: SOUND CARD SCHEMATICS

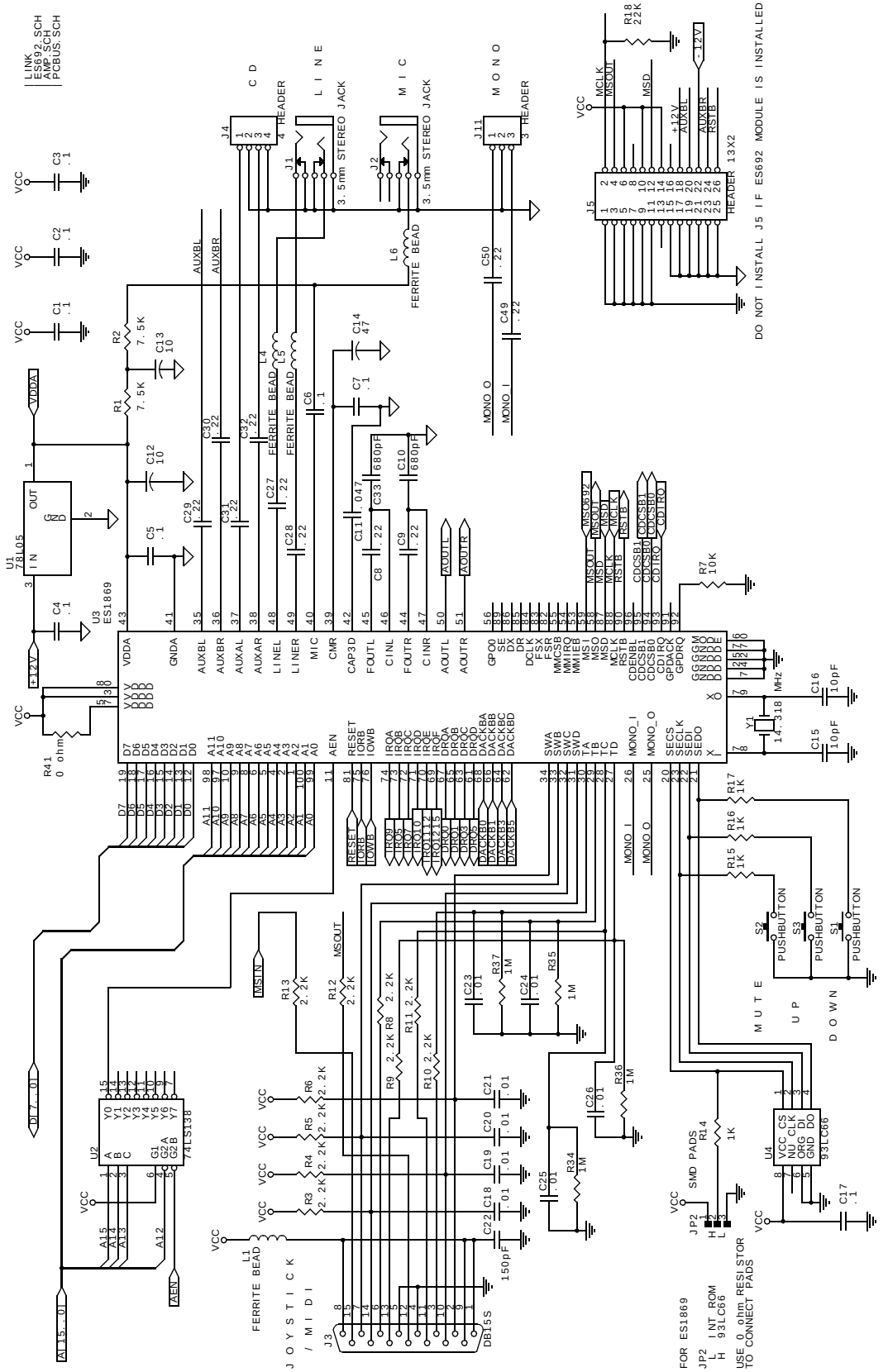


Figure 43 ES1869 – Sound Card Configuration

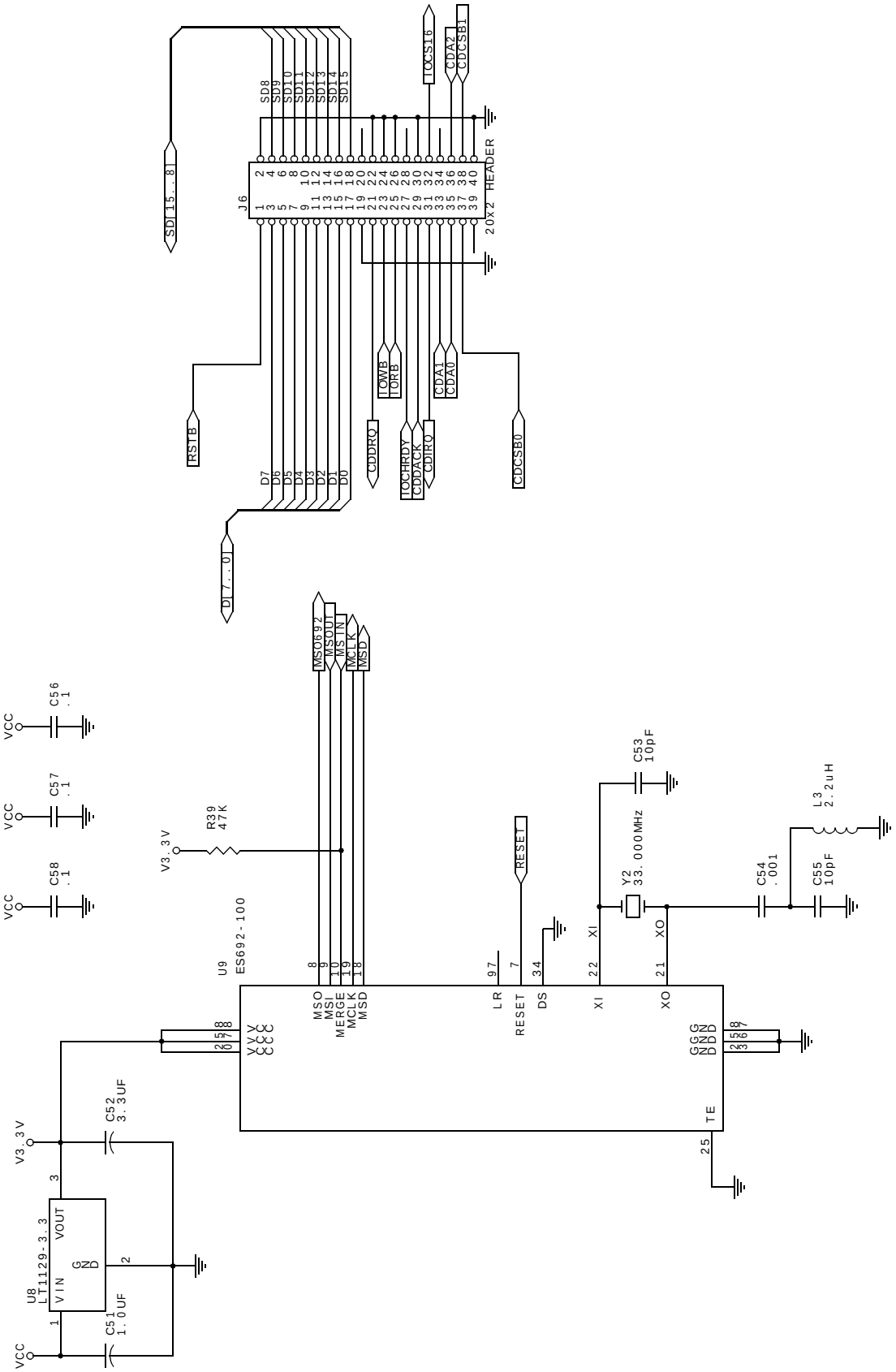


Figure 44 ES1869 and ES692 – Sound Card Configuration

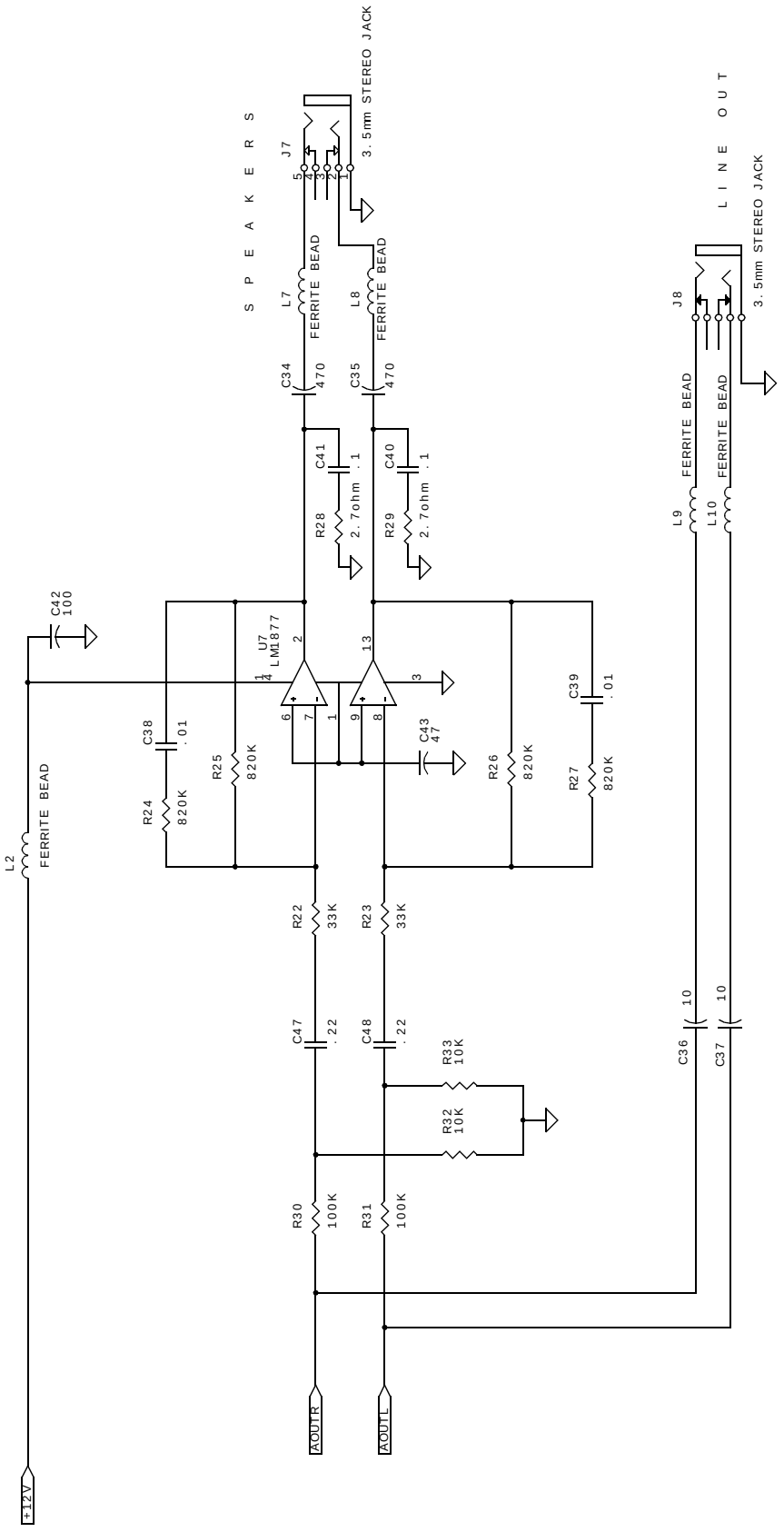


Figure 45 Amplifier – Sound Card Configuration

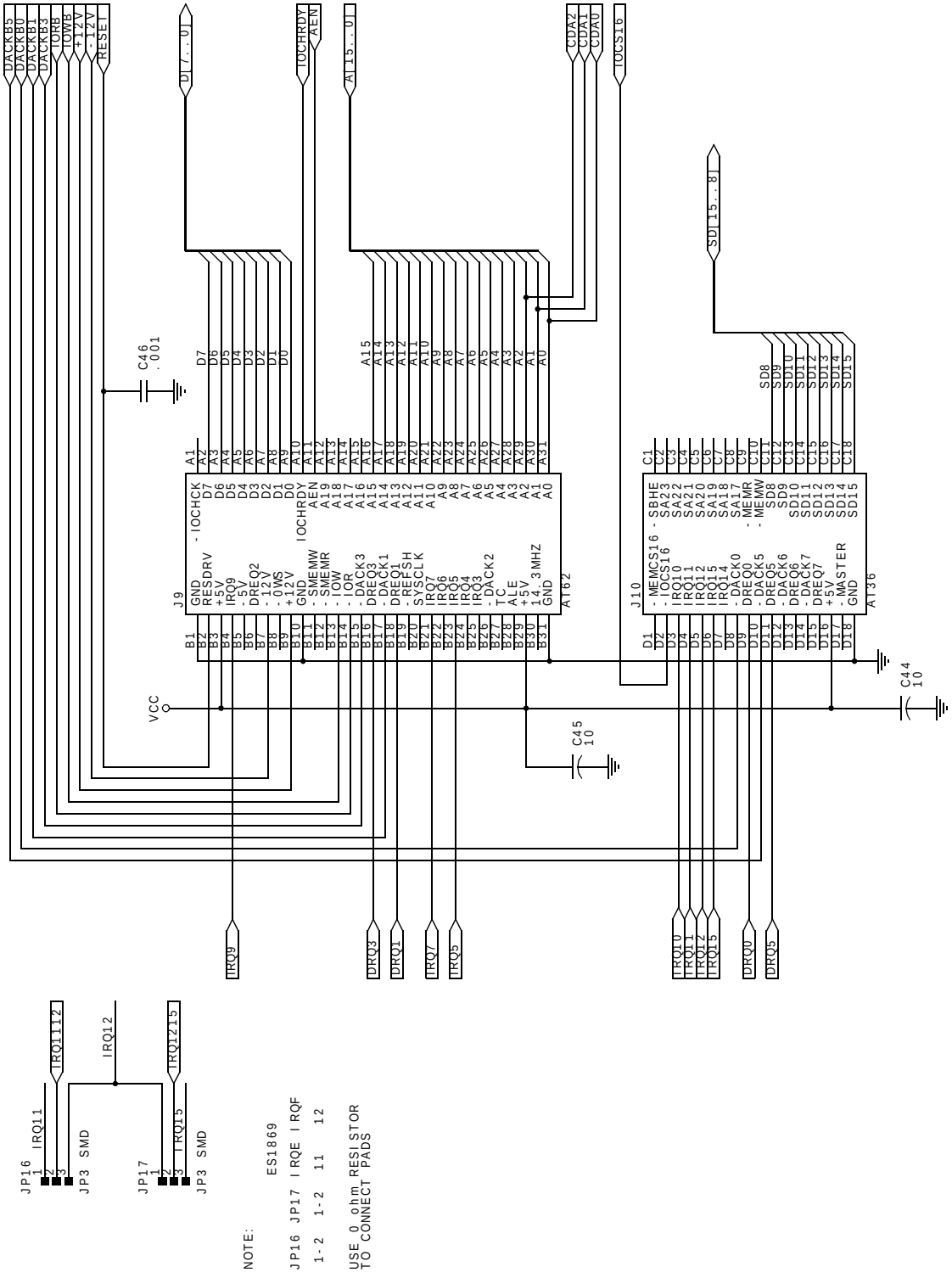


Figure 46 PC Interface – Sound Card Configuration

APPENDIX G: SOUND CARD BILL OF MATERIALS

Table 34 ES1869 Sound Card Bill of Materials (BOM)

Item	Quantity	Reference	Part
1	10	C1,C2,C3,C4,C5,C6,C7,C17,C40,C41	.1 µF
2	12	C8,C9,C27,C28,C29,C30,C31,C32,C47,C48,C49,C50	.22 µF
3	1	C46	.001 µF
4	4	C10,C33	680 pF
5	1	C11	.047 µF
6	6	C12,C13,C36,C37,C44,C45	10 µF
7	2	C14,C43	47 µF
8	2	C15,C16	10 pF
9	10	C18,C19,C20,C21,C23,C24,C25,C26,C38,C39	.01 µF
10	1	C22	150 pF
11	2	C34,C35	470 µF
12	1	C42	100 µF
13	1	JP2 (L), JP6 (11), JP17 (12)	0 ohm
14	4	J1,J2,J7,J8	3.5 mm Stereo Jack
15	1	J3	DB15S
16	1	J4	4x1 Header
17	1	J5	13x2 Header optional wavetable connector
18	1	J6	20x2 Header
19	1	J11	3x1 Header
20	9	L1,L2,L4,L5,L6,L7,L8,L9,L10	Ferrite Bead
21	2	R1,R2	7.5K
22	10	R3,R4,R5,R6,R8,R9,R20,R22,R23,R24	2.2K
23	2	R7,R19	10K
24	4	R14,R15,R16,R17	1K
25	1	R18	22K
26	2	R22,R23	33K
27	4	R24,R25,R26,R27	820K
28	2	R28,R29	2.7 ohm
29	2	R30,R31	100K
30	2	R32,R33	10K
31	4	R34,R35,R36,R37	1M
32	1	R41	0 ohm
33	3	S1,S2,S3	Pushbutton
34	1	U1	78L05
35	1	U2	74LS138
36	1	U3	ES1869F
37	1	U4	93LC66
38	1	U7	LM1877
39	1	Y1	14.318 MHz
WITH OPTIONAL ES692 WAVETABLE MUSIC SYNTHESIZER:			

Table 34 ES1869 Sound Card Bill of Materials (BOM) (Continued)

Item	Quantity	Reference	Part
40	1	U9	ES692-TQFP100
41	1	U8	LT1129-3.3
42	1	Y2	33.000 MHz
43	1	C51	1.0 µF
44	1	C52	3.0 µF
45	2	C53,C55	10 pF
46	1	C54	.001 µF
47	3	C56,C57,C58	.1 µF
48	1	R39	47K
49	1	L3	2.2 µH

APPENDIX H: LAYOUT GUIDELINES

PCB Layout

Notebook, Motherboard, Pen-based, and PDA portable computers have the following similarity in PCB layout design:

1. Multi-layer (usually 4 to 8 layer).
2. Double-sided SMT.
3. CPU, corelogic (chip set), system memory, VGA controller, and video memory reside in the same PCB.

This is a very noisy environment for adding an audio circuit. The following are the guidelines for PCB layout for an ESS *Audio***Drive**® chip application.

Component Placement

The audio circuit-related components, including the audio I/O jack and connector, must be grouped in the same area.

There are two possible placements for these audio components:

A grouped on one side of the PCB.

B separated on both sides of the PCB.

In Case B, audio component grouping will take less space.

Analog Ground Plane

Audio circuits require two layers of analog ground planes for use as shielding for all analog traces.

In component placement case A (Figure 47), the first layer of analog ground plane is on the analog component side, the second analog ground plane is on the inner layer, and the analog traces are embedded between these two planes.

In component placement case B (Figure 48), the analog ground planes are on both sides of the PCB, and the analog traces are shielded in the middle.

Case A:

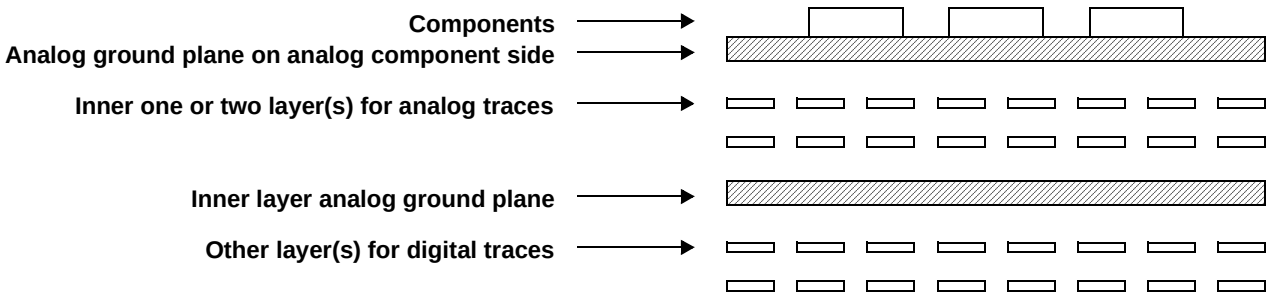


Figure 47 Analog Components on One Side of the PCB

Case B:

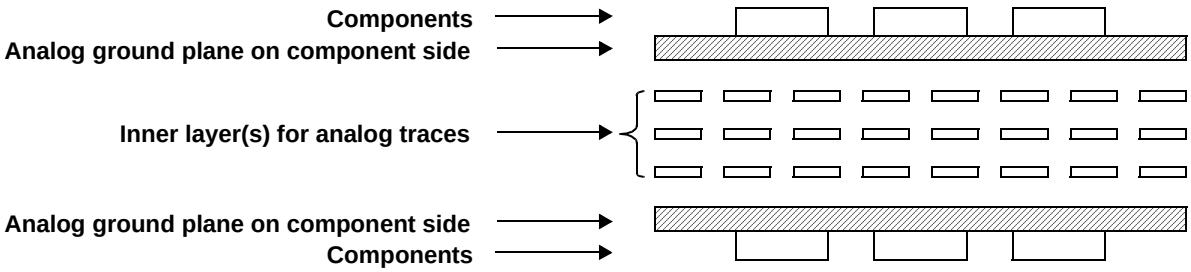


Figure 48 Analog Components on Both Sides of the PCB

Special Notes

The analog traces should be placed as short as possible.

The MIC-IN circuit is the most sensitive of the audio circuits, and requires proper and complete shielding.

ESS Technology, Inc.
48401 Fremont Blvd.
Fremont, CA 94538
Tel: 510-492-1088
Fax: 510-492-1098