Power Factor Controller **SG6561/A**

FEATURES

- Boundary Mode PFC Controller
- Low Input Current THD
- Controlled On-Time PWM
- Zero-Current Detection
- Cycle-by-Cycle Current Limiting
- Leading-Edge Blanking instead of RC Filtering
- Fast Current Sense Propagation Delay
- Low Start-Up Current (20uA)
- Low Operating Current (4.5mA)
- Feedback Open Loop Protection
- Programmable Maximum On-Time (MOT)
- Output Over-Voltage Clamping Protection
- Clamped Gate Output Voltage 17V
- Few External Components Required
- Pin Compatible with the L6561

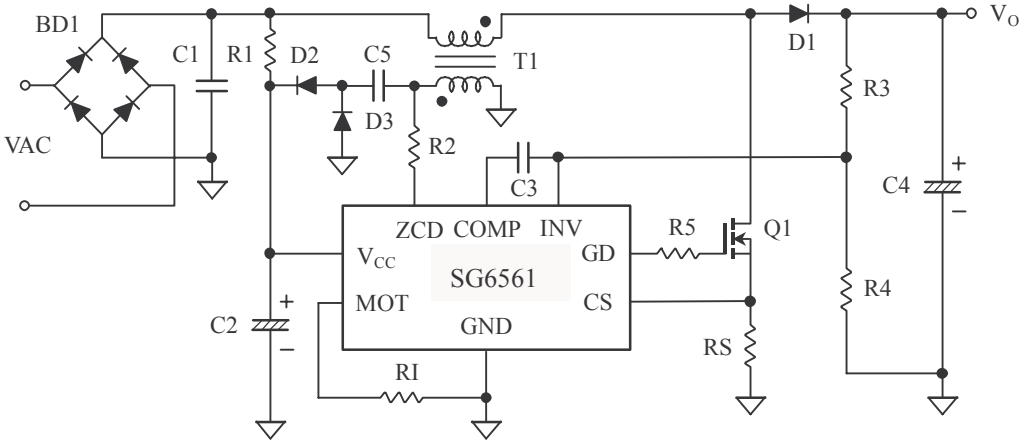
APPLICATIONS

- Electronic Lamp Ballasts
- AC-DC Switching Mode Power Converters
- Open Frame Power Supplies and Power Adapters
- Flyback Power Converters with ZCS/ZVS

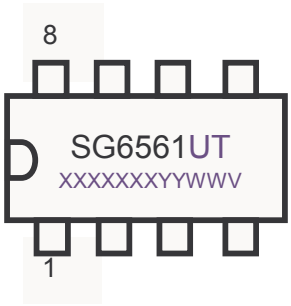
DESCRIPTION

The SG6561/A PFC controller is an 8-pin boundary mode IC intended for controlling PFC pre-regulators. The SG6561/A is pin compatible with the L6561, and it has many new features. It provides a controlled on-time to regulate the output DC voltage and achieve natural power factor correction. The maximum on-time of the switch is programmable to ensure safe operation during brownouts. An innovative multi-vector error amplifier is built in to provide rapid transient response and precise output voltage clamping. A built in circuit will disable the controller if the output feedback loop is opened. The start up current is lower than 20uA and the operating current has been shrunk to 4.5mA. The supply voltage can be up to 25 volts, maximizing application flexibility. The SG6561/A enables cycle-by-cycle current limiting protection for the external power MOSFET to be easily achieved.

TYPICAL APPLICATION



MARKING DIAGRAMS



U: A= With Advanced Features

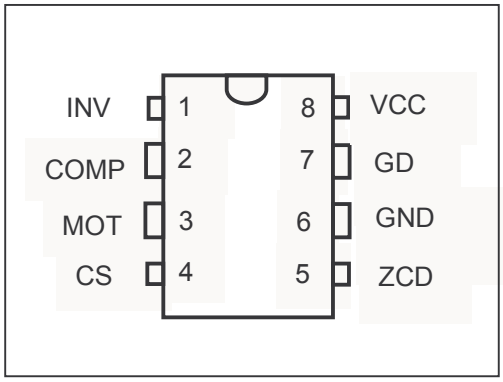
Null=Without Advanced Features

T: D = DIP, S = SOP

XXXXXXX: Wafer Lot

YY: Year; WW: Week

PIN CONFIGURATION



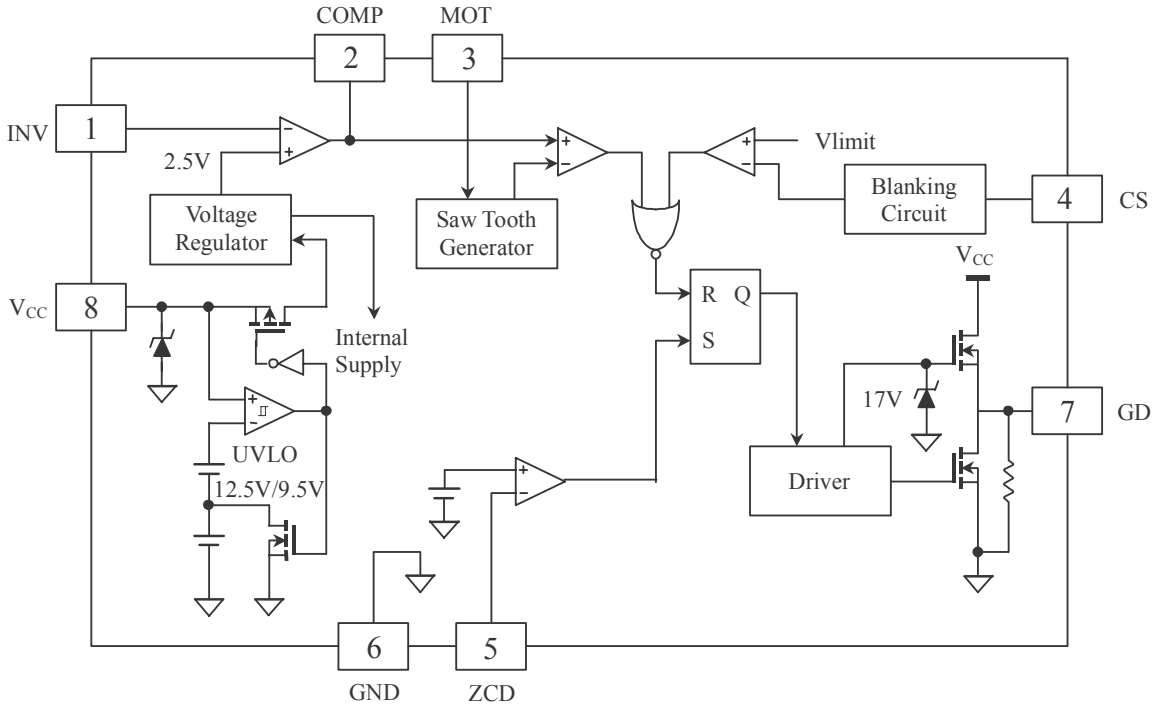
ORDERING INFORMATION

Part Number	Package
SG6561D	8-pin DIP
SG6561S	8-pin SOP
SG6561AD	8-pin DIP
SG6561AS	8-pin SOP

PIN DESCRIPTIONS

Pin	Name	Function
1	INV	Inverting input of the error amplifier. INV is connected to the converter output via a resistive divider. This pin is also used for over-voltage clamping and open loop feedback protection.
2	COMP	The output of the error amplifier. A feedback compensation network can be placed between this pin and the INV(SG6561). In order to create precise clamping protection, a compensation network between this pin and GND is suggested(SG6561A).
3	MOT	A resistor from MOT to GND is used to determine the maximum ON-time of the external switch. The maximum output power of the converter is a function of the maximum ON-time. The MOT pin is used to replace the multiplier stage of L6561.
4	CS	Input to the over-current protection comparator. When the sensed voltage across the sense resistor reaches the internal threshold (0.8V), the switch will be turned off to activate cycle-by-cycle current limiting.
5	ZCD	Zero Current Detection. This pin is connected to an auxiliary winding via a resistor to detect the zero crossing of the switch current. When the zero crossing is detected, a new switching cycle is started.
6	GND	The power ground and signal ground. Placing a 0.1uF decoupling capacitor between V_{CC} and GND is recommended.
7	GD	Totem-pole output to drive the external power MOSFET. The clamped gate output voltage is 17V.
8	V_{CC}	Driver and control circuit supply voltage.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Condition	Value	Unit
V_{CC}	DC Supply Voltage*		27	V
V_{HIGH}	INV, ZCD, GD		-0.3 to 25V	V
V_{LOW}	Others (COMP,CS, MOT)		-0.3 to 7V	V
$R_{\theta J-A}$	Thermal Resistance	Junction-Air DIP SOP	82.5 141	°C/W
T_J	Operating Junction Temperature		+150	°C
T_A	Operating Ambient Temperature		-40 to 125	°C
T_{STG}	Storage Temperature Range		-65 to +150	°C
T_L	Lead Temperature (soldering)	10 sec DIP 20 sec SOP	260 220	°C
	ESD Capability, HBM Model		2.0	kV

*All voltage values, except differential voltages, are given with respect to the network ground terminal.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	-0.3	25	V
R_I	T_{ON}-Max Resistor	10	48	kΩ
T_{ON-MAX}	T_{ON}-Max Time	10	50	usec
T_A	Operating Ambient Temperature	-30	85	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 12V; T_A=25°C)

V_{CC} Section

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$V_{TH(ON)}$	Start Threshold Voltage	V_{CC} Slew Rate= 8V / sec	11	12	13	V
$V_{CC(MIN)}$	Min. Operating Voltage	V_{CC} Slew Rate= 8V / sec	8.5	9.5	10.5	V
$I_{CC\ ST}$	Start-Up Current	V_{CC} = 11V		10	20	uA
$I_{CC\ OP}$	Operating Current	V_{CC} = 12V. Maximum On-Time Conduction (asssuming the output is switching with a 3000pF capacitive load)		4.5	6	mA
V_{CC-OVP}	V_{CC} OVP	PWM Off	25	26.6	28	V

Error Amp (SG6561A compensation capacitor is connected between COMP pin and GND.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{REF}	Reference Voltage		2.45	2.5	2.55	V
A_V	Open Loop Gain			70		dB
B_W	Gain Bandwidth			1		MHz
Z_o	Output Impedance			120		kΩ
I_{FB}	Input Bias Current			-0.1		uA
V_{FBH}	Clamp High Feedback Voltage		2.6	2.65	2.7	V
$V_{FBL\ P}$	Clamp Low Feedback Voltage		2.35	2.4	2.45	V
$V_{OUT\ HIGH}$	Output High Voltage			5		V
V_{oz}	Zero Duty Cycle Output Voltage		0.9	1.1	1.3	V
$V_{inv-ovp}$	OVP for INV Input		2.7	2.75	2.8	V
$V_{inv-UVP}$	UVP for INV Input		0.4	0.45	0.5	V

Error Amp (SG6561 compensation capacitor is connected between COMP pin and INV pin.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{REF}	Reference Voltage		2.45	2.5	2.55	V
A_V	Open Loop Gain			70		dB
B_W	Gain Bandwidth			1		MHz
I_{FB}	Input Bias Current			-0.1		uA
$V_{OUT\ HIGH}$	Output High Voltage			5		V
V_{OZ}	Zero Duty Cycle Output Voltage		0.9	1.1	1.3	V
I_{OVP}	OVP Triggering Current		25	30	35	uA
$V_{INV-OVP}$	OVP for INV Input		2.7	2.75	2.8	V
$V_{INV-UVP}$	UVP for INV Input		0.4	0.45	0.5	V

Current Sense (V_{LIMIT})

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{PK}	Threshold Voltage for Peak Current Limit Cycle by Cycle Limit ($V_{CS} < V_{PK}$)		0.75	0.8	0.85	V
I_{CS}	Input Bias Current			-0.1		uA
T_{PKD}	Propagation Delay				200	nsec
B_{NKT}	Leading-Edge Blanking Time		250	350	500	nsec

Output Driver

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$VZ\text{-}_{OUT}$	Output Voltage Maximum (clamp)	V_{CC}= 24V	16	17	18	V
V_{OL}	Output Voltage Low	V_{CC} = 12V, I_O = 100mA	0.6	1.0	1.4	V
V_{OH}	Output Voltage High	V_{CC} = 12V, I_O = 100mA	6.3	7.3	8.3	V
T_R	Rising Time	V_{CC} =12V, C_L=3nF	80	180	250	nsec
T_F	Falling Time	V_{CC} =12V, C_L=3nF	50	80	120	nsec

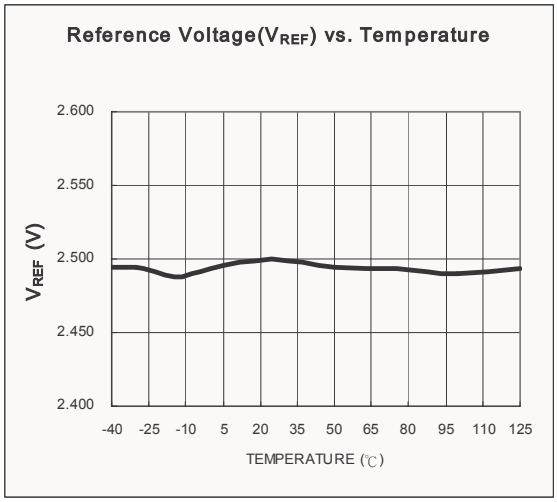
Zero Current Detection

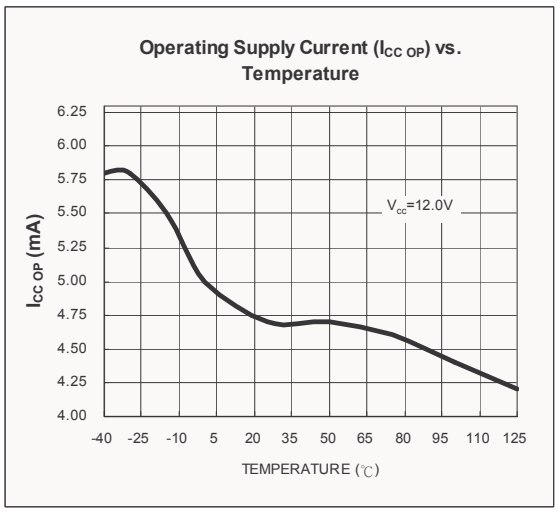
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{ZCD}	Input Threshold Voltage Rising Edge			2.1		V
H_{YS} of V_{ZCD}	Threshold Voltage Hysteresis		0.45	0.65	0.85	V
$I_{ZCD-MAX}$	Sink & Source Current Capability				10	mA
$V_{ZCD-HIGH}$	Upper Clamp Voltage	I = 3 mA			Vcc	V
$V_{ZCD-LOW}$	Lower Clamp Voltage	I = -3 mA		-0.65	-1	V
I_{ZCD-S}	Source Current when V_{ZCD} = 0V	V_{ZCD} = 0V		-0.6		mA
T_{DEAD}	Maximum Delay from ZCD to Output Turn-On (normal mode)	R_I = 24kΩ	100		400	nsec
$T_{RESTART}$	Restart Time	Output Turned Off by ZCD	300	500	700	usec
$V_{DIS-COMP}$	Minimum Comp Voltage to Disable Restart	COMP< V_{DIS_COMP}	1.4	1.7	2.0	V

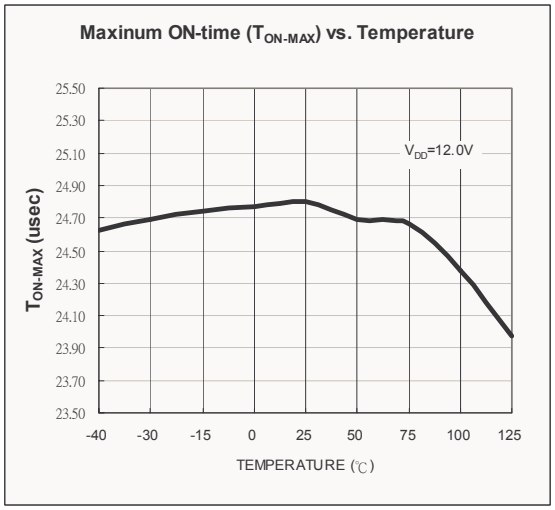
Maximum ON-Time

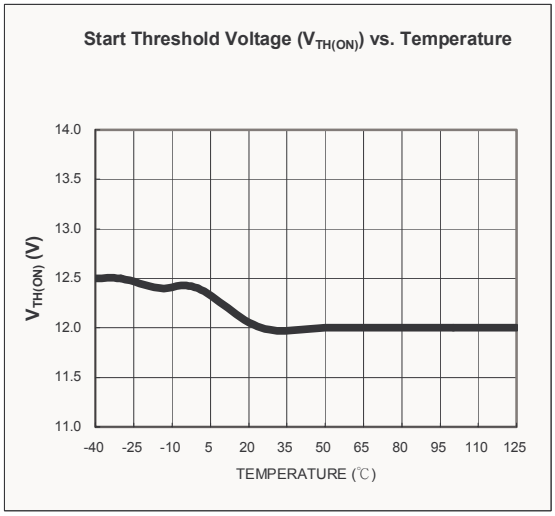
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
VRT	MOT Voltage	R_I = 24K	1.248	1.273	1.298	V
Ton-max	Maximum On-Time Programming (resistor-based)	R_I = 24K	22	25	28	usec

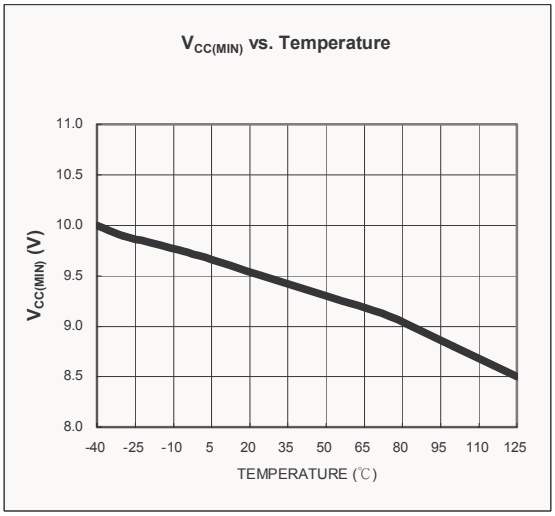
TYPICAL CHARACTERISTICS

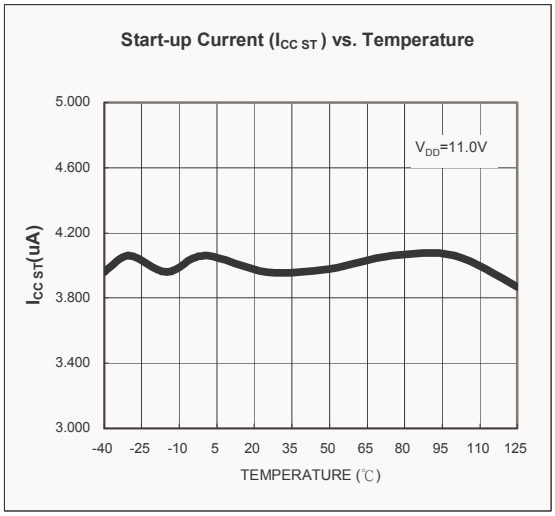


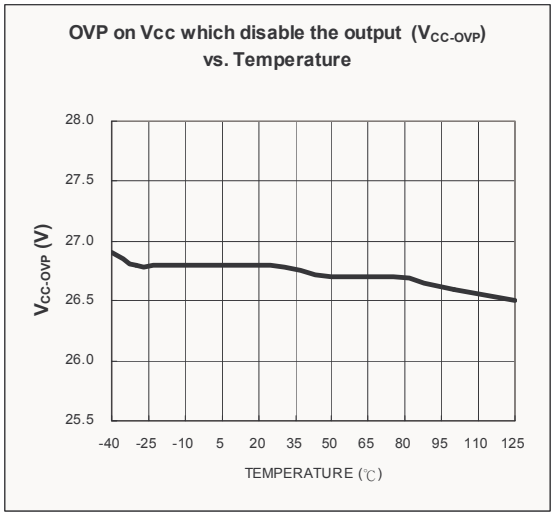


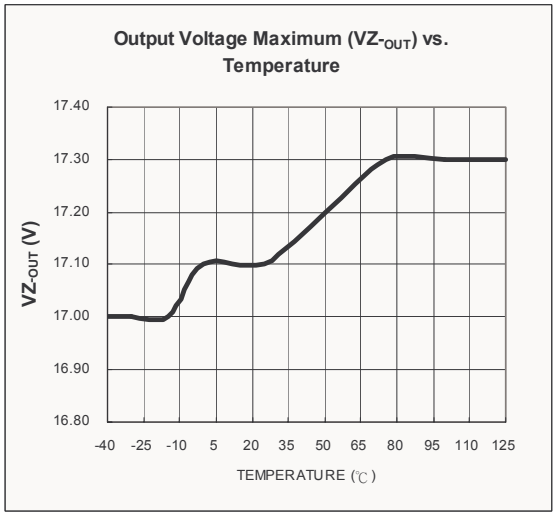


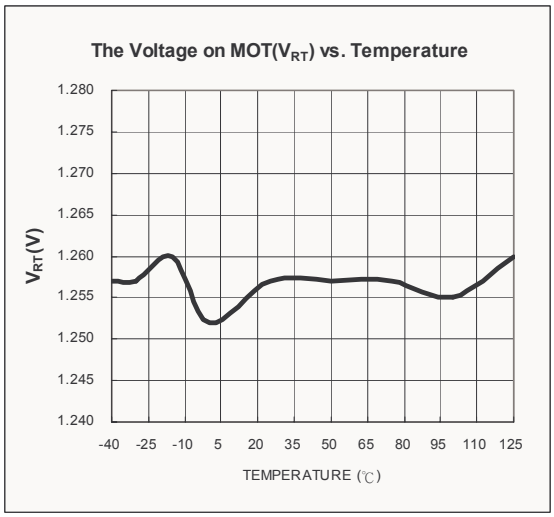


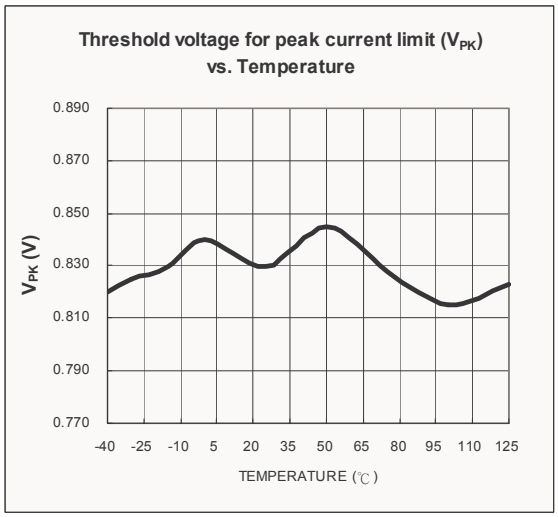





OVP on Vcc which disable the output (V_{CC-OVP}) vs. Temperature
V_{CC-OVP} (V)
28.0
27.5
27.0
26.5
26.0
25.5
-40 -25 -10 5 20 35 50 65 80 95 110 125
TEMPERATURE (℃)


Output Voltage Maximum ($VZ-_{OUT}$) vs. Temperature
VZ_{-OUT} (V)
17.40
17.30
17.20
17.10
17.00
16.90
16.80
-40 -25 -10 5 20 35 50 65 80 95 110 125
TEMPERATURE (℃)


The Voltage on MOT(V_{RT}) vs. Temperature
V_{RT}(V)
1.280
1.275
1.270
1.265
1.260
1.255
1.250
1.245
1.240
-40 -25 -10 5 20 35 50 65 80 95 110 125
TEMPERATURE (℃)


Threshold voltage for peak current limit (V_{PK}) vs. Temperature
V_{PK} (V)
0.890
0.870
0.850
0.830
0.810
0.790
0.770
-40 -25 -10 5 20 35 50 65 80 95 110 125
TEMPERATURE (℃)

OPERATION DESCRIPTION

Error Amplifier

The inverting input of the error amplifier is referenced to INV. The output of the error amplifier is referenced to COMP. The non-inverting input is internally connected to a fixed 2.5V ± 2% voltage. The output of the error amplifier is used to determine the on-time of the PWM output and hence regulate the output voltage. To achieve a low input current THD, the variation of the on-time within one input AC cycle should be very small. A multi-vector error amplifier is built in to provide fast transient response and precise output voltage clamping.

For SG6561A, connecting a high capacitance such as 10 uF between COMP and GND is suggested. The error amplifier is a trans-conductance amplifier that converts voltage to current with a 120k Ω output impedance.

For SG6561, the compensation network should be connected between the COMP pin and the INV pin. A built in circuit will disable the controller if the output feedback loop is opened or if the output voltage is too high.

In order to provide precise voltage clamping protection for output capacitor, it is recommended to use SG6561A. The application circuits of SG6561A and SG6561 are illustrated in REFERENCE CIRCUIT.

Start-Up Current

Typical start-up current is less than 20uA. This ultra-low start-up current allows the usage of a high-resistance, low-wattage start-up resistor. For an AC-to-DC power adaptor with a wide input range of 85-265VAC, a 1MΩ/0.25W start-up resistor and a 10uF/25V (V_{CC} hold-up) capacitor are recommended.

Operating Current

The operating current is typically 4.5mA. The low operating current results in improved efficiency and reduces the V_{CC} hold-up capacitance requirement.

Maximum On-Time Operation

Given a fixed inductor value and maximum output power, the relationship between the on-time and the line voltage is:

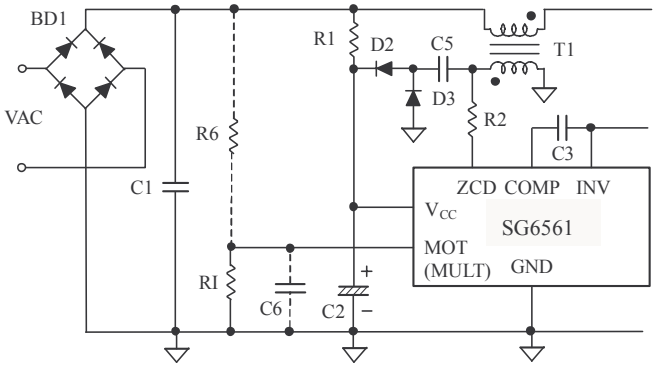
$$T_{ON} = \frac{2LP_O}{V_{rms}^2} \text{ ----------(1)}$$

If the line voltage is too low or if the inductance is too high, the duration of T_{ON} will be too long. To avoid excessively low operating frequencies, and to achieve brownout protection, the maximum value of T_{ON} can be programmed by changing the resistor R_I connected between MOT and GND. A 24kΩ resistor R_I results in a maximum on-time of 25usec.

$$T_{ON(max)} = R_I(k\Omega) \times \frac{25}{24}(u\sec) \text{ ----------(2)}$$

The range of the maximum on-time is designed to be within 10 ~ 50usec.

For direct pin-to-pin drop-in replacement with L6561, the R6 resistor and C6 capacitor is needed to remove from the PCB. RI resistor needs to change to suitable value (10kΩ ~ 48kΩ) for maximum on time of external switch.



Peak Current Limiting

The switch current is sensed across a resistor. The signal is supplied to an input terminal of a comparator via the CS pin. A high voltage at the CS pin will immediately terminate the current switching cycle, thus

activating cycle-by-cycle current limiting. The designed protection point threshold is 0.8V.

Leading-Edge Blanking

A turn-on spike will inevitably occur at the CS pin when the power MOSFET is switched on. At the beginning of each switching pulse, the current-limit comparator is disabled for around 350nsec to avoid premature termination. The gate drive output cannot be switched off during the blanking period. Conventional RC filtering is not necessary, thus the current limit protection propagation delay can be minimized.

Under-Voltage Lockout (UVLO)

The turn-on and turn-off threshold voltages are fixed internally at 12V/9.5V for the SG6561AD/AS. This hysteresis behavior will guarantee a one shot start-up, as long as a proper start-up resistor and hold-up capacitor are used. With an ultra-low start-up current of 20uA, a R_{IN} of 1MΩ will be sufficient to start-up the SG6561A under low input line voltages (eg, $85V_{RMS}$). In this case, the power dissipation across R_{IN} would be less than 0.1W even under high line (V_{AC} = $265V_{RMS}$) conditions.

Output Driver

With a low ON-resistance and a high current driving capability, the output driver can easily drive an external capacitive load larger than 3000pF. Cross conduction currents have been avoided to minimize heat dissipation, allowing the efficiency and reliability to be improved. This output driver is internally clamped by a 17V Zener diode.

Zero Current Detection

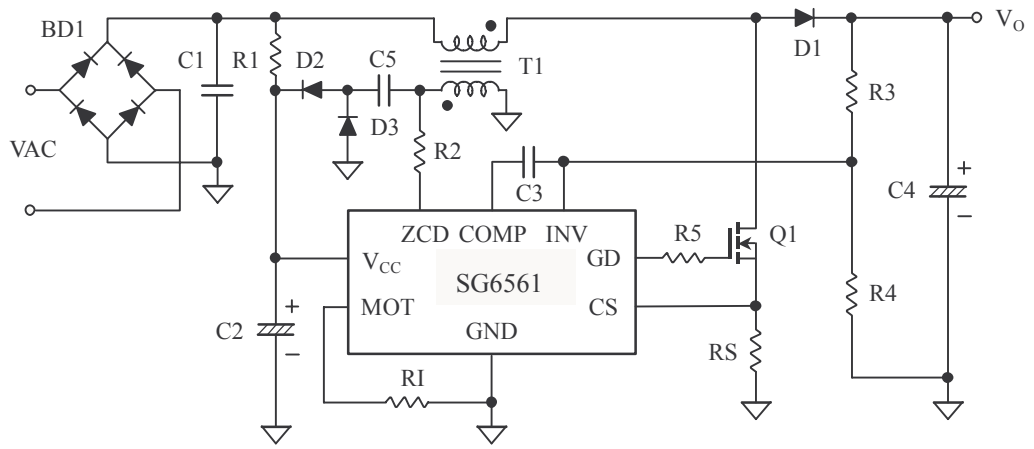
By using an auxiliary winding of the inductor, the SG6561/A can perform zero current detection. When the stored energy of the inductor is fully released to the output, the ZCD voltage will decrease, and a new switching cycle will be initiated following the ZCD trigger. The power MOSFET will always be turned on with zero inductor current, so that turn-on losses and noise can be minimized. The converter will work in boundary mode, so that the peak inductor current will always be exactly twice the average current. Moreover, the SG6561/A has low-bandwidth on-time modulation, resulting in automatic power factor correction function without any additional circuitry. The SG6561/A has a maximum off-time function to ensure proper start-up operation. This pin can be used as a synchronous input.

Noise Immunity

Current sense or control signal noise can cause significant pulse width jitter, particularly during boundary-mode operation. Slope compensation and the built-in debounce circuit can alleviate this problem. However, the SG6561/A has a single ground pin. Therefore, a high sink current at the output cannot be returned separately. Good high frequency or RF layout practices should be followed. The designer should avoid long PCB traces and component leads. Compensation and filter components should be located near the SG6561/A. The power MOSFET gate resistance should be increased as much as possible within operational limits.

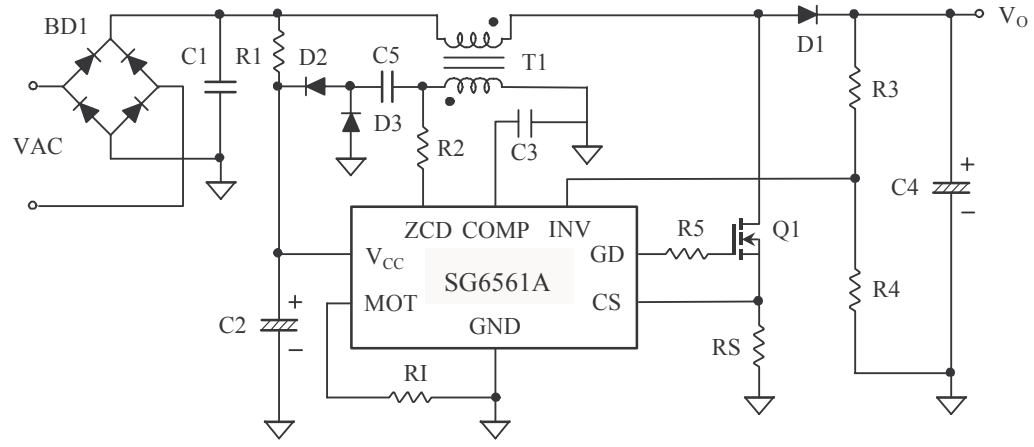
REFERENCE CIRCUIT: SG6561

Circuit: The compensation capacitor C3 is connected from the COMP pin to INV pin.



REFERENCE CIRCUIT: SG6561A

Circuit: The compensation capacitor C3 is connected from the COMP pin to ground.

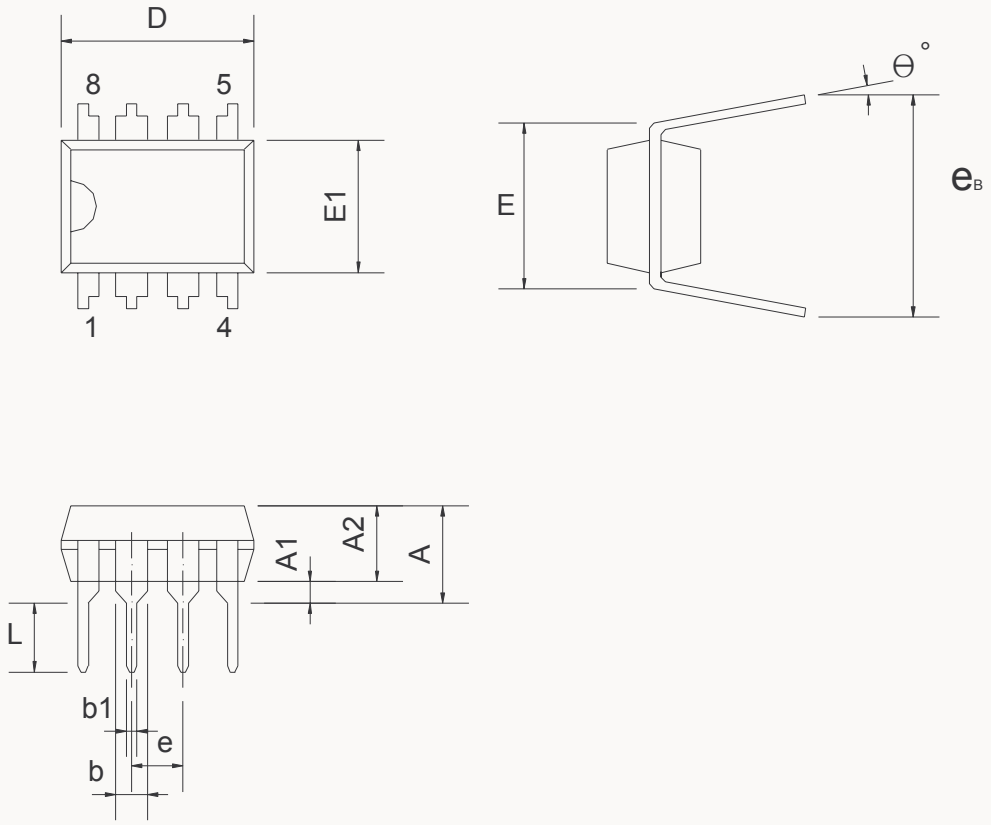


BOM

Reference	Components	Reference	Components
BD1	1N4007×4	T1	
C1	1uF/400V	Q1	MOS STP8NA50
C2	22uF/25V	R1	1MΩ
C3	10uF	R2	68kΩ 1/4W
C4	47uF/450V	R3	998kΩ, 1%
C5	10nF	R4	6.34kΩ, 1%
D1	BYT13-600	R5	10Ω
D2	1N4150	RI	10kΩ~48kΩ
D3	1N5248B	RS	0.4Ω, 1W

PACKAGE INFORMATION

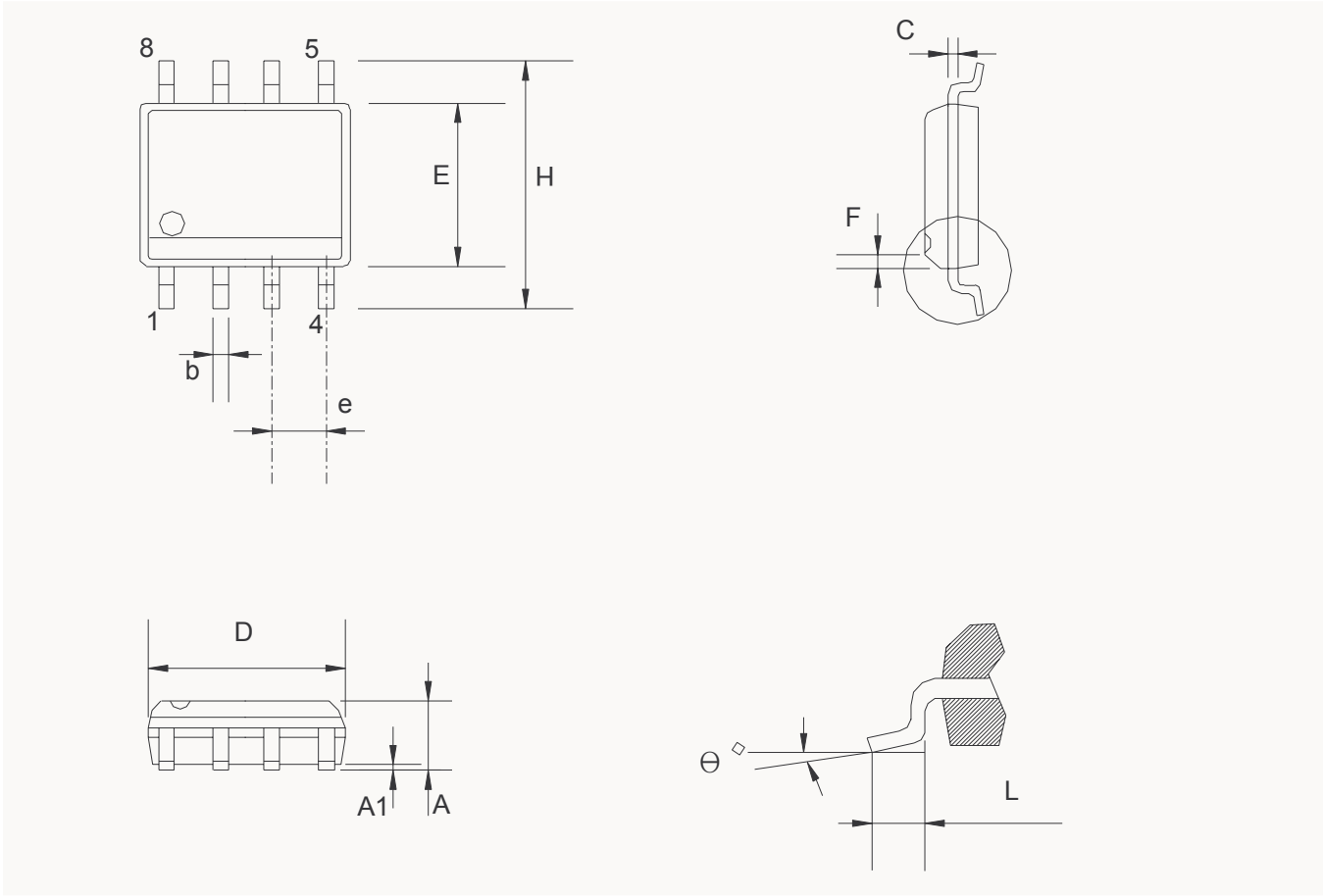
8 PINS-DIP(D)



Dimension

Symbol	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.334			0.210
A1	0.381			0.015		
A2	3.175	3.302	3.429	0.125	0.130	0.135
b		1.524			0.060	
b1		0.457			0.018	
D	9.017	9.271	10.160	0.355	0.365	0.400
E		7.620			0.300	
E1	6.223	6.350	6.477	0.245	0.250	0.255
e		2.540			0.100	
L	2.921	3.302	3.810	0.115	0.130	0.150
e_B	8.509	9.017	9.525	0.335	0.355	0.375
θ°	0°	7°	15°	0°	7°	15°

8 PINS-SO(S)



Dimension

Symbol	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.346		1.752	0.053		0.069
A1	0.101		0.254	0.004		0.010
b		0.406			0.016	
c		0.203			0.008	
D	4.648		4.978	0.183		0.196
E	0.381		3.987	0.150		0.157
e		1.270			0.050	
F		0.381X45°			0.015X45°	
H	5.791		6.197	0.228		0.244
L	0.406		1.270	0.016		0.050
θ°	0°		8°	0°		8°

DISCLAIMERS

LIFE SUPPORT

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