

Real Time Clock Module — RTC 58321



8003329 SARONIX CO

70C 00039 D T-51-19

by SaRonix

Technical Data

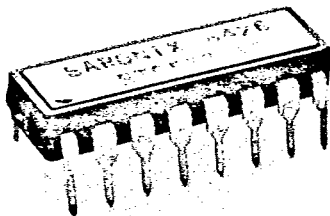
Ref. No. RTC
 Date May 1985
 Page 1 of 2

Description

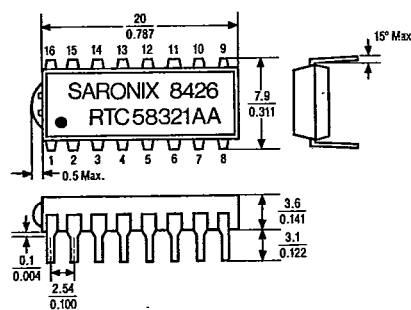
A Real Time Clock incorporating an on board quartz crystal in a single 16-pin DIP package, eliminating the need for external crystal, resistors and capacitors.

Features

- Built in 32.768kHz quartz crystal.
- Low power standby operation.
- Addressable counter start, stop, and reset function.
- 12-hour or 24-hour format.
- Automatic leap year selection.
- Microprocessor compatible 4-bit data bus.
- Standard 16-pin DIP package.
- Pin to pin compatible with MS58321RS.



Package

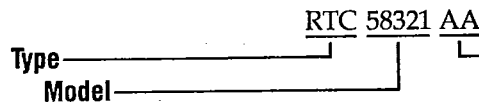


Function Table

Internal Counter	Address	Address Input				Address Output				Count Value	Remarks
		D ₃ (A ₃)	D ₂ (A ₂)	D ₁ (A ₁)	D ₀ (A ₀)	D ₃	D ₂	D ₁	D ₀		
S ₁	0	L	L	L	L	*	*	*	*	0~9	
S ₁₀	1	L	L	L	H	*	*	*	*	0~5	
MI ₁	2	L	L	H	L	*	*	*	*	0~9	
MI ₁₀	3	L	L	H	H	*	*	*	*	0~5	
H ₁	4	L	H	L	L	*	*	*	*	0~9	
H ₁₀	5	L	H	L	H	*1	*	*	*	0~1	D ₂ H for p.m., L for a.m., D ₃ =H for 24-hour clock, L for 12-hour clock. When D ₃ =H is written, the D ₂ bit is reset inside the IC and remains constantly at L.
										0~2	
W	6	L	H	H	L	*	*	*	*	0~6	D ₂ and D ₃ in the D ₁₀ line are for leap year selection.
D ₁	7	L	H	H	H	*	*	*	*	0~9	
D ₁₀	8	H	L	L	L	*2	*2	*	*	0~3	Calendar D ₃ D ₂ Remainder when divided years by 4
MO ₁	9	H	L	L	H	*	*	*	*	0~9	Western L L 0
MO ₁₀	A	H	L	H	L	*	*	*	*	0~1	Japanese L H 3
Y ₁	B	H	L	H	H	*	*	*	*	0~9	H L 2
Y ₁₀	C	H	H	L	L	*	*	*	*	0~9	H H 1
		D	H	H	L	H					These selections are for resetting the 5-stage and the BUSY circuit after the 1/2 ¹⁵ frequency stage. Resetting is activated by latching this code on to the address latch and setting the WRITE input to H.
		E									These selections are for obtaining standard signals. By latching this code on to the address latch and setting READ to H, the standard signals will be output at D ₀ ~D ₃ .
			H	H	H	L/H					
		F									

- Note 1. The blank spaces in the data input/output columns indicate that there are no bits. When READ is performed the L level is output. When WRITE is performed nothing will be stored in the memory because there are no bits.
- Note 2. The bit indicated by the symbol *1 is for selecting the 12hr/24hr clock and those indicated by *2 are for leap year selection. READ and WRITE are possible with all three bits.
- Note 3. For address input, send a signal to the D₀~D₃ bus line, then input ADDRESS WRITE. The ADDRESS data will be latched on to the address latch.

Part Numbering Guide



Stability Tolerance:
 AA = ±10 ppm (0.001%)
 A = ±25 ppm (0.0025%)
 B = ±50 ppm (0.005%)

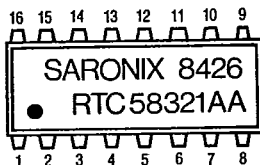


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Ref. No.	RTC
Date	May 1985
Page	2 of 2

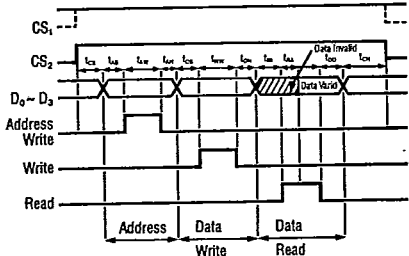
Pin Connections



16	15	14	13	12	11	10	9
V_{DD}	NC	NC	CS_1	TEST	STOP	BUSY	ADRSS WRITE
1	2	3	4	5	6	7	8
CS_2	WRITE	READ	D_0	D_1	D_2	D_3	V_{SS}

NC: Do not connect externally.

Write and Read Timing



($V_{DD} = 5V \pm 5\%$ $T_a = 25^\circ C$)

Item	Symbol	Min	Max	Units
CS set-up time	t_{CS}	0	—	μS
Address set-up time	t_{AS}	0	—	μS
Address write pulse range	t_{AW}	0.5	—	μS
Address hold time	t_{AH}	0.1	—	μS
Data set-up time	t_{DS}	0	—	μS
Write pulse range	t_{WW}	2	—	μS
Data hold time	t_{DH}	0	—	μS
Read inhibit time	t_{RI}	0	—	μS
Read access time	t_{RA}	—	*	μS
Read delay time	t_{RD}	—	1	μS
CS hold time	t_{CH}	0	—	μS

$t_{RA} = 1\mu S + CR \ln \left(\frac{V_{DD}}{V_{DD} - V_H} \right)$

C: Data line wiring capacity
 R: Pull-up resistance value
 V_H : "H" input voltage of the IC connected to the data line
 ln: Natural logarithms

Electrical Characteristics

Absolute Maximum Ratings

Item	Symbol	Conditions	Rated Value	Unit
Power voltage	V_{DD}	$T_a = 25^\circ C$	-0.3~7	V
Input voltage	V_i	$T_a = 25^\circ C$	GND -0.3~ $V_{DD} + 0.3$	V
Output voltage	V_o	$T_a = 25^\circ C$	GND -0.3~ $V_{DD} + 0.3$	V
Storage temperature	T_{stg}	—	-30~+80	$^\circ C$

Working Range

Item	Symbol	Conditions	Range	Units
Power voltage	V_{DD}	—	4.5~5.5	V
Data-holding voltage	V_{DH}	—	2.2~5.5	V
Quartz frequency	f_0	—	32,768	kHz
Working temperature	T_{op}	—	-10~+60	$^\circ C$

Note Data-holding voltage: Data outside the IC is not guaranteed. This voltage guarantees clock operation.

Electrical Properties

$V_{DD} = 5V \pm 5\%$ $T_a = -10 \sim +60^\circ C$

Item	Symbol	Conditions	Min	Typ	Max	Unit
H. Input voltage	V_{IH1} Note 1	—	3.6	—	—	V
	V_{IH2} Note 2	—	$V_{DD} - 0.5$	—	—	V
L. Input voltage	V_{IL}	—	—	—	0.8	V
L. Output voltage	V_{OL}	$I_o = 1.6mA$	—	—	0.4	V
L. Output current	I_{OL}	$V_o = 0.4V$	1.6	—	—	mA
H. Input current	I_{IH} Note 3	$V_i = 5V$	10	30	80	μA
L. Input current	I_{IL} Note 3	$V_i = 0V$	—	—	-1	μA
$D_0 \sim D_3$ terminals input off-leak current	I_{LH}/I_{LL}	$V_i = 5V/V_i = 0V$	—	—	I/-1	μA
Input capacity	C_i	$f = 1MHz$	—	5	—	pF
		$T_a = 25^\circ C$				
Consumption current	I_{op}	$V_{DD} = 5V/V_{DD} = 3V$	—	16.5/6.2	30.0/10.0	μA
Tolerances	$\Delta f/f_0$	$T_a = 25^\circ C$ $V_{DD} = 5V$	—	—	± 10 ± 25 ± 50	ppm ppm ppm

Note 1. CS_2 WRITE, READ, ADDRESS-WRITE, STOP, TEST, $D_0 \sim D_3$ terminals.
 Note 2. CS_1 terminals.
 Note 3. CS_1 , CS_2 , WRITE, READ, ADDRESS-WRITE, STOP, TEST terminals.

Circuit Diagram

