



SP1664

QUAD 2-INPUT OR GATE

The SP1664 comprises four 2-input OR gating functions in a single package. An internal bias reference voltage ensures that the threshold point remains in the centre of the transition region over the temperature range (-30°C to +85°C). Input pull-down resistors eliminate the need to tie unused inputs to V_{EE}.

FEATURES

- Gate Switching Speed 1ns Typ.
- ECL 10000-Compatible
- 50Ω Line Driving Capability
- Operation With Unused I/Ps Open Circuit
- Low Supply Noise Generation

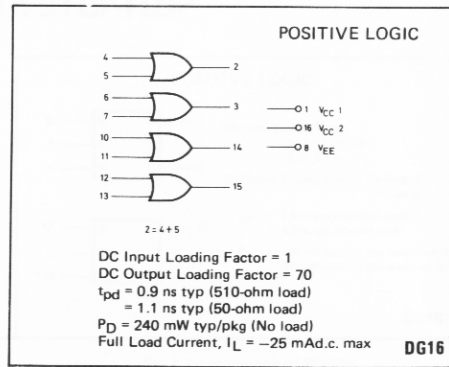


Fig. 1 Logic diagram

APPLICATIONS

- Data Communications
- Instrumentation
- PCM Transmission Systems

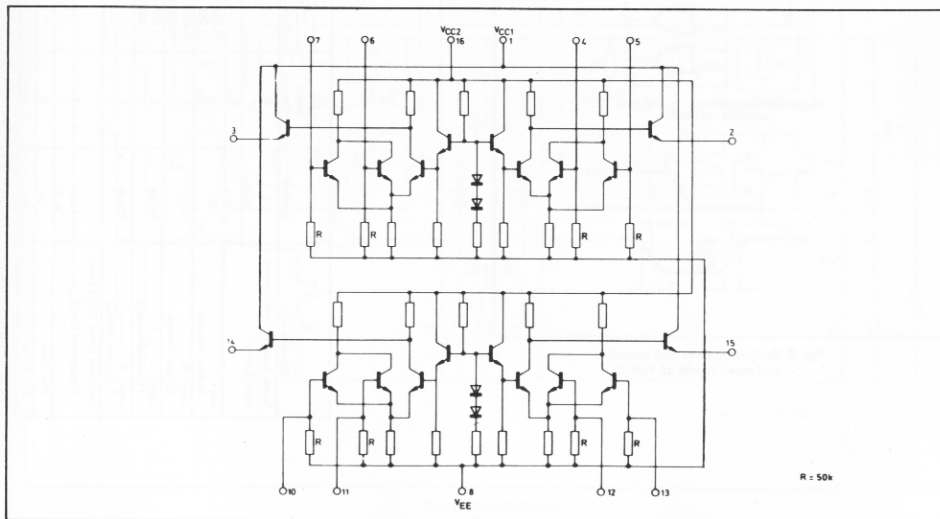


Fig. 2 Circuit diagram

ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc.

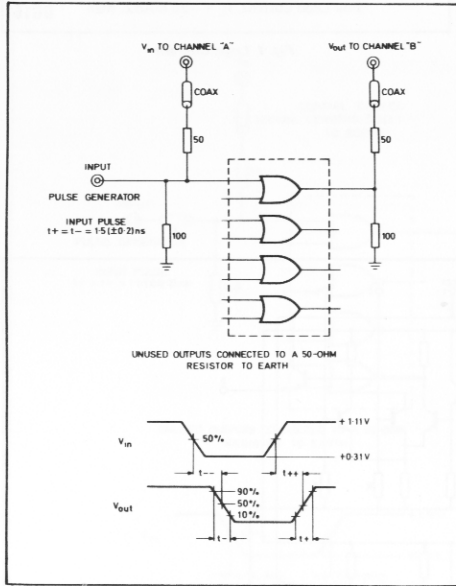


Fig. 3 Switching time test circuit and wave forms at +25°C

Characteristic	Symbol	Pin Under Test	SP1664 Test Limits						TEST VOLTAGE VALUES (Vehi)								
			-30°C		+25°C		+85°C		V _{IH} max	V _{IH} min	V _{IHLA} min	V _{IHLA} max	VEE	Grad			
Power Supply Drain Current	I _{EE}	8															
Input Current	I _{in} H	4			0.5												
Logic '1' Output Voltage	V _{OH}	2	-1.045	-0.975	-0.960	-0.810	-0.890	-0.700	Vdc	4							
Output Voltage	V _{OL}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	5							
Logic '0' Output Voltage	V _{OL}	2	-1.890	-1.675	-1.850	-1.670	-1.830	-1.575	Vdc		4						
Output Voltage	V _{OH}	2	-1.890	-1.650	-1.850	-1.650	-1.830	-1.575	Vdc		5						
Logic '1' Input Voltage	V _{IH}	2	-1.085		-0.980		-0.910		Vdc			4					
Logic '0' Input Voltage	V _{IL}	2	-1.085		-0.980		-0.910		Vdc			5					
Logic '0' Input Voltage	V _{IHLA}	2	-1.830		-1.600		-1.545		Vdc			4					
Logic '1' Input Voltage	V _{IHLA}	2	-1.830		-1.600		-1.545		Vdc			5					
Switching Times (50 Ω Load)																	
Propagation Delay	t _p 1-2	2		1.8		1.5		1.7	ns	4							
	t _p 2-1	2		1.8		1.1		1.9	ns	4							
Rise Time	t _r 2-1	2		2.2		2.1		2.3	ns	4							
Fall Time	t _f 2-1	2		2.2		2.1		2.3	ns	4							

* Individually test each input applying V_{IH} or V_{IL} to input under test.