PLESSEY
Semiconductors

SP1662

QUAD 2-INPUT NOR GATE

The SP1662 comprises four 2-input NOR gating functions in a single package. An internal bias reference voltage ensures that the threshold point remains in the centre of the transition region over the temperature range -30°C to +85°C.

Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

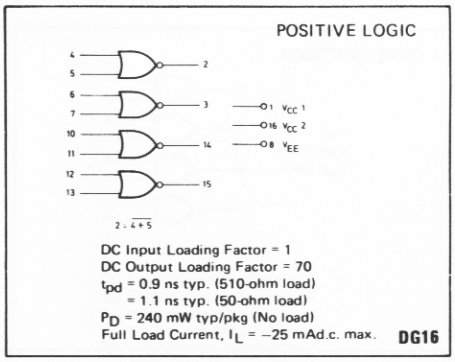

Fig. 1 Logic diagram

FEATURES

- Gate Switching Speed Ins Typ.
- ECL 10000—Compatible
- 50Ω Line Driving Capability
- Operation With Unused I/Ps Open Circuit
- Low Supply Noise Generation

APPLICATIONS

- Data Communications
- Instrumentation
- PCM Transmission Systems

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $\|V_{CC} - V_{EE}\|$	8V
Base input voltage	0V to V_{EE}
O/P source current	< 40mA
Storage temperature	−55°C to +150°C
Junction operating temp.	< +125°C

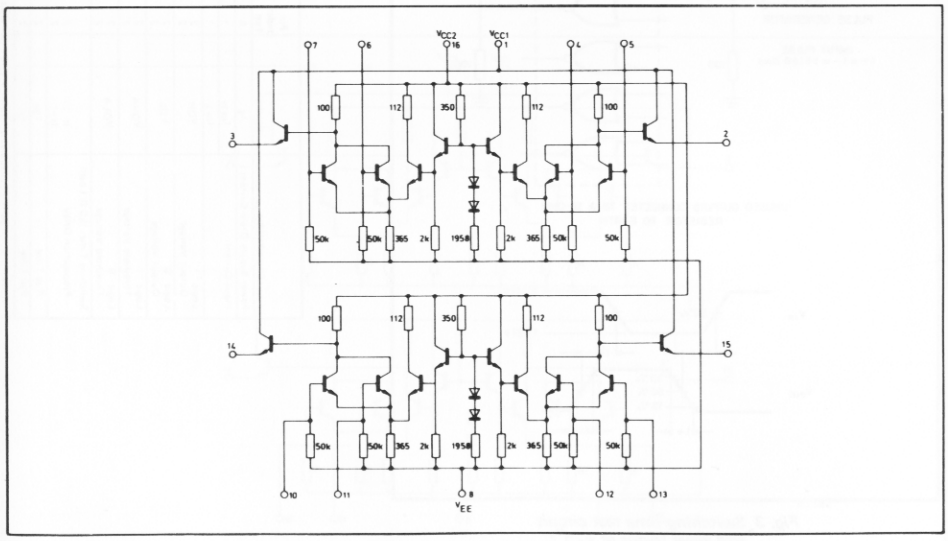

Fig. 2 Circuit diagram

ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equiblirium has been established. The package should be housed in a suitable heat sink or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to −2.0 Vdc.

@ Test Temperature	TEST VOLTAGE VALUES (Volts)					
	V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2	
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2	
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2	

Characteristic	Symbol	Pin Under Test	-30°C Min	-30°C Max	SP1662 Test Limits +25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	Gnd
Power Supply Drain Current	I_E	8	–	–	–	56	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	*	–	–	–	350	–	–	μAdc	*	–	–	–	8	1,16
	I_{inL}	*	–	–	0.5	–	–	–	μAdc	–	*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.045	-0.875	0.960	0.810	-0.890	-0.700	Vdc	–	4	–	–	8	1,16
		2	-1.045	-0.875	0.960	0.810	-0.890	-0.700	Vdc	–	5	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.650	1.850	1.670	-1.830	-1.575	Vdc	4	–	–	–	8	1,16
		2	-1.890	-1.650	1.850	1.620	-1.830	-1.575	Vdc	5	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	–	4	8	1,16
		2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	–	5	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.630	–	-1.605	–	-1.555	Vdc	–	–	4	–	8	1,16
		2	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	5	–	8	1,16
Switching Times (50 Ω Load) Propagation Delay	t_{+-} t_{-+}	2	–	1.6	–	1.5	–	1.7	ns	4	Pulse Out 2	–	–	-3.2 V 8	+2.0 V 1,16
		2	–	1.8	–	1.7	–	1.9	ns	4	2	–	–	8	1,16
Rise Time	t_{2+}	2	–	2.2	–	2.1	–	2.3	ns	4	2	–	–	8	1,16
Fall Time	t_{2-}	2	–	2.2	–	2.1	–	2.3	ns	4	2	–	–	8	1,16

* Individually test each input applying V_{IH} or V_{IL} to input under test

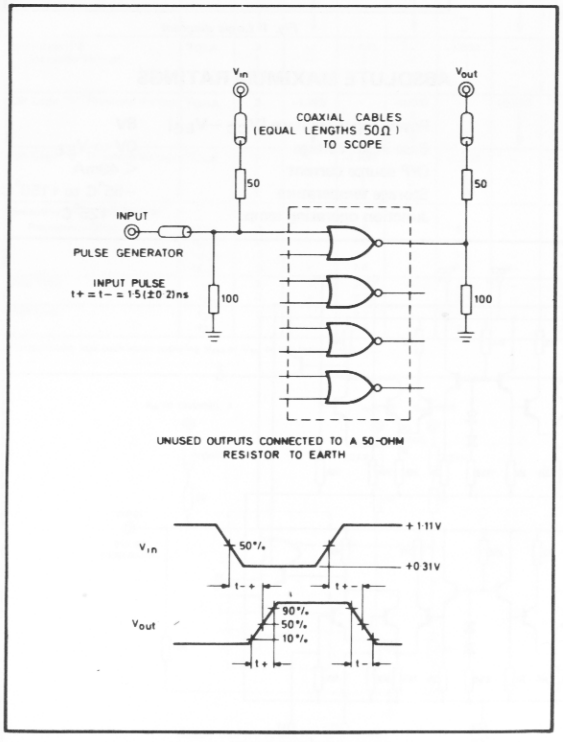

Fig. 3 Switching time test circuit and wave forms at +25°C