AK8811/12

NTSC/PAL Digital Video Encoder

GENERAL DESCRIPTION

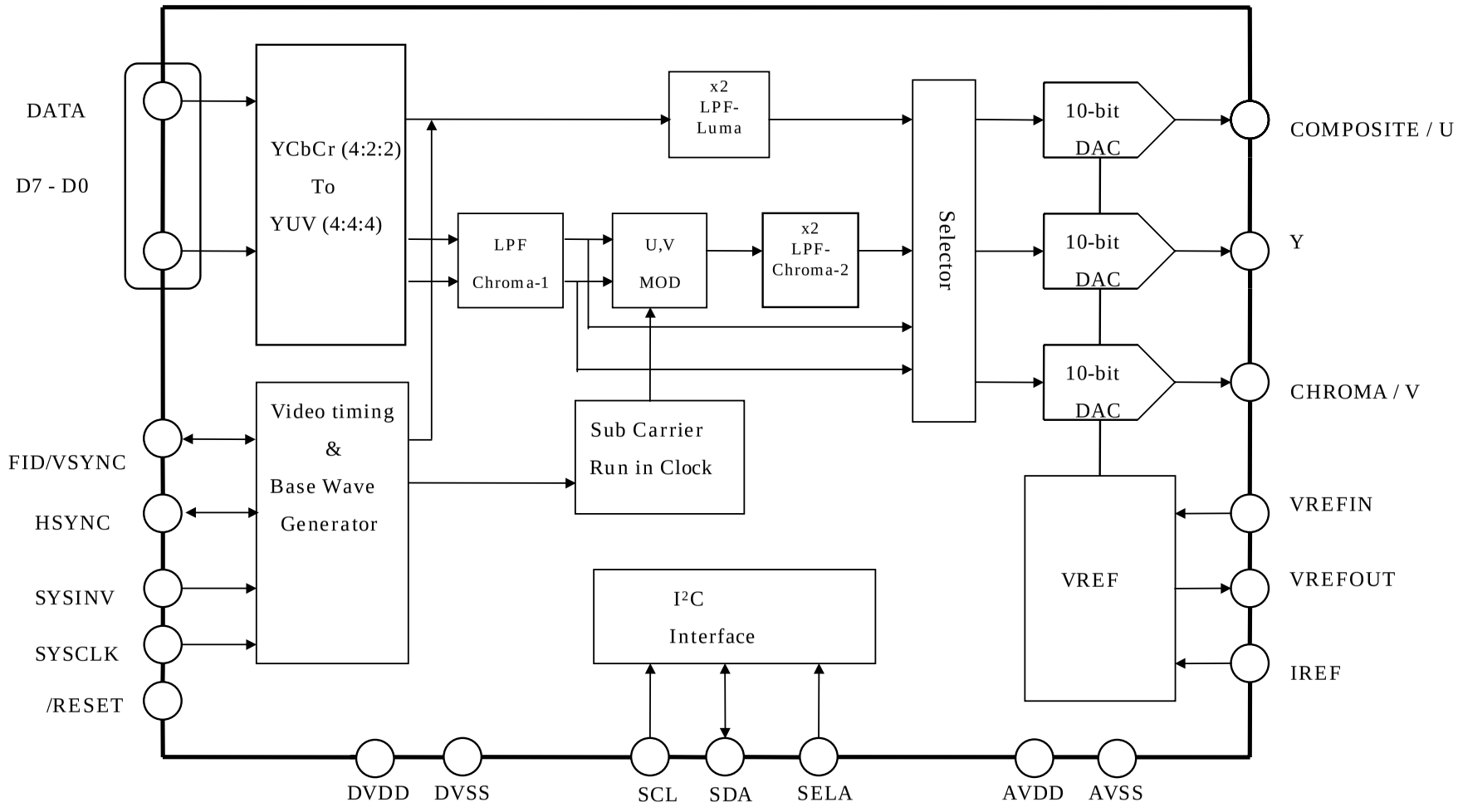
The AK8811 and AK8812 are low voltage, low power and small packaged Digital Video Encoder. They are suitable for a portable DVD or VCD player. They convert ITU-R.BT601/656 standard 8-bit parallel data into analog composite video, S-Video or analog component signals Y/Cb/Cr in NTSC and PAL formats.

AK8812 and AK8811 support Macrovision Copy Protection Rev.7.1(only AK8812), Closed captioning and Video Blanking ID(CGMS). These functions are controlled by high-speed I^2C Bus interface.

FEATURES

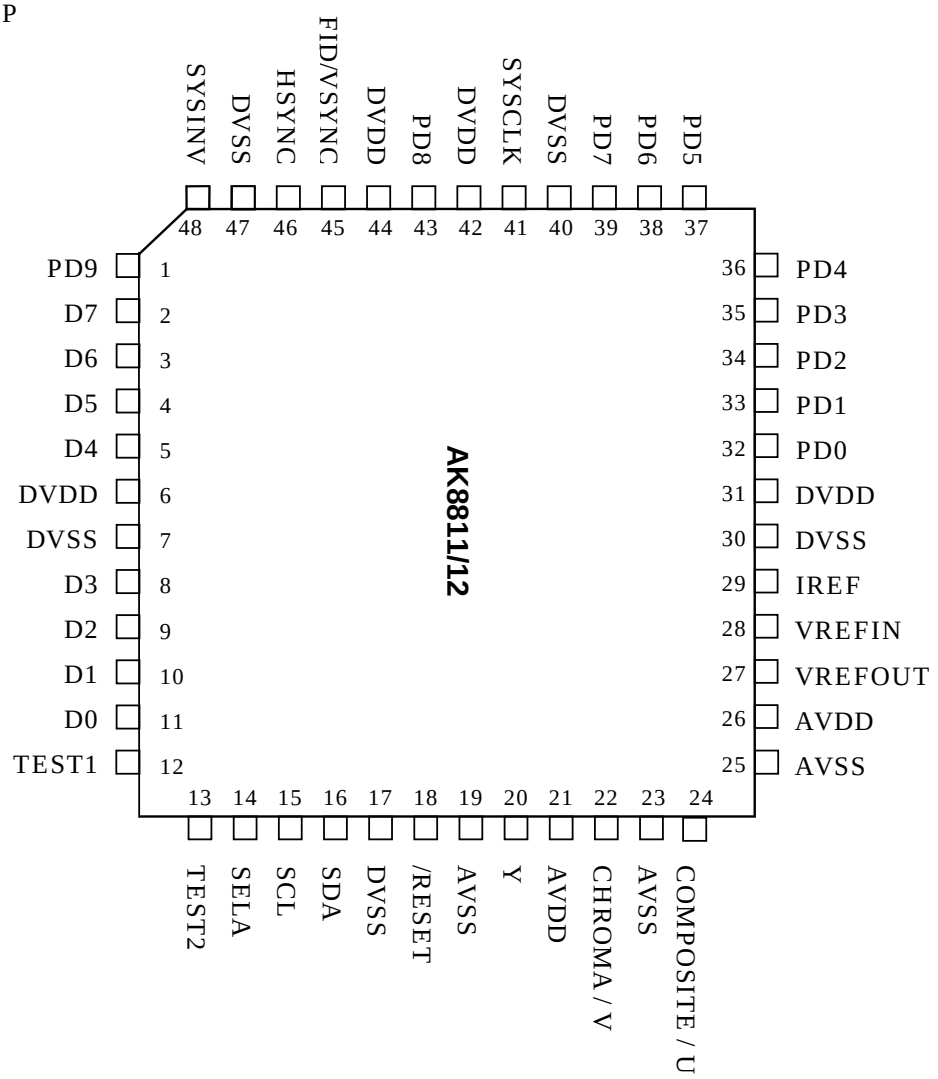
- NTSC-M, PAL-B,D,G,H,I,M,N encoding.
- Simultaneous composite video signal and S-video signal outputs
- Y/Cb/Cr Component output (Based on EIAJ Guideline)
- CCIR-656 4:2:2 8-bit Parallel Input
  - EAV Decoding
- Master/Slave Operation
  - Digital Field Sync I/O
  - Digital Vertical/Horizontal Sync I/O
- Y filtering 2 x over-sampling
- C filtering 4 x over-sampling
- Single 27MHz Clock (The polarity could be inverted by SYSINV pin)
- Triple 10-bit DACs
- I^2C Interface (400kHz)
- Closed Caption encoding (NTSC: line 21,284-SMPTE PAL: line 21,334-CCIR)
- Macrovision Copy Protection Rev. 7.1* (Only for AK8812)
- VBID, CGMS(EIAJ CPR-1024)
- On-chip Color bar generator
- Low Power Consumption
- 3.3V only, CMOS Monolithic
- 48pin LQFP Package

* This device is protected by U.S. patent numbers 4,631,603, 4,577,216, and 4,819,098, and other intellectual rights. The use of Macrovision's copy protection technology in the device must be authorized by Macrovision and is intended for home and other limited pay-per -view use only, unless otherwise authorized in written by Macrovision. Reverse engineering or disassembly is prohibited.



PIN LAYOUT

48pin LQFP



PIN/FUNCTION

No.	Pin Name	I/O	Description
2-5, 8-11	D7 - D0	I	27MHz 8-Bit 4:2:2 multiplexed Y,Cb,Cr Data Input. For Rec.656 format, AK8811/12 decodes EAV. For non-Rec.656 format (without EAV), AK8811/12 operates in Master or Slave mode.
41	SYSCLK	I	27MHz Clock Input. The polarity could be inverted by SYSINV.
48	SYSINV	I	"L " : data is latched with rising edge. "H" : data is latched with falling edge.
18	/RESET	I	After this pin becomes "L", AK8811/12 starts the internal initializing sequence. After initializing sequence, AK8811/12 is set NTSC mode, Rec.656 decoding mode. All DACs Off condition.
45	FID /VSYNC	I/O	Either of FID or VSYNC selected by the register. Rec.656 decode mode :Output Master mode : Output Slave mode : Input FID shows that "L" is odd field and "H" is even field.
46	HSYNC	I/O	Rec.656 decode mode : Output Master mode : Output Slave mode : Input
15	SCL	I	Serial interface clock
16	SDA	I/O	Serial interface data
14	SELA	I	The slave address is set with this pin. "L":40H "H":42H
27	VREFOUT	O	Output of the Internal Vref. Terminate with 0.1uF or more capacitor.
28	VREFIN	I	Input of the Reference Voltage
29	IREF	O	The currents flow this pin adjusts the full-scale output current of the DAC.
24	COMPOSITE/U	O	Output of Composite Video signal or component U
22	CHROMA/V	O	Output of the C signal or component V
20	Y	O	Output of Luminance Signal.
21,26	AVDD	P	Analog +3.3V
6,31, 42,44	DVDD	P	Digital +3.3V
19,23,25	AVSS	G	Analog Ground
7,17,47, 40,30	DVSS	G	Digital Ground
12,13	TEST1 TEST2	I	Test pin. Ground for normal operation
1, 32-39,43	PD[9:0]	I/O	Test pin. Open for normal operation

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (VDD) DVDD, PVDD, AVDD	-0.3	4.6V	V
Input Pin Voltage (Vin)	-0.3	VDD+0.3	V
Input Pin Current (Iin)	-	±10	mA
Analog Reference Current (IREF)	-	0.21	mA
Analog Output Current	-	6.5	mA
Power Dissipation		1000	mW
Storage Temperature	-40	125	°C

(Note)When all Ground pins(DVSS, AVSS) are set to 0V.

Recommended Operating Conditions

Parameter	Min	Typ.	Max	Units
Supply Voltage (VDD)	3.0	3.3	3.6	V
Operating Temperature	-40		85	°C

DC Characteristics

[Power Supply:3.3V Temperature:25°C]

Parameter	Symbol	Min	Max	Units	Conditions
Digital Input High Voltage	VIH1	0.7VDD		V	Note1)
Digital Input Low Voltage	VIL1		0.3VDD	V	Note1)
Digital Input leak Current	IL		±10	uA	Note1)
Digital Output High Voltage	VOH	2.4		V	IOH =-1mA Note 2)
Digital Output Low Voltage	VOL1		0.4	V	IOL = 2mA Note 2)
Digital Maximum Load Capacitance			20	pF	
I^2C Input High Voltage I^2C(SDA,SCL)	VIH2	0.7VDD		V	
I^2C Input Low Voltage I^2C(SDA,SCL)	VIL2		0.3VDD	V	
I^2C(SDA) Output Voltage	VOL2		0.4	V	IOL = 3mA

Note 1) D[9:0],FID/VSYNC, HSYNC, SYSCLK, /RESET pin

Note 2) FID/VSYNC, HSYNC pin

Note) Connected Test Pin to Ground, SELA and SYSINV Pin are desired polarity.

Analog Characteristics and Dissipation Current

[Power Supply:3.3V Temperature:25°C]

Parameter	Min	Typ	Max	Units	Conditions
DAC Resolution		10		bit	
DAC Integral linearity error		±0.6	± 2	LSB	
DAC Differential linearity error		±0.4	± 1	LSB	
DAC Output Full Scale Voltage	1.21	1.28	1.38	V	Note1)
DAC Output offset Voltage			5.0	mV	Note2)
Unbalances between DACs		±1	±5	%	Note3)
Isolation between DACs		50		dB	1MHz Full Scale
DAC Load Capacitance			30	pF	Note4)
Internal Reference Voltage	1.17	1.235	1.33	V	
Internal Reference Drift		50		ppm/°C	
DAC Current (Active mode)		15		mA	Note5)
DAC Current (Sleep mode)		10		uA	Note6)
Total Current		50	72	mA	Note7)

Note 1) Under the condition of output load 390Ω, IREF pin with 12kΩ, using internal reference. The output full-scale current IOUT is calculated as Full scale output voltage (typ. 1.28V) /390Ω=typ. 3.3mA.

Note 2) DAC output when feeding code of 0 (Decimal).

Note 3) Deviation between the DAC output when feeding 1V generating code of 800(Decimal).

Note 4) The value is a design target. This value is not tested.

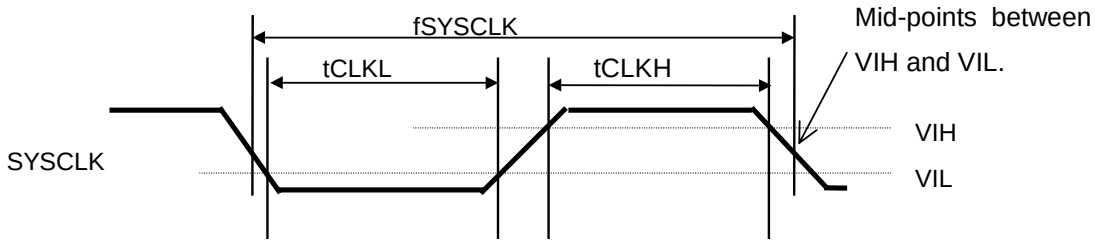
Note 5) All DACs are operating.

Note 6) All DACs are turned off with no system clock.

Note 7) NTSC internal color bar with 3ch DACs operation and slave mode operation. DAC output pins is connected with only 390Ω load.

AC Characteristic

1. SYSCLK



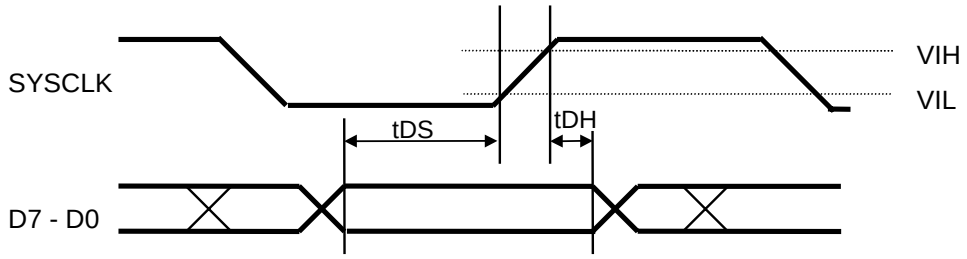
[3.3V Temperature 25°C]

Parameter	Symbol	Min.	Typ.	Max	Unit
SYSCLK	fSYSCLK		27		MHz
SYSCLK Pulse width H	tCLKH	15			nsec
SYSCLK Pulse width L	tCLKL	15			nsec

2. In case of SYSINV = L

(2-1). Pixel Data Input

Pixel Data Input Timing

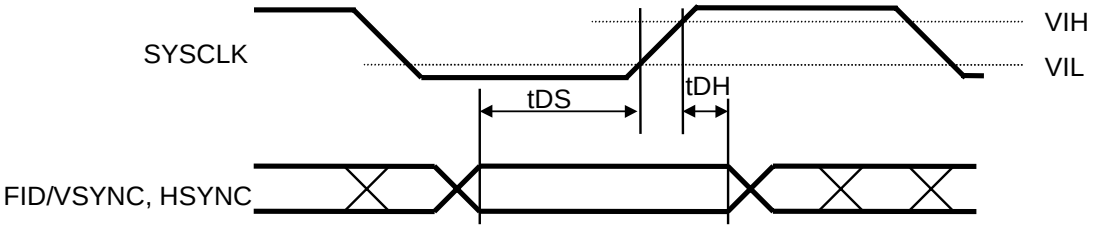


[3.3V Temperature 25°C]

Parameter	Symbol	Min	Typ	Max	Units
Data Setup Time	tDS	5			nsec
Data Hold Time	tDH	8			nsec

(2-2). Synchronizing Signal (FID/VSYNC, HSYNC)

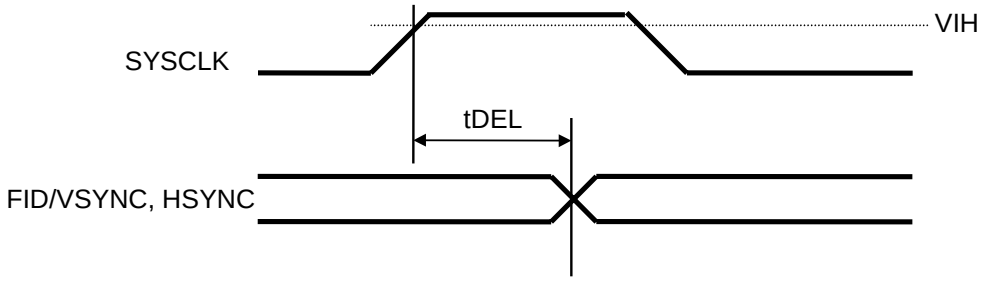
(2-2-1) Input Synchronizing Signal Timing



[3.3V Temperature 25°C]

Parameter	Symbol	Min	Typ.	Max	Units
Data Setup Time	tDS	5			nsec
Data Hold Time	tDH	8			nsec

(2-2-2) Output Synchronizing Signal Timing

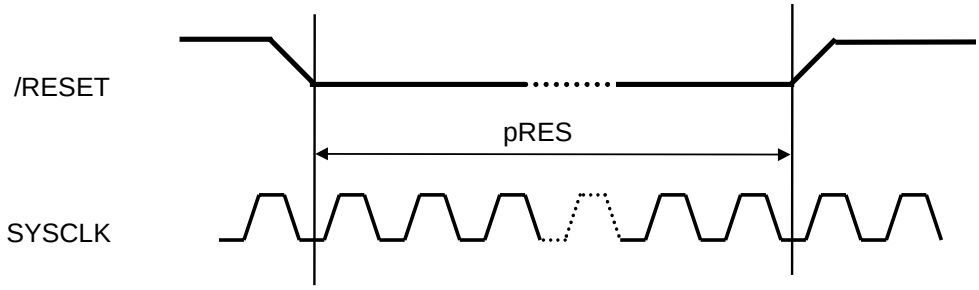


[3.3V Temperature 25°C]

Parameter	Symbol	Min	Typ.	Max	Units
Delay from SYSCLK	tDEL			27	nsec

(2-3). Reset (Initialize)

Reset Timing



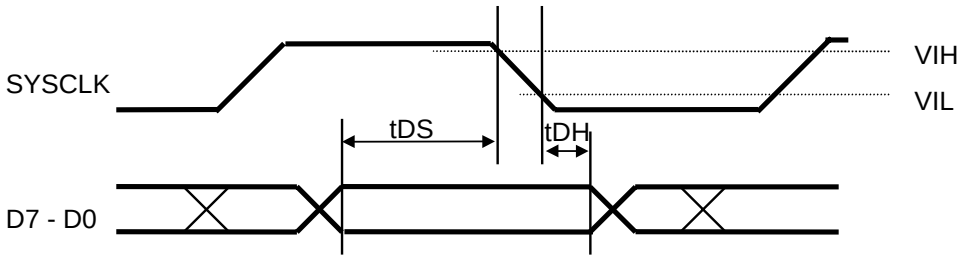
[3.3V Temperature 25°C]

Parameter	Symbol	Min	Typ.	Max	Units
/RESET Pulse Width	pRES	10			SYSCLK

(3). In case of SYSINV = H

(3-1). Pixel Data Input

Pixel Data Input Timing

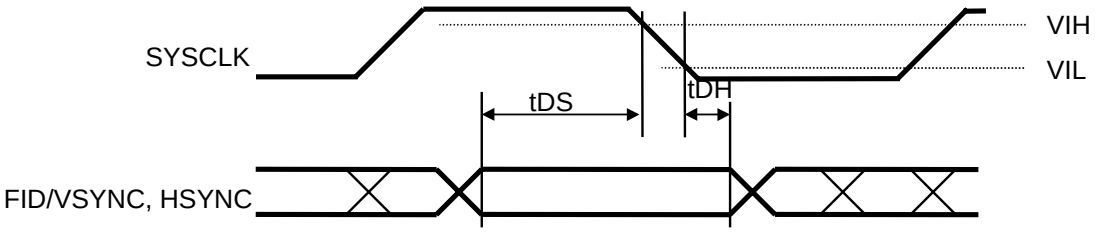


[3.3V Temperature 25°C]

Parameter	Symbol	Min	Typ	Max	Units
Data Setup Time	tDS	5			nsec
Data Hold Time	tDH	8			nsec

(3-2). Synchronizing Signal (FID/VSYNC, HSYNC)

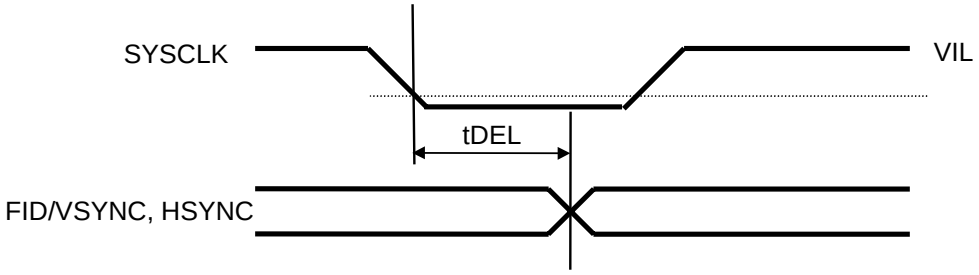
(3-2-1) Input Synchronizing Signal Timing



[3.3V Temperature 25°C]

Parameter	Symbol	Min	Typ.	Max	Units
Data Setup Time	tDS	5			nsec
Data Hold Time	tDH	8			nsec

(3-2-2) Output Synchronizing Signal Timing

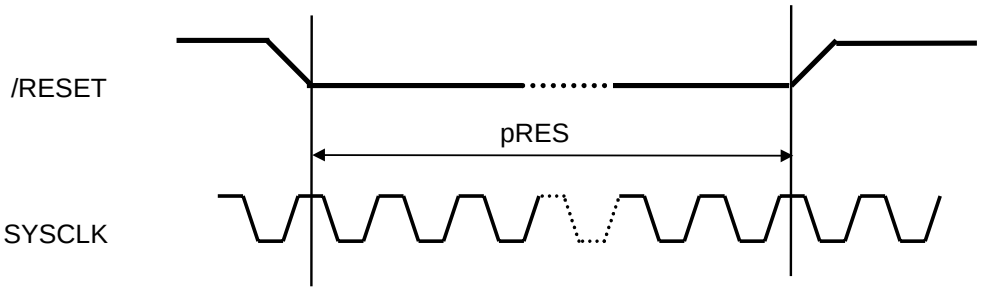


[3.3V Temperature 25°C]

Parameter	Symbol	Min	Typ.	Max	Units
Delay from SYSCLK	tDEL			27	nsec

(3-3). Reset (Initialize)

Reset Timing

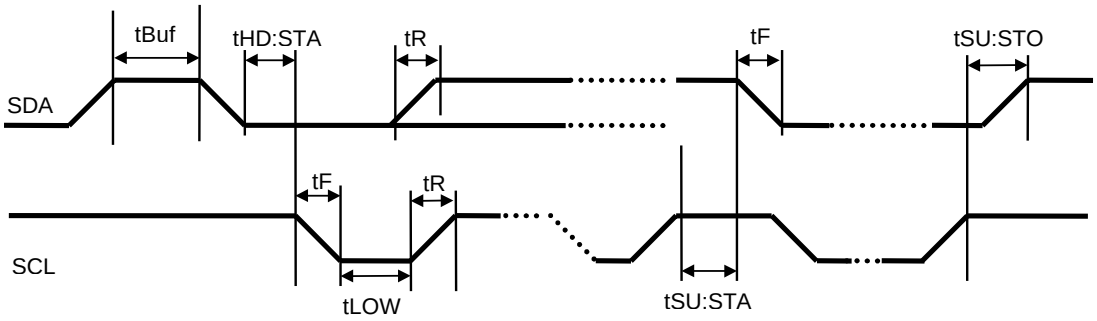


[3.3V Temperature 25°C]

Parameter	Symbol	Min	Typ.	Max	Units
/RESET Pulse Width	pRES	10			SYSCLK

(4). I^{2}C Bus (SCL 400kHz cycle mode)

(4-1) I/O Timing 1

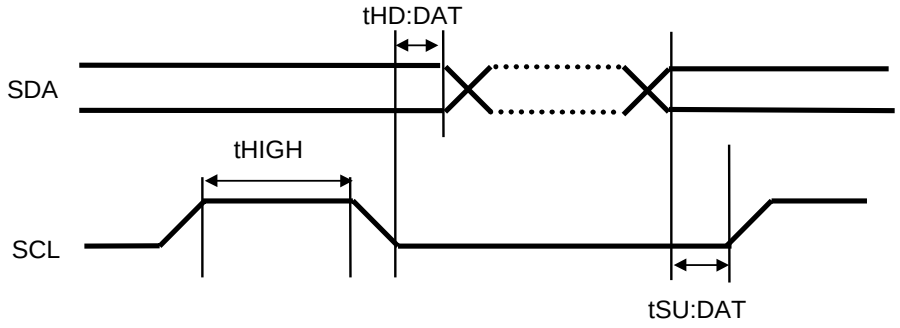


[3.3V Temperature 25°C]

Parameter	Symbol	Min	Max	Units
Bus Free Time	tBUF	1.3		usec
Hold Time (Start Condition)	tHD:STA	0.6		usec
Clock Pulse Low Time	tLOW	1.3		usec
Bus Signal Rise Time	tR		300	nsec
Bus Signal Fall Time	tF		300	nsec
Setup Time(Start Condition)	tSU:STA	0.6		usec
Setup Time(Stop Condition)	tSU:STO	0.6		usec

All the figures shown above list are not restricted by AK8811/12 but are restricted by I^{2}C Bus standard.
Please see the I^{2}C Bus standard for further details.

(4-2) I/O Timing 2



[3.3V Temperature 25°C]

Parameter	Symbol	Min.	Max.	Unit.
Data Setup Time	tSU:DAT	100 (1)		nsec
Data Hold Time	tHD:DAT	0.0	0.9 (2)	usec
Clock Pulse High Time	tHIGH	0.6		usec

(1) In case of normal I^{2}C bus mode tSU:DAT ≥250nsec
(2) Using under minimum tLOW, this value must be satisfied.

FUNCTIONAL DESCRIPTION

♦ Reset

When the reset pin [/RESET] set to “L”, AK8811/12 is in reset state. AK8811/12 starts in the internal initializing sequence at the trailing edge of the first SYSCLK after the reset pin is “L”. All internal registers are set to be default value by this initializing sequence. AK8811/12 needs at least 10 clock counts of SYSCLK for this reset operation. After the reset operation, the video output pins are in high-impedance. AK8811/12 requires SYSCLK for the reset operation.

♦ Master-Clock

AK8811/12 requires 27MHz clock at SYSCLK pin for operation. Video input data (ITU-R BT.656) is sampled at the trailing edge of this 27MHz. SYSINV decides the edge direction.

SYSINV = L Data is sampled at rising edge of SYSCLK.
SYSINV = H Data is sampled at falling edge of SYSCLK.

♦ Video Signal Interface

AK8811/12 can interface with the video input data by the following 3 modes. The mode is set by the register [Interface mode register(00H)].

1. ITU-R BT.656 Format

AK8811/12 decodes EAV in stream data and manages an internal synchronization.
In this case, AK8811/12 outputs FID (odd : “L” even : “H”)/ VSYNC and HSYNC.
CCIR-bit of [Interface mode register (00H)] should be set “1” .

2. ITU-R BT.656 like Format (4:2:2 Y/Cb/Cr)

There are Master and Slave modes, for ITU-R BT.656 like Format which does not include EAV. In this mode, CCIR-bit of [Interface mode register(00H)] should be set “0” .

<Master Mode>

AK8811/12 provides FID/VSYNC and HSYNC to an external device according to the AK8811/12 internal timing counter. AK8811/12 starts to sample the input data at the fixed value on the internal pixel counter.
In this mode, following setting should be done to [Interface mode register(00H)].
CCIR-bit = 0
MAS-bit = 1

<Slave Mode>

FID/VSYNC and HSYNC are supplied by an external device. AK8811/12 samples the data as same manner of Master mode.
In this mode, following setting should be done to [Interface mode register(00H)].
CCIR-bit = 0
MAS-bit = 0

♦ Video Signal Conversion

Video reconstruction module converts the multiplexed data (ITU-R. BT601 Y/Cb/Cr) to the interlace format of NTSC-M, PAL-M, PAL-B,D,G,H,I,N and other formats (ex. NTSC-4.43 and PAL60). The video reconstruction format, the line number, the color encode way(NTSC or PAL) and the frequency of Color Sub-carrier is specified by [Video Process 1 register(01H)]. (cf. Burst Signal Table) The frequency and the phase of Color Sub-carrier are also adjustable by [Sub C. Freq. register(06H)] and [Sub C. Phase register(07H)]. The Sub-carrier has a free-running mode and a reset-mode. In the reset-mode, the Sub-carrier is reset automatically to the initial phase for every 4 fields (NTSC) or 8 fields (PAL).

♦ Component Video Output

Video output mode is set by VS-bit of [Video Process 3 register (03H)].
AK8811/12 can output not only the set of composite video signal and S-video signal but also can output component video signals(Y/Cb/Cr). The component video signals are complied with EIAJ guideline 1998/3.

VS-bit = 0 : composite video signal and S-video signal output
VS-bit = 1 : component video signal output

♦ Luminance Filter

Luminance signal passes through the 2x Low Pass filter Fig.1 is the characteristic of Luminance Filter.

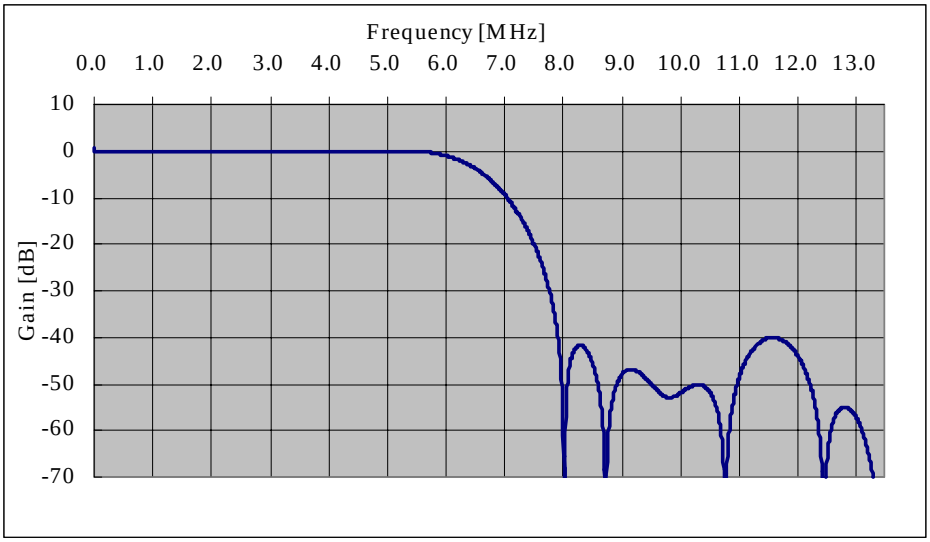


Fig. 1 Luminance Filter

♦ Chroma Filter

Chroma signals (Cb,Cr) before Sub-carrier modulation pass through the 1.3 MHz Low pass filter shown in Fig.2. Chroma signal modulated by Sub-carrier passes through the filter shown in Fig.3.

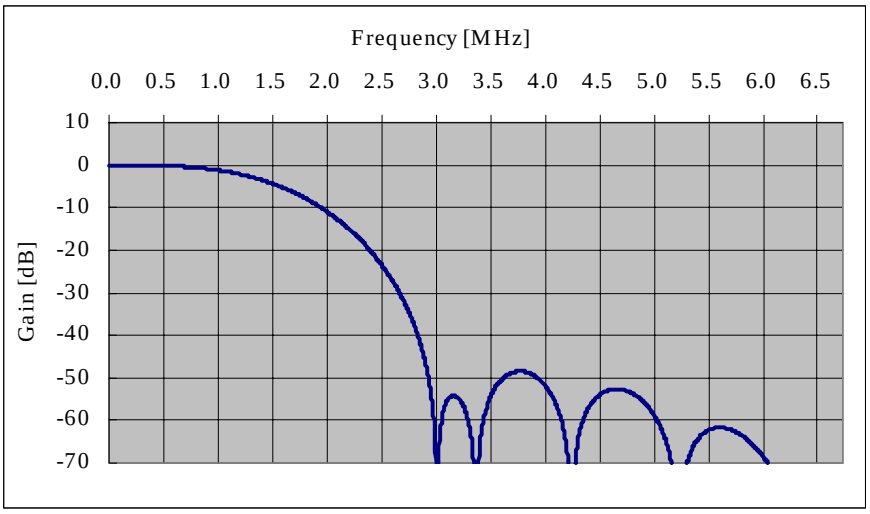


Fig. 2 Chroma-1 LPF

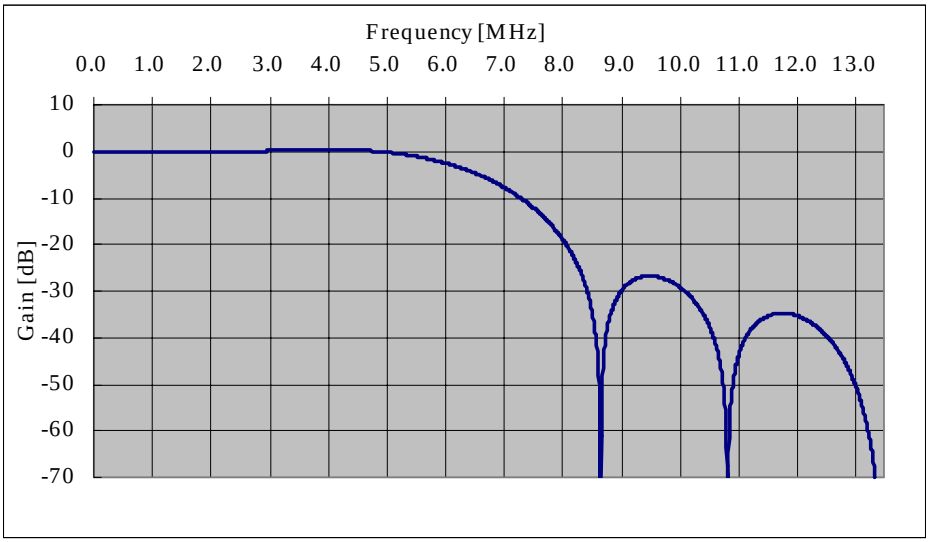


Fig. 3 Chroma-2 LPF

♦ Color burst signal

Color burst signal is generated by 24bits-length Digital Frequency Synthesizer. The Default frequency of the color burst is selected by [Video Process 1 Register(0x01)].

Standard	Sub-carrier Freq. [MHz]	Video Process 1 [VM1,VM0]
NTSC-M	3.57954545	[0,0]
PAL-M	3.57561188	[0,1]
PAL-B,D,G,H,I	4.43361875	[1,1]
PAL-N(Arg.)	3.5820558	[1,0]
PAL-N(non-Arg.)	4.43361875	[1,1]
PAL60	4.43361875	[1,1]
NTSC-4.43	4.43361875	[1,1]

Burst Signal Table

Sub-carrier frequency 3.57561188MHz is allowed when PAL-M mode is selected.

The burst frequency and initial phase resolution are as follows.

Frequency resolution	0.8046Hz
SCH Phase resolution	360°/256

♦ Video DAC

AK8811/12 has the three current driven 10bits-DACs at 27MHz operation. The full scale voltage of DAC is determined by the current output from IREF pin. Typical output voltage is 1.28Vo-p under the condition of VREFIN 1.235V, 12KΩ between IREF pin and Ground(AVSS) and DAC load resistance of 390Ω. This full-scale voltage should be set in the range of 1.17V to 1.33V by adjusting the resistor which terminates IREF pin. Each DAC output can be set to “active state” or to “inactive state” individually by [DAC Mode register(05H)]. When DAC is in “inactive state”, the output is Hi-impedance. When all DACs are set to “inactive state”, the analog part of AK8811/12 goes into sleep mode. In this case AK8811/12 stops outputing the reference voltage(VREF) output. When any DAC is switched over in “active state” from sleep mode, AK8811/12 starts outputing reference voltage. In this case AK8811/12 needs several milisecond for VREF wake-up time.

Using internal VREF as the reference voltage, connect [VREF OUT] pin with [VREF IN] pin and [VREF OUT] pin is terminated with more than 0.1uF capacitor.

♦ Use external Reference Voltage

In order to improve the accuracy of DAC output, external reference voltage may be used. In this case, VREFOUT pin still needs to be terminated with more than 0.1uF capacitor.

♦ Copy Protection

Macrovision Copy Protection Rev.7.1

Information about the Macrovision encoding functions of the AK8812 is available to Macrovision licensees. Macrovision may be contacted at:

Macrovision Corporation
1341 Orleans Drive
Sunnyvale, California 94089
USA

Attention: ACP-PPV Technical Support
FAX: (408) 743 – 8610

♦ Closed Caption and Extended Data

AK8811/12 supports both Closed Captioning and Extended Data. They are controlled “ON” or ”OFF” respectively by [Video Process 2 Register(02H)]. Each data consists of 2 continuous bytes register(Closed Caption R (16H,17H)), and it is recognized as the data is renewed when the second byte(17H register) is written in the register. After the data is renewed, AK8811/12 encodes Closed Captioning and Extended Data at the designated line. If the data isn't renewed, AK8811/12 outputs “ASCII-NULL” code. The data is supposed as Odd Parity and 7 bit US-ASCII code. Host should provide a parity bit.

*In PAL encoding mode, AK8811/12 outputs them at the same timing and same pattern as NTSC.

*The line where Closed Captioning data is encoded is as follows.

	525/60 System (SMPTE)	625/50 System (CCIR)
Closed Caption	21 Line default	21 Line default
Extended Data	284 Line default	334 Line default

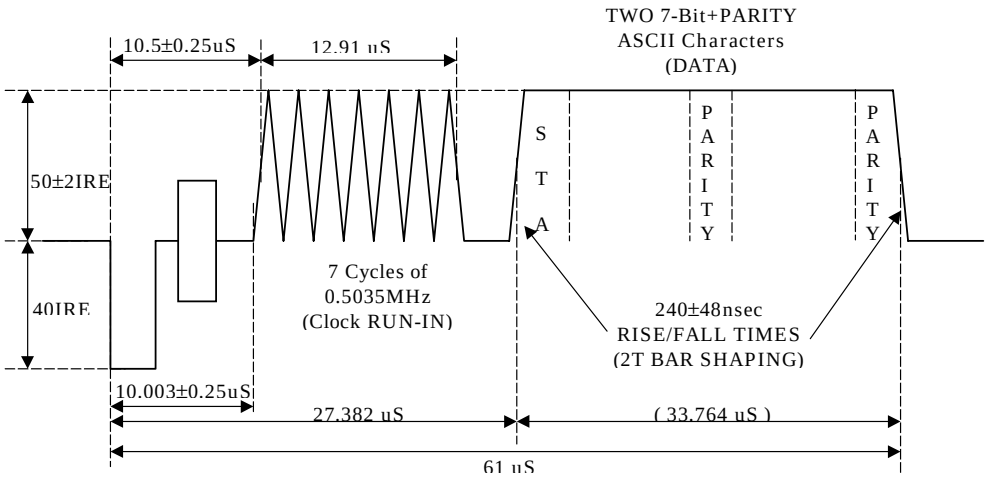


Fig. 4 Closed Captioning Wave form

♦ Video ID

AK8811/12 supports Video ID (EIAJ standard, CPR-1204) encoding for the distinction of an aspect ratio, etc. Setting or Resetting the VBID-bit of [Video Process 2 Register(02H)], this function is switched On/Off. The data is set by using [Video ID Data Register(1AH, 1BH)].

VBID Data Renewal Timing.

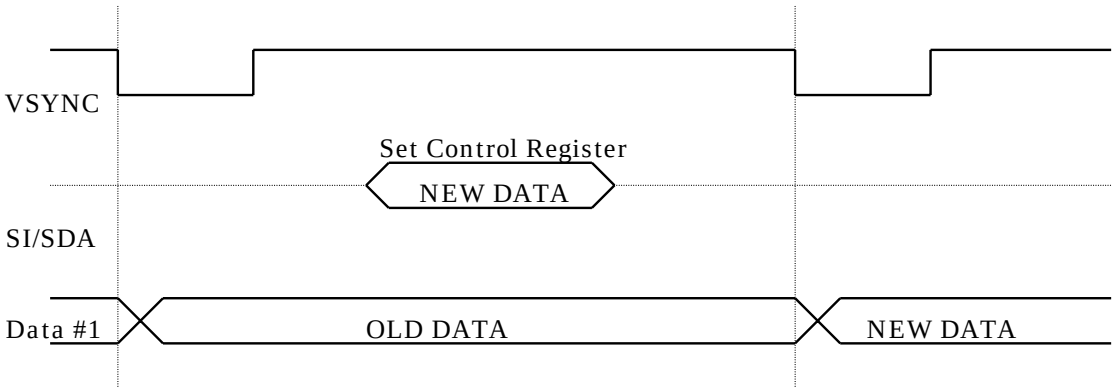


Fig. 5 VBID Data renewal Timing

VBID Data Layout

VBID is consists of 20 bits and its format is shown as follows.

AK8811/12 generates CRC code automatically and appends it to the data. Initial value of the Polynomial is 1.

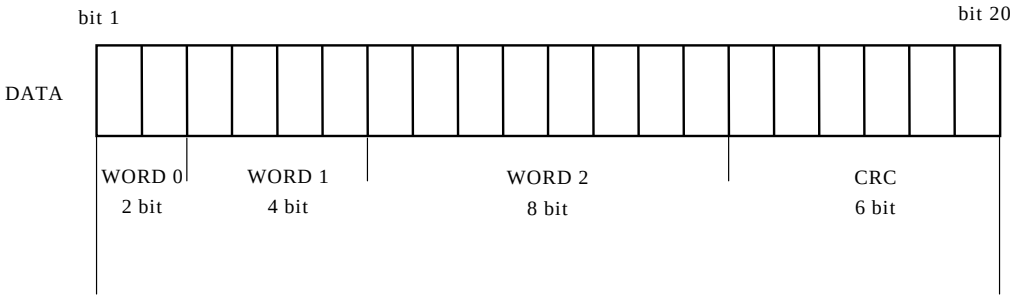


Fig. 6 VBID code assignment

VBID Waveform

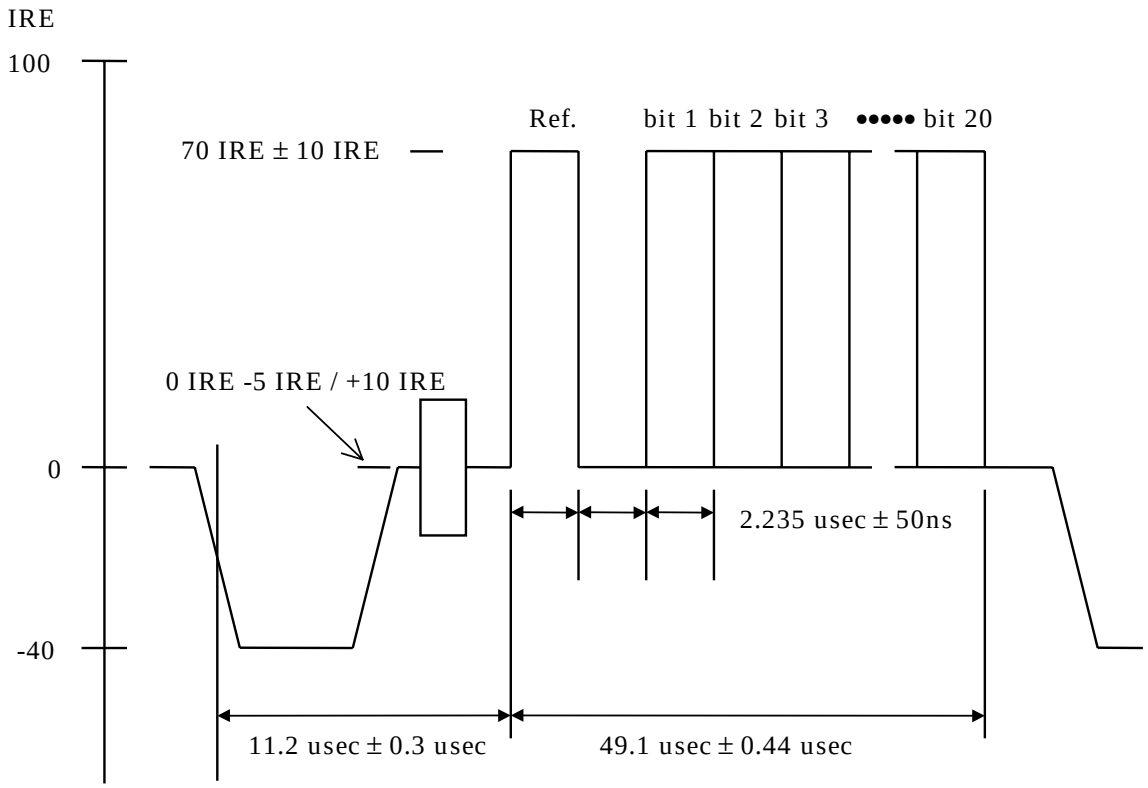


Fig. 7 VBID Wave Form

	525/60 system	625/50 system
Amplitude	70 IRE	490 mV
Encode Line	20/283	20/333

VBID parameter table

♦ AK8811/12 Interface Timing (Part 1) Master mode & ITU-R BT. 656 mode

On ITU-R BT.656 decoding mode or master mode operation, AK8811/12 outputs HSYNC and FID or VSYNC (selected by register).

When AK8811/12 receives ITU-R BT. 656 signal, AK8811/12 decodes [EAV] code in the data for synchronization then outputs the HSYNC. AK8811/12 outputs HSYNC at the rising edge of SYSCLK in the timing of the 32nd/24th(NTSC/PAL) data slot, which is counted from the [EAV] starting point as below. (See also AC Characteristics 2-2[Input Synchronizing Signal])

On master mode operation, the front device connected with AK8811/12 (ex. MPEG Decoder) starts to set Cb on the 276th/288th(NTSC/PAL) slot, after starting to count HSYNC falling edge as 32nd/24th(NTSC/PAL) slot.

FID/VSYNC is output synchronously with HSYNC at the timing of solid line as in Fig. 10 Video Field.

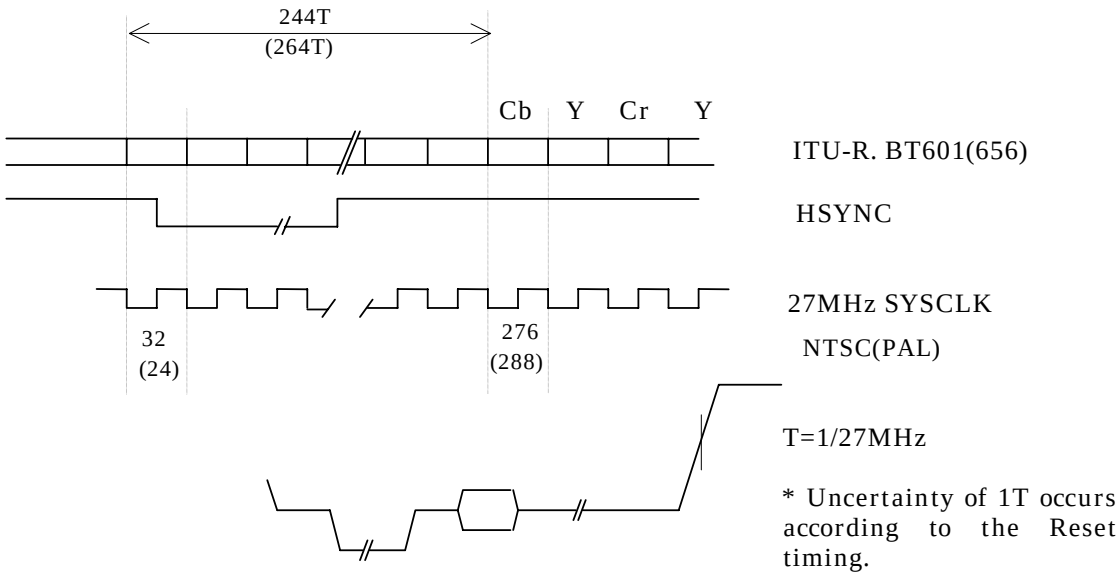


Fig. 8 Interface Timing (ITU-R BT.656 or Master mode)

♦ AK8811/12 Interface Timing (Part 2) Slave mode

On slave mode operation, HSYNC and FID or VSYNC (Selected by register) are input to AK8811/12.

AK8811/12 monitors the transition of HSYNC at the timing of the rising edge of SYSCLK. (Refer to AC Characteristic 2-1. [Input Synchronizing Signal]) After AK8811/12 recognizes HSYNC is Low-logic, AK8811/12 sets the slot number to the 32nd/24th(NTSC/PAL), internally, then AK8811/12 starts to sample the data as Cb on 276th/288th(NTSC/PAL) slot.

Video field is recognized the transition timing between FID/VSYNC and HSYNC. (Fig.10. Video Field) As in the figure, there is a toreralnce of ±1/4H.

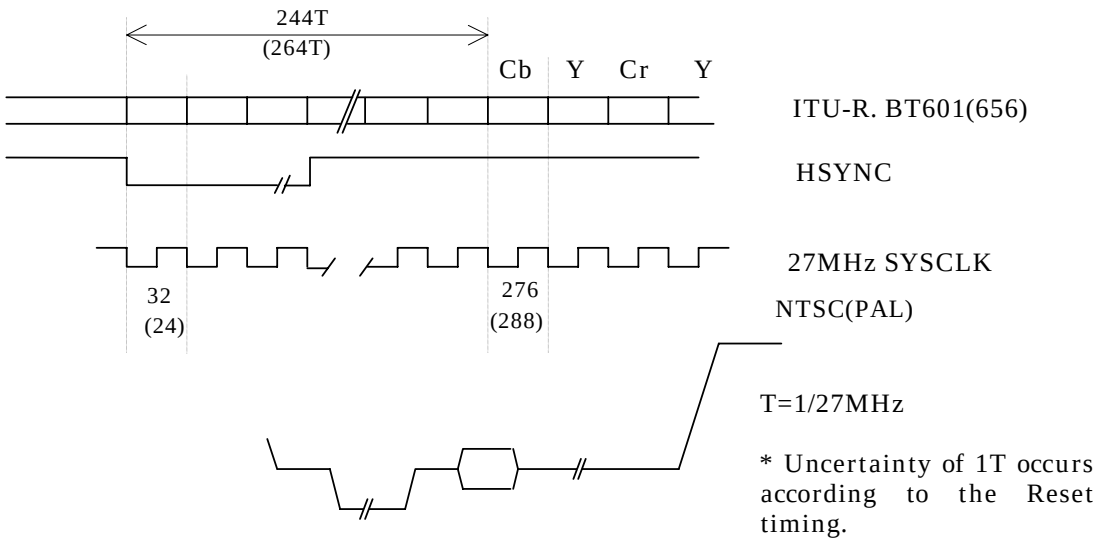


Fig. 9. Interfacing timing (Slave mode)

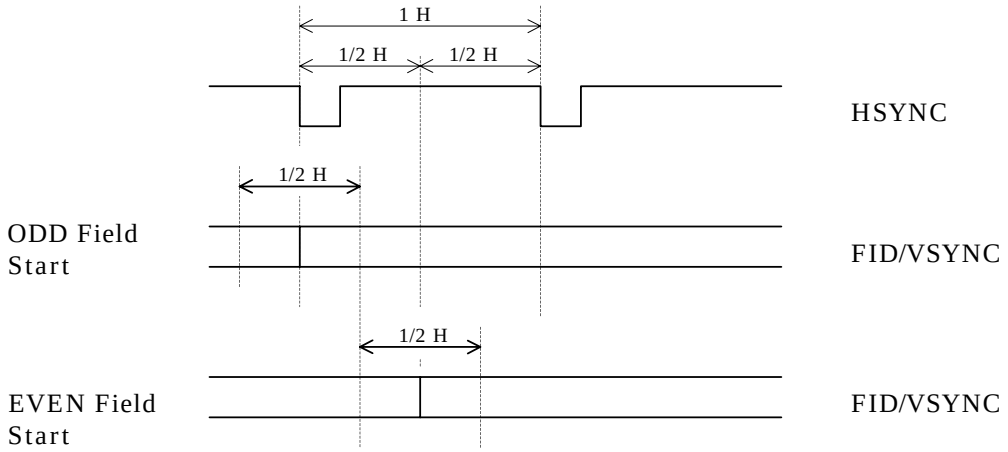


Fig. 10. Video Field

♦ HSYNC FID/VSYNC Timing

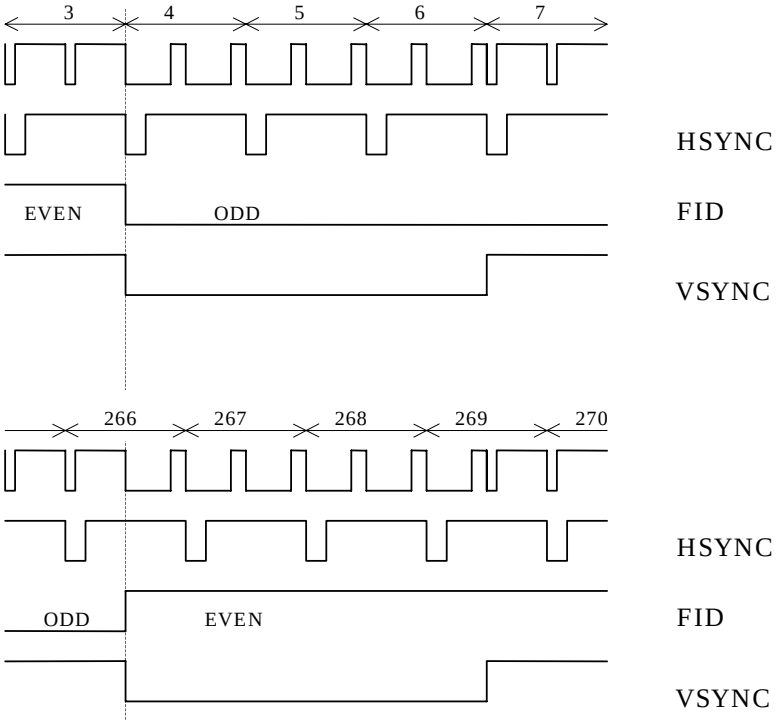


Fig. 11. NTSC / PAL/M

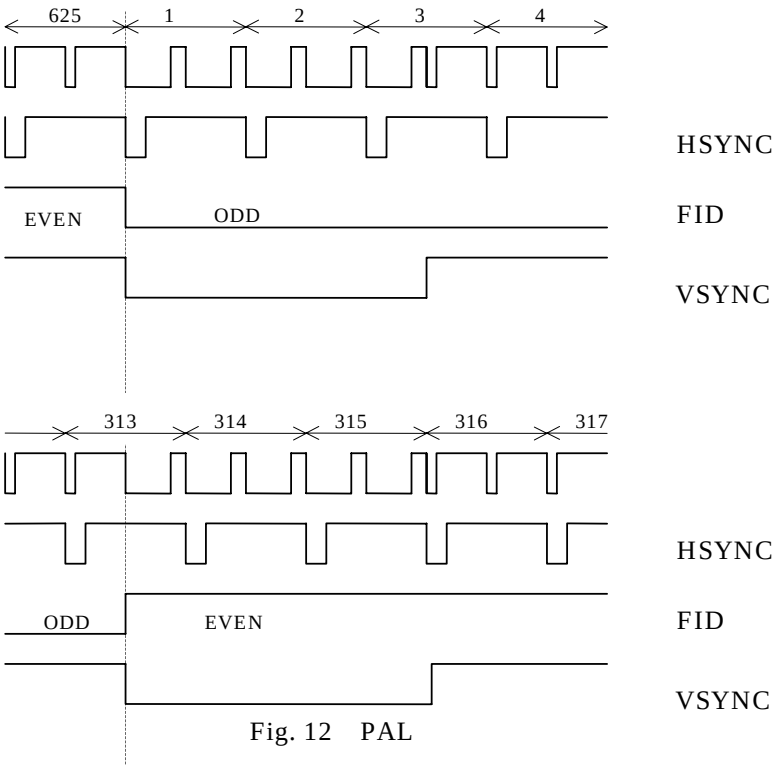
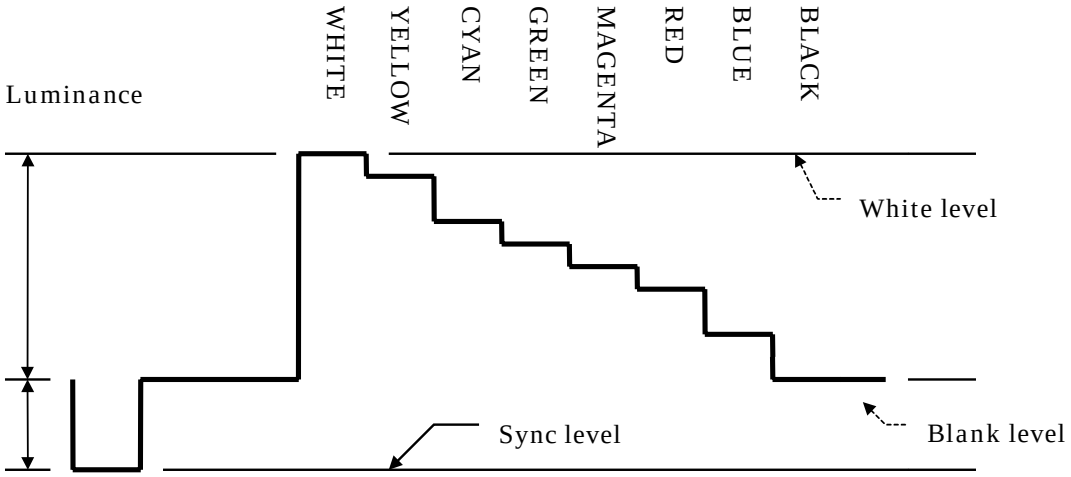
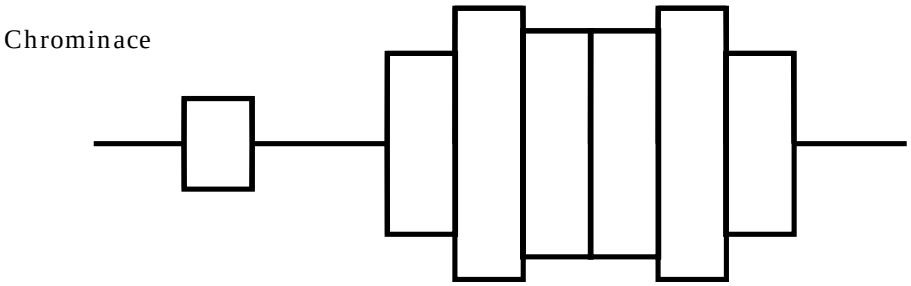


Fig. 12 PAL

♦ Color Bars

AK8811/12 generates the Common Color Bar signal for NTSC and PAL internally. The generated Color Bar is "100% Amplitude, 100% Saturation".





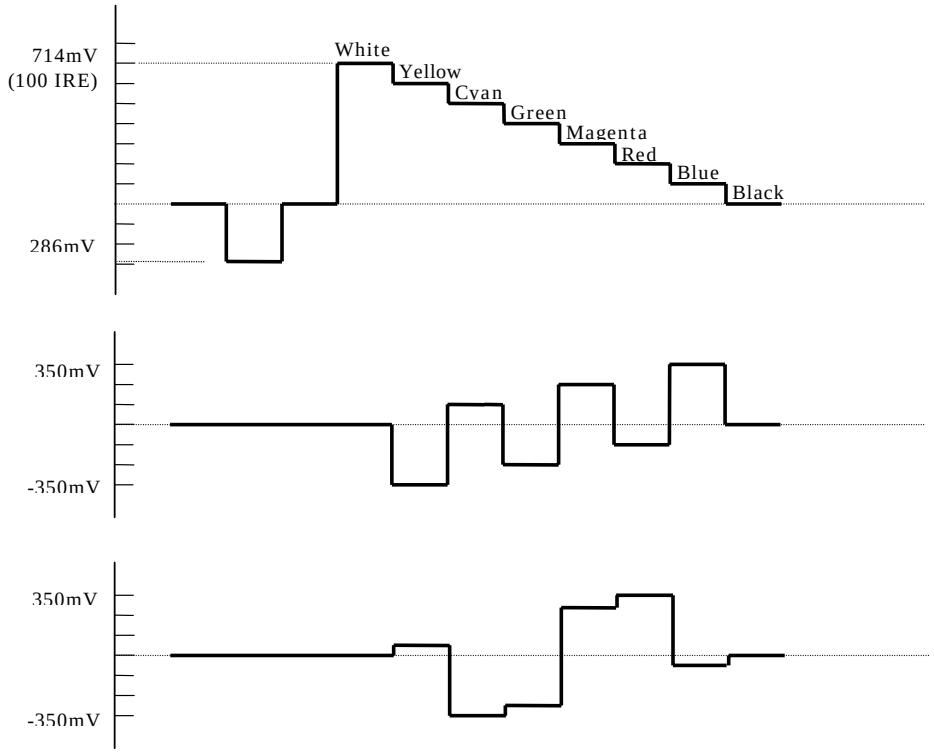
The following values are code for ITU-R. BT601

	WHITE	YELLOW	CYAN	GREEN	MAGENTA	RED	BLUE	BLACK
Cb	128	16	166	54	202	90	240	128
Y	235	210	170	145	106	81	41	16
Cr	128	146	16	34	222	240	110	128

♦ Component video output

The levels of each Component video outputs are following. (Color bar NTSC 100/0/100/0)

Magnitude is compliant to the guideline of EIAJ CPR-1024.



[mV]

	WHITE	YELLOW	CYAN	GREEN	MAGENTA	RED	BLUE	BLACK
Cb	0	-350	118	-232	232	-118	350	0
Y	714	632	500	418	296	213	82	0
Cr	0	57	-350	-293	293	350	-57	0

Y Signal Level : 1.00Vpp

Y (Video Signal Level) : 0.714V

Y (Sync level) : 0.286V

Setup : None

Cb/Cr Signal Level : ± 0.350V

♦ I²C Control Sequence

AK8811/12 is controlled by I²C bus. The slave address can be selected as 40H or 42H by selecting SELA pin.

SELA pull-down	40H
Pull-up	42H

Operation :

Write Sequence:

S	Slave Address	W	A	Sub Address	A	Data_1	A	.....	Data_n	A/$\overline{A}$	Stp

*Continuous data writing is capable for the all registers.

Sequential Read: (Only Sub Address of 24H, 25H, 26H could be read)

S	Slave	W	A	*Sub Address* 24H	A	rS	Slave	R	A				
										DATA_24H	A	DATA_25H	A	DATA_26H	$\overline{A}$	Stp

S : Start Condition

A : Acknowledge(SDA LOW)

$\overline{A}$: Not Acknowledge(SDA HIGH)

Stp : Stop Condition

R/W: 1: Read

0:Write

by Host

by AK8811/12

- It ignores the general call

AK8811/12 REGISTER MAP

Sub Address	Name	R/W	Explanation
00H	Interface Mode	W	Setting Interface mode
01H	Video Process 1	W	Setting Standard (NTSC, PAL etc.)
02H	Video Process 2	W	Setting Closed Caption/Extended Data/VBID
03H	Video Process 3	W	Setting Composite signal or Component Signal Adjusting chroma/Luma Delay
04H	RESERVED		
05H	DAC Mode	W	Each DAC On/Off Switch
06H	Sub C. Freq.	W	Adjusting Sub-carrier frequency
07H	Sub C. Phase	W	Adjusting Sub-carrier phase
08H-15H	RESERVED		
16H	Closed Caption R	W	Closed Caption Lower byte Data
17H	Closed Caption R	W	Closed Caption Upper byte Data
18H	Closed Caption R	W	Extended Lower byte Data
19H	Closed Caption R	W	Extended Upper byte Data
1AH	Video ID Data	W	Video ID Lower byte Data
1BH	Video ID Data	W	Video ID Upper byte Data
1CH-23H	RESERVED		
24H	STS Data	R	Status
25H	Device ID	R	Device ID
26H	Device REV	R	Revision
27H-29H	RESERVED		

Interface Mode Register (W only default A4H)

Sub Add	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
00H	BLN4	BLN3	BLN2	BLN1	BLN0	FID	MAS	CCIR

Symbol	Value	Description	
BLN4 - BLN0	*****	Line Blanking No.	default 10100
FID	0 1	Select VSYNC Select FID	 default
MAS	0 1	Slave mode Master mode When CCIR=0,it's valid	default
CCIR	0 1	CCIR656 non-decode CCIR656 decode	default

Video Process 1 Register (W only default 18H)

Sub Add	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
01H	Reserved	CBG	SETUP	SCR	VM3	VM2	VM1	VM0

Symbol	Value	Description	
CBG	0 1	Video Encode Generates color bar	default
SETUP	0 1	No Set-up 7.5 IRE Set-up	 default
SCR	0 1	Sub C. Phase Reset off Standard Field Reset	 default
VM3 – VM2	00 01 10 11	525/60 525/60 PAL (PAL-M etc.) Reserved PAL	default
VM1-VM0	00 01 10 11	3.57954545 MHz 3.57561188 MHz (PAL-M only) 3.5820558 MHz 4.43361875 MHz	default

Register Setting of each standard is showend as following ;

	VM3-VM0
NTSC-M	0000
PAL-B,D,G,H,I	1111
PAL-M	0101
PAL-60	0111
NTSC4.43	0011

- When SCR is "ON", the Subcarrier Phase is reset every 4 fields for NTSC, every 8 fields for PAL.
- Even when SETUP is "ON", there is no Set-up (Pedestal) during the blanking lines.

Video Process 2 Register (W only default 00H)

Sub Add	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
02H	Reserved	Reserved	Reserved	Reserved	Reserved	CC284	CC21	VBID

Symbol	Value	Description	
CC284	0 1	Extended Data OFF ON	default
CC21	0 1	Closed Caption OFF ON	default
VBID	0 1	Video ID OFF ON	default

Video Process 3 Register (W only default 00H)

Sub Add	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
03H	Reserved	VS	SYD2	SYD1	SYD0	CYD2	CYD1	CYD0

Symbol	Value	Description	
Video Set	0 1	Composite, S-Video set Component set	default
SYD2 - SYD0		S-Video Y Component delay no. from Chroma: 2's comp.	default 000
CYD2 - CYD0		Composite Y Component delay no. from Chroma: 2's comp.	default 000

- VS-bit selects the one of the setting of signals from the 2 signal sets (Composite, Y /C or Y/Cb/Cr)
- S video and Y component of the composite signal can be shifted for the chroma signal independently at ±3-system clock (27MHz).

DAC Mode Register (W only default 00H)

Sub Add	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
05H	Reserved	Reserved	Reserved	Reserved	Reserved	OUTCP	OUTC	OUTY

Symbol	Value	Description	
OUTCP	0 1	Composite video signal or U signal output : OFF Composite video singal or U signal output : ON	default
OUTC	0 1	Chroma signal or V signal output : OFF Chroma signal or V signal output : ON	default
OUTY	0 1	Y signal output : OFF Y signal output : ON	default

- Video output of AK8811/12 (DAC) can be forced “OFF” independently.

  The output of DAC that is forced “OFF” is Hi-impedance. When three DACs are forced “OFF”, then the internal VREF is also forced “OFF”. In this case, it takes several miliseconds before the internal VREF reaches the proper voltage after any DAC becomes “ON”.

SubC Freq. Register (W only default 00H)

Sub Add	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
06H	SUBF7	SUBF6	SUBF5	SUBF4	SUBF3	SUBF2	SUBF1	SUBF0

Symbol	Value	Description	
SUBF7-SUBF0		Adjustment of frequency between +127 and –128 step of 0.8Hz	default 0

- AK8811/12 generates the necessary sub-carrier frequency from a system clock by DFS (Digital Frequency Synthesizer)
- Frequency of default is adjustable by specifying this bit. This bit adjusts the default frequency.

SubC Phase Register (W only default 00H)

Sub Add	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
07H	SUBP7	SUBP6	SUBP5	SUBP4	SUBP3	SUBP2	SUBP1	SUBP0

Symbol	Value	description	
SUBP7 – SUBP0		Step: (360° /256°)	default 0

- Sub- carrier phase is adjustable by (360° /256) step.

Closed Caption Register (W only default 00H)

Sub Add	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
16H	CC1[7]	CC1[6]	CC1[5]	CC1[4]	CC1[3]	CC1[2]	CC1[1]	CC1[0]
17H	CC2[7]	CC2[6]	CC2[5]	CC2[4]	CC2[3]	CC2[2]	CC2[1]	CC2[0]
18H	CC3[7]	CC3[6]	CC3[5]	CC3[4]	CC3[3]	CC3[2]	CC3[1]	CC3[0]
19H	CC4[7]	CC4[6]	CC4[5]	CC4[4]	CC4[3]	CC4[2]	CC4[1]	CC4[0]

Symbol	Description	
CC1[7] – CC1[0]	Line 21 –1	Closed Caption
CC2[7] – CC2[0]	Line 21 –2	
CC3[7] – CC3[0]	Line 284 -1	Extended Data
CC4[7] – CC4[0]	Line 284 -2	

- When the 2nd byte of Closed Caption Data and Extended Data is written in, AK8811/12 recognizes the renewed data and encodes it in the video line. When the data is not renewed AK8811/12 outputs NULL code.

Video ID Data Register (W only default 00H)

Sub Add	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1AH	Reserved	Reserved	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6
1BH	bit 7	bit 8	bit 9	bit 10	bit 11	bit 12	bit 13	bit 14

- Please write value 0 at Reserved bit.
- Bit numbers correspond to Fig. 5 VBID code assignment.
- AK8811/12 generates CRC 6 bit data automatically.

Followings are read only register

STATUS REGISTER (R only)

Sub Add	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
24H	Reserved	Reserved	EN284	EN21	SYNC	STS2	STS1	STS 0

Symbol	Value	Description
EN284	0	Wait for the appointed video line to encode.
	1	Ready for the C.C. data input to the register.
EN21	0	Wait for the appointed video line to encode.
	1	Ready for the C.C. data input to the register.
SYNC	0	Missing synchronization in slave mode.
	1	Synchronization was achieved.
STS2 - STS 0	***	Shows the processing field No.

- Status Register becomes effective when SYNC bit turns to “1”. When in master mode operation, this bit is ”1”.
- STS2-STS2 holds the field number of processing. Some time lag is inevitable for the I^2C acquisition.
- Closed caption data should be renewed after firm that the EN* flag is “1”. EN* flag bit is cleared after the second byte(Sub address 17H,19H) was accessed.
- Reserved-bit is always value 0.

Device ID (R only default 21H)

Sub Add	bit7	bit6	bit5	bit4	Bit3	bit2	bit1	bit0
25H	0	0	0	1	0	0	0	1

- Represents device ID. AK8811 is assigned 11H.

Sub Add	bit7	bit6	bit5	bit4	Bit3	bit2	bit1	bit0
25H	0	0	0	1	0	0	1	0

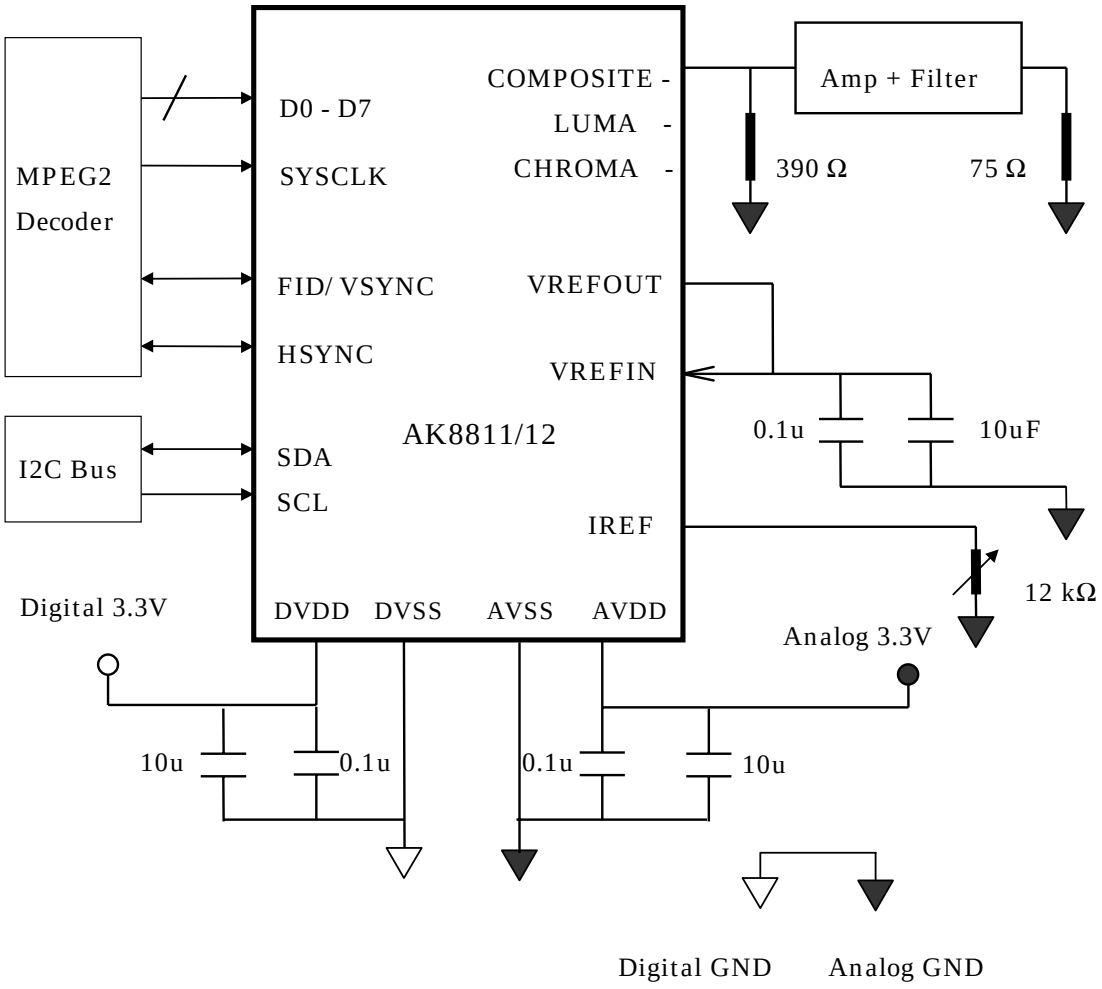
- Represents device ID. AK8811/12 is assigned 12H.

Device REV (R only default 01H)

Sub Add	bit7	bit6	bit5	bit4	Bit3	bit2	bit1	bit0
26H	0	0	0	0	0	0	0	1

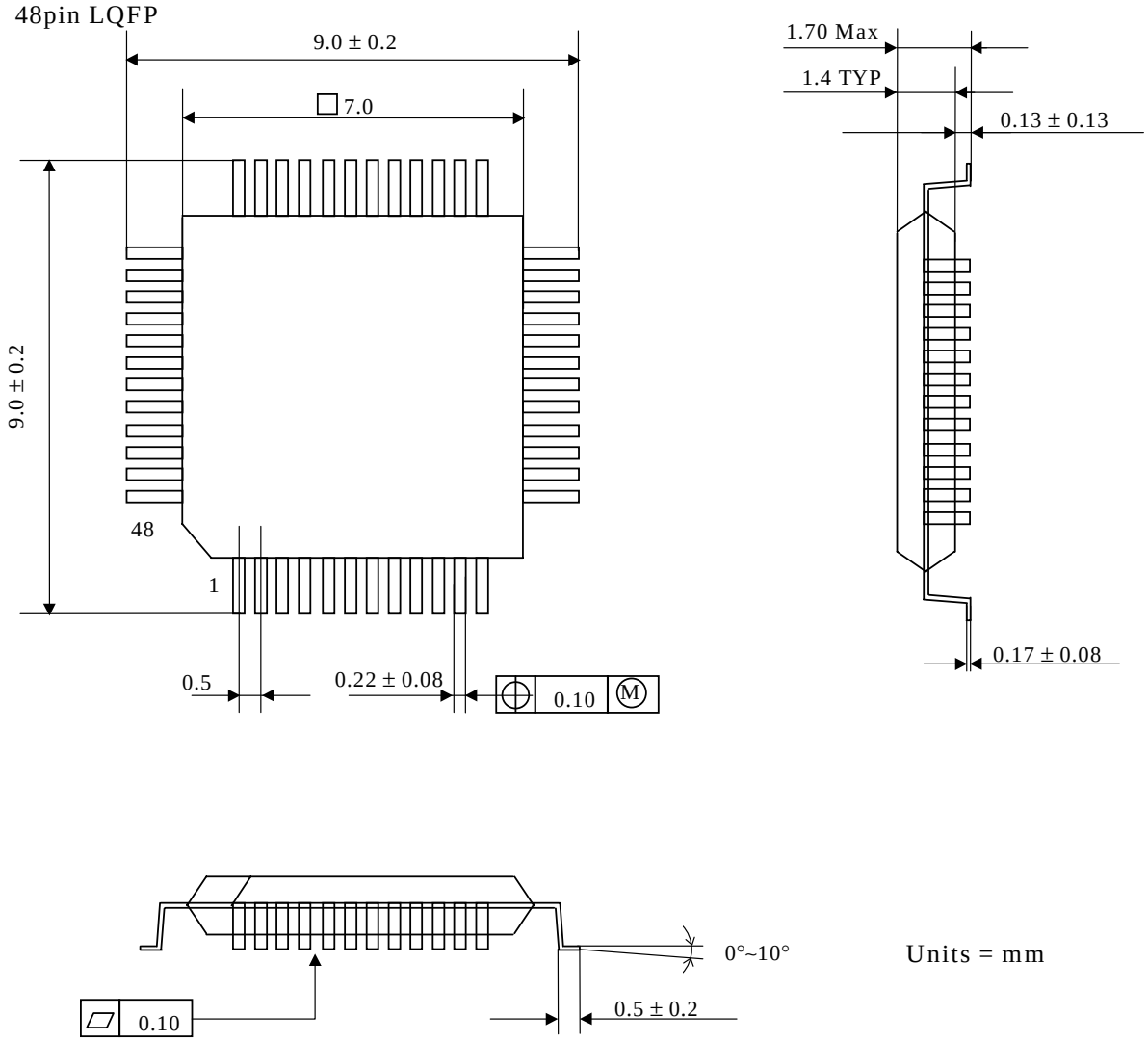
- Represents device revision. Initial is 01H.

SYSTEM CONNECTION EXAMPLE



PACKAGE

48pin LQFP



Units = mm

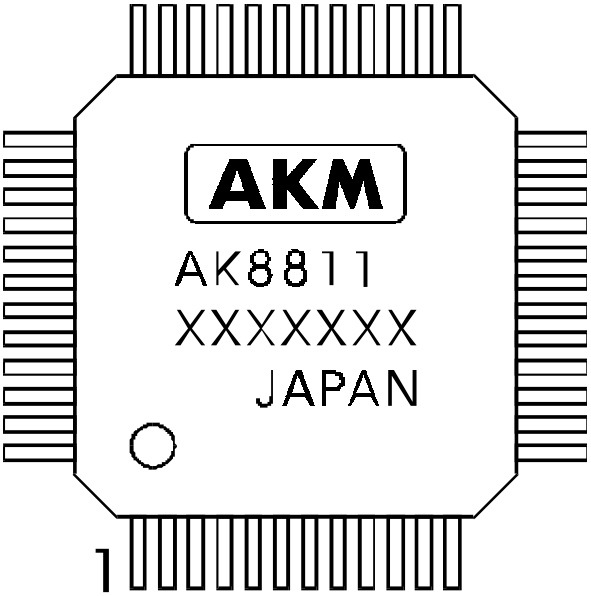
Package & Lead frame material

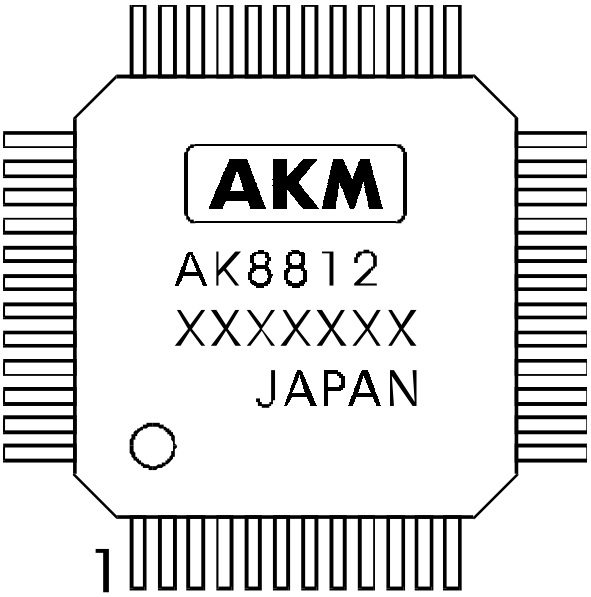
Package molding compound : Epoxy

Lead frame material : Cu

Lead frame surface treatment : Solder plate

MARKING





1) Pin #1 indication
2) Date Code : XXXXXXX (7 digits)
3) Marketing Code : AK8811/AK8812
4) Country of Origin
5) Asahi Kasei Logo