What Does It Do?

Vectron International's TRU-050 module is a user-configured, phase-locked loop (PLL) solution designed to simplify a wide variety of clock recovery and data retiming, frequency translation and clock smoothing applications. The device features a phase-lock loop ASIC with a quartz stabilized VCXO for superior stability and jitter performance. This highly integrated module provides unsurpassed performance, reliability and quality. The proprietary ASIC device includes a refined Phase Detector, a Loop Filter Op-Amp, a Loss of Signal Alarm with Clock Return to Nominal feature, a VCXO circuit, and an optional 2^n divided output.

The ASIC and quartz resonator are housed in a hermetic 16-pin DIL ceramic package with optional thru-hole or surface mount leads. The VCXO frequency (OUT1) and division factor (OUT2) are factory set in accordance with customer specifications. PLL response is optimized for each application by the selection of three external passive components. Software is available from Vectron to aid in loop filter component selection and loop response modeling.

Features:

PLL with quartz stabilized VCXO

Output jitter less than 20 ps

Loss of signal (LOS) alarm

Return to nominal clock upon LOS

Input data rates from 8 kb/s to 65 Mb/s

Surface mount option

Tri-state output

User defined PLL loop response

NRZ data compatible

Robust hermetic ceramic package

Single or +5.0 V supply (+3.3V option available)

Benefits:

Flexible modular solution

Reduce design time

Increase circuit reliability

Less board space

Reduces component count

What is the main benefit of the TRU-050?

It's a single drop-in Quartz Stabilized PLL solution.

What's Inside?

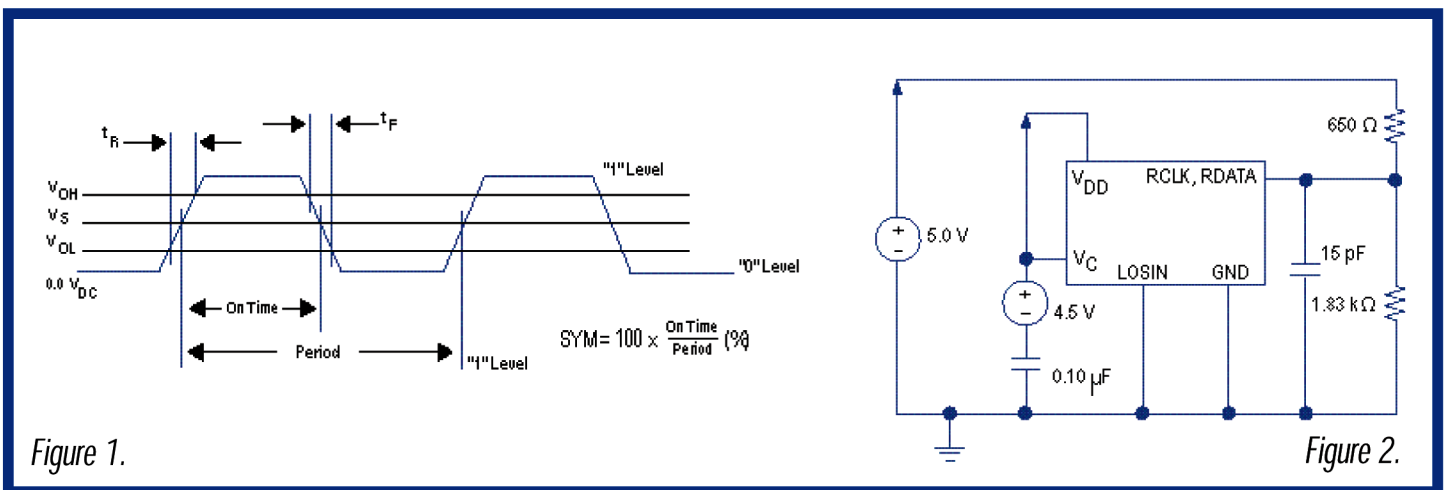| Parameter	Symbol	Min	Max	Unit
Input NRZ Data Rates	DATAIN	0.008	65.536	MHz
Input RZ Data and Clock Rates [1]	DATAIN	0.008	32.768	MHz
Nominal Output Frequency				
Output 1	OUT1	12.0	65.536	MHz
Output 2 [2]	OUT2	0.05	32.768	MHz
Supply Voltage [3]	V_{DD}	4.5	5.5	V
Supply Current (V_{DD} = 5.5 V)	I_{DD}	25	63	mA
Output Voltage Levels (V_{DD} = 4.5 V)				
Output Logic High [4]	V_{OH}	2.5	-	V
Output Logic Low [4]	V_{OL}	-	0.5	V
Transition Times: [4]				
Rise Time (0.5 V to 2.5 V)	t_R	0.5	5	ns
Fall Time (2.5 V to 0.5 V)	t_F	0.5	5	ns
Symmetry or Duty cycle [5]				
Output 1	SYM 1	40	60	%
Output 2	SYM 2	45	55	%
Recovered Clock	R_{CLK}	40	60	%
Input Data				
Input Logic High	V_{IH}	2.0	-	V
Input Logic Low	V_{IL}	-	0.8	V
Control Voltage Bandwith (-3 dB, VC = 2.50 V)	BW	50	-	kHz
Sensitivity @ VC = VO	$\Delta F/\Delta V_C$	See Figure 11		ppm/V
Loss of Signal Indication [6]	L_{OS}			
Output Logic High	V_{OH}	2.5	-	V
Output Logic Low	V_{OL}	-	0.5	V
Nominal Output Frequency on Loss of Signal: [7]				
Output 1	OUT1	-75 ppm	75 ppm	ppm from fo 1
Output 2	OUT2	-75 ppm	75 ppm	ppm from fo 2
Phase Detector Gain	K_D	-0.53 x Data Density		V/rad

Table 1.

1. For input RZ data, Manchester encoded data, and input clock recovery applications, the output clock must run at two times the input rate to ensure that the input is clocked correctly. Since the output clock has a maximum frequency of 65.536 MHz, these inputs are limited to a maximum rate of 32.768 MHz.

2. OUT2 is a binary submultiple of OUT1, or it may be disabled.

3. A 3.3 volt supply option is also available.

4. Figure 1 defines these parameters. Figure 2 illustrates the equivalent five-gate MTTL load and operating conditions under which these parameters are specified and tested.

5. Symmetry is the ON TIME/PERIOD in percent with V_S = 1.4 V for TTL, per figure 1.

6. A loss of signal (LOS) indicator is set to a logic high if no transitions are detected at DATAIN after 256 clock cycles. As soon as a transition occurs at DATAIN, LOS is set to a logic low.

7. Accuracy at room temperature. Stability over temperature is typically ± 20 ppm.

Figure 1.

$SYM = 100 \times \dfrac{On\ Time}{Period}$ (%)

Figure 2.

Pin	Symbol	Function
1	V_C	Control voltage input to internal voltage controlled crystal oscillator (VCXO).
2	OPN	Negative input terminal to internal operational amplifier.
3	OPOUT	Output terminal of internal operational amplifier.
4	OPP	Positive input terminal to internal operational amplifier.
5	LOSIN	With LOSIN set to a logic high, the external input to the VCXO (VC) is disabled and the VCXO returns to it's nominal center frequency. With LOSIN set to logic low, the external input to the VCXO is enabled. The LOSIN input has an internal pull-down resistor.
6	PHO	Output signal produced by phase detector.
7	DATAIN	Input data stream to phase detector (TLL switching thresholds).
8	GND	Circuit and cover ground.
9	CLKIN	Input clock signal to phase detector (TTL switching thresholds).
10	LOS	Loss of signal indicator is set to a logic high if no transitions are detected at DATAIN after 256 clock cycles. As soon as a transition occurs at DATAIN, LOS is set to a logic low.
11	RCLK	TTL compatible recovered clock.
12	RDATA	TTL compatible recovered data stream.
13	OUT2	Divided version of internal VCXO output clock (TTL).
14	HIZ	When set to a logic low, output pins OUT1, OUT2, RCLK, and RDATA buffers are set to high-impedance state. When set to a logic high or no connect, the device functions and output pins OUT1, OUT2, RCLK, and RDATA are active. This input has an internal pull-up resistor.
15	OUT1	Output clock of internal VCXO (TTL).
16	V_{CC}	+5.0 V ±10% supply voltage (+3.3 V option available).

Table 2.

Why would someone buy a TRU-050?

To save design time, reduce component count, conserve board space, and optimize manufacturing efficiency.
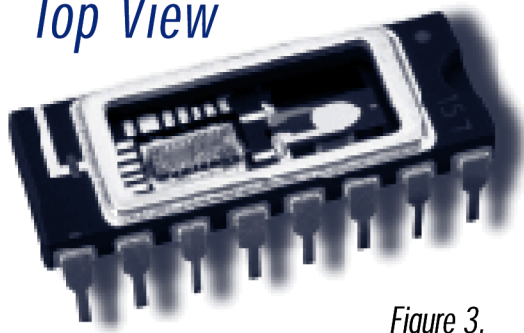
Top View

Figure 3.

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The TRU-050 is a user-configured phase-locked loop (PLL) integrated circuit. It includes a voltage controlled crystal oscillator (VCXO), an operational amplifier, a phase detector, and additional integrated functions for use in digital synchronization applications. These applications include timing recovery and data pulse restoration for data signals, clock frequency translation and smoothing, synchronous distributed clock networks, and clock frequency synthesis.
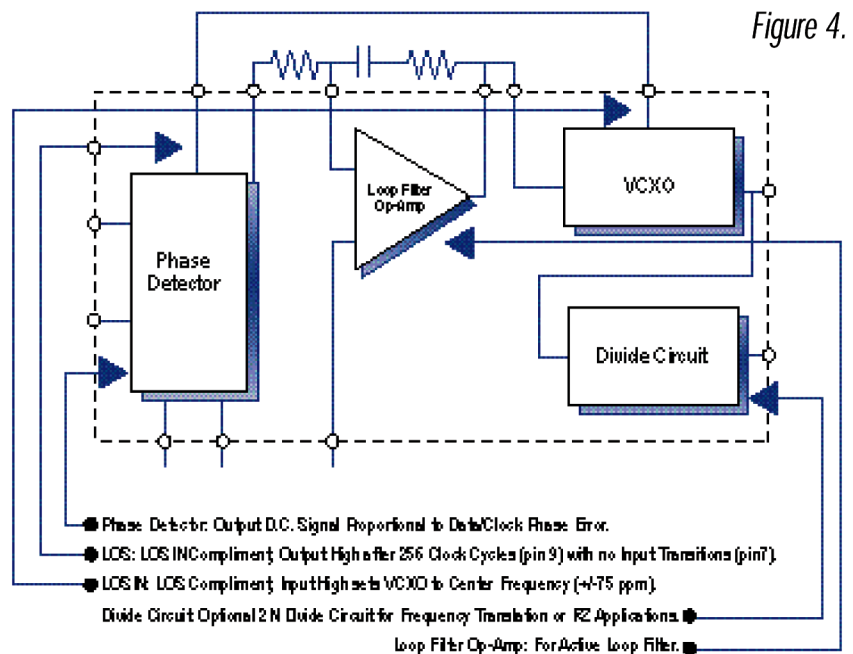
What is the output of the phase detector?

The TRU-050 phase detector output is a DC signal, under locked conditions, and is nominally 2.5 Volts. The phase error (which is typically a pulse for digital phase detectors) is converted to a DC level, making it easy to design the loop filter.

How long does the TRU-050 take to detect a loss of signal?

If there are no transitions on DATAIN for a period of 256 clock cycles, LOS is set to a logic 1. LOS is reset to logic 0 as soon as there are DATAIN transitions.

TRU-050 Elements

Figure 4.

• Phase Detector: Output D.C. Signal Proportional to Data/Clock Phase Error.
• LOS: LOS IN Compliment; Output High after 256 Clock Cycles (pin 9) with no Input Transitions (pin 7).
• LOS IN: LOS Compliment; Input High sets VCXO to Center Frequency (+/-75 ppm).
Divide Circuit Optional 2 N Divide Circuit for Frequency Translation or RZ Applications.
Loop Filter Op-Amp: For Active Loop Filter.

Phase Detector

The phase detector is designed to accept an NRZ data stream at DATAIN (Pin 7- refer to figure 5), but may be used for clock signals and other data types. The input buffers are designed to switch at a TTL switching threshold of 1.4 V.

The phase detector's inputs are:
  • DATAIN (Pin 7) - the input clock or NRZ data signal
  • CLKIN (Pin 9) - the clock signal feedback from the VCXO output OUT1 or OUT2

And the outputs are:
  • RCLK (Pin 11) - the regenerated clock signal
  • RDATA (Pin 12) - the retimed data signal
  • PHO (Pin 6) - the phase detector output
  • LOS (Pin 10) - a loss of signal detector

The phase relationship between the regenerated clock signal, RCLK (Pin 11), and the regenerated data signal, RDATA (Pin 12), is shown in figure 6.
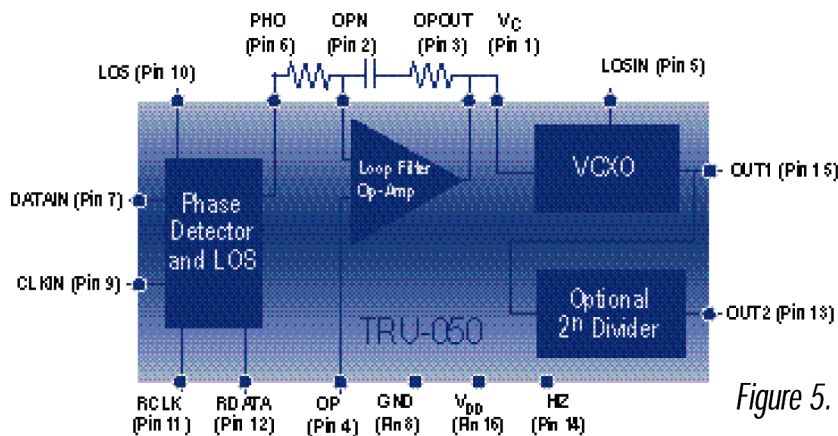
Figure 5.

The falling edge of RCLK is coincident with the center of the regenerated NRZ RDATA pulse. Figure 6 shows a 1010 data stream with a 100% data transition density. In general, this will not be the case and input data will have fewer data transitions. However, the phase detector will still seek to align the falling edge of the RCLK signal with the center of each RDATA pulse.
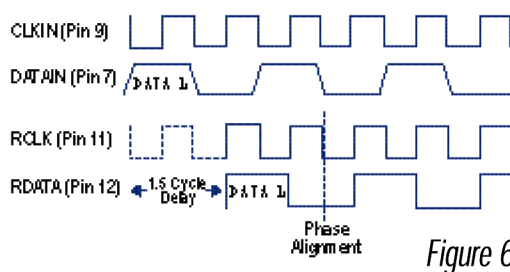

Figure 6.

For applications where the input clock or data signal, DATAIN, is very low in frequency (<200kHz), clock information may pass through the phase detector because of its finite low pass characteristic. In applications such as this, an additional pole may be necessary in the loop filter to attenuate these AC components prior to the VCXO input. Please contact Vectron's Applications Engineering staff for further detail.
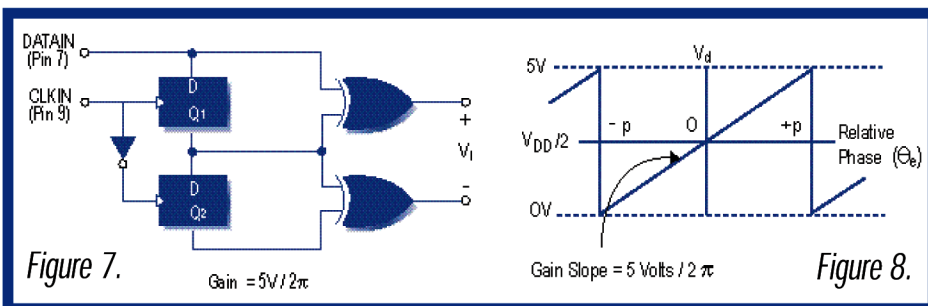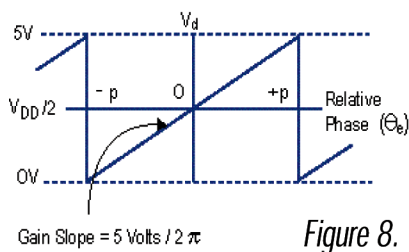

Figure 7.

Figure 8.

Phase Detector Gain Calculation

The schematic diagram (figure 7) shows a simplified representation of the phase detector's basic error generation function. The actual circuit is more complex and includes circuitry to reduce the TRU-050's dependence on input data duty-cycle. In general, the TRU-050 is insensitive to duty cycle and duty cycle changes. This circuit provides a output (V_D) DC level which is proportional to the relative phase of DATAIN (Pin 7) and CLKIN (Pin 9). A plot of the output (V_D) versus relative phase is shown in figure 8. The slope of the output (V_D) versus relative phase (0_e) is $5V/2\pi$.

The phase detector block also includes an output gain stage which should be considered when calculating the gain of the complete phase detector block. This gain stage has a gain of $2/3$, and converts the differential signal to a single-ended DC output.

DATAIN
(Pin 7)

CLKIN
(Pin 9)

D
Q1

D
Q2

20 kΩ

30 kΩ

PHO
(Pin 6

Figure 9.

Gain = 5V / 2 π

Gain = 2/3
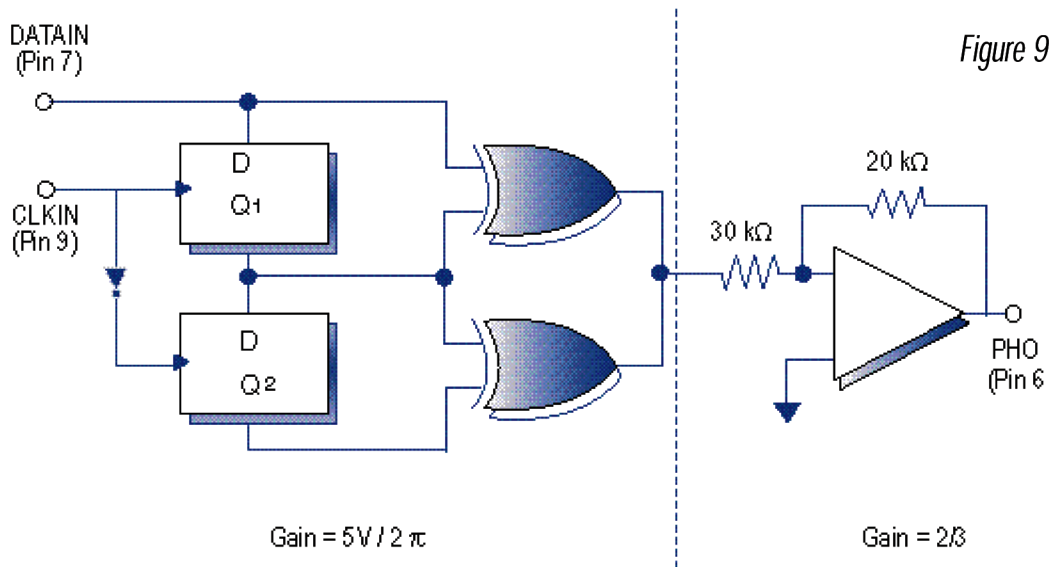
*Phase Detector Gain = [5V/2π] * [2/3] * D = 0.53 * D*
Where D = input data transition density. For example D = 1 for 100% transition density (e.g., clock signal)
and D = 0.5 for 50% transition density (e.g., balanced NRZ data).

LOS and LOSIN

The LOS circuit provides an output alarm flag when the DATAIN input signal is lost. The LOS output is set "logic high" after 256 consecutive CLKIN periods with no DATAIN transitions. This signal can then be used to either flag external alarm circuits and/or drive the TRU-050's LOSIN circuit. When the LOSIN input is set "logic high," the loop filter op-amp output is set mid supply to facilitate fast lockup when DATAIN is restored. In addition, the VCXO control voltage is internally set to hold the VCXO at its nominal frequency (±75 ppm). When LOSIN is low or has no connection, the VCXO's control voltage input is enabled (LOSIN has an internal pull-down resistor).

Loop Filter

Although various loop filter configurations may be considered, most TRU-050 applications use the basic integrator filter of figure 10. This type of filter provides high DC gain to ensure proper clock and data alignment. The ratio of R1 to RF sets midband gain and can be used to adjust the loop bandwidth. The time constant, set by RF and CF, should be selected to be about one decade below the open loop bandwidth to provide good phase margin.   The reference for the non-inverting input is set at midsupply by R2 and R3. Software is available to help in the selection of R1, CF and RF.
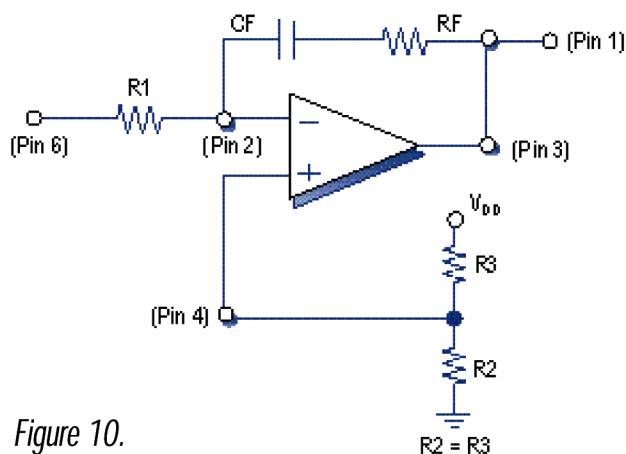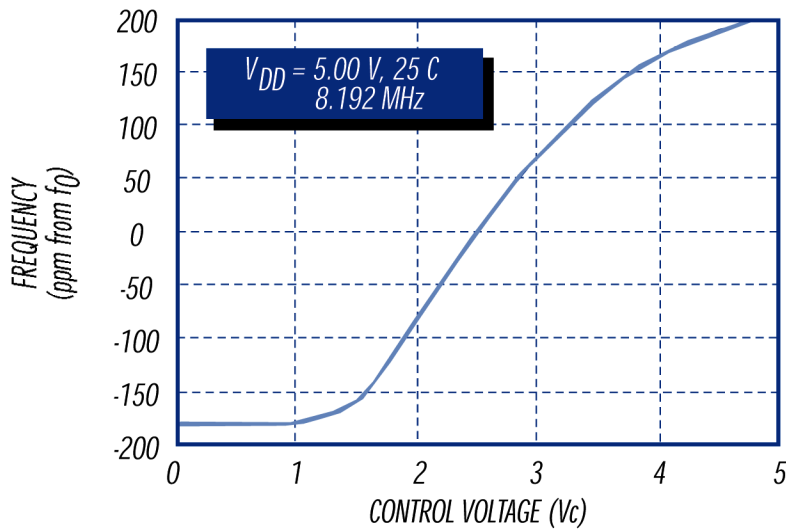

CF   RF   (Pin 1)

R1
(Pin 6)   (Pin 2)   (Pin 3)

V_DD

R3

(Pin 4)

R2

Figure 10.   R2 = R3

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Figure 11.

V_{DD} = 5.00 V, 25 C
8.192 MHz

FREQUENCY (ppm from f$_0$)

CONTROL VOLTAGE (Vc)

TRU-050 VCXO Frequency Deviation vs. Control Voltage

VCXO

The TRU-050's VCXO is a varactor-tuned crystal oscillator which produces an output frequency controlled by a control voltage, V_c. The tracking range of the VCXO is specified as absolute pull range (APR) when ordered. An APR of ±50 ppm guarantees that the TRU-050 can track an input source frequency with ±50 ppm stability over all operating conditions, including temperature, time, power supply and load variations. The value of V_c is varied between 0.5 V to 4.5 V to achieve the specified APR. A typical frequency versus V_c curve for the VCXO in the TRU-050 is shown in figure 11. When designing PLLs, the VCXO gain (kV in Hz/V or rad/Vs) is an important parameter. As a rule of thumb, the frequency deviation for the TRU-050 VCXO is 300 ppm over the 1 V to 4 V range V_c.

For example, a 10 MHz VCXO has an average gain of 1000 Hz/V. The peak value of kV is about twice this value at approximately 2.5 V, and one half this value at 1 V and 4 V.

For many loop calculations, the gain is expressed in rad/Vs which would be 2π (100 ppm * f$_0$/Vs) for the previous example.

Oscillator Aging

Any crystal stabilized oscillator typically exhibits a small shift in output frequency during aging. The major factors which lead to this shift are changes in the mechanical stress on the crystal and mass-loading of foreign material on the crystal.

As the oscillator ages, relaxation of the crystal mounting stress or transfer of environmental stress through the package to the crystal mounting arrangement can lead to frequency variations. Vectron has minimized these two effects through the use of a miniature AT-cut strip resonator crystal which allows a superior mounting arrangement and results in minimal relaxation and almost negligible environmental stress transfer.

How is quality assured?

In addition to extensive testing, the basic design consists of a few highly engineered, robust components; quality is further assured by advanced ceramic packaging and fully automated assembly.

Mass-loading on the crystal generally results in a frequency decrease and is typically due to out-gassing of material within a hermetic package or from contamination by external material in a non-hermetic package. Vectron has minimized the impact of mass loading by ensuring hermetic integrity and minimizing out-gassing by limiting the number of internal components through the use of ASIC technology.

Under normal operating conditions with an operating temperature of 40°C, the TRU-050 will typically exhibit 2 ppm aging in the first year of operation. The device will then exhibit 1 ppm aging the following year with a logarithmic decline each year thereafter.

Absolute Pull Range

Absolute pull range (APR) is specified by the fourth character of the product code (see figure 26). APR is the minimum guaranteed frequency shift from f_0 over variations in temperature, aging, power supply and load. Both frequency and environment limit the specified APR. The total pull range for the VCXO contained in the TRU-050 is typically between 200 ppm and 400 ppm. A 50 ppm APR TRU-050 fully tracks a 50 ppm source oscillator or any other 50 ppm reference over the operating temperature range, life of the product, power supply and measurement variations.

Output Divider Circuit

An internal 2^n divided output is available at OUT2. The value of n varies from 1 to 8 and is set during manufacture. This provides divide ratios from 2 to 256. A "no output" option may also be selected to minimize power usage and jitter.

Divider Note: The frequency of OUT1 is the fundamental frequency of the VCXO used in the TRU-050. The lowest frequency VCXO (OUT1) available in the TRU-050 is 12 MHz, and the highest frequency is 65.536 MHz. Therefore, the frequency range of OUT1 is between 12 MHz and 65.536 MHz. Since OUT2 is a division of OUT1 and can vary from OUT1 ÷ 2 to OUT1 ÷ 256, OUT2 ranges from 46.875 kHz (12 MHz ÷ 256) to 32.768 MHz (65.536 MHz ÷ 2). Lower frequency inputs may be supplied to the phase detector of the TRU-050, but an external divider in the feedback loop is required. With an external divider in the feedback loop, clock and data signals down to 8 kHz can be used as phase detector inputs.

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Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. Vectron employs a human body model (HBM) and a charged device model (CDM) for ESD susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the mode. Although no industry-wide standard has been adopted for CDM, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and therefore can be used for comparison purposes. The HBM ESD threshold presented here was obtained using these circuit parameters.

MODEL	ESD Threshold, Minimum	Unit
Charged Device	2000	V
Human Body	2000*	V

* MIL-STD-883D, Method 3015, Class 1

Table 3.
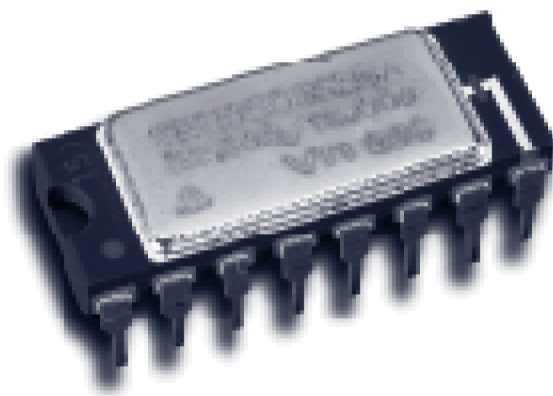
How is it packaged?

The TRU-050 is a very robust product which is assembled on an automated manufacturing line. It is packaged in a 16-pin, ceramic DIP with a seam-welded step lid, hermetically sealed for long term reliability. Options include thru-hole and surface mount terminals and an extended temperature range. Tape and reel packaging is also available.

A typical PLL is illustrated in figure 12. Be advised that many textbook equations describing loop dynamics, such as capture range or lockin time, are based on ideal systems. Such equations may not be accurate for real systems with nonlinearities, DC offsets and noise. A PLL is a feedback system which forces the output frequency to lockin both phase and frequency to the fundamental frequency of the input signal.

When initially out of lock, the output of the phase detector is proportional to the difference in frequency between the two phase detector inputs. This beat note varies the output frequency of the VCXO, and in a properly designed phase-locked loop, the loop action forces V_c to the correct value to bring the system into lock.

Figure 12.

Phase Locked Loop Block Diagram
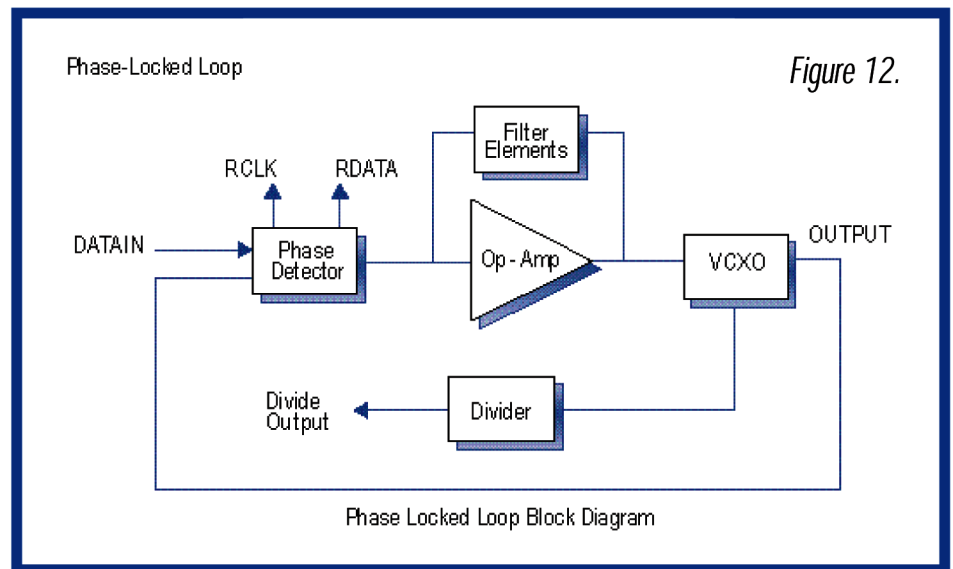
A designer's primary concern is to select a loop filter that ensures lockin and stability, while providing adequate filtering of input signal noise or jitter. An initial design starts with a known DATAIN signal and an output specification. An initial analysis of the open loop gain response provides insight into the response of the system.

Using figure 12, the open loop gain is:

$$G(s) = \frac{Kp\,kV\,AV(s)}{sN}$$

Where:

Kp is the phase detector gain in V/rad (-0.53 x Data Density).

kV is the VCXO gain constant in Rad/Vs.

AV(s) is the loop filter transfer function.

N is the divide ratio.

1/s converts the VCXO frequency output to a phase output.

The open loop gain may be plotted and varied using the SPICE model provided in figure 13. The gain, frequency, and loop filter configurations may be varied to producedesired responses. In the first-order phase-locked loop, where AV(s) and N equal 1, the gain curve has a 20 dB/decade slope with unity gain at:

$$f = \frac{kV\,Kp}{2\pi} \quad \text{where kV is in rad/Vs.}$$

The first-order open loop gain has a constant phase shift of 90 degrees. However, other frequency poles are present in the loop due to the op-amp's limited bandwidth and gain, the phase detector and the VCXO modulation bandwidth (these poles are included in the SPICE model). The loop's bandwidth is approximately equal to the closed loop bandwidth and can be used to assess the stability, lockin range and filtering characteristics of the loop. The loop acts as a bandpass filter centered at the clock frequency, just as if a tank circuit were used to filter the input clock or data stream.

However, the filter Q of the TRU-050 is much greater than that of a tank circuit and typically ranges from 1,000 to 20,000. The PLL tracks input phase jitter inside the loop bandwidth while jitter is attenuated outside the loop bandwidth. Converting the SPICE model (figure 13) to a closed loop illustrates the jitter transfer function shown in figure 15. In general, the PLL rapidly locks those signals with an initial frequency difference (relative to CLKIN) that is within the loop's bandwidth. Lockin time is longer for lower bandwidth loops and may be degraded by jitter or by poor input duty cycle.

Simulated Results

The SPICE model just described can be used to determine the component values necessary to produce a desired loop filter bandwidth, its jitter transfer function and its open loop response for a given application. Alternatively, simulation results can be obtained using Vectron's "TRU-050 Loop Filter Calculation" software. This software runs from DOS and will also provide the user with loop filter component values R1, RF and CF (see figure 15) based on desired loop filter bandwidth, data type, data density, damping factor and data frequency. For assistance with your specific application, or to receive a copy of Vectron's "TRU-050 Loop Filter Calculation" software, please contact Vectron's Application Engineering staff.
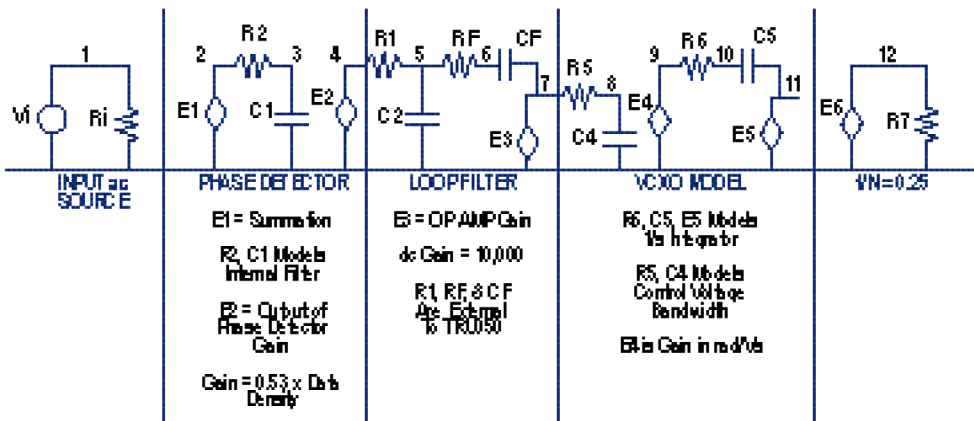
SPICE Model

```
******TRU050 ac Loop Model
vi 1 0 ac 1
ri 1 0 1k


******Phase Detector
e1 2 0 1 0 1
(for closed loop response use:
e1 2 0 1 12 1)
r2 2 3 30k
c1 3 0 60p
******Phase Detector Gain =
     0.53 * Data Density
e2 4 0 3 0 .265
***
******Loop Filter
r1 4 5 10k
c2 5 0 10p
rF 5 6 40k
cF 6 7 .1u
e3 7 0 5 0-10000


******VCXO
******Input Bandwidth = 50 kHz
r5 7 8 160k
c4 8 0 20p
******VCXO Gain 2π Hz/V
******Example 100 ppm *
     30.72 MHz * 2 * π
e4 9 0 8 0 19300


******1/s Model
r6 9 10 1000
c5 10 11 .001
e5 11 0 10 0-1e6


******Divide by N
e6 12 0 11 0 1
r8 12 0 1k
```


Figure 13.

SPICE Simulated Results

Open Loop Response

Figure 14.

* Phase margin is 87.0° at 1000.0 Hz

* Open loop gain margin is -3.92e+01 at 60000.0 Hz

* Closed loop jitter bandwidth (-3 dB) is 1500 Hz.

* The maximum value of the closed loop gain is 0.11614 dB at a frequency of 65.000 Hz

* Damping factor = 4.0

* R1 = 13.5 k ohm

* RF = 79.6 k ohm

* CF = 0.10 μF

* Data density = 100%

* VCXO FREQ = 32.768 MHz

* Feedback divider = 8

Closed Loop Response
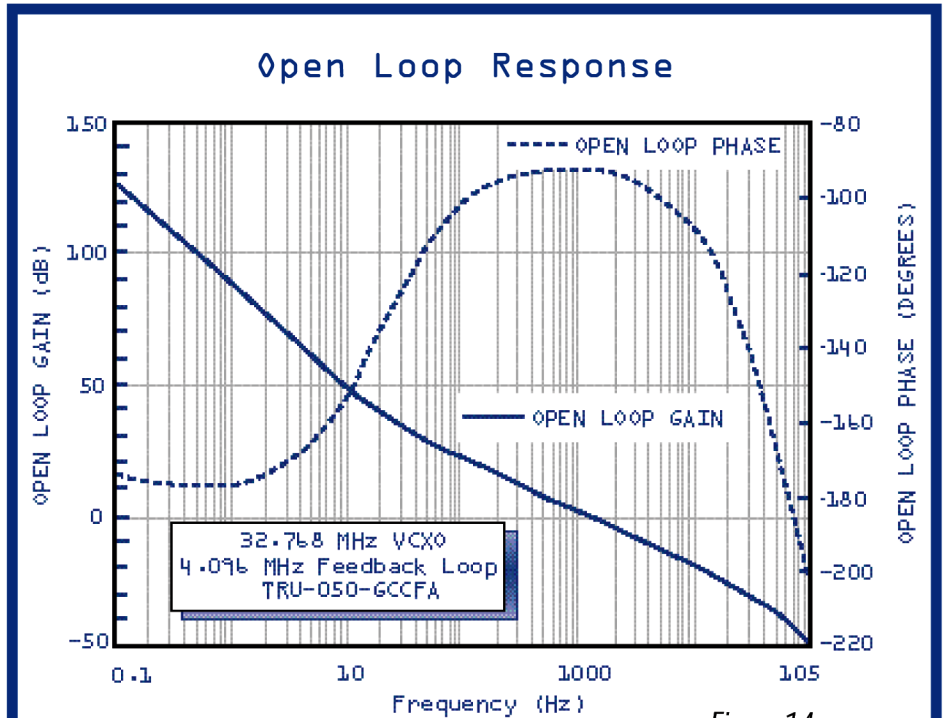

Figure 15.

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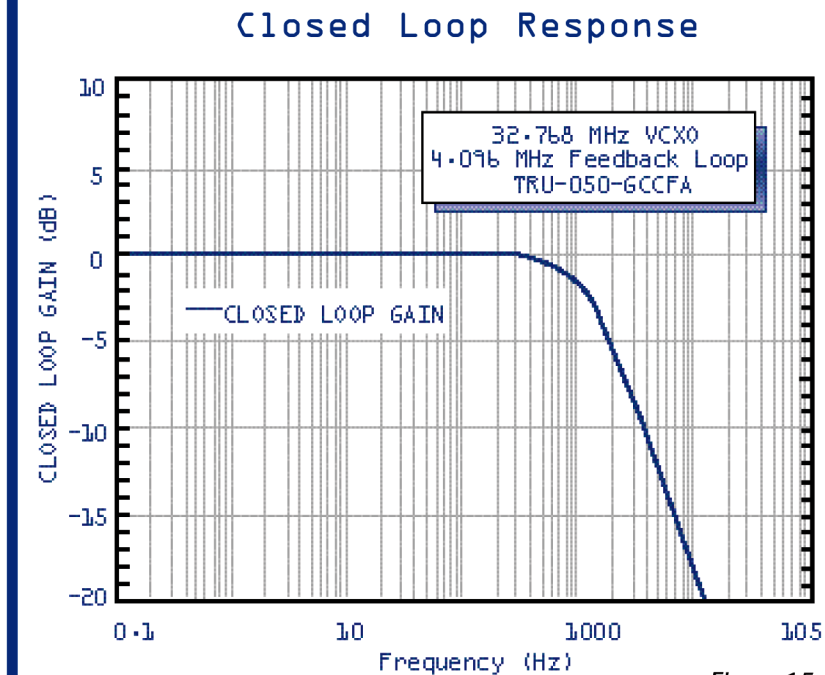
Applications

The three key applications for the TRU-050 are clock recovery of digital data, frequency translation and clock smoothing. These timing needs are required by a wide variety of markets such as telecommunications, datacommunications, digital video and audio, telemetry, test equipment and sensing.

Clock Recovery and Data Retiming

The TRU-050 was designed to recover a clock imbedded in an NRZ data signal, and retime it with a data pattern. In this application, the VCXO frequency is exactly the same as the NRZ data rate and the outputs are taken off Pin 11 (Recovered Clock) and Pin 12 (Recovered Data). The diagram below shows a typical circuit.

Figure 17 shows the relationship between DATAIN (Pin 7) and CLKIN (Pin 9) under locked conditions. The rising edge of the CLKIN is centered to the DATAIN pulse.
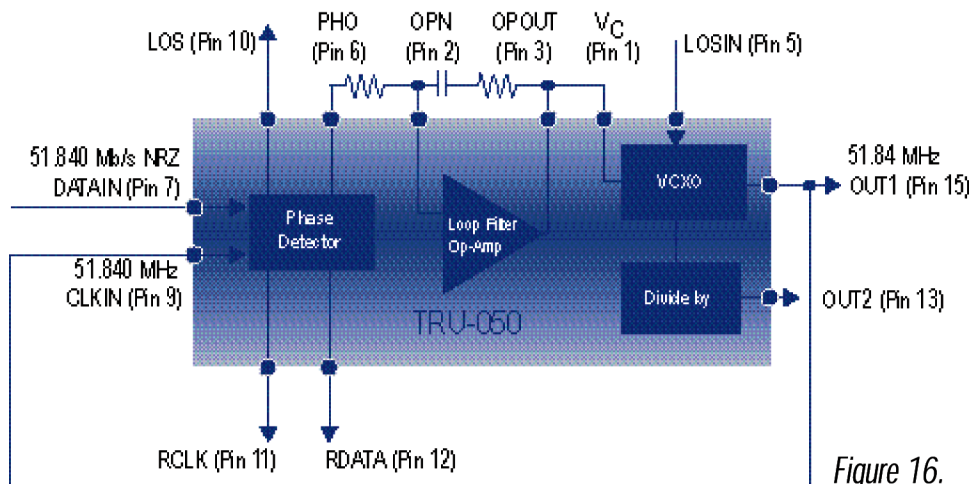

Figure 16.

Relationship of RCLK (Pin 11) and RDATA (Pin 12). The falling edge of the Recovered Clock is in the middle of the data pattern and should be used to clock the data into the next part of the circuit. There is a one and a half cycle delay (frequency of Pin 9) between DATAIN and RDATA. Therefore a 10 MHz signal would have a 150 nS delay between DATAIN and RDATA plus additional circuit delays, which are typically 9 nS.
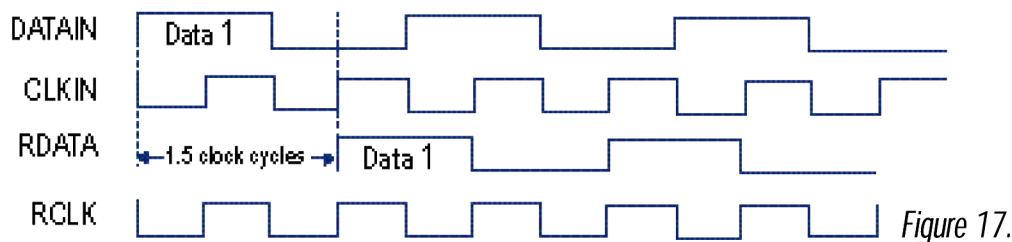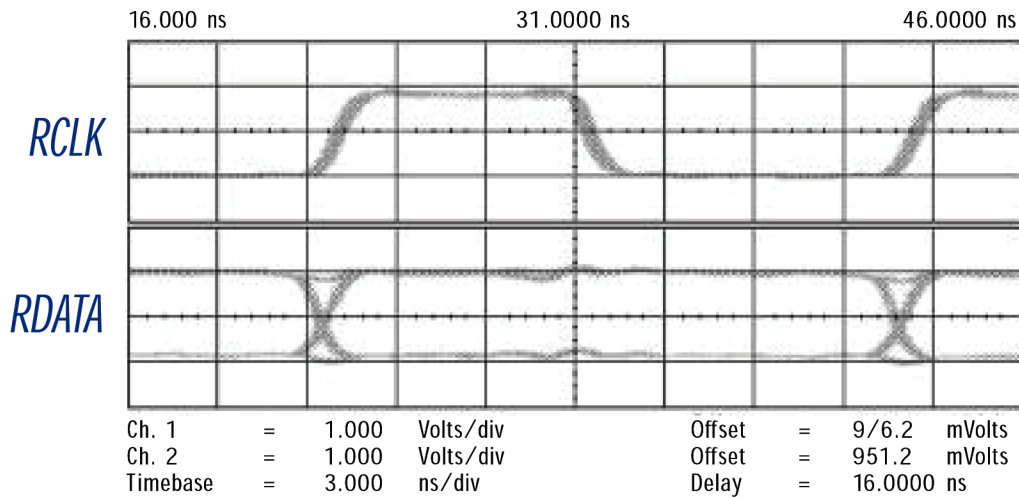

Figure 17.

Is Vectron ISO registered?

Yes! Vectron's quality system was registered to ISO 9001 in October 1996.

16.000 ns   31.0000 ns   46.0000 ns

RCLK

RDATA

Ch. 1	=	1.000	Volts/div	Offset	=	9/6.2	mVolts
Ch. 2	=	1.000	Volts/div	Offset	=	951.2	mVolts
Timebase	=	3.000	ns/div	Delay	=	16.0000	ns

Eye Diagram for

TRU-050 @ 51.84 MHz

The falling edge of RCLK

is centered with respect

to RDATA

Figure 18.

Timing Recovery Using OUT2

Due to the limitations in crystal size, the lowest frequency from OUT1 is 12 MHz. For applications below this frequency, the internal divide-by can be used (Note: an additional external divide-by can also be used). An application for 1.544 MHz clock recovery is shown in figure 19.
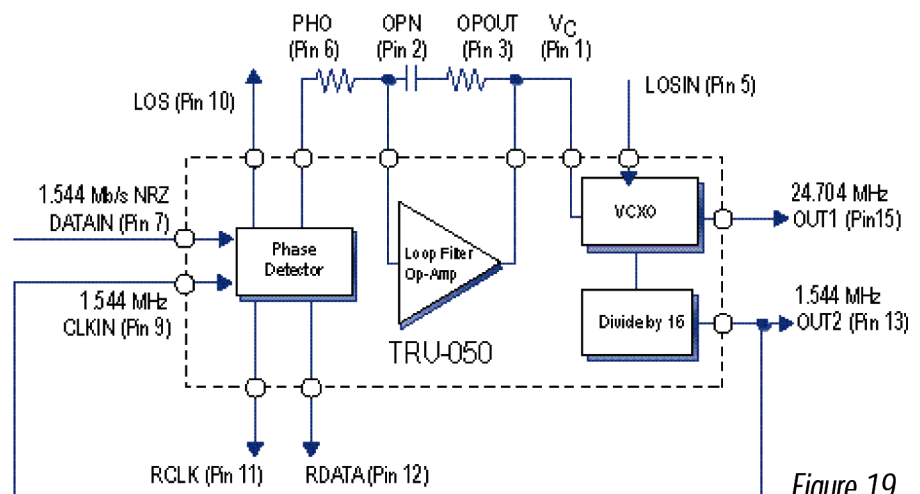

Figure 19.

Frequency Translation

The TRU-050 is most commonly used for frequency translation. For example, in a telecommunications application, when a 2.048 MHz reference clock is multiplied to 32.768 MHz, a very clean 32.768 MHz clock would then be output to other circuits.

Generally, the TRU-050 is specified in terms of NRZ input. Since the TRU-050's phase detector was designed for NRZ data, other inputs such as a clock signal should be considered as an equivalent 1010...NRZ pattern.

Vectron International   267 Lowell Road, Hudson, NH 03051   Tel: 1-88-VECTRON-1   e-mail: vectron@vectron.com

If the DATAIN input to the phase detector is a clock signal, the VCXO, or the divided VCXO output fed back to CLKIN, must be twice the DATAIN rate. In figure 20, the 2.048 MHz system reference clock can be treated as a 4.096 MHz NRZ data stream with a data density of 100%. Therefore, the feedback frequency in the PLL would be 4.096 MHz (the 32.768 MHz clock frequency divided by 8).
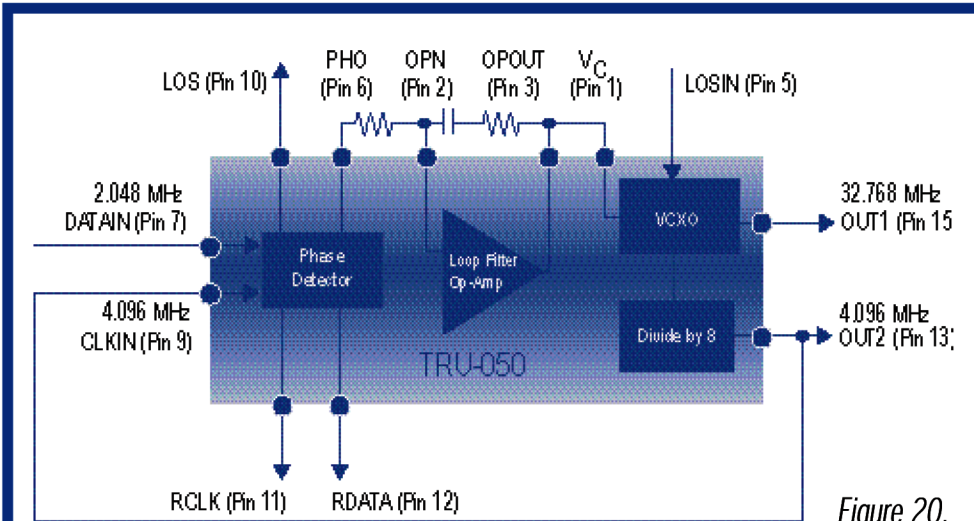

Figure 20.

The Timing diagram above shows a 2.048 MHz clock input being translated to 32.728 MHz clock output.

Figure 21.

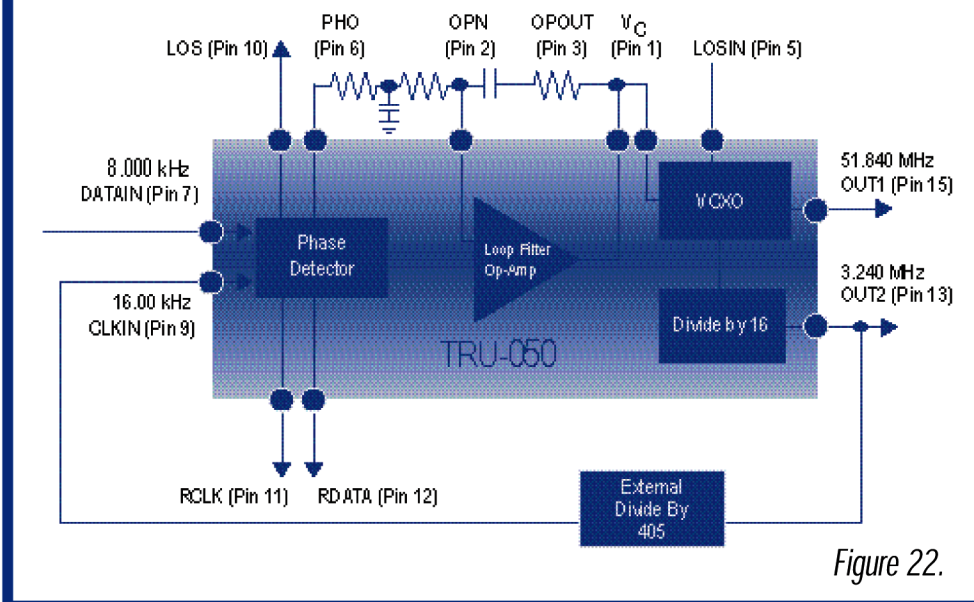Another example would be to translate 8.000 kHz to 51.840 MHz.

Figure 22.

For applications where the DATAIN is very low in frequency (roughly <200 kHz), clock information may pass through the phase detector because of its finite low pass characteristics. In applications such as this, an additional pole may be necessary in the loop filter to attenuate these AC components prior to the VCXO input (note the capacitor to ground in figure 22). Please contact Vectron's Applications Engineering staff for further detail.

Clock Smoothing Example

The third common application of the TRU-050 is for the Regeneration or "Smoothing" of a degraded input clock signal. In this application, the TRU-050 accepts a degraded input clock signal and regenerates the signal to square up the rising and falling edges and remove unwanted jitter. The output is then a clean quartz locked representation of the degraded input signal. Figure 23 illustrates a common example of a clock signal regeneration application. In this example, a degraded 16.384 MHz clock signal is smoothed using the TRU-050. The 16.384 MHz clock is fed into DATAIN (Pin 7). The signal is then regenerated, and a smoothed representation of the signal is available at RDATA (Pin 11).

It is important to note that the signal fed back from OUT1 (Pin 15) to CLKIN (Pin 9) is twice the frequency of the degraded input signal at DATAIN (Pin 7). This is because the TRU-050 was originally designed for input NRZ data patterns. Since an NRZ data pattern has one transition per bit, and its associated clock has two transitions per bit, the TRU-050 phase detector requires twice as many transitions at CLKIN (Pin 9) when compared to DATAIN (Pin 7). In the case of an input clock signal, CLKIN (Pin 9) must be twice the frequency of DATAIN (Pin 7). For a 16.384 MHz clock smoothing application, a TRU-050 with a 32.768 MHz OUT1 should be specified.
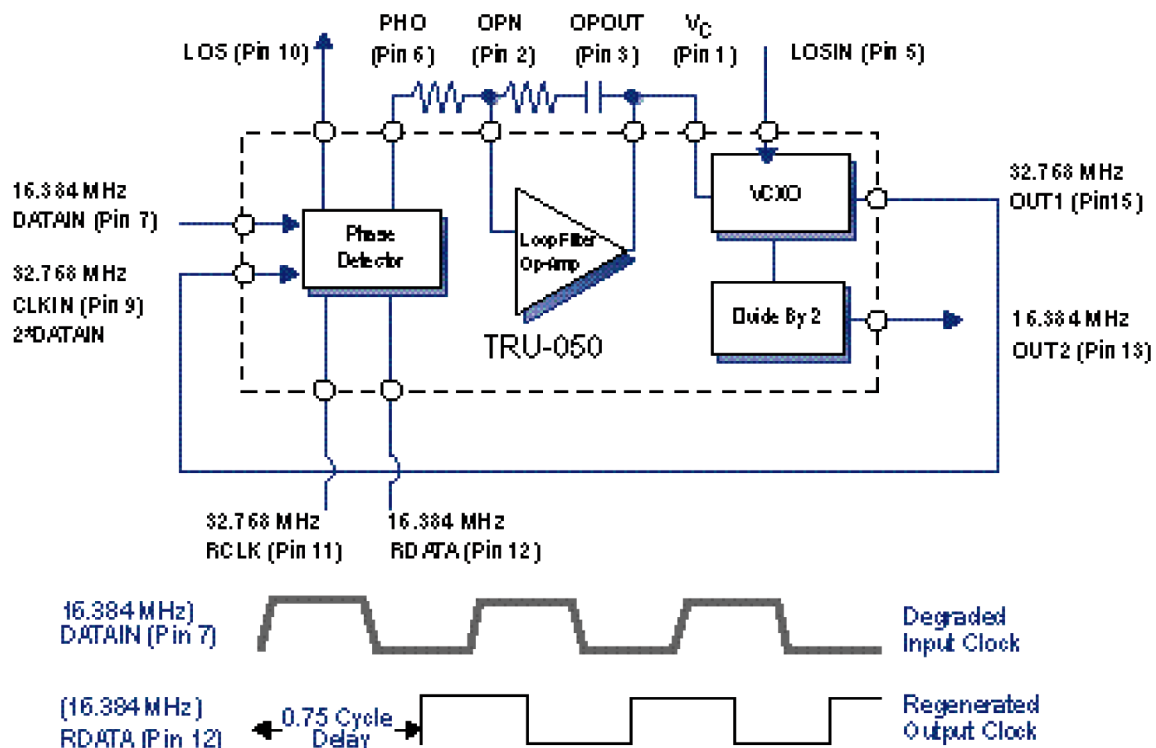

Figure 23.

Figure 24.

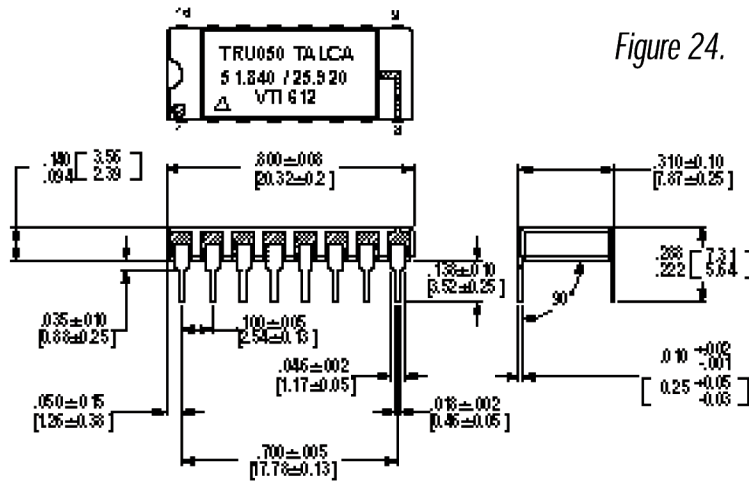## Thru-Hole

Figure 25.

Surface Mount

Questions?
Give us a call:

1-88-VECTRON-1

How Is It Ordered?

TRU050 — T B C C A 51.840 12.960

- OUT 2 Frequency
- OUT 1 Frequency
- Version Number
- Absolute Pull Range
  - C ±20 ppm
  - F ±32 ppm
  - G ±50 ppm
  - H ±100 ppm
- Temperature Range (°C)
  - C 0 to 70
  - L –40 to 85

Package Type
16-Pin Ceramic Dip

Leads
- T Thru-Hole
- G Surface Mount
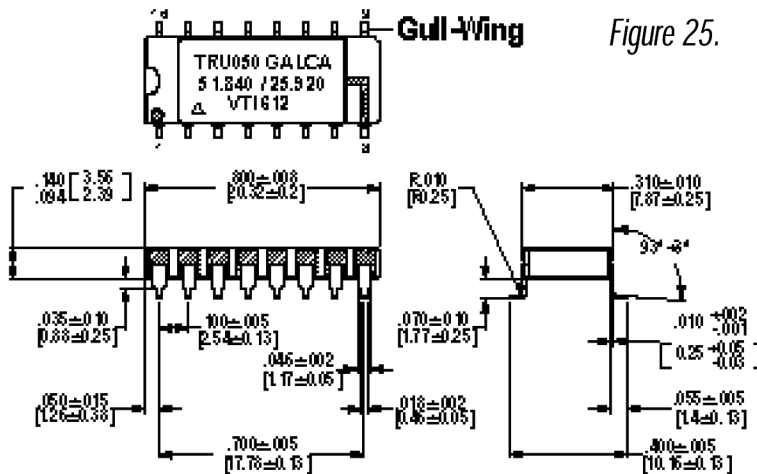
Second Output
- A Divide by 2
- B Divide by 4
- C Divide by 8
- D Divide by 16
- E Divide by 32
- F Divide by 64
- G Divide by 128
- H Divide by 256
- K OUT2 Disabled
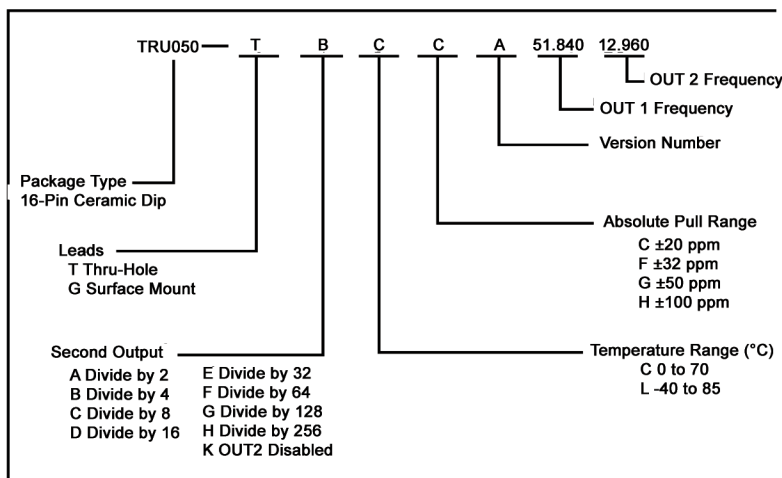
Standard frequencies* (MHz) Using OUT1						
12.032	12.288	12.624	13.824	16.000	16.128	16.384
16.777	16.896	17.920	18.432	18.936	20.000	20.480
22.1184	22.579	24.576	24.704	25.000	25.248	28.000
30.720	32.000	32.768	33.330	34.368	38.880	40.000
41.2416	41.943	44.736	47.457	49.152	49.408	50.000
51.840	65.536	19.440		40.960		

Standard frequencies* (MHz) Using OUT2						
1.000	1.024	1.544	2.048	3.088	3.240	4.032
4.096	4.1925	4.224	5.592	6.016	6.144	6.312
6.480	6.912	7.680	8.000	8.192	8.448	8.960
9.486	9.720	10.000	10.240	11.0592	12.352	12.500
12.960	14.000	16.000	16.384	16.665	19.440	20.000
20.6208	20.9715	22.368	23.7285	24.576	24.704	25.920
32.768						

*Other frequencies available upon request.

Table 4.