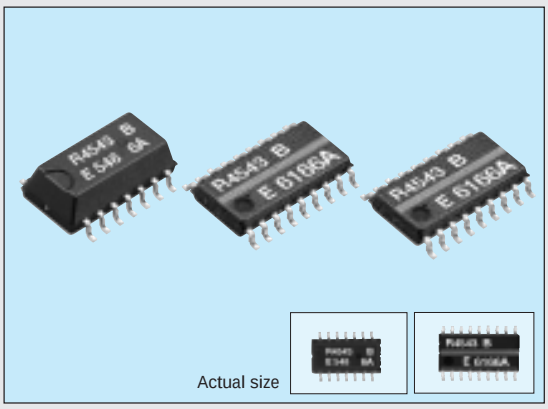
查询RTC4543供应商

SERIAL-INTERFACE REAL TIME CLOCK MODULE

RTC-4543SA/SB

- Builtin crystal unit allows adjustment-free efficient operation.
- Automatic leap year correction.
- Output selectable between 32.768 KHz/1 Hz.
- Operating voltage range: 2.5V to 5.5V.
- Supply voltage detection voltage: 1.7±0.3V.
- Low current consumption: 1.0 µA/2.0V (Max.)



Specifications (characteristics)

Absolute Max. rating

Item	Symbol	Condition	Min.	Max.	Unit
Power source voltage	V_{DD}	V_{DD}-GND	-0.3	7.0	V
Input voltage	V_{IN}	—		V_{DD}+0.3	
Output voltage	V_{OUT}				
Storage temperature	T_{STG}		-55	+125	˚C

Operating range

Item	Symbol	Condition	Min.	Max.	Unit
Operating voltage	V_{DD}	—	2.5	5.5	V
Date holding voltage	V_{CLK}		1.4		
Operating temperature	T_{OPR}		-40	+85	˚C

Frequency characteristics

Item	Symbol	Condition	Range	Unit
Frequency tolerance	Δf/fo	Ta=25˚C, V_{DD}=5V	5±23	ppm
Frequency temperature characteristics	T_{op}	-10 to +70˚C	+10/-120	
Frequency voltage characteristics	f_V	Ta=25˚C, V_{DD}=2.0 to 5.5V	±2	ppm/V
Oscillation start time	t_{OSC}	Ta=25˚C, V_{DD}=2.5V	3	s
Aging	fa	First year Ta=25˚C, V_{DD}=5V	±5	ppm/year

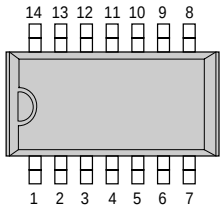
DC characteristics

(V_{DD}=5V±0.5V, Ta=-40 to 85˚C)

Item		Symbol	Condition		Min.	Typ.	Max.	Unit
"H" input voltage		V_{IH}	WR, DATA, CE, CLK, F_{OE},F_{SEL} pins		0.8V_{DD}	—	—	V
"L" input voltage		V_{IL}			—		0.2V_{DD}	
Input off-leak current		I_{OFF}	WR, CE, CLK, F_{OE},F_{SEL} pins				0.5	µA
"H" output voltage		V_{OH1}	V_{DD}=5.0V	I_{OH}=-1.0 mA	4.5	—	—	V
		V_{OH2}	V_{DD}=3.0V	DATA, F_{OUT} pins	2.5			
"L" output voltage		V_{OL1}	V_{DD}=5.0V	I_{OH}=1.0 mA	—		0.5	
		V_{OL2}	V_{DD}=3.0V	DATA, F_{OUT} pins			0.8	
Output leak current		I_{OZH}	V_{OUT}=5.5V	DATA, F_{OUT} pins	-1.0		1.0	µA
		I_{OZL}	V_{OUT}=0V					
Supply detection voltage		V_{DT}	—		1.4	1.7	2.0	V
Output load conditions		C_L	F_{OUT} pin		30 pF(max.)			
		N			2LS-TTL			
Current consumption	1	I_{DD1}	V_{DD}=5.0V	CE="L", F_{OE}="L" F_{SEL}="H"	—	1.5	3.0	µA
	2	I_{DD2}	V_{DD}=3.0V			1.0	2.0	
	3	I_{DD3}	V_{DD}=2.0V			0.5	1.0	
	4	I_{DD4}	V_{DD}=5.0V	CE="L", F_{OE}="H" F_{SEL}="L"		4.0	10.0	
	5	I_{DD5}	V_{DD}=3.0V			2.5	6.5	
	6	I_{DD6}	V_{DD}=2.0V	No load on the F_{OUT} pin		1.5	4.0	

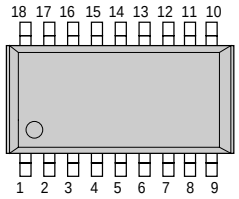
Terminal connection

● **RTC-4543SA**



No.	4543SA	4543SB
1	GND	N.C
2	N.C	N.C
3	CE	N.C
4	F_{SEL}	N.C
5	WR	F_{OE}
6	F_{OE}	WR
7	N.C	F_{SEL}
8	N.C	CE
9	V_{DD}	GND
10	CLK	F_{OUT}
11	DATA	DATA
12	N.C	CLK
13	N.C	N.C
14	F_{OUT}	V_{DD}
15	—	N.C
16	—	N.C
17	—	N.C
18	—	N.C

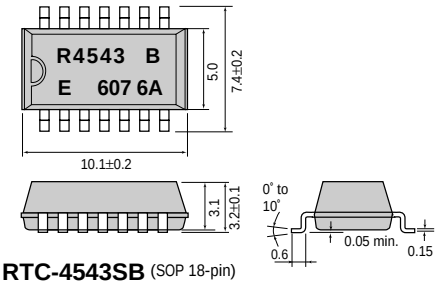
● **RTC-4543SB**



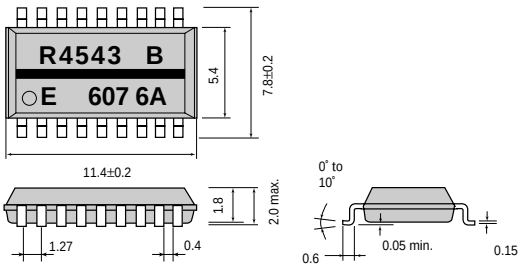
External dimensions

(Unit: mm)

● **RTC-4543SA** (SOP 14-pin)



● **RTC-4543SB** (SOP 18-pin)



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Register table

	MSB							
Seconds (0 to 59)	FDT	s 40	s 20	s 10	s 8	s 4	s 2	s 1
Minutes (0 to 59)	*	mi 40	mi 20	mi 10	mi 8	mi 4	mi 2	mi 1
Hour (0 to 23)	*	*	h 20	h 10	h 8	h 4	h 2	h 1
Day of the week (1 to 7)					*	w 4	w 2	w 1
Day (1 to 31)	*	*	d 20	d 10	d 8	d 4	d 2	d 1
Month (1 to 12)	TM	*	*	mo 10	mo 8	mo 4	mo 2	mo 1
year (0 to 99)	y 80	y 40	y 20	y 10	y 8	y 4	y 2	y 1

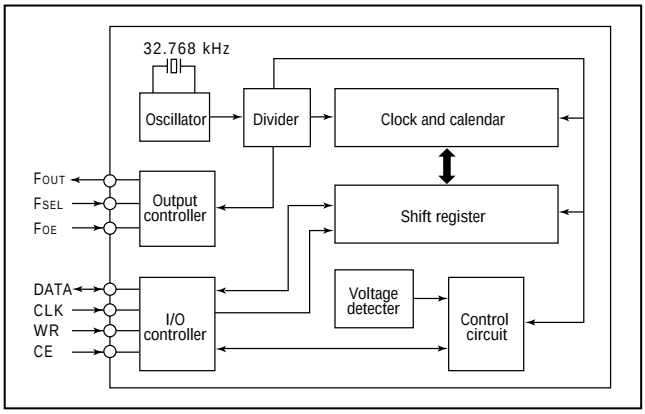
FDT bit: Supply voltage detection bit. TM bit: Test bit always set this bit to "0".

Switching characteristics

(Ta=-40 to +85°C, CL=30 pF)

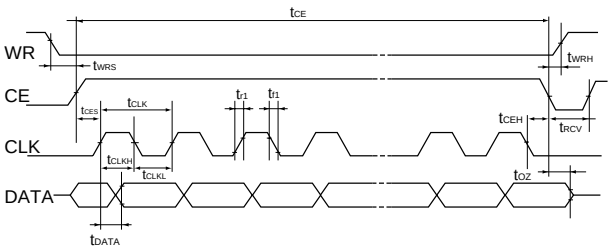
Item		Symbol	VDD= 5V± 10%		VDD= 3V± 10%		Unit
			Min.	Max.	Min.	Max.	
CLK clock cycle		t CLK	0.75	7800	1.5	7800	µs
CLK high pulse width		t CLKH	0.375	3900	0.75	3900	
CLK low pulse width		t CLKL					
CE setup time		t CES					
CE hold time		t CEH		—		—	
CE enable time		t CE	—	0.9	—	0.9	s
Write data setup time		t SD	0.1	—	0.2	—	µs
Write data hold time		t HD			0.1		
WR setup time		t WRS	100		100		ns
WR hold time		t WRH					
DATA output delay time		t DATA	—	0.2	—	0.4	µs
DATA output floating time		t DZ		0.1		0.2	
Clock input rise time		t r1		50		100	ns
Clock input fall time		t f1					
FOUT rise time	CL= 30pF	t r2		100		200	
FOUT fall time		t f2					
Disable time		t XZ					
Enable time		t ZX					
FOUT duty ratio		Duty	40	60	40	60	%
Wait time		t rcv	0.95	—	1.9	—	µs

Block diagram

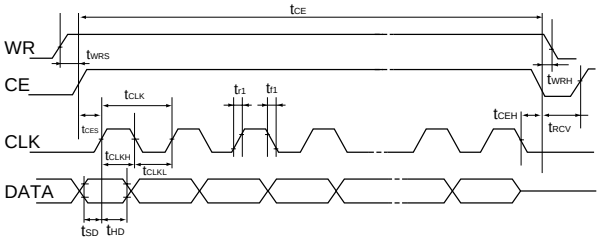


Timing chart

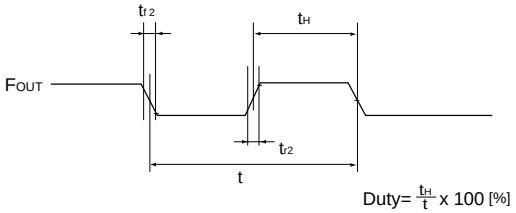
Data read



Data write

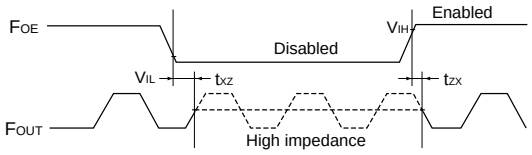


FOUT



Duty= $\frac{t_H}{t}$ x 100 [%]

Disabled and Enabled



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