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INT201

High-side Driver IC

Floating Inputs
Floating High-side Drive

Product Highlights

Floating Control Inputs
- Connects directly to INT200 or INT202 HSD outputs
- No external level translators or transformers required

Gate Drive Output for an External MOSFET
- Provides 300 mA sink/150 mA source current
- Can drive MOSFET gate at up to 15 V
- Floating source for driving high-side N-channel MOSFET
- External MOSFET allows flexibility in design for various motor sizes

Built-in Protection Circuits
- Logic inputs include noise rejection circuitry
- Undervoltage lockout

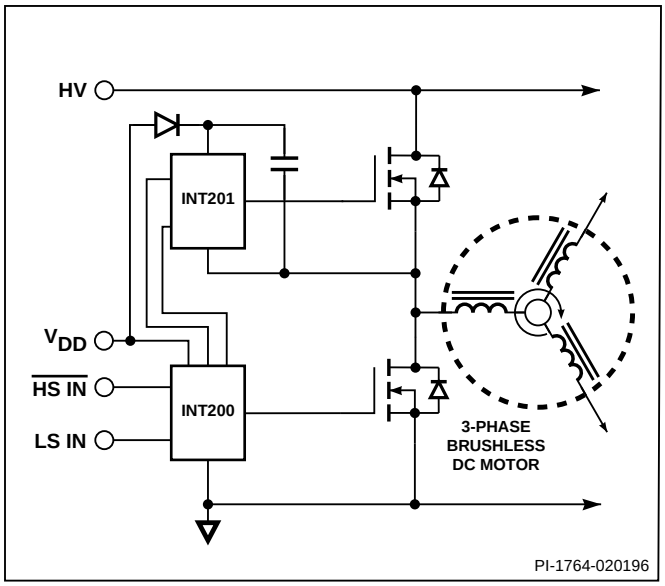

Figure 1. Typical Application.

Description

The INT201 high-side driver IC provides gate drive for an external high-side MOSFET switch. When used in conjunction with the INT200 or INT202 low-side drivers, the INT201 provides a simple, cost-effective interface between low-voltage control logic and high-voltage loads.

Built-in noise rejection circuitry shared between the INT201 and the INT200 or INT202 provides reliable operation in the harshest industrial environments. The INT201 is powered from a ground-referenced low-voltage supply. A floating supply is derived from this rail by using a simple bootstrap technique to provide adequate gate drive for the external N-channel MOSFET.

Applications include motor drives, electronic ballasts, and uninterruptible power supplies. The INT201 can also be used to implement full-bridge and multi-phase configurations.

The INT201 is available in 8-pin plastic DIP and SOIC packages.

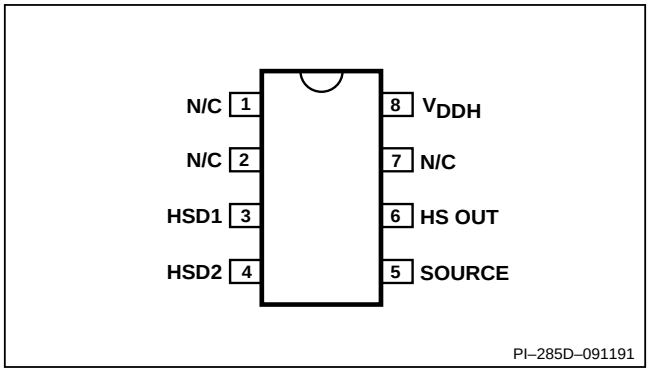

Figure 2. Pin Configuration.

ORDERING INFORMATION		
PART NUMBER	**PACKAGE OUTLINE**	**TEMP RANGE**
INT201PFI	P08A	-40 to 85°C
INT201TFI	T08A	-40 to 85°C

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Pin Functional Description

Pin 1:
No connection.

Pin 2:
No connection.

Pin 3:
Level shift input **HSD 1** works in conjunction with HSD 2 to provide interface from the low side control logic and to give noise immunity.

Pin 4:
Level shift input **HSD 2** works in conjunction with HSD 1 to provide interface from the low side control logic and to give noise immunity.

Pin 5:
SOURCE connection. Analog reference point for the circuit, normally connected to the source of the high side MOSFET.

Pin 6:
HS OUT is the output of the MOSFET driver for the high side.

Pin 7:
No connection.

Pin 8:
$\mathbf{V_{DDH}}$ supplies power to the control logic and output driver.

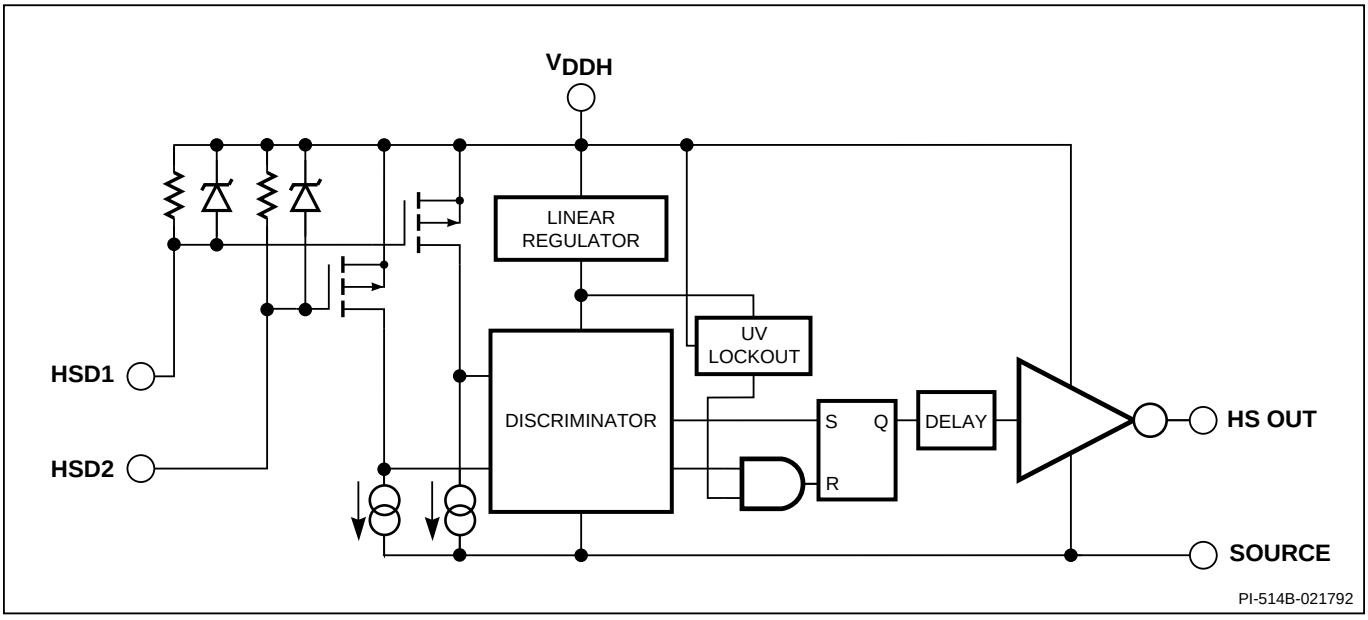

Figure 3. Functional Block Diagram of the INT201.

INT201 Functional Description

5 V Regulator
The 5 V linear regulator circuit provides the supply voltage for the noise rejection circuitry and control logic. This allows the logic section and the driver circuitry to be directly compatible with 5 V CMOS logic without the need of an external 5 V supply.

Undervoltage Lockout
The undervoltage lockout circuit disables the HS OUT pin whenever the V_{DDH} power supply falls below 9.0 V, and maintains this condition until the V_{DDH} power supply rises above 9.35 V. This guarantees that the high side MOSFET will be off during power-up or fault conditions.

Noise Immunization Circuit
This circuit provides noise immunity by combining a sampling circuit with a flip-flop to turn on and off the driver only when required to and not when there is noise on the HSD inputs.

Driver
The CMOS driver circuit provides drive power to the gate of the MOSFET used on the high side of the half bridge circuit. The driver consists of a CMOS buffer capable of driving external transistors at up to 15 V. The SOURCE pin is connected to the source of the external MOSFET to establish a reference for the gate voltage.

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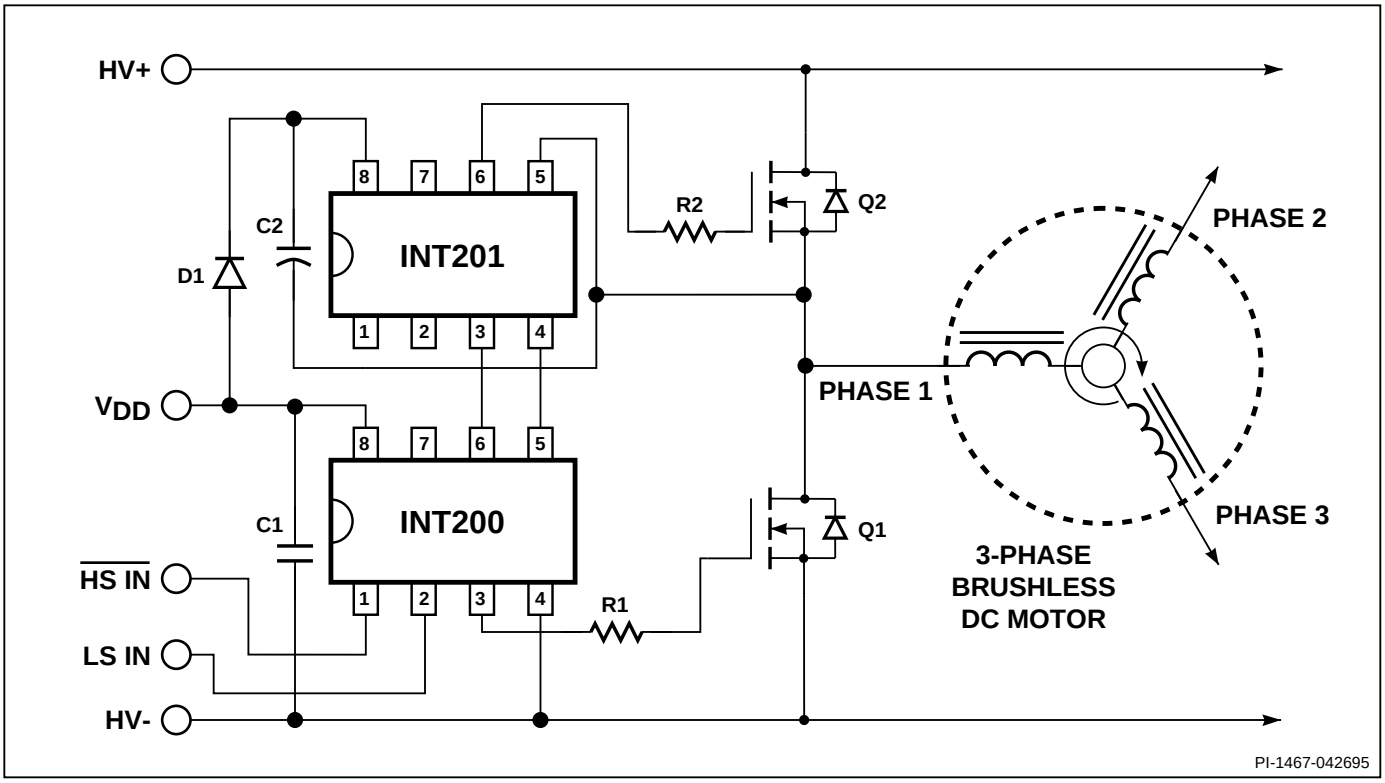

Figure 4. Using the INT200 and INT201 in a 3-phase Configuration.

General Circuit Operation

One phase of a three-phase brushless DC motor drive circuit is shown in Figure 4 to illustrate an application of the INT200/201. The LS IN signal directly controls MOSFET Q1. The $\overline{\text{HS IN}}$ signal causes the INT200 to command the INT201 to turn MOSFET Q2 on or off as required. The INT200 will ignore input signals that would command both Q1 and Q2 to conduct simultaneously, protecting against shorting the HV+ bus to HV-.

Local bypassing for the low-side driver is provided by C1. Bootstrap bias for the high-side driver is provided by D1 and C2. Slew rate and effects of parasitic oscillations in the load waveforms are controlled by resistors R1 and R2.

The inputs are designed to be compatible with 5 V CMOS logic levels and should not be connected to V_{DD}. Normal CMOS power supply sequencing should be observed. The order of signal application should be V_{DD}, logic signals, and then HV+.

The INT201 is latched on and off by the edges of the appropriate low-side logic signal ($\overline{\text{HS IN}}$ for the INT200 and HS IN for the INT202). The high-side driver will latch off and stay off if the bootstrap capacitor discharges below the undervoltage lockout threshold. Undervoltage lockout-induced turn off can occur during conditions such as power ramp up, motor start, or low speed operation.

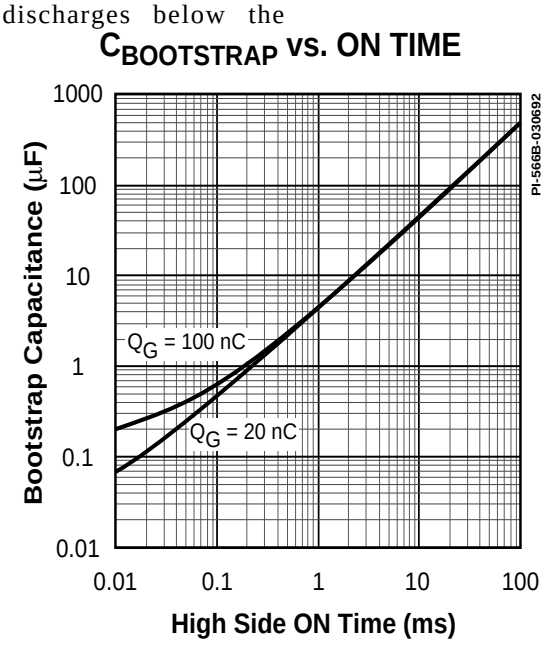

Figure 5. High-side On Time versus Bootstrap Capacitor.

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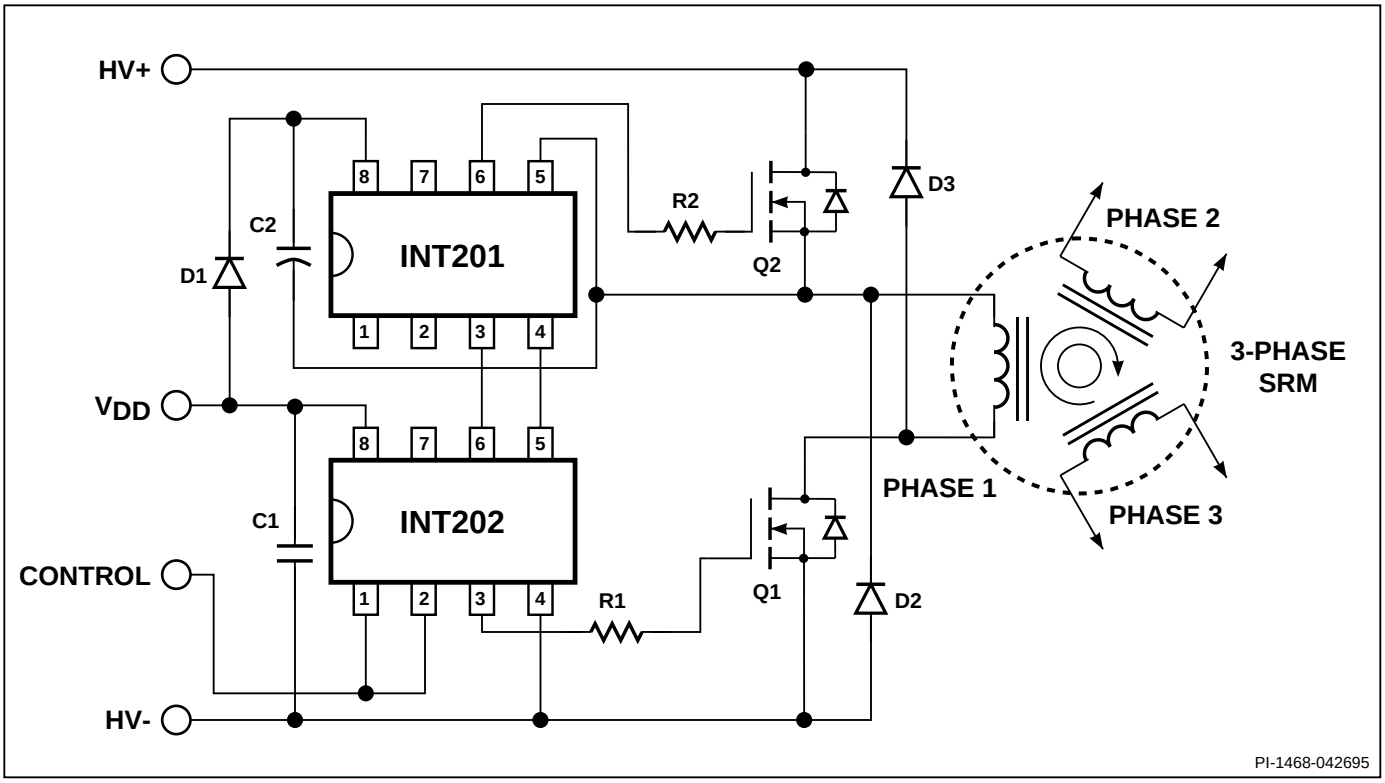

Figure 6. Using the INT202 and INT201 to Drive a Switched Reluctance Motor.

General Circuit Operation (cont.)

The bootstrap capacitor must be large enough to provide bias current over the entire on time interval of the high-side driver without significant voltage sag or decay. The MOSFET gate charge must also be supplied at the desired switching frequency. Figure 5 shows the maximum high-side on time versus gate charge of the external MOSFET. Applications with extremely long high-side on times require special techniques discussed in AN-10.

A three-phase switched reluctance motor example using the INT202/201 is given in Figure 6. The LS IN signal directly controls MOSFET Q1. Unlike the INT200, the INT202 allows both the low and high-side drivers to be on at the same time, as this is required in applications where the load is placed between the low and high-side output MOSFETs.

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ABSOLUTE MAXIMUM RATINGS[1]

V_{DDH} Voltage ..... 16.5 V
Logic Input Voltage ..... -0.3 V to 5.5 V
HS OUT Voltage ..... -0.3 V to V_{DDH} + 0.3 V
Storage Temperature ..... –65 to 125°C
Ambient Temperature ..... -40 to 85°C
Junction Temperature. ..... 150°C
Lead Temperature[(2)]. ..... 260°C

Power Dissipation
PF Suffix (T_A = 25˚C) ..... 1.25 W
PF Suffix (T_A = 70˚C) ..... 800 mW
TF Suffix (T_A = 25˚C) ..... 1.04 W
TF Suffix (T_A = 70˚C) ..... 667 mW
Thermal Impedance (θ_{JA})
PF Suffix ..... 100°C/W
TF Suffix ..... 120°C/W

1. Unless noted, all voltages referenced to SOURCE, T_A = 25˚C
2. 1/16" from case for 5 seconds.

Parameter	Symbol	Conditions (Unless Otherwise Specified) V_{DDH}= 15 V, SOURCE = 0V T_A = -40 to 85°C		Min	Typ	Max	Units
HSD INPUTS							
Input Current Threshold	I_{HSD1}, I_{HSD2}				-5	-2.5	mA
HS OUT							
Output Voltage, High	V_{OH}	I_o= -20 mA		V_{DDH}-1.0	V_{DDH}-0.5		V
Output Voltage, Low	V_{OL}	I_o= 40 mA			0.3	1.0	V
Output Short Circuit Current	I_{OS}	See Note 1	V_O= 0 V			-150	mA
			V_O= V_{DDH}	300			
Turn-on Delay Time	$t_{d(on)}$	See Figure 7			1.0	1.5	µs
Rise Time	t_r	See Figure 7			80	120	ns
Turn-off Delay Time	$t_{d(off)}$	See Figure 7			420	600	ns
Fall Time	t_f	See Figure 7			50	100	ns

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Parameter	Symbol	Conditions (Unless Otherwise Specified) V_{DDH}= 15 V, SOURCE = 0V T_A = -40 to 85°C	Min	Typ	Max	Units
SYSTEM RESPONSE						
Deadtime (Low Off to High On)	Dt_{P+}	See Figure 8	0	450		ns
Deadtime (Low On to High Off)	Dt_{P-}	See Figure 8	0	300		ns
Matching (Low On to High On)	Mt_{P+}	See Figure 9		0.3	1.0	µs
Matching (Low Off to High Off)	Mt_{P-}	See Figure 9		0.3	1.0	µs
UNDERVOLTAGE LOCKOUT						
Input UV Threshold Voltage	$V_{DDH(UV)}$		8.5	9.0	10	V
Input UV Hysteresis			175	350		mV
SUPPLY						
Supply Current	I_{DDH}			1.5	3.0	mA
Supply Voltage	V_{DDH}		10		16	V

NOTES:

1. Applying a short circuit to the HS OUT pin for more than 500 µs will exceed the thermal rating of the package, resulting in destruction of the part.

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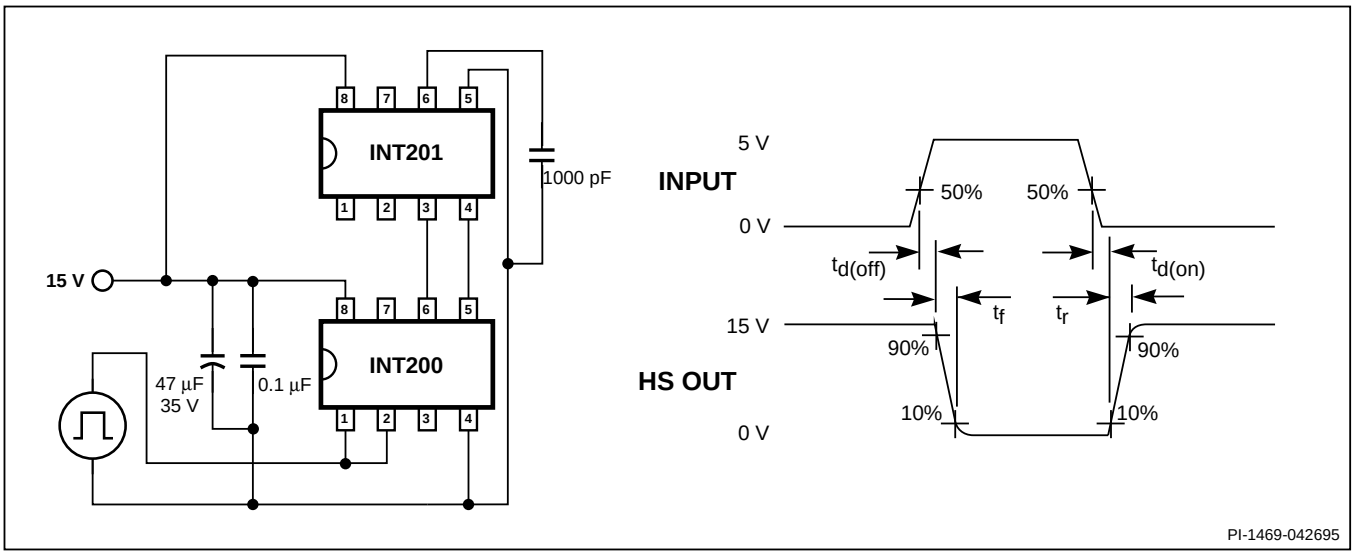

Figure 7. Switching Time Test Circuit.

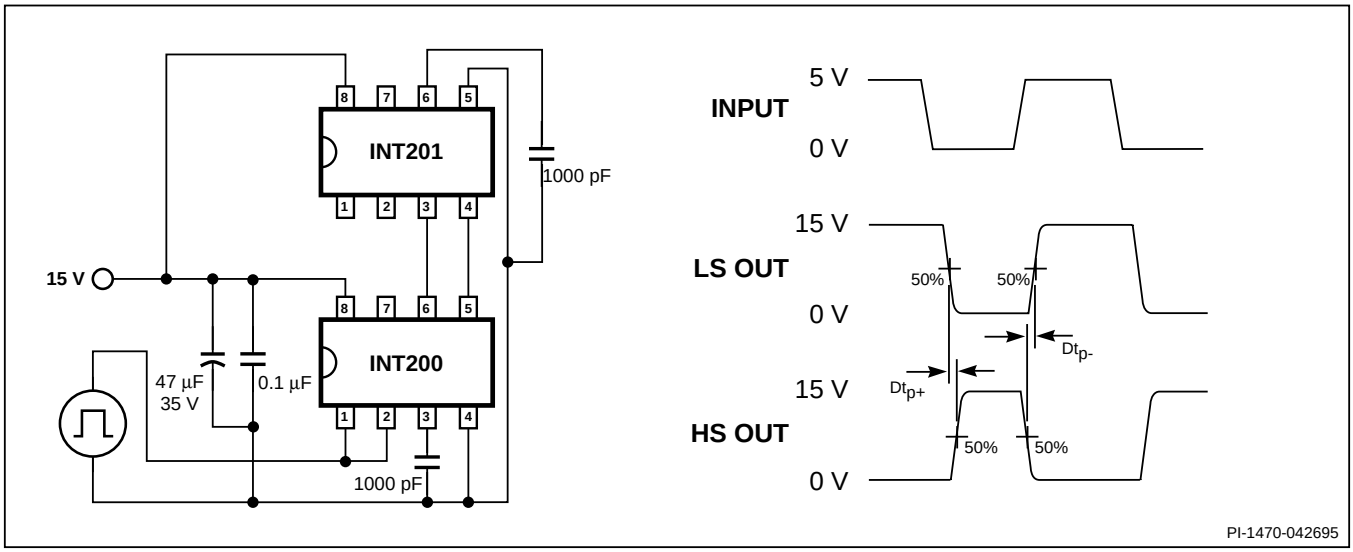

Figure 8. Dead Time Test Circuit.

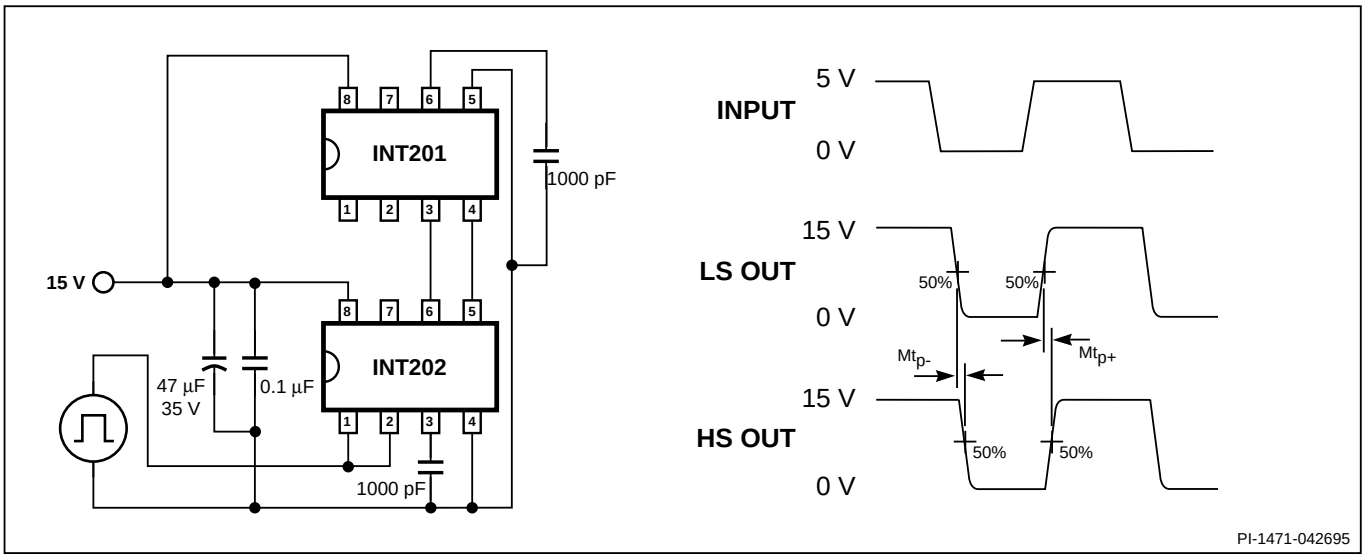

Figure 9. Matching Test Circuit.

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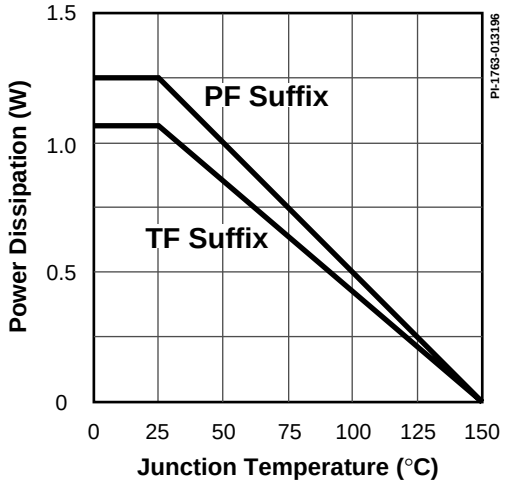
PACKAGE POWER DERATING



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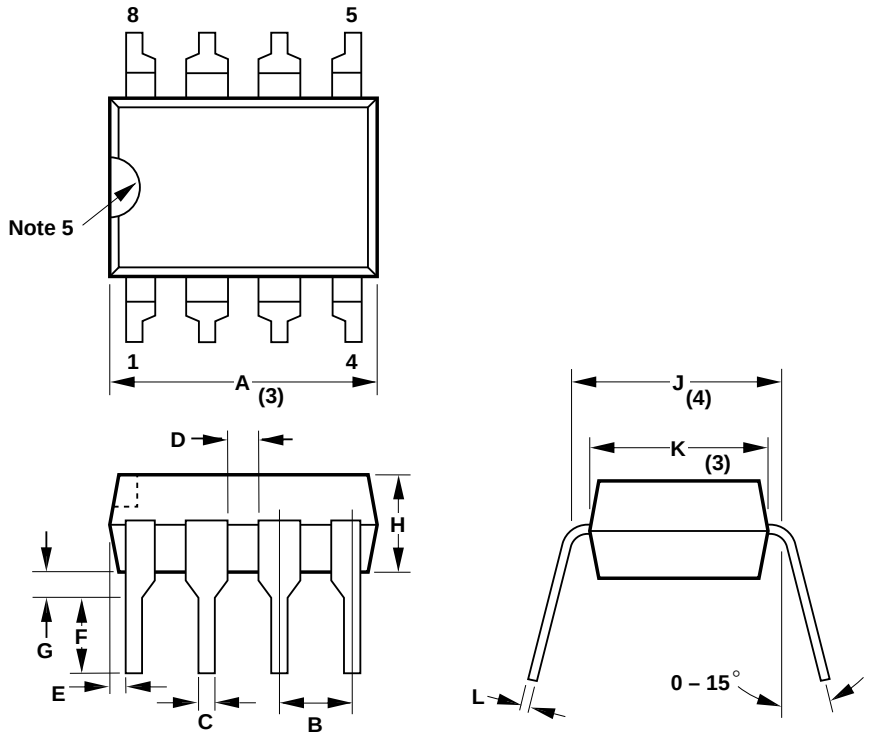
P08A — Plastic DIP-8

Dim.	inches	mm
A	.395 MAX	10.03 MAX
B	.090-.110	2.29-2.79
C	.015-.021	0.38-0.53
D	.040 TYP	1.02 TYP
E	.015-.030	0.38-0.76
F	.125 MIN	3.18 MIN
G	.015 MIN	0.38 MIN
H	.125-.135	3.18-3.43
J	.300-.320	7.62-8.13
K	.245-.255	6.22-6.48
L	.009-.015	0.23-0.38

Notes:
1. Package dimensions conform to JEDEC specification MS-001-AB for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 8 leads (issue B, 7/85).
2. Controlling dimensions: inches.
3. Dimensions are for the molded body and do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .010 inch (.25 mm) on any side.
4. These dimensions measured with the leads constrained to be perpendicular to package bottom.
5. Pin 1 orientation identified by end notch or dot adjacent to Pin 1.

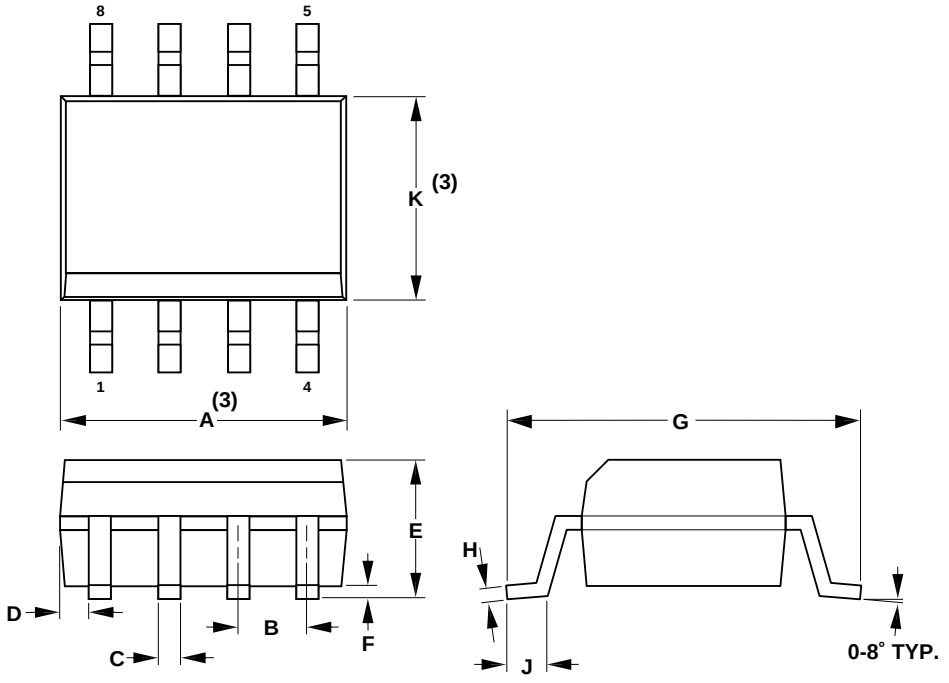


PI-1842-050196

T08A — Plastic SO-8

DIM	inches	mm
A	0.189-0.197	4.80-5.00
B	0.050 TYP	1.27 TYP
C	0.014-0.019	0.35-0.49
D	0.012 TYP	0.31 TYP
E	0.053-0.069	1.35-1.75
F	0.004-0.010	0.10-0.25
G	0.228-0.244	5.80-6.20
H	0.007-0.010	0.19-0.25
J	0.021-0.045	0.51-1.14
K	0.150-0.157	3.80-4.00

Notes:
1. Package dimensions conform to JEDEC specification MS-012-AA for standard small outline (SO) package, 8 leads, 3.75 mm (.150 inch) body width (issue A, June 1985).
2. Controlling dimensions are in mm.
3. Dimensions are for the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15 mm (.006 inch) on any side.
4. Pin 1 side identified edge by chamfer on top of the package body or indent on Pin 1 end.



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